utomation Portal	Totally Integrated

Analog Input / Analog Input MNS [CPU 1214C DC/DC/DC]

S7-1200 station_1

Analog Input MNS General\Project inforn	nation				
lame	Analog Input MNS	Author	Andi Sama	Comment	Early Explorations
lot	1	Rack	0		
General\Catalog information	Mation CPU 1214C DC/DC/DC	Description	Work memory 100 KB; 24VDC power supply with DI14 x 24VDC SINK/SOURCE, DQ10 x 24VDC and AI2 on board; 6 high-speed counters and 4 pulse outputs on-board; signal board expands on-board I/O; up to 3 communication modules for serial communication; up to 8 signal modules for I/O expansion; PROFINET IO controller, I-device, transport protocol TCP/IP, secure Open User Communication, S7 communication, Web server, OPC UA: Server DA	Article number	6ES7 214-1AG40-0XB0
ieneral\Identification	& Maintenance				
lant designation	Lab	Location identifier	01	Installation date	2022-12-10 19:22:00.529
Additional informa- ion					
ieneral\Checksums					
ext lists	FA 70 E8 75 1D 5A 8E 29	Software	53 50 AD D8 74 13 D0 0B		
ROFINET interface [X	, -		F1. 10 1	-	
lame PROFINET interface [Y	PROFINET interface_1 (1]\General\Project information	Author	ThinkPad	Comment	
lame	DI 14/DQ 10_1	Comment		Name	AI 2_1
Comment PROFINET interface [X	[[1]\Ethernet addresses\Interface netw	orked with			
Subnet:	Not connected				
_	1]\Ethernet addresses\Internet proto				
P configuration	Set IP address in the project	IP address:	192.168.0.1	Subnet mask:	255.255.255.0
Jse router	False (1]\Ethernet addresses\PROFINET				
'ROFINET Interface (X PROFINET device	False	Generate PROFINET	True	PROFINET device	analog input mns
name is set directly at the device		device name auto- matically		name:	Liver of miles
Converted name:	analogxainputxamnsd564	Device number:	0		
	(1]\Time synchronization Enable time synchronization via NTP		IP addresses	Server 1	0.0.0.0
ization via NTP serv-			444.65565		3.3.0.0
Server 2	0.0.0.0	Server 3	0.0.0.0	Server 4	0.0.0.0
Jpdate interval	10sec			CPU synchronizes the modules of the device.	No synchronization
	(1]\Digital inputs\Channel0				
Channel address	10.0	Input filters	6.4 millisec	Enable pulse catch	0
'ROFINET interface [X Enable rising edge	(1]\Digital inputs\Channel0\	Prefix Event Rising	49152	Event name:	0
letection		Edge	49132	Event name.	U
lardware interrupt:	I .	Rising edge0	Rising edge0		
	(1]\Digital inputs\Channel0\	D C = := :::	40000	-	
letection	0	Prefix Event Falling Edge	49280	Event name:	0
lardware interrupt:		Falling edge0	Falling edge0		
'ROFINET interface [X Channel address	(1]\Digital inputs\Channel1	Input filters	6.4 millisec	Enable pulse catch	0
-	(1]\Digital inputs\Channel1\	pac inters			,
Enable rising edge detection	0	Prefix Event Rising Edge	49153	Event name:	0
lardware interrupt:		Rising edge1	Rising edge1		!
	(1]\Digital inputs\Channel1\				
Enable falling edge letection	0	Prefix Event Falling Edge	49281	Event name:	0
Hardware interrupt:	0	Falling edge1	Falling edge1		
ROFINET interface [X	[1]\Digital inputs\Channel2				
Channel address	10.2	Input filters	6.4 millisec	Enable pulse catch	0
nable rising edge	(1]\Digital inputs\Channel2\ 0	Prefix Event Rising	49154	Event name:	0
etection lardware interrupt:	0	Edge Rising edge2	Rising edge2		
	(1]\Digital inputs\Channel2\				
	0	Prefix Event Falling Edge	49282	Event name:	0
letection lardware interrupt:	0	Falling edge2	Falling edge2		
	(1]\Digital inputs\Channel3	,			
Channel address PROFINET interface [X	10.3 (1]\Digital inputs\Channel3\	Input filters	6.4 millisec	Enable pulse catch	0
		Prefix Event Rising	49155	Event name:	0
nable rising edge					
		Edge Rising edge3	Rising edge3		

Totally Integrated					
Automation Portal					
PROFINET interface [X1]\Digita Enable falling edge detection	il inputs\Channel3\	Prefix Event Falling Edge	49283	Event name:	0
Hardware interrupt: 0	al innute/Channel/	Falling edge3	Falling edge3		
PROFINET interface [X1]\Digita Channel address 10.4	·	Input filters	6.4 millisec	Enable pulse catch	0
PROFINET interface [X1]\Digita Enable rising edge 0	al inputs\Channel4\	Prefix Event Rising	49156	Event name:	0
detection		Edge		Event name:	U
Hardware interrupt: 0 PROFINET interface [X1]\Digita	al innuts\Channel4\	Rising edge4	Rising edge4		
Enable falling edge 0	in inputs (chainle) i	Prefix Event Falling	49284	Event name:	0
detection Hardware interrupt: 0		Edge Falling edge4	Falling edge4		
PROFINET interface [X1]\Digita	al inputs\Channel5			English make a state	lo.
Channel address 10.5 PROFINET interface [X1]\Digita	al inputs\Channel5\	Input filters	6.4 millisec	Enable pulse catch	0
Enable rising edge 0 detection		Prefix Event Rising Edge	49157	Event name:	0
Hardware interrupt: 0		Rising edge5	Rising edge5		
PROFINET interface [X1]\Digita Enable falling edge 0	al inputs\Channel5\	Prefix Event Falling	49285	Event name:	0
detection		Edge		Event name:	V
Hardware interrupt: 0 PROFINET interface [X1]\Digita	al inputs\Channel6	Falling edge5	Falling edge5		
Channel address 10.6		Input filters	6.4 millisec	Enable pulse catch	0
PROFINET interface [X1]\Digita Enable rising edge 0	al inputs\Channel6\	Prefix Event Rising	49158	Event name:	0
detection		Edge			-
Hardware interrupt: 0 PROFINET interface [X1]\Digita	al inputs\Channel6\	Rising edge6	Rising edge6		
Enable falling edge 0		Prefix Event Falling	49286	Event name:	0
detection Hardware interrupt: 0		Edge Falling edge6	Falling edge6		
PROFINET interface [X1]\Digita	al inputs\Channel7				
Channel address 10.7 PROFINET interface [X1]\Digita	al inputs\Channel7\	Input filters	6.4 millisec	Enable pulse catch	0
Enable rising edge 0 detection		Prefix Event Rising Edge	49159	Event name:	0
Hardware interrupt: 0		Rising edge7	Rising edge7		
PROFINET interface [X1]\Digita Enable falling edge 0	al inputs\Channel7\	Prefix Event Falling	49287	Event name:	0
detection		Edge		Event name:	U
Hardware interrupt: 0 PROFINET interface [X1]\Digita	al inputs\Channel8	Falling edge7	Falling edge7		
Channel address 11.0	·	Input filters	6.4 millisec	Enable pulse catch	0
PROFINET interface [X1]\Digita Enable rising edge 0	al inputs\Channel8\	Prefix Event Rising	49160	Event name:	0
detection		Edge			
Hardware interrupt: 0 PROFINET interface [X1]\Digita	al inputs\Channel8\	Rising edge8	Rising edge8		
Enable falling edge 0 detection		Prefix Event Falling Edge	49288	Event name:	0
Hardware interrupt: 0		Falling edge8	Falling edge8		
PROFINET interface [X1]\Digita Channel address 11.1	al inputs\Channel9	Input filters	6.4 millisec	Enable pulse catch	0
PROFINET interface [X1]\Digita	al inputs\Channel9\	input inters	0.4 IIIIIIsec	Lilable puise catch	U
		Prefix Event Rising			
			49161	Event name:	0
detection Hardware interrupt: 0		Edge Rising edge9	49161 Rising edge9	Event name:	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita	ıl inputs\Channel9\	Edge Rising edge9	Rising edge9		
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge 0 detection	ıl inputs\Channel9\	Edge Rising edge9 Prefix Event Falling Edge	Rising edge9	Event name:	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0		Edge Rising edge9 Prefix Event Falling	Rising edge9		
detection Hardware interrupt: 0 PROFINET interface [X1]\Digitate Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitate Channel address 11.2	ıl inputs\Channel10	Edge Rising edge9 Prefix Event Falling Edge	Rising edge9		
detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Digital Digi	ıl inputs\Channel10	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters	Rising edge9 49289 Falling edge9	Event name:	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge 0 detection	ıl inputs\Channel10	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge	Rising edge9 49289 Falling edge9 6.4 millisec 49162	Event name: Enable pulse catch	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0	al inputs\Channel10 al inputs\Channel10\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising	Rising edge9 49289 Falling edge9 6.4 millisec	Event name: Enable pulse catch	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable falling edge detection	al inputs\Channel10 al inputs\Channel10\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling	Rising edge9 49289 Falling edge9 6.4 millisec 49162	Event name: Enable pulse catch	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Digital Digi	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10	Event name: Enable pulse catch Event name:	0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10	Event name: Enable pulse catch Event name: Event name:	0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.3	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290	Event name: Enable pulse catch Event name:	0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digital Enable rising edge 0	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Falling Edge Falling edge10	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10	Event name: Enable pulse catch Event name: Event name:	0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.3 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 Hardware interrupt: 0	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec	Event name: Enable pulse catch Event name: Event name:	0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 1.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 1.3 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Falling Edge Falling edge10 Input filters	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec 49163 Rising edge11	Event name: Enable pulse catch Event name: Event name: Enable pulse catch Event name:	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.3 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Rising Edge Falling edge10 Input filters Prefix Event Rising Edge Rising edge11 Prefix Event Falling Edge Rising edge11	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec 49163 Rising edge11 49291	Event name: Enable pulse catch Event name: Event name:	0 0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11 al inputs\Channel11	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Rising Edge Falling edge10 Input filters Prefix Event Rising Edge Rising edge11 Prefix Event Falling	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec 49163 Rising edge11	Event name: Enable pulse catch Event name: Event name: Enable pulse catch Event name:	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Channel address 11.2 PROFINET interface [X1]\Digitation Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Channel address 11.3 PROFINET interface [X1]\Digitation Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation Channel address 11.4	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11 al inputs\Channel11\ al inputs\Channel11\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Rising Edge Falling edge10 Input filters Prefix Event Rising Edge Rising edge11 Prefix Event Falling Edge Rising edge11	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec 49163 Rising edge11 49291	Event name: Enable pulse catch Event name: Event name: Enable pulse catch Event name:	0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.2 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable rising edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Enable falling edge detection Hardware interrupt: 0 PROFINET interface [X1]\Digita Channel address 11.4 PROFINET interface [X1]\Digita	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11 al inputs\Channel11\ al inputs\Channel11\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Rising Edge Falling edge10 Input filters Prefix Event Rising Edge Rising edge11 Prefix Event Falling Edge Falling edge11 Input filters	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec 49163 Rising edge11 49291 Falling edge11 6.4 millisec	Event name: Enable pulse catch Event name: Event name: Enable pulse catch Event name: Event name:	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
detection Hardware interrupt: 0 PROFINET interface [X1]\Digitation	al inputs\Channel10 al inputs\Channel10\ al inputs\Channel10\ al inputs\Channel11 al inputs\Channel11\ al inputs\Channel11\	Edge Rising edge9 Prefix Event Falling Edge Falling edge9 Input filters Prefix Event Rising Edge Rising edge10 Prefix Event Falling Edge Falling edge10 Input filters Prefix Event Rising Edge Falling edge11 Prefix Event Falling Edge Rising edge11	Rising edge9 49289 Falling edge9 6.4 millisec 49162 Rising edge10 49290 Falling edge10 6.4 millisec 49163 Rising edge11 49291 Falling edge11	Event name: Enable pulse catch Event name: Event name: Enable pulse catch Event name:	0 0 0 0 0

Totally Integrated Automation Portal					
	K1]\Analog inputs\Noise reduction				
Integration time	50 Hz (20 ms) K1]\Analog inputs\Channel0				
Channel address Smoothing	IW64 Weak (4 cycles)	Measurement type	Voltage	Voltage range Enable overflow diag-	010 V
	K1]\Analog inputs\Channel1			nostics	•
Channel address	IW66	Measurement type	Voltage		010 V
Smoothing	Weak (4 cycles)			Enable overflow diag- nostics	1
PROFINET interface [> Reaction to CPU STOP	Use substitute value				
PROFINET interface [> Channel address	K1]\Digital outputs\Channel0 Q0.0	Substitute a value of	0		
		1 on a change from RUN to STOP.			
PROFINET interface [) Channel address	K1]\Digital outputs\Channel1	Substitute a value of	0		
		1 on a change from RUN to STOP.			
PROFINET interface [> Channel address	K1]\Digital outputs\Channel2	Substitute a value of	0		
Liannei address	Q0.2	1 on a change from RUN to STOP.	U		
	(1]\Digital outputs\Channel3				
Channel address	Q0.3	Substitute a value of 1 on a change from	0		
PROFINET interface [>	 K1]\Digital outputs\Channel4	RUN to STOP.			
Channel address	Q0.4	Substitute a value of 1 on a change from	0		
PROFINET interface [)	 K1]\Digital outputs\Channel5	RUN to STOP.			
Channel address	Q0.5	Substitute a value of 1 on a change from	0		
PPOEINET interface [)	K1]\Digital outputs\Channel6	RUN to STOP.			
Channel address	Q0.6	Substitute a value of	0		
		1 on a change from RUN to STOP.			
PROFINET interface [) Channel address	K1]\Digital outputs\Channel7 Q0.7	Substitute a value of	0		
		1 on a change from RUN to STOP.			
PROFINET interface [) Channel address	K1]\Digital outputs\Channel8 Q1.0	Substitute a value of	0		
	,	1 on a change from RUN to STOP.			
PROFINET interface [> Channel address	K1]\Digital outputs\Channel9	Substitute a value of	0		
enamier daaress	~ · · ·	1 on a change from RUN to STOP.			
PROFINET interface [) IO controller	K1]\Operating mode True			Device number	0
O device	False	IO system		Device number	U
PROFINET interface [> Start address	(1]\I/O addresses\Input addresses 0.0	End address	1.7	Organization block	0
Process image PROFINET interface ()	0 K1]\I/O addresses\Input addresses				
Start address Process image	64	End address	67	Organization block	0
PROFINET interface [>	(1]\I/O addresses\Output addresses	11-	Ta =		
Start address Process image	0.0	End address	1.7	Organization block	0
PROFINET interface [) Support device re-	K1]\Advanced options\Interface option	ns Permit overwriting of	False	Use IEC V2.2 LLDP	False
placement without exchangeable medi-		device names of all assigned IO devices		mode	
um Keep-Alive connec-	30s				
tion monitoring:	 K1]\Advanced options\Real time settir	ngs\IO communication			
Send clock:	1.000ms K1]\Advanced options\Real time settir				
Calculated bandwidth for cyclic IO data:		Calculated bandwidth for cyclic IO data:	0.000%		
PROFINET interface [>	K1]\Advanced options\Port [X1 P1]\Ge	neral	TI: 10 1		
	Port_1 K1]\Advanced options\Port [X1 P1]\Po		·	Comment	
_ocal port:	Analog Input MNS\PROFINET interface_1 [X1]\Port_1 [X1 P1]	Medium:	Copper	Cable name:	
			231,		

Totally Integrated Automation Portal					
OFINITT:+	411.4 d d	+ :+			
OFINET INTERTACE (X	1]\Advanced options\Port [X1 P1]\Por Monitoring of partner port is not pos-	Partner port:	Any partner		
	sible	•	71		
OFINET interface [X tivate this port for	1]\Advanced options\Port [X1 P1]\Por	t options\Activate			
e .					
	(1]\Advanced options\Port [X1 P1]\Por		E L	Frall control water	\ _ .
ansmission rate / ıplex:	Automatic	Monitor	False	Enable autonegotia- tion	True
OFINET interface [X	1]\Advanced options\Port [X1 P1]\Por				
d of detection of cessible devices	False	End of topology dis- covery	False	End of the sync do- main	False
	[1]\Web server access	covery		mani	
nable Web server for e IP address of this	False	The Web server must also be activated in			
terface		the properties of the PLC.			
	HSC)\HSC1\General\Enable				
,	0	Enable this high	0	Enable this high	0
eed counter able this high	0	speed counter Enable this high	0	speed counter Enable this high	0
eed counter		speed counter		speed counter	
	HSC)\HSC1\General\Project information			Name	LISC 2
ame omment	HSC_1	Comment Name	HSC_3	Name Comment	HSC_2
	HSC_4	Comment		Name	HSC_5
mment		Name	HSC_6	Comment	
	HSC)\HSC1\I/O addresses\Input addres		1002.7	Ctout adduce -	1004.0
art address Id address	1000.0	End address Organization block	0	Start address Start address	1004.0
	1011.7	Organization block	0	Process image	0
art address	1012.0	End address	1015.7	Organization block	0
	0	Start address	1016.0	End address	1019.7
<u> </u>	0	Process image	0	Start address	1020.0
	1023.7 0	Organization block Process image	0	Process image Process image	0
	/PWM)\PTO1/PWM1\General\Enable	1 Tocciss image	ļo	i rocess inlage	
nable this pulse gen- ator		Enable this pulse generator	0		
	/PWM)\PTO1/PWM1\General\Project in	1.1		II	
ame omment	Pulse_1	Comment		Name	Pulse_2
	/PWM)\PTO1/PWM1\I/O addresses\Out	tput addresses			
art address	/PWM)\PTO1/PWM1\I/O addresses\Out 1000.0	End address	1001.7	Start address	1002.0
art address nd address	1000.0 1003.7	End address Organization block	0	Start address Organization block	1002.0
tart address nd address rocess image	1000.0	End address		_	
tart address nd address rocess image tartup	1000.0 1003.7 0	End address Organization block Process image	0	Organization block	
art address nd address rocess image artup cartup after POWER	1000.0 1003.7	End address Organization block Process image	0	_	0
art address nd address ocess image artup artup after POWER N Bs should be inter-	1000.0 1003.7 0 Warm restart - mode before POWER	End address Organization block Process image Comparison preset to	0	Organization block	0
art address nd address ocess image artup artup after POWER N Bs should be inter- ptible	1000.0 1003.7 0 Warm restart - mode before POWER	End address Organization block Process image Comparison preset to	0	Organization block Configuration time	60000ms
art address and address ocess image artup artup after POWER N Bs should be interptible ycle ycle monitoring	1000.0 1003.7 0 Warm restart - mode before POWER	End address Organization block Process image Comparison preset to	0	Organization block Configuration time Enable minimum cy-	0 60000ms
art address and address ocess image artup artup after POWER N Bs should be interptible vcle vcle monitoring me [ms]	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1	End address Organization block Process image Comparison preset to	0	Organization block Configuration time	0 60000ms
art address and address occess image artup eartup after POWER N Bs should be inter- ptible //cle //cle //cle monitoring me [ms] inimum cycle time	1000.0 1003.7 0 Warm restart - mode before POWER OFF	End address Organization block Process image Comparison preset to	0	Organization block Configuration time Enable minimum cy-	0 60000ms
art address and address ocess image artup artup after POWER N Bs should be interptible ycle ycle monitoring me [ms] inimum cycle time ommunication load ycle load due to	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1	End address Organization block Process image Comparison preset to	0	Organization block Configuration time Enable minimum cy-	0 60000ms
art address and address ocess image eartup eartup after POWER N Bs should be interptible ycle ycle monitoring me [ms] inimum cycle time ommunication load ycle load due to ommunication [%]	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms	End address Organization block Process image Comparison preset to	0	Organization block Configuration time Enable minimum cy-	0 60000ms
cart address and address rocess image cartup cartup after POWER N Bs should be interpible cycle cycle monitoring me [ms] inimum cycle time communication load cycle load due to communication [%]	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits	End address Organization block Process image Comparison preset to	0	Organization block Configuration time Enable minimum cy-	0 60000ms
rart address and address rocess image rartup rartup after POWER N Bs should be interptible rocle rocle rocle monitoring me [ms] inimum cycle time rommunication load rocle load due to rommunication [%] rstem and clock men hable the use of sys- m memory byte	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx)	0 Startup CPU even if mismatch	Configuration block Configuration time Enable minimum cycle time for cyclic OBs	0 60000ms
art address and address ocess image artup artup after POWER N Bs should be interptible ycle ycle monitoring me [ms] inimum cycle time ommunication load ycle load due to ommunication [%] ystem and clock men nable the use of sys- m memory byte agnostic status	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits	End address Organization block Process image Comparison preset to actual configuration Address of system	0 Startup CPU even if mismatch	Configuration time Enable minimum cycle time for cyclic OBs	0 60000ms
art address and address ocess image artup artup after POWER N Bs should be interptible ycle ycle monitoring me [ms] inimum cycle time ommunication load ycle load due to ommunication [%] ystem and clock men hable the use of sys- m memory byte agnostic status langed	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx)	0 Startup CPU even if mismatch	Configuration block Configuration time Enable minimum cycle time for cyclic OBs	0 60000ms
art address and address ocess image artup artup after POWER N Bs should be interptible ocle ocle ocle monitoring me [ms] inimum cycle time ommunication load ocle load due to ommunication [%] ostem and clock men hable the use of sys- m memory byte agnostic status langed ostem and clock men hable the use of	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high)	0 Startup CPU even if mismatch	Configuration block Configuration time Enable minimum cycle time for cyclic OBs	0 60000ms
art address and address occess image artup artup after POWER N Bs should be interptible ocle ocle ocle monitoring occessimate ommunication load occessimate occess	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx)	Startup CPU even if mismatch	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low)	0 60000ms 0 0 %M0.0 (Clock_10Hz)
art address and address occess image artup artup after POWER Be should be interptible ocle ocle monitoring one [ms] inimum cycle time ommunication load ocle load due to ommunication [%] ostem and clock men able the use of sys- om memory byte agnostic status anged ostem and clock men able the use of ock memory byte distance of ock memory byte distance of	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1 %M0.1 (Clock_5Hz)	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock	O Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address occess image artup artup after POWER N as should be interptible rcle rcle monitoring me [ms] inimum cycle time ommunication load rcle load due to ommunication [%] rstem and clock men hable the use of sys- m memory byte agnostic status hanged rstem and clock men hable the use of ock memory byte hable the use of	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx)	Startup CPU even if mismatch	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low)	0 60000ms 0 0 %M0.0 (Clock_10Hz)
art address and address occess image artup artup after POWER N as should be interptible ocle monitoring me [ms] inimum cycle time ommunication load ocle load due to ommunication [%] ostem and clock men able the use of sys- m memory byte agnostic status anged ostem and clock men bable the use of ock memory byte Az clock B Hz clock E Hz clock eb server\General	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz)	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock	O Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address occess image artup artup after POWER Ses should be interptible ocle monitoring one [ms] onimum cycle time ommunication load ocle load due to ommunication [%] stem and clock men orable the use of sys- om memory byte agnostic status anged stem and clock men ock memory byte distem and clock men ock memory byte distributed web server	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only	O Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address occess image artup artup after POWER N as should be interptible cele monitoring me [ms] inimum cycle time ommunication load cele load due to ommunication [%] retem and clock men hable the use of sys- m memory byte agnostic status langed retem and clock men hable the use of ock memory byte Late of cock memory byte Late of	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock	0 0 Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address occess image artup artup after POWER N Bs should be interptible vole vole vole monitoring me [ms] inimum cycle time ommunication load vole load due to ommunication [%] vstem and clock men nable the use of sys- m memory byte agnostic status langed vstem and clock men nable the use of ock memory byte Hz clock 25 Hz clock 5 Hz clock eb server\General ctivate Web server n all modules of this evice	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only	0 0 Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address ocess image artup artup after POWER N Bs should be interptible vcle vcle monitoring me [ms] inimum cycle time ommunication load vcle load due to ommunication [%] vstem and clock men hable the use of sys- m memory byte agnostic status hanged vstem and clock men hable the use of ock memory byte byte Lz clock 5 Hz clock 5 Hz clock 6 b server\General ctivate Web server hall modules of this evice eb server\Automatic hable automatic up-	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False update	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only	0 0 Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address ocess image artup artup after POWER N Bs should be interptible vole vole monitoring me [ms] inimum cycle time ommunication load vole load due to ommunication [%] vstem and clock men hable the use of sys- m memory byte agnostic status hanged vstem and clock men hable the use of ock memory byte Hz clock 25 Hz clock 5 Hz clock eb server\General ctivate Web server hall modules of this evice eb server\Automatic hable automatic up- hate	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False : update True	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS	0 Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address ocess image artup artup after POWER N Bs should be interptible vcle vcle monitoring me [ms] inimum cycle time ommunication load vcle load due to ommunication [%] vstem and clock men nable the use of sys- m memory byte agnostic status anged vstem and clock men nable the use of bck memory byte Hz clock EB Hz clock EB Hz clock EB Hz clock EB server\General ctivate Web server all modules of this evice eb server\Automatic nable automatic up-	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False : update True	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS	O Startup CPU even if mismatch 1 O %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz) True Os	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address occess image artup artup after POWER N as should be interptible vole monitoring me [ms] inimum cycle time ommunication load vole load due to ommunication [%] vstem and clock men hable the use of sys- m memory byte agnostic status hanged vstem and clock men hable the use of ock memory byte Az clock ES Hz clock ES Hz clock Eb server\General ctivate Web server hall modules of this evice eb server\Automatic hable automatic up- hate eb server\User mana	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False : update True	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS	0 Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz)	Configuration block Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz)
art address and address occess image artup artup after POWER N Bs should be interptible vcle vcle monitoring me [ms] inimum cycle time ommunication load vcle load due to ommunication [%] vstem and clock men hable the use of sys- m memory byte agnostic status hanged vstem and clock men hable the use of bock memory byte Hz clock EB Hz clock EB Hz clock EB server\General ctivate Web server hable automatic up- hable automatic up- hable automatic up- hable server\User mana ser name verybody eb server\User-defin	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False cupdate True agement	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS Update interval	Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz) True 0s	Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock 0.625 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz) %M0.6 (Clock_0.625Hz)
art address d address occess image artup artup after POWER dess should be interptible cle cle monitoring ne [ms] inimum cycle time ommunication load cle load due to mmunication [%] stem and clock men able the use of sys- m memory byte agnostic status anged stem and clock men able the use of ock memory byte dz clock 25 Hz clock 6 Hz clock 6 b server\General ctivate Web server all modules of this ovice eb server\Automatic able automatic up- te eb server\User mana ser name erybody	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% mory\System memory bits 0 mory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False c update True agement	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS Update interval	Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz) True Os Files with dynamic content	Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock 0.625 Hz clock	60000ms 60000ms %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz) %M0.6 (Clock_0.625Hz) Fragment DB number
art address d address cocess image artup artup after POWER d ss should be interptible cle cle monitoring ne [ms] nimum cycle time mmunication load cle load due to mmunication [%] stem and clock men able the use of sys- m memory byte agnostic status anged stem and clock men able the use of ock memory byte dz clock d tz clock d b server\General tivate Web server all modules of this vice eb server\Automatic able automatic up- te eb server\User mana ser name erybody eb server\User-defin oplication name	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False c update True agement ned web pages HTML source path	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS Update interval	Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz) True 0s	Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock 0.625 Hz clock	0 60000ms 0 %M0.0 (Clock_10Hz) %M0.3 (Clock_2Hz) %M0.6 (Clock_0.625Hz)
art address d address cocess image artup artup after POWER d s should be interptible cle cle monitoring ne [ms] nimum cycle time mmunication load cle load due to mmunication [%] stem and clock men able the use of sysmemory byte agnostic status anged stem and clock men able the use of ock memory byte d stem and clock men able the use of ock memory byte d stem and clock men able the use of ock memory byte d stem and clock men able the use of ock memory byte d stem and clock men able the use of ock memory byte d stem and clock d b server\General tivate Web server all modules of this vice eb server\Automatic able automatic up- te eb server\User mana er name erybody eb server\User-defin	1000.0 1003.7 0 Warm restart - mode before POWER OFF 1 150ms 1ms 20% nory\System memory bits 0 nory\Clock memory bits 1 %M0.1 (Clock_5Hz) %M0.4 (Clock_1.25Hz) %M0.7 (Clock_0.5Hz) False c update True agement ned web pages HTML source path	End address Organization block Process image Comparison preset to actual configuration Address of system memory byte (MBx) Always 1 (high) Address of clock memory byte (MBx) 2.5 Hz clock 1 Hz clock Permit access only with HTTPS Update interval	Startup CPU even if mismatch 1 0 %M0.2 (Clock_2.5Hz) %M0.5 (Clock_1Hz) True Os Files with dynamic content	Configuration time Enable minimum cycle time for cyclic OBs First cycle Always 0 (low) 10 Hz clock 2 Hz clock 0.625 Hz clock	60000ms

Totally Integrated Automation Portal								
User interface languages								
Assign project language				User interface lar	nguages			
English (United States)				German				
English (United States)				English				
English (United States)				French				
English (United States)				Spanish				
English (United States)				Italian				
English (United States)				Chinese (simplified	d)			
Time of day\Local time								
Ron	ne, Stockho	Berlin, Bern, Brussels, olm, Vienna						
Time of day\Daylight savir	ng time							
Activate daylight sav- 1			Difference between					
ing time			standard and daylig	ht				
Times of devADevdinlet service	4: a\C4.		saving time					
Time of day\Daylight savir Starting week of the Last		art of daylight saving th	ille	Sunday		of	March	
month:				Suriday		OI .	Water	
	:00 a.m.		.			JI		
Time of day\Daylight savir		art of standard time						
Last	_			Sunday		of	October	
	:00 a.m.			, ,		J1	1	
Protection & Security								
	protection							
Protection & Security\Con								
Permit access with Fals	se							
PUT/GET communica- tion from remote								
partner	•							
Protection & Security\Secu		t						
Summarize diagnos-	e		Length of an interva	al 20		Unit	seconds	
tics in case of high message volume								
Protection & Security\Exte	rnal load	memory						
Disable copying from Fals		illelilory						
internal load memory	se							
to external load mem-								
ory								
Configuration control\Con	nfiguration	n control for central conf	figuration					
Allow to reconfigure 0								
the device via the								
user program								
Connection resources\								
				resources - Reserved - Con-		ources - Dynamic - Con-	- Module resources - Analog Ir	nput
		Station resources - Rese imum	erved - Max-Station figured	resources - Reserved - Con-	Station reso	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] -	nput - Con-
Connection resources\			figured	resources - Reserved - Con-	figured	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured	nput - Con-
	ırces:	imum	figured 34		figured	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68	nput - Con-
Connection resources\ Maximum number of resou	ırces:	imum Maximum	figured		figured	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured	nput · Con-
Maximum number of resou	ırces:	imum Maximum 4	figured 34 Configured -		figured 34 Configured -	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured -	nput · Con-
Maximum number of resou PG communication: HMI communication:	ırces:	imum Maximum 4 12	figured 34 Configured - 0		figured 34 Configured - 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured -	nput · Con-
Maximum number of resources\ PG communication: HMI communication: S7 communication:	ırces:	imum Maximum 4 12	figured 34 Configured - 0 0		figured 34 Configured - 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0	nput - Con-
Connection resources\ Maximum number of resou PG communication: HMI communication: S7 communication: Open user communication:	irces:	imum Maximum 4 12 8 8	figured 34 Configured - 0		figured 34 Configured - 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured -	nput - Con-
Maximum number of resou PG communication: HMI communication: S7 communication: Open user communication: Web communication:	irces:	imum Maximum 4 12 8 8 2	figured 34 Configured - 0 0		figured 34 Configured - 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0	nput - Con-
Connection resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server comm	irces:	imum Maximum 4 12 8 8	figured 34 Configured - 0 0		figured 34 Configured - 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0	nput · Con-
Connection resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication:	irces:	imum Maximum 4 12 8 8 2	figured 34 Configured - 0 0	red	figured 34 Configured - 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication	irces:	imum Maximum 4 12 8 8 2	figured 34 Configured - 0 0	red	figured 34 Configured - 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0	nput - Con-
Connection resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication:	irces:	imum Maximum 4 12 8 8 2	figured 34 Configure 0 0	red	figured 34 Configured - 0 0 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0	nput - Con-
Connection resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources:	irces:	imum Maximum 4 12 8 8 2 0	figured 34 Configure - 0 0 0 34	red	figured 34 Configured - 0 0 0 0 0 0 0	ources - Dynamic - Con	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0	nput - Con-
Maximum number of resounces Maximum number of resounces PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview	irces: : nunica-	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Connection resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources:	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	figured 34 Configure - 0 0 0 34	red	figured 34 Configured - 0 0 0 0 0 0 0	Address gaps	MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieuelder Inputs True	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overview of resources	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieuelder Inputs True	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieuelder Inputs True	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieuelder Inputs True	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieuelder Inputs True	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput • Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieuelder Inputs True	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput • Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of addresses\Overvi	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of a	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-
Maximum number of resources\ Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overlieue	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput · Con-
Maximum number of resources\ PG communication: HMI communication: S7 communication: Open user communication: Web communication: OPC UA client/server communication: Other communication: Total resources used: Available resources: Overview of addresses\Overview of a	urces: : : : : unica- verview of	imum Maximum 4 12 8 8 2 0	34 Configured 34	red	figured 34 Configured - 0 0 0 0 0 0 0		MNS [CPU 1214C DC/DC/DC] - figured 68 Configured - 0 0 0 0 0 68	nput - Con-

Totally Integrated
Automation Portal

Type	Addr. from	Addr. to	Module	PIP	Device name	Device number	Size	Master / IO sys- tem	Rack	Slot
	0	1	DI 14/DQ 10_1	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 1
0	0	1	DI 14/DQ 10_1	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 1
	64	67	AI 2_1	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 2
	1000	1003	HSC_1	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 16
	1004	1007	HSC_2	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 17
	1008	1011	HSC_3	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 18
l	1012	1015	HSC_4	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 19
	1016	1019	HSC_5	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 20
	1020	1023	HSC_6	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	4 Bytes	-	0	1 21
O	1000	1001	Pulse_1	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 32
0	1002	1003	Pulse_2	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 33
)	1004	1005	Pulse_3	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 34
0	1006	1007	Pulse_4	Automatic up- date	Analog Input MNS [CPU 1214C DC/DC/DC]	-	2 Bytes	-	0	1 35

Totally Integrated Automation Portal		
Analog Input / A	nalog Input MNS [CPU 1214C DC/DC/DC]	

Totally Integra Automation Po	ted ortal														
Device view	l.				\$										_
				Analog Input	inter .										
		•		Ana											
	Rack_0		02 101	SIEMENS	1 SIMATIC \$7-1200	2	3	4	5	6	7	8	9		
				MAKIT III		dic C									
				31 PALAN	DQOCA										
						_									
															_