## TC40H367P/F TC40H368P/F

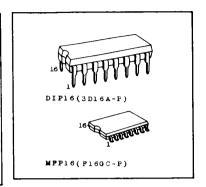
# C2MOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC40H367 HEX BUS BUFFER NONINVERTED 3-STATE OUTPUT TC40H368 HEX BUS BUFFER INVERTED 3-STATE OUTPUT

The TC40H367 and the TC40H368 are hex inverting and non-inverting buffers provided with 3-state output functions. Respective DISABLE inputs for putting outputs in disable conditions are of circuit configuration common in two circuits and four circuits. Therefore, these buffers are suitable for controlling 4-bit data lines.

Further, the output current of each buffer is large, permitting direct drive of then LSTTL input lines.

The TC40H367 and the TC40H368 are compatible in function and pin assignment with the TTL 74LS367 and TTL 74LS368. Further, Toshiba's original product, the TC5012BP, is the same as the TC40H367.



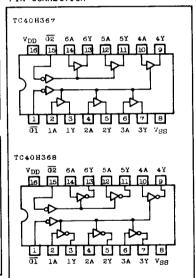
#### MAXIMUM RATINGS

HANTHON WALLINGS				
CHARACTERISTIC	SYMBOL	RATING	UNIT	
Supply Voltage	V <sub>DD</sub>	V <sub>SS-0.5</sub> ~ V <sub>SS+10</sub>	V	
Input Voltage	VIN	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	V	
Output Voltage	VOUT	V <sub>SS</sub> -0.5 ~ V <sub>DD</sub> +0.5	v	
Input Current	IIN	±10	m.A.	
Power Dissipation	P <sub>D</sub>	300(DIP)/180(MFP)	mW	
Storage Temperature	Tstg	-65 ∿ 150	°c	
Lead Temp./Time	Tsol	260°C • 10 sec		

#### TRUTH TARLE

TC40H367P					
DISABLE INPUT	INPUT	OUTPUT			
L	L	L			
L	Н	H			
Н	*	HZ			
TC40H368P					
DISABLE INPUT	INPUT	OUTPUT			
L	L	н			
L	Н	Ĺ			
н ☀ нz					
HZ=HIGH IMPED * = Don't care	ANCE				

#### PIN CONNECTION



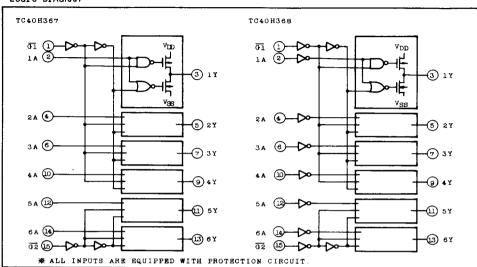
#### RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	v <sub>DD</sub>		2.0	-	8.0	V
Input Voltage	VIN		0	-	v <sub>DD</sub>	v
Operating Temperature	Topr		-40	<del>-</del>	85	°c

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### LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (VSS=0V)

CHARACTERISTIC SYM		CYMBOI	SYMBOL TEST CONDITION VDD		-40°C			25°C		85°		
		SIMBUL			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
High Le Output	vel Voltage	v <sub>OH</sub>	$ I_{OUT}  < 1_{\mu}A$ $v_{IN} = v_{SS}$ , $v_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	
Low Lev Output	el Voltage	v <sub>OL</sub>	VIN=VSS, VDD	5	-	0.05	-	0.0	0.05	-	0.05	V
High Le Output	vel Current	IOH	V <sub>OUT=4.6</sub> V V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	-0.95	-	-0.88	-	_	-0.8	-	
Low Level Output Current		IOL	V <sub>OUT=0.4V</sub> V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	4.7	-	4.4	-	-	4.0	-	mA
Input	"H" Level	VIH	$ I_{OUT}  < 1_{\mu}A$ $V_{OUT}=0.5V$	5	4.0	-	4.0	-	_	4.0	-	
Voltage	"L" Level	VIL	V <sub>OUT=4.5</sub> V	5	-	1.0	-	-	1.0	-	1.0	V
Input	"H" Level	IIH	V <sub>IN=8.0V</sub>	8	-	0.3	-	10-5	0.3	-	1.0	
Current	"L" Level	IIL	VIN=0.0V	8	-	-0.3	-	-10-5	-0.3	-	-1.0	μA
Disable 🗕 —	"H" Level	IDH	VDH=8.0V	8	-	0.5	-	10-4	0.5	-	.5	
	"L" Level	IDL	VDL=0.0V	8	-	-0.5	-	-10-4	-0.5	-	5	μA
Quiescent Supply Current *All input valid com		I <sub>DD</sub>	*V <sub>IN</sub> =V <sub>SS</sub> ,V <sub>DD</sub>	5	-	5.0	-	0.005	5.0	-	25	μA

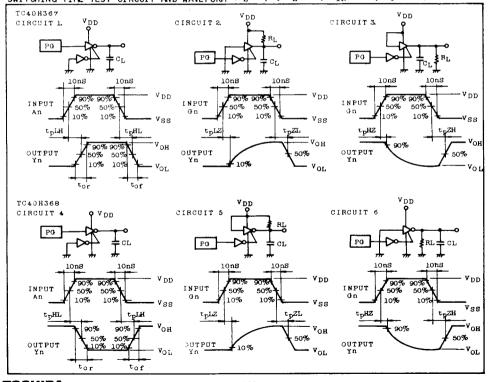
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SWITCHING CHARACTERISTICS (Ta=25°C,  $V_{SS}=0V$ ,  $V_{DD}=5V$ ,  $C_L=50pF$ ,  $R_L=1k\Omega$ )

CHARACTERISTIC		GING OF	TEGE CONDITION	тс40н367			тс40н368			
		SIMBOL	TEST CONDITION	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Output Rise Time Output Fall Time		tor	Fig.1, 4	-	17	35	-	17	35	ns
		tof		-	14	30	_	14	30	
Propagation	High Level	tpLH		-	20	35	-	23	35	
Delay Time	Low Level	t <sub>pHL</sub> Fig.1, 4	-	25	41	-	27	41	ns	
Output Disable	High Level	t <sub>pHZ</sub>	Fig.3, 6	-	26	45	-	26	45	
Time	Low Level	tpLZ	Fig.2, 5	-	26	45	-	26	45	ns
Output Enable	High Level	tpZH	Fig.3, 6	-	26	45	-	26	45	
Time	Low Level	tpZL	ZL Fig. 2, 5	-	30	45	-	30	45	ns
Input Capacitance		CIN		T -	5	-		5	-	
Output Capacitance		COUT		-	16		-	16		pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM ( $C_L=50pF$ ,  $R_L=1k\Omega$ ,  $f_{IN}=1MHz$ ,  $t_f=10ns$ )



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