NEC
NEC Electronics Inc.

T-75-11-90

μPD7755/56/P56/57/58
ADPCM Speech Processors

Description

The μPD775x speech processors utilize adaptive differential pulse-code modulation (ADPCM) to produce high-quality, natural-sounding speech. The μPD775x family includes four types with a built-in ROM and one with a one-time programmable (OTP) ROM.

ROM	OTP ROM
μPD7755	—
μPD7756	μPD77P56
μPD7757	—
μPD7758	—

Note: Unless excluded by context, μPD775x means all types listed above; μPD7756 includes μPD77P56. The μPD7759, which uses external ROM, is also considered part of the μPD775x family but is covered in a separate data sheet.

By combining melody mode, ADPCM, and pause compression, the μPD775x achieves a compressed bit rate that can reproduce sound effects and melodies in addition to speech. A built-in speech data ROM allows reproduction of messages up to 4 seconds (μPD7755), 12 seconds (μPD7756), 24 seconds (μPD7757), or 48 seconds (μPD7758).

A wide range of operating voltages, a compact package, and a standby function permit applications of the μPD775x in a variety of speech output systems, including battery-driven systems.

Features

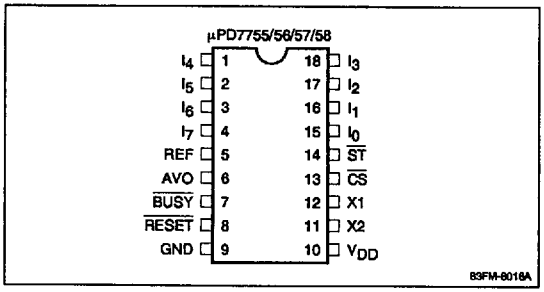
- High-quality speech reproduction using ADPCM
- Low bit rates (10 to 32 kb/s) using a combination of ADPCM and pause compression
- Bit rates to less than 1 kb/s for sound effects, melodies, and tones (DTMF) using melody mode
- D/A converter with 9-bit resolution and unipolar current waveform output
- Built-in speech data ROM
  - —μPD7755: 96K bits
  - —μPD7756/P56: 256K bits
  - —μPD7757: 512K bits
  - —μPD7758: 1M bits
- Sampling frequency: 5, 6, or 8 kHz
- Standby function
- Typical standby current: 1 μA (V_{DD} = 3 V)
- Circuit to eliminate popcorn noise when entering or releasing standby mode
- Wide operating voltage range: 2.7 to 5.5 V
- CMOS technology
- 18- and 20-pin plastic DIP
- 24-pin plastic SOP

Ordering Information

Part Number	Package	ROM (bits)
μPD7755C	18-pin plastic DIP (A, C outline)	96K
55G	24-pin plastic SOP	
μPD7756C	18-pin plastic DIP (A, C outline)	256K
56G	24-pin plastic SOP	
μPD77P56CR	20-pin plastic DIP	256K (OTP)
P56G	24-pin plastic SOP	
μPD7757C	18-pin plastic DIP (SA outline)	512K
57G	24-pin plastic SOP	
μPD7758C	18-pin plastic DIP (SA outline)	1M
58G	24-pin plastic SOP	

Pin Configurations

18-Pin Plastic DIP



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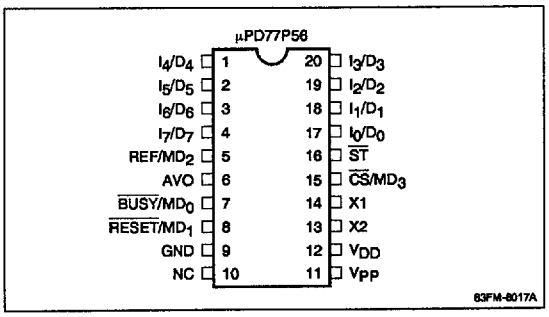
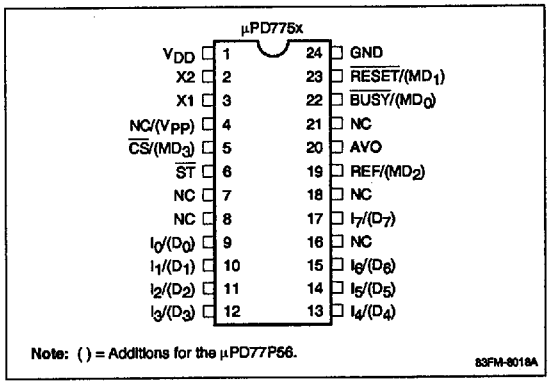
Pin Configurations (cont)

20-Pin Plastic DIP



24-Pin Plastic SOP



Pin Identification

Symbol	Name
AVO	Analog voice output
$\overline{BUSY}$	Busy output
$\overline{CS}$	Chip select input
D_0 - D_7	PROM I/O data bus
I_0 - I_7	Message select code input
MD_0 - MD_3	Operation mode selection input from PROM
REF	D/A converter reference current input
$\overline{RESET}$	Reset input
$\overline{ST}$	Start input
X1, X2	Ceramic resonator clock terminals
V_{DD}	+5 V power
V_{PP}	+12.5 V PROM voltage application
GND	Ground
NC	No connection

PIN FUNCTIONS

AVO (Analog Voice Output)

AVO outputs speech from the D/A converter. This is a unipolar sink-load current. No current flows in standby mode.

$\overline{BUSY}$ (Busy)

$\overline{BUSY}$ outputs the status of the μPD775x. It goes low during speech decode and output operations. When $\overline{ST}$ is received, $\overline{BUSY}$ goes low. While $\overline{BUSY}$ is low, another $\overline{ST}$ will not be accepted. In standby mode, $\overline{BUSY}$ becomes high impedance. This is an active low output.

$\overline{CS}$ (Chip Select)

When the $\overline{CS}$ input goes low, $\overline{ST}$ is enabled.

D_0 - D_7 (Data Bus)

Eight-bit input/output data bus from PROM when programming and verifying data.

I_0 - I_7 (Message Select Code)

I_0 - I_7 input the message number of the message to be decoded. The inputs are latched at the rising edge of the $\overline{ST}$ input. Unused pins should be grounded. In standby mode, these pins should be set high or low. If they are biased at or near typical CMOS switch input, they will drain excess current.

MD_0 - MD_3 (Mode Select Input)

Operation mode selection inputs from PROM when programming and verifying data.

REF (D/A Converter Reference Current)

REF inputs the sink-load current that controls the D/A converter output. REF should be connected to V_{DD} via a resistor. In standby mode, REF becomes high impedance.

$\overline{RESET}$ (Reset)

The $\overline{RESET}$ input initialized the chip. Use $\overline{RESET}$ following power-up to abort speech reproduction or to release standby mode. $\overline{RESET}$ must remain low at least 12 oscillator clocks. At power-up or when recovering from standby mode, $\overline{RESET}$ must remain low at least 12 more clocks after clock oscillation stabilizes.

$\overline{ST}$ (Start)

Setting the $\overline{ST}$ input low while $\overline{CS}$ is low will start speech reproduction of the message in the speech ROM locations addressed by the contents of I_0 - I_7. If the device is in standby mode, standby mode will be released.

X1, X2 (Clock)

Pins X1 and X2 should be connected to a 640 kHz ceramic resonator. In standby mode, X1 goes low and X2 goes high.

V_{DD} (Power)

+5-V power supply.

V_{PP} (PROM Power)

+12.5-V high-voltage application pin for programming and verifying data to PROM.

GND (Ground)

Ground.

NC (No Connection)

These pins are not connected.

OPERATION

The μPD775x can operate with a V_{DD} supply voltage in the 2.7- to 5.5-V range. An external 640-kHz ceramic resonator connected to pins X1 and X2 drives the internal clock oscillator. Initialization is performed by holding the $\overline{RESET}$ pin low for at least 12 oscillator clock cycles.

When the μPD775x has been idle (that is, when $\overline{CS}$, $\overline{ST}$, or $\overline{RESET}$ have not been asserted) for more than 3 seconds, the μPD775x goes to a standby mode. It will automatically release from standby mode when $\overline{CS}$ and $\overline{ST}$ are asserted again or when $\overline{RESET}$ is asserted.

A μPD775x can store 256 different messages and up to 4 (μPD7755), 12 (μPD7756), 24 (μPD7757), or 48 (μPD7758) seconds of speech. The message selection at pins I_0 - I_7 is latched at the rising edge of $\overline{ST}$ when $\overline{CS}$ is asserted. $\overline{BUSY}$ goes low until the selected audio speech output is completed. While $\overline{BUSY}$ is low, a new $\overline{ST}$ will not be accepted.

The internal D/A converter has 9-bit resolution and unipolar current output. Current can be controlled by the voltage applied at the REF pin.

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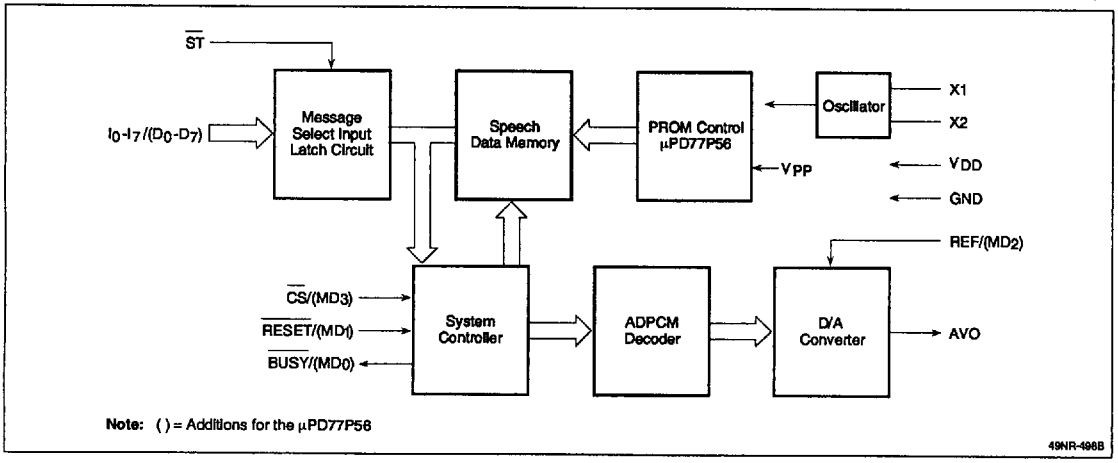
μPD775x Block Diagram



ELECTRICAL SPECIFICATIONS

This section describes the electrical specifications for the μPD775x family of processors. The μPD77P56 electrical specifications in PROM operation mode are described in the later PROM electrical specifications section.

Capacitance

T_A = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			10	pF	fc = 1 MHz
Output capacitance	C_O			20	pF	

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
PROM power voltage, V_{PP}	−0.3 to +13.5 V
PROM output current, I_O (AVO pin only)	50 mA
Operating temperature, T_{OPT}	
7755/56/57/58	−10 to +70°C
77P56	−40 to +85°C
Storage temperature, T_{STG}	
7755/56/57/58	−40 to +125°C
77P56	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Operating temperature	t_{OPT}					Ambient temperature
7755/56/57/58		−10		+70	°C	
77P56		−40		+85	°C	
Power voltage	V_{DD}	2.7		5.5	V	Operation
		5.75		6.25	V	PROM Programming
PROM programming voltage	V_{PP}	2.7		5.5	V	Operation
		12.2		12.8	V	PROM programming
$\overline{\text{RESET}}$ pulse width	t_{RST}	18.5			μs	
$\overline{\text{ST}}$ set-up time	t_{RS}	12.5			μs	From $\overline{\text{RESET}}$ ↑
$\overline{\text{ST}}$ pulse width	t_{CC1}	2			μs	V_{DD} = 2.7 to 5.5 V
	t_{CC2}	350			ns	V_{DD} = 4.5 to 5.5 V
Data set time	t_{DW1}	2			μs	V_{DD} = 2.7 to 5.5 V
	t_{DW2}	350			ns	V_{DD} = 4.5 to 5.5 V
Data hold time	t_{WD}	0			ns	
$\overline{\text{CS}}$ set-up time	t_{CS}	0			ns	
$\overline{\text{CS}}$ hold time	t_{SC}	0			ns	
CLK frequency	f_{OSC}	630	640	650	kHz	

Note: Voltage at AC timing measuring point: $V_{IL} = V_{OL} = 0.3\ V_{DD}$ and $V_{IH} = V_{OH} = 0.7\ V_{DD}$

DC Characteristics

T_A = −10 to +70°C; T_A = −40 to +85°C (μPD77P56); V_{DD} = 2.7 to 5.5 V; f_{OSC} = 640 kHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage high	V_{IH}	0.7 V_{DD}		V_{DD}	V	Applies to I_0 - I_7, $\overline{\text{ST}}$, $\overline{\text{CS}}$, $\overline{\text{RESET}}$
Input voltage low	V_{IL}	0		0.3 V_{DD}	V	Applies to I_0 - I_7, $\overline{\text{ST}}$, $\overline{\text{CS}}$, $\overline{\text{RESET}}$
Output voltage high	V_{OH}	V_{DD} − 0.5		V_{DD}	V	Applies to $\overline{\text{BUSY}}$, I_{OH} = −100 μA
Output voltage low	V_{OL1}			0.4	V	Applies to $\overline{\text{BUSY}}$, V_{DD} = 5 V ±10%, I_{OL} = 1.6 mA
	V_{OL2}	0		0.5	V	Applies to $\overline{\text{BUSY}}$, I_{OL} = −200 μA

DC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input leakage current	I_{LI}			3	μA	Applies to I_0 - I_7, $\overline{ST}$, REF, $\overline{CS}$; V_I = 0 to V_{DD}
Output leakage current	I_{LO}			3	μA	Applies to $\overline{BUSY}$; V_O = 0 to V_{DD} in standby mode
Supply current	I_{DD1}		0.8	2	mA	V_{DD} = 2.7 to 5.5 V
	I_{DD2}		1	20	μA	V_{DD} = 2.7 to 5.5 V in standby mode
	I_{DD3}		250	600	μA	V_{DD} = 2.7 to 3.3 V
	I_{DD4}		1	10	μA	V_{DD} = 2.7 to 3.3 V in standby mode
	I_{PP}		1	20	μA	V_{PP} = V_{DD}
Reference input high current area (figure 1)	I_{REF1}	140	250	440	μA	V_{DD} = 2.7 V, R_{REF} = 0 Ω
	I_{REF2}	500	760	1200	μA	V_{DD} = 5.5 V, R_{REF} = 0 Ω
Reference input low current area (figure 1)	I_{REF3}	21	30	39	μA	V_{DD} = 2.7 V, R_{REF} = 50 kΩ
	I_{REF4}	68	78	88	μA	V_{DD} = 5.5 V, R_{REF} = 50 kΩ
D/A converter output current (figure 1)	I_{AVO}	32	34	36	I_{REF}	V_{DD} = 2.7 to 5.5 V, V_{AVO} = 2.0 V, D/A input = 1FFH
D/A converter output leakage current	I_{LA}			±5	μA	V_{AVO} = 0 to V_{DD} in standby mode

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AC Characteristics

T_A = −10 to +70°C; T_A = −40 to +85°C (μPD77P56); V_{DD} = 2.7 to 5.5 V; f_{OSC} = 640 kHz

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
$\overline{BUSY}$ output time (from $\overline{ST}$ and/or $\overline{CS}$)	t_{SBO}		6.25	10	μs	Operation mode
	t_{SBS}		4	80	ms	Standby mode, including oscillation start time
$\overline{BUSY}$ set time	t_{SB}		6.25	10	μs	Standby mode
Speech output start time	t_{SSO}		2.1	2.2	ms	Operation mode (from $\overline{BUSY}$)
	t_{SSS}		2.1	2.2	ms	Standby mode
D/A converter set-up time	t_{DA}		46.5	47	ms	Entering/releasing standby mode
$\overline{BUSY}$ delay time	t_{BD}			15	μs	From end of speech output
$\overline{BUSY}$ output stop time	t_{RB}			9.5	μs	For $\overline{RESET}$ ↓
Standby transition time	t_{STB}		2.9	3	s	From end of speech output

Figure 1. Measuring Diagram for I_{REF} and I_{AVO}

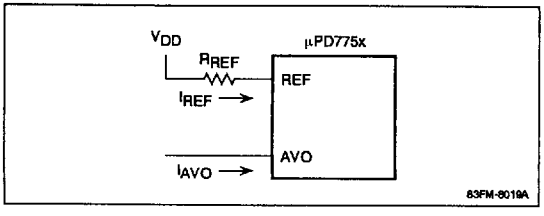
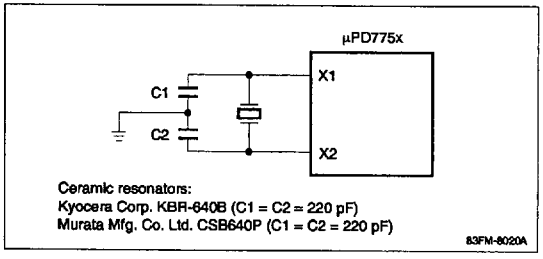
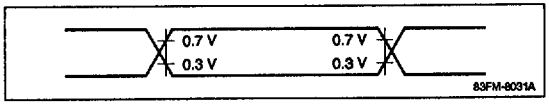


Figure 2. External Oscillator

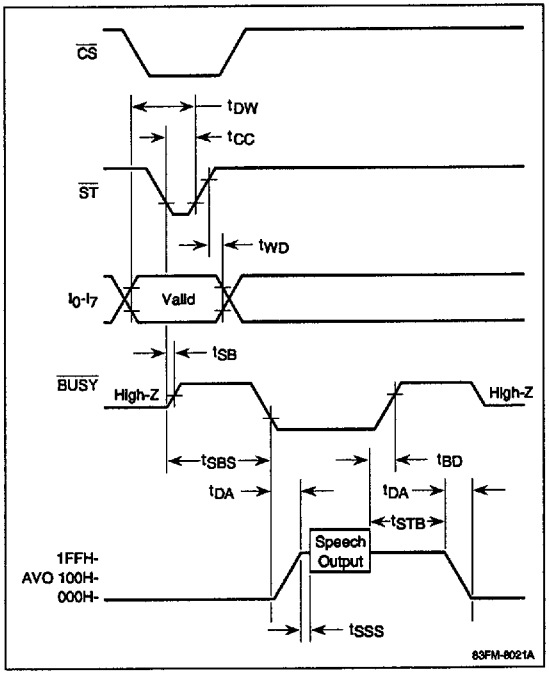


Timing Waveforms

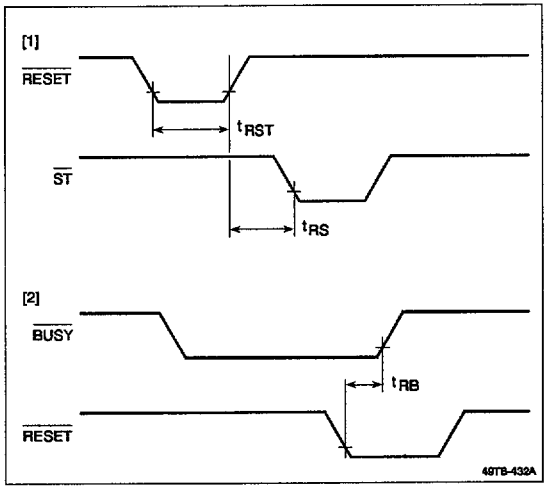
AC Waveform Measurement Points



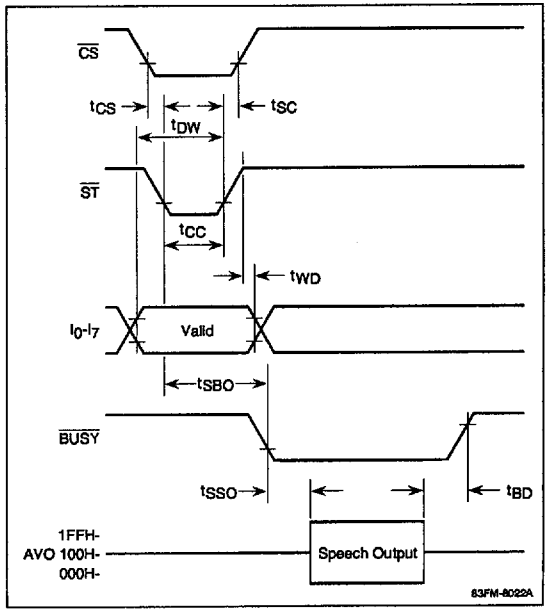
Standby Mode



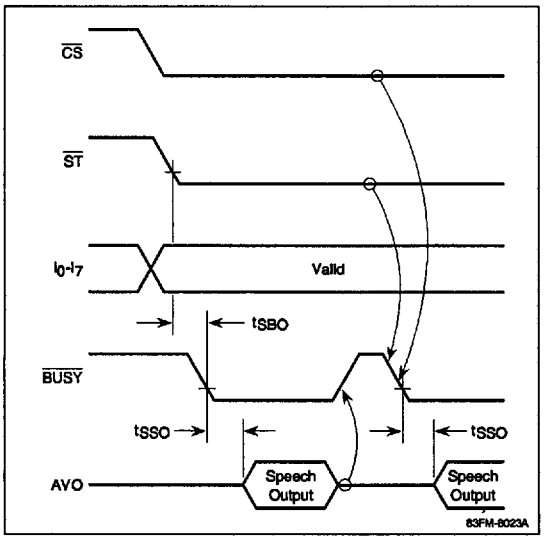
Reset Mode



Operating Mode (ST Input Pulse Mode)



Operating Mode ($\overline{ST}$ Input Hold Low Mode)



USING ONE-TIME PROGRAMMABLE ROM

The μPD77P56 speech processor features a 256K-bit one-time programmable (OTP) ROM. This section describes the PROM initialization procedure, the PROM operation modes, the PROM programming procedure, and the data readout verification procedure.

Initialization

Before programming the PROM, the PROM address 0 clear mode must be set to prevent erroneous programming: set the MD_0 - MD_3 pins to high, low, high, low, respectively. The PROM address 0 clear specifications are also shown in the PROM Operation Modes table.

Permanent data used for the LSI is stored in the system area of the memory from 0001H to 0004H. This data is **5AH, A5H, 69H,** and **55H.** Blank check the memory at 0000H and from 0005H to the end address. Program the memory from 0000H to the end address.

PROM Operation Modes

To enter the PROM operation modes, connect +6 V to V_{DD} and +12.5 V to V_{PP} and set the $\overline{ST}$ pin to low level. Also set AVO and X_2 pins open and X_1 to low level. There are four PROM operation modes. The PROM Operation Modes table identifies and decribes these four modes.

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PROM Operation Modes

Operation Mode	Description	Operation Mode Specifications			
		MD_0	MD_1	MD_2	MD_3
PROM address 0 clear	This mode sets the PROM address to 0, even if set while switching between modes. Setting this mode out of sequence may result in erroneous changes to data.	High	Low	High	Low
Program mode	This mode programs speech data to PROM with data on D_0 - D_7.	Low	High	High	High
Verify mode	This mode checks the speech data stored in PROM. The data can be verified by reading D_0 - D_7.	Low	Low	High	High
Inhibit mode	This precautionary mode can be used while switching between modes. This mode can be passed through to avoid an accidental setting of the program address 0 clear mode.	High	High or Low	High	High

PROM Programming Procedure

This procedure describes how to program the PROM. Data can be programmed into PROM at two timing speeds, low or high. The procedure for both speeds is the same, except that at low speed data is programmed for 1 millisecond and at high speed data is programmed for 250 microseconds. The PROM timing waveforms section has diagrams that illustrate low- and high-speed timing. See figure 3 for a flow-chart diagram of the PROM programming procedure. The procedure is as follows:

(1) Set $\overline{ST}$ pin to low level, AVO and X2 pins to open, and X1 to low level.
(2) Apply +5 V to V_{DD} and to V_{PP}.
(3) Wait 10 μs.
(4) Set PROM address 0 clear mode.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}
(6) Set program inhibit mode.
(7) Program data in 1 ms (low speed) or 250 μs (high speed) of program mode.
(8) Set inhibit mode.
(9) Set verify mode: If data has been programmed, go to step 10, if data has not been programmed, repeat steps 7 to 9.
(10) For low-speed, additional programming: X x 1 ms, where X is equal to the number of times data has been programmed in steps 7 to 9.
(11) Set inhibit mode.
(12) Increment an address by applying a pulse to X1 pin four times.
(13) Repeat steps 7 to 9 up to the final address.
(14) Set PROM address 0 clear mode.
(15) Change voltages V_{DD} and V_{PP} to +5 V.
(16) Turn the power off.

Notes:

(1) Avoid setting the PROM address 0 clear mode when moving to another mode.

(2) This high-speed programming procedure is different from that of μPD27C256A.

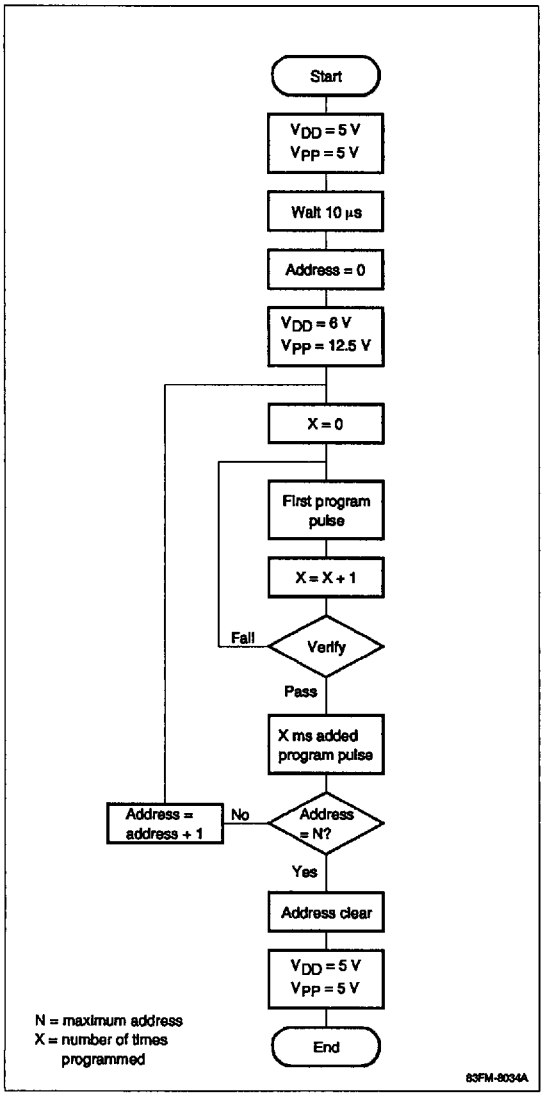
PROM Data Readout Procedure

The programmed processor can read out data from the PROM. The PROM timing waveforms section has a diagram that illustrates the data readout timing. To verify the data, use the following procedure:

(1) Set $\overline{ST}$ pin to low level, AVO and X2 pins to open, and X1 to low level.
(2) Apply +5 V to V_{DD} and to V_{PP}.
(3) Wait 10 μs.
(4) Set PROM address 0 clear mode.
(5) Apply +6 V to V_{DD} and +12.5 V to V_{PP}.
(6) Set inhibit mode.
(7) Set verify mode: Read data for one address on D_0 - D_7; then apply four clock pulses to the X1 pin. Repeat for each address up to the end address.
(8) Set inhibit mode.
(9) Set PROM address 0 clear mode.
(10) Change voltages V_{DD} and V_{PP} to +5 V.
(11) Turn the power off.

Note: Avoid setting the PROM address 0 clear mode when moving to another mode.

Figure 3. PROM Programming Flow Chart



PROM ELECTRICAL SPECIFICATIONS

This section lists the electrical specifications of the μPD77P56 while in PROM operation modes.

DC Characteristics

T_A = 25 ±5°C; V_{DD} = 6 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage high	V_{IH1}	4.2		6	V	D_0 - D_7, MD_0, MD_1, MD_3, $\overline{ST}$, X1
	V_{IH2}	2.5		6	V	MD_2
Input voltage low	V_{IL1}	0		1.8	V	D_0 - D_7, MD_0, MD_1, MD_3, $\overline{ST}$, X1
	V_{IL2}	0		0.5	V	MD_2
Output voltage high	V_{OH}	5.5			V	D_0 - D_7, I_{OH} = −1 mA
Output voltage low	V_{OL}			0.5	V	D_0 - D_7, I_{OL} = +1 mA
Input leakage current	I_{LI}			3	μA	D_0 - D_7, MD_0, MD_1, MD_3, $\overline{ST}$, V_{IN} = 0 to V_{DD}
Clock input current	I_{IH1}	3		20	μA	X1, V_{IN} = V_{DD}
	I_{IL1}	3		20	μA	X1, V_{IN} = 0 V
MD_2 input current	I_{IH2}	0.5		1.4	mA	MD_2, V_{IN} = V_{DD}
		0.12		0.4	mA	MD_2, V_{IN} = 2.5 V
	I_{IL2}			3	μA	MD_2, V_{IN} = 0 V
Supply current	I_{DD}			2	mA	
	I_{PP}			10	mA	

AC Characteristics

T_A = 25 ±5°C; V_{DD} = 6 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Address setup time (for MD_0 ↓)	t_{AS}	2			μs	
MD_1 setup time (for MD_0 ↓)	t_{M1S}	2			μs	
Data setup time (for MD_0 ↓)	t_{DS}	2			μs	
Address hold time (for MD_0 ↑)	t_{AH}	2			μs	
Data hold time (for MD_0 ↑)	t_{DH}	2			μs	
MD_0 ↑ to data output float delay time	t_{DF}	0		130	ns	
V_{PP} setup time (for MD_3 ↑)	t_{VPS}	2			μs	
V_{DD} setup time (for MD_3 ↑)	t_{VDS}	2			μs	
Initial program pulse width	t_{PW}	0.9	1	1.1	ms	Low-speed programming
		240	250	260	μs	High-speed programming
MD_0 setup time (for MD_1 ↑)	t_{MOS}	2			μs	
MD_0 ↓ to data output delay time	t_{DV}			1	μs	MD_0 = MD_1 = V_{IL}
MD_1 hold time (for MD_0 ↑)	t_{M1H}	2			μs	t_{M1H} + t_{M1R} ≥ 50 μs
MD_1 recovery time (for MD_0 ↓)	t_{M1R}	2			μs	
Program counter reset time	t_{PCR}	10			μs	
X1 input high-and low-level widths	t_{XH}, t_{XL}	1			μs	
X1 input frequency	f_X			1	MHz	
Initial mode-setting time	t_I	2			μs	

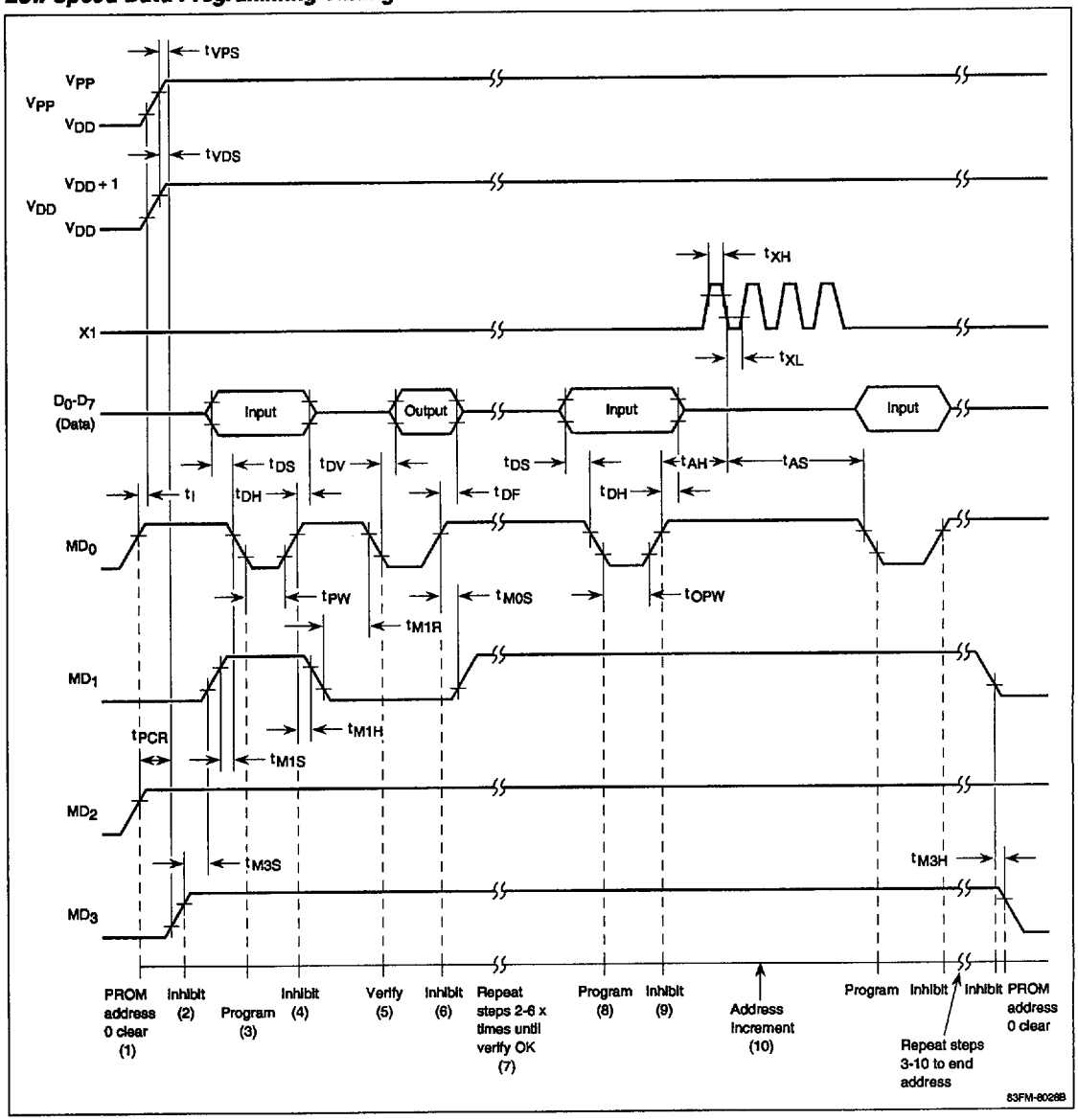
AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
MD_3 setup time (for MD_1 ↑)	t_{M3S}	2			μs	
MD_3 hold time (for MD_1 ↓)	t_{M3H}	2			μs	
MD_3 setup time (for MD_0 ↓)	t_{M3SR}	2			μs	Program memory readout
Address to data output delay time	t_{DAD}	2			μs	
Address to data output hold time	t_{HAD}	0		130	ns	
MD_3 hold time (for MD_0 ↑)	t_{M3HR}	2			μs	
MD_3 ↓ to data output float delay time	t_{DFR}	2			μs	
MD_0 hold time (for MD_2 ↑)	t_{M0HS}	2			μs	
MD_2 ↑ to data output delay time	t_{DDS}	2			μs	
MD_2 hold time (for MD_0 ↓)	t_{M0SS}	2			μs	

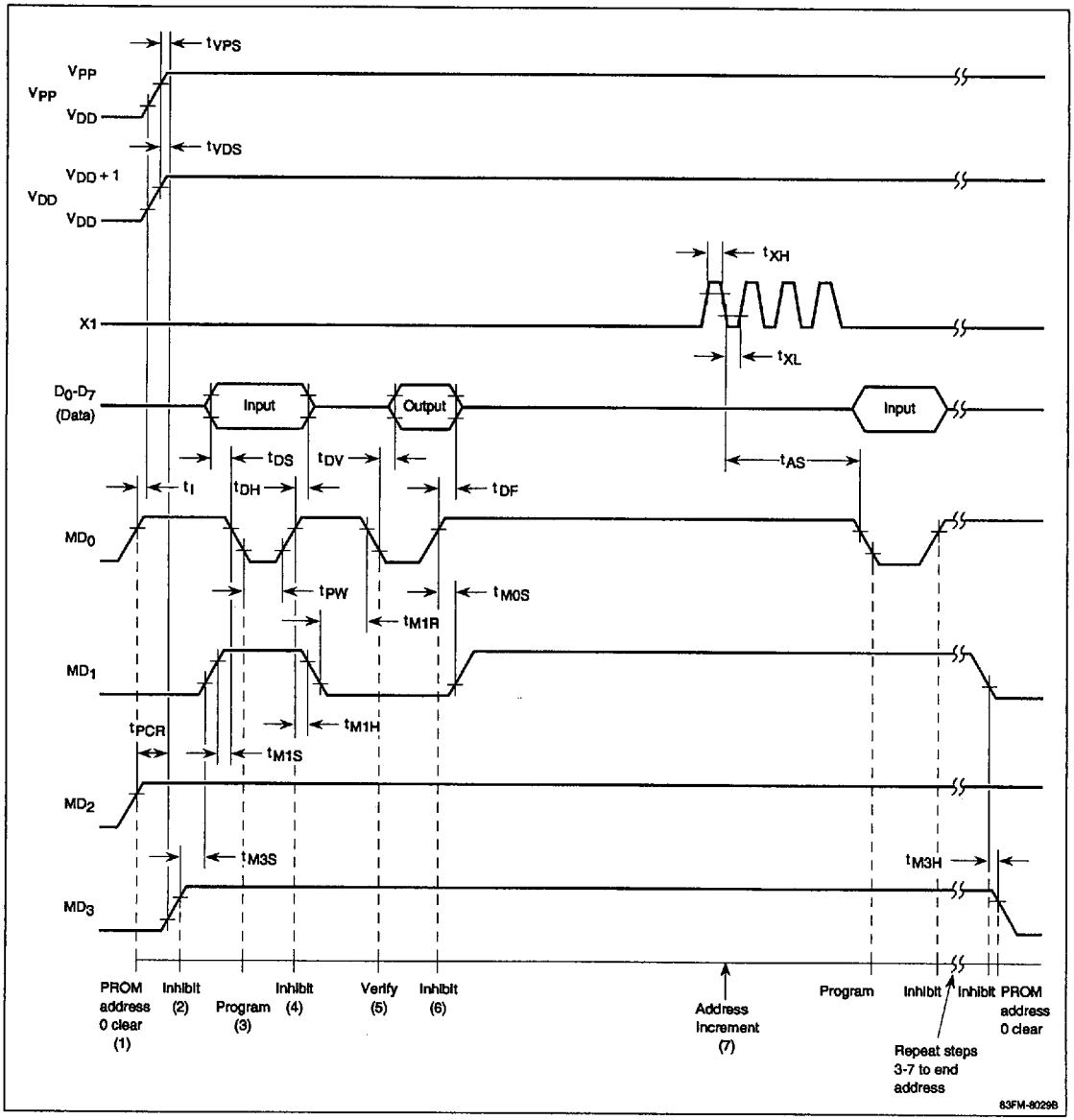
4b

PROM Timing Waveforms

Low-Speed Data Programming Timing



High-Speed Data Programming Timing



4b

Data Readout Timing