Radio Frequency Transceiver Design

Project Work – Ver.D1/2012

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Project description
(Ver.D1)

Introduction

In this project you will design an RF transceiver (TRx) at the system level of abstraction. The familiarity with RF integrated circuits and especially understanding their specs and physical limitations is indispensable to successfully complete this design.
The TRx should operate as 16-QAM system in the full duplex mode (FDD). In this case the receiver (Rx) performance is also affected by the companion transmitter (Tx).
Based on the minimum performance specs defined in Table 1 you will be able to derive the fundamental Rx and Tx metrics like gain, noise figure, linearity, selectivity, local oscillator phase noise, adjacent channel rejection, etc.
Next, they will be distributed among the Rx and Tx stages by using line-up analysis (or assigned to the TRx blocks directly, like LO phase noise). Your design should match the contemporary CMOS technology so the detailed block specs should reflect the performances of the Rx/Tx blocks reported in literature (see Testbenches, Sec.3).
This TRx is supposed to implement direct up-conversion for Tx and Low-IF architecture for Rx that is a good choice in terms of the possible circuit integration.
Once all the TRx blocks are specified your design should be verified by simulation. For this purpose you should develop adequate models of the Rx and Tx and simulate them using ADS™ software. Should some TRx specs go beyond limits, corrections in your design will be necessary.

Table 1. Transceiver specifications

Transceiver			
TRx type		Full duplex (FDD)	
Modulation		16-QAM (with raised cosine shaping)	
Channel BW /Spacing		600 kHz	
Data rate		150 kb/sec	
Receiver		**Transmitter**	
Rx architecture	Low-IF	Tx architecture	Zero-IF
Rx band	1900-1960 MHz	Tx band	1820-1880 MHz
Sensitivity	-95dBm / BER≤10^{-3}	Max output power	27dBm (500mW)
Max input signal	-25dBm	Min output power	-7dBm
Intermodulation IIP3	2×-43dBm @ 1200 &2400kHz offset, S_{in}= -92dBm /BER≤10^{-3}	Output power switch step	5dB
Adjacent channel selectivity	15dBc/ S_{in}=-92dBm /BER≤10^{-3}	$ACPR_{Adj}$	-38dBc/30kHz (centered in channel)

Alternate channel selectivity	40dBc/ S_{in}=-92dBm /BER≤10^{-3}	$ACPR_{Alt}$	-50dBc/30kHz (centered in channel)
Blocking (in band)	56dBc @ 0.6, …3MHz S_{in}=-92dBm /BER≤10^{-3}	EVM (modulation accuracy)	8%
Blocking (in band)	66dBc @ >3MHz S_{in}=-92dBm /BER≤10^{-3}		

Design procedure

I. Receiver part

The design procedure of the Rx part can be performed as follows.

1. **Calculation of the reference noise figure (NF).** A reserve should be taken.
2. **Linearity requirement on IIP_3.** Here, the effect of the Rx noise floor, local oscillator (LO) phase noise (PN), and leakage by own Tx should be included Recall that only a limited isolation is provided by the duplexer and also the Tx signal can leak to LO port of the down-conversion mixer. Reasonable values of PN, LO spurs and isolation between Tx and Rx should be chosen. Additionally, as it is a low-IF receiver the image contribution according to limited image rejection must be included as well.
3. **Linearity requirement on IIP_2 and blocking**. To estimate this spec the down-conversion mixer should be addressed as it is the main contributor of IM2 distortions in a Low-IF receiver. For this purpose the gain of the Rx stages preceding the down-converter should be specified (at least roughly at this step). Not only the interference (blockers) but also the Tx leakage to Rx input and the LO port should be considered in this case (Tx is all the time on). The blockers/Tx leakage can be modeled as two-tone signals. Observe that the required IP2 can largely surpass directly achievable figures so an IP2 calibration technique should be put in perspective.
4. **Selectivity requirement**. Here, the adjacent/alternate channel effect on the wanted signal (wanted signal) must be verified in terms of the PN and LO spurious emission.
5. **Receiver gain and automatic gain control (AGC).** Observe that AGC introduced at BB (in I and Q branches) tends to increase the IQ mismatch in the Rx, so a combination of AGC implemented at RF and BB is an option. For practical reasons it would be a stepwise AGC which provides a few levels of gain. Observe that for reduced gain the amplifier linearity improves. Besides, the channel filter rejection helps to limit the ADC dynamic range. Use, however, a low-order filter to simplify the analog front-end. The ADC dynamic range (resolution) should be chosen according to the channel filter rejection and the blocking profile.

6. **Architecture specification and system line-up analysis**. Recall that there are different variants of the Low-IF receiver. After the Rx architecture is specified, including passives between TRx and antenna and ADCs, then the Rx gain, NF and IIP3 can be distributed among the Rx blocks. Observe that the isolation between Tx and Rx provided by a duplexer is usually not sufficient, so an extra SAW filter would be required at the Rx frontend. An active or passive mixer can be used. Recall that passive mixers have been appreciated for their low 1/f noise.
   The line-up analysis can be supported by Exel™ or Matlab™ programs to facilitate calculations that are usually performed in an iterative way. For simplicity assume the Rx blocks are impedance matched (or their individual specs were measured under conditions that reflect the actual loading in the Rx chain). Note that no unique solution exists in this case. You should avoid extreme figures when exploring the design space as they might be difficult to achieve in practice, power-hungry, and also costly. Rather, try to use typical values for gain, NF, IIP3 of the Rx blocks in a given technology. Also the phase noise of the frequency synthesizer (LO) should not be extremely low.
   In this project basically we stick to CMOS technology. If you find e.g. 180nm CMOS is not sufficient, you can move to 130nm or 90nm. Going more into details you should compare with the reported designs what the typical and extreme spec figures are. Your design should match the real technology (see Testbenches, Sec.3).
   As a result minimum performance values of all the Rx blocks should be derived.

7. **Receiver performance verification**. Once the line-up analysis is completed the Rx performance should be verified. For this purpose you can develop an ADS™ high-level model of your Rx, where performances of all the Rx blocks including LO are well defined. Some blocks can be simplified, specifically AGC can be replaced by fixed gain amplifiers, while A/D conversion can be omitted in this model for simplicity.
   Next, the Rx model would be exposed to all the tests (for sensitivity, linearity, interference, phase noise effect, etc.) discussed above in p.1-5. Intermodulation effects should be verified under LO phase noise and spurs. As it is cumbersome to model the LO spurious content, instead the PN level can be raised accordingly. While IP3 can be verified by 2-tone test, for IP2 the blockers should be used. A blocker can be modeled as closely spaced two- or multiple tones. Remember that your TRx operates in full-duplex, so the Tx is all the time on and so is its leakage that can be modeled by attenuators connecting Tx (as a simple source) with Rx input and LO port as well. The Tx noise can be reflected by increased NF of the duplexer. Adj/Alt channel selectivity should be verified like blockers (including PN and IM2 distortion). Finally, the IQ imbalance and Tx leakage should be verified. That is, the tests should be rerun for typical IQ mismatch values (such as 2-3deg and 0.5-1dB). Note that in practice, such a mismatch can be reduced by correction techniques but not eliminated completely.
   For each test the ADS simulation modes and conditions should be chosen appropriately. Observe that in most cases a measurement of the output SNR or

SNDR would be sufficient to verify the Rx correctness. Alternatively, the BER measurement can be used but it is usually more CPU intensive and the test setup requires tuning for delay as well.
Should SNR or SNDR go beyond limits in some tests, corrections in your design will be necessary until all the tests are passed.

II. Transmitter part
The design procedure of the Tx part can be performed as follows.

1. **Estimation of the modulation accuracy EVM**. Here, the contribution of the LO phase noise can be calculated directly. Contributions by other factors such as ISI, carrier leakage, nonlinearities, etc. would be limited by the target EVM.
2. **Adjacent /Alternate channel power and linearity**. Here, the transmitter OIP3 and OIP5 will be estimated to meet the ACPR requirements. The minimum compression P_{1dB} can be estimated directly from P_{Tx} max, but OIP3 is likely to impose more stringent condition on P_{1dB}.
3. **Transmitter gain, AGC, and DACs**. The Tx output stages (esp. PA) can be supplied using a higher voltage and it is more practical to discuss Tx gain in terms of power rather than voltage. To save power of the mobile Tx the base station would command the Tx to adjust power gain appropriately. Stepwise gain control can be introduced at RF in a PA driver and PA rather than at analog BB (extra DACs can be used for this purpose). Some gain control introduced at BB is an option.
   The DAC dynamic range and operation frequency should be chosen with respect to the BB signal and also the possible gain control.
4. **Architecture specification and line-up analysis** (proceed like for Rx).
5. **Transmitter performance verification**. Once an ADS model is set up the tests for EVM and ACPR should be run. DAC modeling and gain control can be excluded from the simulation model for simplicity.
   All significant specs (esp. nonlinearities, PN, IQ imbalance) should be included. Also the effect of carrier leakage should be verified and its effect on constellation should be shown. Under all conditions the EVM and ACPR should be met.
   Should your Tx fail some tests, appropriate revisions will be necessary.

Supervision and reporting

The project is supervised by your TAs.
The design work should run in two stages. In the first stage the Rx/Tx system analysis including the line-up analysis should be completed and the detailed results summarized in Report_1 (following p.1-6 for Rx and p.1-4 for Tx).
When Report_1 is approved by your TAs you should develop the Rx and Tx model in ADS™ to verify the TRx design by simulation as indicated in p.7 for Rx and p.5 for Tx according to design specs defined in Tab.1.

When all the tests are successfully completed the final report (Report_2) should be prepared and handed-in to the supervisors. Both reports should present good technical quality. Poor-quality reports will not be accepted.

The final report is due by November 15th 2012.