ESP8689 Datasheet

Espressif Systems

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About This Guide

This document provides introduction to the specifications of ESP8689 hardware.

The document structure is as follows:

Chapter	Title	Subject
Chapter 1	Overview	An overview of ESP8689, including featured solutions and basic protocols
Chapter 2	Pin Definitions	Introduction to the pin layout and descriptions
Chapter 3	Functional Description	Description of the major functional modules
Chapter 4	Peripherals	Description of the peripherals integrated on ESP8689
Chapter 5	Electrical Characteristics	The electrical characteristics and data of ESP8689
Chapter 6	Package Information	The package details of ESP8689

Release Notes

Date	Version	Release notes
2016.10	V1.0	First release.
2016.11	V1.1	Added Available GPIO Interfaces of ESP8689 for Expansion.
2016.12	V1.2	• Updated Table 1; • Added description of the strapping pin MTDI/GPIO12 in Section 2.4.
2017.05	V1.3	• Changed the Maximum drive capability in Table 5 from 12 mA to 80 mA; • Changed the input impedance value of 50Ω in Table 7 Wi-Fi Radio Characteristics to output impedance value of 30+j10Ω.
2017.06	V1.4	• Changed the input power supply range of CPU/RTC IO to 1.8V ~ 3.6V; • Changed the output power supply range of VDD_SDIO to 1.8V or the same voltage as VDD3P3_RTC; • Updated the note in Section 2.3 Power Scheme; • Updated Table 5 Absolute Maximum Ratings; • Added Documentation Change Notification.

Documentation Change Notification

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1. Overview

ESP8689 is a single chip 2.4 GHz Wi-Fi and Bluetooth combo chip designed with TSMC ultra low power 40 nm technology. It is designed and optimized for the best power performance, RF performance, robustness, versatility, features and reliability, for a wide variety of applications, and different power profiles.

1.1 Featured Solutions

1.1.1 Ultra Low Power Solution

ESP8689 is designed for mobile devices. It has many features of the state-of-the-art low power chips, including fine resolution clock gating, power modes, and dynamic power scaling.

Note:
For more information, refer to Section 3.4 RTC and Low-Power Management.

1.1.2 Complete Integration Solution

ESP8689 is the most integrated solution for Wi-Fi + Bluetooth applications in the industry with less than 16 external components. ESP8689 integrates the antenna switch, RF balun, power amplifier, low noise receive amplifier, filters, and power management modules. As such, the entire solution occupies minimal Printed Circuit Board (PCB) area.

ESP8689 uses CMOS for single-chip fully-integrated radio and baseband, and also integrates advanced calibration circuitries that allow the solution to dynamically adjust itself to remove external circuit imperfections or adjust to changes in external conditions.

As such, the mass production of ESP8689 solutions does not require expensive and specialized Wi-Fi test equipment.

1.2 Basic Protocols

1.2.1 Wi-Fi

- 802.11 b/g/n/e/i
- 802.11 n (2.4 GHz), up to 150 Mbps
- 802.11 e: QoS for wireless multimedia technology
- WMM-PS, UAPSD
- A-MPDU and A-MSDU aggregation
- Block ACK
- Fragmentation and defragmentation
- Automatic Beacon monitoring/scanning
- 802.11 i security features: pre-authentication and TSN
- Wi-Fi Protected Access (WPA)/WPA2/WPA2-Enterprise/Wi-Fi Protected Setup (WPS)

- Infrastructure BSS Station mode/SoftAP mode
- Wi-Fi Direct (P2P), P2P Discovery, P2P Group Owner mode and P2P Power Management
- UMA compliant and certified
- Antenna diversity and selection

Note:
For more information, refer to Section 3.2 Wi-Fi.

1.2.2 Bluetooth

- Compliant with Bluetooth v4.2 BR/EDR and BLE specification
- Class-1, class-2 and class-3 transmitter without external power amplifier
- Enhanced power control
- +10 dBm transmitting power
- NZIF receiver with -98 dBm sensitivity
- Adaptive Frequency Hopping (AFH)
- Standard HCI based on SDIO/SPI/UART
- High speed UART HCI, up to 4 Mbps
- BT 4.2 controller stack
- Bluetooth Low Energy (BLE)
- CVSD and SBC for audio codec
- Bluetooth Piconet and Scatternet

1.3 Block Diagram

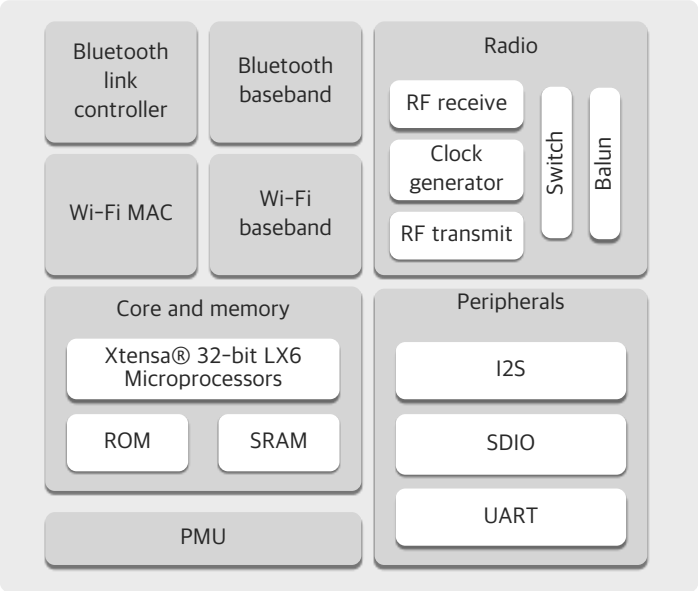


Figure 1: Function Block Diagram

2. Pin Definitions

2.1 Pin Layout

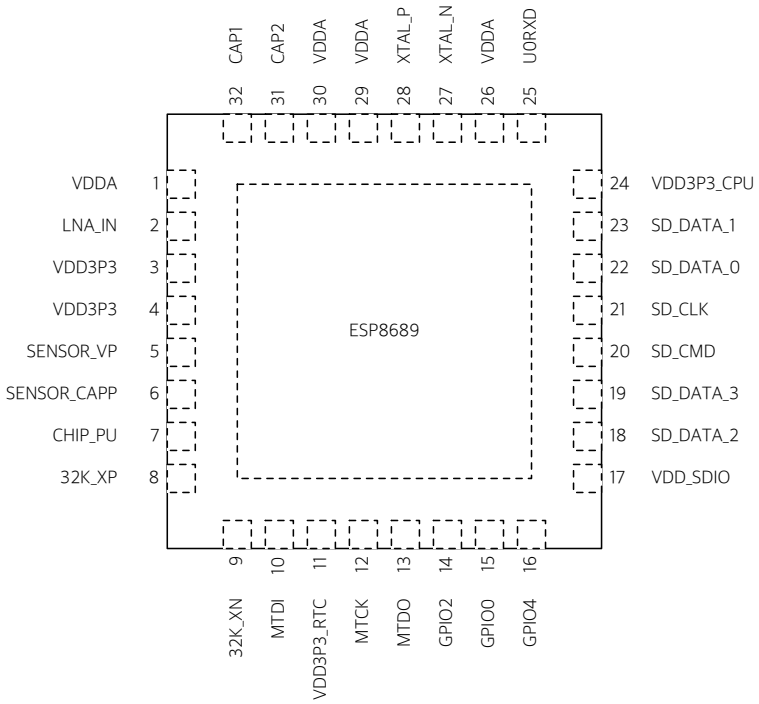


Figure 2: ESP8689 Pin Layout

2.2 Pin Description

Table 1: Pin Description

Name	No.	Type	Function
Analog			
VDDA	1	P	Analog power supply (2.3V ~ 3.6V)
LNA_IN	2	I/O	RF input and output
VDD3P3	3	P	Amplifier power supply (2.3V ~ 3.6V)
VDD3P3	4	P	Amplifier power supply (2.3V ~ 3.6V)
VDD3P3_RTC			
SENSOR_VP	5	I	GPIO36
SENSOR_CAPP	6	I	GPIO37
CHIP_PU	7	I	Chip Enable (Active High) High: On, chip works properly Low: Off, chip works at the minimum power Note: Do not leave CHIP_PU pin floating
32K_XP	8	I/O	GPIO32
32K_XN	9	I/O	GPIO33
MTDI	10	I/O	GPIO12, MTDI

Name	No.	Type	Function
VDD3P3_RTC	11	P	Input power supply for RTC IO (1.8V ~ 3.6V)
MTCK	12	I/O	GPIO13 MTCK
MTDO	13	I/O	GPIO15, MTDO
GPIO2	14	I/O	GPIO2
GPIO0	15	I/O	GPIO0
GPIO4	16	I/O	GPIO4
VDD_SDIO			
VDD_SDIO	17	P	Output power supply: 1.8V or the same voltage as VDD3P3_RTC
SD_DATA_2	18	I/O	GPIO9, SD_DATA2, SPIHD, U1RXD
SD_DATA_3	19	I/O	GPIO10, SD_DATA3, SPIWP, U1TXD
SD_CMD	20	I/O	GPIO11, SD_CMD, SPICS0, U1RTS
SD_CLK	21	I/O	GPIO6, SD_CLK, SPICLK, U1CTS
SD_DATA_0	22	I/O	GPIO7, SD_DATA0, SPIQ
SD_DATA_1	23	I/O	GPIO8, SD_DATA1, SPID
VDD3P3_CPU			
VDD3P3_CPU	24	P	Input power supply for CPU IO (1.8V ~ 3.6V)
U0RXD	25	I/O	GPIO3
Analog			
VDDA	26	P	Analog power supply (2.3V ~ 3.6V)
XTAL_N	27	O	External crystal output
XTAL_P	28	I	External crystal input
VDDA	29	P	Analog power supply (2.3V ~ 3.6V)
VDDA	30	P	Analog power supply (2.3V ~ 3.6V)
CAP2	31	I	Connects with a 3.3 nF capacitor and 20 kΩ resistor in parallel to CAP1
CAP1	32	I	Connects with a 10 nF series capacitor to ground

2.3 Power Scheme

ESP8689 digital pins are divided into two different power domains:

- VDD3P3_RTC
- VDD3P3_CPU

VDD3P3_RTC is also the input power supply for RTC and CPU. VDD3P3_CPU is also the input power supply for CPU.

Note:

- CHIP_PU mst be activated after the 3.3V rails have been brought up. The recommended delay time (T) is given by the parameter of the RC circuit. For reference design, please refer to Figure **ESP-WROOM-32 Peripheral Schematics** in the *ESP-WROOM-32 Datasheet*.
- CHIP_PU is used to reset the chip. The input level should be below 0.6V and stays for at least 200 μs.
- The operating voltage for ESP8689 ranges from 2.3V to 3.6V. When using a single power supply, the recommended voltage of the power supply is 3.3V, and its recommended output current is 500 mA or more.

2.4 Strapping Pins

ESP8689 has four strapping pins:

- GPIO0: internal pull-up
- GPIO2: internal pull-down
- MTDO/GPIO15: internal pull-up
- MTDI/GPIO12: internal pull-down

Software can read the value of these three bits from the register "GPIO_STRAPPING".

During the chip power-on reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device boot mode, the operating voltage of VDD_SDIO and other system initial settings.

Each strapping pin is connected with its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impendence, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or apply the host MCU's GPIOs to control the voltage level of these pins when powering on ESP8689.

After reset, the strapping pins work as the normal functions pins.

Refer to Table 2.4 for detailed boot modes configuration by strapping pins.

Table 2: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)			
Pin	Default	3.3V	1.8V
MTDI/GPIO12	Pull-down	0	1
Booting Mode			
Pin	Default	Download Boot	
GPIO0	Pull-up	0	
GPIO2	Pull-down	0	
Timing of SDIO Slave			
Pin	Default	Falling-edge Input Rising-edge Output	Rising-edge Input Rising-edge Output
MTDO/GPIO15	Pull-up	0	1

3. Functional Description

This chapter describes the functions integrated in ESP8689.

3.1 Radio

The ESP8689 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

3.1.1 2.4 GHz Receiver

The 2.4 GHz receiver down-converts the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits and baseband filters are integrated within ESP8689.

3.1.2 2.4 GHz Transmitter

The 2.4 GHz transmitter up-converts the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high powered Complementary Metal Oxide Semiconductor (CMOS) power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling state-of-the-art performance of delivering +20.5 dBm of average power for 802.11b transmission and +17 dBm for 802.11n transmission.
Additional calibrations are integrated to cancel any imperfections of the radio, such as:

- Carrier leakage
- I/Q phase matching
- Baseband nonlinearities
- RF nonlinearities
- Antenna matching

These built-in calibration routines reduce the amount of time and required for product test and make test equipment unnecessary.

3.1.3 Clock Generator

The clock generator generates quadrature 2.4 GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on the chip, including all inductors, varactors, filters, regulators and dividers. The clock generator has built-in calibration and self test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best performance of the receiver and transmitter.

3.2 Wi-Fi

ESP8689 implements TCP/IP, full 802.11 b/g/n/e/i WLAN MAC protocol, and Wi-Fi Direct specification. It supports Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF) and P2P group operation compliant with the latest Wi-Fi P2P protocol.

Passive or active scanning, as well as the P2P discovery procedure are performed autonomously when initiated by appropriate commands. Power management is handled with minimum host interaction to minimize active duty period.

3.2.1 Wi-Fi Radio and Baseband

The ESP8689 Wi-Fi Radio and Baseband support the following features:

- 802.11b and 802.11g data-rates
- 802.11n MCS0-7 in both 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μs guard-interval
- Data-rate up to 150 Mbps
- Receiving STBC 2x1
- Up to 21 dBm transmitting power
- Adjustable transmitting power
- Antenna diversity and selection (software-managed hardware)

3.2.2 Wi-Fi MAC

The ESP8689 Wi-Fi MAC applies low level protocol functions automatically as follows:

- Request To Send (RTS), Clear To Send (CTS) and Acknowledgement (ACK/BA)
- Fragmentation and defragmentation
- Aggregation AMPDU and AMSDU
- WMM, U-APSD
- 802.11 e: QoS for wireless multimedia technology
- CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4) and CRC
- Frame encapsulation (802.11h/RFC 1042)
- Automatic beacon monitoring/scanning

3.2.3 Wi-Fi Firmware

The ESP8689 Wi-Fi Firmware provides the following functions:

- Clock/power gating combined with 802.11-compliant power management dynamically adapted to current connection condition providing minimal power consumption
- Adaptive rate fallback algorithm sets the optimal transmission rate and transmit power based on actual Signal Noise Ratio (SNR) and packet loss information
- Automatic retransmission and response on MAC to avoid packet discarding on slow host environment

3.2.4 Packet Traffic Arbitration (PTA)

ESP8689 has a configurable Packet Traffic Arbitration (PTA) that provides flexible and exact timing Bluetooth co-existence support. It is a combination of both Frequency Division Multiplexing (FDM) and Time Division Multiplexing (TDM), and coordinates the protocol stacks.

- It is preferable that Wi-Fi works in the 20 MHz bandwidth mode to decrease its interference with BT.
- BT applies AFH (Adaptive Frequency Hopping) to avoid using the channels within Wi-Fi bandwidth.
- Wi-Fi MAC limits the time duration of Wi-Fi packets, and does not transmit the long Wi-Fi packets by the lowest data-rates.
- Normally BT packets are of higher priority than normal Wi-Fi packets.
- Protect the critical Wi-Fi packets, including beacon transmission and receiving, ACK/BA transmission and receiving.
- Protect the highest BT packets, including inquiry response, page response, LMP data and response, park beacons, the last poll period, SCO/eSCO slots, and BLE event sequence.
- Wi-Fi MAC apply CTS-to-self packet to protect the time duration of BT transfer.
- In the P2P Group Own (GO) mode, Wi-Fi MAC applies a Notice of Absence (NoA) packet to disable Wi-Fi transfer to reserve time for BT.
- In the STA mode, Wi-Fi MAC applies a NULL packet with the Power-Save bit to disable WiFi transfer to reserve time for BT.

3.3 Bluetooth

ESP8689 integrates Bluetooth link controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packets processing, bit stream processing, frequency hopping, etc.

3.3.1 Bluetooth Radio and Baseband

The ESP8689 Bluetooth Radio and Baseband support the following features:

- Class-1, class-2 and class-3 transmit output powers and over 30 dB dynamic control range
- $\pi/4$ DQPSK and 8 DPSK modulation
- High performance in NZIF receiver sensitivity with over 98 dB dynamic range
- Class-1 operation without external PA
- Internal SRAM allows full speed data transfer, mixed voice and data, and full piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping
- ACL, SCO, eSCO and AFH
- A-law, μ-law and CVSD digital audio CODEC in PCM interface
- SBC audio CODEC
- Power management for low power applications
- SMP with 128-bit AES

3.3.2 Bluetooth Interface

- Provides UART HCI interface, up to 4 Mbps
- Provides SDIO / SPI HCI interface
- Provides PCM / I2S audio interface

3.3.3 Bluetooth Stack

The Bluetooth stack of ESP8689 is compliant with Bluetooth v4.2 BR / EDR and BLE specification.

3.3.4 Bluetooth Link Controller

The link controller operates in three major states: standby, connection and sniff. It enables multi connection and other operations like inquiry, page, and secure simple pairing, and therefore enables Piconet and Scatternet. Below are the features:

- Classic Bluetooth
  - Device Discovery (inquiry and inquiry scan)
  - Connection establishment (page and page scan)
  - Multi connections
  - Asynchronous data reception and transmission
  - Synchronous links (SCO/eSCO)
  - Master/Slave Switch
  - Adaptive Frequency Hopping and Channel assessment
  - Broadcast encryption
  - Authentication and encryption
  - Secure Simple Pairing
  - Multi-point and scatternet management
  - Sniff mode
  - Connectionless Slave Broadcast (transmitter and receiver)
  - Enhanced power control
  - Ping
- Bluetooth Low Energy
  - Advertising
  - Scanning
  - Multiple connections
  - Asynchronous data reception and transmission
  - Adaptive Frequency Hopping and Channel assessment
  - Connection parameter update
  - Date Length Extension

- Link Layer Encryption
- LE Ping

3.4 Low-Power Management

With the advanced power management technologies, the power mode switches between the active mode and sleep mode during the association sleep pattern. The CPU, Wi-Fi, Bluetooth, and radio are woken up at predetermined intervals to keep Wi-Fi/BT connections alive, with the current of 0.9 mA@DTIM3 and 1.2 mA@DTIM1. (see Table 3).

- Active mode: The chip radio is powered on. The chip can receive, transmit, or listen.
- Sleep mode: The CPU is paused. The RTC and ULP-coprocessor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.

Table 3: Power Consumption by Power Modes

Power mode	Description	Power consumption
Active (RF working)	Wi-Fi Tx packet 13 dBm ~ 21 dBm	160 ~ 260 mA
	Wi-Fi / BT Tx packet 0 dBm	120 mA
	Wi-Fi / BT Rx and listening	80 ~ 90 mA
	Association sleep pattern (by sleep)	0.9 mA@DTIM3, 1.2 mA@DTIM1
Sleep	-	0.8 mA

Note:
For more information about RF power consumption, refer to Section 5.2 RF Power Consumption Specifications.

4. Peripherals

4.1 General Purpose Input / Output Interface (GPIO)

ESP8689 has 32 GPIO pins which can be assigned to various functions by programming the appropriate registers. There are several kinds of GPIOs: digital only GPIOs, analog enabled GPIOs, capacitive touch enabled GPIOs, etc. Analog enabled GPIOs can be configured as digital GPIOs. Capacitive touch enabled GPIOs can be configured as digital GPIOs.

Each digital enabled GPIO can be configured to internal pull-up or pull-down, or set to high impedance. When configured as an input, the input value can be read through the register. The input can also be set to edge-trigger or level-trigger to generate CPU interrupts. In short, the digital IO pins are bi-directional, non-inverting and tristate, including input and output buffer with tristate control.

These pins can be multiplexed with other functions, such as the SDIO interface, UART, SI, etc. For low power operations, the GPIOs can be set to hold their states.

Some pins can be used to expand the GPIO interfaces. The host can access to these pins directly as if they were the host's own GPIO pins. For those GPIO interfaces that can be expanded, refer to Table 4.

Table 4: Available GPIO Interfaces of ESP8689 for Expansion

No.	Name	Electrical level	Default pin state on power-up (before downloading software)	Required function	Equivalent GPIO pad number
Available GPIOs recommended for normal usage and expansion					
10	MTDI	-	Input, internal pull-down	-	GPIO12 (supports internal pull-up and internal pull-down)
12	MTCK	-	Input, high impedance	-	GPIO13 (supports internal pull-up and internal pull-down)
16	GPIO4	-	Input, internal pull-down	-	GPIO4 (supports internal pull-up and internal pull-down)
23	SD_DATA_1	-	Input, internal pull-up	-	GPIO8 (supports internal pull-up and internal pull-down)
25	U0RXD	-	Input, internal pull-up	-	GPIO3 (supports internal pull-up and internal pull-down)
Available GPIOs not recommended for regular use. Please note the electrical levels.					
13	MTDO	Fixed level	Input, internal pull-up	-	GPIO15 (supports internal pull-up and internal pull-down)
14	GPIO2	Low level	Input, internal pull-down	-	GPIO2 (supports internal pull-up and internal pull-down)
15	GPIO0	Low level	Input, internal pull-up	-	GPIO0 (supports internal pull-up and internal pull-down)
GPIOs not available for expansion					
18	SD_DATA_2	-	Input, internal pull-up	-	Unavailable
19	SD_DATA_3	-	Input, internal pull-up	SPI_CS_INT	Unavailable
20	SD_CMD	-	Input, internal pull-up	SPI_MOSI	Unavailable
21	SD_CLK	-	Input, internal pull-up	SPI_CLK	Unavailable
22	SD_DATA_0	-	Input, internal pull-up	SPI_MISO	Unavailable

Note:

1. GPIO2 must be kept at a low level during power-up. If GPIO2 is not needed, it can be pulled down internally and left in a floating state externally. If GPIO2 is not used for expanding GPIO0, the external circuit should not have a low impedance when the Wi-Fi chip is powered up.
2. GPIO0 must be kept at a low level during power-up. It should be controlled by the external circuit during power-up.
3. During power-up, the external circuit should pull MTDO high or low according to the delay line requirement of SDIO. Two pins can be pulled up in the chip by default.
4. On power-up, before the software is downloaded, Pin No.10, 12, 16, 26 and 8 ~ 22 are at input state (Besides MTCK, other pins have enabled pull-up or pull-down resistors). After downloading software for the first time, the pins mentioned above can be configured as input, input with internal pull-up / pull-down, output high level or output low level.

4.2 SDIO/SPI Slave Controller

ESP8689 integrates an SD device interface that conforms to the industry-standard SDIO Card Specification Version 2.0 and allows a host controller to access the SoC device using the SDIO bus interface and protocol. ESP8689 acts as the slave on the SDIO bus. The host can access SDIO interface registers directly and can access shared memory via a DMA engine, thus maximizing performance without engaging the processor cores.

The SDIO/SPI slave controller supports the following features:

- SPI, 1-bit SDIO, and 4-bit SDIO transfer modes over the full clock range of 0 to 50 MHz.
- Configurable sampling and driving clock edge
- Special registers for direct access by host
- Interrupt to host for initiating data transfer
- Allows card to interrupt host
- Automatic loading of SDIO bus data and automatic discarding of padding data
- Block size of up to 512 bytes
- Interrupt vectors between the host and the slave to allow both to interrupt each other
- Linked List DMA for data transfer

4.3 Universal Asynchronous Receiver Transmitter (UART)

ESP8689 has three UART interfaces, i.e., UART0, UART1 and UART2, which provide asynchronous communication (RS232 and RS485) and IrDA support, and communicate at up to 5 Mbps. UART provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All of the interfaces can be accessed by the DMA controller or directly by CPU.

4.4 I2S Interface

Two standard I2S interfaces are available in ESP8689. They can operate in master or slave mode, in full duplex and half-duplex communication modes, and can be configured to operate with an 8-/16-/32-/40-/48-/64-bit resolution as input or output channels. BCK clock frequency from 10 kHz up to 40 MHz are supported. When one or both of the I2S interfaces are configured in the master mode, the master clock can be output to the external CODEC.

Both of the I2S interfaces have dedicated DMA controllers. PDM and BT PCM interfaces are supported.

5. Electrical Characteristics

Note:
The specifications in this chapter have been tested under the following general condition: VDD = 3.3V, T_A = 27°C, unless otherwise specified.

5.1 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Power supply	VDD	2.3	3.3	3.6	V
Input low voltage	V_{IL}	-0.3	-	0.25×V_{IO}	V
Input high voltage	V_{IH}	0.75×V_{IO}	-	V_{IO}+0.3	V
Input leakage current	I_{IL}	-	-	50	nA
Output low voltage	V_{OL}	-	-	0.1×V_{IO}	V
Output high voltage	V_{OH}	0.8×V_{IO}	-	-	V
Input pin capacitance	C_{pad}	-	-	2	pF
VDDIO	V_{IO}	1.8	3.3	3.6	V
CMOS threshold voltage	V_{TH}	-	0.5 x V_{IO}	-	V
Maximum drive capability	I_{MAX}	-	-	40	mA
Storage temperature range	T_{STR}	-40	-	150	°C
Operating temperature range	T_{OPR}	-40	-	125	°C

5.2 RF Power Consumption Specifications

The current consumption measurements are conducted with 3.0V supply and 25°C ambient, at antenna port. All the transmitters' measurements are based on 90% duty cycle and continuous transmit mode.

Table 6: RF Power Consumption Specifications

Mode	Min	Typ	Max	Unit
Transmit 802.11b, DSSS 1 Mbps, POUT = +19.5 dBm	-	225	-	mA
Transmit 802.11b, CCK 11 Mbps, POUT = +18.5 dBm	-	205	-	mA
Transmit 802.11g, OFDM 54 Mbps, POUT = +16 dBm	-	160	-	mA
Transmit 802.11n, MCS7, POUT = +14 dBm	-	152	-	mA
Receive 802.11b, packet length = 1024 bytes, -80 dBm	-	85	-	mA
Receive 802.11g, packet length = 1024 bytes, -70 dBm	-	85	-	mA
Receive 802.11n, packet length = 1024 bytes, -65 dBm	-	80	-	mA
Receive 802.11n HT40, packet length = 1024 bytes, -65 dBm	-	80	-	mA

5.3 Wi-Fi Radio

Table 7: Wi-Fi Radio Characteristics

Description	Min	Typical	Max	Unit
Input frequency	2412	-	2484	MHz
Output impedance	-	35+j10	-	Ω
Input reflection	-	-	-10	dB
Output power of PA for 72.2 Mbps	15.5	16.5	17.5	dBm
Output power of PA for 11b mode	19.5	20.5	21.5	dBm
DSSS, 1 Mbps	-	-98	-	dBm
CCK, 11 Mbps	-	-91	-	dBm
OFDM, 6 Mbps	-	-93	-	dBm
OFDM, 54 Mbps	-	-75	-	dBm
HT20, MCS0	-	-93	-	dBm
HT20, MCS7	-	-73	-	dBm
HT40, MCS0	-	-90	-	dBm
HT40, MCS7	-	-70	-	dBm
MCS32	-	-89	-	dBm
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7	-	20	-	dB

5.4 Bluetooth Radio

5.4.1 Receiver - Basic Data Rate

Table 8: Receiver Characteristics-Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @0.1% BER	-	-	-98	-	dBm
Maximum received signal @0.1% BER	-	0	-	-	dBm
Co-channel C/I	-	-	+7	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-	-6	dB
	F = F0 - 1 MHz	-	-	-6	dB
	F = F0 + 2 MHz	-	-	-25	dB
	F = F0 - 2 MHz	-	-	-33	dB
	F = F0 + 3 MHz	-	-	-25	dB
	F = F0 - 3 MHz	-	-	-45	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

5.4.2 Transmitter - Basic Data Rate

Table 9: Transmitter Characteristics - Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	+4	+4	dBm
RF power control range	-	-	25	-	dB
20 dB bandwidth	-	-	0.9	-	MHz
Adjacent channel transmit power	F = F0 + 1 MHz	-	-24	-	dBm
	F = F0 - 1 MHz	-	-16.1	-	dBm
	F = F0 + 2 MHz	-	-40.8	-	dBm
	F = F0 - 2 MHz	-	-35.6	-	dBm
	F = F0 + 3 MHz	-	-45.7	-	dBm
	F = F0 - 3 MHz	-	-40.2	-	dBm
	F = F0 + > 3 MHz	-	-45.6	-	dBm
	F = F0 - > 3 MHz	-	-44.6	-	dBm
Δ f1$_{avg}$	-	-	-	155	kHz
Δ f2$_{max}$	-	133.7	-	-	kHz
Δ f2$_{avg}$/Δ f1$_{avg}$	-	-	0.92	-	-
ICFT	-	-	-7	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift (1 slot packet)	-	-	6	-	kHz
Drift (5 slot packet)	-	-	6	-	kHz

5.4.3 Receiver - Enhanced Data Rate

Table 10: Receiver Characteristics - Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
π/4 DQPSK					
Sensitivity @0.01% BER	-	-	-98	-	dBm
Maximum received signal @0.1% BER	-	-	0	-	dBm
Co-channel C/I	-	-	11	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-7	-	dB
	F = F0 - 1 MHz	-	-7	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
8DPSK					
Sensitivity @0.01% BER	-	-	-84	-	dBm
Maximum received signal @0.1% BER	-	0	-	-	dBm
C/I c-channel	-	-	18	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	2	-	dB
	F = F0 - 1 MHz	-	2	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-25	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-38	-	dB

5.4.4 Transmitter - Enhanced Data Rate

Table 11: Transmitter Characteristics - Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
Maximum RF transmit power	-	-	+2	-	dBm
Relative transmit control	-	-	-1.5	-	dB
π/4 DQPSK max w0	-	-	-0.72	-	kHz
π/4 DQPSK max wi	-	-	-6	-	kHz
π/4 DQPSK max |wi + w0|	-	-	-7.42	-	kHz
8DPSK max w0	-	-	0.7	-	kHz
8DPSK max wi	-	-	-9.6	-	kHz
8DPSK max |wi + w0|	-	-	-10	-	kHz
π/4 DQPSK modulation accuracy	RMS DEVM	-	4.28	-	%
	99% DEVM	-	-	30	%
	Peak DEVM	-	13.3	-	%
8 DPSK modulation accuracy	RMS DEVM	-	5.8	-	%
	99% DEVM	-	-	20	%
	Peak DEVM	-	14	-	%

Parameter	Conditions	Min	Typ	Max	Unit
In-band spurious emissions	F = F0 + 1 MHz	-	-34	-	dBm
	F = F0 - 1 MHz	-	-40.2	-	dBm
	F = F0 + 2 MHz	-	-34	-	dBm
	F = F0 - 2 MHz	-	-36	-	dBm
	F = F0 + 3 MHz	-	-38	-	dBm
	F = F0 - 3 MHz	-	-40.3	-	dBm
	F = F0 +/- > 3 MHz	-	-	-41.5	dBm
EDR differential phase coding	-	-	100	-	%

5.5 Bluetooth LE Radio

5.5.1 Receiver

Table 12: Receiver Characteristics - BLE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @0.1% BER	-	-	-98	-	dBm
Maximum received signal @0.1% BER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-10	-	-	dBm
	2000 MHz ~ 2400 MHz	-27	-	-	dBm
	2500 MHz ~ 3000 MHz	-27	-	-	dBm
	3000 MHz ~ 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-36	-	-	dBm

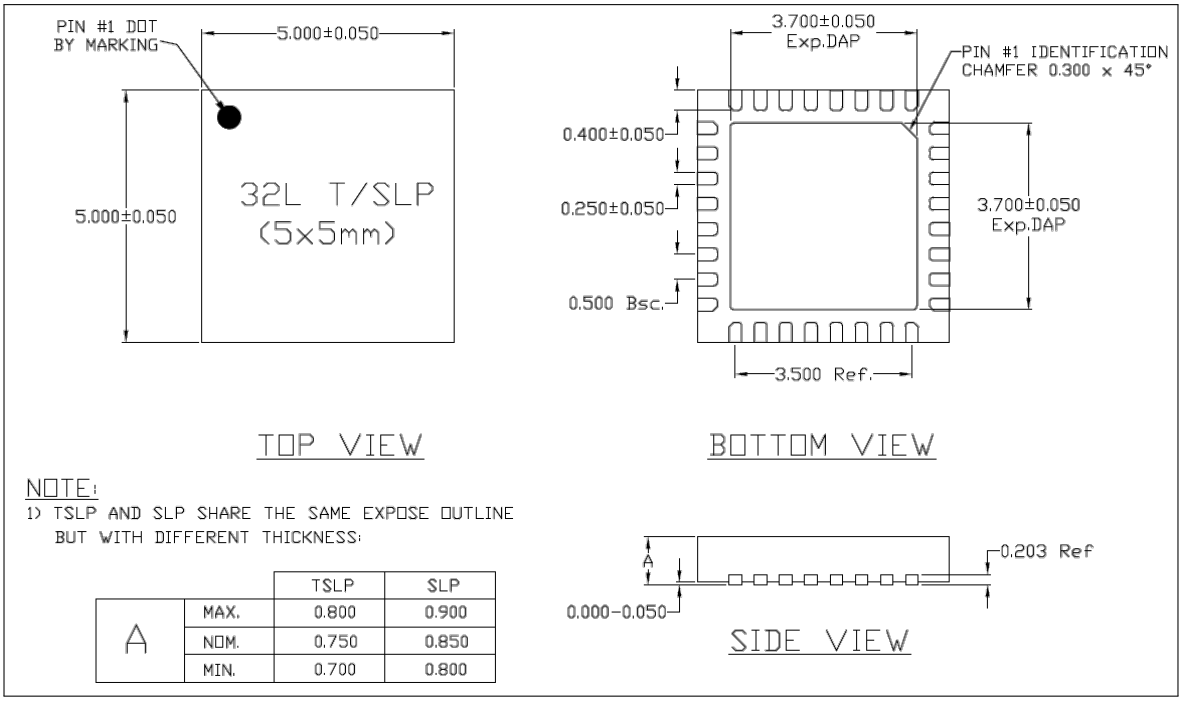
5.5.2 Transmitter

Table 13: Transmitter Characteristics - BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power	-	-	+7.5	+10	dBm
RF power control range	-	-	25	-	dB
Adjacent channel transmit power	F = F0 + 1 MHz	-	-14.6	-	dBm
	F = F0 - 1 MHz	-	-12.7	-	dBm
	F = F0 + 2 MHz	-	-44.3	-	dBm
	F = F0 - 2 MHz	-	-38.7	-	dBm
	F = F0 + 3 MHz	-	-49.2	-	dBm
	F = F0 - 3 MHz	-	-44.7	-	dBm
	F = F0 + > 3 MHz	-	-50	-	dBm

Parameter	Conditions	Min	Typ	Max	Unit
	F = F0 - > 3 MHz	-	-50	-	dBm
Δ f1$_{avg}$	-	-	-	265	kHz
Δ f2$_{max}$	-	247	-	-	kHz
Δ f2$_{avg}$/Δ f1$_{avg}$	-	-	-0.92	-	-
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	kHz/50 μs
Drift	-	-	2	-	kHz

6. Package Information



		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800

Figure 3: QFN32 (5x5 mm) Package