ESP8689 Hardware Design Guidelines

Espressif Systems

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About This Guide

ESP8689 Hardware Design Guidelines provide technical information on ESP8689.

Related Resources

For additional documentation and resources on ESP8689, please visit the website: ESP8689 Datasheet.

Release Notes

Date	Version	Release notes
2016.12	V1.0	First release.
2017.06	V1.1	• Updated Section 3.1.1.1 Digital Power Supply; • Updated Section 3.1.2 Power-on Sequence and System Reset; • Updated Section 3.1.4.1 External Clock Source (Compulsory); • Changed the input power supply range of CPU/RTC IO to 1.8V ~ 3.6V; • Added Documentation Change Notification.

Documentation Change Notification

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1. Overview

ESP8689 is a single 2.4 GHz Wi-Fi and Bluetooth combo chip designed with TSMC ultra-low power 40 nm technology. It is designed to achieve the best power performance and RF performance in a wide variety of applications and different power profiles, with robustness, versatility and reliability.

Ultra Low Power Solution

ESP8689 is designed for mobile devices. It is a state-of-the-art low power chip with fine-grained clock gating, power modes, and dynamic power scaling.

Complete Integration Solution

With only 16 external components, ESP8689 has the optimal level of integration in the industry. It integrates the complete transmit/receive RF functionality including the antenna switches, RF balun, power amplifier, low noise receive amplifier, filters, and power management modules. As such, the entire solution occupies minimal Printed Circuit Board (PCB) area.

ESP8689 uses CMOS for single-chip fully-integrated radio and baseband, and also integrates advanced calibration circuitries that allow the solution to remove external circuit imperfections or dynamically adjust to changes in external conditions. Therefore, the mass production of ESP8689 solutions does not require expensive and specialized Wi-Fi testing equipment.

1.1 Basic Protocols

1.1.1 Wi-Fi

- 802.11 b/g/n/e/i
- 802.11 n (2.4 GHz), up to 150 Mbps
- 802.11 e: QoS for wireless multimedia technology
- WMM-PS, UAPSD
- A-MPDU and A-MSDU aggregation
- Block ACK
- Fragmentation and defragmentation
- Automatic Beacon monitoring/scanning
- 802.11 i security features: pre-authentication and TSN
- Wi-Fi Protected Access (WPA)/WPA2/WPA2-Enterprise/Wi-Fi Protected Setup (WPS)
- Infrastructure BSS Station mode/SoftAP mode
- Wi-Fi Direct (P2P), P2P Discovery, P2P Group Owner mode and P2P Power Management
- UMA compliant and certified
- Antenna diversity and selection

1.1.2 Bluetooth

- Compliant with Bluetooth v4.2 BR/EDR and BLE specification
- Class-1, class-2 and class-3 transmitter without external power amplifier
- Enhanced power control
- +10 dBm transmitting power
- NZIF receiver with -98 dBm sensitivity
- Adaptive Frequency Hopping (AFH)
- Standard HCI based on SDIO/SPI/UART
- High-speed UART HCI, up to 4 Mbps
- BT 4.2 controller stack
- Bluetooth Low Energy (BLE)
- CVSD and SBC for audio codec
- Bluetooth Piconet and Scatternet

1.2 Application

- Internet music players
- Audio streaming devices
- Video streaming from camera
- Support for Wi-Fi/Bluetooth
  - Over The Top (OTT) devices
  - Tablet computers
  - Smart devices

1.3 Function Block Diagram

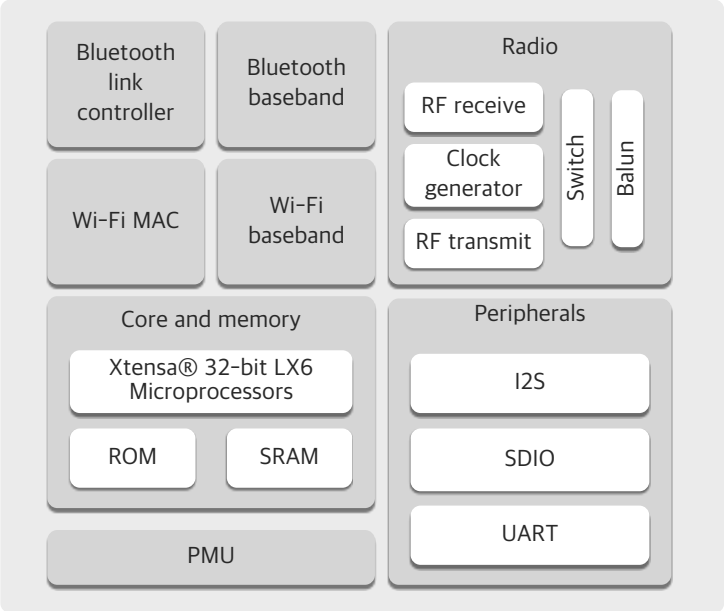

Figure 1: ESP8689 Function Block Diagram

2. Pin Definitions

2.1 Pin Layout

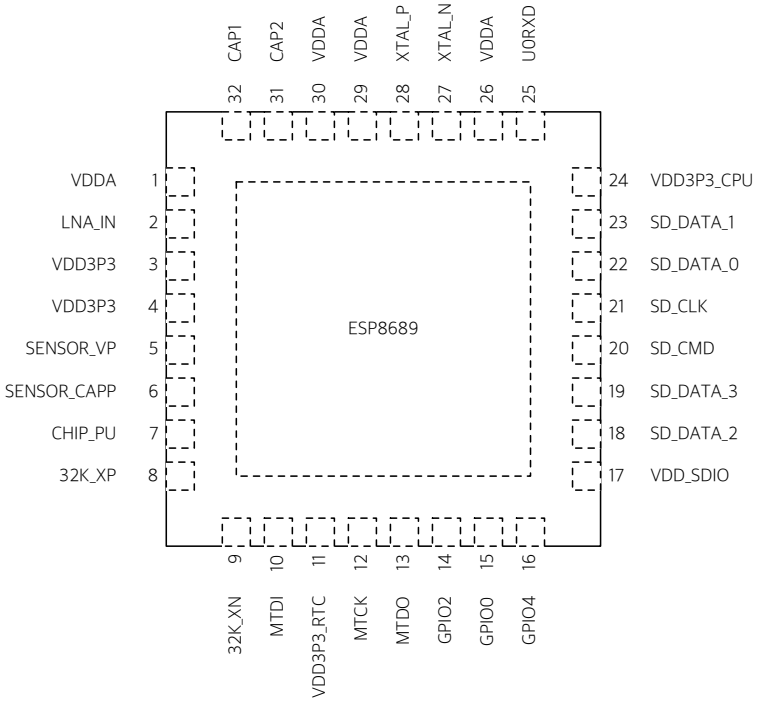

Figure 2: ESP8689 Pin Layout

2.2 Pin Description

Table 1: Pin Description

Name	No.	Type	Function
Analog			
VDDA	1	P	Analog power supply (2.3V ~ 3.6V)
LNA_IN	2	I/O	RF input and output
VDD3P3	3	P	Amplifier power supply (2.3V ~ 3.6V)
VDD3P3	4	P	Amplifier power supply (2.3V ~ 3.6V)
VDD3P3_RTC			
SENSOR_VP	5	I	GPIO36
SENSOR_CAPP	6	I	GPIO37
CHIP_PU	7	I	Chip Enable (Active High) High: On; chip works normally Low: Off; chip works at the minimum power Note: Do not leave CHIP_PU pin floating.
32K_XP	8	I/O	GPIO32
32K_XN	9	I/O	GPIO33
MTDI	10	I/O	GPIO12, MTDI
VDD3P3_RTC	11	P	RTC IO power supply input (1.8V ~ 3.6V)

Name	No.	Type	Function
MTCK	12	I/O	GPIO13, MTCK
MTDO	13	I/O	GPIO15, MTDO
GPIO2	14	I/O	GPIO2
GPIO0	15	I/O	GPIO0
GPIO4	16	I/O	GPIO4
VDD_SDIO			
VDD_SDIO	17	P	1.8V or the same voltage as VDD3P3_RTC
SD_DATA_2	18	I/O	GPIO9, SD_DATA2, SPIHD, U1RXD
SD_DATA_3	19	I/O	GPIO10, SD_DATA3, SPIWP, U1TXD
SD_CMD	20	I/O	GPIO11, SD_CMD, SPICS0, U1RTS
SD_CLK	21	I/O	GPIO6, SD_CLK, SPICLK, U1CTS
SD_DATA_0	22	I/O	GPIO7, SD_DATA0, SPIQ
SD_DATA_1	23	I/O	GPIO8, SD_DATA1, SPID
VDD3P3_CPU			
VDD3P3_CPU	24	P	CPU IO power supply input (1.8V ~ 3.6V)
U0RXD	25	I/O	GPIO3
Analog			
VDDA	26	P	Analog power supply (2.3V ~ 3.6V)
XTAL_N	27	O	External crystal output
XTAL_P	28	I	External crystal input
VDDA	29	P	Analog power supply (2.3V ~ 3.6V)
VDDA	30	P	Analog power supply (2.3V ~ 3.6V)
CAP2	31	I	Connects with a 3.3 nF capacitor and 20 kΩ resistor in parallel to CAP1
CAP1	32	I	Connects with a 10 nF series capacitor to ground
GND			
GND	33	G	Exposed ground pad

2.3 Strapping Pins

ESP8689 has four strapping pins.

- GPIO0: internal pull-up
- GPIO2: internal pull-down
- MTDO/GPIO15: internal pull-up
- MTDI/GPIO12: internal pull-down

Software can read the value of these four bits from the register ”GPIO_STRAPPING”.

During the chip power-on reset, the latches of the strapping pins sample the voltage level as strapping bits with states ”0” or ”1”, and hold these bits until the chip is powered down or shut down. The strapping bits configure the device boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected with its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impendence, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP8689.

After the reset procedure is complete, the strapping pins work as normal-function pins.

Please see Table 2 for detailed information on boot mode configuration using strapping pins.

Table 2: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)			
Pin	Default	3.3V	1.8V
MTDI/GPIO12	Pull-down	0	1
Booting Mode			
Pin	Default	Download Boot	
GPIO0	Pull-up	0	
GPIO2	Pull-down	0	
Timing of SDIO Slave			
Pin	Default	Falling-edge Input Rising-edge Output	Rising-edge Input Rising-edge Output
MTDO/GPIO15	Pull-up	0	1

3. Schematic Checklist and PCB Layout Design

ESP8689's integrated circuitry requires about 15 resistors, capacitors and inductors, and one crystal. ESP8689 integrates the complete transmit/receive RF functionality including the antenna switches, RF balun, power amplifier, low-noise receive amplifier, filters, power management module, and advanced calibration circuitries.

While the high level of integration makes the PCB design and layout process simple, the performance of the system strongly depends on system design aspects. To achieve the best overall system performance, please follow the guidelines specified in this document for circuit design and PCB layout. All the common rules associated with good PCB design still apply, and this document is not an exhaustive list of good design practices.

3.1 Schematic Checklist

ESP8689 schematics is as shown in Figure 3.

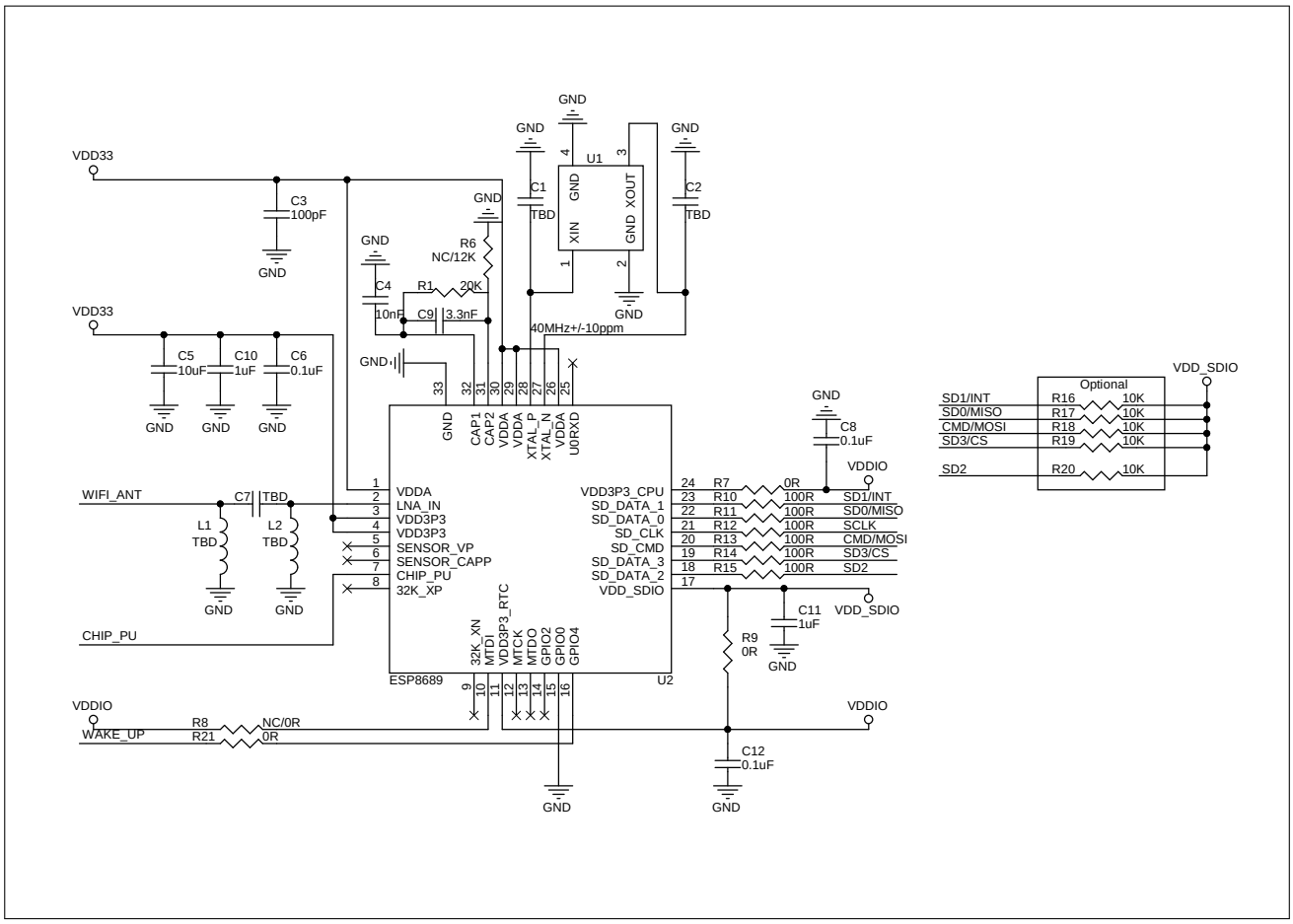

Figure 3: ESP8689 Schematics (ESP8089 Compatible)

Notice:

1. External capacitors:
   - When using ESP8689, R7, C4, R1, and C9 are populated, while R6 is not populated.
   - When using ESP8089, R7, C4, R1, and C9 are populated, and the value of R6 is 12K±1%.
2. Power supply for VDD_SDIO:
   - When using the external VDDIO power supply (3.3V or 1.8V), R8 is not populated whereas R9 is populated.
   - When using 3.3V of ESP8689's internal LDO power supply, neither R9 nor R8 is populated.
   - When using 1.8V of ESP8689's internal LDO power supply, R9 is not populated whereas R8 is populated.
3. ESP8689 supports the function of waking up the host. Do not populate R21 if the function is not needed.

Any basic ESP8689 circuit design may be broken down into six major sections:

- Power supply
- Power-on sequence and system reset
- RF
- Crystal oscillator
- SDIO/SPI interface
- External capacitors

A detailed description of these aspects follows.

3.1.1 Power Supply

3.1.1.1 Digital Power Supply

Pin11 and Pin24 are the power supply pins for RTC and CPU, respectively. The digital power supply operates in a voltage range of 1.8V ~ 3.6V. We recommend adding extra filter capacitors close to the digital power supply pins.

The internal LDO of VDD_SDIO can be used as the power supply (1.8V or the same voltage as VDD3P3_RTC) for the external circuitry, with a maximum current of about 40 mA. The user can add a 1μF filter capacitor close to VDD_SDIO. When VDD_SDIO is tied to VDD3P3_RTC, the LDO will be disabled.

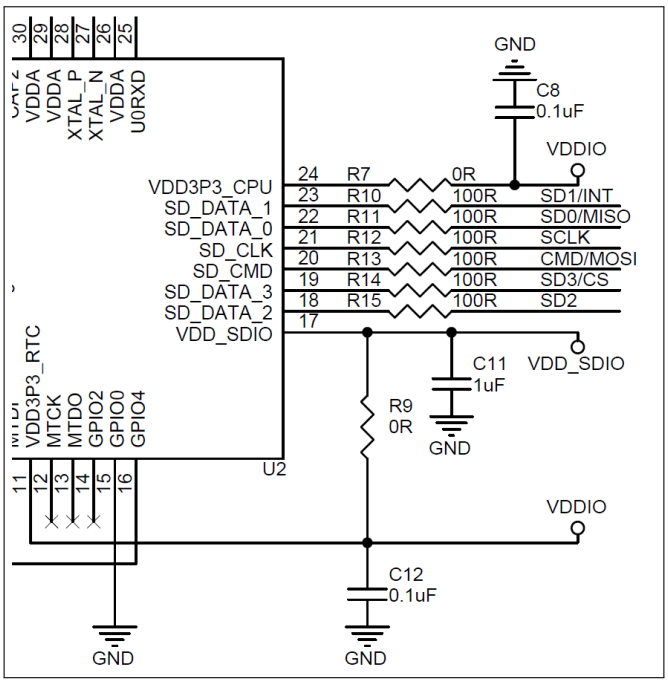

Figure 4: ESP8689 Digital Power Supply Pins

3.1.1.2 Analog Power Supply

Pin1, Pin26, Pin29 and Pin30 are the analog power supply pins. Pin3 and Pin4 are the power supply pins for the power amplifiers. It should be noted that the sudden increase in current draw, when ESP8689 is in transmission mode, may cause a power rail collapse. Therefore, we highly recommended that users add another 0603 10 μF capacitor to the power trace, which can work in conjunction with the 0402 0.1 μF capacitor.

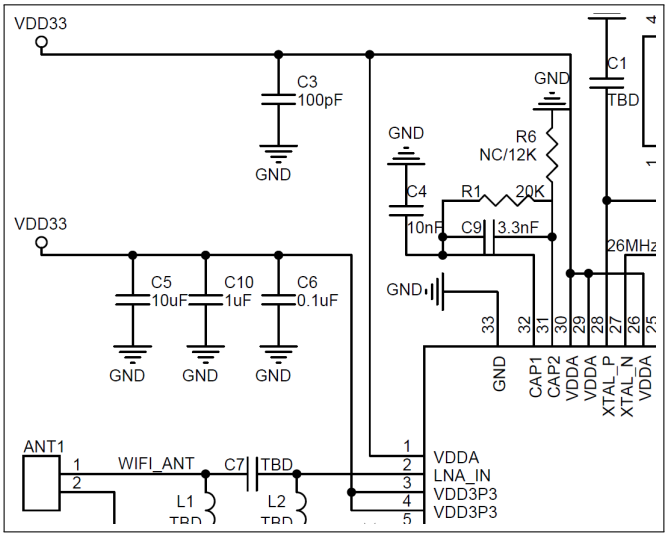

Figure 5: ESP8689 Analog Power Supply Pins

Notice:

The ESP8689 can also be powered by one single power supply. When using a single power supply, the recommended voltage range is 2.8V ~ 3.6V, and the recommended current is 500 mA and above.

3.1.2 Power-on Sequence and System Reset

3.1.2.1 Power-on Sequence

ESP8689 uses a 3.3V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of CHIP_PU (Pin7) by time T after the 3.3V rails have been brought up. The recommended delay time (T) is given by the parameter of the RC circuit. For reference design, please refer to Figure **ESP-WROOM-32 Peripheral Schematics** in the *ESP-WROOM-32 Datasheet*.

Notice:

If CHIP_PU is driven by a power management chip, then the power management chip controls the ESP8689 power state. When the power management chip turns on/off Wi-Fi through the high/low level on GPIO, a pulse current may be generated. To avoid level instability on CHIP_PU, an RC delay (R=10 kΩ, C=100 nF) circuit is required.

3.1.2.2 Reset

CHIP_PU serves as the reset pin of ESP8689. ESP8689 will power off when CHIP_PU is held low and the input level is below 0.6V and stays for at least 200 μs. To avoid reboots caused by external interferences, the CHIP_PU trace should be as short as possible and routed away from the clock lines. A pull-up resistor and a ground capacitor are highly recommended.

Notice:

CHIP_PU pin must not be left floating.

3.1.3 RF

In the circuit design, a π-type matching network is essential for antenna matching.

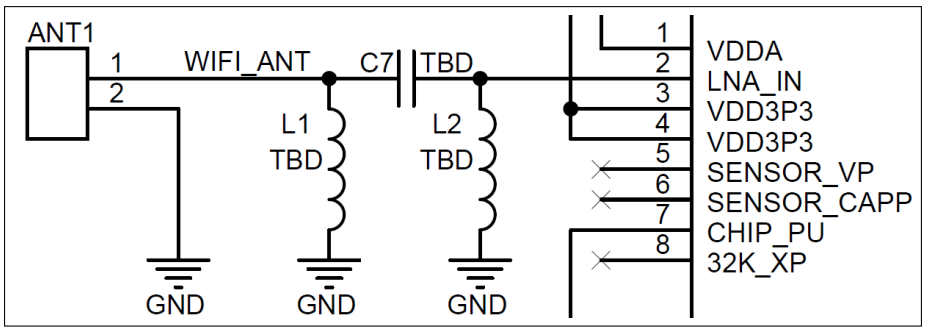

Figure 6: ESP8689 RF

3.1.4 Crystal Oscillator

There are two clock sources for the ESP8689, that is, an external crystal oscillator clock source and an RTC clock source.

3.1.4.1 External Clock Source (Compulsory)

The ESP8689 Wi-Fi/BT firmware can only support 40 MHz crystal oscillator for now.

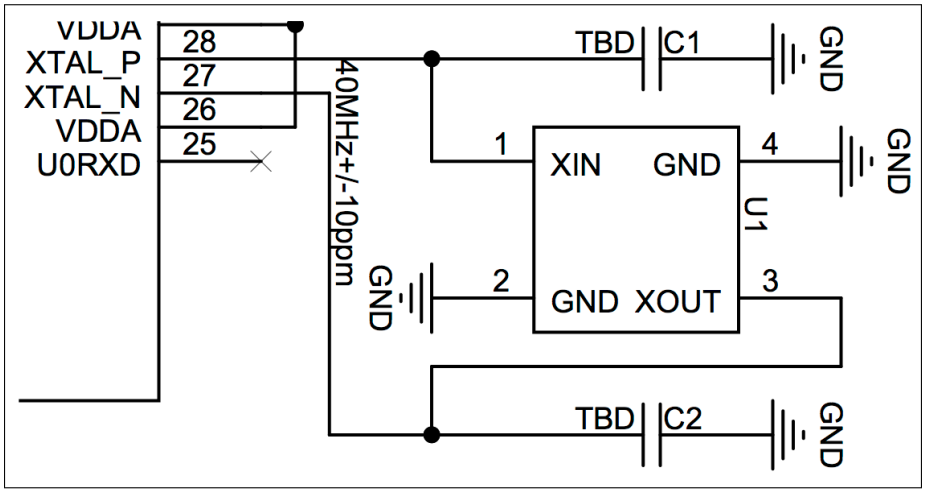

Figure 7: ESP8689 Crystal Oscillator

Notice:

Defects in the quality of the crystal oscillators (for example, high frequency deviation) and unstable working temperature may lead to the malfunction of ESP8689, resulting in a decrease of the overall performance.

3.1.4.2 RTC (Optional)

ESP8689 supports an external 32 kHz crystal oscillator to act as the RTC sleep clock.

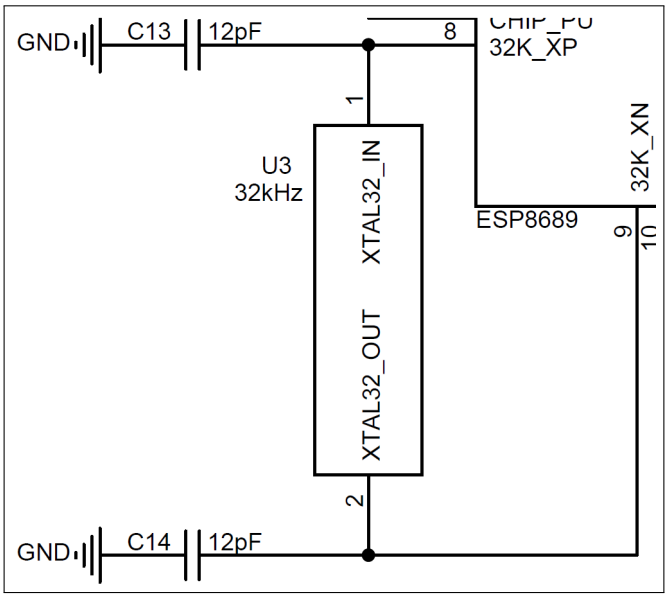

Figure 8: ESP8689 Crystal Oscillator (RTC)

Notice:

If the RTC source is not required, then Pin12 32K_XP and Pin13 32K_XN can be used as digital GPIOs.

3.1.5 SDIO/SPI Interface

It is recommended that a series resistor of 100Ω be added to the SDIO/SPI interface to reduce the noise. If ESP8689 is far away from the CPU, a resistor with a smaller resistance is needed. In addition, pull-up resistors can be optionally added to the SDIO/SPI interface, if needed.

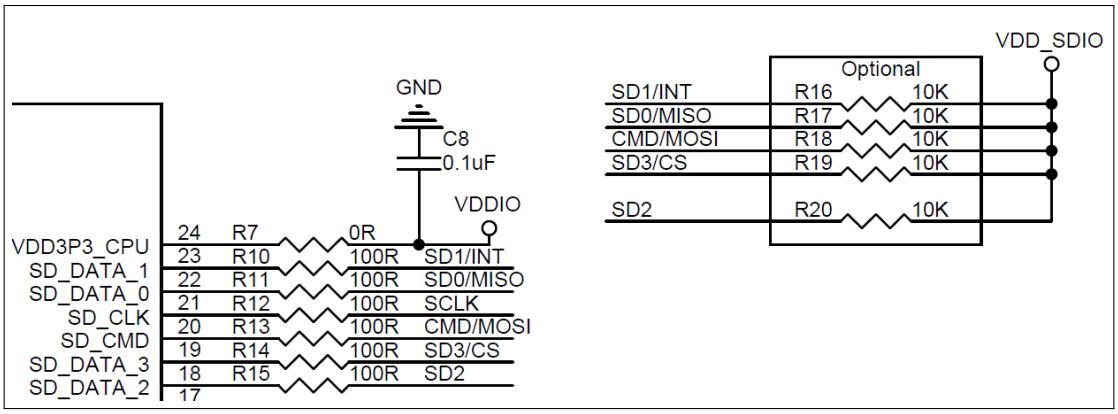

Figure 9: ESP8689 SDIO/SPI

3.1.6 External Capacitor

The schematics of Pin31 CAP2 and Pin32 CAP1 is shown in Figure 10. 10 nF is an external capacitor whose precision should be ±10%. For the RC circuit between CAP1 and CAP2 pins, please refer to Figure 10. Removing the RC circuit may slightly affect ESP8689 in Deep-sleep mode.

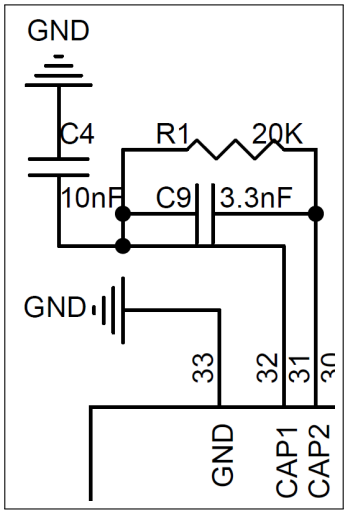

Figure 10: ESP8689 External Capacitor

3.2 PCB Layout

The PCB layout design guidelines are applicable to cases when the

- ESP8689 module functions as a standalone device, and when the
- ESP8689 functions as a slave device.

3.2.1 Standalone ESP8689 Module

3.2.1.1 General Principles of PCB Layout

We recommend a four-layer PCB design.

- The first layer is the TOP layer for signal traces and components.
- The second layer is the GND layer without signal traces being routed so as to ensure a complete GND plane.
- The third layer is the POWER layer. It is acceptable to route signal traces on this layer, provided that there is a complete GND plane under the RF and crystal oscillator.
- The fourth layer is the BOTTOM layer, where power traces are routed. Placing any components on this layer is not recommended.

3.2.1.2 Power Supply

The 3.3V power traces are highlighted in yellow in Figure 11. The width of these power traces should be larger than 15 mil. Before power traces reach the analog power-supply pins (Pin 1, 3, 4, 29, 30), a 0603 10 μF capacitor is required. A 0.1 μF capacitor should be added to each digital power-supply pin, if possible.

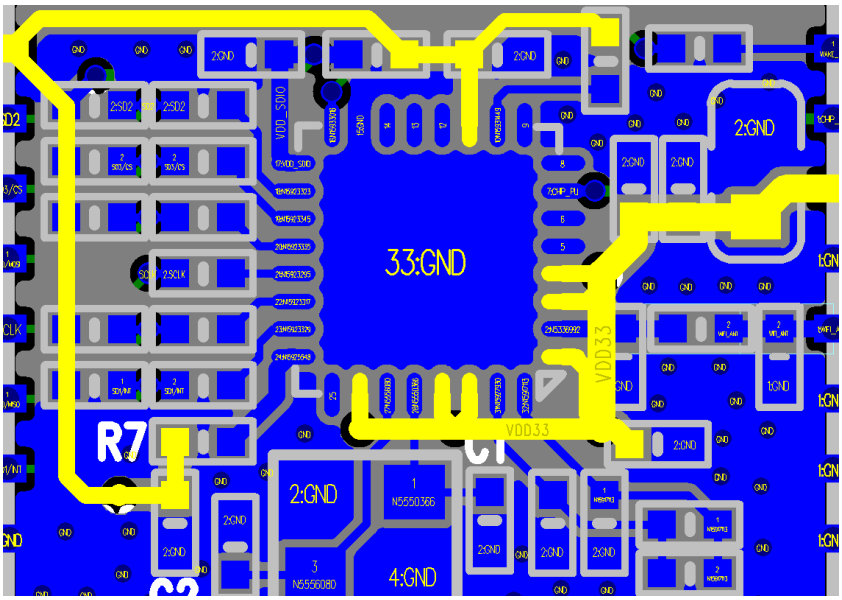

Figure 11: ESP8689 PCB Layout

Notice:

All decoupling capacitors should be placed as close as possible to the power-supply pins. It is good practice to route the power traces on the fourth (bottom) layer. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. The diameter of the drill should exceed the width of the power traces. The diameter of the via pad should be 1.5 times that of the drill.

3.2.1.3 Crystal Oscillator

For the design of the crystal oscillator section, please refer to Figure 12. In addition, the following should be noted:

- The crystal oscillator should be placed far from the clock pin. **The recommended gap is 2.7 mm**. It is good practice to add high-density ground via stitching around the clock trace for containing the high-frequency clock signal.
- There should be no vias for the clock input and output traces, which means that the traces cannot cross layers.
- The external regulating capacitor should be placed on the near left or right side of the crystal oscillator and at the end of the clock trace.
- Do not route high-frequency digital signal traces under the crystal oscillator. It is best not to route any signal trace under the crystal oscillator. The larger the copper area on the top layer is, the better.
- As the crystal oscillator is a sensitive component, do not place any magnetic components nearby that may cause interference, such as, power-switching converters or unshielded inductors.

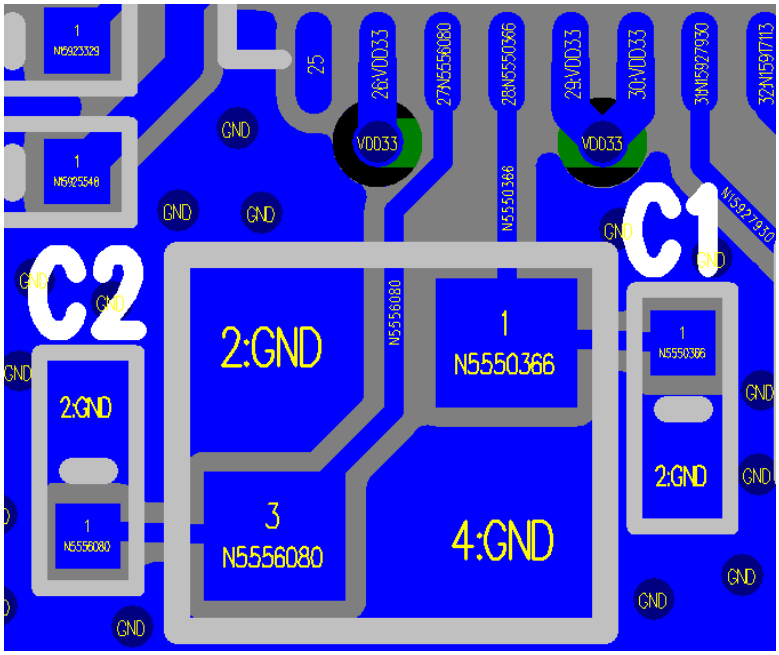

Figure 12: ESP8689 Crystal Oscillator

3.2.1.4 RF

- The characteristic RF impedance must be 50Ω. The ground plane on the adjacent layer needs to be complete. Make sure you keep the width of the RF trace consistent, and do not branch the trace. The RF trace should be as short as possible with dense ground via stitching around it for isolation.
- However, there should be no vias for the RF trace. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- π-type matching circuitry should be reserved on the RF trace and placed close to the chip.
- No high-frequency signal traces should be routed close to the RF trace. The RF antenna should be placed away from high-frequency transmitting devices, such as crystal oscillators, DDR, clocks (SDIO_CLK), etc.

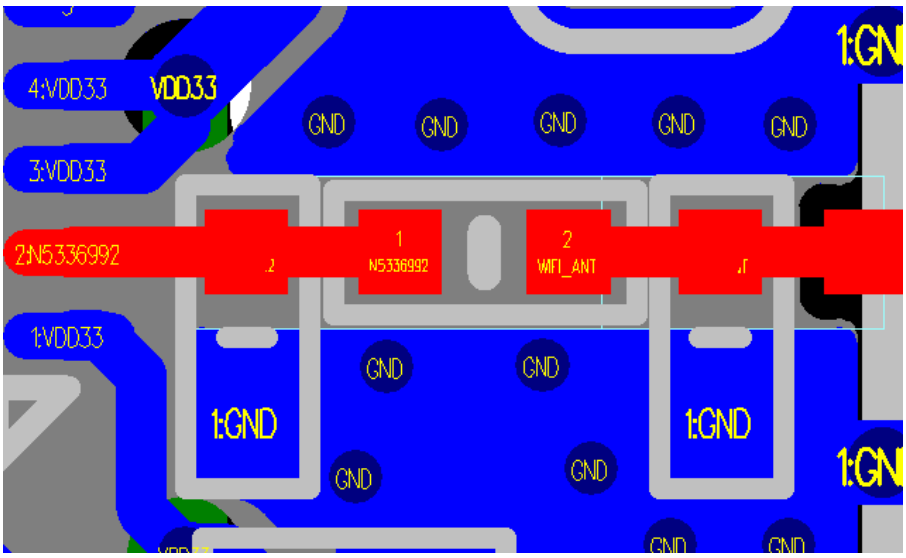

Figure 13: ESP8689 RF

3.2.2 ESP8689 as a Slave Device

When ESP8689 works as a slave device in a system, users need to pay more attention to signal integrity in the PCB design. It is important to keep ESP8689 away from the interferences caused by the complexity of the system and an increased number of high-frequency signals. We use the mainboard of a PAD or TV Box as an example here to provide guidelines for the PCB layout and design.

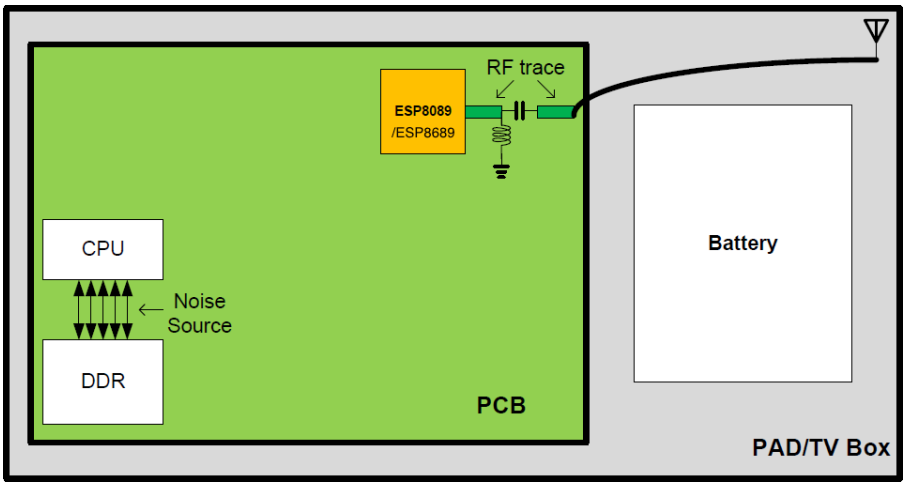

Figure 14: PAD/TV Box Layout

The digital signals between the CPU and DDR are the main producers of the high-frequency noise that interferes with Wi-Fi radio. Therefore, the following should be noted with regards to the PCB design.

- As can be seen in Figure 14, ESP8689 should be placed near the edge of the PCB and away from the CPU and DDR, the main high-frequency noise sources. The distance between the chip and the noise sources decreases the interference and reduces the coupled noise.
- It is suggested that a 100Ω series resistor is added to the six signal traces when ESP8689 communicates with the CPU via SDIO to decrease the drive current and any interferences, and also to eliminate the sequencing problem caused by the inconsistent length of the SDIO traces.
- On-board PCB antenna is not recommended, as it receives much interference and coupling noise, both of which impact the RF performance. We suggest that you use an external antenna which should be directed

away from the PCB board via a cable, in order to weaken the high frequency interference with Wi-Fi.

- The high-frequency signal traces between the CPU and associated memory should be routed strictly according to the routing guidelines (please refer to the DDR trace routing guidelines). We recommend that you add ground vias around the CLK traces separately, and around the parallel data or address buses.
- The GND of the Wi-Fi circuit and that of other high-power devices should be separated and connected through wires if there are high-power components, such as motors, in the design.
- The antenna should be kept away from high-frequency noise sources, such as LCD, HDMI, Camera Sensor, USB, etc.

3.2.3 Typical Layout Problems and Solutions

3.2.3.1 Q: The current ripple is not large, but the Tx performance of RF is rather poor.

Analysis:

The current ripple has a strong impact on the RF Tx performance. It should be noted that the ripple must be tested when ESP8689 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the ripple should be <100 mV when ESP8689 sends 11n MCS7 packets, and < 120 mV when ESP8689 sends 11b 11m packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the ESP8689 analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable current ripples.

3.2.3.2 Q: The power ripple is small, but RF Tx performance is poor.

Analysis:

The RF Tx performance can be affected not only by power ripples, but also by the crystal oscillator itself. Poor quality and big frequency offsets of the crystal oscillator decrease the RF Tx performance. The crystal oscillator clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO trace and UART trace under the crystal oscillator, could also result in the malfunction of the crystal oscillator. Besides, sensitive components or radiation components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Chapter 3.2 for details.

3.2.3.3 Q: When ESP8689 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance

mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the reserved π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.2.3.4 Q: Tx performance is not bad, but the Rx sensitivity is low.

Analysis:

Good Tx performance indicates proper RF impedance matching. External coupling to the antenna can affect the Rx performance. For instance, the crystal oscillator signal harmonics could couple to the antenna. If the Tx and Rx traces of UART cross over with RF trace, then, they will affect the Rx performance, as well. If ESP8689 serves as a slave device, there will be other high-frequency interference sources on the board, which may affect the Rx performance.

Solution:

Keep the antenna away from crystal oscillators. Do not route high-frequency signal traces close to the RF trace. High performance digital circuitry should be placed away from the RF block on large board designs. Please see Chapter 3.2 for details.