GW2AR Series of FPGA Products GW2AR-18 Pinout Version History



Date	Version	Description
09/02/2016	1.0E	Initial version published.
03/282019	1.1E	The info. of EQ176 package added.
03/10/2020	1.2E	The descriptions of pin MODE0/MODE1/MODE2 improved.
06/30/2020	1.2.1E	QN88/EQ144 package embedded with PSRAM renamed QN88P/EQ144P.
08/07/2020	1.3E	The info. of QN88PF and EQ144PF packages added. The power supply pin in package LQ176 and EQ176 modified.
04/22/2021	1.4E	The info. of PG256S package added.
10/25/2021	1.5E	Pin definitions updated.
08/12/2022	1.6E	The info. of PG256S package removed.
10/20/2022	1.6.1E	The note in Power sheet updated. The note in Pin Definitions sheet updated.
03/10/2023	1.7E	LQ176 and LQ144 packages removed. The note of EQ144/QN88/EQ176/QN88P/EQ144P/EQ144PF/QN88PF package in Power sheet added. The description of CLKHOLD_N pin in Pin Definitions sheet updated.
06/30/2023	1.7.1E	The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.

GW2AR Series of FPGA Products GW2AR-18 Pinout Pin Definitions



Pin Name	I/O	Description
User I/O		
		[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
IO[End][Row/Column Number][A/B]	1/0	[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Nu	umber][A/B]/MMM	/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	0	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	0	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
	О	High, the programming configuration has been completed successfully;
DONE ^[1]	9	Low, the programming configuration has not been completed or failed.
	l	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY ^[1]	I/O	High, the device can be programmed and configured currently;
	"	Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode
MO	0	MO in MSPI mode

GW2AR Series of FPGA Products GW2AR-18 Pinout Pin Definitions



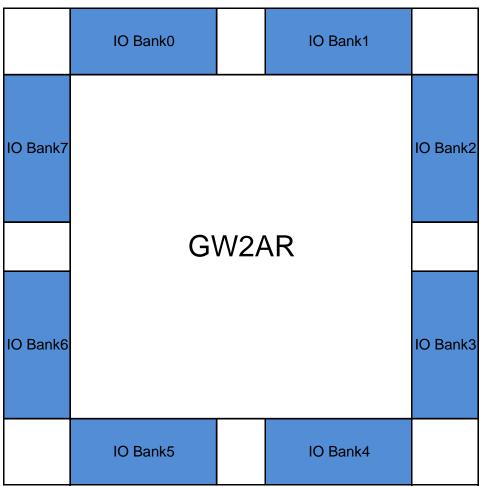
Pin Name	1/0	Description
MCS_N	0	Enable signal MCS_N in MSPI mode, active-low
MCLK	0	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK		Clock input in SSPI, SERIAL, and CPU modes
SO	0	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x]: global clock No. [2]
GCLKT_[x]	I	Global clock input pin, T(True), [x]: global clock No.
LPLL_C_fb/RPLL_C_fb		Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as "VCCIO", it's internally powered; if this pin is marked as "GND", it's internally grounded.
Other Pins		
EXTR	NA	External 10K 1% resistor to ground
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
VCCPLLL0/1	NA	Left PLL0/1 voltage supply pin, LQFP is separately packaged.
VCCPLLR0/1	NA	Right PLL0/1 voltage supply pin, LQFP is separately packaged.
VCCPLLL	NA	Package PBGA: Left PLL0/1 voltage supply pin
VCCPLLR	NA	Package PBGA: Right PLL0/1 voltage supply pin
Notel		

Note!

[2] When the input is single-ended, GCLKC_[x] pin is not a global clock pin.

^[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.





- [1] Each Bank has independent reference voltage (VREF).
- [2] You can select to use IOB internal VREF (equals to 0.5 X VCCIO).
- [3] You can also select to use external VREF input (use any IO pins as external VREF input).

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
EXTR	Ground		N/A				47	75	91	47	75	75	47
IOB12A	I/O	DQ5	5		True_of_IOB12B	TRUE		44	53		44	44	
IOB12B	I/O	DQ5	5		Comp_of_IOB12A	TRUE		45	54		45	45	
IOB13A	I/O	DQ5	5		True_of_IOB13B	NONE							
IOB13B	I/O	DQ5	5		Comp_of_IOB13A	NONE							
IOB14A	I/O	DQ5	5		True_of_IOB14B	TRUE	29	46	55	29	46		29
IOB14B	I/O	DQ5	5		Comp_of_IOB14A	TRUE	30	47	56	30	47	47	30
IOB15A	I/O	DQ5	5		True_of_IOB15B	NONE							
IOB15B	I/O	DQ5	5		Comp_of_IOB15A	NONE							
IOB16A	I/O	DQ5	5		True_of_IOB16B	TRUE							
IOB16B	I/O	DQ5	5		Comp_of_IOB16A	TRUE							
IOB17A	I/O	DQ5	5		True_of_IOB17B	NONE		48	57		48	48	
IOB17B	I/O	DQ5	5		Comp_of_IOB17A	NONE		49	58		49	49	
IOB18A	I/O	DQ5	5		True_of_IOB18B	TRUE	31		59	31			31
IOB18B	I/O	DQ5	5		Comp_of_IOB18A	TRUE	32		60	32			32
IOB19A	I/O	DQ5	5		True_of_IOB19B	NONE							
IOB19B	I/O	DQ5	5		Comp_of_IOB19A	NONE							
IOB20A	I/O	DQ5	5		True_of_IOB20B	TRUE		50			50	50	
IOB20B	I/O	DQ5	5		Comp_of_IOB20A	TRUE		51			51	51	
IOB21A	I/O	DQS5	5		True_of_IOB21B	NONE			61				
IOB21B	I/O	DQS5	5		Comp_of_IOB21A	NONE			62				
IOB22A	I/O	DQ5	5		True_of_IOB22B	TRUE		52			52	52	
IOB22B	I/O	DQ5	5		Comp_of_IOB22A	TRUE		54			54	54	
IOB23A	I/O	DQ5	5		True_of_IOB23B	NONE							
IOB23B	I/O	DQ5	5		Comp_of_IOB23A	NONE							
IOB24A	I/O	DQ5	5		True_of_IOB24B	TRUE	33			33			33
IOB24B	I/O	DQ5	5		Comp_of_IOB24A	TRUE	34			34			34
IOB25A	I/O	DQ5	5		True_of_IOB25B	NONE							
IOB25B	I/O	DQ5	5		Comp_of_IOB25A	NONE							
IOB26A	I/O	DQ5	5		True_of_IOB26B	TRUE							
IOB26B	I/O	DQ5	5		Comp_of_IOB26A	TRUE							
IOB27A/GCLKT_5	I/O	DQ5	5	GCLKT_5	True_of_IOB27B	NONE			63				
IOB27B/GCLKC_5	I/O	DQ5	5	GCLKC_5	Comp_of_IOB27A	NONE			64				

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOB2A	I/O	DQ4	5		True_of_IOB2B	TRUE							
IOB2B	I/O	DQ4	5		Comp_of_IOB2A	TRUE							
IOB30A/GCLKT_4	I/O	DQ6	4	GCLKT_4	True_of_IOB30B	TRUE	35	56	68	35	56	56	35
IOB30B/GCLKC_4	I/O	DQ6	4	GCLKC_4	Comp_of_IOB30A	TRUE	36	57	69	36	57	57	36
IOB31A	I/O	DQ6	4		True_of_IOB31B	NONE							
IOB31B	I/O	DQ6	4		Comp_of_IOB31A	NONE							
IOB32A	I/O	DQ6	4		True_of_IOB32B	TRUE							
IOB32B	I/O	DQ6	4		Comp_of_IOB32A	TRUE							
IOB33A	I/O	DQ6	4		True_of_IOB33B	NONE		58			58	58	
IOB33B	I/O	DQ6	4		Comp_of_IOB33A	NONE		59			59	59	
IOB34A	I/O	DQ6	4		True_of_IOB34B	TRUE	37	60	70	37	60	60	37
IOB34B	I/O	DQ6	4		Comp_of_IOB34A	TRUE	38	61	71	38	61	61	38
IOB35A	I/O	DQ6	4		True_of_IOB35B	NONE							
IOB35B	I/O	DQ6	4		Comp_of_IOB35A	NONE							
IOB36A	I/O	DQ6	4		True_of_IOB36B	TRUE							
IOB36B	I/O	DQ6	4		Comp_of_IOB36A	TRUE							
IOB37A	I/O	DQS6	4		True_of_IOB37B	NONE			72				
IOB37B	I/O	DQS6	4		Comp_of_IOB37A	NONE			73				
IOB38A	I/O	DQ6	4		True_of_IOB38B	TRUE		62	74		62	62	
IOB38B	I/O	DQ6	4		Comp_of_IOB38A	TRUE		63	75		63	63	
IOB39A	I/O	DQ6	4		True_of_IOB39B	NONE							
IOB39B	I/O	DQ6	4		Comp_of_IOB39A	NONE							
IOB3A	I/O	DQ4	5		True_of_IOB3B	NONE							
IOB3B	I/O	DQ4	5		Comp_of_IOB3A	NONE							
IOB40A	I/O	DQ6	4		True_of_IOB40B	TRUE	39	64	76	39	64	64	39
IOB40B	I/O	DQ6	4		Comp_of_IOB40A	TRUE	40	65	77	40	65	65	40
IOB41A	I/O	DQ6	4		True_of_IOB41B	NONE							
IOB41B	I/O	DQ6	4		Comp_of_IOB41A	NONE							
IOB42A	I/O	DQ6	4		True_of_IOB42B	TRUE		66	78		66	66	
IOB42B	I/O	DQ6	4		Comp_of_IOB42A	TRUE	42	67	79	42	67	67	42
IOB43A	I/O	DQ6	4		True_of_IOB43B	NONE	41			41			41
IOB43B	I/O	DQ6	4		Comp_of_IOB43A	NONE							
IOB44A	I/O	DQ6	4		True_of_IOB44B	TRUE			80				

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOB44B	I/O	DQ6	4		Comp_of_IOB44A	TRUE			81				
IOB45A	I/O	DQ6	4		True_of_IOB45B	NONE							
IOB45B	I/O	DQ6	4		Comp_of_IOB45A	NONE							
IOB48A	I/O	DQS7	4		True_of_IOB48B	TRUE		68	82		68	68	
IOB48B	I/O	DQS7	4		Comp_of_IOB48A	TRUE		69	83		69	69	
IOB49A	I/O	DQ7	4		True_of_IOB49B	NONE							
IOB49B	I/O	DQ7	4		Comp_of_IOB49A	NONE							
IOB4A	I/O	DQ4	5		True_of_IOB4B	TRUE							
IOB4B	I/O	DQ4	5		Comp_of_IOB4A	TRUE			47				
IOB50A	I/O	DQ7	4		True_of_IOB50B	TRUE			84				
IOB50B	I/O	DQ7	4		Comp_of_IOB50A	TRUE			85				
IOB51A	I/O	DQ7	4		True_of_IOB51B	NONE							
IOB51B	I/O	DQ7	4		Comp_of_IOB51A	NONE							
IOB52A	I/O	DQ7	4		True_of_IOB52B	TRUE			86				
IOB52B	I/O	DQ7	4		Comp_of_IOB52A	TRUE							
IOB53A	I/O	DQ7	4		True_of_IOB53B	NONE		70			70	70	
IOB53B	I/O	DQ7	4		Comp_of_IOB53A	NONE		71			71	71	
IOB54A	I/O	DQ7	4		True_of_IOB54B	TRUE							
IOB54B	I/O	DQ7	4		Comp_of_IOB54A	TRUE							
IOB55A	I/O	DQ7	4		True_of_IOB55B	NONE							
IOB55B	I/O	DQ7	4		Comp_of_IOB55A	NONE		72			72	72	
IOB5A	I/O	DQ4	5		True_of_IOB5B	NONE		38	48		38	38	
IOB5B	I/O	DQ4	5		Comp_of_IOB5A	NONE		39			39	39	
IOB6A	I/O	DQ4	5		True_of_IOB6B	TRUE	25	40	49	25	40	40	25
IOB6B	I/O	DQ4	5		Comp_of_IOB6A	TRUE	26	41	50	26	41	41	26
IOB7A	I/O	DQ4	5		True_of_IOB7B	NONE		42			42	42	
IOB7B	I/O	DQ4	5		Comp_of_IOB7A	NONE		43			43	43	
IOB8A	I/O	DQ4	5		True_of_IOB8B	TRUE	27		51	27			27
IOB8B	I/O	DQ4	5		Comp_of_IOB8A	TRUE	28		52	28			28
IOB9A	I/O	DQS4	5		True_of_IOB9B	NONE							
IOB9B	I/O	DQS4	5		Comp_of_IOB9A	NONE							
IOL11A	I/O	DQ1	7		True_of_IOL11B	TRUE			6				
IOL11B	I/O	DQ1	7		Comp_of_IOL11A	TRUE							

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOL12A	I/O	DQ1	7		True_of_IOL12B	NONE							
IOL12B	I/O	DQ1	7		Comp_of_IOL12A	NONE							
IOL13A	I/O	DQ1	7		True_of_IOL13B	TRUE							
IOL13B	I/O	DQ1	7		Comp_of_IOL13A	TRUE							
IOL14A	I/O	DQ1	7		True_of_IOL14B	NONE							
IOL14B	I/O	DQ1	7		Comp_of_IOL14A	NONE			7				
IOL15A	I/O	DQ1	7		True_of_IOL15B	TRUE			8				
IOL15B	I/O	DQ1	7		Comp_of_IOL15A	TRUE			9				
IOL16A	I/O	DQ1	7		True_of_IOL16B	NONE							
IOL16B	I/O	DQ1	7		Comp_of_IOL16A	NONE							
IOL17A	I/O	DQ1	7		True_of_IOL17B	TRUE			10				
IOL17B	I/O	DQ1	7		Comp_of_IOL17A	TRUE			11				
IOL18A	I/O	DQ1	7		True_of_IOL18B	NONE			12				
IOL18B	I/O	DQ1	7		Comp_of_IOL18A	NONE							
IOL20A	I/O	DQ1	7		True_of_IOL20B	TRUE							
IOL20B	I/O	DQ1	7		Comp_of_IOL20A	TRUE							
IOL21A	I/O	DQ1	7		True_of_IOL21B	NONE							
IOL21B	I/O	DQ1	7		Comp_of_IOL21A	NONE							
IOL22A	I/O	DQS1	7		True_of_IOL22B	TRUE		9			9	9	
IOL22B	I/O	DQS1	7		Comp_of_IOL22A	TRUE		10			10	10	
IOL23A	I/O	DQ1	7		True_of_IOL23B	NONE			14				
IOL23B	I/O	DQ1	7		Comp_of_IOL23A	NONE							
IOL24A	I/O	DQ1	7		True_of_IOL24B	TRUE			15				
IOL24B	I/O	DQ1	7		Comp_of_IOL24A	TRUE			16				
IOL25A	I/O	DQ1	7		True_of_IOL25B	NONE							
IOL25B	I/O	DQ1	7		Comp_of_IOL25A	NONE			18				
IOL26A	I/O	DQ1	7		True_of_IOL26B	TRUE			17				
IOL26B	I/O	DQ1	7		Comp_of_IOL26A	TRUE			19				
IOL27A/GCLKT_7	I/O	DQ1	7	GCLKT_7	True_of_IOL27B	NONE		11	20		11	11	
IOL27B/GCLKC_7	I/O	DQ1	7	GCLKC_7	Comp_of_IOL27A	NONE		12	21		12	12	
IOL29A/GCLKT_6	I/O	DQ2	6	GCLKT_6	True_of_IOL29B	TRUE	10	25		10	25	25	10
IOL29B/GCLKC_6	I/O	DQ2	6	GCLKC_6	Comp_of_IOL29A	TRUE	11	26		11	26	26	11
IOL2A	I/O	DQ0	7	_	True_of_IOL2B	TRUE		3	3		3	3	

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOL2B	I/O	DQ0	7		Comp_of_IOL2A	TRUE		4	4		4	4	
IOL30A	I/O	DQ2	6		True_of_IOL30B	NONE							
IOL30B	I/O	DQ2	6		Comp_of_IOL30A	NONE							
IOL31A	I/O	DQ2	6		True_of_IOL31B	TRUE							
IOL31B	I/O	DQ2	6		Comp_of_IOL31A	TRUE							
IOL32A	I/O	DQ2	6		True_of_IOL32B	NONE		23			23	23	
IOL32B	I/O	DQ2	6		Comp_of_IOL32A	NONE		24			24	24	
IOL33A	I/O	DQ2	6		True_of_IOL33B	TRUE		27			27	27	
IOL33B	I/O	DQ2	6		Comp_of_IOL33A	TRUE		28			28	28	
IOL34A	I/O	DQ2	6		True_of_IOL34B	NONE							
IOL34B	I/O	DQ2	6		Comp_of_IOL34A	NONE							
IOL35A	I/O	DQ2	6		True_of_IOL35B	TRUE							
IOL35B	I/O	DQ2	6		Comp_of_IOL35A	TRUE							
IOL36A	I/O	DQS2	6		True_of_IOL36B	NONE		29			29	29	
IOL36B	I/O	DQS2	6		Comp_of_IOL36A	NONE		30			30	30	
IOL38A	I/O	DQ2	6		True_of_IOL38B	TRUE			24				
IOL38B	I/O	DQ2	6		Comp_of_IOL38A	TRUE			25				
IOL39A	I/O	DQ2	6		True_of_IOL39B	NONE							
IOL39B	I/O	DQ2	6		Comp_of_IOL39A	NONE							
IOL3A	I/O	DQ0	7		True_of_IOL3B	NONE							
IOL3B	I/O	DQ0	7		Comp_of_IOL3A	NONE							
IOL40A	I/O	DQ2	6		True_of_IOL40B	TRUE			26				
IOL40B	I/O	DQ2	6		Comp_of_IOL40A	TRUE			27				
IOL41A	I/O	DQ2	6		True_of_IOL41B	NONE							
IOL41B	I/O	DQ2	6		Comp_of_IOL41A	NONE							
IOL42A	I/O	DQ2	6		True_of_IOL42B	TRUE		32	28		32	32	
IOL42B	I/O	DQ2	6		Comp_of_IOL42A	TRUE		33	29		33	33	
IOL43A	I/O	DQ2	6		True_of_IOL43B	NONE							
IOL43B	I/O	DQ2	6		Comp_of_IOL43A	NONE							
IOL44A	I/O	DQ2	6		True_of_IOL44B	TRUE			30				
IOL44B	I/O	DQ2	6		Comp_of_IOL44A	TRUE			31				
IOL45A/LPLL2_T_in	I/O	DQ2	6	LPLL2_T_in	True_of_IOL45B	NONE	13	34	32	13	34	34	13
IOL45B/LPLL2_C_in	I/O	DQ2	6	LPLL2_C_in	Comp_of_IOL45A	NONE		35	33		35	35	

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOL47A/LPLL2_T_fb	I/O	DQ3	6	LPLL2_T_fb	True_of_IOL47B	TRUE	15		35	15			15
IOL47B/LPLL2_C_fb	I/O	DQ3	6	LPLL2_C_fb	Comp_of_IOL47A	TRUE	16		36	16			16
IOL48A	I/O	DQ3	6		True_of_IOL48B	NONE							
IOL48B	I/O	DQ3	6		Comp_of_IOL48A	NONE							
IOL49A	I/O	DQ3	6		True_of_IOL49B	TRUE	17		37	17			17
IOL49B	I/O	DQ3	6		Comp_of_IOL49A	TRUE	18			18			18
IOL4A	I/O	DQ0	7		True_of_IOL4B	TRUE							
IOL4B	I/O	DQ0	7		Comp_of_IOL4A	TRUE							
IOL50A	I/O	DQS3	6		True_of_IOL50B	NONE			38				
IOL50B	I/O	DQS3	6		Comp_of_IOL50A	NONE			39				
IOL51A	I/O	DQ3	6		True_of_IOL51B	TRUE	19			19			19
IOL51B	I/O	DQ3	6		Comp_of_IOL51A	TRUE	20			20			20
IOL52A	I/O	DQ3	6		True_of_IOL52B	NONE							
IOL52B	I/O	DQ3	6		Comp_of_IOL52A	NONE							
IOL53A	I/O	DQ3	6		True_of_IOL53B	TRUE			41				
IOL53B	I/O	DQ3	6		Comp_of_IOL53A	TRUE			42				
IOL54A	I/O	DQ3	6		True_of_IOL54B	NONE							
IOL54B	I/O	DQ3	6		Comp_of_IOL54A	NONE							
IOL5A	I/O	DQ0	7		True_of_IOL5B	NONE							
IOL5B	I/O	DQ0	7		Comp_of_IOL5A	NONE							
IOL6A	I/O	DQS0	7		True_of_IOL6B	TRUE							
IOL6B	I/O	DQS0	7		Comp_of_IOL6A	TRUE							
IOL7A/LPLL1_T_in	I/O	DQ0	7	LPLL1_T_in	True_of_IOL7B	NONE	4	6		4	6	6	4
IOL7B/LPLL1_C_in	I/O	DQ0	7	LPLL1_C_in	Comp_of_IOL7A	NONE		7			7	7	
IOL8A/LPLL1_T_fb	I/O	DQ0	7	LPLL1_T_fb	True_of_IOL8B	TRUE							
IOL8B/LPLL1_C_fb	I/O	DQ0	7	LPLL1_C_fb	Comp_of_IOL8A	TRUE							
IOL9A	I/O	DQ0	7		True_of_IOL9B	NONE							
IOL9B	I/O	DQ0	7		Comp_of_IOL9A	NONE							
IOR11A	I/O	DQ10	2		True_of_IOR11B	TRUE							
IOR11B	I/O	DQ10	2		Comp_of_IOR11A	TRUE							
IOR12A	I/O	DQ10	2		True_of_IOR12B	NONE							
IOR12B	I/O	DQ10	2		Comp_of_IOR12A	NONE							
IOR13A	I/O	DQ10	2		True_of_IOR13B	TRUE							

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOR13B	I/O	DQ10	2		Comp_of_IOR13A	TRUE							
IOR14A	I/O	DQ10	2		True_of_IOR14B	NONE			126				
IOR14B	I/O	DQ10	2		Comp_of_IOR14A	NONE							
IOR15A	I/O	DQ10	2		True_of_IOR15B	TRUE							
IOR15B	I/O	DQ10	2		Comp_of_IOR15A	TRUE							
IOR16A	I/O	DQ10	2		True_of_IOR16B	NONE							
IOR16B	I/O	DQ10	2		Comp_of_IOR16A	NONE							
IOR17A	I/O	DQ10	2		True_of_IOR17B	TRUE							
IOR17B	I/O	DQ10	2		Comp_of_IOR17A	TRUE							
IOR18A	I/O	DQ10	2		True_of_IOR18B	NONE							
IOR18B	I/O	DQ10	2		Comp_of_IOR18A	NONE							
IOR20A	I/O	DQ10	2		True_of_IOR20B	TRUE		102	125		102	102	
IOR20B	I/O	DQ10	2		Comp_of_IOR20A	TRUE		101	124		101	101	
IOR21A	I/O	DQ10	2		True_of_IOR21B	NONE							
IOR21B	I/O	DQ10	2		Comp_of_IOR21A	NONE							
IOR22A	I/O	DQS10	2		True_of_IOR22B	TRUE		100	123		100	100	
IOR22B	I/O	DQS10	2		Comp_of_IOR22A	TRUE		99	122		99	99	
IOR23A	I/O	DQ10	2		True_of_IOR23B	NONE							
IOR23B	I/O	DQ10	2		Comp_of_IOR23A	NONE							
IOR24A	I/O	DQ10	2		True_of_IOR24B	TRUE							
IOR24B	I/O	DQ10	2		Comp_of_IOR24A	TRUE							
IOR25A/TDO	I/O	DQ10	2	TDO	True_of_IOR25B	NONE	8	18	121	8	18	18	8
IOR25B/TMS	I/O	DQ10	2	TMS	Comp_of_IOR25A	NONE	5	13	119	5	13	13	5
IOR26A/TCK	I/O	DQ10	2	TCK	True_of_IOR26B	TRUE	6	14	120	6	14	14	6
IOR26B/TDI	I/O	DQ10	2	TDI	Comp_of_IOR26A	TRUE	7	16	117	7	16	16	7
IOR27A/GCLKT_2	I/O	DQ10	2	GCLKT_2	True_of_IOR27B	NONE		98	116			98	
IOR27B/GCLKC_2	I/O	DQ10	2	GCLKC_2	Comp_of_IOR27A	NONE		97			97	97	
IOR29A/GCLKT_3	I/O	DQ9	3	GCLKT_3	True_of_IOR29B	TRUE	63		114	63			63
IOR29B/GCLKC_3	I/O	DQ9	3	GCLKC_3	Comp_of_IOR29A	TRUE							
IOR2A	I/O	DQ11	2		True_of_IOR2B	TRUE							
IOR2B	I/O	DQ11	2		Comp_of_IOR2A	TRUE							
IOR30A/MODE0	I/O	DQ9	3	MODE0	True_of_IOR30B	NONE	88	144	113	88	144	144	88
IOR30B/MODE1	I/O	DQ9	3	MODE1	Comp_of_IOR30A	NONE	87	142	111	87	142	142	87

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS		EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOR31A/MODE2	I/O	DQ9	3	MODE2	True_of_IOR31B	TRUE	GND ^[4]	143	112	GND ^[4]	143	143	GND ^[4]
IOR31B/RECONFIG_N	I/O	DQ9	3	RECONFIG_N	Comp_of_IOR31A	TRUE	9	20	108	9	20	20	9
IOR32A/READY	I/O	DQ9	3	READY	True_of_IOR32B	NONE		22	109		22	22	
IOR32B/DONE	I/O	DQ9	3	DONE	Comp_of_IOR32A	NONE		21	107		21	21	
IOR33A/MI/D7	I/O	DQ9	3	MI/D7	True_of_IOR33B	TRUE	62	96	106	62	96	96	62
IOR33B/MO/D6	I/O	DQ9	3	MO/D6	Comp_of_IOR33A	TRUE	61		105				61
IOR34A/MCS_N/D5	I/O	DQ9	3	MCS_N/D5	True_of_IOR34B	NONE	60	94	104	60	94	94	60
IOR34B/MCLK/D4	I/O	DQ9	3	MCLK/D4	Comp_of_IOR34A	NONE	59	93	103	59	93	93	59
IOR35A/FASTRD_N/D3	I/O	DQ9	3	FASTRD_N /D3	True_of_IOR35B	TRUE	57	92	102	57	92	92	57
IOR35B/SI/D2	I/O	DQ9	3	SI/D2	Comp_of_IOR35A	TRUE		90	101		90	90	
IOR36A/SO/D1	I/O	DQS9	3	SO/D1	True_of_IOR36B	NONE	56	88	100	56	88	88	56
IOR36B/SSPI_CS_N/D0	I/O	DQS9	3	SSPI_CS_N/D 0	Comp_of_IOR36A	NONE	55	87	99	55	87	87	55
IOR38A/DIN/CLKHOLD_ N	I/O	DQ9	3	DIN/CLKHOLD _N	True_of_IOR38B	TRUE	54	86	98	54	86	86	54
IOR38B/DOUT/WE_N	I/O	DQ9	3	DOUT/WE_N	Comp_of_IOR38A	TRUE	53	85	97	53	85	85	53
IOR39A/SCLK	I/O	DQ9	3	SCLK	True_of_IOR39B	NONE	52	15	96	52	15	15	52
IOR39B	I/O	DQ9	3		Comp_of_IOR39A	NONE							
IOR3A	I/O	DQ11	2		True_of_IOR3B	NONE							
IOR3B	I/O	DQ11	2		Comp_of_IOR3A	NONE							
IOR40A	I/O	DQ9	3		True_of_IOR40B	TRUE							
IOR40B	I/O	DQ9	3		Comp_of_IOR40A	TRUE							
IOR41A	I/O	DQ9	3		True_of_IOR41B	NONE							
IOR41B	I/O	DQ9	3		Comp_of_IOR41A	NONE							
IOR42A	I/O	DQ9	3		True_of_IOR42B	TRUE		84				84	
IOR42B	I/O	DQ9	3		Comp_of_IOR42A	TRUE		83			83	83	
IOR43A	I/O	DQ9	3		True_of_IOR43B	NONE							
IOR43B	I/O	DQ9	3		Comp_of_IOR43A	NONE							
IOR44A	I/O	DQ9	3		True_of_IOR44B	TRUE							
IOR44B	I/O	DQ9	3		Comp_of_IOR44A	TRUE							
IOR45A/RPLL2_T_in	I/O	DQ9	3	RPLL2_T_in	True_of_IOR45B		51	82	93	51	82	82	51
IOR45B/RPLL2_C_in	I/O	DQ9	3	RPLL2_C_in	Comp_of_IOR45A	NONE							

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.
 [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOR47A/RPLL2_T_fb	I/O	DQ8	3	RPLL2_T_fb	True_of_IOR47B	TRUE			92				
IOR47B/RPLL2_C_fb	I/O	DQ8	3	RPLL2_C_fb	Comp_of_IOR47A	TRUE							
IOR48A	I/O	DQ8	3		True_of_IOR48B	NONE							
IOR48B	I/O	DQ8	3		Comp_of_IOR48A	NONE							
IOR49A	I/O	DQ8	3		True_of_IOR49B	TRUE	49	80		49	80	80	49
IOR49B	I/O	DQ8	3		Comp_of_IOR49A	TRUE	48	79		48	79	79	48
IOR4A	I/O	DQ11	2		True_of_IOR4B	TRUE							
IOR4B	I/O	DQ11	2		Comp_of_IOR4A	TRUE							
IOR50A	I/O	DQS8	3		True_of_IOR50B	NONE		78			78	78	
IOR50B	I/O	DQS8	3		Comp_of_IOR50A	NONE		76			76	76	
IOR51A	I/O	DQ8	3		True_of_IOR51B	TRUE							
IOR51B	I/O	DQ8	3		Comp_of_IOR51A	TRUE							
IOR52A	I/O	DQ8	3		True_of_IOR52B	NONE							
IOR52B	I/O	DQ8	3		Comp_of_IOR52A	NONE							
IOR53A	I/O	DQ8	3		True_of_IOR53B	TRUE							
IOR53B	I/O	DQ8	3		Comp_of_IOR53A	TRUE							
IOR54A	I/O	DQ8	3		True_of_IOR54B	NONE							
IOR54B	I/O	DQ8	3		Comp_of_IOR54A	NONE							
IOR5A	I/O	DQ11	2		True_of_IOR5B	NONE							
IOR5B	I/O	DQ11	2		Comp_of_IOR5A	NONE							
IOR6A	I/O	DQS11	2		True_of_IOR6B	TRUE							
IOR6B	I/O	DQS11	2		Comp_of_IOR6A	TRUE							
IOR7A/RPLL1_T_in	I/O	DQ11	2	RPLL1_T_in	True_of_IOR7B	NONE		106	129		106	106	
IOR7B/RPLL1_C_in	I/O	DQ11	2	RPLL1_C_in	Comp_of_IOR7A	NONE		105	128		105	105	
IOR8A/RPLL1_T_fb	I/O	DQ11	2	RPLL1_T_fb	True_of_IOR8B	TRUE							
IOR8B/RPLL1_C_fb	I/O	DQ11	2	RPLL1_C_fb	Comp_of_IOR8A	TRUE							
IOR9A	I/O	DQ11	2		True_of_IOR9B	NONE							
IOR9B	I/O	DQ11	2		Comp_of_IOR9A	NONE							
IOT12A	I/O	DQ14	0		True_of_IOT12B	TRUE		134	169		134	134	
IOT12B	I/O	DQ14	0		Comp_of_IOT12A	TRUE		133	168		133	133	
IOT13A	I/O	DQ14	0		True_of_IOT13B	NONE							
IOT13B	I/O	DQ14	0		Comp_of_IOT13A	NONE							
IOT14A	I/O	DQ14	0		True_of_IOT14B	TRUE		132	167		132	132	

GO₩IN

- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOT14B	I/O	DQ14	0		Comp_of_IOT14A	TRUE		131	166		131	131	
IOT15A	I/O	DQ14	0		True_of_IOT15B	NONE							
IOT15B	I/O	DQ14	0		Comp_of_IOT15A	NONE							
IOT16A	I/O	DQ14	0		True_of_IOT16B	TRUE			165				
IOT16B	I/O	DQ14	0		Comp_of_IOT16A	TRUE			164				
IOT17A	I/O	DQ14	0		True_of_IOT17B	NONE	82	130		82	130	130	82
IOT17B	I/O	DQ14	0		Comp_of_IOT17A	NONE	81	129		81	129	129	81
IOT18A	I/O	DQ14	0		True_of_IOT18B	TRUE			163				
IOT18B	I/O	DQ14	0		Comp_of_IOT18A	TRUE			162				
IOT19A	I/O	DQ14	0		True_of_IOT19B	NONE		128			128	128	
IOT19B	I/O	DQ14	0		Comp_of_IOT19A	NONE							
IOT20A	I/O	DQ14	0		True_of_IOT20B	TRUE							
IOT20B	I/O	DQ14	0		Comp_of_IOT20A	TRUE							
IOT21A	I/O	DQS14	0		True_of_IOT21B	NONE			161				
IOT21B	I/O	DQS14	0		Comp_of_IOT21A	NONE			160				
IOT22A	I/O	DQ14	0		True_of_IOT22B	TRUE		125			125	125	
IOT22B	I/O	DQ14	0		Comp_of_IOT22A	TRUE							
IOT23A	I/O	DQ14	0		True_of_IOT23B	NONE		126			126	126	
IOT23B	I/O	DQ14	0		Comp_of_IOT23A	NONE		124			124	124	
IOT24A	I/O	DQ14	0		True_of_IOT24B	TRUE			159				
IOT24B	I/O	DQ14	0		Comp_of_IOT24A	TRUE			158				
IOT25A	I/O	DQ14	0		True_of_IOT25B	NONE							
IOT25B	I/O	DQ14	0		Comp_of_IOT25A	NONE							
IOT26A	I/O	DQ14	0		True_of_IOT26B	TRUE							
IOT26B	I/O	DQ14	0		Comp_of_IOT26A	TRUE							
IOT27A/GCLKT_0	I/O	DQ14	0	GCLKT_0	True_of_IOT27B	NONE	80	123	157	80	123	123	80
IOT27B/GCLKC_0	I/O	DQ14	0	GCLKC_0	Comp_of_IOT27A	NONE	79	122	156	79	122	122	79
IOT2A	I/O	DQ15	0		True_of_IOT2B	TRUE							
IOT2B	I/O	DQ15	0		Comp_of_IOT2A	TRUE		141			141	141	
IOT30A/GCLKT_1	I/O	DQ13	1	GCLKT_1	True_of_IOT30B	TRUE	77	121	152	77	121	121	77
IOT30B/GCLKC_1	I/O	DQ13	1	GCLKC_1	Comp_of_IOT30A	TRUE	76	120	151	76	120	120	76
IOT31A	I/O	DQ13	1		True_of_IOT31B	NONE							
IOT31B	I/O	DQ13	1		Comp_of_IOT31A	NONE							

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
 [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOT32A	I/O	DQ13	1		True_of_IOT32B	TRUE							
IOT32B	I/O	DQ13	1		Comp_of_IOT32A	TRUE							
IOT33A	I/O	DQ13	1		True_of_IOT33B	NONE							
IOT33B	I/O	DQ13	1		Comp_of_IOT33A	NONE							
IOT34A	I/O	DQ13	1		True_of_IOT34B	TRUE	75			75			75
IOT34B	I/O	DQ13	1		Comp_of_IOT34A	TRUE	74			74			74
IOT35A	I/O	DQ13	1		True_of_IOT35B	NONE							
IOT35B	I/O	DQ13	1		Comp_of_IOT35A	NONE							
IOT36A	I/O	DQ13	1		True_of_IOT36B	TRUE							
IOT36B	I/O	DQ13	1		Comp_of_IOT36A	TRUE							
IOT37A	I/O	DQS13	1		True_of_IOT37B	NONE			150				
IOT37B	I/O	DQS13	1		Comp_of_IOT37A	NONE			149				
IOT38A	I/O	DQ13	1		True_of_IOT38B	TRUE		119	148		119	119	
IOT38B	I/O	DQ13	1		Comp_of_IOT38A	TRUE		118	147		118	118	
IOT39A	I/O	DQ13	1		True_of_IOT39B	NONE							
IOT39B	I/O	DQ13	1		Comp_of_IOT39A	NONE							
IOT3A	I/O	DQ15	0		True_of_IOT3B	NONE							
IOT3B	I/O	DQ15	0		Comp_of_IOT3A	NONE							
IOT40A	I/O	DQ13	1		True_of_IOT40B	TRUE	73	117	146	73	117	117	73
IOT40B	I/O	DQ13	1		Comp_of_IOT40A	TRUE	72	116	145	72	116	116	72
IOT41A	I/O	DQ13	1		True_of_IOT41B	NONE							
IOT41B	I/O	DQ13	1		Comp_of_IOT41A	NONE							
IOT42A	I/O	DQ13	1		True_of_IOT42B	TRUE		115	144		115	115	
IOT42B	I/O	DQ13	1		Comp_of_IOT42A	TRUE		114	143		114	114	
IOT43A	I/O	DQ13	1		True_of_IOT43B	NONE							
IOT43B	I/O	DQ13	1		Comp_of_IOT43A	NONE							
IOT44A	I/O	DQ13	1		True_of_IOT44B	TRUE	71		142	71			71
IOT44B	I/O	DQ13	1		Comp_of_IOT44A	TRUE	70		141	70			70
IOT45A	I/O	DQ13	1		True_of_IOT45B	NONE							
IOT45B	I/O	DQ13	1		Comp_of_IOT45A	NONE							
IOT48A	I/O	DQS12	1		True_of_IOT48B	TRUE		113	140		113	113	
IOT48B	I/O	DQS12	1		Comp_of_IOT48A	TRUE		112	139		112	112	
IOT49A	I/O	DQ12	1		True_of_IOT49B	NONE							

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.
 [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOT49B	I/O	DQ12	1		Comp_of_IOT49A	NONE							
IOT4A	I/O	DQ15	0		True_of_IOT4B	TRUE	86	140		86	140		86
IOT4B	I/O	DQ15	0		Comp_of_IOT4A	TRUE	85	139	174	85	139	139	85
IOT50A	I/O	DQ12	1		True_of_IOT50B	TRUE	69	111	138	69	111	111	69
IOT50B	I/O	DQ12	1		Comp_of_IOT50A	TRUE		110	137		110	110	
IOT51A	I/O	DQ12	1		True_of_IOT51B	NONE							
IOT51B	I/O	DQ12	1		Comp_of_IOT51A	NONE							
IOT52A	I/O	DQ12	1		True_of_IOT52B	TRUE			136				
IOT52B	I/O	DQ12	1		Comp_of_IOT52A	TRUE			135				
IOT53A	I/O	DQ12	1		True_of_IOT53B	NONE							
IOT53B	I/O	DQ12	1		Comp_of_IOT53A	NONE							
IOT54A	I/O	DQ12	1		True_of_IOT54B	TRUE							
IOT54B	I/O	DQ12	1		Comp_of_IOT54A	TRUE							
IOT55A	I/O	DQ12	1		True_of_IOT55B	NONE							
IOT55B/JTAGSEL_N	I/O	DQ12	1	JTAGSEL_N	Comp_of_IOT55A	NONE							
IOT5A	I/O	DQ15	0		True_of_IOT5B	NONE							
IOT5B	I/O	DQ15	0		Comp_of_IOT5A	NONE							
IOT6A	I/O	DQ15	0		True_of_IOT6B	TRUE	84	138	173	84	138	138	84
IOT6B	I/O	DQ15	0		Comp_of_IOT6A	TRUE	83	137	172	83	137		83
IOT7A	I/O	DQ15	0		True_of_IOT7B	NONE		136			136	136	
IOT7B	I/O	DQ15	0		Comp_of_IOT7A	NONE		135			135	135	
IOT8A	I/O	DQ15	0		True_of_IOT8B	TRUE							
IOT8B	I/O	DQ15	0		Comp_of_IOT8A	TRUE							
IOT9A	I/O	DQS15	0		True_of_IOT9B	NONE			171				
IOT9B	I/O	DQS15	0		Comp_of_IOT9A	NONE			170				
VCC	Power		N/A				1			1			1
VCC	Power		N/A				22		44	22			22
VCC	Power		N/A				45		89	45			45
VCC	Power		N/A				66		132	66			66
VCC	Power		N/A						1				
VCC	Power		N/A										
VCC/VCCPLLL1	Power		N/A					1					
VCC/VCCPLLL1	Power		N/A					36					

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.
 [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
VCC/VCCPLLL1	Power		N/A					73					
VCC/VCCPLLL1	Power		N/A					108					
VCC/VCCPLLL1	Power		N/A								1	1	
VCC/VCCPLLL1	Power		N/A								36	36	
VCC/VCCPLLL1	Power		N/A								73	73	
VCC/VCCPLLL1	Power		N/A								108	108	
VCCIO0	Power		N/A				78		155	78			78
VCCIO0	Power		N/A					127			127	127	
VCCIO0	Power		N/A						176				
VCCIO1	Power		N/A				67	109	133		109	109	
VCCIO1	Power		N/A						153				
VCCIO2	Power		N/A									103	64
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						5				
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						13				
6/VCCIO/	Power		N/A						22				
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						40				
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						95				
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						110				
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						118				
VCCIO2/VCCIO3/VCCIO 6/VCCIO7	Power		N/A						130				
VCCIO2/VCCIO7	Power		N/A								5		
VCCIO2/VCCIO7	Power		N/A								19		
VCCIO2/VCCIO7	Power		N/A								103		
VCCIO2/VCCIO7	Power		N/A							3			
VCCIO2/VCCIO7	Power		N/A							64			

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
VCCIO3	Power		N/A				58	91		58		91	58
VCCIO3	Power		N/A					77			77	77	
VCCIO4	Power		N/A				44		88	44			44
VCCIO4	Power		N/A					55	67				
VCCIO5	Power		N/A				23	37	45	23	37	37	23
VCCIO5	Power		N/A						65				
VCCIO7	Power		N/A									5	3
VCCIO7	Power		N/A									19	
VCCPLLL	Power		N/A										
VCCPLLL0	Power		N/A					8			8	8	
VCCPLLL1	Power		N/A				14		34	14			14
VCCPLLR	Power		N/A										
VCCPLLR0	Power		N/A					104	127		104	104	
VCCPLLR1	Power		N/A				50	81	94	50	81	81	50
VCCX	Power		N/A						23				
VCCX	Power		N/A						66				
VCCX	Power		N/A						115				
VCCX	Power		N/A						154				
VCCX/VCCIO1/VCCIO6	Power		N/A							12			12
VCCX/VCCIO1/VCCIO6	Power		N/A							67			67
VCCX/VCCIO2/	Power		N/A				3						
VCCIO6/VCCIO7	rowei		IN/A				3						<u> </u>
VCCX/VCCIO2/	Power		N/A				12						
VCCIO6/VCCIO7	rowei		IN/A				12						
VCCX/VCCIO2/	Power		N/A				64						
VCCIO6/VCCIO7	rowei		IN/A				04						
VCCX/VCCIO2/	Power		N/A					5					
VCCIO6/VCCIO7	I OWEI		IN/A					3					
VCCX/VCCIO2/	Power		N/A					19					
VCCIO6/VCCIO7	1 OWGI		14/7					13					
VCCX/VCCIO2/ VCCIO6/VCCIO7	Power		N/A					31					

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor" indicates the pin is connected to the ground with 10K resistance.
- [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
VCCX/VCCIO2/ VCCIO6/VCCIO7	Power		N/A					103					
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.
 [4] The pin is internally grounded.

[1] The partie internally great													
Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO2/ VCCIO3/VCCIO6/ VCCIO7	Power		N/A										
VCCX/VCCIO4/VCCIO6	Power		N/A									31	
VCCX/VCCIO4/VCCIO6	Power		N/A								55	55	
VSS	Ground		N/A					2	2	2	2		2
VSS	Ground		N/A				21			21			21
VSS	Ground		N/A				24		-	24			24
VSS	Ground		N/A				43			43			43

Pin List



- [1] It is embedded with SDRAM.
- [2] It is embedded with PSRAM.
- [3] "Tie to VSS by 10K Resisitor"indicates the pin is connected to the ground with 10K resistance.
 [4] The pin is internally grounded.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
VSS	Ground		N/A				46	74	90	46	74	74	46
VSS	Ground		N/A				65		131	65	107	107	65
VSS	Ground		N/A				68			68			68
VSS	Ground		N/A					17	134		17	17	
VSS	Ground		N/A					53	175		53	53	
VSS	Ground		N/A					89			89	89	
VSS	Ground		N/A					107					
VSS	Ground		N/A						43				
VSS	Ground		N/A						46				
VSS	Ground		N/A						87				
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
VSS	Ground		N/A										
NC	N/A		N/A										



Note!

[1] It is embedded with SDRAM. [2] It is embedded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
BANK7 True LVDS Pa	ir												
IOL11A	I/O	DQ1	7		True_of_IOL11B	TRUE							
IOL11B	I/O	DQ1	7		Comp_of_IOL11A	TRUE							
IOL13A	I/O	DQ1	7		True_of_IOL13B	TRUE							
IOL13B	I/O	DQ1	7		Comp_of_IOL13A	TRUE							
IOL15A	I/O	DQ1	7		True_of_IOL15B	TRUE			8				
IOL15B	I/O	DQ1	7		Comp_of_IOL15A	TRUE			9				
IOL17A	I/O	DQ1	7		True_of_IOL17B	TRUE			10				
IOL17B	I/O	DQ1	7		Comp_of_IOL17A	TRUE			11				
IOL20A	I/O	DQ1	7		True_of_IOL20B	TRUE							
IOL20B	I/O	DQ1	7		Comp_of_IOL20A	TRUE							
IOL22A	I/O	DQS1	7		True_of_IOL22B	TRUE		9			9	9	
IOL22B	I/O	DQS1	7		Comp_of_IOL22A	TRUE		10			10	10	
IOL24A	I/O	DQ1	7		True_of_IOL24B	TRUE			15				
IOL24B	I/O	DQ1	7		Comp_of_IOL24A	TRUE			16				
IOL26A	I/O	DQ1	7		True_of_IOL26B	TRUE			17				
IOL26B	I/O	DQ1	7		Comp_of_IOL26A	TRUE			19				
IOL2A	I/O	DQ0	7		True_of_IOL2B	TRUE		3	3		3	3	
IOL2B	I/O	DQ0	7		Comp_of_IOL2A	TRUE		4	4		4	4	
IOL4A	I/O	DQ0	7		True_of_IOL4B	TRUE							
IOL4B	I/O	DQ0	7		Comp_of_IOL4A	TRUE							
IOL6A	I/O	DQS0	7		True_of_IOL6B	TRUE							
IOL6B	I/O	DQS0	7		Comp_of_IOL6A	TRUE							
IOL8A/LPLL1_T_fb	I/O	DQ0	7	LPLL1_T_fb	True_of_IOL8B	TRUE							
IOL8B/LPLL1_C_fb	I/O	DQ0	7	LPLL1_C_fb	Comp_of_IOL8A	TRUE							
BANK6 True LVDS Pa	ir				<u> </u>								
IOL29A/GCLKT_6	I/O	DQ2	6	GCLKT_6	True_of_IOL29B	TRUE	10	25		10	25	25	10
IOL29B/GCLKC_6	I/O	DQ2	6	GCLKC_6	Comp_of_IOL29A	TRUE	11	26		11	26	26	11
IOL31A	I/O	DQ2	6		True_of_IOL31B	TRUE							
IOL31B	I/O	DQ2	6		Comp_of_IOL31A	TRUE							
IOL33A	I/O	DQ2	6		True_of_IOL33B	TRUE		27			27	27	
IOL33B	I/O	DQ2	6		Comp_of_IOL33A	TRUE		28			28	28	
IOL35A	I/O	DQ2	6		True_of_IOL35B	TRUE							
IOL35B	I/O	DQ2	6		Comp_of_IOL35A	TRUE							



Note!

[1] It is embedded with SDRAM. [2] It is embedded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOL38A	I/O	DQ2	6		True_of_IOL38B	TRUE			24				
IOL38B	I/O	DQ2	6		Comp_of_IOL38A	TRUE			25				
IOL40A	I/O	DQ2	6		True_of_IOL40B	TRUE			26				
IOL40B	I/O	DQ2	6		Comp_of_IOL40A	TRUE			27				
IOL42A	I/O	DQ2	6		True_of_IOL42B	TRUE		32	28		32	32	
IOL42B	I/O	DQ2	6		Comp_of_IOL42A	TRUE		33	29		33	33	
IOL44A	I/O	DQ2	6		True_of_IOL44B	TRUE			30				
IOL44B	I/O	DQ2	6		Comp_of_IOL44A	TRUE			31				
IOL47A/LPLL2_T_fb	I/O	DQ3	6	LPLL2_T_fb	True_of_IOL47B	TRUE	15		35	15			15
IOL47B/LPLL2_C_fb	I/O	DQ3	6	LPLL2_C_fb	Comp_of_IOL47A	TRUE	16		36	16			16
IOL49A	I/O	DQ3	6		True_of_IOL49B	TRUE	17			17			17
IOL49B	I/O	DQ3	6		Comp_of_IOL49A	TRUE	18			18			18
IOL51A	I/O	DQ3	6		True_of_IOL51B	TRUE	19			19			19
IOL51B	I/O	DQ3	6		Comp_of_IOL51A	TRUE	20			20			20
IOL53A	I/O	DQ3	6		True_of_IOL53B	TRUE			41				
IOL53B	I/O	DQ3	6		Comp_of_IOL53A	TRUE			42				
BANK5 True LVDS Pair													
IOB12A	I/O	DQ5	5		True_of_IOB12B	TRUE		44	53		44	44	
IOB12B	I/O	DQ5	5		Comp_of_IOB12A	TRUE		45	54		45	45	
IOB14A	I/O	DQ5	5		True_of_IOB14B	TRUE	29	46	55	29	46	46	29
IOB14B	I/O	DQ5	5		Comp_of_IOB14A	TRUE	30	47	56	30	47	47	30
IOB16A	I/O	DQ5	5		True_of_IOB16B	TRUE							
IOB16B	I/O	DQ5	5		Comp_of_IOB16A	TRUE							
IOB18A	I/O	DQ5	5		True_of_IOB18B	TRUE	31		59	31			31
IOB18B	I/O	DQ5	5		Comp_of_IOB18A	TRUE	32		60	32			32
IOB20A	I/O	DQ5	5		True_of_IOB20B	TRUE		50			50	50	
IOB20B	I/O	DQ5	5		Comp_of_IOB20A	TRUE		51			51	51	
IOB22A	I/O	DQ5	5		True_of_IOB22B	TRUE		52			52	52	
IOB22B		DQ5	5		Comp_of_IOB22A	TRUE		54			54	54	
IOB24A	I/O	DQ5	5		True_of_IOB24B	TRUE	33			33			33
IOB24B	I/O	DQ5	5		Comp_of_IOB24A	TRUE	34			34			34
IOB26A	I/O	DQ5	5		True_of_IOB26B	TRUE							
IOB26B	I/O	DQ5	5		Comp_of_IOB26A	TRUE							
IOB2A	I/O	DQ4	5		True_of_IOB2B	TRUE							



Note!

[1] It is embedded with SDRAM.

[2] It is embedded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOB2B	I/O	DQ4	5		Comp_of_IOB2A	TRUE							
IOB4A	I/O	DQ4	5		True_of_IOB4B	TRUE							
IOB4B	I/O	DQ4	5		Comp_of_IOB4A	TRUE							
IOB6A	I/O	DQ4	5		True_of_IOB6B	TRUE		40	49	25	40	40	25
IOB6B	I/O	DQ4	5		Comp_of_IOB6A	TRUE	26	41	50	26	41	41	26
IOB8A	I/O	DQ4	5		True_of_IOB8B	TRUE	27		51	27			27
IOB8B	I/O	DQ4	5		Comp_of_IOB8A	TRUE	28		52	28			28
BANK4 True LVDS Pair	•												
IOB30A/GCLKT_4	I/O	DQ6	4	GCLKT_4	True_of_IOB30B	TRUE	35	56	68	35	56	56	35
IOB30B/GCLKC_4	I/O	DQ6	4	GCLKC_4	Comp_of_IOB30A	TRUE	36	57	69	36	57	57	36
IOB32A	I/O	DQ6	4		True_of_IOB32B	TRUE							
IOB32B	I/O	DQ6	4		Comp_of_IOB32A	TRUE							
IOB34A	I/O	DQ6	4		True_of_IOB34B	TRUE	37	60	70	37	60	60	37
IOB34B	I/O	DQ6	4		Comp_of_IOB34A	TRUE	38	61	71	38	61	61	38
IOB36A	I/O	DQ6	4		True_of_IOB36B	TRUE							
IOB36B	I/O	DQ6	4		Comp_of_IOB36A	TRUE							
IOB38A	I/O	DQ6	4		True_of_IOB38B	TRUE		62	74		62	62	
IOB38B	I/O	DQ6	4		Comp_of_IOB38A	TRUE		63	75		63	63	
IOB40A	I/O	DQ6	4		True_of_IOB40B	TRUE	39	64	76	39	64	64	39
IOB40B	I/O	DQ6	4		Comp_of_IOB40A	TRUE	40	65	77	40	65	65	40
IOB42A	I/O	DQ6	4		True_of_IOB42B	TRUE		66	78		66	66	
IOB42B	I/O	DQ6	4		Comp_of_IOB42A	TRUE		67	79		67	67	
IOB44A	I/O	DQ6	4		True_of_IOB44B	TRUE			80				
IOB44B	I/O	DQ6	4		Comp_of_IOB44A	TRUE			81				
IOB48A	I/O	DQS7	4		True_of_IOB48B	TRUE		68	82		68	68	
IOB48B	I/O	DQS7	4		Comp_of_IOB48A	TRUE		69	83		69	69	
IOB50A	I/O	DQ7	4		True_of_IOB50B	TRUE			84				
IOB50B	I/O	DQ7	4		Comp_of_IOB50A	TRUE			85				
IOB52A	I/O	DQ7	4		True_of_IOB52B	TRUE							
IOB52B	I/O	DQ7	4		Comp_of_IOB52A	TRUE							
IOB54A	I/O	DQ7	4		True_of_IOB54B	TRUE							
IOB54B	I/O	DQ7	4		Comp_of_IOB54A	TRUE							



Note!

[1] It is embedded with SDRAM. [2] It is embedded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
BANK3 True LVDS Pair	•												
IOR29A/GCLKT_3	I/O	DQ9	3	GCLKT_3	True_of_IOR29B	TRUE							
IOR29B/GCLKC_3	I/O	DQ9	3	GCLKC_3	Comp_of_IOR29A	TRUE							
IOR31A/MODE2	I/O	DQ9	3	MODE2	True_of_IOR31B	TRUE		143	112		143	143	
IOR31B/RECONFIG_N	I/O	DQ9	3	RECONFIG_N	Comp_of_IOR31A	TRUE		20	108		20	20	
IOR33A/MI/D7	I/O	DQ9	3	MI/D7	True_of_IOR33B	TRUE	62	96	106	62	96	96	62
IOR33B/MO/D6	I/O	DQ9	3	MO/D6	Comp_of_IOR33A	TRUE	61	95	105	61	95	95	61
IOR35A/FASTRD_N/D3	I/O	DQ9	3	FASTRD_N /D3	True_of_IOR35B	TRUE		92	102		92	92	
IOR35B/SI/D2	I/O	DQ9	3	SI/D2	Comp_of_IOR35A	TRUE		90	101		90	90	
IOR38A/DIN/CLKHOLD _N	I/O	DQ9	3	DIN/CLKHOLD_ N	True_of_IOR38B	TRUE	54	86	98	54	86	86	54
IOR38B/DOUT/WE_N	I/O	DQ9	3	DOUT/WE_N	Comp_of_IOR38A	TRUE	53	85	97	53	85	85	53
IOR40A	I/O	DQ9	3		True_of_IOR40B	TRUE							
IOR40B	I/O	DQ9	3		Comp_of_IOR40A	TRUE							
IOR42A	I/O	DQ9	3		True_of_IOR42B	TRUE		84			84	84	
IOR42B	I/O	DQ9	3		Comp_of_IOR42A	TRUE		83			83	83	
IOR44A	I/O	DQ9	3		True_of_IOR44B	TRUE							
IOR44B	I/O	DQ9	3		Comp_of_IOR44A	TRUE							
IOR47A/RPLL2_T_fb	I/O	DQ8	3	RPLL2_T_fb	True_of_IOR47B	TRUE							
IOR47B/RPLL2_C_fb	I/O	DQ8	3	RPLL2_C_fb	Comp_of_IOR47A	TRUE							
IOR49A	I/O	DQ8	3		True_of_IOR49B	TRUE	49	80		49	80	80	49
IOR49B	I/O	DQ8	3		Comp_of_IOR49A	TRUE	48	79		48	79	79	48
IOR51A	I/O	DQ8	3		True_of_IOR51B	TRUE							
IOR51B	I/O	DQ8	3		Comp_of_IOR51A	TRUE							
IOR53A	I/O	DQ8	3		True_of_IOR53B	TRUE							
IOR53B	I/O	DQ8	3		Comp_of_IOR53A	TRUE							
BANK2 True LVDS Pair													
IOR11A	I/O	DQ10	2		True_of_IOR11B	TRUE							
IOR11B	I/O	DQ10	2		Comp_of_IOR11A	TRUE							
IOR13A	I/O	DQ10	2		True_of_IOR13B	TRUE							
IOR13B	I/O	DQ10	2		Comp_of_IOR13A	TRUE							
IOR15A	I/O	DQ10	2		True_of_IOR15B	TRUE							
IOR15B	I/O	DQ10	2		Comp_of_IOR15A	TRUE							
IOR17A	I/O	DQ10	2		True_of_IOR17B	TRUE							



Note!

[1] It is embedded with SDRAM. [2] It is embedded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOR17B	I/O	DQ10	2		Comp_of_IOR17A	TRUE							
IOR20A	I/O	DQ10	2		True_of_IOR20B	TRUE		102	125		102	102	
IOR20B	I/O	DQ10	2		Comp_of_IOR20A	TRUE		101	124		101	101	
IOR22A		DQS10	2		True_of_IOR22B	TRUE		100	123		100	100	
IOR22B	I/O	DQS10	2		Comp_of_IOR22A	TRUE		99	122		99	99	
IOR24A	I/O	DQ10	2		True_of_IOR24B	TRUE							
IOR24B	I/O	DQ10	2		Comp_of_IOR24A	TRUE							
IOR26A/TCK	I/O	DQ10	2	TCK	True_of_IOR26B	TRUE	6	14	120	6	14	14	6
IOR26B/TDI	I/O	DQ10	2	TDI	Comp_of_IOR26A	TRUE	7	16	117	7	16	16	7
IOR2A	I/O	DQ11	2		True_of_IOR2B	TRUE							
IOR2B	I/O	DQ11	2		Comp_of_IOR2A	TRUE							
IOR4A	I/O	DQ11	2		True_of_IOR4B	TRUE							
IOR4B	I/O	DQ11	2		Comp_of_IOR4A	TRUE							
IOR6A	I/O	DQS11	2		True_of_IOR6B	TRUE							
IOR6B	I/O	DQS11	2		Comp_of_IOR6A	TRUE							
IOR8A/RPLL1_T_fb	I/O	DQ11	2	RPLL1_T_fb	True_of_IOR8B	TRUE							
IOR8B/RPLL1_C_fb	I/O	DQ11	2	RPLL1_C_fb	Comp_of_IOR8A	TRUE							
BANK1 True LVDS Pair	•												
IOT30A/GCLKT_1	I/O	DQ13	1	GCLKT_1	True_of_IOT30B	TRUE	77	121	152	77	121	121	77
IOT30B/GCLKC_1	I/O	DQ13	1	GCLKC_1	Comp_of_IOT30A	TRUE	76	120	151	76	120	120	76
IOT32A	I/O	DQ13	1		True_of_IOT32B	TRUE							
IOT32B	I/O	DQ13	1		Comp_of_IOT32A	TRUE							
IOT34A	I/O	DQ13	1		True_of_IOT34B	TRUE	75			75			75
IOT34B	I/O	DQ13	1		Comp_of_IOT34A	TRUE	74			74			74
IOT36A	I/O	DQ13	1		True_of_IOT36B	TRUE							
IOT36B	I/O	DQ13	1		Comp_of_IOT36A	TRUE							
IOT38A	I/O	DQ13	1		True_of_IOT38B	TRUE		119	148		119	119	
IOT38B	I/O	DQ13	1		Comp_of_IOT38A	TRUE		118	147		118	118	
IOT40A	I/O	DQ13	1		True_of_IOT40B	TRUE	73	117	146	73	117	117	73
IOT40B	I/O	DQ13	1		Comp_of_IOT40A	TRUE	72	116	145	72	116	116	72
IOT42A	I/O	DQ13	1		True_of_IOT42B	TRUE		115	144		115	115	
IOT42B	I/O	DQ13	1		Comp_of_IOT42A	TRUE		114	143		114	114	
IOT44A	I/O	DQ13	1		True_of_IOT44B	TRUE	71		142	71			71
IOT44B	I/O	DQ13	1		Comp_of_IOT44A	TRUE	70		141	70			70



Note!

[1] It is embedded with SDRAM.

[2] It is embedded with PSRAM.

Pin Name	Function	DQS	BANK	Configuration Function	Differential Pair	LVDS	QN88 ^[1]	EQ144 ^[1]	EQ176 ^[1]	QN88P ^[2]	EQ144P ^[2]	EQ144PF ^[2]	QN88PF ^[2]
IOT48A		DQS12	1		True_of_IOT48B	TRUE		113	140		113	113	
IOT48B	I/O	DQS12	1		Comp_of_IOT48A	TRUE		112	139		112	112	
IOT50A	I/O	DQ12	1		True_of_IOT50B	TRUE		111	138		111	111	
IOT50B		DQ12	1		Comp_of_IOT50A	TRUE		110	137		110	110	
IOT52A		DQ12	1		True_of_IOT52B	TRUE			136				
IOT52B	I/O	DQ12	1		Comp_of_IOT52A	TRUE			135				
IOT54A	I/O	DQ12	1		True_of_IOT54B	TRUE							
IOT54B	I/O	DQ12	1		Comp_of_IOT54A	TRUE							
BANK0 True LVDS Pair													
IOT12A	I/O	DQ14	0		True_of_IOT12B	TRUE		134	169		134	134	
IOT12B	I/O	DQ14	0		Comp_of_IOT12A	TRUE		133	168		133	133	
IOT14A	I/O	DQ14	0		True_of_IOT14B	TRUE		132	167		132	132	
IOT14B	I/O	DQ14	0		Comp_of_IOT14A	TRUE		131	166		131	131	
IOT16A	I/O	DQ14	0		True_of_IOT16B	TRUE			165				
IOT16B	I/O	DQ14	0		Comp_of_IOT16A	TRUE			164				
IOT18A	I/O	DQ14	0		True_of_IOT18B	TRUE			163				
IOT18B	I/O	DQ14	0		Comp_of_IOT18A	TRUE			162				
IOT20A	I/O	DQ14	0		True_of_IOT20B	TRUE							
IOT20B	I/O	DQ14	0		Comp_of_IOT20A	TRUE							
IOT22A	I/O	DQ14	0		True_of_IOT22B	TRUE							
IOT22B	I/O	DQ14	0		Comp_of_IOT22A	TRUE							
IOT24A	I/O	DQ14	0		True_of_IOT24B	TRUE			159				
IOT24B	I/O	DQ14	0		Comp_of_IOT24A	TRUE			158				
IOT26A		DQ14	0		True_of_IOT26B	TRUE							
IOT26B	I/O	DQ14	0		Comp_of_IOT26A	TRUE							
IOT2A	I/O	DQ15	0		True_of_IOT2B	TRUE							
IOT2B		DQ15	0		Comp_of_IOT2A	TRUE							
IOT4A		DQ15	0		True_of_IOT4B	TRUE	86	140		86	140	140	86
IOT4B	I/O	DQ15	0		Comp_of_IOT4A	TRUE	85	139		85	139	139	85
IOT6A		DQ15	0		True_of_IOT6B	TRUE	84	138	173	84	138	138	84
		DQ15	0		Comp_of_IOT6A	TRUE	83	137	172	83	137	137	83
IOT8A	I/O	DQ15	0		True_of_IOT8B	TRUE							
IOT8B	I/O	DQ15	0		Comp_of_IOT8A	TRUE							



Note!

VCCX should be greater than or equal to VCCIO.

Recommended Operating C	onditions of EQ144/QN88 Package Embedded with SDR SDRMA in GW2AR-18
Namo	Description

постиненто предина	on mondad operating contained or 1411,41100 t dendege 1 mondad with option the contained in						
Name	Description	Min.	Max.				
VCC	Core voltage	0.95V	1.05V				
VCCPLLL0/1	Left PLL 0/1 supply voltage, VCC/VCCPLLL1 in package LQ144 are internally connected.	0.95V	1.05V				
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V				
VCCIO0, VCCIO1, VCCIO4, VCCIO5	I/O Bank power supply voltage	1.14V	3.6V				
VCCIO2, VCCIO3, VCCIO6, VCCIO7	I/O Bank power supply voltage, connected to SDR SDRAM port	3.135V	3.6V				
VCCX/VCCIO2/ VCCIO6/VCCIO7	VCCX, VCCIO2, and VCCIO7 provide SDR SDRAM voltage; VCCX/VCCIO2/VCCIO6/VCCIO7 are internally connected.	3.135V	3.6V				

Note!

It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of EQ176 Package Embedded with DDR SDRMA in GW2AR-18

Name	Description	Min.	Max.
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCIO0, VCCIO1, VCCIO4, VCCIO5	I/O Bank power supply voltage	1.14V	3.6V
VCCIO2, VCCIO3, VCCIO6, VCCIO7	I/O Bank power supply voltage, connected to DDR SDRAM and provides power for DDR SDRAM.	2.3V	2.7V
VCCX	Auxiliary voltage	2.7V	3.6V

Note!

It is highly recommended that the epad connect to GND, but not a requirement.



Note!

VCCX should be greater than or equal to VCCIO.

Recommended Operating C	onditions of QN88P Package Embedded with PSRAM in GW2AR-18		
Name	Description	Min.	Max.
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCIO0, VCCIO3, VCCIO4, VCCIO5	I/O Bank power supply voltage	1.14V	3.6V
VCCIO2/7	I/O Bank power supply voltage, connected to PSRAM port. VCCIO2/VCCIO7 provides power for PSRAM.	1.71V	1.89V
VCCX/VCCIO1/VCCIO6	VCCX/VCCIO1/VCCIO6 are internally connected.	2.7V	3.6V

Note!

It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of EQ144P Package Embedded with PSRAM in G	n GW2AR-18
---	------------

Name	Description	Min.	Max.
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCIO0, VCCIO1, VCCIO3, VCCIO5	I/O Bank power supply voltage	1.14V	3.6V
VCCIO2/7	I/O Bank power supply voltage, connected to PSRAM port. VCCIO2/VCCIO7 provides power for PSRAM.	1.71V	1.89V
VCCX/VCCIO4/VCCIO6	VCCX/VCCIO4/VCCIO6 are internally connected.	2.7V	3.6V

Note!

It is highly recommended that the epad connect to GND, but not a requirement.



Note!

VCCX should be greater than or equal to VCCIO.

Recommended Operating	Conditions of EQ144PF Package Embedded with PSRAM in GW2AR-18
riocommonaca oporating	godinationic of Eq. () is a deliago Embodada with a orth in otter it to

Name	Description	Min.	Max.
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCIO0, VCCIO1, VCCIO2, VCCIO3, VCCIO5	I/O Bank power supply voltage	1.14V	3.465V
VCCIO7	I/O Bank power supply voltage, connected to PSRAM port. VCCIO7 provides power for PSRAM.	1.71V	1.89V
VCCX/VCCIO4/VCCIO6	VCCX/VCCIO4/VCCIO6 are internally connected.	2.7V	3.465V

Note!

It is highly recommended that the epad connect to GND, but not a requirement.

Recommended Operating Conditions of QN88PF Package Embedded with PSRAM in GW2AR-18

Name	Description	Min.	Max.
VCC	Core voltage	0.95V	1.05V
VCCPLLL0/1	Left PLL 0/1 supply voltage	0.95V	1.05V
VCCPLLR0/1	Right PLL 0/1 supply voltage	0.95V	1.05V
VCCIO0, VCCIO2, VCCIO3,	I/O Bank power supply voltage	1.14V	3.6V
VCCIO4, VCCIO5	livo Barik power supply voltage	1.14 V	3.0 V
VCCIO7	I/O Bank power supply voltage, connected to PSRAM port. VCCIO7 provides power for PSRAM.	1.71V	1.89V
VCCX/VCCIO1/VCCIO6	VCCX/VCCIO1/VCCIO6 are internally connected.	2.7V	3.6V

Note!

It is highly recommended that the epad connect to GND, but not a requirement.