Hardware Design Checklist and Guidelines: T13 F169 FPGA, SPI Active Parallel (x4) Configuration

Power Pin Checklist

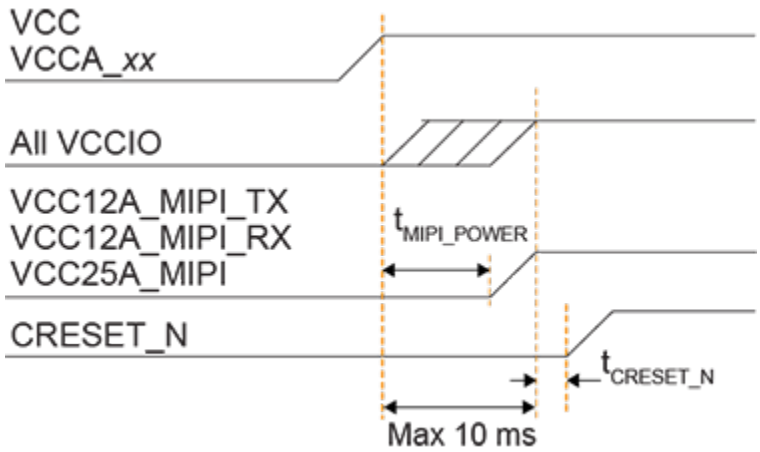
Check	Pin Name	Package Pins	Description
☐	All	All	Proper decoupling capacitors are placed near all power input pins. A good rule of thumb is to vary the use of 10 uF, 1 uF, 0.1 uF, 0.01 uF,and 1 nF capacitors per device power pin.
☐	All	All	My system follows the recommended power-up sequence (t_{CRESET_N} = 320 ns min and t_{MIPI_POWER} = 1 us min). See guideline.
☐	All	All	I have used the power estimator to ensure that the system power requirements are met.
☐	All	All	My system follows the connection requirements for unused resources and features. See guideline.
☐	VCC	E4 F7 F9 G5 G8 G9 H6 J6	The core supply voltage is 1.2 V +/- 50 mV or 1.1 V +/- 50 mV.
☐	VCC12A_MIPIx_xx	C3 E10 E6 E8	☐ The MIPI analog voltage is 1.2 V +/- 50 mV or 1.1 V +/- 50 mV. ☐The MIPI analog power supply has a separate filtering circuit. ☐ If you are not using the MIPI signals associated with this power pin, this pin is tied to VCC (1.2 V).
☐	VCC25A_MIPIx	E7 E9	☐ The MIPI analog voltage is 2.5 V +/- 5%. ☐ The MIPI analog power supply has a separate filtering circuit. ☐ If you are not using the MIPI RX channel associated with this power pin, this pin is tied to VCC (1.2 V).
☐	VCCA_xx	G10 G4 J10	☐ The PLL analog power supply is 1.2 V +/- 50 mV or 1.1 V +/- 50 mV. ☐ The PLL analog power supply has a separate filtering circuit. ☐ The PLL power pin is connected to VCC regardless of whether you are using the PLL or not.
☐	VCCIOxx	F10 F4 H10 H4 H5 H7 H8 H9 J4 J5 J9	☐ The VCCIO voltage is 1.8 V, 2.5 V, or 3.3 V. ☐ All I/O banks with LVDS pins use 3.3 V. ☐ The VCCIO voltage matches the external configuration interfaces.

Power Pin General Guidelines

Recommended Power Up Sequence

1. Power up VCC and VCCA_xx first.
2. When VCC and VCCA_xx are stable, power up all VCCIO pins. There is no specific timing delay between the VCCIO pins.
3. Apply power to VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI at least t_{MIPI_POWER} after VCC is stable. Note: Connect VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI to VCC when you are not using the MIPI instance.
4. After all power supplies are stable, hold CRESET_N low for a duration of t_{CRESET_N} (320 ns min) before asserting CRESET_N from low to high to trigger active SPI programming (the FPGA loads the configuration data from an external flash device).

Power-Up Sequence



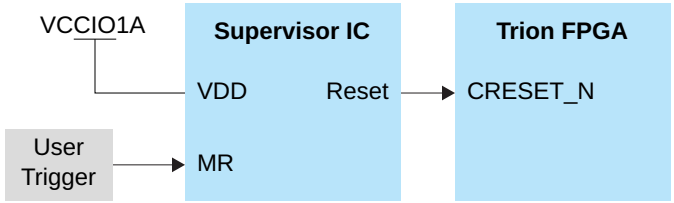
Holding CRESET_N Low

Use one of the following methods to hold the CRESET_N pin of the FPGA low after the power supplies are stable:

- Supervisor integrated circuit (IC)
- Microprocessor or microcontroller

Important: Do not drive a signal to any I/O pins before the FPGA is powered up. Most FPGAs have electrostatic discharge (ESD) circuits to protect the devices from ESD events. Driving the I/O pins before VCCIO will result in an in-rush current driving the I/O pins to a specific voltage through the ESD circuit to the VCCIO rail. Titanium FPGAs will remain in configuration mode after power-up if this unexpected voltage exists on CRESET_N due to the improper power-up sequence

Supervisor IC Circuitry Example

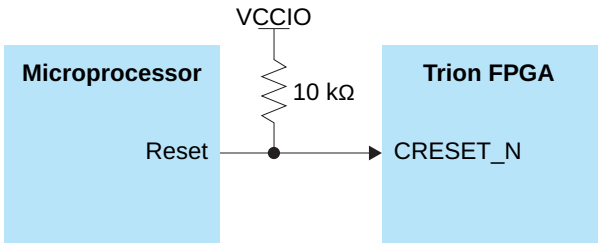


Assuming that the VCCIO1A is the last power supply to be stable in the system, the supervisor IC must hold the CRESET_N pin low for a duration of t_{RP} (reset timeout period) after the VCCIO1A reaches the stable threshold.

Ensure that the t_{RP} of the selected supervisor IC is more than the required t_{CRESET_N}. Refer to the supervisor IC vendor for the recommended operating circuitry.

Note: The user trigger (push-button, FTDI cable or module) must be connected to the MR pin of the supervisor IC.

Microprocessor or Microcontroller Circuitry Example



The microprocessor or microcontroller must hold the CRESET_N pin low more than the required t_{CRESET_N} duration.

Recommended Power Down Sequence

There are no power down sequence requirements.

Recommended Decoupling Capacitors

When designing your board, Efinix recommends that you place all of the decoupling capacitors as close to each power pin as possible.

- The minimum number of decoupling capacitors is at least one 0.0 1uF and one 0.1 uF.
- If you have room on the board, use two 10 uF, three 1 uF, three 0.1 uF, two 0.01 uF, and two 1 nF.

Recommended Energy Storage Capacitor

You should place at least one 47 uF capacitor at the output of each power regulator as energy storage.

Recommended Filtering Circuit

- π filter (C-L-C) or τ filter (L-C) of an inductor or a magnetic bead is required for every power outlet.
- The nominal current should be at least 30% higher than the current of a particular power trail.
- VCCA, VCC12A_MIPI_TX, VCC12A_MIPI_RX, VCC25A_MIPI must have separate filtering circuits.
- Efinix recommends that the VCC pins have separate filtering circuits.

Unused Resources and Features

For unused resources and features, follow these connection requirements:

Unused Resource/Feature	Pin	Note
GPIO Bank	VCCIOxx	Connect to either 1.8 V, 2.5 V, or 3.3 V.
PLL	VCCA_PLL	Connect to VCC.
MIPI	VCC12A_MIPI_TX	Connect to VCC (1.2 V).
	VCC12A_MIPI_RX	Connect to VCC (1.2 V).
	VCC25A_MIPI	Connect to VCC (1.2 V).

Configuration Pin Checklist

Check	Pin Name	Package Pins	Description
☐	All	All	If using internal reconfiguration, the system follows the recommended guidelines. See guideline.
☐	All	All	The system follows the guidelines for the SPI flash capacity. See guideline.
☐	CBSEL[1:0]	D1 D2	The system follows the guidelines for CBSEL. See guideline.
☐	CBUS[2:0]	G13 J11	Connect according to the configuration mode. See SPI Active Parallel (x4) guideline.

☐	CCK	K1	Connect according to the configuration mode. See SPI Active Parallel (x4) guideline.
☐	CDI[n:0]	C1 E1 E13 F1 F2 F3 G11 G2 J1 J2	Connect according to the configuration mode. See SPI Active Parallel (x4) guideline.
☐	CDONE	L2	The system does not hold CDONE low (if held low, the FPGA does not enter user mode). See SPI Active Parallel (x4) guideline.
☐	CRESET_N	K3	The system pulses CRESET_N low for a minimum pulse width of 320 ns (t_{CRESET_N}) during power up or reconfiguration. See SPI Active Parallel (x4) guideline.
☐	CSI		Connect according to the configuration mode. See SPI Active Parallel (x4) guideline.
☐	NSTATUS	C2	(Optional) Connect NSTATUS to an LED to indicate configuration completes without errors. See guideline.
☐	SS_N	L1	SPI slave select (active low). Connect to weak pull-up or pull-down resistors depending on the configuration mode. See SPI Active Parallel (x4) guideline.
☐	TCK	H1	Pull up to VCCIO with a 10 KOhm resistor. See guideline.
☐	TDI	J3	Pull up to VCCIO with a 10 KOhm resistor. See guideline.
☐	TDO	G1	Pull up to VCCIO with a 10 KOhm resistor. See guideline.
☐	TEST_N	H12	Pull up to VCCIO with a 10 KOhm resistor. See SPI Active Parallel (x4) guideline.
☐	TMS	H2	Pull up to VCCIO with a 10 KOhm resistor. See guideline.

Configuration Pin General Guidelines

Internal Reconfiguration

CBUS2, CBUS1, CBUS0, SS_N, and TEST_N are dual-purpose configuration pins, which can be used for internal reconfiguration. When internal reconfiguration is triggered, all GPIOs that are configured as outputs are driven high or low depending on the design. The rising time and falling time of the external network must fall within 800 ns to ensure that the configuration pins are stable and the reconfiguration is successful.

For more information about this feature, refer to AN 010: Using the Internal Reconfiguration Feature to Remotely Update Trion FPGAs (https://www.efinixinc.com/support/docsdl.php?s=ef&pn=AN010)

SPI Flash Capacity

For SPI active configuration (single image), you should use a SPI flash device that (at minimum) has the capacity to store the following maximum bitstream size: 5,261,920 bits.

Multi-Image Select Pins

CBSEL[1:0] are optional multi-image selection input pins that are used with multi-image configuration mode.
If you **are** using multi-image configuration, connect CBSEL for the image you want to use.

- Set CBSEL[1:0] to 00 for image 1
- Set CBSEL[1:0] to 01 for image 2
- Set CBSEL[1:0] to 10 for image 3
- Set CBSEL[1:0] to 11 for image 4

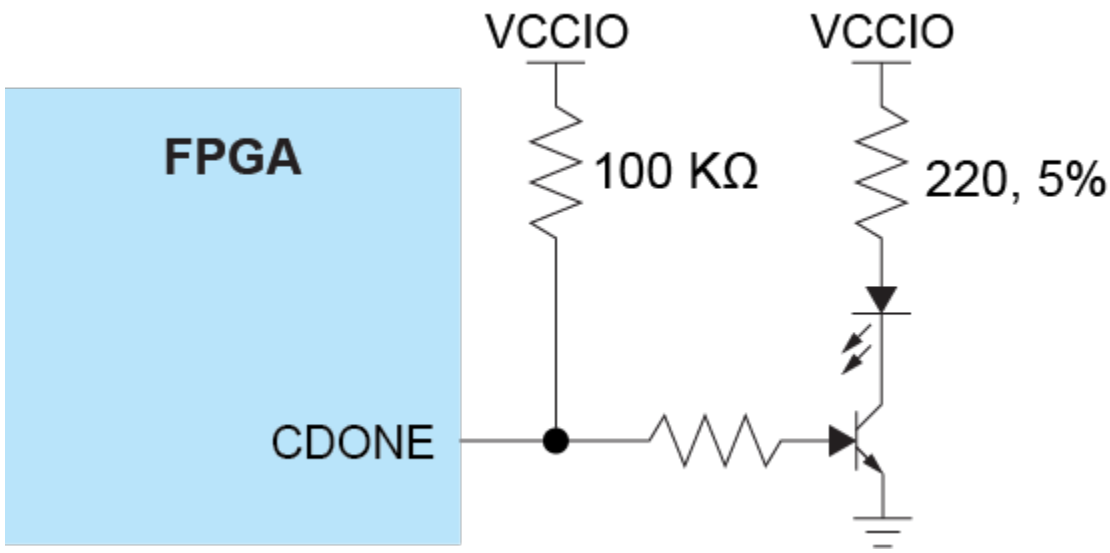
The CBSEL[1:0] pins do not require any weak pull-up or pull-down resistors if you are **not** using multi-image configuration.

CDONE

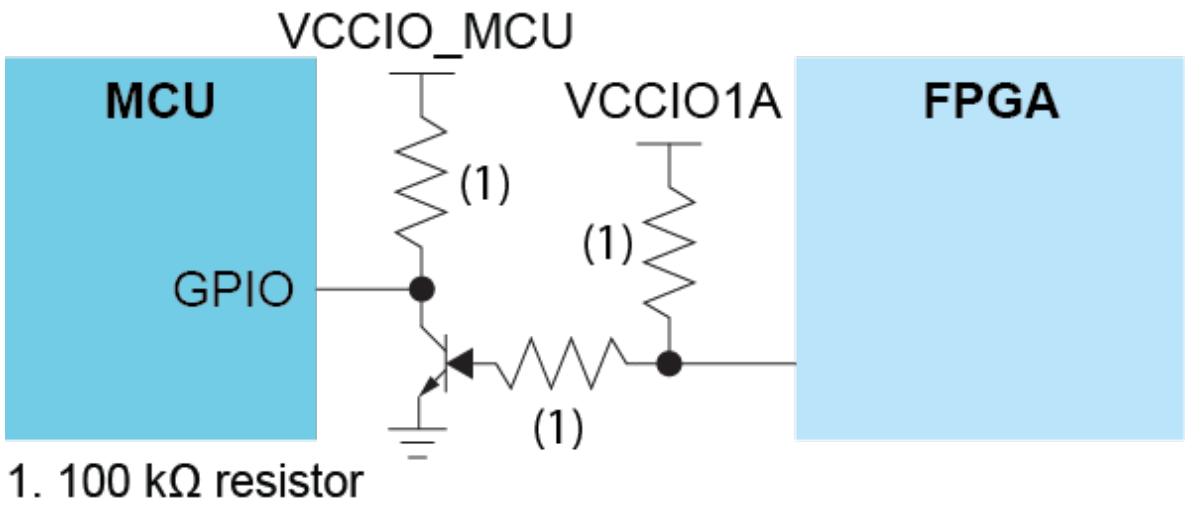
CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold

CDONE low, the device will not enter user mode.

(Optional) Connect CDONE to an LED to indicate when configuration is complete.

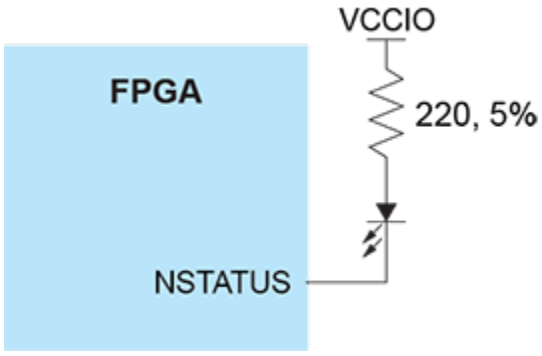


(Optional) Monitor CDONE with a microcontroller or microprocessor.



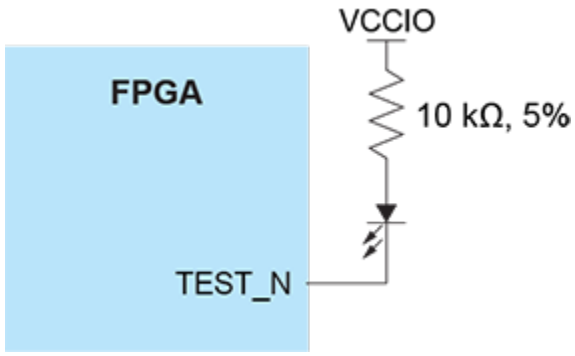
NSTATUS

(Optional) Connect NSTATUS to an LED to indicate configuration completes without errors:



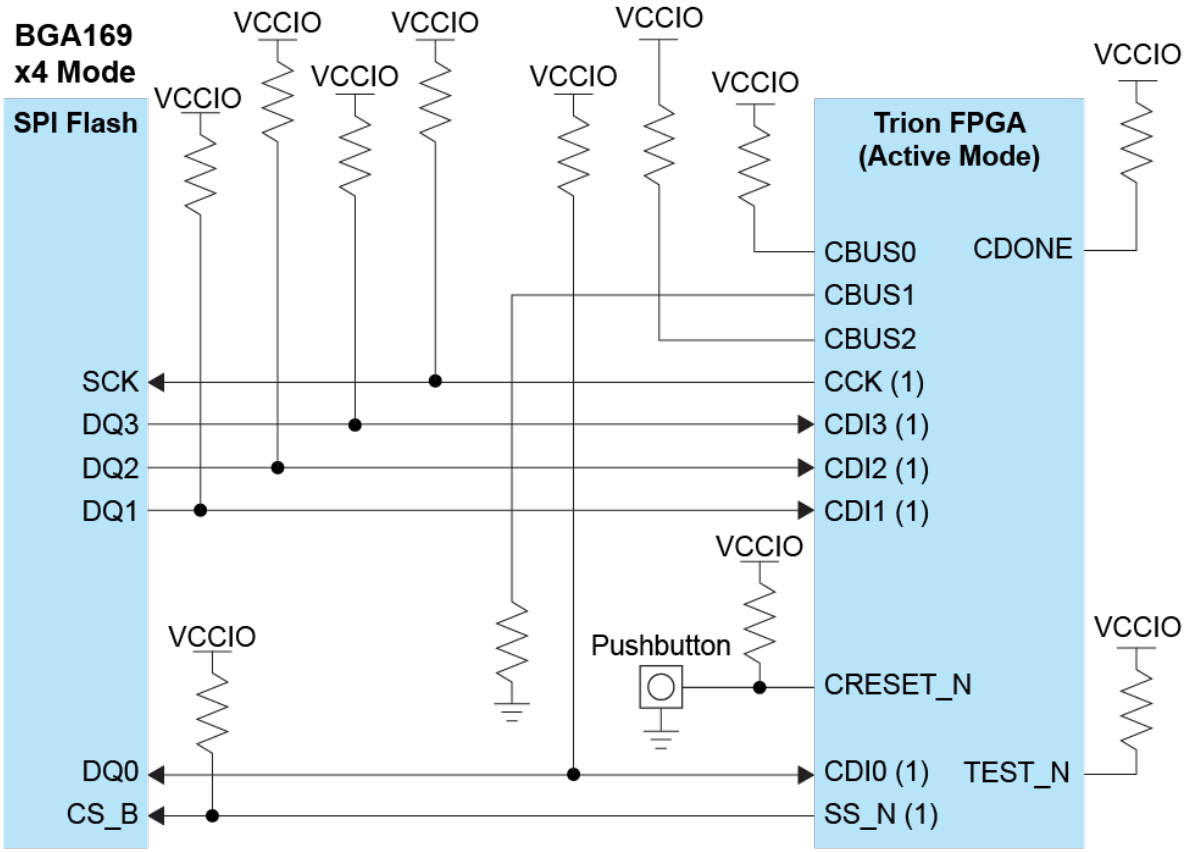
TEST_N Guidelines

During configuration, rely on the external weak pull-up or drive this pin high.



SPI Active Parallel (x4) Configuration Pin Circuitry

The BGA169 package does not have the CSI or CBUS2 signals bonded out. Therefore, you cannot enable or disable the FPGA from another host such as a microprocessor. Additionally, you cannot cascade configuration.



Note:
1. Pull-up connection is optional when external load pull-up is not required.

Efinix recommends that you use 10 kΩ for all unspecified pull-up and pull-down resistors in configuration circuitries. However, because of different board setups and environment noises, the configuration may fail when using 10 kΩ resistors. You can decrease the resistor values to improve signal integrity. Typically, you can also use 1 kΩ resistors.

Alternatively, you can calculate your own pull-up or pull-down resistance, R_{USER}, shown in the following sections.

Notice: The internal weak pull-up resistance, internal weak pull-down resistance, and Schmitt Trigger thresholds values used in the following formulas are included in the FPGA data sheets in the Support Center (https://www.efinixinc.com/support/docs.php).

User-Defined Pull-Up Resistor Values

$R_{USER} = (R_{CPU} * R_{IPU}) / (R_{IPU} - R_{CPU})$

where:

- R_{USER} = User-defined pull-up resistance
- R_{CPU} = Combined pull-up resistance
- R_{IPU} = Internal weak pull-up resistance

The combined pull-up resistance, R_{CPU}, can be derived using the following formula:

$VT+ \leq VCCIO * (R_{CPU} / (R_{CPU} + R_{IPD}))$

where:

- VT+ = Schmitt Trigger low-to-high threshold
- VCCIO = I/O bank power supply
- R_{IPD} = Internal weak pull-down resistance

User-Defined Pull-Down Resistor Values

$R_{USER} = (R_{CPD} * R_{IPD}) / (R_{IPD} - R_{CPD})$

where:

- R_{USER} = User-defined pull-down resistance
- R_{CPD} = Combined pull-down resistance
- R_{IPD} = Internal weak pull-down resistance

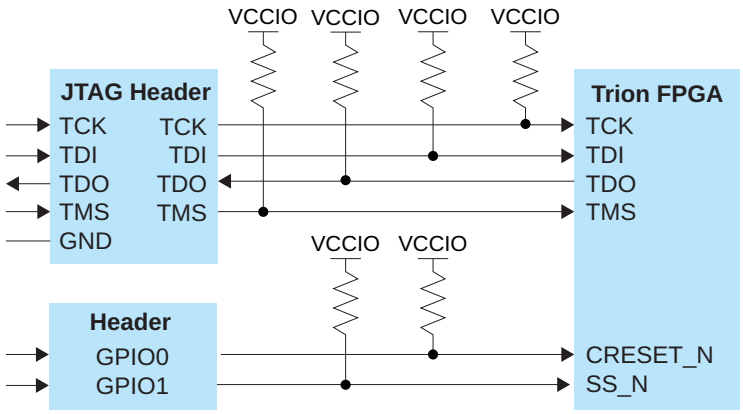
The combined pull-down resistance, R_{CPD}, can be derived using the following formula:

$VT- \geq VCCIO * (R_{CPD} / (R_{CPU} + R_{IPU}))$

where:

- VT- = Schmitt Trigger high-to-low threshold
- VCCIO = I/O bank power supply
- R_{IPU} = Internal weak pull-up resistance

JTAG Configuration Pin Circuitry



GPIO Pin Checklist

Check	Pin Name	Package Pins	Description
☐	CLKn	G12 G3 H11 H3	My design uses these global clock network inputs as dedicated clock input pins for input clocks.
☐	CTRLn	E1 F13 F2	My system uses these global control network input pins for high fanout and global reset.
☐	TXNn, TXPn, RXNn, RXPn	J13 K10 K11 K13 K4 K5 K6 K7 K8 K9 L10 L11 L3 L4 L5 L6 L7 L8 L9 M1 M10 M11 M12 M2 M3 M5 M6 M7 M8 M9 N10 N11 N12 N2 N3 N5 N6 N7 N8 N9	When used as GPIO, these LVDS pins follow the guidelines. See guidelines.

GPIO Pin General Guidelines

Unused GPIO Banks or Pins

If you are not using any of the GPIO in an I/O bank, connect the bank's VCCIOxx pins to 1.8 V, 2.5 V, or 3.3 V.

The VCCIOxx pins for unused GPIO bancks do not require decoupling capacitors.

If you are not using a GPIO pin, you can leave it floating.

PLL Pin Checklist

Check	Pin Name	Package Pins	Description
☐	All	All	The PLL reference clock must be between 10 and 200 MHz.
☐	PLLINn	B1 D13 E3 F12 J12	Assign the PLL reference clock port based on the PLL that you are using. See guideline.

PLL Pin General Guidelines

Unused PLLs

If you are not using a PLL, connect it's VCCA_PLL pin to VCC.

The VCCA_PLL pins for unused PLLs do not require decoupling capacitors.

PLL Reference Clocks

The PLL reference clock port can be driven by single ended I/O pins or a differential pair clock. For applications with a continuous clock, e.g., RGMII, Efinix recommends that you connect the clock pin as a PLL reference clock to maintain the source synchronous property.

PLL Reference Clock Resource Assignments

PLL	REFCLK1	REFCLK2
PLL_BR0	Differential: GPIOB_CLKP0, GPIOB_CLKN0 Single Ended: GPIOB_CLKP0	GPIOR_157_PLLIN
PLL_TR0	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
PLL_TR1	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
PLL_TL0	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1
PLL_TL1	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1

LVDS Pin Checklist

Check	Pin Name	Package Pins	Description
☐	All	All	The system follows the guidelines for differential traces. See guideline.
☐	All	All	The system follows the guidelines for impedance matching. See guideline.
☐	All	All	The system follows the guidelines for avoiding crosstalk. See guideline.
☐	All	All	The system follows the guidelines for LVDS pins used as GPIO. See guideline.
☐	REF_RES	N4	REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kOhm resistor with a tolerance of +/-1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating. See guideline.
☐	RXNn RXPn	J13 K10 K11 K13 K7 K8 K9 L10 L11 L7 L8 L9 M10 M11 M12 M7 M8 M9 N10 N11 N12 N7 N8 N9	LVDS receiver. Trion FPGAs have a 100 Ohm on-die termination resistor for the LVDS receiver. Therefore, do not use external termination. If the incoming LVDS signals are AC-coupled, my system should add external DC-biased circuit.See guideline.

LVDS Pin General Guidelines

Differential Traces

Follow these design guidelines for LVDS traces:

- The P and N channel in an LVDS pair should be as close to each other as possible, and the distance between the pair's P and N channel should be constant.
- The LVDS TX and RX should be as close as possible to any connectors.
- To minimize skew, the electrical length of traces:
    - between the differential LVDS P and N channels should be +/- 0.15 mm
    - between one LVDS pair to another LVDS pair should be +/- 1.50 mm
- Minimize the number of vias on the signal path.
- If there is any parasitic loading (such as capacitance), it should be in equal amounts to each line.
- Traces should be bend >135 degrees to avoid signal loss and jitter.

Impedance Matching

The LVDS trace impedance should be:

- LVDS differential: 100 ohms +/- 10%
- LVDS single-ended: 50 ohms +/- 10%

Avoiding Crosstalk between LVDS and Single-Ended Signals

Differential LVDS signals must be isolated from single-ended signals; the single-ended signals may cause interference on the differential signals. You can implement the isolation by:

- Designing the trace for differential LVDS pairs to be at least 12 mm from the trace for single-ended I/O, if both are on the same PCB layer.
- Isolating the differential LVDS pair signals from the single-ended signals using power or ground planes.
- Minimize stub lengths because they increase reflection noise.

LVDS Used as GPIO

You can use the LVDS TX and LVDS RX channels as 3.3 V single-ended GPIO pins. In this mode, these pins:

- Support a weak pull-up
- Do not support DDIO, Schmitt trigger, variable drive strength, slew rate, or pull down

There is a maximum of 16 LVDS GPIO in an I/O bank.

When using LVDS as GPIO, Efinix recommends that you leave at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS pins. This rule applies for pins on each side of the device (top, bottom, left, right). This separation reduces noise. The Efinity software issues a warning if you do not leave this separation.

Separate the I/O placement evenly in a single bank.

Termination

On board terminations is not required.

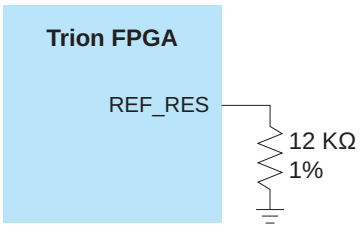
Unused LVDS Pins

Leave unused LVDS pins floating.

Guideline for REF_RES Pin

Connect a 12 kOhm resistor with a tolerance of +/-1% to the REF_RES pin with respect to ground.

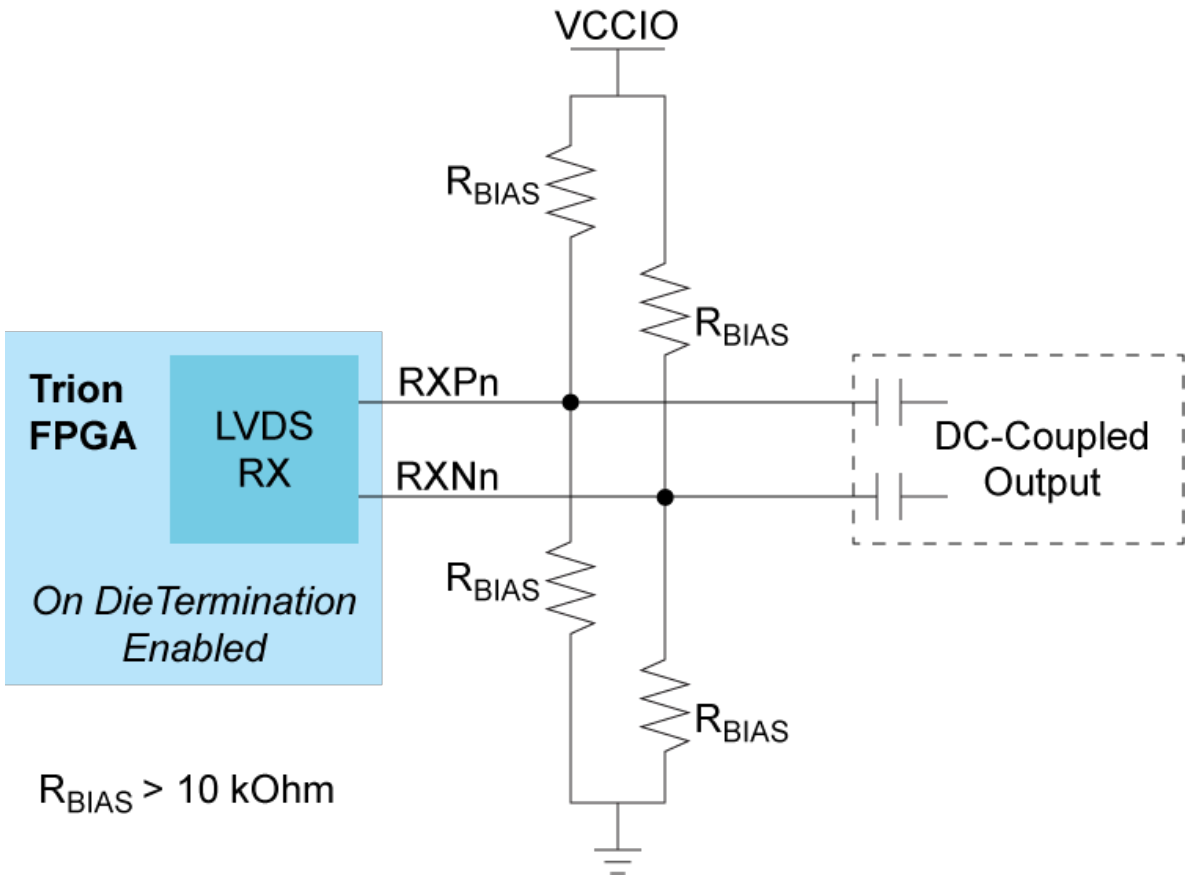
If none of the pins in a bank are used for LVDS, leave this pin floating.



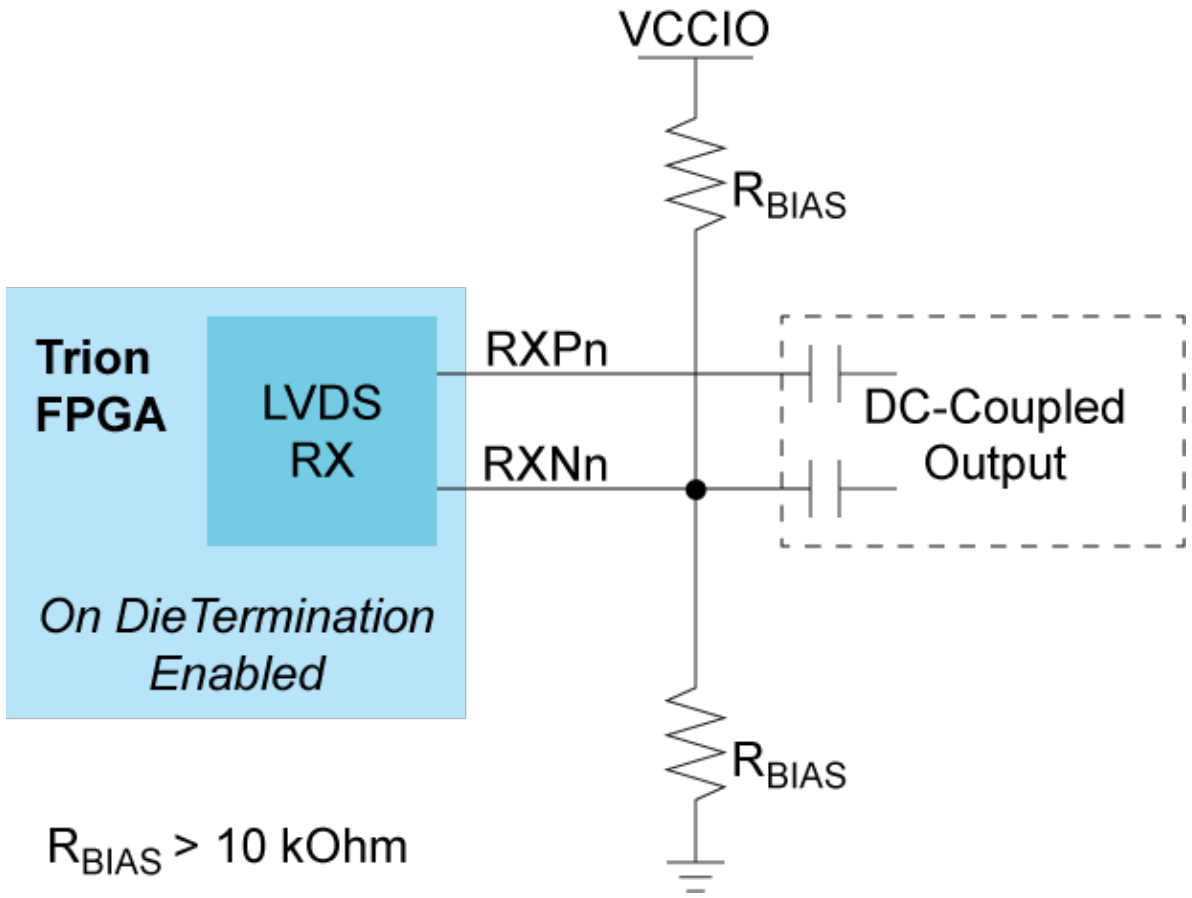
External DC-biased Circuit for Incoming AC-coupled LVDS RX Signals

Efinix recommends either one of these external DC-biased circuits:

DC components on Both Signals (P and N)
With DC bias on both P and N, the bias voltages can be slightly different. This may create an offset. However, since the resistor values are >10 kOhms, the difference is very small. This method requires more parts, and board space especially with multi-bits LVDS bus.



DC components on One Signal (P or N)
With DC bias on only one side, the capacitive loads on P and N are slightly different. With one side T-off to bias and other side does not, the P and N can become unmatched. This method requires less parts, and board space.


VCCIO
R_{BIAS}
Trion
FPGA
LVDS
RX
RXPn
RXNn
DC-Coupled
Output
On DieTermination
Enabled
R_{BIAS}
R_{BIAS} > 10 kOhm

MIPI Pin Checklist

Check	Pin Name	Package Pins	Description
☐	All	All	Refer to Trion MIPI Interface PCB Design User Guide (https://www.efinixinc.com/support/docsdl.php?s=ef&pn=PCB-MIPI) for detailed guidelines.
☐	MIPIn_TXDPm, MIPIn_TXDNm	A10 A2 A3 A4 A8 A9 B10 B2 B3 B4 B8 B9 C4 C5 C8 C9 D4 D5 D8 D9	The system follows the guidelines for MIPI traces. See guidelines.
☐	MREFCLK	F11	If you are using MIPI RX, you must use MREFCLK as your reference clock input. See guideline.

MIPI Pin General Guidelines

Unused MIPI Hard Blocks

If you are not using a MIPI hard block, connect it's VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI pins to VCC.

The VCC12A_MIPI_TX, VCC12A_MIPI_RX, and VCC25A_MIPI pins for unused MIPI hard blocks do not require decoupling capacitors.

Leave all other MIPI pins floating.

MIPI Pin Assignment

To simplify your PCB layout, all of the MIPI interface clock and data lanes are interchangeable. In the Efinity Interface Designer, click the MIPI block and then go to the **Lane Mapping** tab to change the lane assignments.

Guidelines for MIPI Traces

To reduce signal reflections and impedance changes, route high-speed signals using:

- A minimum number of vias and corners
- The same PCB layer for all the lanes in the same channel

The MIPI trace impedance should be:
MIPI D-PHY RX or TX differential 100 Ohm +/- 10%
MIPI D-PHY RX or TX single-ended 50 Ohm +/- 10%

Match routing length for 1.5 Gbps:
MIPI D-PHY RX or TX P/N pair +/- 0.10 mm
MIPI D-PHY RX or TX CLK/DATA +/- 1.00 mm

Match routing length for 1.0 Gbps:
MIPI D-PHY RX or TX P/N pair +/- 0.15 mm
MIPI D-PHY RX or TX CLK/DATA +/- 1.5 mm

MIPI MREFCLK

MREFCLK supports the following frequencies:
6, 12, 19.2, 25, 26, 27, 38.4, and 52 MHz.
