

Preliminary



GW5A series of FPGA Products

Data Sheet

DS1103-1.0E, 12/08/2023

Preliminary

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Preliminary

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1 General Description

GOWINSEMI's GW5A series of FPGA products are the 5th-generation of the Arora family with rich internal resources, including high-performance DSP resources with a new architecture and support for AI computing, high-speed LVDS interfaces, and rich BSRAM resources. At the same time, the GW5A series of FPGA provide independently-developed DDR3 and a variety of packages. They are suitable for applications such as low power, high performance and compatibility designs.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
 - 22nm SRAM process
 - Core Power (LV version): 0.9V/ 1.0V
 - Core voltage (EV version): 1.2V^[1]
- **Note!**
 - [1] The EV version (supported by GW5A-25) has a built-in LDO and supports 1.2V V_{CC}.
- Supports dynamic on/off of clock
- Abundant basic logic cells
 - GW5A-25 provides 23K LUT4s
 - GW5A-138 provides up to 138K LUT4s
 - Supports shadow SRAMs
- Block SRAMs with multiple modes
 - Supports Dual Port, Single Port, Semi Dual Port, and ROM
 - Supports bytes write enable
 - Supports ECC detection and error correction
- Supports MIPI D-PHY RX hard core
 - Supports MIPI DSI and MIPI CSI-2 RX
 - Up to 2.5 Gbps per MIPI lane
 - Supports up to eight data lanes and two clock lanes, with the max. transmission speed up to 20Gbps
- Supports MIPI D-PHY RX/TX

- hard core (GW5A-25)
 - Supports MIPI DSI and MIPI CSI-2 RX/TX
 - Up to 2.5 Gbps per MIPI lane(RX/TX)
 - Supports up to 4 data lanes and 1 clock lane
- GPIO supports MIPI D-PHY RX (GW5A-138)
 - GPIO can be configured as MIPI DSI and MIPI CSI-2 RX interfaces
 - Up to 1.5 Gbps per MIPI lane
- GPIO supports D-PHY RX/TX (GW5A-25)
 - GPIO can be configured as MIPI DSI and MIPI CSI-2 RX/TX interfaces
 - Up to 1.2 Gbps per MIPI lane
- High performance DSP blocks with a new architecture
 - High performance digital signal processing
 - Supports 27 x 18, 12 x 12, 27 x 36 multiplier and 48-bit accumulator
 - Supports cascading of multipliers
 - Supports Pipeline mode and Bypass mode
 - Pre-addition operation for filter function
 - Supports barrel shifter
- A new and flexible X-channel oversampling ADC with high accuracy, no external voltage source required
 - 60dB SNR
 - 1kHz Signal Bandwidth
- Supports multiple SDRAM interfaces, up to DDR3 1333 Mbps (GW5A-138) or 1066 Mbps (GW5A-25)
- Multiple I/O standards
 - Hysteresis option for input signals
 - Supports drive strengths of 2mA^[1], 4mA, 6mA^[1], 8mA, 16mA, 24mA^[2], etc.

Note!

[1] 2mA and 6mA are only supported by GW5A-25.

[2] 24mA is only supported by GW5A-138.

 - Individual Bus Keeper, Pull-up, Pull-down, and Open Drain options
 - Hot Socket
- 16 global clocks, 6/12 high-performance PLLs, 16/24 high speed clocks
- Configuration & Programming
 - JTAG configuration
 - Four GowinConfig configuration modes: SSPI, MSPI, CPU, SERIAL
 - Supports programming the SPI Flash directly in JTAG and SSPI modes; For other modes, you can program the SPI Flash using IP
 - Supports background upgrade
 - Supports bitstream file encryption and security bit settings
 - Supports configuration memory soft error recovery (CMSER)
 - Supports mDRP
 - Supports OTP. Offers a unique 64-bit DNA identifier

for each device

1.2 Product Resources

Table 1-1 Product Resources

| Device | GW5A-25 | GW5A-45 | GW5A-138 |
|---|---|---|---|
| LUT4 | 23040 | 44928 | 138240 |
| Flip-Flop (REG) | 23040 | 44928 | 138240 |
| Distributed Static Random Access Memory SSRAM(Kb) | 180 | 351 | 1080 |
| Block Static Random Access Memory BSRAM(Kb) | 1008 | 2106 | 6120 |
| Number of BSRAMs | 56 | 117 | 340 |
| DSP (27-bit x 18-bit) | 28 | 81 | 298 |
| Maximum phase locked loop ^[1] (PLLs) | 6 | 4 | 12 |
| Global Clocks | 16 | 16 | 16 |
| High-speed Clocks | 16 | 12 | 24 |
| LVDS Gbps | 1.25 | 1.25 | 1.25 |
| DDR3 Mbps | 1066 | 1333 | 1333 |
| MIPI DPHY hard core | 2.5Gbps (RX/TX), 4 data lanes 1 clock lanes | 2.5Gbps (RX/TX), 4 data lanes 1 clock lanes | 2.5Gbps (RX) 8 data lanes 2 clock lanes |
| ADC | 1 | 2 | 2 |
| Number of GPIO banks | 8 ^[2] | 6 | 6 |
| Maximum number of I/Os | 239 | 330 | 312 |
| Core voltage | 0.9V/1.0V/1.2V ^[3] | 0.9V/1.0V | 0.9V/1.0V |

Note!

- [1] Different packages support different numbers of PLLs.
- [2] In addition to GPIO Banks, there is one JTAG Bank with four I/Os and one Config Bank with one I/O.
- [3] The EV version has a built-in LDO and supports 1.2V V_{CC}.

Table 1-2 GW5A-25 Package Information

| Package ^[1] | Pitch (mm) | Size (mm) | GW5A-25 | |
|------------------------|------------|-----------|----------------------|--|
| | | | I/O (True LVDS Pair) | MIPI D-PHY Hardcore |
| MG121N | 0.5 | 6 x 6 | 82 (38) | RX/TX (Configurable) 4 data lanes 1 clock lanes |
| UG324S | 0.8 | 15 x 15 | 239 (116) | – |
| UG256C | 0.8 | 14 x 14 | 191 (90) | – |
| PG256C | 1.0 | 17 x 17 | 191 (90) | – |
| PG256 | 1.0 | 17 x 17 | 184 (88) | RX/TX (Configurable) 4 data lanes 1 clock lanes |
| PG256S | 1.0 | 17 x 17 | 194 (93) | – |
| UG324 | 0.8 | 15 x 15 | 222 (104) | RX/TX (Configurable) 4 data lanes 1 clock lanes |
| MG196S | 0.5 | 8 x 8 | 114 (53) | – |
| UG225S | 0.8 | 13 x 13 | 168 (80) | – |
| LQ100 | 0.5 | 14 x 14 | 80 (36) | – |
| LQ144 | 0.5 | 20 x 20 | 109 (50) | – |

Note!

[1] The package types in this data sheet are written with abbreviations. See [4.1 Part Name](#) for further information.

Table 1-3 GW5A-138 Package Information

| Package ^[1] | Pitch (mm) | Size (mm) | GW5A-138 | |
|------------------------|------------|-----------|----------------------|---------------------|
| | | | I/O (True LVDS Pair) | MIPI D-PHY Hardcore |
| UG324A | 0.8 | 15 x 15 | 222 (106) | – |

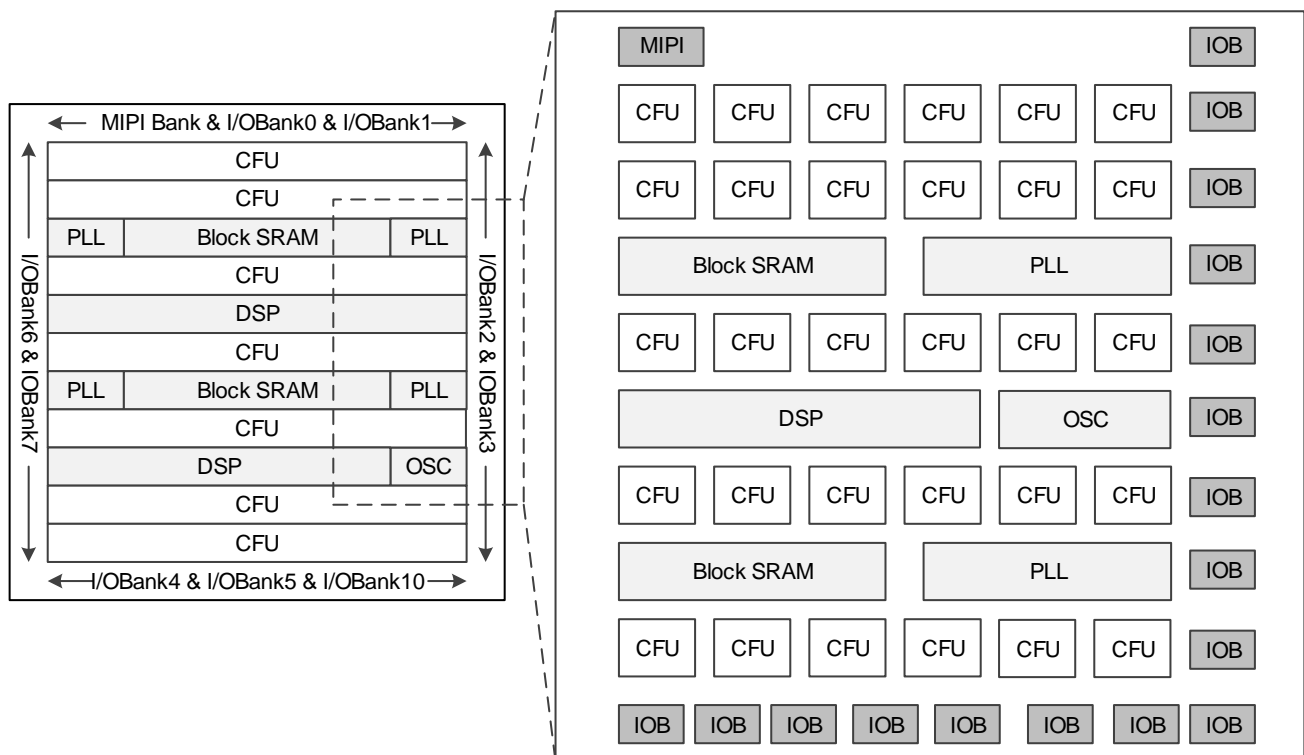
Note!

[1] The package types in this data sheet are written with abbreviations. See [4.1 Part Name](#) for further information.

2 Architecture

2.1 Architecture

Figure 2-1 Architecture Diagram (GW5A-138)



See Figure 2-1 for an overview of the architecture of the GW5A-138 device. Please refer to Table 1-1 for more information on its internal resources. The core of the device is an array of Configurable Logic Units (CFU) surrounded by IO blocks. Besides, BSRAMs, DSP blocks, MIPI D-PHY, ADC, PLLs, and on chip oscillators are provided.

Configurable Function Unit (CFU) is the base cell for the array of the GW5A series of FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. For more detailed information, see [2.2 Configurable Function Units](#).

The I/O resources in the GW5A series of FPGA products are arranged around the periphery of the devices in groups referred to as banks. I/O resources support multiple I/O standards, and support regular mode, SRD mode, generic DDR mode, and DDR_MEM mode. For more detailed information, see [2.3 Input/Output Blocks](#).

The BSRAM is embedded as a row in GW5A series of FPGA products. Each BSRAM has a maximum capacity of 36Kbits and consists of two 18Kbits BSRAMs. It supports multiple configuration modes and operation modes. For more detailed information, see [2.4 Block SRAM \(BSRAM\)](#).

GW5A series of FPGA products are embedded with a brand-new DSP, which can meet the high-performance digital signal processing requirements. For details, refer to [2.5 DSP Blocks](#).

GW5A series of FPGA products provide a MIPI D-PHY hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. For details, see [2.6 MIPI D-PHY](#).

GW5A series of FPGA products integrate a new and flexible oversampling ADC. For details, see [2.7 ADC](#).

GW5A series of FPGA products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. This series of FPGAs also have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 2.5 MHz to 105MHz, providing clocking resources for the MSPI mode. The on-chip clock oscillator also provides programmable user clocks. For more information, see [2.11 On Chip Oscillator](#).

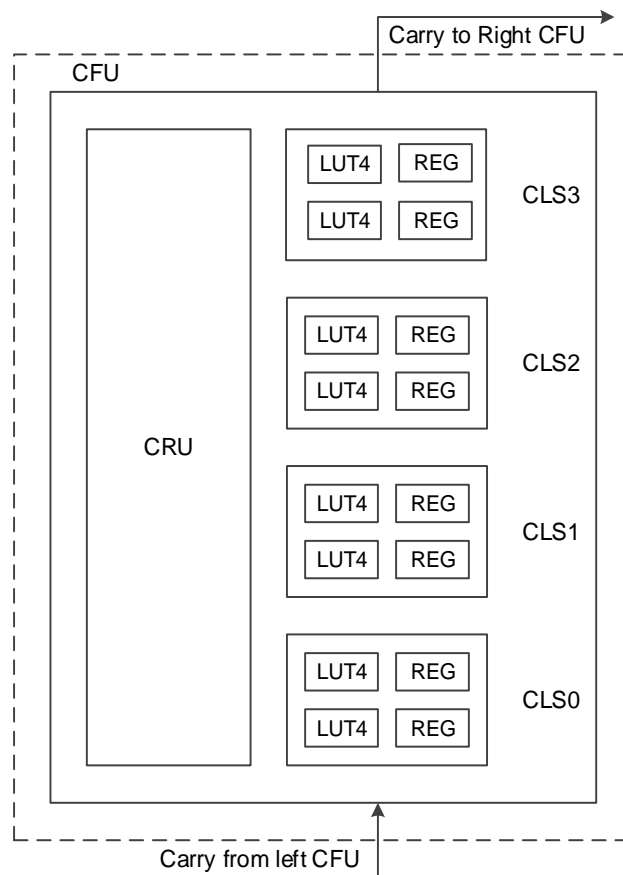
FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW5A series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more details, see [2.9 Global Set/Reset \(GSR\)](#), and [2.10 Programming & Configuration](#).

2.2 Configurable Function Units

Configurable Function Units (CFUs) are the basic cells for the array of GOWINSEMI FPGA Products. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs). Each CLS includes two 4 input look-up-tables (LUTs) and two registers (REGs), as shown in Figure 2-2 .

CLSs in the CFUs can be configured as basic look-up tables, arithmetic logic units, static random access memories, and read only memories according to application scenarios.

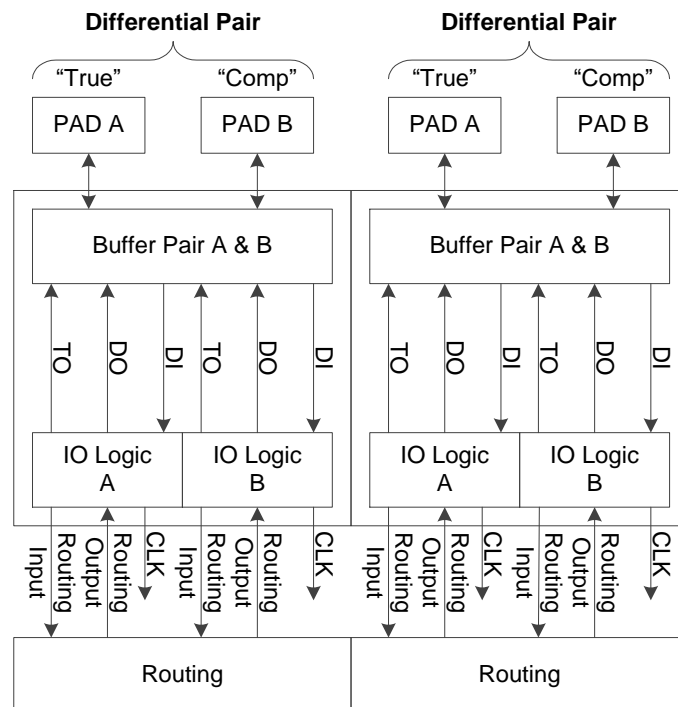
For more details, please see [UG303, Arora V Configurable Function Unit \(CFU\) User Guide](#).

Figure 2-2 CFU Structure View

2.3 Input/Output Blocks

The IOB in the GW5A series of FPGA products includes IO buffer, IO logic, and its routing unit. As shown in Figure 2-3, each IOB connects to two Pins (Marked as A and B). They can be used as a differential pair or as a single-ended input/output.

Figure 2-3 IOB Structure View

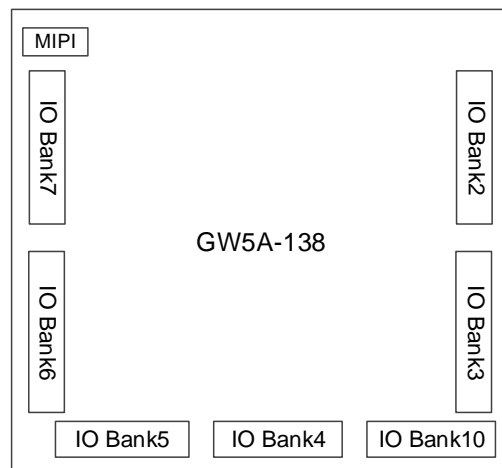


IOB Features:

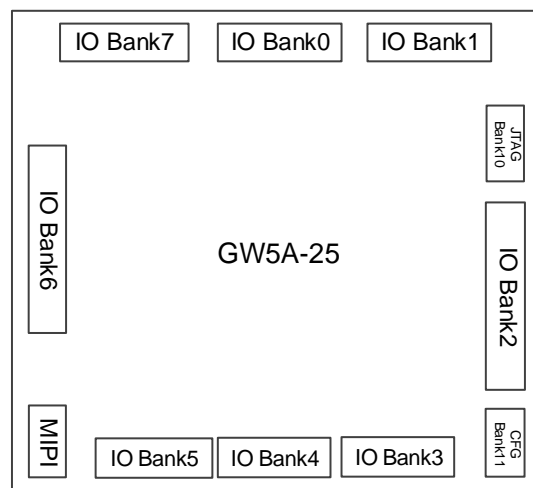
- V_{CCIO} supplied with each bank
- All banks support True differential input
- Supports multiple levels: LVCMOS, PCI, LVTTTL, SSTL, HSTL, LVDS, Mini_LVDS, RSDS, PPDS, BLVDS
- Input hysteresis option
- Output drive strength option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports SDR mode, DDR mode, etc.

2.3.1 I/O Buffer

GW5A-138 has six GPIO Banks (Bank2~7) and a Bank for configuration (Bank 10), as shown in Figure 2-4. Bank 10 can also be used as an I/O Bank.

Figure 2-4 Bank Distribution View of GW5A-138

GW5A-25 has eight GPIO Banks. Bank10 is a JTAG Bank with four IOs, Bank11 is a Config Bank with one IO, as shown in Figure 2-5.

Figure 2-5 Bank Distribution View of GW5A-25

Each Bank has its independent I/O power supply V_{CCIO} .

GW5A-25's V_{CCIO} can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, or 1.2V.

GW5A-138's V_{CCIO} can be set as 3.3V, 2.5V, 1.8V, 1.5V, 1.35V, 1.2V, or 1V.

Note!

- GW5A-138: To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.675V, 0.75V, 0.9V, and (33%,42%,50%,58%) V_{CCIO}) or the external reference voltage using any IO from the bank.
- GW5A-25: To support SSTL, HSTL, etc., each bank also provides one independent voltage source (VREF) as the reference voltage. You can choose from the internal reference voltage of the bank (0.6V, 0.75V, 0.9V, 1.25V, 1.5V, and (36%,50%,64%) V_{CCIO}) or the external reference voltage using any IO from the bank.

The auxiliary voltage V_{CCX} of GW5A-25 devices supports 2.5V~3.3V.

The auxiliary voltage V_{CCX} of GW5A-138 devices supports 1.8V.

Different banks in the GW5A series of FPGA Products support different on-chip resistor settings, including single-ended resistor and differential resistor. Single-ended resistor is set for SSTL/HSTL I/O. Differential resistor is set for LVDS/PPDS/ RSDS input. For more details, refer to [UG304, Arora V Programmable IO \(GPIO\) User Guide](#).

Note!

Before and during configuration, all GPIOs of the device have weak pull-up by default. The default I/O state is None after configuration is complete and it can be configured via the Gowin software. The status of configuration-related I/Os differs depending on the configuration mode.

For the V_{CCIO} requirements of different I/O standards, see Table 2-1, Table 2-2, Table 2-3, and Table 2-4.

Table 2-1 Output I/O Standards and Configuration Options supported by GW5A-138

| I/O output standard | Single-ended / Differential | Bank V_{CCIO} (V) | Drive Strength (mA) | Typical Applications |
|---------------------------|-----------------------------|---------------------|---------------------|---|
| LVDS25 | Differential(TLVDS) | 2.5/3.3 | 3.5/2.5/4.5/6 | High-speed point-to-point data transmission |
| BLVDS25 | | 2.5/3.3 | 3.5/2.5/4.5/6 | Multi-point high-speed data transmission |
| RSDS | | 2.5/3.3 | 3.5/2.5/4.5/6 | High-speed point-to-point data transmission |
| MINILVDS | | 2.5/3.3 | 3.5/2.5/4.5/6 | LCD timing driver interface and column driver interface |
| PPLVDS | | 2.5/3.3 | 3.5/2.5/4.5/6 | LCD row/column driver |
| LVDS25E | Differential | 2.5 | 8/4/12/16/24 | High-speed point-to-point data transmission |
| BLVDS25E | | 2.5 | 8/4/12/16/24 | Multi-point high-speed data transmission |
| MLVDS25E | | 2.5 | 8/4/12/16/24 | LCD timing driver interface and column driver interface |
| RSDS25E | | 2.5 | 8/4/12/16/24 | High-speed point-to-point data transmission |
| LVPECL33E | | 3.3 | 8/4/12/16/24 | Universal interface |
| HSUL12D | | 1.2 | 8/4/12 | LPDDR2 |
| HSUL12D_I | | 1.2 | 8/4/12 | LPDDR2 |
| HSTL15D_I | | 1.5 | 8/4/12/16 | Memory interface |
| HSTL15D_II ^[4] | | 1.5 | 8/4/12/16 | Memory interface |

| I/O output standard | Single-ended / Differential | Bank V_{CCIO} (V) | Drive Strength (mA) | Typical Applications |
|---------------------|-----------------------------|---------------------|---------------------|------------------------|
| HSTL18D_I | | 1.8 | 8/4/12/16 | Memory interface |
| HSTL18D_II | | 1.8 | 8/4/12/16 | Memory interface |
| SSTL135D | | 1.35 | 8/4/12 | Memory interface |
| SSTL15D | | 1.5 | 8/4/12/16 | Memory interface |
| SSTL18D_I | | 1.8 | 8/4/12/16/24 | Memory interface |
| SSTL18D_II | | 1.8 | 8/4/12/16/24 | Memory interface |
| LPDDR | | 1.8 | 8/4/12/16/24 | LPDDR and Mobile DDR |
| LVC MOS10D | | 1.0 | 4 | Universal interface |
| LVC MOS12D | | 1.2 | 4/8 | Universal interface |
| LVC MOS15D | | 1.5 | 4/8/12 | Universal interface |
| LVC MOS18D | | 1.8 | 4/8/12/16/24 | Universal interface |
| LVC MOS25D | | 2.5 | 4/8/12/16/24 | Universal interface |
| LVC MOS33D | | 3.3 | 8/4/12/16/24 | Universal interface |
| HSUL12 | Single-ended | 1.2 | 8/4/12 | Memory interface |
| HSTL12_I | | 1.2 | 8/4/12 | Memory interface |
| HSTL15_I | | 1.5 | 8/4/12/16 | Memory interface |
| HSTL15_II | | 1.5 | 8/4/12/16 | Memory interface |
| HSTL18_I | | 1.8 | 8/4/12/16/24 | Memory interface |
| HSTL18_II | | 1.8 | 8/4/12/16/24 | Memory interface |
| SSTL135 | | 1.35 | 8/4/12 | Memory interface |
| SSTL15 | | 1.5 | 8/4/12/16 | Memory interface |
| SSTL18_I | | 1.8 | 8/4/12/16/24 | Memory interface |
| SSTL18_II | | 1.8 | 8/4/12/16/24 | Memory interface |
| LVC MOS10 | | 1.0 | | Universal interface |
| LVC MOS12 | | 1.2 | 4/8 | Universal interface |
| LVC MOS15 | | 1.5 | 4/8/12 | Universal interface |
| LVC MOS18 | | 1.8 | 4/8/12/16/24 | Universal interface |
| LVC MOS25 | | 2.5 | 4/8/12/16/24 | Universal interface |
| LVC MOS33/L VTTL33 | | 3.3 | 8/4/12/16/24 | Universal interface |
| LPDDR | | 1.8 | 8/4/12/16/24 | LPDDR and Mobile DDR |
| PCI33 | | 3.3 | 8/4/12/16/24 | PC and embedded system |

Table 2-2 Input I/O Standards and Configuration Options supported by GW5A-138

| I/O Input Standard | Single-ended / Differential | Bank V_{CCIO} (V) | Hysteresis | Need V_{REF} |
|--------------------|-----------------------------|-------------------------|------------|----------------|
| MIPI | Differential | 1.2 | No | No |
| ADC_in | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |

| I/O Input Standard | Single-ended / Differential | Bank V _{CCIO} (V) | Hysteresis | Need V _{REF} |
|--------------------|-----------------------------|------------------------------------|------------|-----------------------|
| LVDS25 | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| BLVDS25 | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| RSDS | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| MINILVDS | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| PPLVDS | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| HSUL12D | | 1.2/1.0/1.5/1.8/2.5/3.3 | No | No |
| HSTL12D_I | | 1.2/1.0/1.5/1.8/2.5/3.3 | No | No |
| HSTL15D_I | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| HSTL15D_II | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| HSTL18D_I | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| HSTL18D_II | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| SSTL135D | | 1.35/ 1.0/ 1.2/ 1.5/ 1.8/ 2.5/ 3.3 | No | No |
| SSTL15D | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| SSTL18D_I | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| SSTL18D_II | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| LPDDR | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| LVC MOS10D | | 1.0/1.2/1.5/1.8/2.5/3.3 | No | No |
| LVC MOS12D | | 1.2/1.0/1.5/1.8/2.5/3.3 | No | No |
| LVC MOS15D | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| LVC MOS18D | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| HSUL12 | Single-ended | 1.2 | No | Yes |
| HSTL12_I | | 1.2 | No | Yes |
| HSTL15_I | | 1.5 | No | Yes |
| HSTL15_II | | 1.5 | No | Yes |
| HSTL18_I | | 1.8 | No | Yes |
| HSTL18_II | | 1.8 | No | Yes |
| SSTL135 | | 1.35 | No | Yes |
| SSTL15 | | 1.5 | No | Yes |
| SSTL18_I | | 1.8 | No | Yes |
| SSTL18_II | | 1.8 | No | Yes |
| LVC MOS10 | | 1.0 | No | No |
| LVC MOS10UD12 | | 1.2 | No | No |
| LVC MOS10UD15 | | 1.5 | No | No |
| LVC MOS10UD18 | | 1.8 | No | No |
| LVC MOS10UD25 | | 2.5 | No | No |
| LVC MOS10UD33 | | 3.3 | No | No |
| LVC MOS12 | | 1.2 | Yes | No |
| LVC MOS15 | | 1.5 | Yes | No |

| I/O Input Standard | Single-ended / Differential | Bank V _{CCIO} (V) | Hysteresis | Need V _{REF} |
|--------------------|-----------------------------|----------------------------|------------|-----------------------|
| LVC MOS15OD10 | | 1.0 | Yes | No |
| LVC MOS15OD12 | | 1.2 | Yes | No |
| LVC MOS15UD18 | | 1.8 | Yes | No |
| LVC MOS15UD25 | | 2.5 | Yes | No |
| LVC MOS15UD33 | | 3.3 | Yes | No |
| LVC MOS18 | | 1.8 | Yes | No |
| LVC MOS18OD10 | | 1.0 | Yes | No |
| LVC MOS18OD12 | | 1.2 | Yes | No |
| LVC MOS18OD15 | | 1.5 | Yes | No |
| LVC MOS18UD25 | | 2.5 | Yes | No |
| LVC MOS18UD33 | | 3.3 | Yes | No |
| LVC MOS25 | | 2.5 | Yes | No |
| LVC MOS25UD33 | | 3.3 | Yes | No |
| LVC MOS33/LVTT L33 | | 3.3 | Yes | No |
| LVC MOS33OD25 | | 2.5 | Yes | No |
| LPDDR | | 1.8 | Yes | No |
| PCI33 | | 3.3 | Yes | No |
| VREF1_DRIVER | | 1.8/1.2/1.35/1.5 | No | Yes |

Table 2-3 Output I/O Standards and Configuration Options supported by GW5A-25

| I/O output standard | Single-ended / Differential | Bank V _{CCIO} (V) | Drive Strength (mA) | Typical Applications |
|---------------------|-----------------------------|----------------------------|---------------------|---|
| MIPI | Differential (MIPI) | 1.8/2.5/3.3 | 2/4 | Mobile Industry Processor Interface |
| MIPI_4MA | Differential (ELVDS) | 1.8 | 4 | Mobile Industry Processor Interface |
| LVDS25 | Differential(TLVDS) | 2.5/3.3 | 3.5/2.5/4.5/6 | High-speed point-to-point data transmission |
| BLVDS25 | | 2.5/3.3 | 3.5/2.5/4.5/6 | Multi-point high-speed data transmission |
| RSDS | | 2.5/3.3 | 3.5/2.5/4.5/6 | High-speed point-to-point data transmission |
| MINILVDS | | 2.5/3.3 | 3.5/2.5/4.5/6 | LCD timing driver interface and column driver interface |
| PPLVDS | | 2.5/3.3 | 3.5/2.5/4.5/6 | LCD row/column driver |
| LVDS25E | Differential | 2.5 | 8/2/4/6/12/16 | High-speed point-to-point data transmission |

| I/O output standard | Single-ended / Differential | Bank V _{CCIO} (V) | Drive Strength (mA) | Typical Applications |
|---------------------|-----------------------------|----------------------------|---------------------|---|
| BLVDS25E | | 2.5 | 8/2/4/6/12/16 | Multi-point high-speed data transmission |
| MLVDS25E | | 2.5 | 8/2/4/6/12/16 | LCD timing driver interface and column driver interface |
| RSDS25E | | 2.5 | 8/2/4/6/12/16 | High-speed point-to-point data transmission |
| LVPECL33E | | 3.3 | 8/2/4/6/12/16 | Universal interface |
| HSUL12D | | 1.2 | 8/2/4/6 | LPDDR2 |
| HSUL12D_I | | 1.2 | 8/2/4/6 | LPDDR2 |
| HSTL15D_I | | 1.5 | 8/4/12 | Memory interface |
| HSTL18D_I | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| HSTL18D_II | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| SSTL12D_I | | 1.2 | 8/2/4/6 | Memory interface |
| SSTL135D_I | | 1.35 | 8/2/4/6 | Memory interface |
| SSTL15D_I | | 1.5 | 8/2/4/6/12 | Memory interface |
| SSTL18D_I | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| SSTL18D_II | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| SSTL25D_I | | 2.5 | 8/2/4/6/12/16 | Memory interface |
| SSTL25D_II | | 2.5 | 8/2/4/6/12/16 | Memory interface |
| SSTL33D_I | | 3.3 | 8/2/4/6/12/16 | Memory interface |
| SSTL33D_II | | 3.3 | 8/2/4/6/12/16 | Memory interface |
| LPDDR | | 1.8 | 8/2/4/6/12/16 | LPDDR and Mobile DDR |
| LVC MOS10D | | 1.0 | 2/4 | Universal interface |
| LVC MOS12D | | 1.2 | 8/2/4/6 | Universal interface |
| LVC MOS15D | | 1.5 | 8/2/4/6/12 | Universal interface |
| LVC MOS18D | | 1.8 | 8/2/4/6/12/16 | Universal interface |
| LVC MOS25D | | 2.5 | 8/2/4/6/12/16 | Universal interface |
| LVC MOS33D | | 3.3 | 8/2/4/6/12/16 | Universal interface |
| HSUL12 | Single-ended | 1.2 | 8/2/4/6 | Memory interface |
| HSTL12_I | | 1.2 | 8/2/4/6 | Memory interface |
| HSTL15_I | | 1.5 | 8/2/4/6/12 | Memory interface |
| HSTL18_I | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| HSTL18_II | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| SSTL12_I | | 1.2 | 8/2/4/6 | Memory interface |
| SSTL135_I | | 1.35 | 8/2/4/6 | Memory interface |
| SSTL15_I | | 1.5 | 8/2/4/6/12 | Memory interface |
| SSTL18_I | | 1.8 | 8/2/4/6/12/16 | Memory interface |

| I/O output standard | Single-ended / Differential | Bank V _{CCIO} (V) | Drive Strength (mA) | Typical Applications |
|---------------------|-----------------------------|----------------------------|---------------------|------------------------|
| SSTL18_II | | 1.8 | 8/2/4/6/12/16 | Memory interface |
| SSTL25_I | | 2.5 | 8/2/4/6/12/16 | Memory interface |
| SSTL25_II | | 2.5 | 8/2/4/6/12/16 | Memory interface |
| SSTL33_I | | 3.3 | 8/2/4/6/12/16 | Memory interface |
| SSTL33_II | | 3.3 | 8/2/4/6/12/16 | Memory interface |
| LVC MOS10 | | 1.0 | 2/4 | Universal interface |
| LVC MOS12 | | 1.2 | 8/2/4/6 | Universal interface |
| LVC MOS15 | | 1.5 | 8/2/4/6/12 | Universal interface |
| LVC MOS18 | | 1.8 | 8/2/4/6/12/16 | Universal interface |
| LVC MOS25 | | 2.5 | 8/2/4/6/12/16 | Universal interface |
| LVC MOS33/L VTTL33 | | 3.3 | 8/2/4/6/12/16 | Universal interface |
| LPDDR | | 1.8 | 8/2/4/6/12/16 | LPDDR and Mobile DDR |
| PCI33 | | 3.3 | 8/2/4/6/12/16 | PC and embedded system |

Table 2-4 Input I/O Standards and Configuration Options Supported by GW5A-25

| I/O Input Standard | Single-ended / Differential | Bank V _{CCIO} (V) | Hysteresis | Need V _{REF} |
|--------------------|-----------------------------|------------------------------------|------------|-----------------------|
| MIPI | Differential | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| ADC_in | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| LVDS25 | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| BLVDS25 | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| RSDS | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| MINILVDS | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| PPLVDS | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| HSUL12D | | 1.2/1.0/1.5/1.8/2.5/3.3 | No | No |
| HSTL12D_I | | 1.2/1.0/1.5/1.8/2.5/3.3 | No | No |
| HSTL15D_I | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| HSTL18D_I | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| HSTL18D_II | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| SSTL135D_I | | 1.35/ 1.0/ 1.2/ 1.5/ 1.8/ 2.5/ 3.3 | No | No |
| SSTL15D_I | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| SSTL18D_I | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| SSTL18D_II | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| SSTL2D_I | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| SSTL2D_II. | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| SSTL3D_I | | 3.3/1.0/1.2/1.5/1.8/2.5 | No | No |
| SSTL3D_II. | | 3.3/1.0/1.2/1.5/1.8/2.5 | No | No |
| LPDDR | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |

| I/O Input Standard | Single-ended / Differential | Bank V_{CCIO} (V) | Hysteresis | Need V_{REF} |
|--------------------|-----------------------------|-------------------------|------------|----------------|
| LVC MOS10D | | 1.0/1.2/1.5/1.8/2.5/3.3 | No | No |
| LVC MOS12D | | 1.2/1.0/1.5/1.8/2.5/3.3 | No | No |
| LVC MOS15D | | 1.5/1.0/1.2/1.8/2.5/3.3 | No | No |
| LVC MOS18D | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | No |
| LVC MOS25D | | 2.5/1.0/1.2/1.5/1.8/3.3 | No | No |
| LVC MOS33D | | 3.3/1.0/1.2/1.5/2.5/1.8 | No | No |
| HSUL12 | Single-ended | 1.2 | No | Yes |
| HSTL12_I | | 1.2 | No | Yes |
| HSTL15_I | | 1.5 | No | Yes |
| HSTL15_II | | 1.5 | No | Yes |
| HSTL18_I | | 1.8 | No | Yes |
| HSTL18_II | | 1.8 | No | Yes |
| SSTL135_I | | 1.35 | No | Yes |
| SSTL15_I | | 1.5 | No | Yes |
| SSTL18_I | | 1.8 | No | Yes |
| SSTL18_II | | 1.8 | No | Yes |
| SSTL2_I | | 2.5 | No | Yes |
| SSTL2_II | | 2.5 | No | Yes |
| SSTL3_I | | 3.3 | No | Yes |
| SSTL3_II | | 3.3 | No | Yes |
| LVC MOS10 | | 1.0 | Yes | No |
| LVC MOS12 | | 1.2 | Yes | No |
| LVC MOS15 | | 1.5 | Yes | No |
| LVC MOS18 | | 1.8 | Yes | No |
| LVC MOS25 | | 2.5 | Yes | No |
| LVC MOS33/LVTT L33 | | 3.3 | Yes | No |
| LPDDR | | 1.8 | Yes | No |
| PCI33 | | 3.3 | Yes | No |
| LVC MOS10UD12 | | 1.2 | No | No |
| LVC MOS10UD15 | | 1.5 | No | No |
| LVC MOS10UD18 | | 1.8 | No | No |
| LVC MOS10UD25 | | 2.5 | No | No |
| LVC MOS10UD33 | | 3.3 | No | No |
| LVC MOS12OD10 | | 1.0 | No | No |
| LVC MOS12UD15 | | 1.5 | No | No |
| LVC MOS12UD18 | | 1.8 | No | No |
| LVC MOS12UD25 | | 2.5 | No | No |
| LVC MOS12UD33 | | 3.3 | No | No |

| I/O Input Standard | Single-ended / Differential | Bank V_{CCIO} (V) | Hysteresis | Need V_{REF} |
|--------------------|-----------------------------|-------------------------|------------|----------------|
| LVC MOS15OD10 | | 1.0 | No | No |
| LVC MOS15OD12 | | 1.2 | No | No |
| LVC MOS15UD18 | | 1.8 | No | No |
| LVC MOS15UD25 | | 2.5 | No | No |
| LVC MOS15UD33 | | 3.3 | No | No |
| LVC MOS18OD10 | | 1.0 | No | No |
| LVC MOS18OD12 | | 1.2 | No | No |
| LVC MOS18OD15 | | 1.5 | No | No |
| LVC MOS18UD25 | | 2.5 | No | No |
| LVC MOS18UD33 | | 3.3 | No | No |
| LVC MOS25OD10 | | 2.5 | No | No |
| LVC MOS25OD12 | | 3.3 | No | No |
| LVC MOS25OD15 | | 1.5 | No | No |
| LVC MOS25OD18 | | 1.8 | No | No |
| LVC MOS25UD33 | | 3.3 | No | No |
| LVC MOS33OD10 | | 1.0 | No | No |
| LVC MOS33OD12 | | 1.2 | No | No |
| LVC MOS33OD15 | | 3.3 | No | No |
| LVC MOS33OD18 | | 1.8 | No | No |
| LVC MOS33OD25 | | 2.5 | No | No |
| VREF1_DRIVER | | 1.8/1.0/1.2/1.5/2.5/3.3 | No | Yes |

2.3.2 I/O Logic

Figure 2-6 shows the I/O logic output of GW5A series of FPGA products.

Figure 2-6 I/O Logic Output

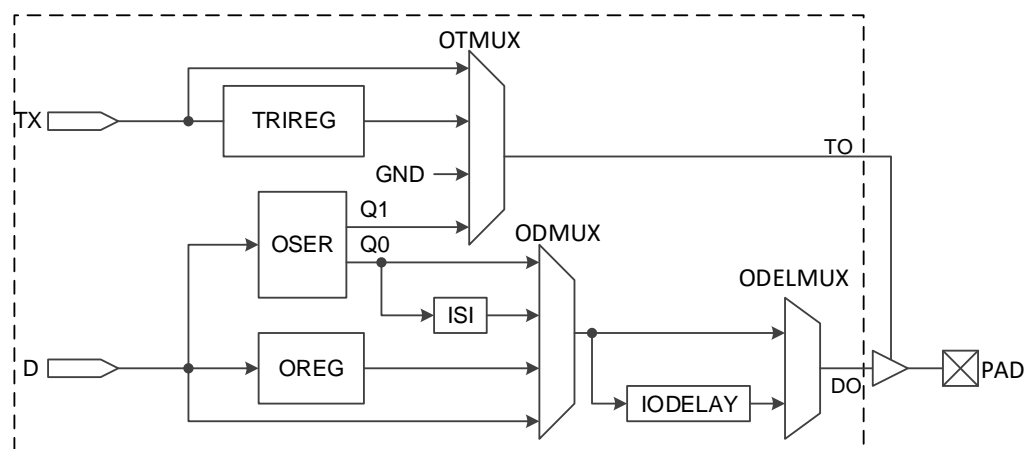
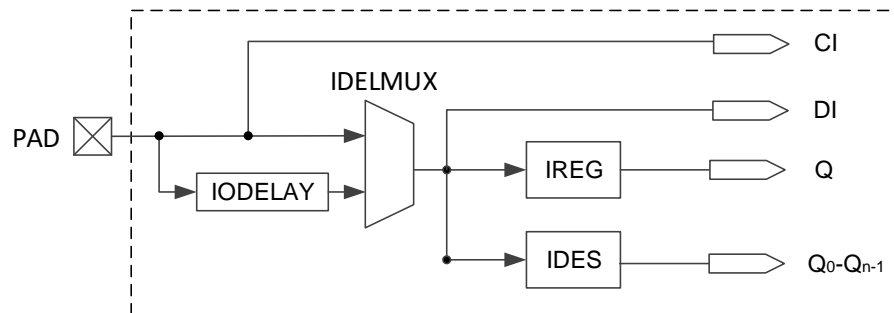


Figure 2-7 shows the I/O logic input of the GW5A series of FPGA products.

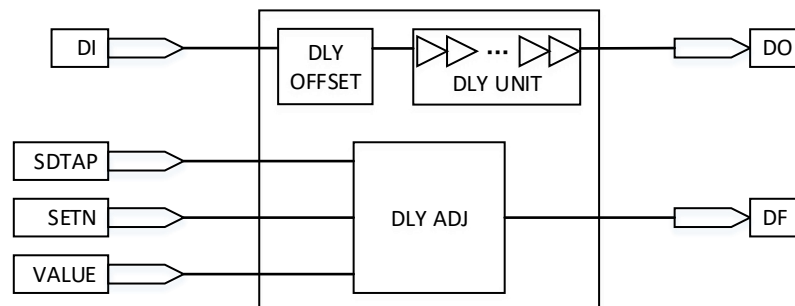
Figure 2-7 I/O Logic Input**Note!**

CI is a GCLK input signal and cannot be connected to the fabric; DI is input directly to the fabric.

Descriptions of the I/O logic modules of GW5A series of FPGA products are presented below.

Delay Modules

See Figure 2-8 for an overview of the IODELAY. Each I/O of GW5A includes IODELAY, providing a total of 256 (0~255) delays, with a single-step delay time of about 15.5ps. The total delay time achieved by IODELAY is $DLYOFFSET + DLY\ UNIT * SDTAP$.

Figure 2-8 IODELAY

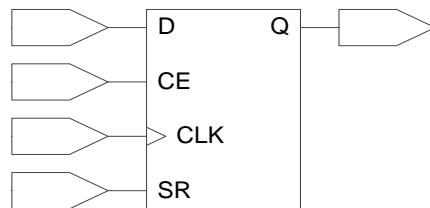
There are three ways to control the delay:

- Static control.
- Dynamic control, which can be combined with logic function circuits to achieve dynamic delay adjustment.
- Adaptive control.

I/O Register

See Figure 2-9 for the I/O register in GW5A series of FPGA products. Each I/O of the GW5A series of FPGA products provides one input register (IREG), one output register (OREG), and one tristate Register (TREG).

Figure 2-9 Diagram of I/O registers of GW5A

**Note!**

- CE can be either active low (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The registers can be programmed as registers(DFFs) or latches.

De-serializer DES and Serializer SER

The GW5A series of FPGA Products support serialization and deserialization of various ratios, as shown in Table 2-5.

Table 2-5 DES /SER Ratios Supported by the GW5A Series of FPGA Products

| | Ratios Supported |
|--------------|---|
| Input logic | 1:2 / 1:4 / 1:7 / 1:8 / 1:10 / 1:14 / 1:16 / 1:32 |
| Output logic | 2:1 / 4:1 / 7:1 / 8:1 / 10:1 / 16:1 / 14:1 ^[1] |

Note!

Only GW5A-25 supports 14:1 OSER.

2.3.3 I/O Logic Modes

The I/O Logic in GW5A series of FPGA products supports several modes. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

For more details, refer to [UG304, Arora V Programmable IO \(GPIO\) User Guide](#).

2.4 Block SRAM (BSRAM)

2.4.1 Introduction

GW5A series of FPGA products provide abundant block SRAM resources. These memory resources are distributed throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). Up to 36Kbits can be configured for each BSRAM. There are five operation modes: Single Port mode, Dual Port mode, Semi Dual Port mode, Semi Dual Port mode with ECC function^[1], and ROM mode.

Note!

Only GW5A-138 supports Semi Dual Port mode with ECC function.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM's features:

- GW5A-25: Up to 18Kbits per BSRAM
- GW5A-138: Up to 36Kbits per BSRAM
- Clock frequency up to 380MHz (230MHz in Read-before-Write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi Dual Port Mode
- Supports ECC detection and error correction Function
- Supports ROM Mode
- GW5A-25: Data width up to 36bits
- GW5A-138: Data width up to 72bits
- Dual Port and Semi-dual Port support independent clocks and independent data width
- Read mode supports Register Output and Bypass Output
- Write mode supports Normal, Read-before-Write ^[1], and Write-Through

Note!

[1] Only GW5A-25 supports Read-before-Write mode.

2.4.2 Configuration Mode

BSRAMs in the GW5A series of FPGA products support various data widths. See Table 2-6.

Table 2-6 Memory Size Configuration

| Capacity | Single Port Mode | Dual Port Mode | Semi Dual Port Mode | Semi Dual Port Mode with ECC Function | Read Only Mode |
|----------|------------------|----------------|---------------------|---------------------------------------|----------------|
| 16Kbits | 16K x 1 | 16K x 1 | 16K x 1 | — | 16K x 1 |
| | 8K x 2 | 8K x 2 | 8K x 2 | — | 8K x 2 |
| | 4K x 4 | 4K x 4 | 4K x 4 | — | 4K x 4 |
| | 2K x 8 | 2K x 8 | 2K x 8 | — | 2K x 8 |
| | 1K x 16 | 1K x 16 | 1K x 16 | — | 1K x 16 |
| | 512 x 32 | — | 512 x 32 | — | 512 x 32 |
| 18Kbits | 2K x 9 | 2K x 9 | 2K x 9 | — | 2K x 9 |
| | 1K x 18 | 1K x 18 | 1K x 18 | — | 1K x 18 |
| | 512 x 36 | — | 512 x 36 | — | 512 x 36 |
| 36Kbits | — | — | — | 512 x 72 | — |

Single Port Mode

In the single port mode, BSRAM can write to or read from one port at one clock edge. It supports 2 read modes (Bypass and Pipeline) and 3 write modes (Normal, Write-Through, and Read-before-Write^[1]). In Normal-Write Mode, the written data will be stored in the internal memory array. In Write-Through Mode, the written data will not only be stored in the internal memory array, but also be written to the output of BSRAM. When the output register is Bypassed, the new data will show at the same write clock rising edge.

Note!

[1] Only GW5A-25 supports Read-before-Write mode.

For more information on single port mode, please refer to [UG300, Arora V BSRAM & SSRAM User Guide](#).

Dual Port Mode

BSRAM supports Dual Port mode. It supports 2 read modes (Bypass mode and Pipeline mode) and 3 write modes (Normal mode, Write-Through mode, and Read-before-Write mode^[1]). The applicable operations are as follows:

- Two independent read, reading data from any given address.
- Two independent write, writing data to any address that is different.
- An independent read and an independent write at different clock frequencies.

Note!

- [1] Only GW5A-25 supports Read-before-Write mode.
- In Dual-port mode, Port A and Port B can read from or write to the same address. Null or repeated reads do not damage the storage module.
- In Dual-port mode, when Port A and Port B write to the same address at the same time, the dual ports writing fail at the same time.
- When Port A reads, Port B writes, and they access the same address, the write port succeeds, but the read port fails, and the output data is unknown. BSRAM contents are the values from the write port.

Dual Port supports independent read/write clocks and independent read/write data width. For more information on dual port mode, please refer to [UG300, Arora V BSRAM & SSRAM User Guide](#).

Semi Dual Port Mode

Semi-dual ports support independent read/write operations in the form of A port write-only ("Normal") and B port read-only. When Port A reads, Port B writes, and they access the same address, the write port succeeds, but the read port fails, and the output data is unknown. BSRAM contents are the values from the write port.

Semi-dual Port supports independent read/write clocks and independent read/write data width. For more information on semi dual port mode, please refer to [UG300, Arora V BSRAM & SSRAM User Guide](#).

Semi Dual Port Mode with ECC Function

Semi-dual ports with ECC Function support independent read/write operations in the form of A port write-only and B port read-only. Independent read/write data width is also supported. This mode provides ECC function. For more information on this mode, please refer to [UG300, Arora V BSRAM & SSRAM User Guide](#).

Read Only Mode

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For more information on read only mode, please refer to [UG300, Arora V BSRAM & SSRAM User Guide](#).

2.4.3 Data Width Configuration

BSRAMs in the GW5A series of FPGA products support independent data width for read/write operations. In Dual Port mode, Semi Dual Port mode, and Semi Dual Port mode with ECC function (GW5A-138), the data width for Port A and Port B can be different. For the data width supported by Port A and Port B, see Table 2-7, Table 2-8, and Table 2-9.

Table 2-7 Read/Write Data Width Configuration in Dual Port Mode

| Capacity | Port B | Port A | | | | | | |
|----------|---------|---------|--------|--------|--------|---------|--------|---------|
| | | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 2K x 9 | 1K x 18 |
| 16Kbits | 16K x 1 | Yes | Yes | Yes | Yes | Yes | N/A | N/A |
| | 8K x 2 | Yes | Yes | Yes | Yes | Yes | N/A | N/A |
| | 4K x 4 | Yes | Yes | Yes | Yes | Yes | N/A | N/A |
| | 2K x 8 | Yes | Yes | Yes | Yes | Yes | N/A | N/A |
| | 1K x 16 | Yes | Yes | Yes | Yes | Yes | N/A | N/A |
| 18Kbits | 2K x 9 | N/A | N/A | N/A | N/A | N/A | Yes | Yes |
| | 1K x 18 | N/A | N/A | N/A | N/A | N/A | Yes | Yes |

Table 2-8 Read/Write Data Width Configuration in Semi Dual Port Mode

| Capacity | Port B | Port A | | | | | | | | | | |
|----------|---------|---------|--------|--------|--------|---------|----------|--------|---------|----------|---------|----------|
| | | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 512 x 32 | 2K x 9 | 1K x 18 | 512 x 36 | 1K x 36 | 512 x 72 |
| 16Kbits | 16K x 1 | Yes | Yes | Yes | Yes | Yes | Yes | N/A | N/A | N/A | N/A | N/A |
| | 8K x 2 | Yes | Yes | Yes | Yes | Yes | Yes | N/A | N/A | N/A | N/A | N/A |
| | 4K x 4 | Yes | Yes | Yes | Yes | Yes | Yes | N/A | N/A | N/A | N/A | N/A |
| | 2K x 8 | Yes | Yes | Yes | Yes | Yes | Yes | N/A | N/A | N/A | N/A | N/A |
| | 1K x 16 | Yes | Yes | Yes | Yes | Yes | Yes | N/A | N/A | N/A | N/A | N/A |

| Capacity | Port B | Port A | | | | | | | | | | |
|----------|----------|---------|--------|--------|--------|---------|---------|--------|---------|----------|---------|----------|
| | | 16K x 1 | 8K x 2 | 4K x 4 | 2K x 8 | 1K x 16 | 512x 32 | 2K x 9 | 1K x 18 | 512 x 36 | 1K x 36 | 512 x 72 |
| | 512 x 32 | Yes | Yes | Yes | Yes | Yes | Yes | N/A | N/A | N/A | N/A | N/A |
| 18Kbits | 2K x 9 | N/A | N/A | N/A | N/A | N/A | N/A | Yes | Yes | Yes | N/A | N/A |
| | 1K x 18 | N/A | N/A | N/A | N/A | N/A | N/A | Yes | Yes | Yes | N/A | N/A |

Table 2-9 Read/Write Data Width Configuration in Semi Dual Port Mode with ECC Function(GW5A-138)

| Capacity | Port B | Port A | |
|----------|----------|---------|----------|
| | | 1K x 36 | 512 x 72 |
| 36Kbits | 512 x 72 | N/A | Yes |

2.4.4 ECC(GW5A-138)

The BSRAM of GW5A-138 has a built-in ECC hardcore module, which is mainly used for data detection and correction during data transfer and storage. ECC features are as follows:

- ECC error detection and correction only supported in SDP 512 x 64 mode
- Supports 1-bit error correction and 2-bit error alarm in 64-bit SRAM data
- 72-bit ECC module contains 64-bit data bits and 8-bit parity bits;
- Bit 31 and bit 63 support 1-bit and 2-bit error injection

2.4.5 Byte-enable

BSRAM supports the byte_enable function- only the selected byte can be written. The byte_enable function is used for writing only and is available when the bit width is 16/18, 32/36. Read/write enable ports (WREA, WREB), and byte parameter options can be used to control the BSRAM write operation.

2.4.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write.
- The output register can be used as a Pipeline register to improve design performance.
- The output registers can be bypassed.

2.4.7 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass and Pipeline e) and three write operations (Normal, Write-Through, and Read-before-Write).

Read Mode

Read data from the BSRAM via output registers or without using the registers.

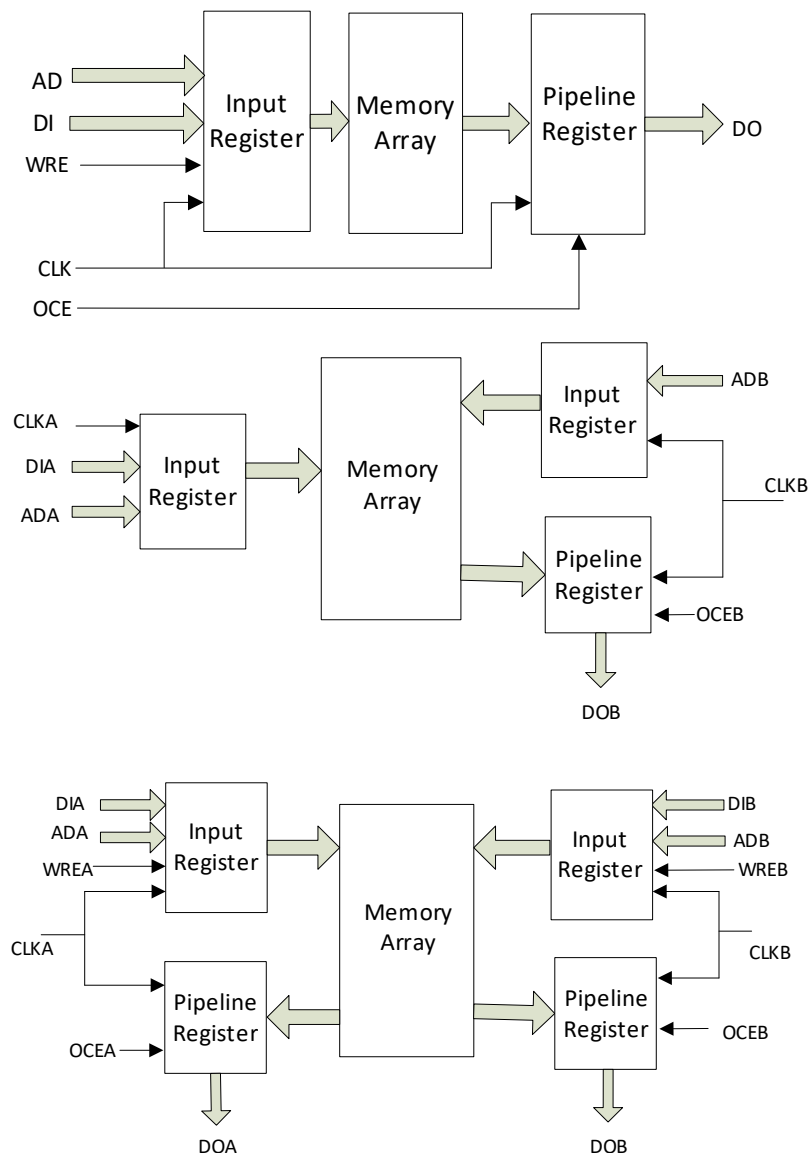
PIPELINE

When reading data, the data is synchronously read out via the output register according to the clock beat. This mode supports up to 72-bit data width.

BYPASS

In this mode, the output register is not used. When reading data, the data is directly sent to the output port.

Figure 2-10 Pipeline in Single Port, Dual Port, and Semi-Dual Port Mode



Write Mode

NORMAL

In this mode, when the user writes data to one port, and the output

data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE^[1]

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

Note!

[1] Only GW5A-25 supports Read-before-Write mode.

2.4.8 Clock Modes

Table 2-10 lists the clock modes in different BSRAM modes:

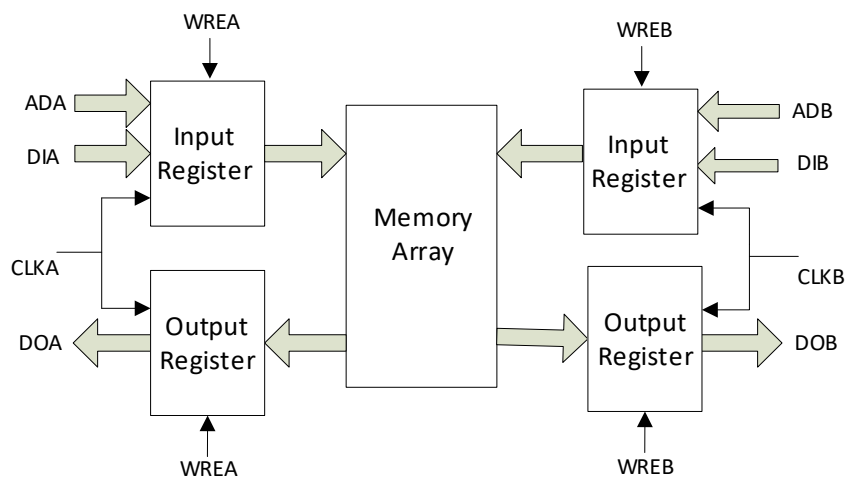
Table 2-10 Clock Modes in Different BSRAM Modes

| Clock Mode | BSRAM Mode | | |
|------------------------|----------------|---------------------|------------------|
| | Dual Port Mode | Semi Dual Port Mode | Single Port Mode |
| Independent Clock Mode | Yes | No | No |
| Read/Write Clock Mode | Yes | Yes | No |
| Single Port Clock Mode | No | No | Yes |

Independent Clock Mode

Figure 2-11 shows the independent clocks in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

Figure 2-11 Independent Clock Mode

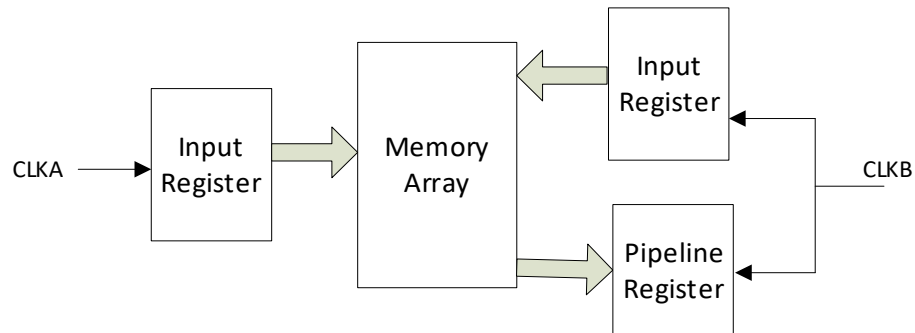


Read/Write Clock Operation

Figure 2-12 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls

Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

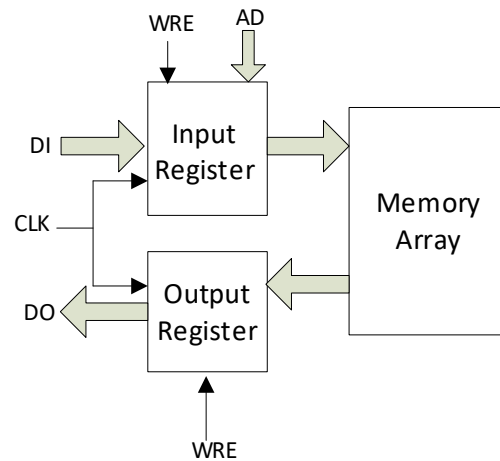
Figure 2-12 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-13 shows the clock operation in single port mode.

Figure 2-13 Single Port Clock Mode



2.5 DSP Blocks

GW5A series of FPGA Products provide brand new DSP resources. This DSP solution can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high resource utilization, and low power consumption.

The features of DSP are as follows.

- Can be configured as 12 x 12, 27 x 28, and 27 x 36 signed multipliers
- 48-bit ALU
- Multipliers cascading to support wider data
- Barrel Shifter
- Adaptive filtering through signal feedback
- Supports Pipeline mode and Bypass mode.
- All operands for arithmetic operation are signed numbers

Each DSP consists of three main parts:

- PADD
- MULT
- Arithmetic logic unit (ALU)

2.5.1 PADD

Each DSP features one PADD(pre-adder) for implementing pre-addition, pre-subtraction, and shifting.

PADD is located at the first stage with two inputs:

- 26-bit input C;
- Parallel 26-bit input A or SIA.

Each input end supports Pipeline mode and Bypass mode.

2.5.2 MULT

Each DSP has one 27 x 18 multiplier M0 and one 12 x 12 multiplier M1. The multipliers are located after the pre-adders to implement multiplication operations, and both the inputs and outputs support register mode and Bypass mode.

Multiplier M0 can be configured as:

- One 27 x 18 multiplier
- One 12 x 12 multiplier
- Two DSPs can form one 27 x 36 multiplier

Multiplier M1 can only be configured as one 12 x 12 multiplier.

When multiplier M0 and multiplier M1 are both configured as a 12 x

12 multiplier and the ALU is enabled, 12 x 12 SUM mode can be achieved.

2.5.3 Arithmetic Logic Unit

Each DSP has one four-input 48-bit ALU, which can further enhance MULT's functions. Register mode and Bypass mode are supported both in the inputs and outputs. The ALU supports the addition/subtraction operations of multiplier M0 output, multiplier M1 output(48bit operand D), ALU cascade input CASI, and ALU output feedback or static PRE_LOAD value.

2.5.4 Operation Mode

Based on control signals, DSP can be configured as different operation modes. Operation Modes:

- Multiplier
- Accumulator
- MULTADDALU

For more information on DSP Blocks, see [UG305, Arora V Digital Signal Processing \(DSP\) User Guide](#).

2.6 MIPI D-PHY

2.6.1 MIPI D-PHY RX(GW5A-138)

GW5A-138 provides a MIPI D-PHY RX hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The main features are as follows:

- High Speed RX with the bandwidth up to 20 Gbps (eight data lanes).
- One MIPI Quad supports up to four data lanes and one clock lane.
- Bidirectional Low-power (LP) mode at up to 10Mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports MIPI DSI and MIPI CSI-2 link layers

For more information on Gowin MIPI D-PHY RX/TX, please refer to [UG296, Arora V Hardened MIPI D-PHY User Guide](#).

2.6.2 MIPI D-PHY RX/TX(GW5A-25)

GW5A-25 provides a MIPI D-PHY RX/TX hardcore supporting the “MIPI Alliance Standard for D-PHY Specification(V1.2)”. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The main features are as follows:

- High Speed RX/TX with the bandwidth up to 10 Gbps (four data lanes)

- One MIPI Quad supports up to four data lanes and one clock lane.
- Bidirectional Low-power (LP) mode at up to 10Mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports MIPI DSI and MIPI CSI-2 link layers

For more information on Gowin MIPI D-PHY RX/TX, please refer to [UG296, Arora V Hardened MIPI D-PHY User Guide](#).

2.7 ADC

The GW5A series of FPGA products integrate a new flexible analog interface as a temperature and power sensor. When combined with the programmable logic capability of the FPGA, the sensor can address the data acquisition and monitoring requirements for temperature and power monitoring.

Highlights of the sensor architecture include:

- On-chip reference, no off-chip voltage reference required
- 60dB SNR
- 10-bit oversampling @ 2MHz
- 1kHz Signal Bandwidth
- GW5A-138: two dedicated analog channels, able to detect input signals from GPIO at the same time
- GW5A-25: one dedicated analog channels, able to detect input signals from GPIO at the same time
- On-chip temperature ($\pm 4^{\circ}\text{C}$ max error) and voltage ($\pm 1\%$ max error) sensors
- Continuous access to ADC measurements

The sensor optionally uses an on-chip reference circuit ($\pm 1\%$), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails.

For more information on ADC, see [UG299, Arora V Analog to Digital Converter \(ADC\) User Guide](#).

2.8 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. GW5A series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. In addition to the GCLK, PLL, HCLK, DDR memory interface, and DQS, etc. are also provided.

Figure 2-14 GW5A-138 Clock Resources

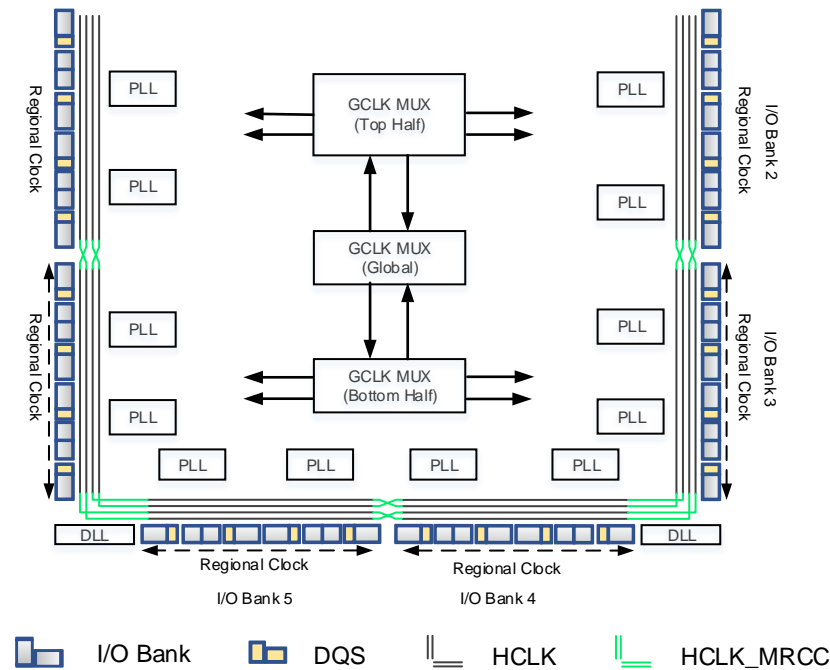
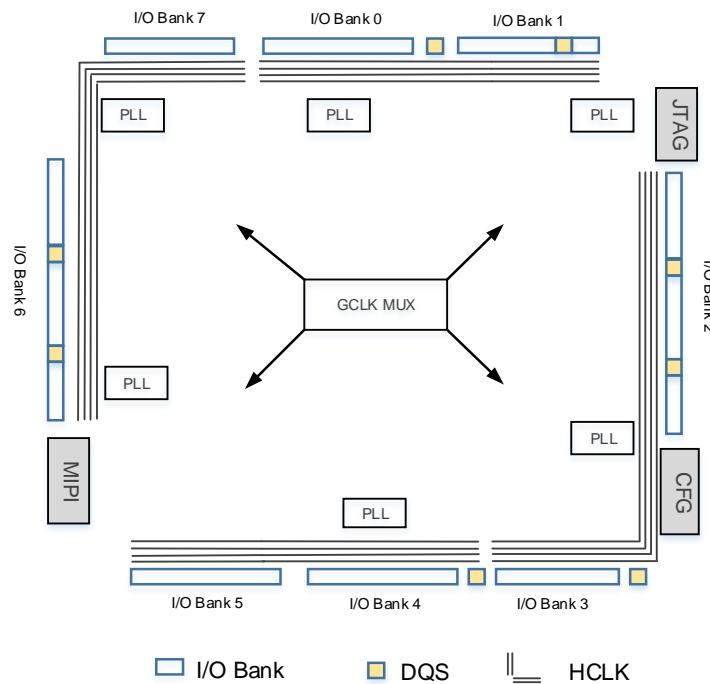


Figure 2-15 GW5A-25 Clock Resources



Please refer to 2.8.1 ~ 2.8.4 for a brief introduction. For further detailed information on the GCLK, HCLK, DDR memory interface, and DQS, see [UG306, Arora V Clock User Guide](#).

2.8.1 Global Clock

GW5A series FPGA products provide 16 global clocks. The clock source of GCLK comes from dedicated clock pins, PLL output, SERDES

clock, HCLK output and common wiring resources. Dedicated clock input pins offer better clock performance and enable global driving.

2.8.2 HCLK

HCLK is the high-speed clock with low jitter and low skew. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. One bank supports 4 HCLKs, as shown in Figure 2-16 and Figure 2-17.

Figure 2-16 GW5A-138 HCLK Distribution

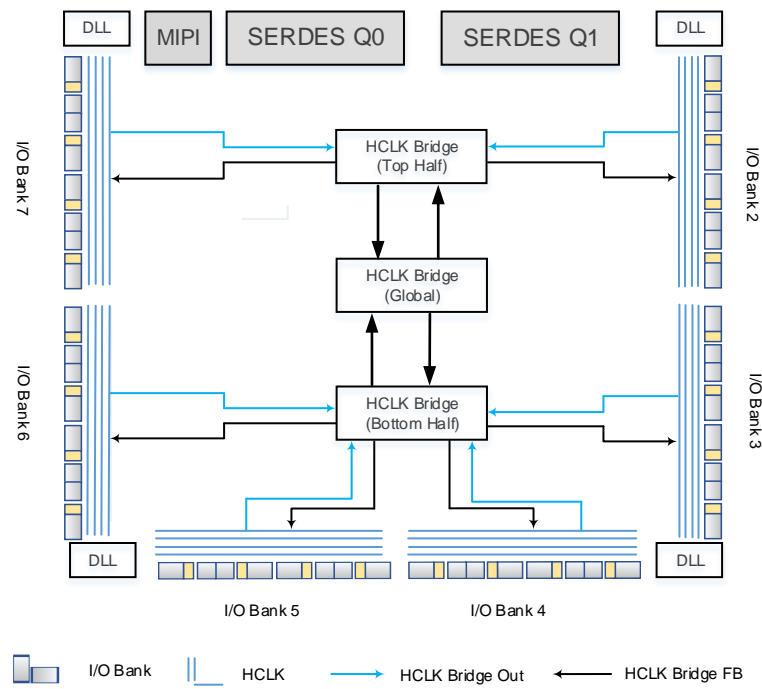
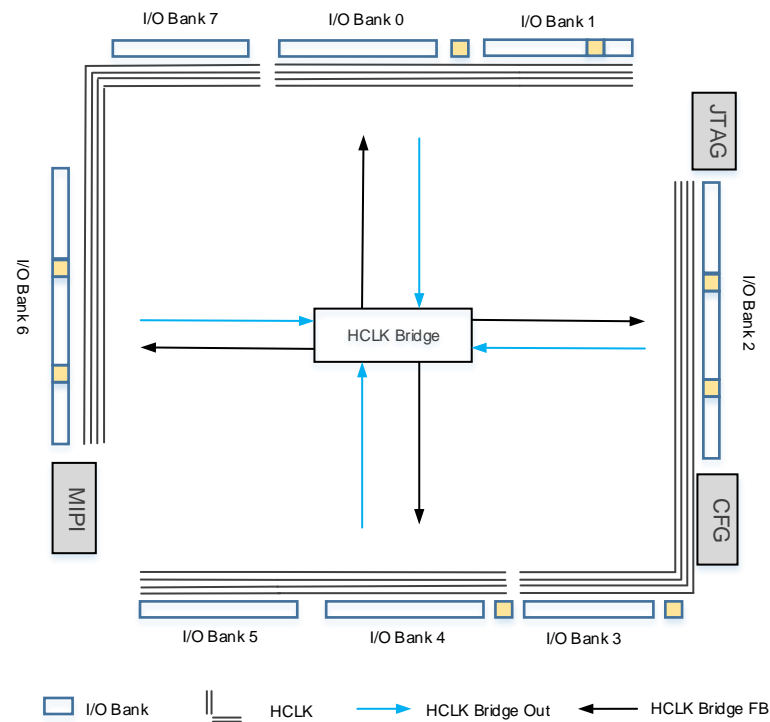


Figure 2-17 GW5A-138 HCLK Distribution

HCLK can provide users with the function modules as follows:

- Dynamic high-speed clock enable module. Able to dynamically turn on/off the high-speed clock signal.
- High speed clock frequency division module, generating a divided clock of the input clock. Used in the IO logic mode.
- Dynamic high speed clock selector.
- Dynamic delay adjustment module, producing the clock signal for the dedicated clock pin input.
- The HCLK bridge module is able to send HCLK clock signals to any of the Banks. In addition, the HCLK clock signal can span to the clock tree of the adjacent IO Bank after entering from the IO Bank.

Note!

For high speed signals of the same source, it is recommended to put them in the same IO Bank to achieve a minimum skew between signals.

2.8.3 Phase-locked Loop

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

The PLL module of the GW5A series FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

The features of the PLL module of the GW5A series FPGA products are as follows:

- Supports seven clock outputs
- Integer PLL, the first clock output and feedback clock output support 1/8 fractional output division
- Supports phase shift and duty cycle adjustment
- Frequency Lock detection
- Supports spread spectrum clock generation (IP required)
- VCO frequency range: 800 MHz ~ 2000 MHz
- GW5A-138 CLKIN frequency range: 10 MHz ~ 400 MHz
- GW5A-25 CLKIN frequency range: 19 MHz ~ 800 MHz

2.8.4 DDR Memory Interface Clock Management DQS

The DQS module of the GW5A series of FPGA products provides the following features to support the clock requirements of the DDR memory interface:

- Receive DQS input, sort out waveform and shift 1/4 phase
- Provide a read / write pointer for input buffer
- Provide valid data for internal logic
- Provide DDR output clock signal
- Support DDR3 write voltage control

The DQS module supports multiple operating modes to meet the needs of different I/O interfaces.

2.8.5 Long Wire

As a supplement to CRU, the GW5A series of FPGA products provide another routing resource- Long Wire, which is suitable for clock, clock enable, set/reset, or other high fan out signals.

2.9 Global Set/Reset (GSR)

A global set/reset (GSR) network is built in the GW5A series of FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

2.10 Programming & Configuration

The GW5A series of FPGA products support SRAM configuration. Each time the device is powered on, the bitstream needs to be downloaded to configure the device. Of course, you can also save the configuration data in an external Flash. After power-up, the GW5A device loads configuration data from the external Flash into the SRAM.

Besides JTAG, the GW5A series of FPGA products also support GOWINSEMI's own GowinCONFIG configuration mode: SSPI, MSPI, CPU, SERIAL. The FPGAs also support background programming, datastream file encryption and security bit setting, SEU detection and error correction, and OTP. For more information, please refer to [UG704, Arora V FPGA Products Programming and Configuration User Guide](#).

Background Upgrade

GW5A series of FPGAs support background upgrade by JTAG/SSPI/QSSPI or UserLogic, that is, the device supports programming the embedded Flash or the external Flash without affecting the existing working state, the device can work normally according to the original configuration during the programming process. And after the programming is completed, trigger RECONFIG_N with a low level to complete the online upgrade. This feature applies to the applications requiring long online time and irregular upgrades.

Bitstream File Encryption & Security Bit Setting

GW5A series of FPGA products support bitstream data encryption with 128-bit AES encryption algorithm. At the same time, GOWINSEMI adds CRC and sets security bits in the bitstream file of FPGA products by default in order to guarantee the safe and accurate transmission of configuration data. During the data configuration process, the input data is verified in real time for errors, and the device cannot be woken up by incorrect data. After the configuration of the bitstream with security bit is complete, data readback cannot be performed.

CM SER (GW5A-138)

The configuration SRAM of GW5A series of FPGA products supports configuration memory soft error recovery (CM SER), which are mainly used for data detection and correction of the FPGA configuration data and are disabled by default. The features are as follows:

- Supports ECC and CRC error detection and correction. Turning on the auto-on mode after wakeup according to the user configuration or using the user design logic control to turn on/off error detection and correction.
- ECC supports 1-bit error location report and error correction^[1] and 2-bit error alarm per 64-bit SRAM data.

Note!

Advanced CM SER supports faster error correction.

- CRC supports any bit error alarm.
- Supports 1-bit error injection at any position, one error per 64-bit SRAM data.
- The detection and error correction function of SRAM in this storage area will be automatically turned off when the user turns on the SSRAM storage function.

CMSER (GW5A-25)

The configuration SRAM of GW5A series of FPGA products supports configuration memory soft error recovery (CMSER), which are mainly used for data detection and correction of the FPGA configuration data and are disabled by default. The features are as follows:

- Supports ECC and CRC error detection and correction. Turning on the auto-on mode after wakeup according to the user configuration or using the user design logic control to turn on/off error detection and correction.
- ECC supports 2-bit error location report and error correction^[1] and 4-bit error alarm in each SRAM Frame.

Note!

Advanced CMSER supports faster error correction.

- CRC supports any bit error alarm.
- Supports 1-bit error injection at any position, two errors in each SRAM Frame.
- The detection and error correction function of SRAM in this storage area will be automatically turned off when the user turns on the SSRAM storage function.

mDRP

GW5A series FPGA products support independent mDRP ports, allowing point-to-point structure access.

OTP

GW5A series of FPGAs provide a 128-bit OTP space and support one-time programming. Bit0 ~ Bit31 is the user space, which can be used to store security and other important information. Bit32~Bit95 is the DNA space, which stores the 64-bit unique identification information of the device.

2.11 On Chip Oscillator

There is an internal oscillator in each of the GW5A series of FPGA products. During the configuration process, it can provide a clock for the MSPI mode. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

$$f_{\text{out}} = 210\text{MHz}/\text{Param.}$$

Note!

“Param” is the configuration parameter. It should 3 or an even number between 2 and 126.

3 AC/DC Characteristics

Note!

You should ensure GOWINSEMI® products are always used within recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI® does not guarantee that all devices will operate as expected beyond the standard operating conditions and range.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings(GW5A-25)

| Name | Description | Min. | Max. |
|----------------------|--------------------------------------|-------|--------|
| FPGA Logic | | | |
| V _{CC} | Core voltage, LV | -0.5V | 1.05V |
| | Core voltage, EV | -0.5V | 3.75V |
| V _{CCIO} | I/O Bank voltage | -0.5V | 3.75V |
| V _{CCX} | Auxiliary voltage | -0.5V | 3.75V |
| V _{CC_REG} | Regulator voltage | -0.5V | 3.75V |
| V _{IN} | Single-ended input | -0.4V | 3.75V |
| | Differential input | -0.4V | 2.625V |
| MIPI | | | |
| M0_VDD_12 | Power supply pin of MIPI LP voltage. | -0.5V | 1.32V |
| Temperature | | | |
| Storage Temperature | Storage Temperature | -65℃ | +150℃ |
| Junction Temperature | Junction Temperature | -40℃ | +125℃ |

Table 3-2 Absolute Max. Ratings(GW5A-138)

| Name | Description | Min. | Max. |
|-----------------------|----------------------------------|-------|--------|
| FPGA Logic | | | |
| V _{CC} | Core voltage | -0.5V | 1.05V |
| V _{CCIO} | I/O Bank voltage | -0.5V | 3.75V |
| V _{CCX} | Auxiliary voltage | -0.5V | 1.98V |
| V _{CC_REG} | Regulator voltage | -0.5V | 1.98V |
| V _{IN} | Single-ended input | -0.4V | 3.75V |
| | Differential input | -0.4V | 2.625V |
| MIPI | | | |
| V _{dda} | Analog core power supply | -0.5V | 1.05V |
| V _{ddx_dphy} | Analog high voltage power supply | -0.5V | 1.98V |
| Temperature | | | |
| Storage Temperature | Storage Temperature | -65℃ | +150℃ |
| Junction Temperature | Junction Temperature | -40℃ | +125℃ |

3.1.2 Recommended Operating Conditions

Table 3-3 Recommended Range(GW5A-25)

| Name | Description | Min. | Max. |
|---------------------|---|--------|--------|
| V _{CC} | Core voltage, LV | 0.855V | 1.0V |
| | Core voltage, EV ^[1] | 1.14V | 1.8V |
| V _{CCIO} | I/O Bank voltage | 1V | 3.465V |
| V _{CCX} | Auxiliary voltage | 2.375V | 3.465V |
| V _{CC_REG} | Regulator voltage | 1.14V | 3.3V |
| MIPI | | | |
| M0_VDD_12 | Power supply pin of MIPI LP voltage. | 1.14V | 1.32V |
| Temperature | | | |
| T _{JCOM} | Junction temperature Commercial operation | 0 °C | +85 °C |
| T _{JIND} | Junction temperature Industrial operation | -40℃ | +100℃ |

Note!

- [1] The 1.2V core voltage of EV version devices is generated by the built-in LDO. The higher the V_{CC} voltage, the higher the system power consumption.
- [2] Please refer to [UG985, GW5A-25 Pinout](#) for the supply voltage information of the devices in different packages.

Table 3-4 Recommended Range^[1] (GW5A-138)

| Name | Description | Min. | Max. |
|------------------------------------|---|-------|--------|
| V _{CC} | Core voltage | 0.87V | 1.0V |
| V _{CCIO} | I/O Bank voltage | 1V | 3.465V |
| V _{CCX} | Auxiliary voltage | 1.71V | 1.89V |
| V _{CC_REG} ^[2] | Regulator voltage | 1.14V | 1.89V |
| MIPI | | | |
| V _{dda} | Analog core power supply | 0.87V | 1.0V |
| V _{ddx_dphy} | Analog high voltage power supply | 1.71V | 1.89V |
| Temperature | | | |
| T _{JCOM} | Junction temperature Commercial operation | 0 °C | +85 °C |
| T _{JIND} | Junction temperature Industrial operation | -40°C | +100°C |

Note!

- [1] Please refer to [UG982, GW5A-138 Pinout](#) for the supply voltage information of the devices in different packages.
- [2] When the V_{CC_REG} voltage is higher, the power consumption is higher.

3.1.3 Power Supply Ramp Rates

Table 3-5 Power Supply Ramp Rates

| Name | Description | Min. | Typ. | Max. |
|-------------------------|-------------------------|-----------|------|---------|
| V _{CC} Ramp | Power supply ramp rates | 0.02mV/μs | TBD | 50mV/μs |

3.1.4 Hot Socket Specifications

Table 3-6 Hot Socket Specifications

| Name | Description | Condition | I/O | Max. |
|----------|-----------------------|-----------------------|----------------------|-------|
| I_{HS} | Input leakage current | $V_{IN}=V_{IL}$ (MAX) | I/O | 150uA |
| I_{HS} | Input leakage current | $V_{IN}=V_{IL}$ (MAX) | TDI, TDO TMS, TCK | 120uA |

3.1.5 POR Specifications

Table 3-7 POR Parameters

| Name | Description | Device | Name | Typ. |
|-------------|------------------------|----------|---------------------|-------|
| POR Voltage | Power on reset voltage | GW5A-138 | V_{CC} | 0.72V |
| | | | V_{CCX} | 1.5V |
| | | | V_{CCIO} (Bank10) | 1.04V |

3.2 ESD performance

Table 3-8 GW5A ESD - HBM

| Device | HBM |
|----------|------------------------|
| GW5A-25 | HBM $\geq 1000V^{[1]}$ |
| GW5A-138 | HBM $\geq 1000V$ |

Note!

1000V is the expected ESD performance.

Table 3-9 GW5A ESD - CDM

| Device | GW5A-25 |
|----------|-----------------|
| GW5A-25 | CDM $\geq 500V$ |
| GW5A-138 | CDM $\geq 250V$ |

3.3 DC Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 3-10 DC Electrical Characteristics over Recommended Operating Conditions

| Name | Description | Condition | Min. | Typ. | Max. |
|------------------|---------------------------------------|--|------|-------|--------|
| I_{IL}, I_{IH} | Input or I/O leakage | $V_{CCO} < V_{IN} < V_{IH}(\text{MAX})$ | - | - | 210uA |
| | | $0V < V_{IN} < V_{CCO}$ | - | - | 10uA |
| I_{PU} | I/O Active Pull-up Current | $0 < V_{IN} < 0.7V_{CCO}$, Pull Strength=Strong | - | - | -400uA |
| | | $0 < V_{IN} < 0.7V_{CCO}$, Pull Strength=Medium | - | - | -150uA |
| | | $0 < V_{IN} < 0.7V_{CCO}$, Pull Strength=Weak | - | - | -50uA |
| I_{PD} | I/O Active Pull-down Current | $V_{IL}(\text{MAX}) < V_{IN} < V_{CCO}$, Pull Strength=Strong | - | - | 400uA |
| | | $V_{IL}(\text{MAX}) < V_{IN} < V_{CCO}$, Pull Strength=Medium | - | - | 150uA |
| | | $V_{IL}(\text{MAX}) < V_{IN} < V_{CCO}$, Pull Strength=Weak | - | - | 50uA |
| C1 | I/O Capacitance | | | 5pF | 8pF |
| V_{HYST} | Hysteresis for Schmitt Trigger inputs | $V_{CCO}=3.3V$, Hysteresis=ON | - | 400mV | - |
| | | $V_{CCO}=2.5V$, Hysteresis=ON | - | 250mV | - |
| | | $V_{CCO}=1.8V$, Hysteresis=ON | - | 150mV | - |
| | | $V_{CCO}=1.5V$, Hysteresis=ON | - | 130mV | - |
| | | $V_{CCO}=1.2V$, Hysteresis=ON | - | 40mV | - |

3.3.2 Static Current

Table 3-11 Static Current

| Name | Description | LV/UV | Device | Typ. ^[1] |
|---------------------|---|------------|----------|---------------------|
| I _{CC} | Core Current | LV version | GW5A-138 | 100 mA |
| I _{CCX} | V _{CCX} current (V _{CCX} =2.5V) | LV version | GW5A-138 | 9 mA |
| I _{CCIO} | I/O Bank current (V _{CCIO} =3.3V) | LV version | GW5A-138 | 5 mA |
| I _{CC_REG} | Built-in regulator static current | LV version | GW5A-138 | 6 mA |

Note!

[1] Typical values are tested at 25°C.

3.3.3 Recommended I/O Operating Conditions

Table 3-12 I/O Operating Conditions Recommended

| Name | Output V _{CCIO} (V) | | | Input V _{REF} (V) | | |
|----------------------|------------------------------|------|-------|----------------------------|------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVTTL33 | 3.135 | 3.3 | 3.465 | - | - | - |
| LVC MOS33 | 3.135 | 3.3 | 3.465 | - | - | - |
| LVC MOS25 | 2.375 | 2.5 | 2.625 | - | - | - |
| LVC MOS18 | 1.71 | 1.8 | 1.89 | - | - | - |
| LVC MOS15 | 1.425 | 1.5 | 1.575 | - | - | - |
| LVC MOS12 | 1.14 | 1.2 | 1.26 | - | - | - |
| SSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| SSTL18_I | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL18_II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25_I | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL25_II | 2.375 | 2.5 | 2.645 | 1.15 | 1.25 | 1.35 |
| SSTL33_I | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| SSTL33_II | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL18_I | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL18_II | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| HSTL15 | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| PCI33 | 3.135 | 3.3 | 3.465 | - | - | - |
| LVPECL33E | 3.135 | 3.3 | 3.465 | - | - | - |
| MLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| BLVDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| RSDS25E | 2.375 | 2.5 | 2.625 | - | - | - |
| LVDS25E ¹ | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL15D | 1.425 | 1.5 | 1.575 | - | - | - |

| Name | Output V_{CCIO} (V) | | | Input V_{REF} (V) | | |
|------------|-----------------------|-------|-------|---------------------|------|------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| SSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |
| SSTL25D_I | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL25D_II | 2.375 | 2.5 | 2.625 | - | - | - |
| SSTL33D_I | 3.135 | 3.3 | 3.465 | - | - | - |
| SSTL33D_II | 3.135 | 3.3 | 3.465 | - | - | - |
| HSTL15D | 1.425 | 1.575 | 1.89 | - | - | - |
| HSTL18D_I | 1.71 | 1.8 | 1.89 | - | - | - |
| HSTL18D_II | 1.71 | 1.8 | 1.89 | - | - | - |

Note!

V_{CCIO} of Banks with True LVDS is recommended to be set to 2.5 V.

3.3.4 Single-ended I/O DC Characteristics

Table 3-13 Single-ended DC Characteristics

| Name | V_{IL} | | V_{IH} | | V_{OL} (Max) | V_{OH} (Min) | $I_{OL}^{[1]}$ (mA) | $I_{OH}^{[1]}$ (mA) |
|----------------------|----------|-----------------------|-----------------------|---------------|-------------------|-------------------|------------------------|------------------------|
| | Min | Max | Min | Max | | | | |
| LVCMOS33 LVTTTL33 | -0.3V | 0.8V | 2.0V | 3.45V | 0.4V | $V_{CCO}-0.4V$ | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | 0.2V | $V_{CCO}-0.2V$ | 0.1 | -0.1 |
| LVCMOS25 | -0.3V | 0.7V | 1.7V | $V_{CCO}+0.3$ | 0.4V | $V_{CCO}-0.4V$ | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | 0.2V | $V_{CCO}-0.2V$ | 0.1 | -0.1 |
| LVCMOS18 | -0.3V | $0.35 \times V_{CCO}$ | $0.65 \times V_{CCO}$ | $V_{CCO}+0.3$ | 0.4V | $V_{CCO}-0.4V$ | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | | | 12 | -12 |
| | | | | | | | 16 | -16 |
| | | | | | 0.2V | $V_{CCO}-0.2V$ | 0.1 | -0.1 |
| LVCMOS15 | -0.3V | $0.35 \times V_{CCO}$ | $0.65 \times V_{CCO}$ | $V_{CCO}+0.3$ | 0.4V | $V_{CCO}-0.4V$ | 4 | -4 |
| | | | | | | | 8 | -8 |
| | | | | | 0.2V | $V_{CCO}-0.2V$ | 12 | -12 |
| | | | | | | | 0.1 | -0.1 |
| LVCMOS12 | -0.3V | $0.35 \times V_{CCO}$ | $0.65 \times V_{CCO}$ | $V_{CCO}+0.3$ | 0.4V | $V_{CCO}-0.4V$ | 4 | -4 |
| | | | | | | | 8 | -8 |

| Name | V _{IL} | | V _{IH} | | V _{OL} (Max) | V _{OH} (Min) | I _{OL} ^[1] (mA) | I _{OH} ^[1] (mA) |
|-----------|-----------------|--------------------------|--------------------------|---------------------------|-------------------------------|-------------------------------|--|--|
| | Min | Max | Min | Max | | | | |
| | | | | | 0.2V | V _{CCO} -0.2V | 0.1 | -0.1 |
| LVC MOS10 | -0.3 | 0.35 x V _{CCO} | 0.65 x V _{CCO} | 1.1V | 0.4V | V _{CCO} -0.4V | 2 | -2 |
| PCI33 | -0.3V | 0.3 x V _{CCO} | 0.5 x V _{CCO} | V _{CCO} + 0.3 | 0.1x V _{CCO} | 0.9 x V _{CCO} | 1.5 | -0.5 |
| SSTL33_I | -0.3V | V _{REF} -0.2V | V _{REF} +0.2V | V _{CCO} + 0.3 | V _{CCO} /2- 0.6 | V _{CCO} /2+0.6 | 8 | -8 |
| SSTL33_II | -0.3V | V _{REF} -0.2V | V _{REF} +0.2V | V _{CCO} + 0.3 | V _{CCO} /2- 0.8 | V _{CCO} /2+0.8 | 13.4 | -13.4 |
| SSTL25_I | -0.3V | V _{REF} -0.15V | V _{REF} +0.15V | V _{CCO} + 0.3 | V _{CCO} /2- 0.61 | V _{CCO} /2+0.6 1 | 8 | -8 |
| SSTL25_II | -0.3V | V _{REF} -0.15V | V _{REF} +0.15V | V _{CCO} + 0.3 | V _{CCO} /2- 0.81 | V _{CCO} /2+0.8 1 | 13.4 | -13.4 |
| SSTL18_I | -0.3V | V _{REF} -0.125V | V _{REF} +0.125V | V _{CCO} + 0.3 | V _{CCO} /2- 0.47 | V _{CCO} /2+0.4 7 | 8 | -8 |
| SSTL18_II | -0.3V | V _{REF} -0.125V | V _{REF} +0.125V | V _{CCO} + 0.3 | V _{CCO} /2- 0.6 | V _{CCO} /2+0.6 | 13.4 | -13.4 |
| SSTL15 | -0.3V | V _{REF} -0.1V | V _{REF} + 0.1V | V _{CCO} + 0.3 | V _{CCO} /2- 0.175 | V _{CCO} /2+0.1 75 | 8 | -8 |
| SSTL135 | -0.3 | V _{REF} -0.09V | V _{REF} +0.09V | V _{CCO} + 0.3 | V _{CCO} /2- 0.15 | V _{CCO} /2+0.1 5 | 8 | -8 |
| SSTL12 | -0.3 | V _{REF} -0.1V | V _{REF} +0.1V | V _{CCO} + 0.3 | 0.2 x V _{CCO} | 0.8 x V _{CCO} | 0.1 | -0.1 |
| HSTL18_I | -0.3V | V _{REF} -0.1V | V _{REF} + 0.1V | V _{CCO} + 0.3 | 0.40V | V _{CCO} -0.40V | 8 | -8 |
| HSTL18_II | -0.3V | V _{REF} -0.1V | V _{REF} + 0.1V | V _{CCO} + 0.3 | 0.40V | V _{CCO} -0.40V | 16 | -16 |
| HSTL15_I | -0.3V | V _{REF} -0.1V | V _{REF} + 0.1V | V _{CCO} + 0.3 | 0.40V | V _{CCO} -0.40V | 8 | -8 |
| HSTL12_I | -0.3V | V _{REF} -0.1V | V _{REF} + 0.1V | V _{CCO} + 0.3 | 0.2 x V _{CCO} | 0.8 x V _{CCO} | 8 | -8 |
| HSUL12 | -0.3 | V _{REF} -0.13V | V _{REF} + 0.13V | V _{CCO} + 0.3 | 0.2 x V _{CCO} | 0.8 x V _{CCO} | 0.1 | -0.1 |

Note!

[1] The total DC current limit (sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

3.3.5 Differential I/O DC Characteristic

Table 3-14 Differential I/O DC Characteristic

| Name | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------|------------------------------------|---|-----------|-----------|-----------|---------|
| V_{INA}, V_{INB} | Input Voltage | TBD | 0 | | 2.4 | V |
| V_{CM} | Input Common Mode Voltage | Half the Sum of the Two Inputs | 0.3 | | 2.35 | V |
| V_{THD} | Differential Input Threshold | Difference Between the Two Inputs | ± 100 | ± 350 | ± 600 | mV |
| I_{IN} | Input Current | Power On or Power Off | | | 20 | μA |
| V_{OH} | Output High Voltage for VOP or VOM | $R_T = 100 \Omega$ | | | 1.675 | V |
| V_{OL} | Output High Voltage for VOP or VOM | $R_T = 100 \Omega$ | 0.7 | | | V |
| V_{OD} | Output Voltage Differential | $(V_{OP} - V_{OM}), R_T = 100 \Omega$ | 180 | 350 | 440 | mV |
| ΔV_{OD} | Change in VOD Between High and Low | TBD | | | 50 | mV |
| V_{OS} | Output Voltage Offset | $(V_{OP} + V_{OM})/2, R_T = 100 \Omega$ | 1.000 | 1.250 | 1.425 | V |
| ΔV_{OS} | Change in VOS Between High and Low | TBD | | | 50 | mV |
| I_S | Short-circuit current | $V_{OD} = 0V$ two outputs shorted | | | 12 | mA |

3.4 AC Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-15 CFU Timing Parameters

| Name | Description | Speed Grade | | Unit |
|-----------------|------------------------------|-------------|-----|------|
| | | Min | Max | |
| t_{LUT4_CFU} | LUT4 delay | - | - | ns |
| t_{SR_CFU} | Set/Reset to Register output | - | - | ns |
| t_{CO_CFU} | Clock to Register output | - | - | ns |

3.4.2 BSRAM Switching Characteristics

Table 3-16 BSRAM Timing Parameters

| Name | Description | Speed Grade | | Unit |
|-------------------|--|-------------|-----|------|
| | | Min | Max | |
| t_{COAD_BSRAM} | Clock to output from read address/data | - | - | ns |
| t_{COOR_BSRAM} | Clock to output from output register | - | - | ns |

3.4.3 DSP Switching Characteristics

Table 3-17 DSP Timing Parameters

| Name | Description | Speed Grade | | Unit |
|-----------------------|--|-------------|-----|------|
| | | Min | Max | |
| t _{COIR_DSP} | Clock to output from input register | - | - | ns |
| t _{COPR_DSP} | Clock to output from Pipeline register | - | - | ns |
| t _{COOR_DSP} | Clock to output from output register | - | - | ns |

3.4.4 Clock and I/O Switching Characteristic

Table 3-18 External Switching Characteristics

| Name | Description | Device | -8 | | -7 | | Unit |
|----------------------------------|------------------------------|----------|-----|-----|-----|-----|------|
| | | | Min | Max | Min | Max | |
| Pin-LUT-Pin Delay ⁽¹⁾ | Pin(IOxA) to Pin(IOxB) delay | GW5A-138 | - | - | - | - | ns |
| T _{HCLKdly} | HCLK tree delay | GW5A-138 | - | - | - | - | ns |
| T _{GCLKdly} | GCLK tree delay | GW5A-138 | - | - | - | - | ns |

3.4.5 On chip Oscillator Switching Characteristics

Table 3-19 On chip Oscillator Switching Characteristics

| Device | Name | Description | Min. | Typ. | Max. |
|--------------------|--------------------|-----------------------------------|-----------|--------|----------|
| GW5A-25 / GW5A-138 | f _{MAX} | Output Frequency (0 to + 85° C) | 199.5 MHz | 210MHz | 220.5MHz |
| | | Output Frequency (-40 to +100° C) | 189 MHz | 210MHz | 231MHz |
| | t _{DT} | Output Clock Duty Cycle | - | 50% | - |
| | t _{OPJIT} | Output Clock Period Jitter | TBD | TBD | TBD |

3.4.6 PLL Switching Characteristics

Table 3-20 PLL Switching Characteristic

| Device | Name | Min. | Max. |
|----------|--------|------------------------|---------|
| GW5A-25 | CLKIN | 19MHz | 800MHz |
| | PFD | 19MHz | 400MHz |
| | VCO | 800MHz | 1600MHz |
| | CLKOUT | 6.25MHz ^[1] | 1600MHz |
| GW5A-138 | CLKIN | 10MHz | 400MHz |
| | PFD | 10MHz | 400MHz |
| | VCO | 800MHz | 2GHz |
| | CLKOUT | 6.25MHz ^[1] | 1GHz |

Note!

6.25MHz is the minimum frequency of CLKOUT in non-cascade mode.

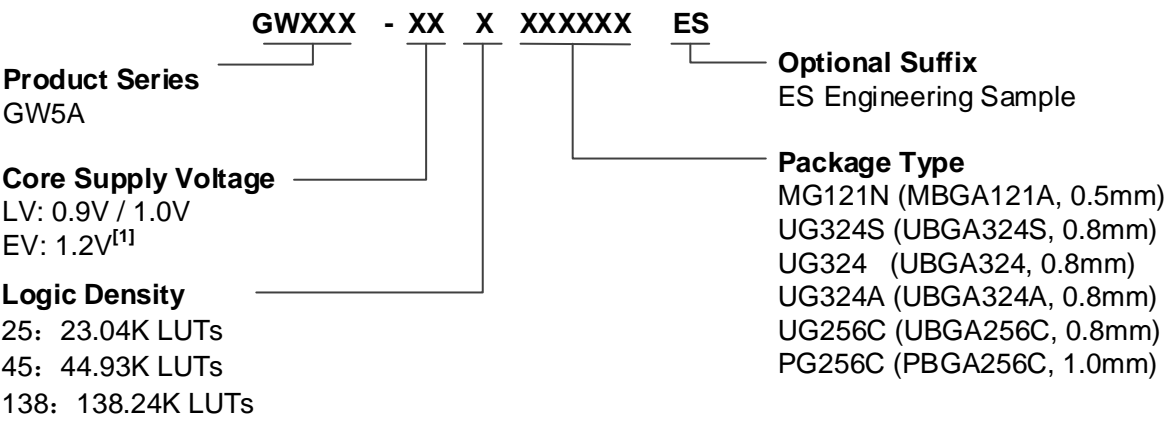
3.5 Configuration Interface Timing Specification

The GW5A series of FPGA Products support multiple GowinCONFIG modes: SSPI, MSPI, SERIAL, and CPU. For more detailed information, please refer to [UG704, Arora V FPGA Products Programming and Configuration Guide](#).

4Ordering Information

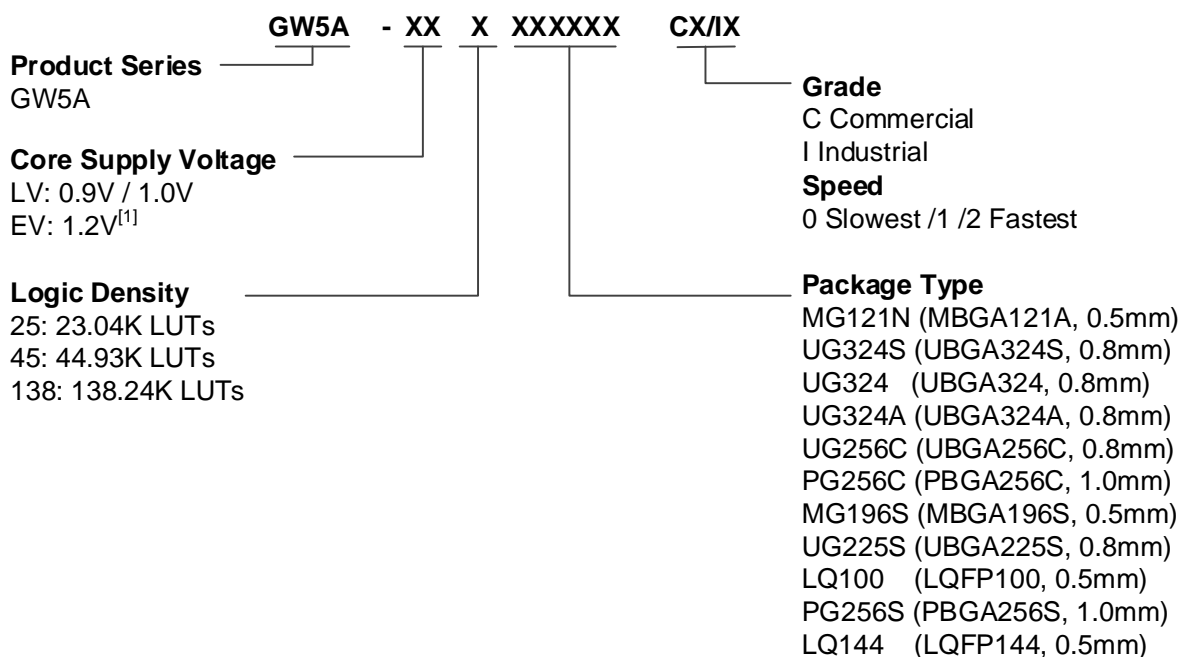
4.1 Part Name

Figure 4-1 Part Naming Examples-ES



Note!
[1] Currently, GW5A-25 of the GW5A series devices supports the EV version.

Figure 4-2 Part Naming Examples-Production

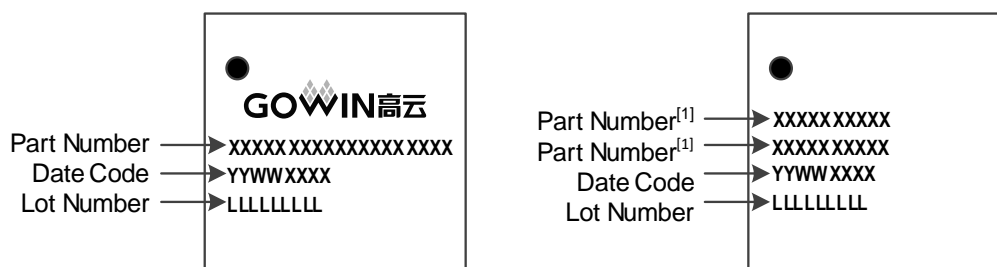
**Note!**

- [1] Currently, GW5A-25 of the GW5A series devices supports the EV version.
- For the further detailed information about the package information, please refer to 1.2 Product Resources.
- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in GOWIN part name marking for one device, such as C2/I1, C1/I0, etc. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100, and the maximum temperature of the commercial grade is 85. Therefore, if the same chip meets the speed grade 2 in the commercial grade application, the speed grade is 1 in the industrial grade application.

4.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 4-3.

Figure 4-3 Package Mark Examples

**Note!**

[1] The first two lines in the right figure above are the “Part Number”.

5 About This Guide

5.1 Purpose

This data sheet describes the features, product resources, structure, AC/DC characteristics, and the ordering information of the GW5A series of FPGA products, making it easier to understand the GW5A series of FPGA products and select and use our devices.

5.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [UG704, Arora V 138K FPGA Products Programming and Configuration User Guide](#)
- [UG983, GW5A series of FPGA Products Package and Pinout Manual](#)
- [UG985, GW5A-25 Pinout](#)
- [UG988, GW5A-138 Pinout](#)
- [UG984, Arora V FPGA Products Schematic Manual](#)

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

| Terminology and Abbreviations | Full Name |
|-------------------------------|--|
| ADC | Analog to Digital Converter |
| AER | Advanced Error Reporting |
| ALU | Arithmetic Logic Unit |
| BSRAM | Block Static Random Access Memory |
| CFU | Configurable Function Unit |
| CLS | Configurable Logic Section |
| CMSE | Configuration Memory Soft Error Recovery |
| CRU | Configurable Routing Unit |

| Terminology and Abbreviations | Full Name |
|-------------------------------|-------------------------------------|
| CSI | Camera Serial Interface |
| CTC | Clock Tolerance Compensation |
| CTLE | Continuous Time Linear Equalizer |
| DCS | Dynamic Clock Selector |
| DFF | D Flip-flop |
| DNA | Device Identifier |
| DP | True Dual Port 16K BSRAM |
| DSI | Display Serial Interface |
| DSP | Digital Signal Processing |
| ECC | Error Correction Code |
| ECRC | End-to-End Cyclic Redundancy Check |
| ESD | Electro-Static Discharge |
| FIFO | First In First Out |
| FPG | FCPBGA |
| FPGAs | Field Programmable Gate Array |
| GCLK | Global Clock |
| GPIO | Gowin Programmable IO |
| GSR | Global Set/Reset |
| HCLK | High Speed Clock |
| IOB | Input/Output Block |
| LUT | Look-up Table |
| LW | Long Wire |
| MIPI | Mobile Industry Processor Interface |
| OTP | One Time Programmable |
| PLL | Phase-locked Loop |
| REG | Register |
| SDP | Semi Dual Port 16K BSRAM |
| SP | Single Port 16K BSRAM |
| SSRAM | Shadow Static Random Access Memory |
| TDM | Time Division Multiplexing |

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Preliminary

