GOWIN
PROGRAMMING FOR THE FUTURE

GW1N Series of FPGA Products

Data Sheet

DS100-2.9.8E, 04/27/2023

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Revision History

Date	Version	Description
06/08/2018	1.19E	Initial version published.
07/31/2018	1.2E	● PLL Structure diagram updated; ● User Flash timing parameters added; ● The description of systemIO status for blank chips added.
09/12/2018	1.3E	The UG256 package added.
12/10/2018	1.4E	● The BANK0 and BANK2 of GW1N-6 and GW1N-9 support I3C OpenDrain/PushPull conversion; ● Change the step delay of IODELAY from 25ps to 30 ps.
01/09/2019	1.5E	Oscillator frequency updated.
02/14/2019	1.6E	● Power supply for UV devices updated; ● Recommended Operating Conditions for UV devices updated; ● Part naming figures updated.
06/04/2019	1.7E	● Operating temperature changed to Junction temperature; ● GW1N-1S added; ● Power supply restrictions of BANK0/1/3 in GW1N-6/9 added; ● Description of User Flash in GW1N-2/2B/4/4B/6/9 added; ● GW1N-6/9 EQ144 added.
07/08/2019	1.8E	● GW1N-6/9 MG196, UG169, and EQ176 added; ● GW1N-1S CS30 added.
10/10/2019	1.9E	● Packages of GW1N-1 LQ100X-LV and LQ100X-UV added; ● GW1N-1S BSRAM does not support Dual port mode; ● The package size of LQ100 / LQ144 / EQ144 / LQ176 / EQ176 fixed; ● Junction temperature of automotive operation added; ● Power supply ramp rates updated.
11/15/2019	2.0E	● The number of Max. I/O updated; ● Automotive grade description added in 5.1 Part Name; ● IODELAY description added.
01/02/2020	2.1E	● The package name of LQ100X-LV and LQ100X-UV updated; ● GW1N-4 MG132X added; ● CLU description updated.
03/17/2020	2.2E	● GW1N-9 CS81M added; ● The description of PLL CLKIN frequency updated.
04/09/220	2.3E	● GW1N-2/GW1N-2B/GW1N-6 removed; ● CFU view updated;
05/28/2020	2.3.1E	Further description of “C” and “I” in the part name marking added.
09/30/2020	2.4E	● GW1N-2 added; ● GW1N-9 MG100 added; ● GW1N-9 QN48F added.
01/13/2021	2.4.1E	I/O Input/Output type updated.
01/22/2021	2.4.2E	GW1N-2 QN48 and QN48M added.
02/08/2021	2.4.3E	AC/DC parameters added.
03/02/2021	2.4.4E	GW1N-2 MG132 added.
04/20/202	2.5E	GW1N-1P5 added.
05/28/2021	2.6E	● GW1N-1P5 LQ100 added; ● GW1N-2 MG132/LQ100/LQ144 added, and MG132 renamed to MG132H, QN48M renamed to QN48H. ● GW1N-9 MG100T added; ● GW1N-1 LQ100X removed; ● “Table 2-3 Configuration Modes Supported by Different Packages”

Date	Version	Description
		added.
06/25/2021	2.6.1E	● One note on the “RECONFIG_N” pin added; ● Part naming figures updated.
07/16/2021	2.6.2E	● GW1N-2 MG121/MG121X added; ● The description of User Flash inproved.
10/28/2021	2.6.3E	● GW1N-1 QN32/QN48/LQ100/LQ144 removed; ● GW1N-2 MG49 and GW1N-1P5 FN48X added; ● The recommended working range of V_{CC}/V_{CCIO}/V_{CCX} modified.
01/20/2022	2.6.4E	● GW1N-2/GW1N-1P5 C5/I4 devices added; ● Static current and Programming current improved; ● I/O Logic Input and output view updated and port description added; ● GW1N-2 QN32X, QN88, and CS42H added; ● GW1N-1P5 FN48X removed; GW1N-1P5 QN48X added.
03/11/2022	2.6.5E	The static current of GW1N-1P5 and GW1N-2 device updated.
05/20/2022	2.7E	● GW1N-4 UG169 added. ● GW1N-2 CS42H updated. ● The output drive strength of MIPI IO updated. ● Recommended I/O operating conditions updated. ● On chip oscillator output frequency updated. ● Gearbox internal timing parameters updated.
06/02/2022	2.7.1E	GW1N-1 QN32/QN48/LQ100/LQ144 added.
06/23/2022	2.7.2E	GW1N-1 CS30/FN32 removed.
07/01/2022	2.7.3E	GW1N-1 CS30 added.
07/21/2022	2.8E	● GW1N-2 QN32 added； ● GW1N-2 CS100H added； ● GW1N-2 LQ144F added； ● The maximum value of the differential input threshold V_{THD} updated. ● Note about loading frequency for the GW1N-2 device added; ● Description of configuration modes supported by GW1N-1 CS30 added; ● GW1N-1S CS30/FN32 removed.
08/18/2022	2.8.1E	GW1N-1 QN32/QN48/LQ100/LQ144 removed.
09/29/2022	2.9E	● Note about DC current limit added. ● Table 4-2 Recommended Operating Conditions updated. ● Note about Vcc of GW1N-4/GW1N-9 UV version devices added. ● Architecture overviews of GW1N series of FPGA products updated. ● Table 4-5 POR Voltage updated. ● Table 4-9 Static Current updated. ● Section 4.4 Switching Characteristics updated.
11/11/2022	2.9.1E	● Table 4-3 Power Supply Ramp Rate updated. ● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Description of configuration Flash added. ● Note about byte-enable added.
11/21/2022	2.9.2E	● Table 4-1 Absolute Max. Ratings updated. ● Table 4-9 Static Current updated. ● Description of the background upgrade feature in section 3.12 Programming Configuration updated.

Date	Version	Description
12/08/2022	2.9.3E	● Table 4-1 Absolute Max. Ratings updated. ● Table 4-22 GW1N-1/ GW1N-1S User Flash DC Characteristics updated. ● Table 4-23 GW1N-2/4/9 User Flash DC Characteristics(I) added. ● Table 4-24 GW1N-2/4/9 User Flash DC Characteristics(II)[4] updated. ● Note for Table 3-4 Memory Size Configuration revised.
12/19/2022	2.9.4E	GW1N-1P5 QN48XF added.
01/12/2023	2.9.5E	● Table 2-2 Package Information and Max. User I/O, True LVDS Pairs updated. ● Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions updated.
02/22/2023	2.9.6E	● Information on Slew Rate removed. ● Table 4-26 GW1N-1P5/2/4/9 User Flash Timing Parameters updated. ● Description added to 3.5 User Flash (GW1N-1 and GW1N-1S) and 3.6 User Flash (GW1N-1P5/2/4/9). ● Description of true LVDS design modified.
04/13/2023	2.9.7E	● Note about the default state of GPIO modified. ● Note for Figure 3-5 CFU View modified. ● Table 4-3 Power Supply Ramp Rates updated. ● The I/O logic output diagram and the I/O logic input diagram combined into Figure 3-13 I/O Logic Input and Output. ● Description of MIPI input/output updated.
04/27/2023	2.9.8E	● Description of Flash resources updated. ● Note for Table 3-4 Memory Size Configuration modified. ● Description of the V_{CCIO} power supply restrictions of the GW1N-9 device updated.

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1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1N series of FPGA products. It is designed to help you to understand the GW1N series of FPGA products quickly and select and use devices appropriately.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG103, GW1N series of FPGA Products Package and Pinout
- UG107, GW1N-1 Pinout
- UG167, GW1N-1S Pinout
- UG171, GW1N-2 Pinout
- UG105, GW1N-4 Pinout
- UG114, GW1N-9 Pinout
- UG174, GW1N-1P5 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section

Abbreviations and Terminology	Name
CRU	Configurable Routing Unit
CS	WLCSP
CSI	Camera Serial Interface
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
DSI	Display Serial Interface
DSP	Digital Signal Processing
FF	Flip-Flop
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable I/O
IOB	Input/Output Block
LQ	LQFP
LUT4	4-input Look-up Table
LUT5	5-input Look-up Table
LUT6	6-input Look-up Table
LUT7	7-input Look-up Table
LUT8	8-input Look-up Table
MG	MBGA
MIPI	Mobile Industry Processor Interface
PG	PBGA
PLL	Phase-locked Loop
QN	QFN
REG	Register
SDP	Semi Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
UG	UBGA

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 General Description

The GW1N series of FPGA products are the first generation products in the LittleBee® family. They offer abundant logic resources, multiple I/O standards, embedded BSRAM, DSP, PLL, and built-in Flash. They are non-volatile FPGA products with low power, instant-start, low-cost, high-security, small size, various packages, and flexible usage.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1N series of FPGA products and applies to FPGA synthesizing, placement and routing, data bitstream generation and download, etc.

2.1 Features

- Lower power consumption
  - 55nm embedded flash technology
  - LV [1]: Supports 1.2 V core voltage
  - UV: Supports unique power supply for V_{CC}/ V_{CCIO}/ V_{CCx}

    Note!

    [1] GW1N-1S supports LV Version only.
  - Clock dynamically turns on and off
- User Flash (GW1N-1, GW1N-1S)
  - NOR Flash
  - 100,000 write cycles
  - Greater than10 years data retention at +85℃
  - Selectable 8/16/32 bits data-in and data-out
  - Page size: 256 bytes
  - 3 μA standby current
  - Page write time: 8.2 ms
- User Flash (GW1N-1P5/2/4/9)
  - NOR Flash
  - 10,000 write cycles

  - Greater than10 years Data Retention at +85℃
  - Data Width: 32
  - GW1N-1P5/2 capacity: 48 rows x 64 columns x 32 = 96K bits
  - GW1N-4 capacity: 128 rows x 64 columns x 32 = 256K bits
  - GW1N-9 capacity: 304 rows x 64 columns x 32 = 608 K bits
  - Page Erase Capability: 2,048 bytes per page
  - Word Programming Time: ≤16 μs
  - Page Erasure Time: ≤120 ms
- Configuration Flash (GW1N-1, GW1N-1S)
  - NOR Flash
  - 100,000 write cycles
  - Greater than10 years data retention at +85℃
- Configuration Flash (GW1N-1P5/2/4/9)
  - NOR Flash
  - 10,000 write cycles
  - Greater than10 years Data Retention at +85℃
- Hard Core - MIPI D-PHY RX (GW1N-2)
  - Interfaces to MIPI DSI and MIPI CSI-2, RX devices
  - IO Bank6 in CS42, CS42H, QN48H, QN88, and MG132H packages supports MIPI D-PHY RX
  - MIPI transmission rate up to 2Gbps per lane, 8Gbps per D-PHY interface;
  - Supports up to 4 data lanes and one clock lane
- GPIO - MIPI D-PHY RX/TX
  - Interfaces to MIPI CSI-2 and MIPI DSI, RX and TX devices
  - MIPI transmission rate up to 1.2Gbps per lane
  - Bank0/Bank1 of GW1N-1S support MIPI IO input
  - Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 support MIPI IO output(with dynamic ODT)
  - Bank2 of GW1N-2/GW1N-1P5 supports MIPI IO input(with dynamic ODT)
  - Bank0 of GW1N-9 supports MIPI IO input(with dynamic ODT)
  - The Bottom layer of GW1N-9 supports MIPI IO output
  - The Top layer and Bottom layer of GW1N-9 support I3C OpenDrain/PushPull conversion
- Multiple I/O Standards
  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE

    MLVDSE, LVPECLE, RSDSE

  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA, etc. drive options
  - Individual bus keeper, weak pull-up, weak pull-down, and open drain option
  - Hot socket
- High performance DSP(GW1N-4/9)
  - High performance digital signal processing ability
  - Supports 9 x 9,18 x 18,36 x 36 bits multiplier and 54 bits accumulator;
  - Multipliers cascading
  - Registers pipeline and bypass
  - Adaptive filtering through signal feedback
  - Supports barrel shifter
- Abundant slices
  - Four input LUT (LUT4)
  - Supports shift register and distributed register
- Block SRAM with multiple modes
  - Supports dual port, single port, and semi-dual port
  - Supports bytes write enable
- Flexible PLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Supports background update
  - Offers up to seven GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT, I^2C Slave

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9	GW1N-1S
LUT4	1,152	1584	2304	4,608	8,640	1,152
Flip-Flop (FF)	864	1584	2016	3,456	6,480	864
Shadow SRAM Capacity (bits)	0	12672	18432	0	17,280	0
Block SRAM Capacity(bits)	72 K	72K	72K	180 K	468 K	72K
Number of BSRAM	4	4	4	10	26	4
User Flash (bits)	96 K	96K	96K	256 K	608 K	96K
18 x 18 Multiplier	0	0	0	16	20	0
PLLs	1	1	1	2	2	1
Total number of I/O banks	4	6	6[2]	4	4	3
Max. I/O	120	125	125	218	276	44
Core Voltage (LV)	1.2 V	1.2V	1.2V	1.2 V	1.2 V	1.2V
Core Voltage (UV)	1.8V/2.5V/3.3V[1]	1.8V/2.5V/3.3V		1.8V[3]/2.5V/3.3V		–

Note!

- [1] In GW1N-1 series, only package in LQ100X offers both UV and LV version, other packages in GW1N-1 series only offer LV version at present.
- [2] In GW1N-2 seires, the package in CS42/QN48H/MG132H/QN88/CS42H has seven IO banks.
- [3] For GW1N-4/GW1N-9 UV version devices, if V_{CC} and Vccx share a pin in a package, the Vccx range (2.5V~3.3V) of GW1N-4/GW1N-9 will limit the Vcc range to 2.5 V~3.3V, in this case Vcc does not support 1.8V.

2.3 Package Information

Table 2-2 Package Information and Max. User I/O, True LVDS Pairs

Package	Pitch(mm)	Size(mm)	GW1N-1S	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
CS30	0.4	2.3 x 2.4	-	24	-	-	-	-
QN32	0.5	5 x 5	-	-	-	21 (1)	24 (3)	-
QN32X	0.5	5 x 5	-	-	-	21 (1)	-	-
FN32	0.4	4 x 4	-	-	-		-	-
CS42	0.4	2.4 x 2.9	-	-	-	24 (7)	-	-
CS42H	0.4	2.4 x 2.9	-	-	-	36(3)	-	-
QN48	0.4	6 x 6	-	-	-	40(12)	40 (9)	40(12)
QN48H	0.4	6 x 6	-	-	-	30(8)	-	-
QN48F	0.4	6 x 6	-		-			39(11)
QN48X	0.5	7 x 7	-	-	39(10)	-	-	-
QN48XF	0.5	7 x 7	-	-	40(11)	-	-	-
CM64	0.5	4.1 x 4.1	-	-	-		-	55(16)
CS72	0.4	3.6 x 3.3	-		-		57 (19)	-
CS81M	0.4	4.1 x 4.1	-	-	-		-	55(15)
QN88	0.4	10 x 10	-	-	-	57(17)	70 (11)	70(19)
CS100H	0.4	4 x 4	-	-	-	88(27)	-	-
LQ100	0.5	14 x 14	-	-	80(16)	80(15)	79 (13)	79(20)
LQ100X	0.5	14 x 14	-	-	80(15)	80(15)	-	-
LQ144	0.5	20 x 20	-	-	-	113(28)	119 (22)	120(28)
LQ144X	0.5	20 x 20	-	-	-	113(28)	-	-
LQ144F	0.5	20 x 20	-	-	-	115(27)	-	-
EQ144	0.5	20 x 20	-	-	-	-	-	120(28)
MG49	0.5	3.8 x 3.8	-	-	-	42(11)	-	-
MG100	0.5	5 x 5	-	-	-	-	-	87(25)
MG100T	0.5	5 x 5	-	-	-	-	-	87(17)
MG121	0.5	6 x 6	-	-	-	100(28)	-	-
MG121X	0.5	6 x 6	-	-	-	100(28)	-	-
MG132	0.5	8 x 8	-	-	-	104(29)		
MG132H	0.5	8 x 8				94(29)		
MG132X	0.5	8 x 8	-	-	-	104 (29)	105(23)	-
MG160	0.5	8 x 8	-	-	-	-	131 (25)	131(38)

Package	Pitch(mm)	Size(mm)	GW1N-1S	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
UG169	0.8	11 x 11	-	-	-	-	129(27)	129(38)
LQ176	0.4	20 x 20	-	-	-	-	-	147(37)
EQ176	0.4	20 x 20	-	-	-	-	-	147(37)
MG196	0.5	8 x 8	-	-	-	-	-	113(35)
PG256	1.0	17 x 17	-	-	-	-	207(32)	207(36)
PG256M	1.0	17 x 17	-	-	-	-	207(32)	-
UG256	0.8	14 x 14	-	-	-	-	-	207(36)
UG332	0.8	17 x 17	-	-	-	-	-	273(43)

Note!

- JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O is increased by one. See *UG103, GW1N series of FPGA Products Package and Pinout* for further details.
- The package types in this data sheet are written with abbreviations. See 5.1Part Name.
- GW1N-1 CS30 only supports SSPI mode.

Table 2-3 Configuration Modes Supported by Different Packages

Device	Package	Mode[2:0]	Configuration Mode	Notes
GW1N-2[1]	QN32 CS42 LQ100 LQ144 LQ144F MG121 MG132	000	JTAG Autoboot	-
	LQ100X LQ144X MG121X MG132X MG49 QN32X CS42H	100	JTAG I^2C Autoboot	When I^2C is supported, the SDA and SCL pins need to be external pulled up; when Mode[2,0] is configured as 100 and Autoboot is used, SDA pin needs to be external pulled up.
	QN48 QN48H	00X	JTAG Autoboot SSPI	-

Device	Package	Mode[2:0]	Configuration Mode	Notes
	MG132H CS100H	X0X	JTAG I²C Autoboot SSPI	When I²C is supported, the SDA and SCL pins need to be externally pulled up; when Mode[2,0] is configured as 100 and Autoboot is used, SDA pin needs to be external pulled up.
	QN88	XXX	JTAG I²C Autoboot SSPI MSPI DUAL BOOT SERIAL CPU	-
GW1N-1P5	LQ100X QN48X	100	JTAG I²C Autoboot	When I²C is supported, the SDA and SCL pins need to be external pulled up; when Mode[2,0] is configured as 100 and Autoboot is used, SDA pin needs to be external pulled up.
	LQ100 QN48XF	000	JTAG Autoboot	-

Note!

[1] For the GW1N-2 device, if its MODE[2] value is fixed to 1, its loading frequency can only be 2.5MHz.

3 Architecture

3.1 Architecture Overview

Figure 3-1 Architecture Overview of GW1N-9

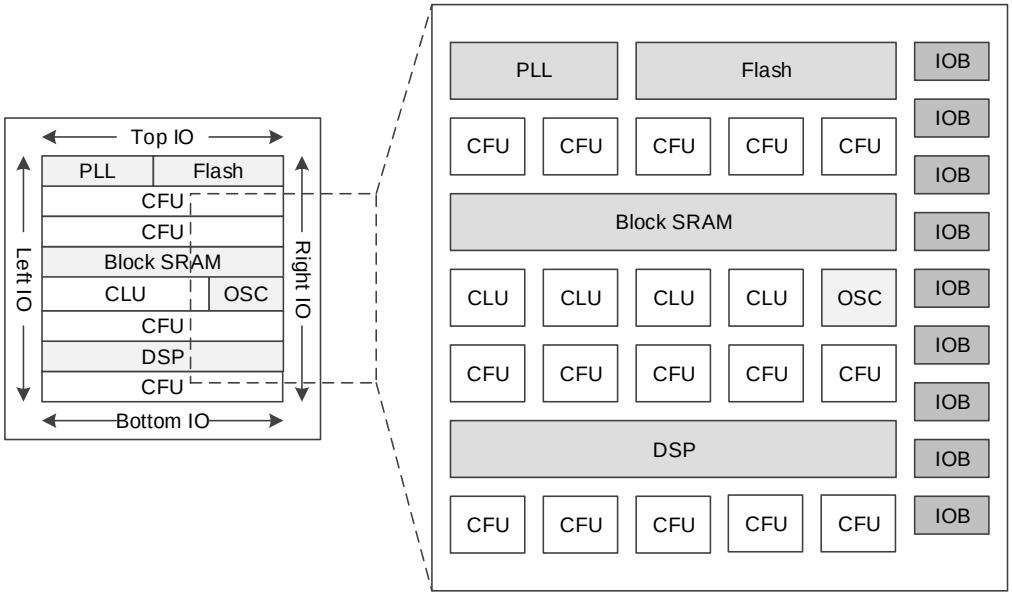


Figure 3-2 Architecture Overview of GW1N-4

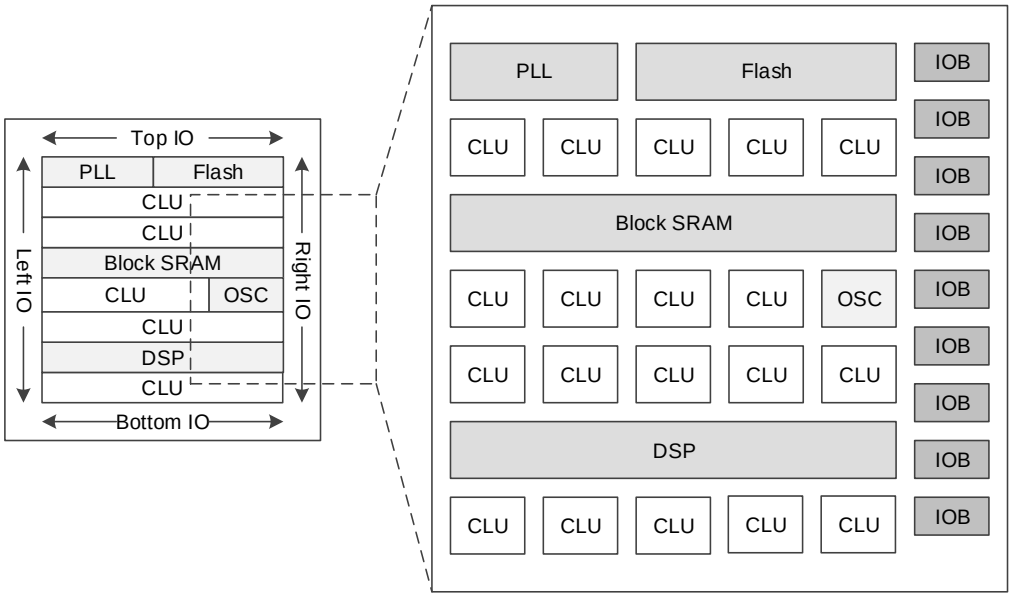


Figure 3-3 Architecture Overview of GW1N-1

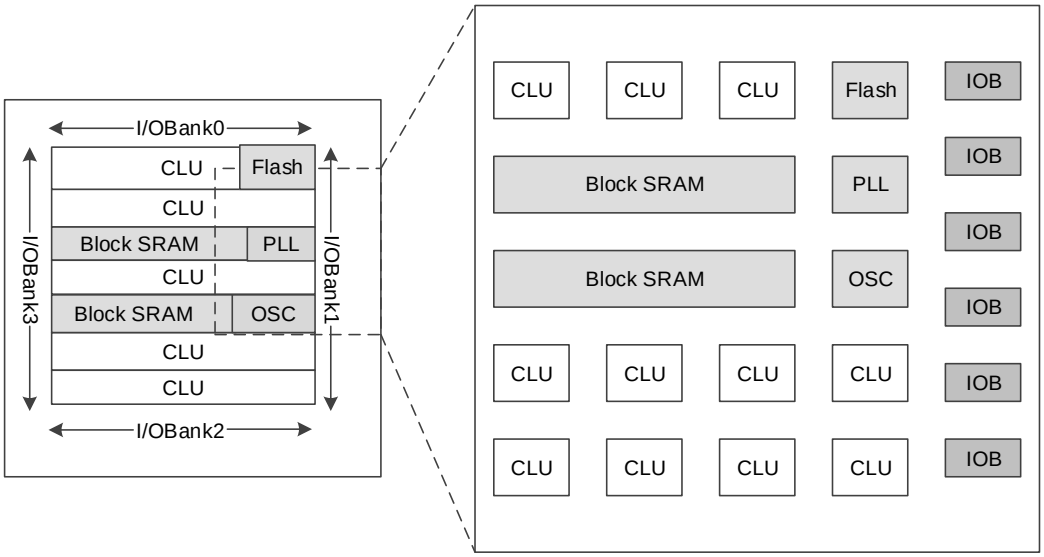
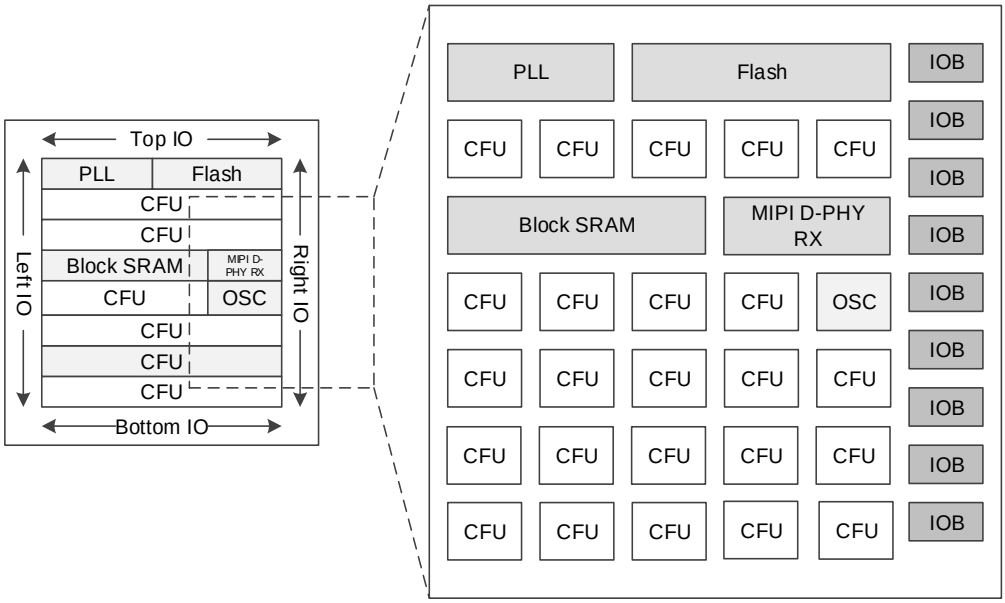


Figure 3-4 Architecture Overview of GW1N-2



As shown in Figure 3-1 to Figure 3-3, the core of GW1N series of FPGA products is CFU. The GW1N series of FPGA products also provide BSRAMs, PLLs, on-chip oscillator, and Flash resources that support Instant-on. Figure 3-4 is the architecture overview of GW1N-2. MIPI D-PHY RX is also embedded in GW1N-2. See Table 2-1 for more detailed information.

Note!

GW1N series of FPGA products include the devices of GW1N-1, GW1N-1S, GW1N-1P5, GW1N-2, GW1N-4, and GW1N-9. In these devices, CFU, BSRAM, GCLK, and on chip crystals are the same, but the other resources, such as DSP, Flash, I/Os, PLL, high-speed clock, etc., are slightly different.

Configurable Function Unit (CFU) is the base cell for the array of GW1N series FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. Memory mode is supported in GW1N-1P5/2/9. For more detailed information, see 3.2 Configurable Function Unit.

The I/O resources in the GW1N series of FPGA products are arranged around the periphery of the devices in groups referred to as banks[1]. Up to four Banks are supported, including Bank0, Bank1, Bank2, and Bank3. The I/O resources support multiple level standards, and support basic mode, SDR mode, and generic DDR mode. For more detailed information, see 3.3 IOB.

Note!

[1]GW1N-1S includes three Banks, which are Bank0, Bank1, and Bank2 respectively. For further detailed information, please refer to the I/O BANK distribution view in 3.3.1 I/O Buffer.

The BSRAM is embedded as a row in the GW1N series of FPGA products. Each BSRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. For more detailed information, see 3.4 Block SRAM (BSRAM).

The GW1N series of FPGA products are embedded with Flash resources, including configuration Flash resources and user Flash resources. Configuration Flash resources are used for internal Flash programming, please refer to 3.12 Programming Configuration for detailed information. User Flash resources are used for user storage, for more detailed information, see 3.5 User Flash (GW1N-1 and GW1N-1S) and 3.6 User Flash (GW1N-1P5/2/4/9).

GW1N-4 and GW1N-9 support DSP. DSP blocks are embedded as a row in the FPGA array. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. For more detailed information, see 3.7 DSP.

Note!

GW1N-1 and GW1N-1S do not support DSP currently.

GW1N-1, GW1N-2, and GW1N-1S provide one PLL. GW1N-4 and GW1N-9 provide PLLs. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by the configuration of parameters. There is an internal programmable on-chip oscillator in each GW1N series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125 MHz, providing the clock resource for the MSPI mode. It also provides a clock resource for user designs with the clock precision reaching ±5%. For more detailed information, see 3.9 Clock, 3.13 On Chip Oscillator.

GW1N-2 provides the hard core MIPI D-PHY RX and also the flexible highspeed FPGA IO which supports both MIPI D-PHY RX and TX interfaces. For further details, please refer to 3.8 MIPI D-PHY.

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1N series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For further detailed information, see 3.9 Clock, 3.10 Long Wire (LW), 3.11 Global Set/Reset (GSR).

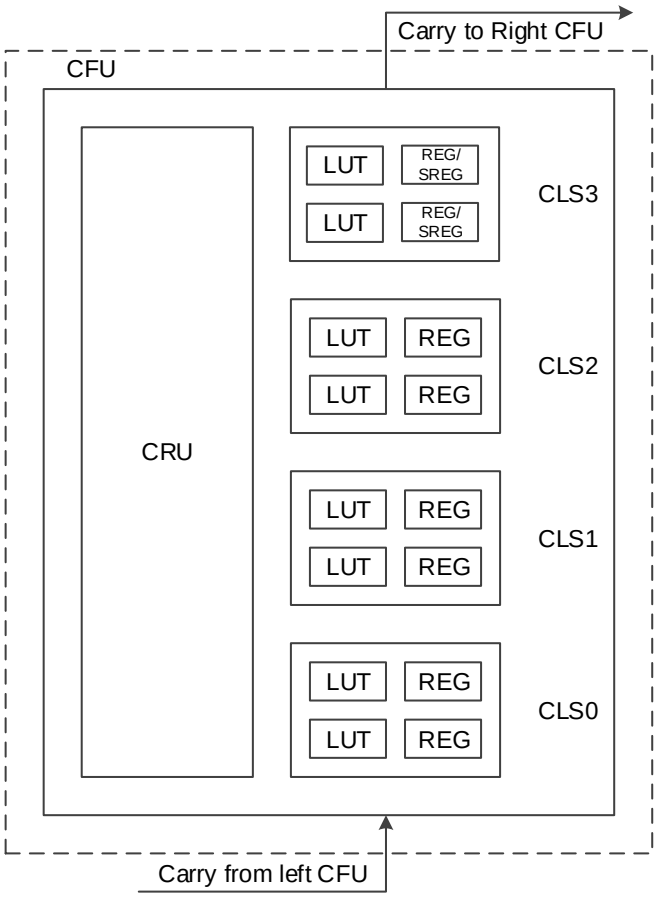
3.2 Configurable Function Unit

The configurable function unit and the configurable logic unit are two basic units for FPGA core of GOWINSEMI. As shown in Figure 3-5, each unit consists of four configurable logic sections and its configurable routing unit. Each of the three configurable logic sections contains two 4-input LUTs and two registers, and the other one only contians two 4-input LUTs.

Configurable logical sections in CLU cannot be configured as SRAM, but as basic logic, ALU, and ROM. The configurable logic sections in the CFU can be configured as basic logic, ALU, SRAM, and ROM depending on the applications.

For further more information about CFU, please refer to UG288, Gowin Configurable Function Unit (CFU) User Guide.

Figure 3-5 CFU View



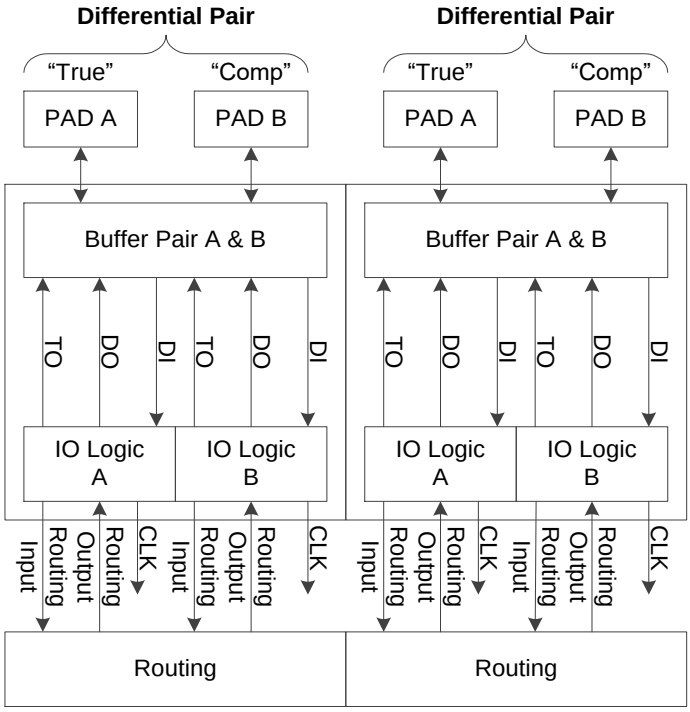
Note!

- SREG needs special patch support. Please contact Gowin technical support or local Office for this patch.
- Only GW1N-1P5 and GW1N-2 support REG in CLS3 currently, and the CLK, CE, and SR of CLS3 and CLS2 are driven by the same source.

3.3 IOB

The IOB in the GW1N series of FPGA products includes I/O buffer, I/O logic, and its routing unit. As shown in Figure 3-6, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-ended input/output.

Figure 3-6 IOB Structure View



IOB Features:

- V_{CCIO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL (true LVDS not supported in GW1N-1 and GW1N-1S)
- Input hysteresis option
- Output drive strength option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option
- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode
- Bank0/Bank1 of GW1N-1S support MIPI IO input
- Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 support MIPI IO output(with dynamic ODT)
- Bank2 of GW1N-2/GW1N-1P5 supports MIPI IO input(with dynamic ODT)
- Bank0 of GW1N-9 supports MIPI IO input(with dynamic ODT)
- The Bottom layer of GW1N-9 supports MIPI IO output
- The Top layer and Bottom layer of GW1N-9 support I3C

OpenDrain/PushPull conversion

Note!

GW1N-1 and GW1N-1S do not support true LVDS output.

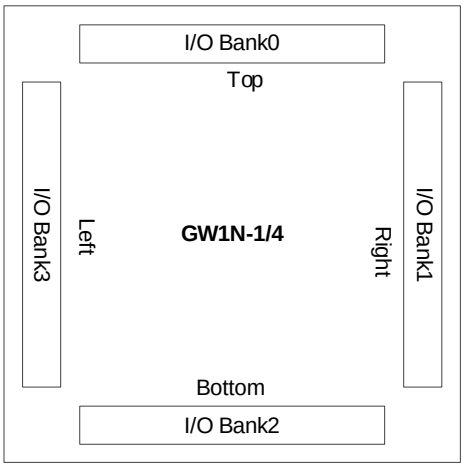
3.3.1 ~ 3.3.4 describe I/O buffer, True LVDS design, I/O logic, and I/O logic modes. For further information about IOB, please refer to UG289,Gowin Programmable IO (GPIO) User Guide.

3.3.1 I/O Buffer

Each Bank supports single power supply and has independent I/O power supply V_{CCIO}. To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as referenced voltage. The user can choose from the internal reference voltage of the bank (0.5 x V_{CCIO}) or the external reference voltage using any IO from the bank.

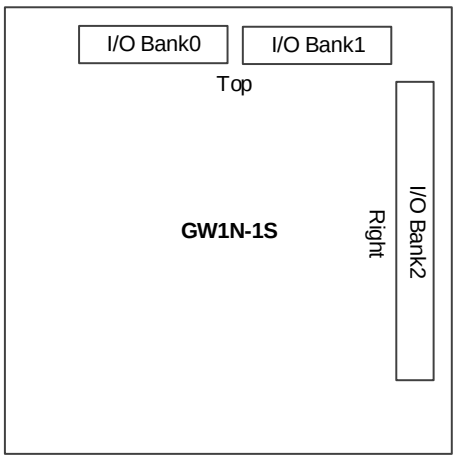
There are four IO Banks in the GW1N-1/4 products, as shown in Figure 3-7.

Figure 3-7 I/O Bank Distribution View of GW1N-1/4



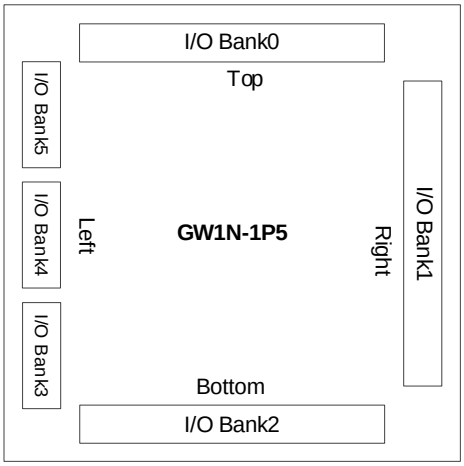
GW1N-1S includes three IO Banks, as shown in Figure 3-8.

Figure 3-8 I/O Bank Distribution View of GW1N-1S



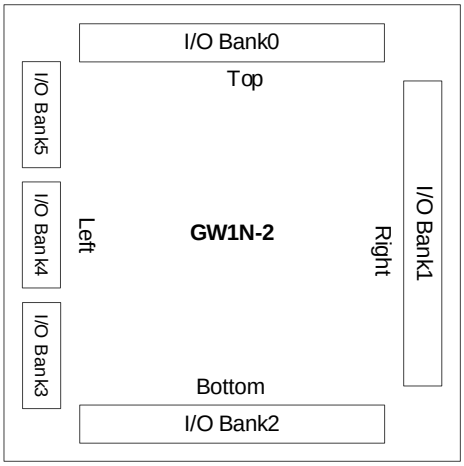
GW1N-1P5 includes six IO Banks, as shown in Figure 3-10.

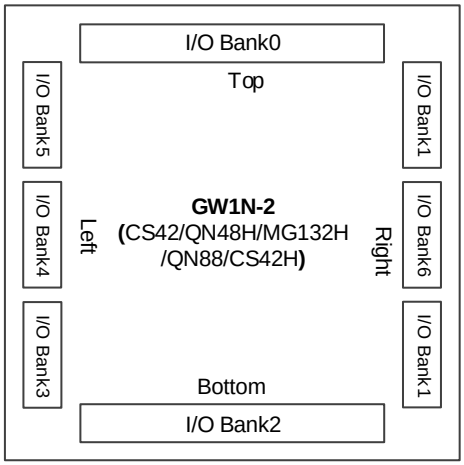
Figure 3-9 I/O Bank Distribution View of GW1N-1P5



GW1N-2 includes six IO Banks, and GW1N-2 in the CS42, CS42H, QN48H, QN88, and MG132H packagesincludes seven IO Banks, as shown in Figure 3-10.

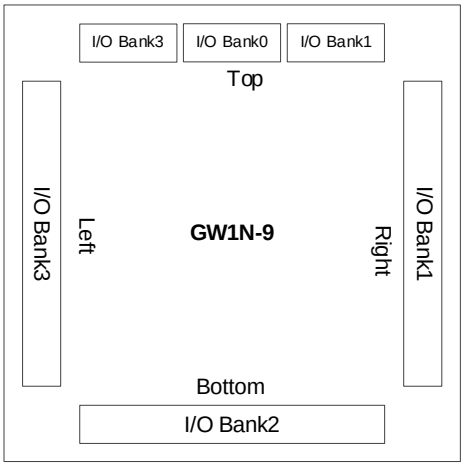
Figure 3-10 I/O Bank Distribution View of GW1N-2





There are four IO Banks in the GW1N-9 product, as shown in Figure 3-11.

Figure 3-11 I/O Bank Distribution View of GW1N-9



The GW1N series of FPGA products support LV, and UV, among which GW1N-1S supports LV version.

LV devices support 1.2 V V_{CC} to meet users' low power needs.

V_{CCIO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V aCCIOrding to requirements[1].

GW1N-1S does not support V_{CCX}. V_{CCX} of the other devices supports 2.5 V or 3.3 V power supply.

UV devices support 1.8V, 2.5 V, and 3.3 V, and linear voltage regulator is integrated to facilitate single power supply.

Bank0/Bank1 of GW1N-1S support MIPI IO input; Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 support MIPI IO output(with dynamic ODT); Bank2 of GW1N-2/GW1N-1P5 supports MIPI IO input(with dynamic ODT); Bank0 of GW1N-9 supports MIPI IO input(with dynamic ODT); The Bottom layer of GW1N-9 supports MIPI IO output; The Top layer and Bottom layer of GW1N-9 support I3C OpenDrain/PushPull conversion.

Note!

- During configuration, all GPIOs of the device are internally weak pull-up. After the configuration is complete, the I/O state is controlled by user programs and constraints. The state of CONFIG-related I/Os varies depending on the configuration mode.
- For the recommended operating conditions of different devices, please refer to 4.1 Operating Conditions.
- When the I/Os of Bank0/Bank1 of GW1N-1S are used as MIPI input, V_{CCIO0}/ V_{CCIO1} need to be supplied with 1.2V power supply.
- When the I/Os of Bank0/Bank3/Bank4/Bank of GW1N-2/GW1N-1P5 are used as MIPI output, V_{CCIO0}/V_{CCIO3}/V_{CCIO4}/V_{CCIO5} need to be supplied with 1.2V power supply.
- When the I/Os of Bank2 of GW1N-2/GW1N-1P5 are used as MIPI input, V_{CCIO2} needs to be supplied with 1.2V power supply.
- When the I/Os of Bank0 of GW1N-9 are used as MIPI input, V_{CCIO0} needs to be supplied with 1.2V power supply.
- When the I/Os in Bottom layer of GW1N-9 are used as MIPI output, V_{CCIO2} needs to be supplied with 1.2V power supply.

- The I/O power supply restrictions of BANK0, BANK1, BANK3 in GW1N-9 are as follows:
  - When V_{CCIO0} is greater than or equal to 1.8V, V_{CCIO1} and V_{CCIO3} support 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
  - When V_{CCIO0} is 1.5V, V_{CCIO1} and V_{CCIO3} support 1.2V, 1.5V, 1.8V, and 2.5V.

For the V_{CCIO} requirements of different I/O standards, see Table 3-1 and Table 3-2.

Table 3-1 Output I/O Standards and Configuration Options

I/O Type (Output)	Single-ended/ Differential	Bank V_{CCIO} (V)	Drive Strength (mA)	Typical Application
MIPI[1]	Differential (TLVDS)	1.2	3.5	Mobile industry processor interface
LVDS25[2]	Differential (TLVDS)	2.5/3.3	3.5/2.5/2/1.25	High-speed point-to-point data transmission
RSDS[2]	Differential (TLVDS)	2.5/3.3	2	High-speed point-to-point data transmission
MINILVDS[2]	Differential (TLVDS)	2.5/3.3	2	LCD timing driver interface and column driver interface
PPLVDS[2]	Differential (TLVDS)	2.5/3.3	1.25/2.0/2.5/3.5	LCD row/column driver
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmissio
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVPECL33E	Differential	3.3	16	High-speed data transmission
HSTL18D_I	Differential	1.8	8	memory interface
HSTL18D_II	Differential	1.8	8	memory interface
HSTL15D_I	Differential	1.5	8	memory interface
SSTL15D	Differential	1.5	8	memory interface
SSTL18D_I	Differential	1.8	8	memory interface

I/O Type (Output)	Single-ended/ Differential	Bank V_{CCIO} (V)	Drive Strength (mA)	Typical Application
SSTL18D_II	Differential	1.8	8	memory interface
SSTL25D_I	Differential	2.5	8	memory interface
SSTL25D_II	Differential	2.5	8	memory interface
SSTL33D_I	Differential	3.3	8	memory interface
SSTL33D_II	Differential	3.3	8	memory interface
LVCMOS12D	Differential	1.2	4/8	universal interface
LVCMOS15D	Differential	1.5	4/8	universal interface
LVCMOS18D	Differential	1.8	4/8/12	universal interface
LVCMOS25D	Differential	2.5	4/8/12/16	universal interface
LVCMOS33D	Differential	3.3	4/8/12/16/24	universal interface
HSTL15_I	Single-ended	1.5	8	memory interface
HSTL18_I	Single-ended	1.8	8	memory interface
HSTL18_II	Single-ended	1.8	8	memory interface
SSTL15	Single-ended	1.5	8	memory interface
SSTL18_I	Single-ended	1.8	8	memory interface
SSTL18_II	Single-ended	1.8	8	memory interface
SSTL25_I	Single-ended	2.5	8	memory interface
SSTL25_II	Single-ended	2.5	8	memory interface
SSTL33_I	Single-ended	3.3	8	memory interface
SSTL33_II	Single-ended	3.3	8	memory interface
LVCMOS12	Single-ended	1.2	4/8	universal interface
LVCMOS15	Single-ended	1.5	4/8	universal interface
LVCMOS18	Single-ended	1.8	4/8/12	universal interface
LVCMOS25	Single-ended	2.5	4/8/12/16	universal interface
LVCMOS33/ LVTTL33	Single-ended	3.3	4/8/12/16/24	universal interface
PCI33	Single-ended	3.3	4/8	PC and embedded system

Note!

- [1] Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 support MIPI I/O output; Bank2 of GW1N-9 supports MIPI I/O output.
- [2] GW1N-1/GW1N-1S does not support this I/O type.

Table 3-2 Input I/O Standards and Configuration Options

I/O Type (Input)	Single-ended/ Differential	Bank V_{CCIO} (V)	HYSTERESIS	Need V_{REF}
MIPI[1]	Differential (TLVDS)	1.2	No	No
LVDS25[2]	Differential (TLVDS)	2.5/3.3	No	No
RSDS[2]	Differential (TLVDS)	2.5/3.3	No	No
MINILVDS[2]	Differential (TLVDS)	2.5/3.3	No	No
PPLVDS[2]	Differential (TLVDS)	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
LVCMOS12D	Differential	1.2/1.5/1.8/2.5/3.3	No	No
LVCMOS15D	Differential	1.5/1.8/2.5/3.3	No	No
LVCMOS18D	Differential	1.8/2.5/3.3	No	No
LVCMOS25D	Differential	2.5/3.3	No	No
LVCMOS33D	Differential	3.3	No	No
HSTL15_I	Single-ended	1.5 or 1.5/1.8/2.5/3.3[3]	No	Yes
HSTL18_I	Single-ended	1.8 or 1.8/2.5/3.3[4]	No	Yes
HSTL18_II	Single-ended	1.8 or 1.8/2.5/3.3[4]	No	Yes

I/O Type (Input)	Single-ended/ Differential	Bank V_{CCIO} (V)	HYSTERESIS	Need V_{REF}
SSTL15	Single-ended	1.5 or 1.5/1.8/2.5/3.3[3]	No	Yes
SSTL18_I	Single-ended	1.8 or 1.8/2.5/3.3[4]	No	Yes
SSTL18_II	Single-ended	1.8 or 1.8/2.5/3.3[4]	No	Yes
SSTL25_I	Single-ended	2.5 or 2.5/3.3[5]	No	Yes
SSTL25_II	Single-ended	2.5 or 2.5/3.3[5]	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
LVCMOS12	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS33/ LVTTL33	Single-ended	1.2/1.5/1.8/2.5/3.3	Yes	No
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	No	No
LVCMOS33OD18	Single-ended	1.8	No	No
LVCMOS33OD15	Single-ended	1.5	No	No
LVCMOS25OD18	Single-ended	1.8	No	No
LVCMOS25OD15	Single-ended	1.5	No	No
LVCMOS18OD15	Single-ended	1.5	No	No
LVCMOS15OD12	Single-ended	1.2	No	No
LVCMOS25UD33	Single-ended	3.3	No	No
LVCMOS18UD25	Single-ended	2.5	No	No
LVCMOS18UD33	Single-ended	3.3	No	No
LVCMOS15UD18	Single-ended	1.8	No	No
LVCMOS15UD25	Single-ended	2.5	No	No
LVCMOS15UD33	Single-ended	3.3	No	No
LVCMOS12UD15	Single-ended	1.5	No	No
LVCMOS12UD18	Single-ended	1.8	No	No
LVCMOS12UD25	Single-ended	2.5	No	No
LVCMOS12UD33	Single-ended	3.3	No	No

Note!

- [1] Bank2 of GW1N-2/GW1N-1P5, Bank6 (Hard core) of GW1N-2, Bank0 of GW1N-9, and Bank0/ Bank1 of GW1N-1S support MIPI I/O input.
- [2] GW1N-1S does not support this I/O type.
- [3] When VREF is INTERNAL, the V_{CCIO} of this I/O type is 1.5V; when VREF is VREF1_LOAD, the V_{CCIO} of this I/O type is 1.5 V/1.8 V/2.5 V/3.3 V.
- [4] When VREF is INTERNAL, the V_{CCIO} of this I/O type is 1.8 V; when VREF is VREF1_LOAD, the V_{CCIO} of this I/O type is 1.8 V /2.5 V /3.3 V.
- [5] When VREF is INTERNAL, the V_{CCIO} of this I/O type is 2.5 V; when VREF is VREF1_LOAD, the V_{CCIO} of this I/O type is 2.5 V /3.3 V.

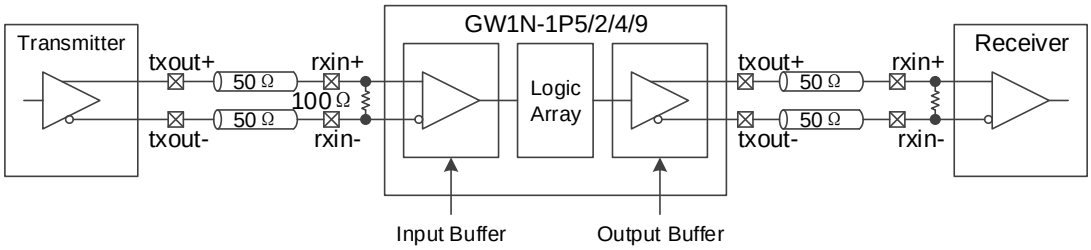
3.3.2 True LVDS Design

Except GW1N-1 / GW1N-1S, the other devices of GW1N series products support true LVDS output. GW1N series of FPGA products also support LVDS25E, MLVDS25E, BLVDS25E, etc.

For more detailed information about true LVDS, please refer to *UG174 GW1N-1P5 Pinout*, *UG171, GW1N-2 Pinout*, *UG105, GW1N-4 Pinout,* and *UG114, GW1N-9 Pinout*.

True LVDS input I/O needs a 100Ω termination resistor. See Figure 3-12 for the true LVDS design. Specific banks of the GW1N series of FPGA products support a programmable on-chip 100 ohm input differential termination resistor, see *UG289, Gowin Programable IO User Guide*.

Figure 3-12 True LVDS Design



For more information about termination for LVDS25E, MLVDS25E, and BLVDS25E , please refer to *UG289, Gowin Programable IO User Guide*.

3.3.3 I/O Logic

Figure 3-13 shows the I/O logic input and output of the GW1N series of FPGA products.

Figure 3-13 I/O Logic Input and Output

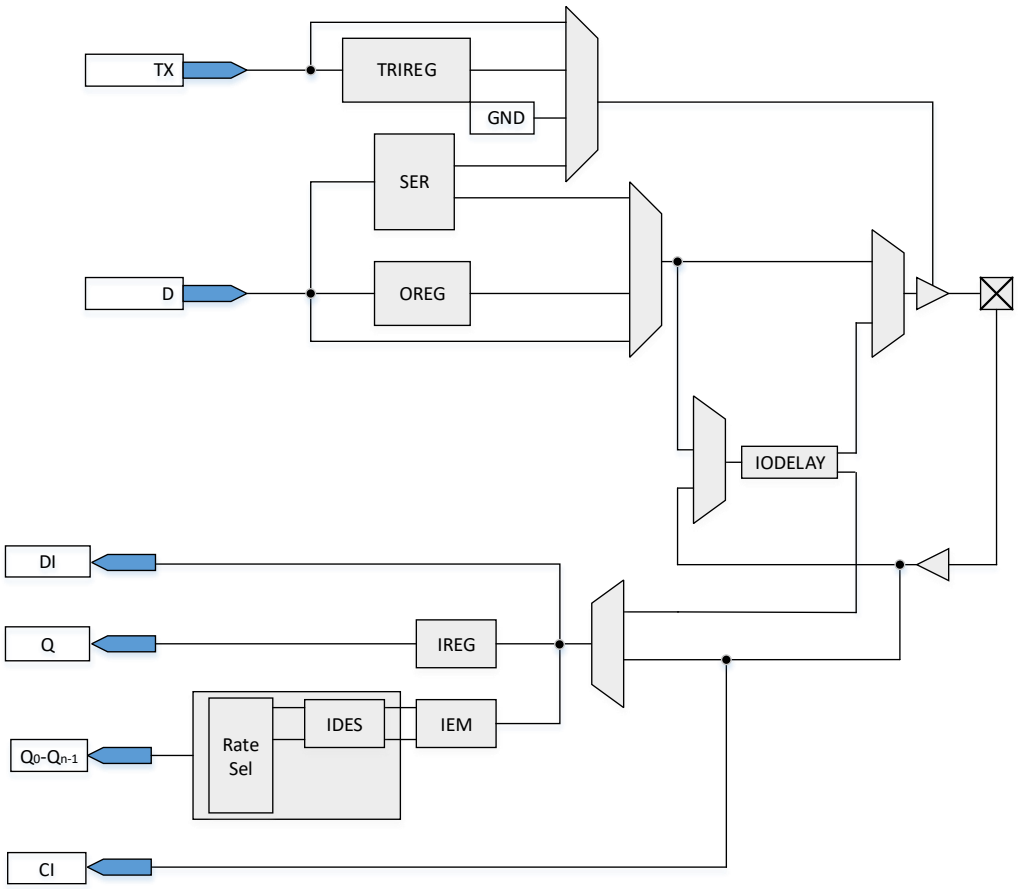


Table 3-3 Port Descsription

Ports	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to *UG107, GW1N-1 Pinout, UG169, GW1N-1S Pinout*, *UG171, GW1N-2 Pinout*, *UG174, GW1N-1P5 Pinout*, *UG105, GW1N-4 Pinout*, and *UG114, GW1N-9 Pinout.*
DI	Input	IO port low-speed input signal, entering into Fabric directly.
Q	Output	IREG output signal in SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in DDR module.

Note!

When CI is used as GCLK input, DI, Q, and Q_0-Q_{n-1} cannot be used as I/O input and output.

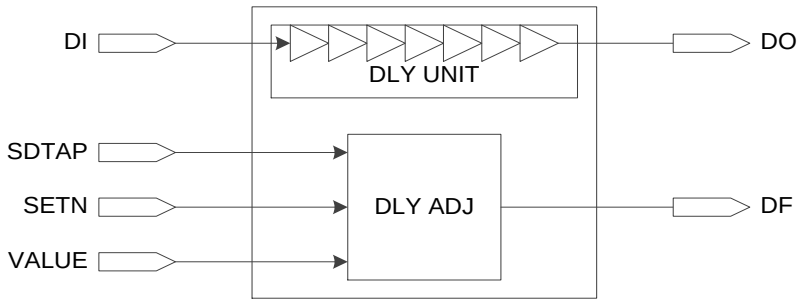
A description of the I/O logic modules of the GW1N series FPGA products is presented below.

IODELAY

See Figure 3-14 for an overview of the IODELAY. Each I/O of the

GW1N series of FPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 30ps.

Figure 3-14 IODELAY



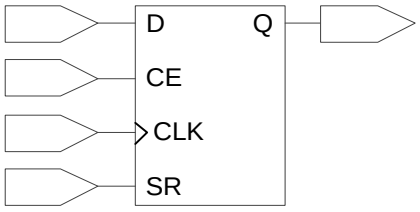
There are two ways to control the delay cell:

- Static control:
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

See Figure 3-15 for I/O register in the GW1N series of FPGA products. Each I/O provides one input register(IREG), one output register (OREG), and a tristate register(TRIREG).

Figure 3-15 Register Structure in I/O Logic



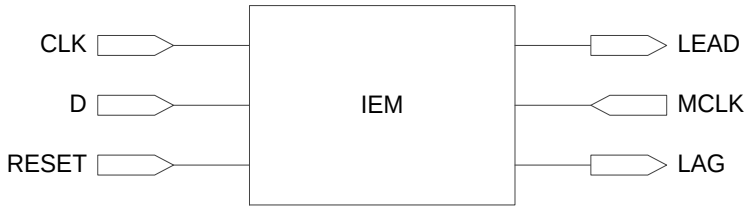
Note!

- CE can be either active low (0: enable) or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-16 for the IEM structure.

Figure 3-16 IEM Structure



De-serializer DES

The GW1N series of FPGA products provide a simple De-serializer DES for each output I/O to support advanced I/O protocols.

Serializer SER

The GW1N series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

3.3.4 I/O Logic Modes

The I/O Logic in the GW1N series of FPGA products supports several operations. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

GW1N-1S and GW1N-9 pins support IO logic. The GW1N-1 pins IOL6 (A, B,C….J) and IOR6 (A,B,C….J) do not support IO logic. The other pins of GW1N-1 support IO logic. The GW1N-4 pins IOL10 (A,B,C….J) and IOR10(A,B,C….J) do not support IO logic. The other pins of GW1N-4 support IO logic. The GW1N-1P5/2 pins IOT (A, B) and IOT3A do not support IO logic. The other pins of GW1N-1P5/2 support IO logic.

3.4 Block SRAM (BSRAM)

3.4.1 Introduction

The GW1N series of FPGA products provide abundant BSRAMs. The Block SRAM (BSRAM) is embedded as a row in the FPGA array and is different from SSRAM (Shadow SRAM). Each BSRAM has 18,432 bits (18Kbits). There are four operation modes: Single Port, Dual Port, Semi Dual Port, and ROM.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. BSRAM features include the following:

- Max.18,432 bits per BSRAM
- BSRAM itself can run at 190 MHz at max
- Single Port
- Dual Port
- Semi Dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Normal Read and Write Mode
- Read-before-write Mode

- Write-through Mode

3.4.2 Configuration Mode

The BSRAM mode in the GW1N series of FPGA products supports different data bus widths. See Table 3-4.

Table 3-4 Memory Size Configuration

Single Port Mode	Dual Port Mode[1]	Semi-Dual Port Mode	Read Only
16 K x 1	16 K x 1	16 K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Note!

[1] GW1N-1S does not support Dual Port Mode; For the GW1N-9 devices, only the C version supports Dual Port Mode.

Single Port Mode

In the single port mode, BSRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of BSRAM. Normal-Write Mode and Write–through Mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge.

Dual Port Mode

BSRAM supports dual port mode. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

For further information about Dual Port Block Memory ports and the related description, please refer to *UG285, Gowin BSRAM&SSRAM User Guide*.

Semi-Dual Port Mode

Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

For further information about Semi-Dual Port Block Memory ports and

the related description, please refer to *UG285E, Gowin BSRAM&SSRAM User Guide*.

Read Only

BSRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each BSRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to *UG285, Gowin BSRAM&SSRAM User Guide*.

3.4.3 Mixed Data Bus Width Configuration

The BSRAM in the GW1N series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-5 and Table 3-6 below.

Table 3-5 Dual Port Mixed Read/Write Data Width Configuration[1],[2]

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

- [1] GW1N-1S does not support Dual Port Mode; For the GW1N-9K series, only GW1N-9C supports dual-port mode.
- [2] ”*”denotes the modes supported.

Table 3-6 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*"denotes the modes supported.

3.4.4 Byte-enable

The BSRAM in the GW1N series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the BSRAM write operation.

Note!

For the GW1N series, only the GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1N-2, GW1N-2B, GW1N-2C, and GW1N-4D support the byte-enable function.

3.4.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

3.4.6 Synchronous Operation

- All the input registers of BSRAM support synchronous write;
- The output registers can be used as pipeline registers to improve design performance;
- The output registers are bypass-able.

3.4.7 Power up Conditions

BSRAM initialization is supported when powering up. During the power-up process, BSRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.4.8 BSRAM Operation Modes

BSRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the BSRAM via output registers or without using the output registers.

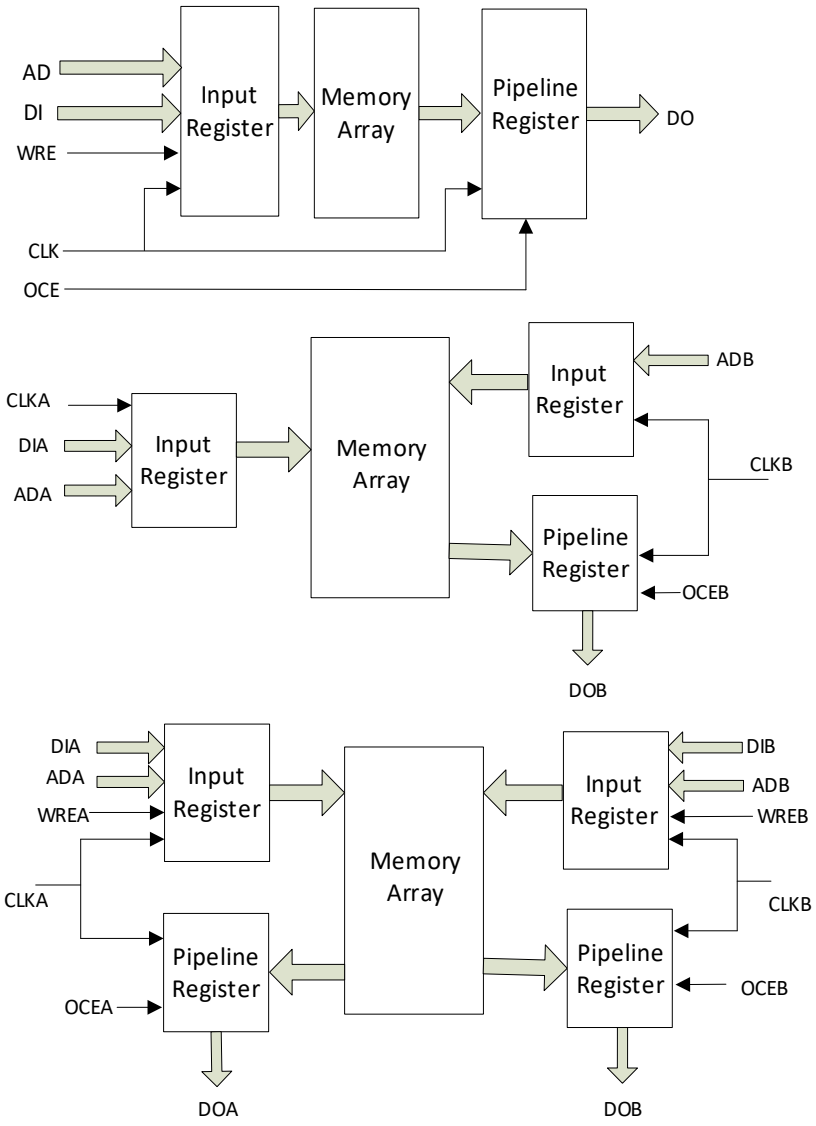
Pipeline Mode

When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

Bypass Mode

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

Figure 3-17 Pipeline Mode in Single Port, Dual Port and Semi Dual Port



Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data

written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory aCCIOrding to the address. The original data in this address will appear at the output of this port.

3.4.9 Clock Operations

Table 3-7 lists the clock operations in different BSRAM modes:

Table 3-7 Clock Operations in Different BSRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

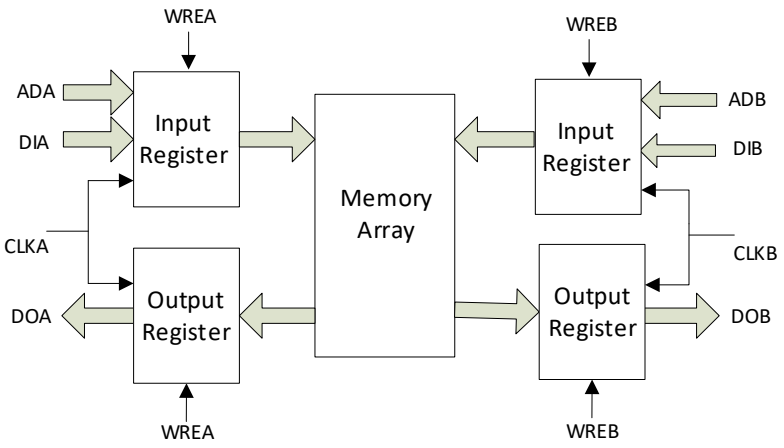
Note!

GW1N-1S does not support Dual Port Mode.

Independent Clock Mode

Figure 3-18 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

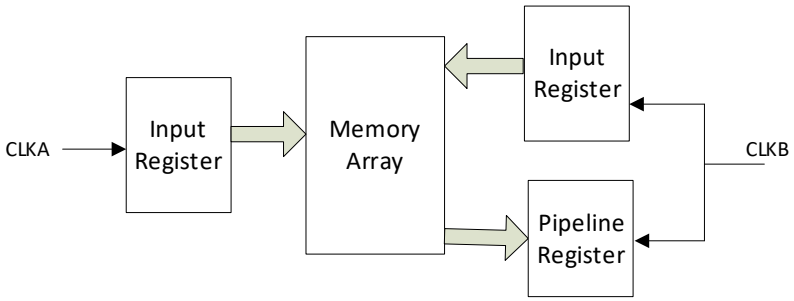
Figure 3-18 Independent Clock Mode



Read/Write Clock Operation

Figure 3-19 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

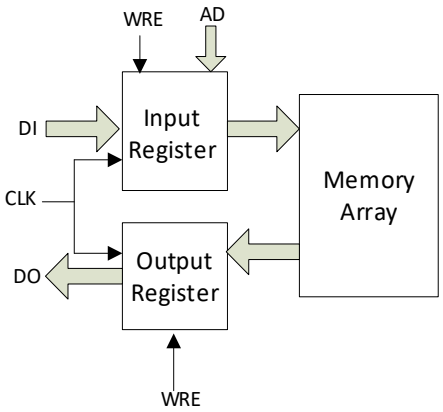
Figure 3-19 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-20 shows the clock operation in single port mode.

Figure 3-20 Single Port Clock Mode



3.5 User Flash (GW1N-1 and GW1N-1S)

GW1N-1 and GW1N-1S devices support User Flash with 12 Kbytes (48 page x 256 Bytes). The features are as following:

- NOR Flash
- 100,000 write cycles
- Greater than10 years Data Retention at +85 ℃
- Selectable 8/16/32 bits data-in and data-out
- Page size: 256 Bytes
- 3 μA standby current
- Page Write Time: 8.2 ms

For further information about the user Flash in GW1N-1 and GW1N-1S, please refer to UG295, Gowin User Flash User Guide. For the correspondence between user Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295, Gowin User Flash User Guide.

3.6 User Flash (GW1N-1P5/2/4/9)

GW1N-1P5/2/4/9 offers User Flash. The capacity of the User Flash in GW1N-1P5/2 is 96Kbits.The capacity of the User Flash in GW1N-4 is 256Kbits. The capacity of the User Flash in GW1N-9 is 608Kbits. The user Flash memory is composed of row memory and column memory. One row memory is composed of 64 column memories. The capacity of one column memory is 32 bits, and the capacity of one row memory is 64*32=2048 bits. Page erase is supported, and one page capacity is 2048 bytes, i.e., one page includes 8 rows. The features are shown below:

- NOR Flash
- 10,000 write cycles
- Greater than10 years Data Retention at +85 ℃
- Data Width: 32
- GW1N-1P5/2 capacity: 48 rows x 64 columns x 32 = 96kbits
- GW1N-4 capacity: 128 rows x 64 columns x 32 = 256kbits
- GW1N-9 capacity: 304 rows x 64 columns x 32 = 608kbits
- Page Erase Capability: 2,048 bytes per page
- Fast Page Erasure/Word Programming Operation
- Clock frequency: 40 MHz
- Word Programming Time:≤16 μs
- Page Erasure Time:≤120 ms
- Electric current
  - Read current/duration:2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX)
  - Program/Erase operation: 12/12 mA(MAX)

For more information about the user Flash in GW1N-1P5/2/4/9, please refer to *UG295, Gowin User Flash User Guide*. For the correspondence between user Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295.

3.7 DSP

GW1N-4/9 devices offer abundant DSP resources. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel shifter

- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

3.7.1 Macro

DSP blocks are embedded as rows in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

PADD

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs.,

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

Note!

Each input end supports pipeline mode and bypass mode.

GOWINSEMI PADD can be used as a function block independently, which supports 9-bit and 18-bit width.

MULT

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Register mode and bypass mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Note!

Two adjacent DSP macros can form a 36 x 36 multiplier.

ALU

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. The register mode and bypass mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

3.7.2 DSP Operations

- Multiplier

- Accumulator
- MULTADDALU

For further information about DSP, please refer to *UG287, Gowin DSP User Guide*.

3.8 MIPI D-PHY

3.8.1 Hard Core - MIPI D-PHY RX(GW1N-2)

GW1N-2 provides provides a standalone MIPI RX D-PHY supporting the v2.1 specification of MIPI Alliance Standard. The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays.

- High Speed RX at up to 8 Gbps per quad
- 1, 2 or 4 data lane and 1 clock lane support per PHY
- Bidirectional Low-power (LP) mode at up to 10mbps per lane
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports MIPI DSI and MIPI CSI-2 link layers
- Availible on bank 6

For further detailed information, please refer to *IPUG778, Gowin GW1N-2 Hardened MIPI D-PHY RX User Guide*.

3.8.2 GPIO support for MIPI D-PHY RX and TX

The GPIOs of GW1N-1P5, GW1N-2, and GW1N-9 support MIPI D-PHY RX and TX interfaces. The GPIOs of GW1N-1S only support MIPI D-PHY RX interface. Highspeed FPGA IO supports MIPI DSI and CSI-2 video interfaces for cameras and displays in both transmit and receive modes.

- MIPI Alliance Standard for D-PHY Specification, Version 1.2
- High Speed RX and TX at up to 4.8 Gbps per port
- 1, 2 or 4 data lane and 1 clock lane support per PHY
- Multiple PHY support (number of IO permitting)
- Bidirectional Low-power (LP) mode
- Supports MIPI DSI and MIPI CSI-2 link layers
- Built-in HS Sync, bit and lane alignment
- 1:8 and 1:16 deserialization modes to FPGA fabric's user interface
- Supports multiple IO Types
  - ELVDS, TLVDS, SLVS200, LVDS and MIPI D-PHY IO
- Bank0/Bank1 of GW1N-1S support MIPI IO input
- Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 support MIPI IO output(with dynamic ODT)
- Bank2 of GW1N-2/GW1N-1P5 supports MIPI IO input(with dynamic

ODT)

- Bank0 of GW1N-9 supports MIPI IO input(with dynamic ODT)
- The Bottom layer of GW1N-9 supports MIPI IO output
- The Top layer and Bottom layer of GW1N-9 support I3C OpenDrain/PushPull conversion

For further detailed information, please refer to *IPUG948, Gowin MIPI D-PHY RX TX Advance user guide*.

3.9 Clock

The clock resources and routing are critical to high-performance applications in FPGA. The GW1N series of FPGA products provide the global clock network (GCLK) that is connected to all the registers directly. Besides the global clock network, the GW1N series of FPGA products provide high-speed clock HCLK, PLLs, etc.

For further detailed information, please refer to *UG286, Gowin Clock User Guide*.

3.9.1 Global Clock

The GCLK is distributed in the device as quadrants. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

3.9.2 PLL

Phase-locked Loop (PLL) is a feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

GW1N PLL blocks in the GW1N series of FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by parameters configuration.

3.9.3 HCLK

HCLK is the high-speed clock in the GW1N series of FPGA products, which can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-21, Figure 3-22, Figure 3-23, Figure 3-24, and Figure 3-25.

Note!

The features of the HCLK in GW1N-1 and GW1N-4 are the same; the features of the HCLK in GW1N-1S and GW1N-9 are slightly different.

Figure 3-21 GW1N-1 HCLK Distribution

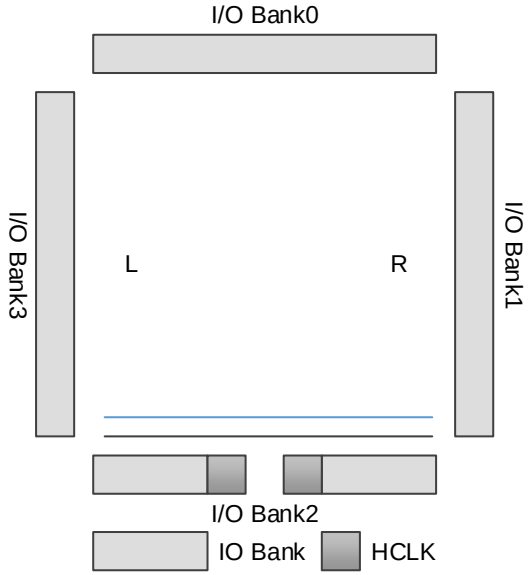


Figure 3-22 GW1N-1P5 / GW1N-2 HCLK Distribution

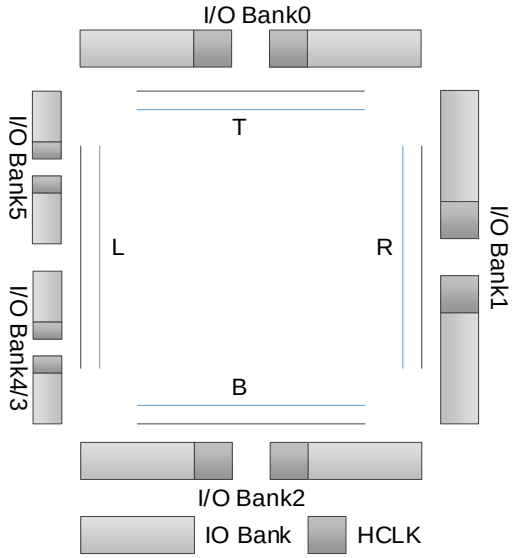


Figure 3-23 GW1N-4 HCLK Distribution

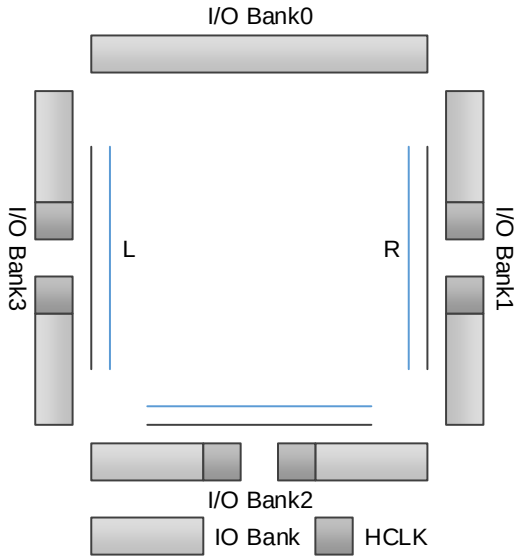


Figure 3-24 GW1N-9 HCLK Distribution

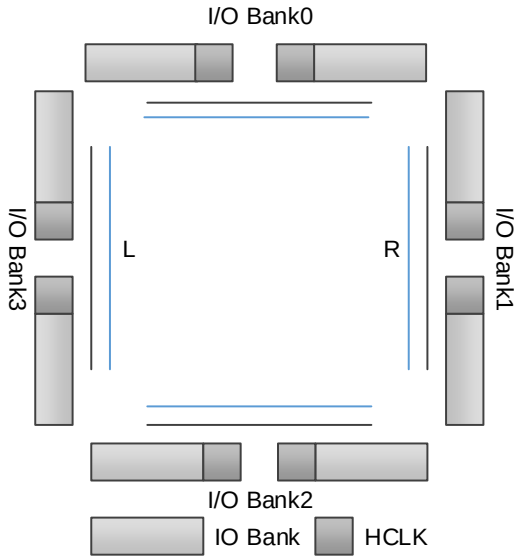
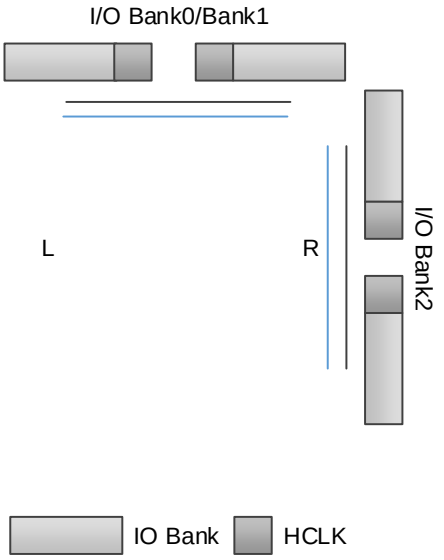


Figure 3-25 GW1N-1S HCLK Distribution



3.10 Long Wire (LW)

As a supplement to CRU, the GW1N series of FPGA products provide another routing resource- Long Wire, which is suitable for clock, clock enable, set/reset, or other high fan out signals.

3.11 Global Set/Reset (GSR)

A global set/rest (GSR) network is built in the GW1N series of FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset. The registers in CFU and I/O can be individually configured to use GSR.

3.12 Programming Configuration

The GW1N series of FPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash. The GW1N series of FPGA products support DUAL BOOT, providing a selection for users to backup data to off-chip Flash aCCIOrding to requirements.

Besides JTAG, the GW1N series of FPGA products also support GOWINSEMI own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, CPU, and I^2C Slave. All the devices support JTAG and AUTO BOOT. For more detailed information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

SRAM Configuration

When you adopt SRAM to configure the device, and each time the device is powered on, it needs to download the bit stream file to configure.

Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the

Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”.

The GW1N series of FPGA products (except the GW1N-4 A version) support the feature of background upgrade. That is to say, you can program the embedded Flash or external Flash via the JTAG[1] interface without affecting the current working state. During programming, the device works aCCIOrding to the previous configuration. After programming, RECONFIG_N[2] is triggered at low pulse to complete the online upgrade. This feature applies to the applications requiring long online time and irregular upgrades.

Note!

- [1] GW1N-1P5 and GW1N-2 can support the I^2C background upgrade by using the goConfig I2C IP. It is recommended to use the JTAG interface to implement the background upgrade.
- [2] As a configuration pin, RECONFIG_N is an input pin with internal weak pull-up, but as a GPIO pin, RECONFIG_N can only be used as the output type. For further detailed information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

The GW1N series of FPGA products also support off-chip Flash configuration and dual-boot. Please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

3.13 On Chip Oscillator

There is an internal oscillator in each of the GW1N series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125MHz. It provides programmable user clock with clock precision ±5%. During the configuration process, it can provide a clock for MSPI mode.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is used to get GW1N-1/1S output clock frequency: fout=240MHz/Param.

The following formula is used to get GW1N-1P5/2/9 output clock frequency: fout=250MHz/Param.

The following formula is used to get GW1N-4 output clock frequency: fout=210MHz/Param

Note!

“Param” is the configuration parameter with a range of 2~128. It supports even numbers only.

See Table 3-8 for GW1N-4 output frequency; see Table 3-9 for GW1N-1P5/2/9 output frequency; see Table 3-10 for GW1N-1/1S output frequency.

Table 3-8 GW1N-4 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.1MHz[1]	8	6.6MHz	16	13.1MHz
1	4.6MHz	9	7MHz	17	15MHz
2	4.8MHz	10	7.5MHz	18	17.5MHz
3	5MHz	11	8.1MHz	19	21MHz
4	5.3MHz	12	8.8MHz	20	26.3MHz
5	5.5MHz	13	9.5MHz	21	35MHz
6	5.8MHz	14	10.5MHz	22	52.5MHz
7	6.2MHz	15	11.7MHz	23	105MHz[2]

Table 3-9 GW1N-1P5/2/9 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Table 3-10 GW1N-1/1S Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.4MHz[1]	8	7.5MHz	16	15MHz
1	5.2MHz	9	8MHz	17	17MHz
2	5.5MHz	10	8.6MHz	18	20MHz
3	5.7MHz	11	9MHz	19	24MHz
4	6MHz	12	10MHz	20	20MHz
5	6.3MHz	13	11MHz	21	40MHz
6	6.7MHz	14	12MHz	22	60MHz
7	7MHz	15	13MHz	23	120MHz[2]

Note!

- [1] Default frequency
- [2] 125MHz is not suitable for MSPI.

4 AC/DC Characteristics

Note!

Please ensure that you use GOWINSEMI devices within the recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate normally beyond the operating conditions and range.

4.1 Operating Conditions

4.1.1 Absolute Max. Ratings

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	-0.5V	1.32V
	UV: Core Power	-0.5V	3.75V
V_{CCIO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	Auxiliary Voltage	-0.5V	3.75V
-	I/O Voltage Applied[1]	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65℃	+150℃
Junction Temperature	Junction Temperature	-40℃	+125℃

Note!

[1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	1.14V	1.26V
	UV: Core Power	1.71V	3.6V
V_{CCIO}	I/O Bank Power	1.14V	3.6V
V_{CCX}	Auxiliary voltage(GW1N-4/9)	2.375V	3.6V
	Auxiliary voltage(GW1N-1P5/2)	1.71V	3.6V
T_{JCOM}	Junction temperature (Commercial operation)	0℃	+85℃
T_{JIND}	Junction temperature (Industrial operation)	-40℃	+100℃

Note!

- For some packages, V_{CCIO} and V_{CCX} may share one pin. In this case, V_{CCX} requirements must be met first.
- For further power supply info, please refer to *UG107, GW1N-1 Pinout, UG169, GW1N-1S Pinout*, *UG171, GW1N-2 Pinout*, *UG174, GW1N-1P5 Pinout*, *UG105, GW1N-4 Pinout,* and *UG114, GW1N-9 Pinout.*

4.1.3 Power Supply Ramp Rates

Table 4-3 Power Supply Ramp Rates

Name	Description	Device	Min.	Typ.	Max.
V_{CC} Ramp	Power supply ramp rates for V_{CC}	GW1N-1/GW1N-1S	1.2mV/μs	-	40mV/μs
		GW1N-1P5/2/4/9	0.6mV/μs	-	6mV/μs
V_{CCX} Ramp	Power supply ramp rates for V_{CCX}	GW1N	0.6mV/μs	-	10mV/us
V_{CCIO} Ramp	Power supply ramp rates for V_{CCIO}	GW1N	0.1mV/μs	-	10mV/us

Note!

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 4-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

4.1.4 Hot Socket Specifications

Table 4-4 Hot Socket Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI, TDO, TMS,TCK	120uA

4.1.5 POR Feature

Table 4-5 POR Voltage

Name	Description	Device	Name	Value
V_{POR_UP}	Power on reset ramp up trip point	GW1N-1	V_{CC}	0.75V
			V_{CCIO}	0.85V
		GW1N-1P5、GW1N-2	V_{CC}	0.8V
			V_{CCX}	1.5V
			V_{CCIO}	0.95V
		GW1N-4	V_{CC}	0.95V
			V_{CCX}	1.95V
			V_{CCIO}	0.95V
		GW1N-9	V_{CC}	0.95V
			V_{CCX}	1.95V
			V_{CCIO}	0.95V
V_{POR_DOWN}	Power on reset ramp down trip point	GW1N-1	V_{CC}	TBD
			V_{CCIO}	TBD
		GW1N-1P5、GW1N-2	V_{CC}	0.65V
			V_{CCX}	1.3V
			V_{CCIO}	0.75V
		GW1N-4	V_{CC}	0.75V
			V_{CCX}	1.8V
			V_{CCIO}	0.6V
		GW1N-9	V_{CC}	0.75V
			V_{CCX}	1.8V
			V_{CCIO}	0.6V

4.2 ESD

Table 4-6 GW1N ESD - HBM

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9	GW1N-1S
LQ100	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
LQ100X	-	HBM>1,000V	HBM>1,000V	-	-	-
LQ144	-	-	-	-	-	-
LQ144X	-	-	HBM>1,000V	-	-	-
LQ144F	-	-	HBM>1,000V	-	-	-
EQ144	-	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
LQ176	-	-	-	-	HBM>1,000V	-
EQ176	-	-	-	-	HBM>1,000V	-
MG100	-	-	-	-	HBM>1,000V	-
MG100T	-	-	-	-	HBM>1,000V	-
MG49	-	-	HBM>1,000V	-	-	-
MG121	-	-	HBM>1,000V	-	-	-
MG121X	-	-	HBM>1,000V	-	-	-
MG132	-	-	HBM>1,000V	-	-	-
MG132X	-	-	HBM>1,000V	HBM>1,000V	-	-
MG132H	-	-	HBM>1,000V	-	-	-
MG160	-	-	-	HBM>1,000V	HBM>1,000V	-
MG196	-	-	-	-	HBM>1,000V	-
PG256	-	-	-	HBM>1,000V	HBM>1,000V	-
PG256M	-	-	-	HBM>1,000V	-	-
UG169	-	-	-	HBM>1,000V	HBM>1,000V	-
UG256	-	-	-	-	HBM>1,000V	-
UG332	-	-	-	-	HBM>1,000V	-
QN32X	-	-	HBM>1,000V	-	-	-
QN32	-	-	HBM>1,000V	HBM>1,000V	-	-
QN48	-	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
QN48H	-	-	HBM>1,000V	-	-	-
QN48F	-	-	-	-	HBM>1,000V	-
QN48X	-	HBM>1,000V	-	-	-	-
QN48XF	-	HBM>1,000V	-	-	-	-
CS30	HBM>1,000V	-	-	-	-	-

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9	GW1N-1S
CS42	-	-	HBM>1,000V	-	-	-
CS42H	-	-	HBM>1,000V	-	-	-
CS72	-	-	-	HBM>1,000V	-	-
CS81M	-	-	-	-	HBM>1,000V	
CS100H	-	-	HBM>1,000V	-	-	-
QN88	-	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
FN32	-	-	-	-	-	-

Table 4-7 GW1N ESD - CDM

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9	GW1N-1S
LQ100	-	-	CDM>500V	CDM>500V	CDM>500V	-
LQ100X	-	CDM>500V	CDM>500V	-	-	-
LQ144	-	-	CDM>500V	CDM>500V	CDM>500V	-
LQ144X		-	CDM>500V	-	-	-
LQ144F	-	-	CDM>500V	-	-	-
EQ144	-	-	-	CDM>500V	CDM>500V	-
LQ176	-	-	-	-	CDM>500V	-
EQ176	-	-	-	-	CDM>500V	-
MG49	-	-	CDM>500V	-	-	-
MG100	-	-	-	-	CDM>500V	-
MG121	-	-	CDM>500V	-	-	-
MG121X	-	-	CDM>500V	-	-	-
MG132	-	-	CDM>500V	-	-	-
MG132X	-	-	CDM>500V	CDM>500V	-	-
MG132H	-	-	CDM>500V	-	-	-
MG160	-	-	-	CDM>500V	CDM>500V	-
MG196	-	-	-	-	CDM>500V	-
MG100T		-	-	-	-	CDM>500V
PG256	-	-	-	CDM>500V	CDM>500V	-
PG256M	-	-	-	CDM>500V	-	-
UG169	-	-	-	CDM>500V	CDM>500V	
UG256	-	-	-	-	CDM>500V	-
UG332	-	-	-	-	CDM>500V	-
QN32	-	-	CDM>500V	CDM>500V	-	-

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9	GW1N-1S
QN32X	-	-	CDM>500V	-	-	-
QN48	-	-	-	CDM>500V	CDM>500V	-
QN48H	-	-	CDM>500V	-	-	-
QN48F	-	-	-	-	CDM>500V	-
QN48X	-	CDM>500V	-	-	-	-
QN48XF	-	CDM>500V	-	-	-	-
CS30	CDM>500V	-	-	-	-	-
CS42	-	-	CDM>500V	-	-	-
CS42H	-	-	CDM>500V	-	-	-
CS72	-		-	CDM>500V	-	-
CS81M	-	-	-	-	CDM>500V	-
CS100H	-	-	CDM>500V	-	-	-
QN88	-	-	CDM>500V	CDM>500V	CDM>500V	-
FN32	-	-	-	-	-	-

4.3 DC Characteristic

4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

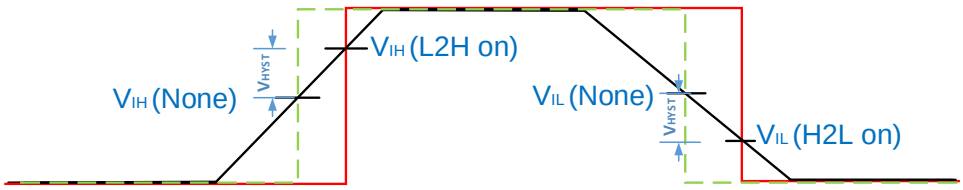
Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCIO}<V_{IN}<V_{IH}$ (MAX)	-	-	210 μA
		$0V<V_{IN}<V_{CCIO}$	-	-	10 μA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCIO}$	-30 μA	-	-150 μA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX)$<V_{IN}<V_{CCIO}$	30 μA	-	150 μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$ (MAX)	30 μA	-	-
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCIO}$	-30 μA	-	-
I_{BHLO}	Bus Hold Low Overdrive Current	$0\le V_{IN}\le V_{CCIO}$	-	-	150 μA
I_{BHHO}	Bus Hold High Overdrive Current	$0\le V_{IN}\le V_{CCIO}$	-	-	-150 μA
V_{BHT}	Bus hold trip points		V_{IL} (MAX)	-	V_{IH} (MIN)

Name	Description	Condition	Min.	Typ.	Max.
C1	I/O Capacitance			5 pF	8 pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis= L2H[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis= L2H	-	125mV	-
		V_{CCIO}=1.8V, Hysteresis= L2H	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis= L2H	-	40mV	-
		V_{CCIO}=1.2V, Hysteresis= L2H	-	20mV	-
		V_{CCIO}=3.3V, Hysteresis= H2L[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis= H2L	-	125mV	-
		V_{CCIO}=1.8V, Hysteresis= H2L	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis= H2L	-	40mV	-
		V_{CCIO}=1.2V, Hysteresis= H2L	-	20mV	-
		V_{CCIO}=3.3V, Hysteresis= HIGH[1],[2]	-	400mV	-
		V_{CCIO}=2.5V, Hysteresis= HIGH	-	250mV	-
		V_{CCIO}=1.8V, Hysteresis= HIGH	-	120mV	-
		V_{CCIO}=1.5V, Hysteresis= HIGH	-	80mV	-
		V_{CCIO}=1.2V, Hysteresis= HIGH	-	40mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see *SUG935, Gowin Design Physical Constraints User Guide*.
- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(L2H). The diagram is shown below.



4.3.2 Static Current

Table 4-9 Static Current

Device	Name	Description	LV/UV	C7/I6	C6/I5	C5/I4	Units
GW1N-1	I_{CC}	Core Current(V_{CC}=1.2V)	LV	2.5	1.8	1.5	mA
	I_{CCIO}	I/O Bank Current (V_{CCIO}=2.5V)	LV	1	0.8	0.6	mA
GW1N-2	I_{CC} + I_{CCX}	Core Current and V_{CCX} Current(Vccx=Vcc=3.3V)	UV	15	12	10	mA

Device	Name	Description	LV/UV	C7/I6	C6/I5	C5/I4	Units
	I_{CCIO}	I/O Bank Current (V_{CCIO}=2.5V)	UV	1.2	1	0.8	mA
	I_{CC}	Core Current (V_{CC}=1.2V)	LV	3	2.5	2.2	mA
	I_{CCX}	V_{CCX} Current (V_{CCX}=3.3V)	LV	1.5	0.75	0.6	mA
	I_{CCIO}	I/O Bank Current (V_{CCIO}=2.5V)	LV	0.6	0.5	0.4	mA
GW1N-1P5	I_{CC} + I_{CCX}	Core Current and V_{CCX} Current(Vccx=Vcc=3.3V)	UV	15	12	10	mA
	I_{CCIO}	I/O Bank Current (V_{CCIO}=2.5V)	UV	1.2	1	0.8	mA
	I_{CC}	Core Current (V_{CC}=1.2V)	LV	3	2.5	2.2	mA
	I_{CCX}	V_{CCX} Current(V_{CCX}=3.3V)	LV	1.5	0.75	0.6	mA
	I_{CCIO}	I/O Bank Current(V_{CCIO}=2.5V)	LV	0.6	0.5	0.4	mA
GW1N-4	I_{CC}	Core Current (V_{CC}=1.2V)	LV	3.4	2.8	2.4	mA
	I_{CC}	Core Current (V_{CC}=3.3V)	UV	20	18	16	mA
	I_{CCX}	V_{CCX} Current(V_{CCX}=3.3V)	LV/UV	1.4	0.9	0.7	mA
	I_{CCIO}	I/O Bank Current(V_{CCIO}=2.5V)	LV/UV	0.7	0.55	0.4	mA
GW1N-9	I_{CC}	Core Current(V_{CC}=1.2V)	LV	2.8	2.4	2	mA
	I_{CC}	Core Current(V_{CC}=3.3V)	UV	20	18	16	mA
	I_{CCX}	V_{CCX} Current(V_{CCX}=3.3V)	LV/UV	1.5	1.3	1	mA
	I_{CCIO}	I/O Bank Current(V_{CCIO}=2.5V)	LV/UV	0.9	0.7	0.5	mA

Note！

The values in Table 4-9 are the typical values at 25℃.

4.3.3 Programming Current

Table 4-10 Programming Current

Device	Description	LV/UV	Max.(mA)
GW1N-1	Core current when programming Flash (V_{CC}=1.2V)	LV	4.8
	I/O Bank current when programming Flash (V_{CCIO}=2.5V)	LV	2.8
GW1N-2	Core current when programming Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming Flash (V_{CCX}=3.3V)	LV	12
	I/O Bank current when programming Flash (V_{CCIO}=2.5V)	LV	2
GW1N-1P5	Core current when programming Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming Flash (V_{CCX}=3.3V)	LV	12
	I/O Bank current when programming Flash (V_{CCIO}=2.5V)	LV	2
GW1N-4	Core current when programming Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming Flash (V_{CCX}=3.3V)	LV	12
	I/O Bank current when programming Flash (V_{CCIO}=2.5V)	LV	2
GW1N-9	Core current when programming Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming Flash (V_{CCX}=3.3V)	LV	12
	I/O Bank current when programming Flash (V_{CCIO}=2.5V)	LV	2

Note!

The current value in Table 4-10 is the max. programming current at room temperature under normal atmospheric pressure

4.3.4 I/O Operating Conditions Recommended

Table 4-11 I/O Operating Conditions Recommended

Name	Output V_{CCIO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-

Name	Output V_{CCIO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.5	1.575	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

4.3.5 IOB Single - Ended DC Electrical Characteristic

Table 4-12 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCIO}	0.5 x V_{CCIO}	3.6V	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCIO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCIO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Note!

[1] The total DC current limit(sourced and sinked) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

4.3.6 IOB Differential Electrical Characteristics

Table 4-13 IOB Differential Electrical Characteristics

Name	Description	Condition	Min.	Typ.	Max.	Units
V_{INA},V_{INB}	Input Voltage		0	-	2.15	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	-	2.1	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±20	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristics

4.4.1 Internal Switching Characteristics

Table 4-14 CFU Block Internal Timing Parameters[1], [2]

Device	Name	Description	C7/I6		C6/I5		C5/I4		Units
			Min	Max	Min	Max	Min	Max	
GW1N-1	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns
GW1N-2/ GW1N-1P5	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns
GW1N-4	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns
GW1N-9	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns
GW1N-1S	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns

Note!

- [1] The min/max values are based on the rising edge delay.
- [2] LUT4 delay values are based on the delay of input port I3->F.

4.4.2 BSRAM Switching Characteristics

Table 4-15 BSRAM Internal Timing Parameters

Device	Name	Description	C7/I6		C6/I5		C5/I4		Units
			Min	Max	Min	Max	Min	Max	
GW1N-1	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns
GW1N-2/GW1N-1P5	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns
GW1N-4	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns
GW1N-9	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns
GW1N-1S	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns

Note!

t_{COAD_BSRAM} values refer to the delays in bypass mode.

4.4.3 DSP Switching Characteristics

Table 4-16 DSP Internal Timing Parameters

Device	Name	Description	C7/I6		C6/I5		C5/I4		Units
			Min	Max	Min	Max	Min	Max	
GW1N-1	t_{COIR_DSP}	Clock to output time of input register	0.219	0.239	0.295	0.318	0.369	0.398	ns

Device	Name	Description	C7/I6		C6/I5		C5/I4		Units
			Min	Max	Min	Max	Min	Max	
	t_{COPR_DSP}	Clock to output time of pipeline register	0.063	0.075	0.085	0.101	0.106	0.127	ns
	t_{COOR_DSP}	Clock to output time of output register	0.034	0.038	0.046	0.052	0.057	0.065	ns
GW1N-2/GW1N-1P5	t_{COIR_DSP}	Clock to output time of input register	0.219	0.239	0.295	0.318	0.369	0.398	ns
	t_{COPR_DSP}	Clock to output time of pipeline register	0.063	0.075	0.085	0.101	0.106	0.127	ns
	t_{COOR_DSP}	Clock to output time of output register	0.034	0.038	0.046	0.052	0.057	0.065	ns
GW1N-4	t_{COIR_DSP}	Clock to output time of input register	0.219	0.239	0.295	0.318	0.369	0.398	ns
	t_{COPR_DSP}	Clock to output time of pipeline register	0.063	0.075	0.085	0.101	0.106	0.127	ns
	t_{COOR_DSP}	Clock to output time of output register	0.034	0.038	0.046	0.052	0.057	0.065	ns
GW1N-9	t_{COIR_DSP}	Clock to output time of input register	0.219	0.239	0.295	0.318	0.369	0.398	ns
	t_{COPR_DSP}	Clock to output time of pipeline register	0.063	0.075	0.085	0.101	0.106	0.127	ns
	t_{COOR_DSP}	Clock to output time of output register	0.034	0.038	0.046	0.052	0.057	0.065	ns
GW1N-1S	t_{COIR_DSP}	Clock to output time of input register	0.219	0.239	0.295	0.318	0.369	0.398	ns
	t_{COPR_DSP}	Clock to output time of pipeline register	0.063	0.075	0.085	0.101	0.106	0.127	ns
	t_{COOR_DSP}	Clock to output time of output register	0.034	0.038	0.046	0.052	0.057	0.065	ns

4.4.4 Gearbox Switching Characteristics

Table 4-17 Gearbox Internal Timing Parameters

Device	Name	Description	C7/I6		C6/I5		C5/I4		Units
			Min	Max	Min	Max	Min	Max	
GW1N-1/4/9	$FMAX_{IDDR}$	2:1 Gearbox maximum input serial rate	-	600	-	550	-	500	Mbps
	$FMAX_{IDES4}$	4:1 Gearbox maximum input serial rate	-	800	-	750	-	700	Mbps
	$FMAX_{IDESx}$	8:1/10:1 Gearbox maximum input serial rate	-	1000	-	900	-	800	Mbps
	$FMAX_{ODDR}$	1:2 Gearbox maximum input serial rate	-	600	-	550	-	500	Mbps
	$FMAX_{OSER4}$	1:4 Gearbox maximum output serial rate	-	800	-	750	-	700	Mbps
	$FMAX_{OSERx}$	1:8/1:10 Gearbox maximum output serial rate	-	1000	-	900	-	800	Mbps
GW1N-1P5/2	$FMAX_{IDDR}$	2:1 Gearbox maximum input serial rate	-	600	-	550	-	500	Mbps
	$FMAX_{IDES4}$	4:1 Gearbox maximum input serial rate	-	900	-	800	-	700	Mbps
	$FMAX_{IDESx}$	8:1/10:1 Gearbox maximum input serial rate	-	1200	-	1000	-	900	Mbps
	$FMAX_{ODDR}$	1:2 Gearbox maximum input serial rate	-	600	-	550	-	500	Mbps
	$FMAX_{OSER4}$	1:4 Gearbox maximum output serial rate	-	900	-	800	-	700	Mbps
	$FMAX_{OSERx}$	1:8/1:10 Gearbox maximum output serial rate	-	1200	-	1000	-	900	Mbps

Note!

- LVDS IO speed can be up to 1Gbps, but note that for 1:4 Gearbox and 1:2 Gearbox, the internal core may not reach the corresponding speed.
- Driver=3.5 mA.

Table 4-18 Single-ended IO Fmax

Name	Fmax	
	Min. Value(Mhz)	
	DriverStrength = 4mA	DriverStrength > 4mA
LVTTL33	150	300
LVCMOS33	150	300
LVCMOS25	150	300
LVCMOS18	150	300
LVCMOS15	150	200
LVCMOS12	150	150

Note!

The test loading is 30pF capacitor.

4.4.5 Clock and I/O Switching Characteristics

Table 4-19 External Switching Characteristics

Device	Name	C7/I6	C6/I5	C5/I4	Units
		Typ.	Typ.	Typ.	
GW1N-1	HCLK Tree delay	1	1.2	1.4	ns
	PCLK Tree delay(GCLK0~5)	2.2	2.4	2.6	ns
	PCLK Tree delay(GCLK6~7)	2.4	2.7	2.9	ns
	Pin-LUT-Pin Delay	4	4.3	4.6	ns
GW1N-1P5	HCLK Tree delay	0.6	0.8	1.1	ns
	PCLK Tree delay(GCLK0~5)	1.8	2.1	2.4	ns
	PCLK Tree delay(GCLK6~7)	2.1	2.5	2.8	ns
	Pin-LUT-Pin Delay	2.5	3	3.5	ns
GW1N-2	HCLK Tree delay	0.6	0.8	1.1	ns
	PCLK Tree delay(GCLK0~5)	1.8	2.1	2.4	ns
	PCLK Tree delay(GCLK6~7)	2.1	2.5	2.8	ns
	Pin-LUT-Pin Delay	2.5	3	3.5	ns
GW1N-4	HCLK Tree delay	0.8	1	1.2	ns
	PCLK Tree delay(GCLK0~5)	2	2.2	2.5	ns

Device	Name	C7/I6	C6/I5	C5/I4	Units
		Typ.	Typ.	Typ.	
	PCLK Tree delay(GCLK6~7)	2.2	2.5	2.8	ns
	Pin-LUT-Pin Delay	4	4.2	4.5	ns
GW1N-9	HCLK Tree delay	0.8	1	1.2	ns
	PCLK Tree delay(GCLK0~5)	2	2.2	2.5	ns
	PCLK Tree delay(GCLK6~7)	2.2	2.5	2.8	ns
	Pin-LUT-Pin Delay	4	4.2	4.5	ns
GW1N-1S	HCLK Tree delay	0.9	1.1	1.3	ns
	PCLK Tree delay(GCLK0~5)	2.1	2.4	2.6	ns
	PCLK Tree delay(GCLK6~7)	2.3	2.6	2.8	ns
	Pin-LUT-Pin Delay	4.1	4.3	4.6	ns

4.4.6 On chip Oscillator Switching Characteristics

Table 4-20 On chip Oscillator Output Frequency

Name	Description		Min.	Typ.	Max.
f_{MAX}	On chip Oscillator Output Frequency (0 ~ +85℃)	GW1N-4	97.25MHz	105MHz	112.85MHz
		GW1N-1/1S	114MHz	120MHz	126MHz
		GW1N-1P5/2/9	118.75MHz	125MHz	131.25MHz
	On chip Oscillator Output Frequency (-40 ~ +100℃)	GW1N-4	91.85MHz	105MHz	118.25MHz
		GW1N-1/1S	108MHz	120MHz	132MHz
		GW1N-1P5/2/9	112.5MHz	125MHz	137.5MHz
t_{DT}	Clock Duty Cycle		43%	50%	57%
t_{OPJIT}	Clock Period Jitter		0.01 UIPP	0.012 UIPP	0.02 UIPP

4.4.7 PLL Switching Characteristics

Table 4-21 PLL Parameters

Device	Speed Grade	Parameter	Min.	Max.	Units
GW1N-1		CLKIN	3	400	MHz

Device	Speed Grade	Parameter	Min.	Max.	Units
	C7/I6	PFD	3	400	MHz
		VCO	400	900	MHz
		CLKOUT	3.125	450	MHz
	C6/I5	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	900	MHz
		CLKOUT	3.125	450	MHz
	C5/I4	CLKIN	3	320	MHz
		PFD	3	320	MHz
		VCO	320	720	MHz
		CLKOUT	2.5	360	MHz
GW1N-1S	C7/I6	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	1200	MHz
		CLKOUT	3.125	600	MHz
	C6/I5	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	1200	MHz
		CLKOUT	3.125	600	MHz
	C5/I4	CLKIN	3	320	MHz
		PFD	3	320	MHz
		VCO	320	960	MHz
		CLKOUT	2.5	480	MHz
GW1N-4 GW1N-9	C7/I6	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	1000	MHz
		CLKOUT	3.125	500	MHz
	C6/I5	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	1000	MHz
		CLKOUT	3.125	500	MHz
	C5/I4	CLKIN	3	320	MHz
		PFD	3	320	MHz

Device	Speed Grade	Parameter	Min.	Max.	Units
		VCO	320	800	MHz
		CLKOUT	2.5	400	MHz
GW1N-1P5 GW1N-2	C7/I6	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	800	MHz
		CLKOUT	3.125	800	MHz
	C6/I5	CLKIN	3	400	MHz
		PFD	3	400	MHz
		VCO	400	800	MHz
		CLKOUT	3.125	800	MHz
	C5/I4	CLKIN	3	320	MHz
		PFD	3	320	MHz
		VCO	320	640	MHz
		CLKOUT	2.5	640	MHz

Note!

[1] The min. output frequency for different channels may be different. The min. output frequency for channel A is VCO/128, which is 3.125MHz/2.5MHz; Channel B/C/D needs to be judged aCCIOrding to whether it is cascaded (parameter). If it is not cascaded, it is the same as channel A; if it is cascaded, it needs to be divided by 128 again.

4.5 User Flash Characteristics

4.5.1 DC Characteristics

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 4-22 GW1N-1/ GW1N-1S User Flash DC Characteristics

Name	Description	Spec.			Unit
		Min.	Typ.	Max.	
Tj	Junction Temperature	-40	25	100	℃
Ilkg	Leakage current	-	-	1[1]	μA
Isb	Standby current	-	-	3(Ta=25)	μA
		-	-	20(Ta=85)	
Icc0	Idle current	-	-	1.3	mA
Icc1	Read operation current	-	-	2(Rmod=00)	mA
		-	-	2.5(Rmod=01)	mA
		-	-	3(Rmod=00)	mA
Icc2	Page write current	-	-	2	mA
Icc3	programming/ erasing current	-	-	3	mA

Note!

[1] The leakage current of Flash is included in the leakage current of the device, see Table 4-4 Hot Socket Specifications.

Table 4-23 GW1N-2/4/9 User Flash DC Characteristics(I)

Name	Description	Spec.			Unit
		Min.	Typ.	Max.	
Tj	Junction Temperature	-40	25	125	℃

Table 4-24 GW1N-2/4/9 User Flash DC Characteristics(II)[4]

Name	Param-eter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode (w/I 25ns)[1]	I_{CC1}[2]	2.19	0.5	mA	NA	Min. Clock period, duty cycle 100%, VIN = “1/0”
Write mode		0.1	12	mA	NA	
Erase mode		0.1	12	mA	NA	
Page Erasure Mode		0.1	12	mA	NA	

Name	Param-eter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode static current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE="1",between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Note!

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Calculated in different T_{new} clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - T_{new}>50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns x I_{CC2}/T_{new} + I_{SB}
  - t > 50ns, $I_{CC2} = I_{SB}$
- [3] V_{CC} must be greater than 1.08V from the zero wake-up time.
- [4] The leakage current of Flash is included in the leakage current of the device, see Table 4-4 Hot Socket Specifications.

4.5.2 Timing Parameters[1],[5],[6]

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 4-25 GW1N-1/GW1N-1S User Flash Timing Parameters

Name	Description	Spec.			Unit
		Min.	Normal	Max.	
Taa	Data acquisition time	-	-	38	ns
Tcy	Read cycle	43	-	-	ns
Taw	Aclk high-level time	10	-	-	ns
Tawl	Aclk low-level time	10	-	-	ns
Tas	Setup time	3	-	-	ns
Tah	Hold-up time	3	-	-	ns
Toz	Oe down to high resistance	-	-	2	ns
Toe	Oe up to Dout	-	-	2	ns
Twcy	Write cycle	40	-	-	ns
Tpw	Pw high-level time	16	-	-	ns
Tpwl	Pw low-level time	16	-	-	ns
Tpas	Page address set up time	3	-	-	ns
Tpah	Page address hold-up time	3	-	-	ns
Tds	Data set up time	16	-	-	ns
Tdh	Data hold-up time	3	-	-	ns

Name	Description	Spec.			Unit
		Min.	Normal	Max.	
Ts0	Seq0 cycle	6	-	-	μs
Ts1	Seq1 cycle	15	-	-	μs
Ts2p	Set up time from Aclk to Pe rising edge	5	-	10	μs
Ts3	Seq3 cycle	5	-	10	μs
Tps3	Set up time from Pe falling edge to Aclk	60	-	-	μs
Tpe	Mode=1000 erasure time	5.7	6	6.3	ms
	Mode=1100 programming time	1.9	2	2.1	ms
	Mode=11xx preprogramming time	190	200	210	us

Table 4-26 GW1N-1P5/2/4/9 User Flash Timing Parameters

User Modes	Parameter	Name	Min.	Max.	Unit
Access time[2]	WC1	T_{acc}[3]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs
Data storage hold time (Overall erase)		T_{nvh1}	100	-	μs
Time from data storage to program setup		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Program time		T_{prog}	8	16	μs
Write ready time		T_{wpr}	>0	-	ns
Erase hold time		T_{whd}	>0	-	ns
Time from control signal to write/Erase setup		T_{cps}	-10	-	ns
Time from SE to read setup		T_{as}	0.1	-	ns
SE pulse high level time		T_{pws}	5	-	ns
Address/data setup time		T_{ads}	20	-	ns
Address/data hold time		T_{adh}	20	-	ns
Data hold-up time		T_{dh}	0.5	-	ns
Read mode address hold time[3]	WC1	T_{ah}	25	-	ns
	TC	-	22	-	ns

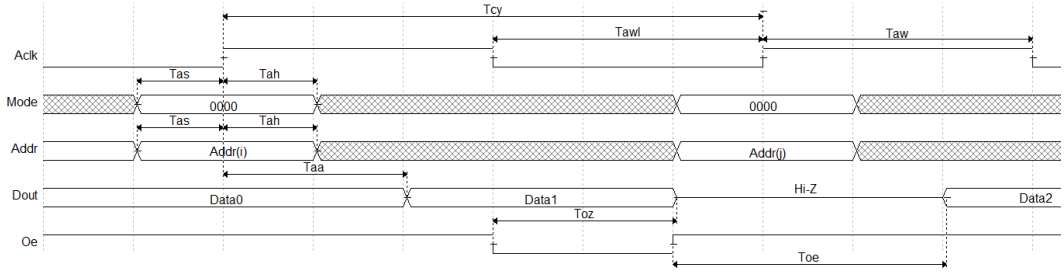
User Modes	Parameter	Name	Min.	Max.	Unit
	BC	-	21	-	ns
	LT	-	21	-	ns
	WC	-	25	-	ns
SE pulse low level time		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[4]	-	6	ms
Erasure time		T_{erase}	100	120	ms
Overall erase time		T_{me}	100	120	ms
Wake-up time from power down to standby mode		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

Note!

- [1] The parameter values may change;
- [2] The values are simulation data only.
- [3]After XADR, YADR, XE, and YE are valid, T_{acc} start time is SE rising edge. DOUT is kept until the next valid read operation;
- [4]T_{hv} is the time between write and the next erasure. The same address cannot be written twice before erasure, so does the same register. This limitation is for safety;
- [5]Both the rising edge time and falling edge time for all waveform is 1ns;
- [6] TX, YADR, XE, and YE hold time need to be T_{acc} at least, and T_{acc} starts from SE rising edge.

4.5.3 Operation Timing Diagrams (GW1N-1/ GW1N-1S)

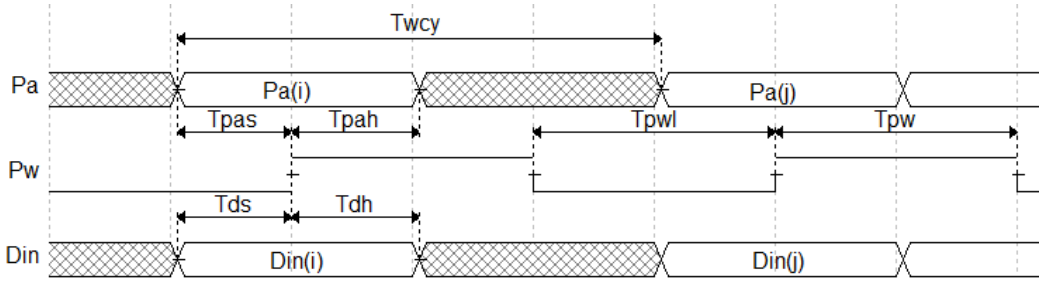
Figure 4-1 Read Mode



Note!

Read operation cycle Seq=0, Addr signal contains Ra, Ca, Rmod, and Rbytesel.

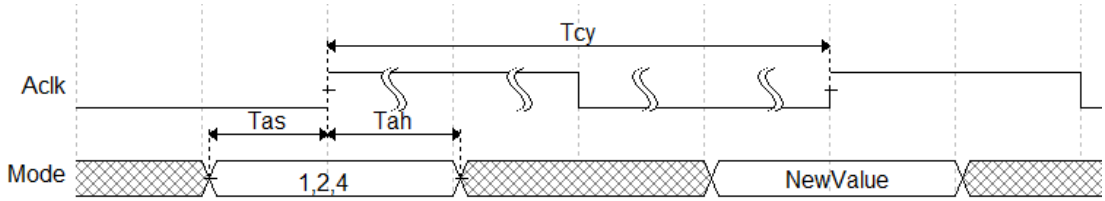
Figure 4-2 Write Page Latches Mode



Note!

Write Page Latches Cycle Seq=0, Mode=0000.

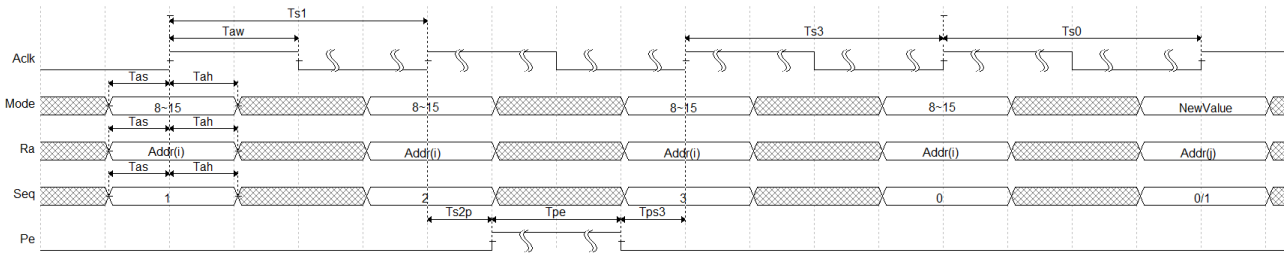
Figure 4-3 Clear Page Latches Mode



Note!

The timing parameters of Setting PEP, writing to all pages, and clearing page latches are all the same. The MODE values are different.

Figure 4-4 High Level Cycle



4.5.4 Operation Timing Diagrams (GW1N-1P5/2/4/9)

Figure 4-5 User Flash Read Operation

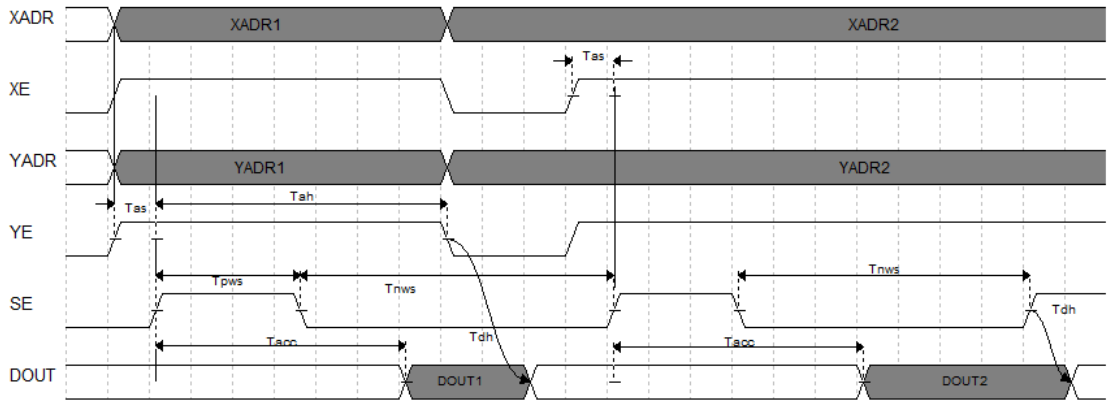


Figure 4-6 User Flash Program Operation

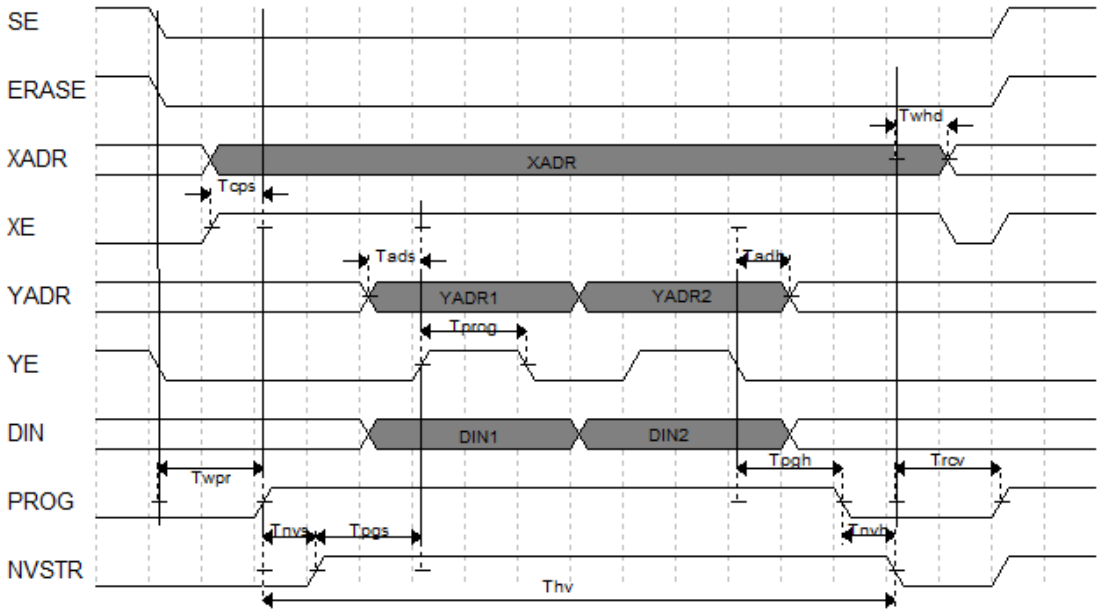
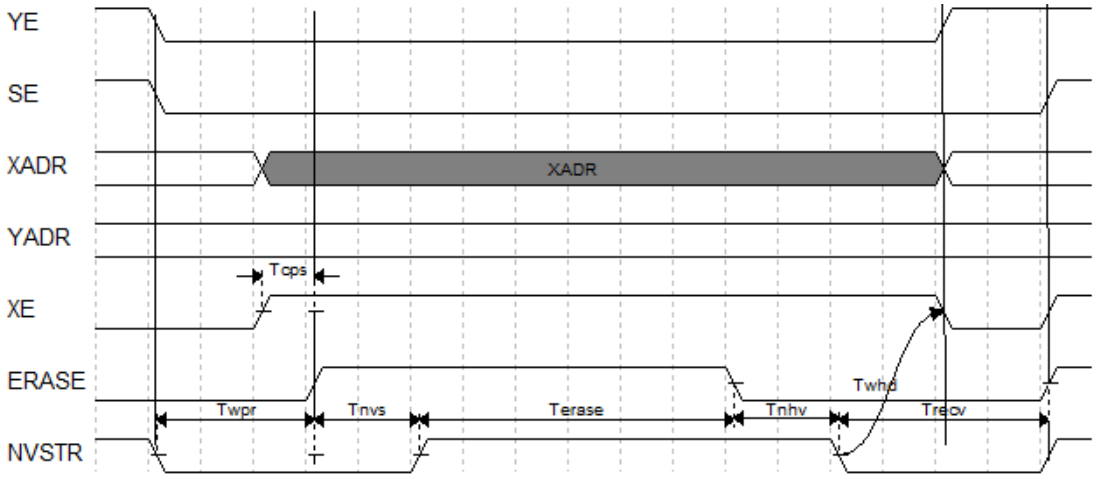


Figure 4-7 User Flash Erase Operation



4.6 Configuration Interface Timing Specification

The GW1N series of FPGA products support seven GowinCONFIG modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, CPU, and I²C Slave. For more detailed information, please refer to *UG290, Gowin FPGA Products Programming and Configuration User Guide*.

5 Ordering Information

5.1 Part Name

Note!

- GW1N-1S parts support LV only;
- For the further detailed information about the package information, please refer to 2.2 Product Resources and 2.3 Package Information.

Figure 5-1 Part Naming–ES

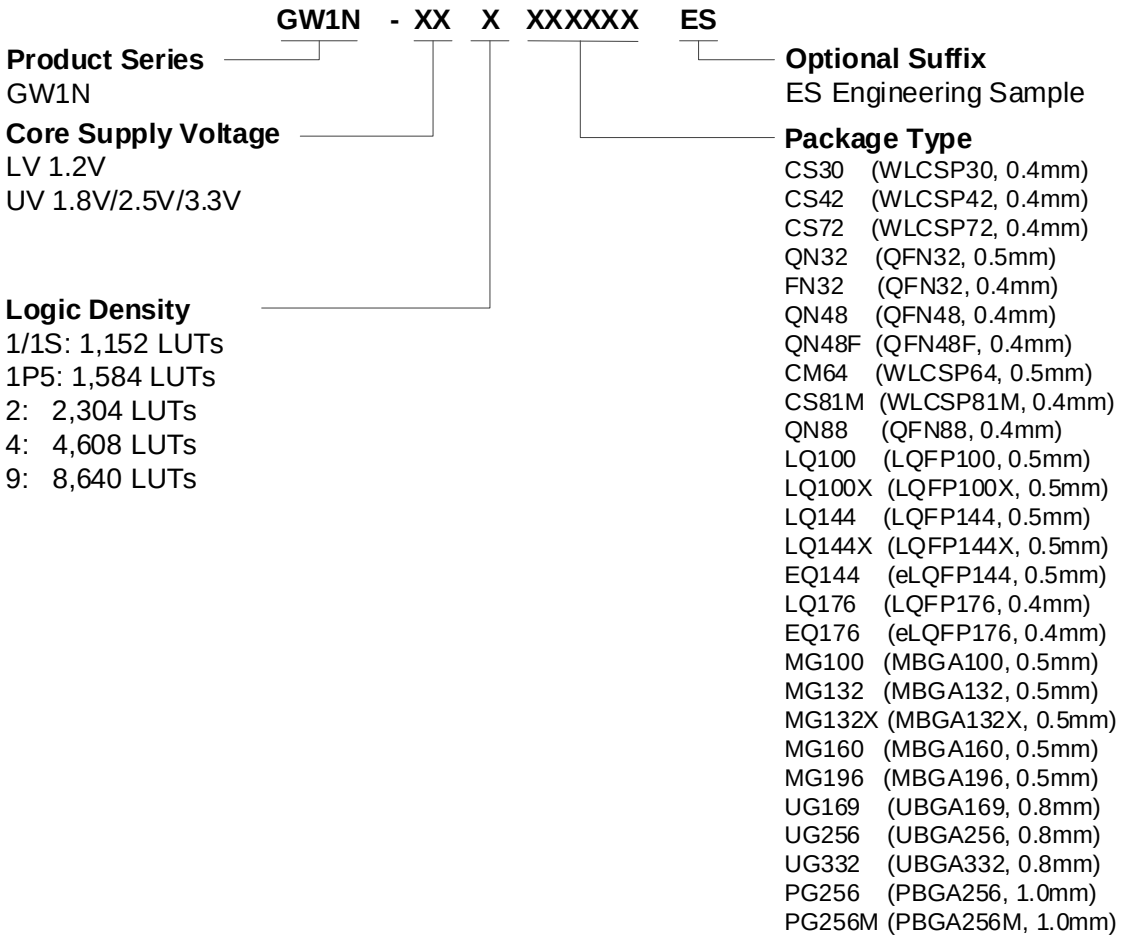
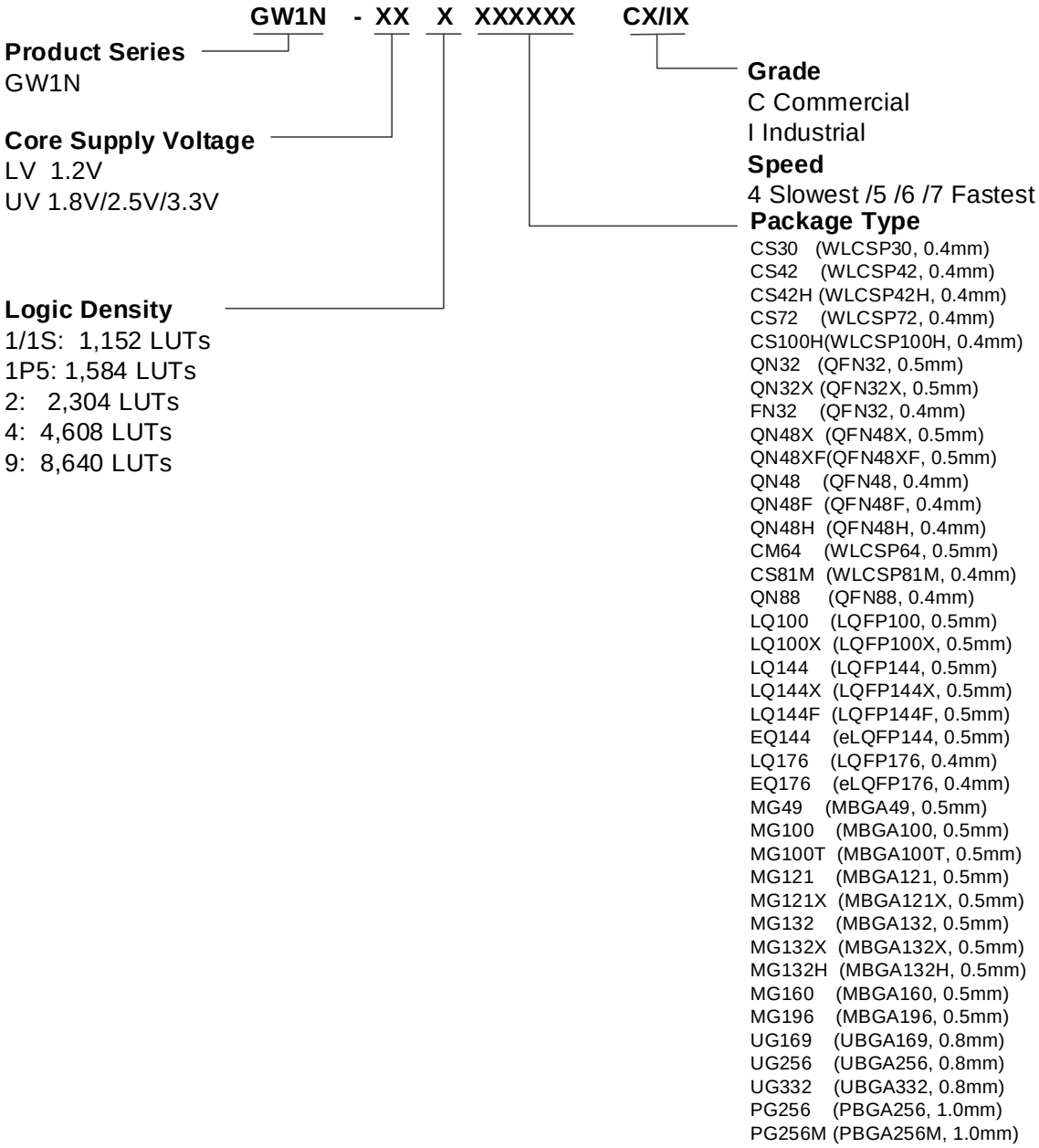


Figure 5-2 Part Naming–Production



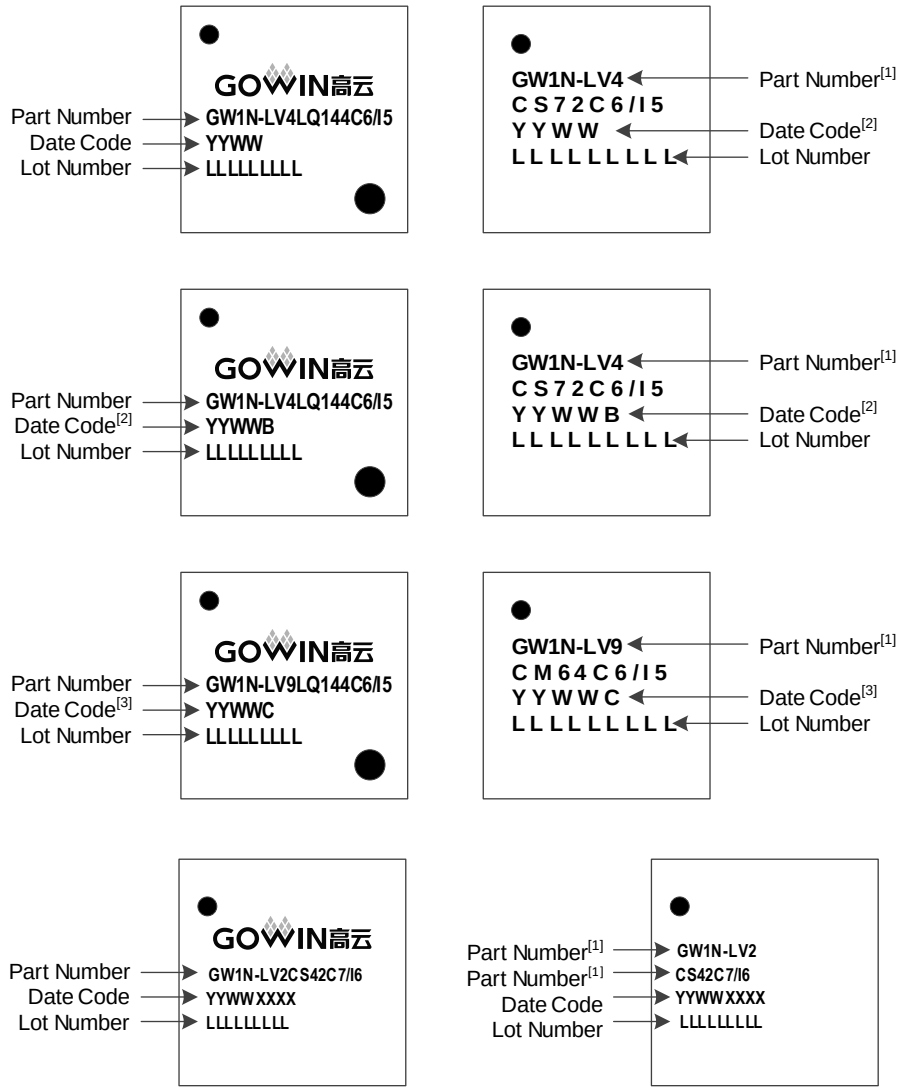
Note!

- The LittleBee® family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in GOWIN part name marking for one device. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the same chip meets the speed grade 7 in the commercial grade application, the speed grade is 6 in the industrial grade application.

5.2 Package Mark

The device information is marked on the chip surface, as shown in Figure 5-3.

Figure 5-3 Package Mark



Note!

- [1] The first two lines in the right figure above are the “Part Number”
- [2] The Date Code followed by a “B” is for B version devices.
- [3] The Date Code followed by a “C” is for C version devices.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