



GW1N series of FPGA Products

Package & Pinout User Guide

UG103-2.8.3E, 12/20/2022

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Revision History

Date	Version	Description
03/03/2016	1.05E	Initial version.
04/16/2020	2.0E	GW1N-2/GW1N-2B/GW1N-6 removed.
07/08/2020	2.1E	<ul style="list-style-type: none"> ● GW1N-9 MG100 added. ● GW1N-9 QN48F added.
07/30/2020	2.1.1E	<ul style="list-style-type: none"> ● "Table 3-67 Other Pins in GW1N-9 UG332" updated; ● View of GW1N-9 QN48F Pins Distribution added.
12/31/2020	2.2E	The new device of GW1N-2 added.
01/22/2021	2.2.1E	GW1N-2 QN48/QN48M added.
03/02/2021	2.2.2E	GW1N-2 MG132 added.
04/19/2021	2.3E	The new device of GW1N-1P5 added.
05/20/2021	2.4E	<ul style="list-style-type: none"> ● GW1N-1P5 LQ100 added; ● GW1N-2 MG132/LQ100/LQ144 added, and MG132 renamed to MG132H, QN48M renamed to QN48H. ● GW1N-9 MG100T added; ● GW1N-1 LQ100X removed.
07/16/2021	2.4.1E	GW1N-2 MG121/MG121X added.
08/26/2021	2.4.2E	EQ144 and EQ176 package outlines updated.
10/28/2021	2.5E	<ul style="list-style-type: none"> ● GW1N-2 MG49 and GW1N-1P5 FN48X added; ● GW1N-1 QN32, QN48, LQ100, and LQ144 removed.
01/20/2022	2.6E	<ul style="list-style-type: none"> ● GW1N-2 QN32X, QN88, and CS42H added; ● GW1N-1P5 FN48X removed; GW1N-1P5 QN48X added.
05/19/2022	2.7E	<ul style="list-style-type: none"> ● GW1N-4 UG169 package added; ● GW1N-2 CS42H package updated.
06/02/2022	2.7.1E	GW1N-1 QN32, QN48, LQ100, and LQ144 added.
06/23/2022	2.7.2E	GW1N-1 CS30/FN32 removed.
07/21/2022	2.8E	<ul style="list-style-type: none"> ● GW1N-1 CS30 added; ● GW1N-2 QN32, CS100H, and GW1N-2 LQ144F added; ● The units in the package outlines unified to millimeters; ● Note about thickness of QN88 package added.
08/08/2022	2.8.1E	GW1N-9 QN48/QN48F package outline added.
08/18/2022	2.8.2E	<ul style="list-style-type: none"> ● Pin information for GW1N-2 QN32 and QN32X packages updated. ● GW1N-1S CS30/FN32 removed. ● GW1N-1 QN32, QN48, LQ100, and LQ144 removed.
12/20/2022	2.8.3E	<ul style="list-style-type: none"> ● GW1N-1P5 QN48X package added. ● QN32X package and GW1N-2 QN32 package updated.

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1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1N series of FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guidelines are available on GOWINSEMI website at www.gowinsemi.com:

1. [UG290, Gowin FPGA Products Programming and Configuration User Guide](#)
2. [DS100, GW1N series of FPGA Products Datasheet](#)
3. [UG107, GW1N-1 Pinout](#)
4. [UG167, GW1N-1S Pinout](#)
5. [UG171, GW1N-2 Pinout](#)
6. [UG105, GW1N-4 Pinout](#)
7. [UG114, GW1N-9 Pinout](#)
8. [UG174, GW1N-1P5 Pinout](#)

1.3 Abbreviations and Terminology

The abbreviations and terminologies that are used in this manual are described in Table 1-1.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
CS	WLCSP
QN	QFN
FN	QFN
CM	WLCSP
MG	MBGA
LQ	LQFP
EQ	ELQFP
PG	PBGA256
UG	UBGA

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly via the following channels.

Website: www.gowinsemi.com

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2 Overview

The GW1N series of FPGA Products are the first-generation products of GOWINSEMI® (LittleBee®) family. They are available in various forms that offer high I/O compatibility and flexible usage.

2.1 PB-Free Package

The GW1N series of FPGA products are PB free in line with the EU RoHS environmental directives. The substances used in the GW1N series of FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package and Max. User I/O Information

Table 2-1 Package and Max. User I/O Information, and LVDS Pairs

Package	Pitch(mm)	Size(mm)	Max. User I/O (LVDS Pairs)					
			GW1N-1S	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
CS30	0.4	2.3 x 2.4	-	24	-	-	-	-
QN32	0.5	5 x 5	-	-	-	21 (1)	24 (3)	-
QN32X	0.5	5 x 5	-	-	-	21 (1)	-	-
FN32	0.4	4 x 4	-	-	-	-	-	-
CS42	0.4	2.4 x 2.9	-	-	-	24 (7)	-	-
CS42H	0.4	2.4 x 2.9	-	-	-	36 (3)	-	-
QN48	0.4	6 x 6	-	-	-	40 (12)	40 (9)	40 (12)
QN48H	0.4	6 x 6	-	-	-	30 (8)	-	-
QN48F	0.4	6 x 6	-	-	-	-	-	39 (11)
QN48X	0.5	7 x 7	-	-	39 (10)	-	-	-
QN48XF	0.5	7 x 7	-	-	40 (11)	-	-	-
CM64	0.5	4.1 x 4.1	-	-	-	-	-	55 (16)
CS72	0.4	3.6 x 3.3	-	-	-	-	57 (19)	-
CS81M	0.4	4.1 x 4.1	-	-	-	-	-	55 (15)
QN88	0.4	10 x 10	-	-	-	57 (17)	70 (11)	70 (19)
CS100H	0.4	4 x 4	-	-	-	88 (27)	-	-
LQ100	0.5	14 x 14	-	-	80 (16)	80 (15)	79 (13)	79 (20)

Package	Pitch(mm)	Size(mm)	Max. User I/O (LVDS Pairs)					
			GW1N-1S	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
LQ100X	0.5	14 x 14	-	-	80 (16)	80 (15)	-	-
MG49	0.5	3.8 x 3.8	-	-	-	42 (11)	-	-
MG100	0.5	5 x 5	-	-	-	-	-	87 (25)
MG100T	0.5	5 x 5	-	-	-	-	-	87 (17)
MG121	0.5	6 x 6	-	-	-	100 (28)	-	-
MG121X	0.5	6 x 6	-	-	-	100 (28)	-	-
MG132	0.5	8 x 8	-	-	-	104 (29)	-	-
MG132H	0.5	8 x 8	-	-	-	94 (29)	-	-
MG132X	0.5	8 x 8	-	-	-	104 (29)	105 (23)	-
LQ144	0.5	20 x 20	-	-	-	113 (28)	119 (22)	120 (28)
LQ144X	0.5	20 x 20	-	-	-	113 (28)	-	-
LQ144F	0.5	20 x 20	-	-	-	115 (27)	-	-
EQ144	0.5	20 x 20	-	-	-	-	-	120 (28)
MG132X	0.5	8 x 8	-	-	-	-	105 (23)	-
MG160	0.5	8 x 8	-	-	-	-	131 (25)	131 (38)
UG169	0.8	11 x 11	-	-	-	-	129 (27)	129 (38)
LQ176	0.4	20 x 20	-	-	-	-	-	147 (37)
EQ176	0.4	20 x 20	-	-	-	-	-	147 (37)
MG196	0.5	8 x 8	-	-	-	-	-	113 (35)
PG256	1.0	17 x 17	-	-	-	-	207 (32)	207 (36)
PG256M	1.0	17 x 17	-	-	-	-	207 (32)	-
UG256	0.8	14 x 14	-	-	-	-	-	207 (36)
UG332	0.8	17 x 17	-	-	-	-	-	273 (43)

Note!

- In this manual, abbreviations are employed to refer to the package types. See section 1.3 Abbreviations and Terminology;
- The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. The table shows the data when the four JTAG mode pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O is increased by one.

2.3 Dedicated Pins

Table 2-2 GW1N Pins

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCIO4	VCCIO5	VCCX
VSS	NC		

2.4 Pin Quantity

2.4.1 Quantity of GW1N-1 Pins

Table 2-3 Quantity of GW1N-1 Pins

Pin Type		
	GW1N-1	CS30
I/O Single ended/Differential pair ^[1]	BANK0	0/0
	BANK1	10/4
	BANK2	2/1
	BANK3	11/5
Max. User I/O ^[2]	24	
Differential Pair	10	
VCC	1	
VCCIO0	0	
VCCIO1	0	
VCCIO2	0	
VCCIO3	0	
VCCIO0/VCCIO3 ^[3]	1	
VCCIO1/VCCIO2 ^[3]	2	
VSS	2	
MODE0	1	
MODE1	0	
MODE2	0	
JTAGSEL_N	0	
NC	0	

Note!

- [1]The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2]The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3]Pin multiplexing.

2.4.2 Quantity of GW1N-2 Pins

Table 2-4 Quantity of GW1N-2 Pins

Pin Type		GW1N-2																	
		CS42	MG132X ^[4]	MG132X ^[5]	LQ100X ^[4]	LQ100X ^[5]	LQ144X ^[4]	LQ144X ^[5]	QN48	QN48H	MG132H ^[4]	MG132H ^[5]	MG132X ^[4]	MG121X ^[4]	MG121X ^[5]	MG121X ^[4]	MG121X ^[5]	MG49	
Single-ended I/O /Differential pair/LVDS ^[1]	BANK0	6/3/1	25/12/7	25/12/7	19/8/4	19/8/4	28/13/7	28/13/7	10/4/1	12/5/2	25/11/7	25/12/7	25/12/7	24/11/7	24/11/7	24/11/7	24/11/7	14/7/4	
	BANK1	0/0/0	26/13/7	26/13/7	21/10/3	21/10/3	28/14/7	28/14/7	10/5/5	0/0/0	16/8/7	26/13/7	26/13/7	26/13/7	26/13/7	26/13/7	26/13/7	12/6/3	
	BANK2	6/3/0	28/14/8	28/14/8	20/10/3	20/10/3	29/14/7	29/14/7	8/4/1	28/14/8	28/14/8	28/14/8	26/12/7	26/12/7	26/12/7	26/12/7	8/4/2		
	BANK3	4/2/2	7/3/2	7/3/2	6/3/2	6/3/2	8/4/2	8/4/2	4/2/2	4/2/2	7/3/2	7/3/2	7/3/2	7/3/2	7/3/2	7/3/2	4/2/1		
	BANK4	2/1/1	8/4/2	8/4/2	6/3/1	6/3/1	10/5/2	10/5/2	2/1/1	2/1/1	8/4/2	8/4/2	8/4/2	7/3/2	7/3/2	7/3/2	4/2/1		
	BANK5	6/3/3	10/5/3	10/5/3	8/4/2	8/4/2	10/5/3	10/5/3	6/3/2	4/2/2	10/5/3	10/5/3	10/5/3	10/5/3	10/5/3	10/5/3	0/0/0		
Max. User I/O ^[2]		24	104	104	80	80	113	113	40	30	94	104	104	100	100	100	100	42	
Differential Pair		17	51	51	38	38	55	55	19	19	45	51	51	47	47	47	47	21	
True LVDS Output		7	29	29	15	15	28	28	12	8	29	29	29	28	28	28	28	11	
VCC		1	0	4	0	2	0	4	1	0	4	4	0	4	0	4	0	1	
VCCIO0		0	3	3	2	2	3	3	1	1	3	3	3	1	1	1	1	1	
VCCIO1		0	3	0	2	0	3	0	1	0	2	0	3	0	1	0	1	1	
VCCIO2		0	3	3	2	2	3	3	0	0	3	3	3	1	1	1	1	0	
VCCIO3		0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0	
VCCIO4		0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0	
VCCIO5		0	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	0	
VCCX		1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	
VCC/VCCX		0	4	0	2	0	4	0	0	0	0	0	4	0	4	0	4	0	
VCC/VCCIO1		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
VCCIO1/VCCX		0	0	3	0	2	0	3	0	0	0	3	0	1	0	1	0	0	
VCCIO2/VCCX		0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	

Pin Type	GW1N-2																
	CS42	MG132X ^[4]	MG132X ^[5]	LQ100X ^[4]	LQ100X ^[5]	LQ144X ^[4]	LQ144X ^[5]	QN48	QN48H	MG132H	MG132 ^[4]	MG132 ^[5]	MG121X ^[4]	MG121X ^[5]	MG121 ^[4]	MG121 ^[5]	MG49
VCCIO2/VCCIO3/VCCIO4/VCCIO5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
VCCD/VCCIO1/VCCIOD	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VCCD/VCCIOD	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
VCCIO3/VCCIO4/VCCIO5	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
VCCIO0/VCCIO2 ^[3]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VSS	2	10	10	8	8	12	12	2	2	10	10	10	10	10	10	10	2
MODE0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
MODE1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MODE2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
JTAGSEL_N	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NC	0	1	1	0	0	2	2	0	0	0	1	1	0	0	0	0	0

Continued

Pin Type		GW1N-2									
		QN32X ^[4]	QN32X ^[5]	QN32 ^[4]	QN32 ^[5]	QN88 ^[4]	QN88 ^[5]	CS42H	CS100H	LQ144F ^[4]	LQ144F ^[5]
Single-ended I/O /Differential pair/LVDS ^[1]	BANK0	8/3/0	8/3/0	8/3/0	8/3/0	19/9/5	19/9/5	12/3/0	26/11/6	28/13/7	28/13/7
	BANK1	2/1/1	2/1/1	2/1/1	2/1/1	5/2/1	5/2/1	6/3/3	17/8/7	29/14/6	29/14/6
	BANK2	9/4/0	9/4/0	9/4/0	9/4/0	18/9/4	18/9/4	12/0/0	23/11/7	29/14/7	29/14/7
	BANK3	2/1/0	2/1/0	2/1/0	2/1/0	5/2/2	5/2/2	2/0/0	7/3/2	9/4/2	9/4/2
	BANK4	0/0/0	0/0/0	0/0/0	0/0/0	4/2/2	4/2/2	2/0/0	8/4/2	10/5/2	10/5/2
	BANK5	0/0/0	0/0/0	0/0/0	0/0/0	6/3/3	6/3/3	2/0/0	6/3/3	10/5/3	10/5/3
Max. User I/O ^[2]		21	21	21	21	57	57	36	88	115	115
Differential Pair		9	9	9	9	27	27	6	40	55	55
True LVDS Output		1	1	1	1	17	17	3	27	27	27
VCC		0	0	0	0	4	4	1	0	4	0
VCCIO0		0	2	0	2	2	2	1	1	3	3
VCCIO1		1	1	1	1	1	1	1	1	0	3
VCCIO2		2	2	2	2	2	2	1	1	3	3
VCCIO3		1	1	1	1	1	1	0	1	1	1
VCCIO4		0	0	0	0	1	1	0	1	1	1
VCCIO5		0	0	0	0	1	1	0	1	1	1
VCC/VCCX		0	0	0	0	0	0	0	0	0	4
VCC/VCCIO4/VCCIO5		2	0	2	0	0	0	0	0	0	0
VCC/VCCIO4/VCCIO5/VCCX		0	2	0	2	0	0	0	0	0	0
VCCIO0/VCCX ^[3]		2	0	2	0	0	0	0	0	0	0
VCCIO1/VCCIO4/VCCIO5		0	0	0	0	0	0	0	0	0	0
VCCIO1/VCCX									3	0	
VCCIO3/VCCIO4/VCCIO5		0	0	0	0	0	0	1	0	0	0

Pin Type	GW1N-2									
	QN32X ^[4]	QN32X ^[5]	QN32 ^[4]	QN32 ^[5]	QN88 ^[4]	QN88 ^[5]	CS42H	CS100H	LQ144F ^[4]	LQ144F ^[5]
VCCD/VCCIOD	0	0	0	0	1	1	1	1	0	0
VCCX	0	0	0	0	2	2	2	1	0	0
VSS	1	1	1	1	5	5	3	2	12	12
MODE0	0	0	0	0	1	1	0	1	0	0
MODE1	0	0	0	0	1	1	0	0	0	0
MODE2	0	0	0	0	1	1	0	1	0	0
JTAGSEL_N	1	1	1	1	1		0	1	1	1
NC	1	1	1	1	0		0	0	0	0

Note!

- [1] The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [3] Pin multiplexing;
- [4] Package for LV version;
- [5] Package for UV version.

2.4.3 Quantity of GW1N-1P5 Pins

Table 2-5 Quantity of GW1N-1P5 Pins

Pin Type	GW1N-1P5								
	LQ100X ^[1]	LQ100X ^[2]	LQ100 ^[1]	LQ100 ^[2]	QN48X ^[1]	QN48X ^[2]	QN48XF ^[1]	QN48XF ^[2]	
Single-ended I/O /Differential pair/ LVDS ^[3]	BANK0	19/8/4	19/8/4	19/8/4	19/8/4	9/4/0	9/4/0	10/5/1	10/5/1
	BANK1	20/10/3	20/10/3	20/10/3	20/10/3	10/5/5	10/5/5	10/5/5	10/5/5
	BANK2	20/10/3	20/10/3	20/10/3	20/10/3	10/5/1	10/5/1	10/5/1	10/5/1
	BANK3	6/3/2	6/3/2	6/3/2	6/3/2	2/1/1	2/1/1	2/1/1	2/1/1
	BANK4	8/4/2	8/4/2	8/4/2	8/4/2	4/2/1	4/2/1	4/2/1	4/2/1
	BANK5	6/3/2	6/3/2	6/3/2	6/3/2	4/2/2	4/2/2	4/2/2	4/2/2
Max. User I/O ^[4]	80	80	80	80	39	39	40	40	
Differential Pair	38	38	38	38	19	19	20	20	
True LVDS output	16	16	16	16	10	10	11	11	
VCC	0	2	0	2	0	2	0	2	
VCCIO0	2	2	2	2	2	2	2	2	
VCCIO1	2	0	2	0	1	0	1	0	
VCCIO2	2	2	2	2	2	2	2	2	
VCCIO3	1	1	1	1	0	0	0	0	
VCCIO4/VCCIO5 ^[5]	1	1	1	1	0	0	0	0	
VCCIO3/VCCIO4/VCCIO5	0	0	0	0	1	1	1	1	
VCCIO1/VCCX	0	2	0	2	0	1	0	1	
VCC/VCCX	2	0	2	0	2	0	2	0	
VSS	8	8	8	8	0	0	0	0	
MODE0	0	0	0	0	0	0	0	0	
MODE1	0	0	0	0	0	0	0	0	
MODE2	0	0	0	0	0	0	0	0	
JTAGSEL_N	1	1	1	1	1	1	0	0	
NC	1	1	1	1	0	0	0	0	

Note!

- [1] UV version
- [2] LV version
- [3] The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [4] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O;
- [5] Pin multiplexing.

2.4.4 Quantity of GW1N-4 Pins

Table 2-6 Quantity of GW1N-4 Pins

Pin Type		GW1N-4										
		QN32	QN48	CS72	QN88	LQ100	MG132X	LQ144	MG160	UG169	PG256	PG256M
I/O Single end/ Differential pair ^[1]	BANK0	3/1/0	10/5/0	9/4/0	18/6/0	21/10/0	26/13/0	33/14/0	32/16/0	30/15/12	51/24/0	51/25/0
	BANK1	9/4/1	9/4/2	11/5/4	15/6/2	16/8/1	28/13/5	24/12/5	26/13/6	38/19/8	42/21/8	42/21/8
	BANK2	4/2/2	12/6/6	22/11/11	23/9/7	26/12/10	26/13/11	38/18/12	43/20/13	33/16/7	70/36/16	70/35/16
	BANK3	7/2/0	8/3/1	14/6/4	12/4/2	15/7/2	25/12/7	24/11/5	27/12/6	28/13/0	41/20/8	41/20/8
Max. User I/O ^[2]		24	40	57	70	79	105	119	131	129	207	207
Differential Pair		9	18	26	25	37	51	55	61	63	101	101
True LVDS output		3	9	19	11	13	23	22	25	27	32	32
VCC		2	2	3	4	4	4	4	4	4	8	8
VCCIO0		1	0	1	1	2	3	2	2	3	4	4
VCCIO1		1	0	1	1	2	3	2	2	4	3	3
VCCIO2		1	0	1	2	2	3	2	2	3	4	4
VCCIO3		1	0	1	1	2	3	2	2	4	3	3
VCCIO0/VCCIO3 ^[3]		0	1	0	0	0	0	0	0	0	0	0
VCCIO1/VCCIO2 ^[3]		0	1	0	0	0	0	0	0	0	0	0
VCCX		1	1	1	2	2	0	2	4	5	2	2
VSS		1	2	6	6	6	10	10	12	16	24	24
MODE0		0	0	1	1	1	0	1	1	0	1	1
MODE1		1	1	0	1	0	0	1	1	0	1	1
MODE2		0	0	0	0	0	0	0	1	0	1	1
JTAGSEL_N		0	1	1	1	1	1	1	1	1	1	1

Note!

- [1] The number of single-ended/ Differential I/O pins includes CLK pins and download pins;

- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

2.4.5 Quantity of GW1N-9 Pins

Table 2-7 Quantity of GW1N-9 Pins

Pin Type		GW1N-9																	
		QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	PG256	UG256	UG332	QN48F	MG100T
I/O Single end/ Differential pair ^[1]	BANK0	4/2/0	12/6/0	14/7/0	0/0/0	9/4/0	22/11/0	18/9/0	18/9/0	20/10/0	28/13/0	17/8/0	17/8/0	30/15/0	36/16/0	46/23/0	46/23/0	9/4/0	12/6/0
	BANK1	13/6/3	12/6/4	14/7/5	25/6/4	24/12/4	16/8/5	32/16/8	32/16/8	34/17/9	38/19/1 2	36/17/7	36/17/7	26/13/11	56/28/1 0	58/29/1 2	68/34/1 1	9/3/2	22/5/1
	BANK2	12/6/6	18/9/9	14/7/7	23/9/11	26/13/1 2	32/15/1 4	40/19/1 4	40/19/1 4	43/21/1 9	30/15/1 5	54/26/2 0	54/26/2 0	35/17/1 6	70/35/1 6	52/26/1 2	90/45/2 0	12/6/6	32/15/14
	BANK3	11/4/3	13/5/3	13/5/4	22/4/4	20/9/4	17/7/6	30/13/6	30/13/6	34/16/1 0	33/15/11	40/18/1 0	40/18/1 0	22/9/8	49/23/1 0	51/25/1 2	69/34/1 2	9/4/3	21/4/2
Max. User I/O ^[2]		40	55	55	70	79	87	120	120	131	129	147	147	113	207	207	273	39	87
Differential Pair		18	26	26	30	38	41	57	57	64	62	69	69	54	102	103	136	17	30
True LVDS output		12	16	15	19	20	25	28	28	38	38	37	37	35	36	36	43	11	17
VCC		2	2	5	4	4	3	4	4	4	4	4	4	15	8	8	8	2	3
VCCX		1	2	4	2	2	1	2	2	4	5	4	4	8	2	1	2	1	1
VCCIO0		0	0	1	1	2	1	2	2	2	3	3	3	4	4	4	3	1	1
VCCIO1		0	0	1	1	2	1	2	2	2	4	3	3	6	3	4	4	0	1
VCCIO2		0	0	1	2	2	1	2	2	2	3	3	3	4	4	4	5	0	1
VCCIO3		0	0	1	1	2	0	2	2	2	4	3	3	6	3	3	3	1	1
VCCIO0/ VCCIO3 ^[3]		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VCCIO1/ VCCIO2 ^[3]		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
VCCIO0/ VCCIO2 ^[3]		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pin Type	GW1N-9																	
	QN48	CM64	CS81M	QN88	LQ100	MG100	LQ144	EQ144	MG160	UG169	LQ176	EQ176	MG196	PG256	UG256	UG332	QN48F	MG100T
VCCIO1/ VCCIO3 ^[3]	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VSS	2	2	12	6	6	4	9	9	12	16	8	8	39	24	24	27	2	4
MODE0	0	0	0	1	1	0	1	1	1	0	1	1	0	1	0	1	1	0
MODE1	0	0	0	1	0	1	1	1	1	0	1	1	0	1	0	1	0	1
MODE2	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0	0
MODE1/ MODE2 ^[3]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
JTAGSEL_N	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
NC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	0	0

Note!

- [1] The number of single-ended/ Differential I/O pins includes CLK pins and download pins;
- [2] The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The table shows the data when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.
- [3] Pin multiplexing.

2.5 Introduction to the I/O BANK

GW1N-1/4/9 includes four I/O Banks.

GW1N-1S includes three I/O Banks.

GW1N-1P5/GW1N-2 includes six I/O Banks. GW1N-2 CS42 includes seven I/O Banks.

This manual provides an overview of the distribution view of the pins in the GW1N series of FPGA products. Please refer to 3 View of Pin Distribution for further details. Different IO Banks in the GW1N series FPGA products are marked with different colors.

User I/O, power, and ground are marked with different symbols and colors. The various symbols and colors used for various pins are defined as follows:

- "  " denotes I/Os in BANK0.
- "  " denotes I/Os in BANK1.
- "  " denotes I/Os in BANK2.
- "  " denotes I/Os in BANK3.
- "  " denotes I/Os in BANK4.
- "  " denotes I/Os in BANK5.
- "  " denotes I/Os in BANK6.
- "  " denotes VCC, VCCX, and VCCIO. The filling color does not change.
- "  " denotes VSS. The filling color does not change.
- "  " denotes NC.

3 View of Pin Distribution

3.1 View of GW1N-1 Pins Distribution

3.1.1 View of CS30 Pins Distribution

Figure 3-1 View of GW1N-1 CS30 Pin Distribution (Top View)

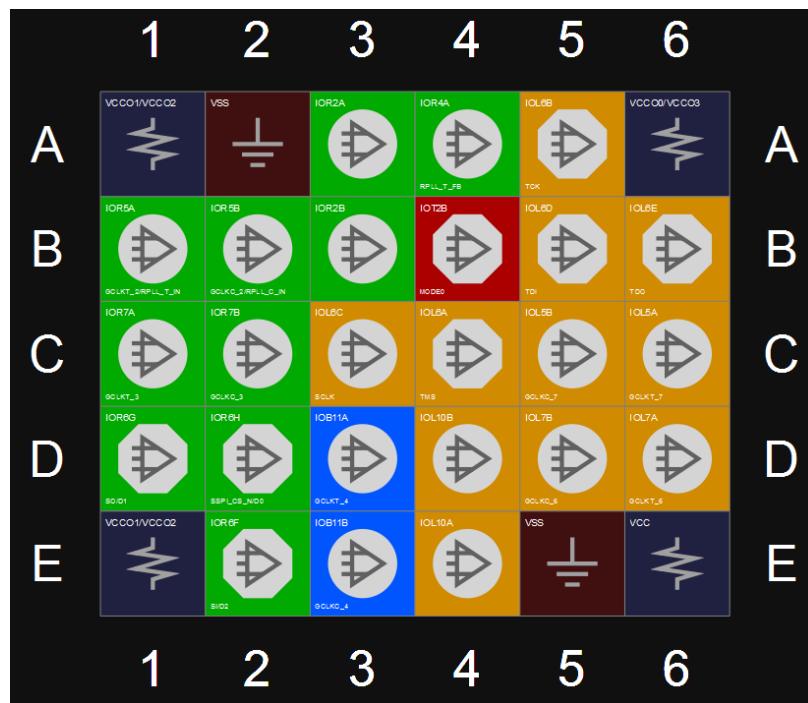


Table 3-1 Other Pins in GW1N-1 CS30

VCC	E6
VCCIO0/VCCIO3	A6
VCCIO1/VCCIO2	E1,A1
VSS	A2,E5

3.2 View of GW1N-2 Pins Distribution

3.2.1 View of CS42 Pins Distribution

Figure 3-2 View of GW1N-2 CS42 Pins Distribution (Top View)

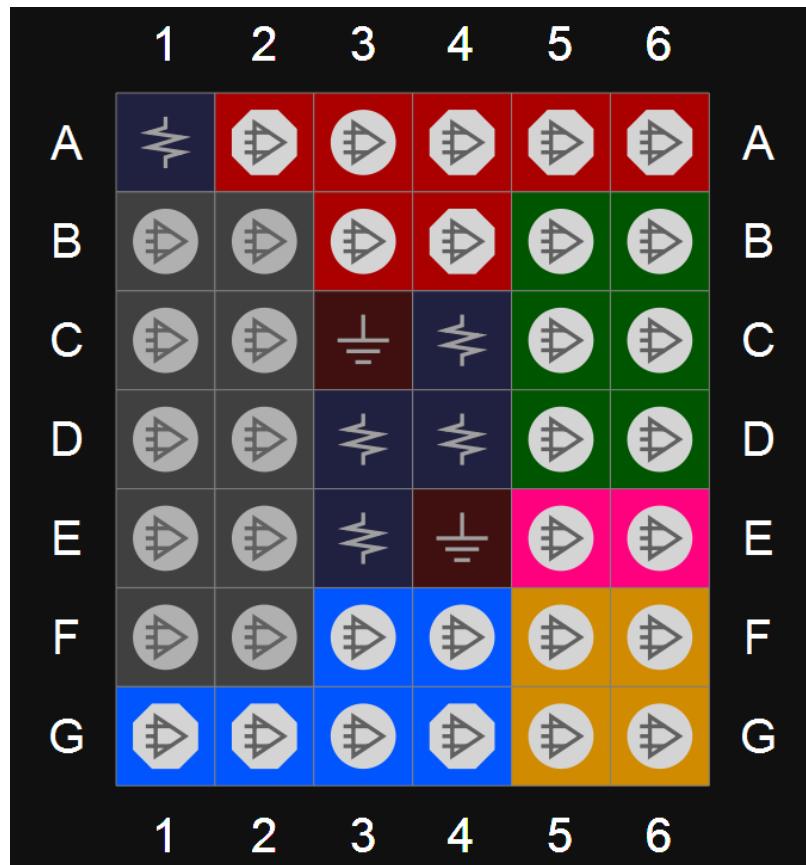


Table 3-2 Other Pins in GW1N-2 CS42

VCC	D4
VCCIO0/VCCIO2	A1
VCCIO3/VCCIO4/VCCIO5	C4
VCCIOD/VCCIO1/VCCIOD	D3
VCCX	E3
VSS	C3,E4

3.2.2 View of CS42H Pins Distribution

Figure 3-3 View of GW1N-2 CS42H Pins Distribution (Top View)

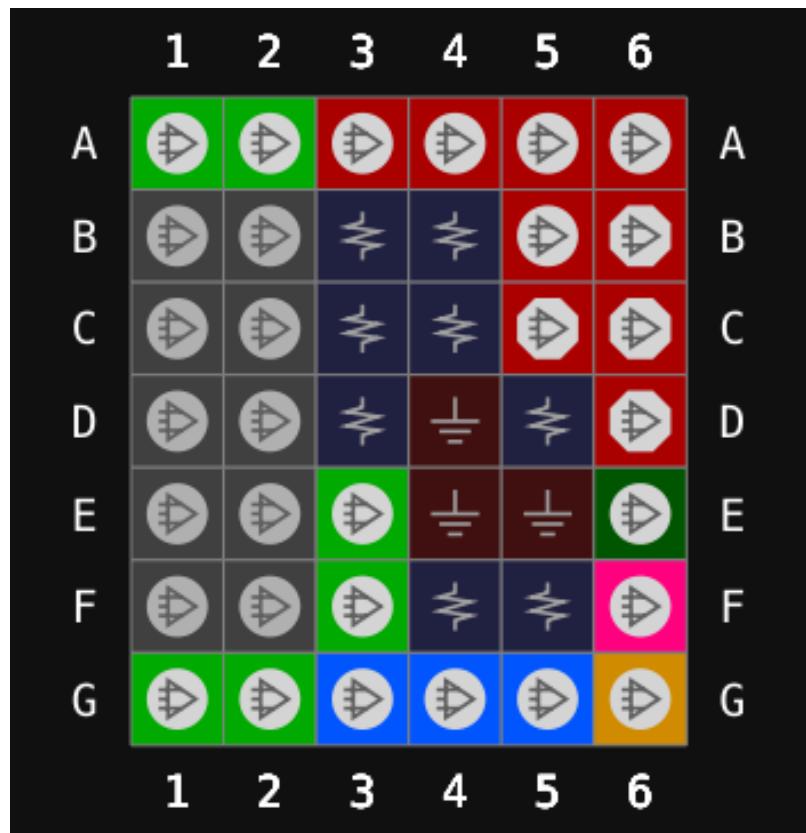


Table 3-3 Other Pins in GW1N-2 CS42H

VCC	D3
VCCIO0	B4
VCCIO1	B3
VCCIO2	F5
VCCIO3/ VCCIO4/ VCCIO5	C4
VCCX	D5,F4
VCCD/VCCIOD	C3
VSS	D4,E4,E5

3.2.3 View of CS100H Pins Distribution

Figure 3-4 View of GW1N-2 CS100H Pins Distribution (Top View)

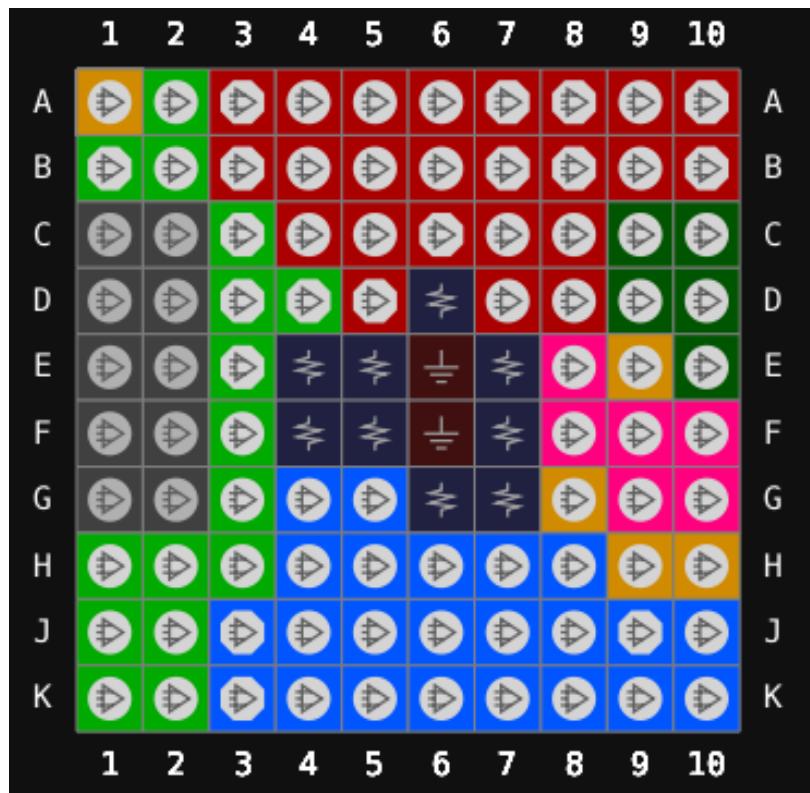


Table 3-4 Other Pins in GW1N-2 CS100H

VCC	E5
VCCIO0	D6
VCCIO1	E4
VCCIO2	G6
VCCIO3	G7
VCCIO4	F7
VCCIO5	E7
VCCD/VCCIOD	F4
VCCX	F5
VSS	E6, F6

3.2.4 View of MG132X Pins Distribution (UV Version)

Figure 3-5 View of GW1N-2 MG132X Pins Distribution (UV Version, Top View)

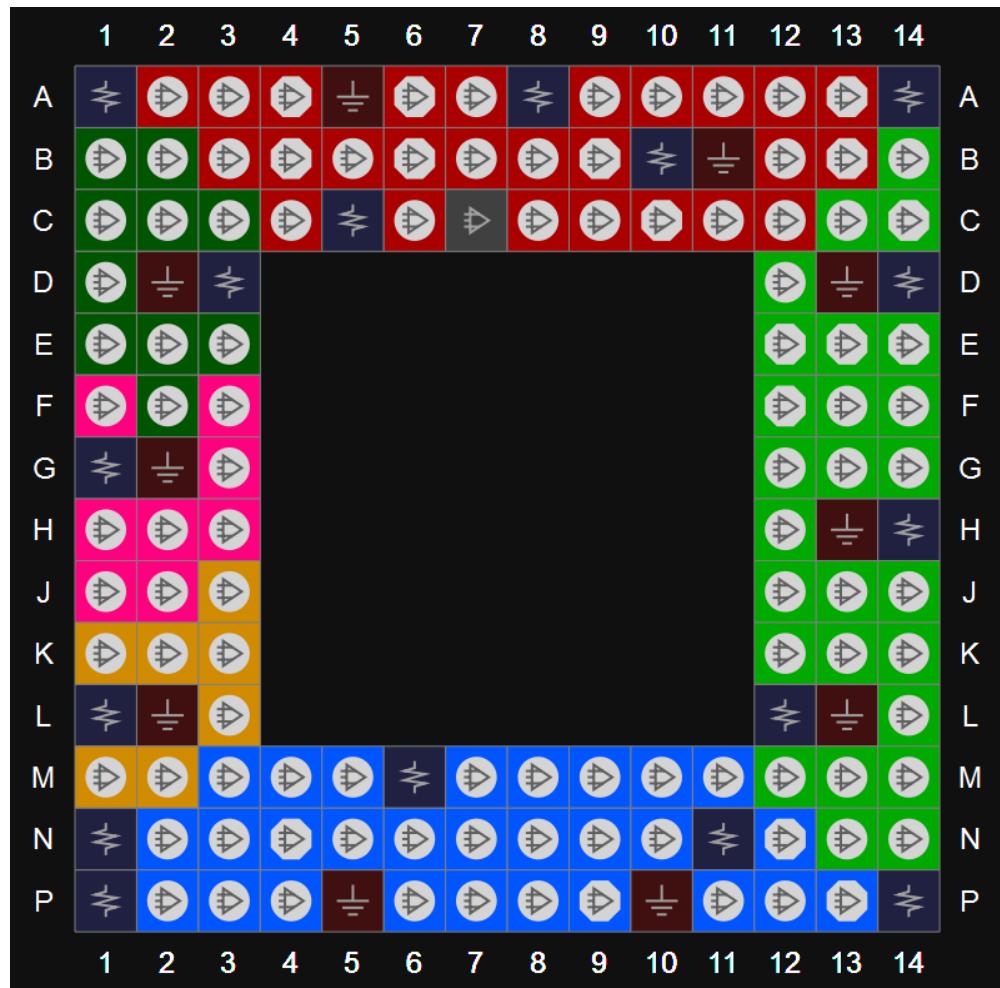


Table 3-5 Other Pins in GW1N-2 MG132X (UV Version)

VCC/VCCX	A1,A14,N1,P14
VCCIO0	A8,B10,C5
VCCIO1	D14,H14,L12
VCCIO2	M6,N11,P1
VCCIO3	L1
VCCIO4	G1
VCC05	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,,P5,P10
NC	C7

3.2.5 View of MG132X Pins Distribution (LV Version)

Figure 3-6 View of GW1N-2 MG132X Pins Distribution (LV Version, Top View)

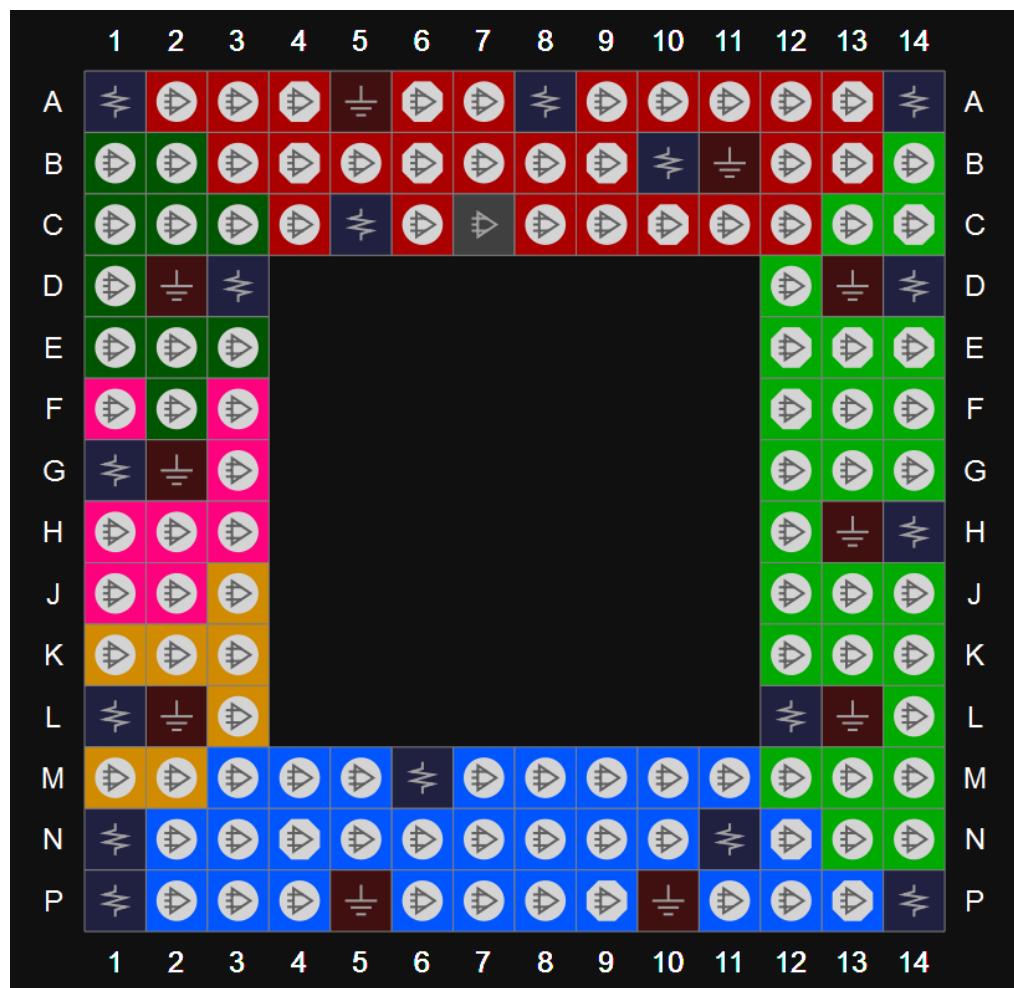


Table 3-6 Other Pins in GW1N-2 MG132X (LV Version)

VCC	A1,A14,N1,P14
VCCIO0	A8,B10,C5
VCCIO1/VCCX	D14,H14,L12
VCCIO2	M6,N11,P1
VCCIO3	L1
VCCIO4	G1
VCC05	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,,P5,P10
NC	C7

3.2.6 View of LQ100X Pins Distribution (UV Version)

Figure 3-7 View of GW1N-2 LQ100X Pins Distribution (UV Version, Top View)

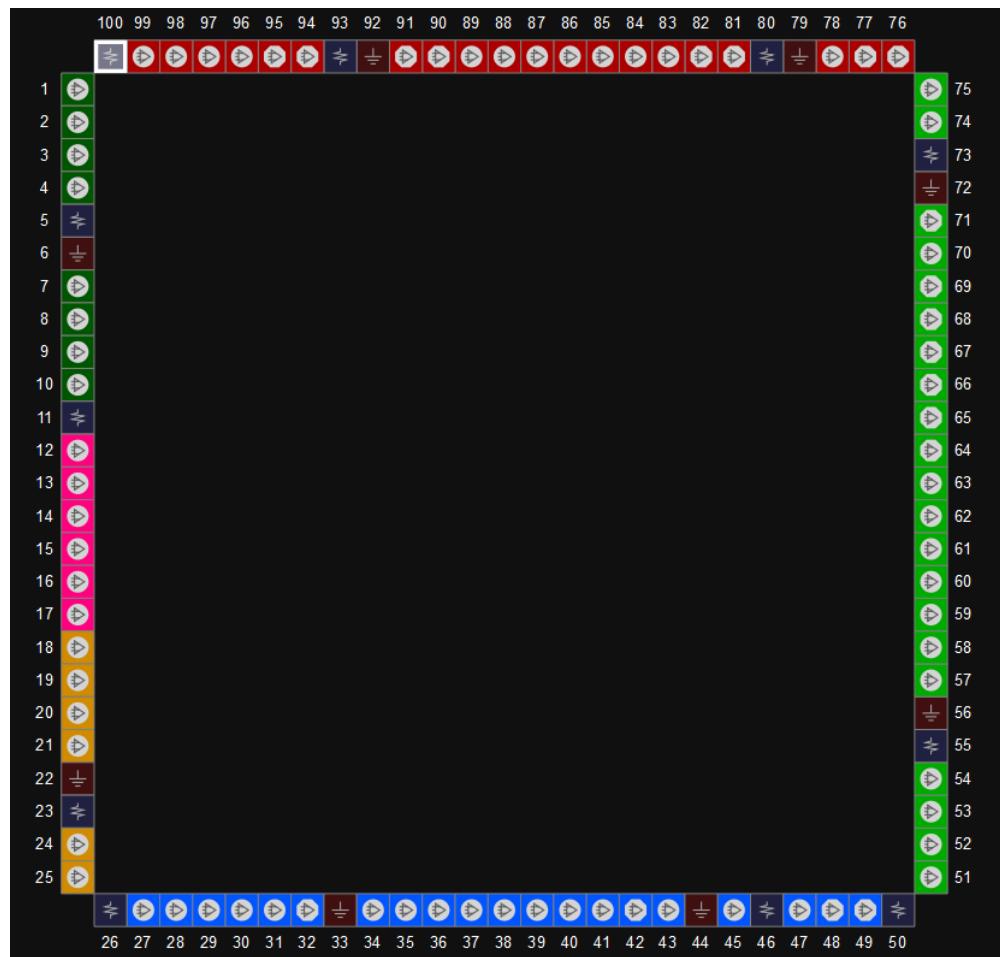


Table 3-7 Other Pins in GW1N-2 LQ100X (UV Version)

VCC/VCCX	100,50
VCCIO0	80,93
VCCIO1	55,73
VCCIO2	26,46
VCCIO3	23
VCCIO4	11
VCCIO5	5
VSS	6,22,33,44,56,72,79,92

3.2.7 View of LQ100X Pins Distribution (LV Version)

Figure 3-8 View of GW1N-2 LQ100X Pins Distribution (LV Version, Top View)

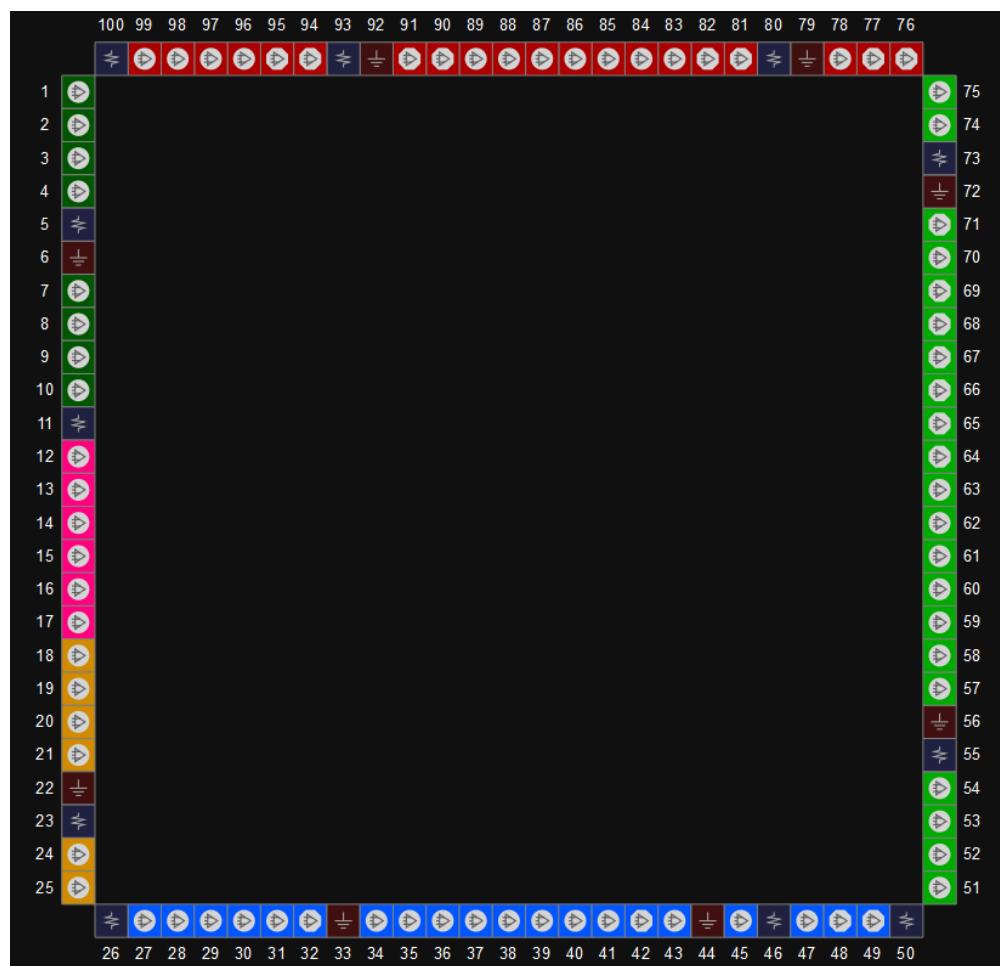


Table 3-8 Other Pins in GW1N-2 LQ100X (LV Version)

VCC	100,50
VCCIO0	80,93
VCCIO1/VCCX	55,73
VCCIO2	26,46
VCCIO3	23
VCCIO4	11
VCCIO5	5
VSS	6,22,33,44,56,72,79,92

3.2.8 View of LQ100 Pins Distribution (UV Version)

Figure 3-9 View of GW1N-2 LQ100 Pins Distribution (UV Version, Top View)

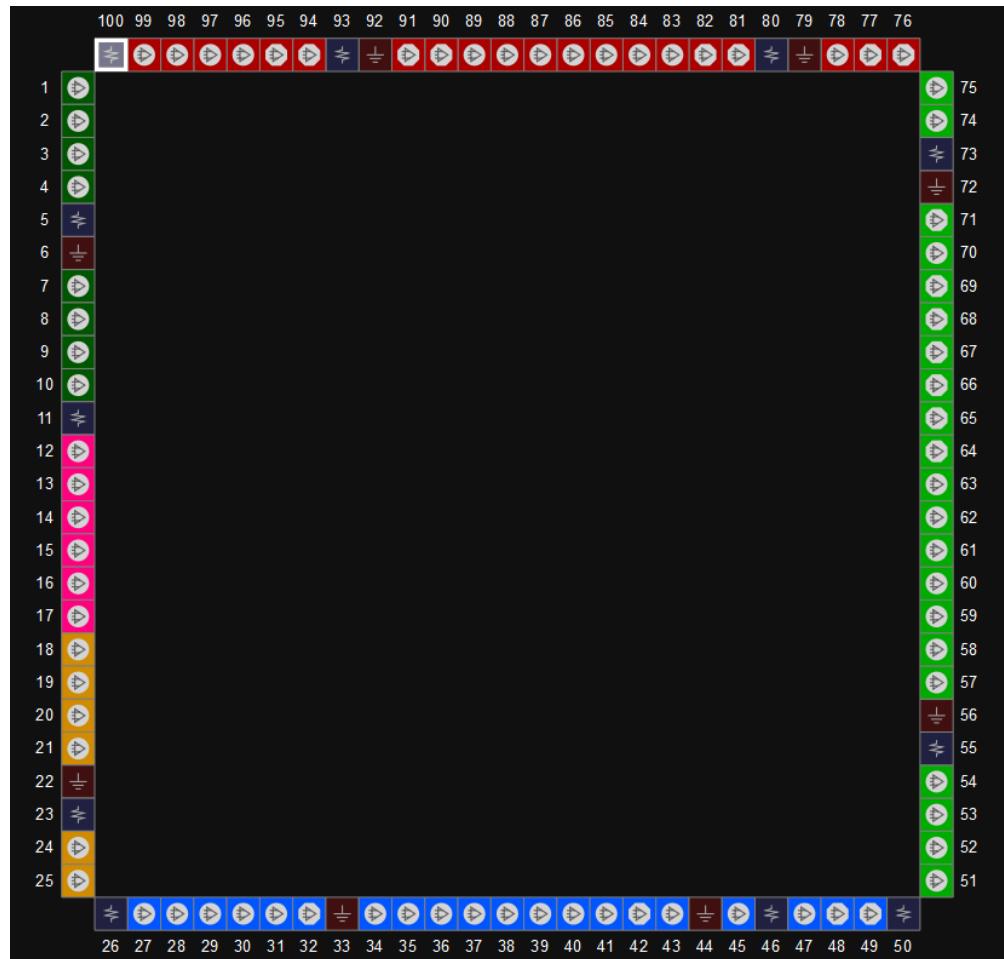


Table 3-9 Other Pins in GW1N-2 LQ100 (UV Version)

VCC/VCCX	100,50
VCCIO0	80,93
VCCIO1	55,73
VCCIO2	26,46
VCCIO3	23
VCCIO4	11
VCCIO5	5
VSS	6,22,33,44,56,72,79,92

3.2.9 View of LQ100 Pins Distribution (LV Version)

Figure 3-10 View of GW1N-2 LQ100 Pins Distribution (LV Version, Top View)

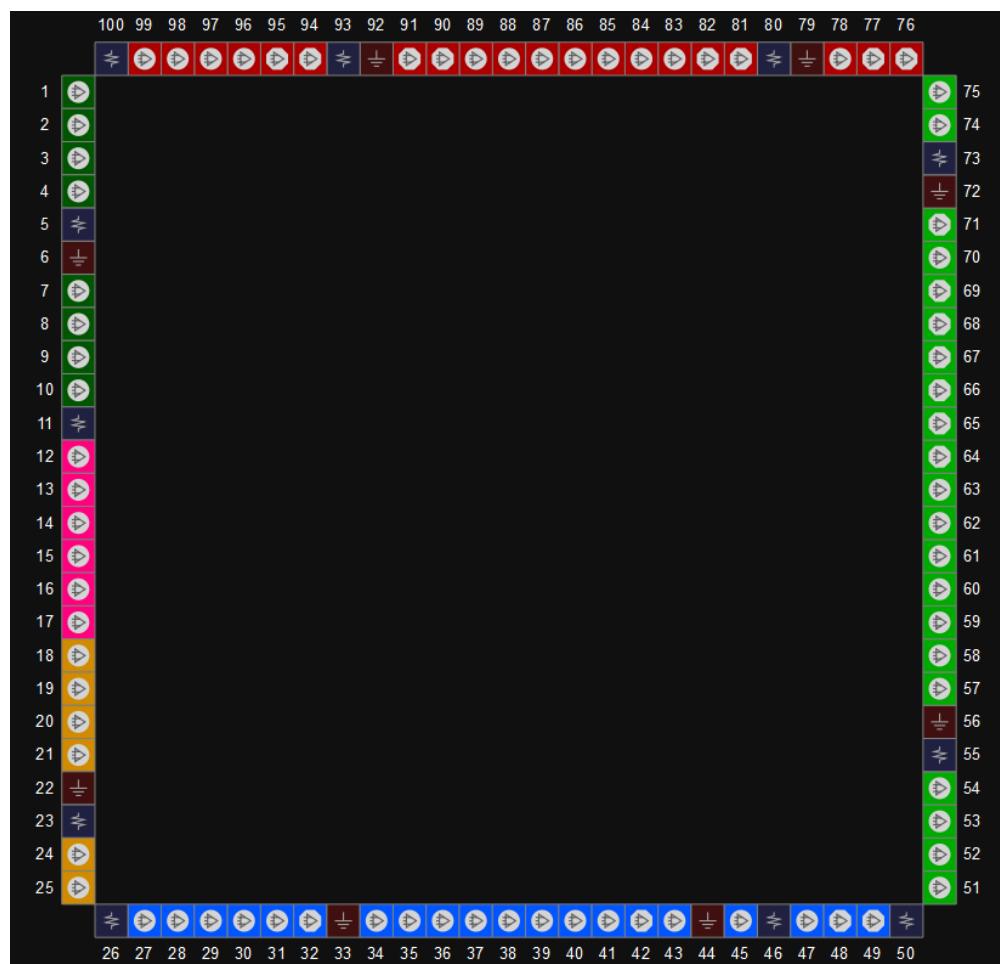


Table 3-10 Other Pins in GW1N-2 LQ100 (LV Version)

VCC	100,50
VCCIO0	80.93
VCCIO1/VCCX	55,73
VCCIO2	26,46
VCCIO3	23
VCCIO4	11
VCCIO5	5
VSS	6,22,33,44,56,72,79,92

3.2.10 View of LQ144X Pins Distribution (UV Version)

Figure 3-11 View of GW1N-2 LQ144X Pins Distribution (UV Version, Top View)



Table 3-11 Other Pins in GW1N-2 LQ144X (UV Version)

VCC/VCCX	144,36,72,108
VCCIO0	118,123,135
VCCIO1	79,88,102
VCCIO2	37,51,66
VCCIO3	30
VCCIO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.2.11 View of LQ144X Pins Distribution (LV Version)

Figure 3-12 View of GW1N-2 LQ144X Pins Distribution (LV Version, Top View)



Table 3-12 Other Pins in GW1N-2 LQ144X (LV Version)

VCC	144,36,72,108
VCCIO0	118,123,135
VCCIO1/VCCX	79,88,102
VCCIO2	37,51,66
VCCIO3	30
VCCIO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.2.12 View of LQ144 Pins Distribution (UV Version)

Figure 3-13 View of GW1N-2 LQ144 Pins Distribution (UV Version, Top View)



Table 3-13 Other Pins in GW1N-2 LQ144 (UV Version)

VCC/VCCX	144,36,72,108
VCCIO0	118,123,135
VCCIO1	79,88,102
VCCIO2	37,51,66
VCCIO3	30
VCCIO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.2.13 View of LQ144 Pins Distribution (LV Version)

Figure 3-14 View of GW1N-2 LQ144 Pins Distribution (LV Version, Top View)



Table 3-14 Other Pins in GW1N-2 LQ144 (LV Version)

VCC	144,36,72,108
VCCIO0	118,123,135
VCCIO1/VCCX	79,88,102
VCCIO2	37,51,66
VCCIO3	30
VCCIO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134
NC	103,31

3.2.14 View of LQ144F Pins Distribution (UV Version)

Figure 3-15 View of GW1N-2 LQ144F Pins Distribution (UV Version, Top View)



Table 3-15 Other Pins in GW1N-2 LQ144F (UV Version)

VCC/VCCX	144,36,72,108
VCCIO0	118,123,135
VCCIO1	79,88,102
VCCIO2	37,51,66
VCCIO3	30
VCCIO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134

3.2.15 View of LQ144F Pins Distribution (LV Version)

Figure 3-16 View of GW1N-2 LQ144F Pins Distribution (LV Version, Top View)



Table 3-16 Other Pins in GW1N-2 LQ144F (LV Version)

VCC	144,36,72,108
VCCIO0	118,123,135
VCCIO1/VCCX	79,88,102
VCCIO2	37,51,66
VCCIO3	30
VCCIO4	16
VCC05	7
VSS	8,18,29,46,53,64,80,90,101,116,124,134

3.2.16 View of QN48 Pins Distribution

Figure 3-17 View of GW1N-2 QN48 Pins Distribution (Top View)

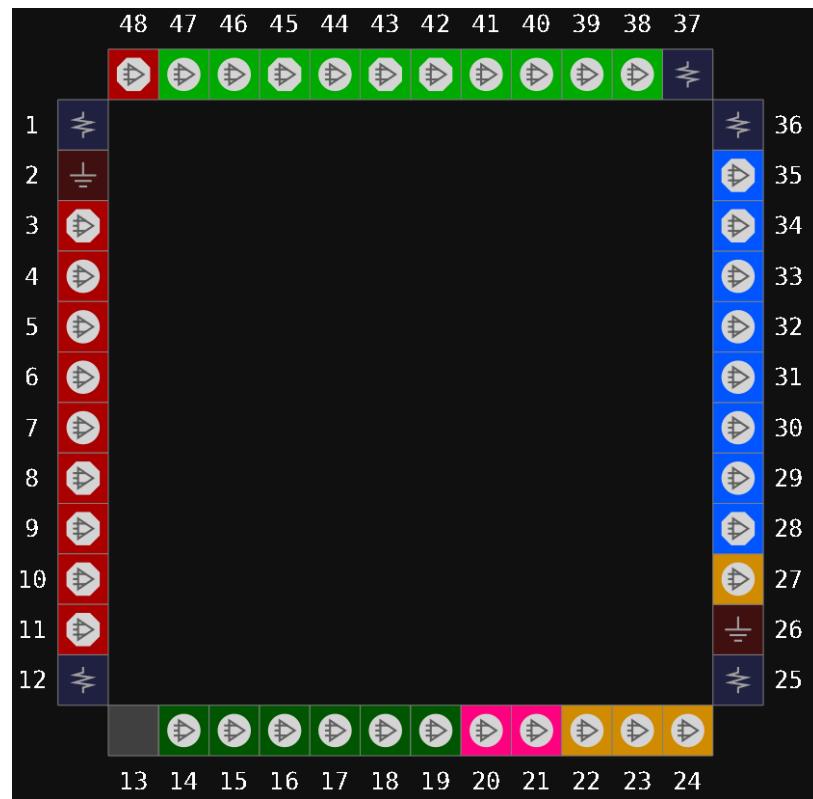


Table 3-17 Other Pins in GW1N-2 QN48

VCC	12
VCCIO0	1
VCCIO1	37
VCCIO2/VCCX	36
VCCIO3/VCCIO4/VCCIO5	25
VSS	2,26

3.2.17 View of QN48H Pins Distribution

Figure 3-18 View of GW1N-2 QN48H Pins Distribution (Top View)

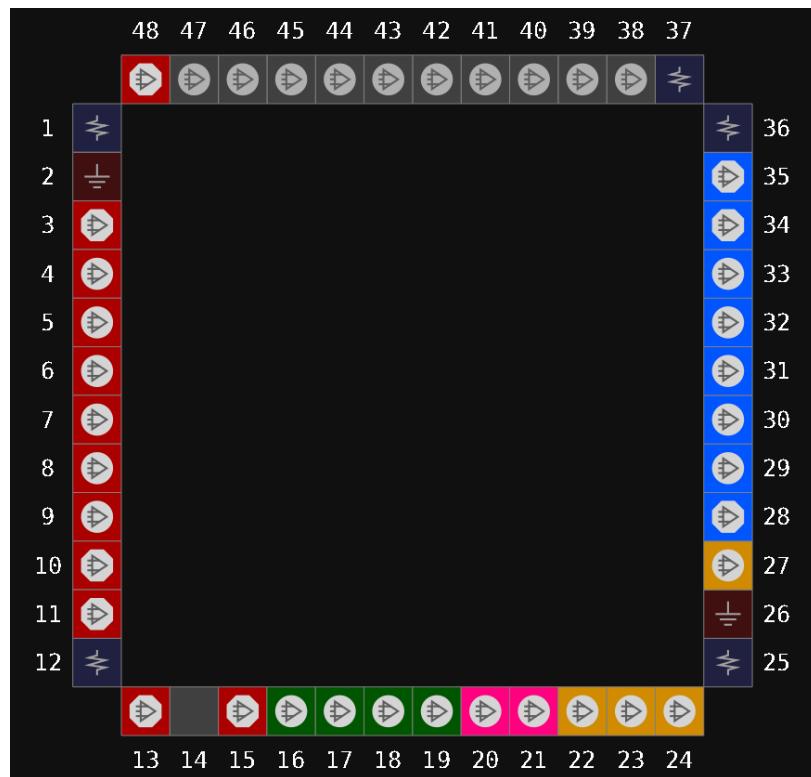


Table 3-18 Other Pins in GW1N-2 QN48H

VCC/VCCIO1	37
VCCIO0	12
VCCIO2/VCCX	36
VCCIO3/VCCIO4/VCCIO5	25
VCCD/VCCIOD	1
VSS	2,26

3.2.18 View of MG132H Pins Distribution

Figure 3-19 View of GW1N-2 MG132H Pins Distribution (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	A
B	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	B
C	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	C
D	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	D
E	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	E
F	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	F
G	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	G
H	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	H
J	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	J
K	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	K
L	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	L
M	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	M
N	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	N
P	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	⚡	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 3-19 Other Pins in GW1N-2 MG132H

VCC	A1,A14,N1,P14
VCCIO0	A8,B10,C5
VCCIO1	D14,L12
VCCIO2	M6,N11,P1
VCCIO3	L1
VCCIO4	G1
VCCIO5	D3
VCCX	H14
VCCD/VCCIOD	C7
VSS	A5,B11,D2,D13,G2,H13,L2,L13,P5,P10

3.2.19 View of MG132 Pins Distribution (UV Version)

Figure 3-20 View of GW1N-2 MG132 Pins Distribution (UV Version, Top View)

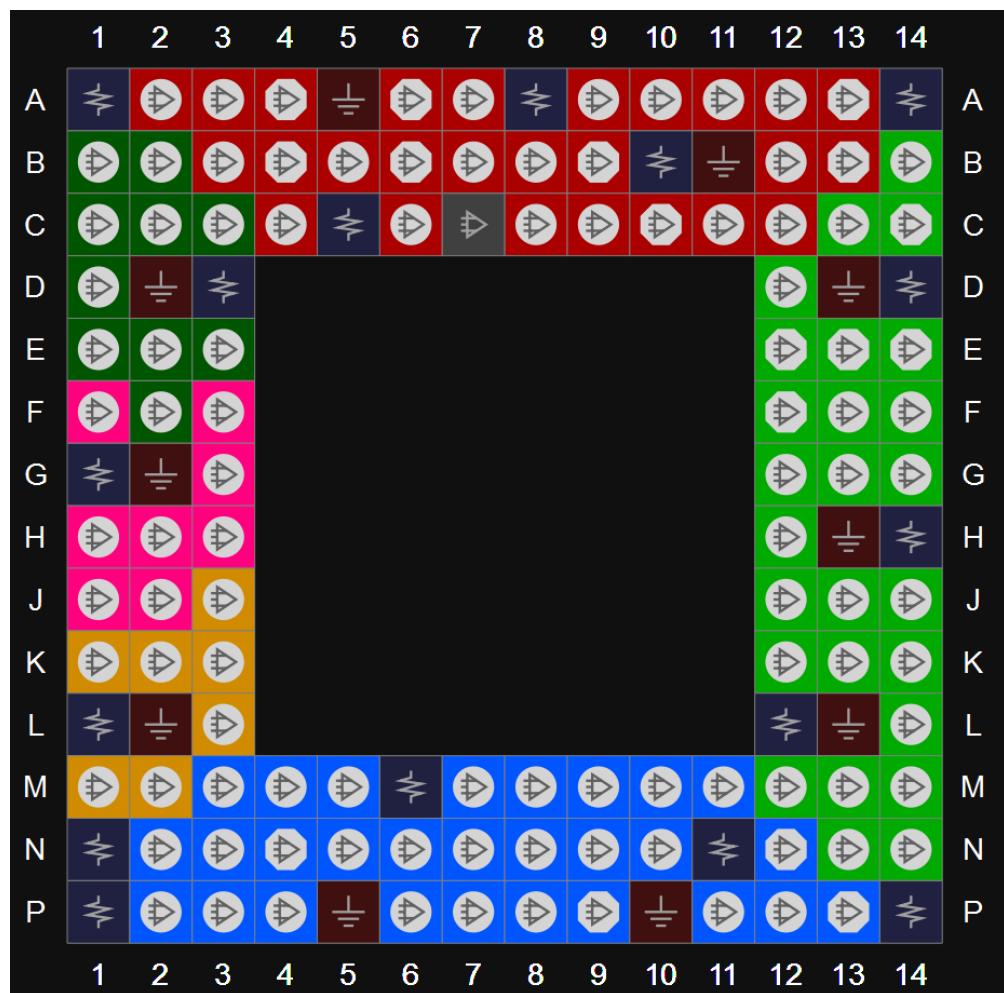


Table 3-20 Other Pins in GW1N-2 MG132 (UV Version)

VCC/VCCX	A1,A14,N1,P14
VCCIO0	A8,B10,C5
VCCIO1	D14,H14,L12
VCCIO2	M6,N11,P1
VCCIO3	L1
VCCIO4	G1
VCCIO5	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,P5,P10
NC	C7

3.2.20 View of MG132 Pins Distribution (LV Version)

Figure 3-21 View of GW1N-2 MG132 Pins Distribution (LV Version, Top View)

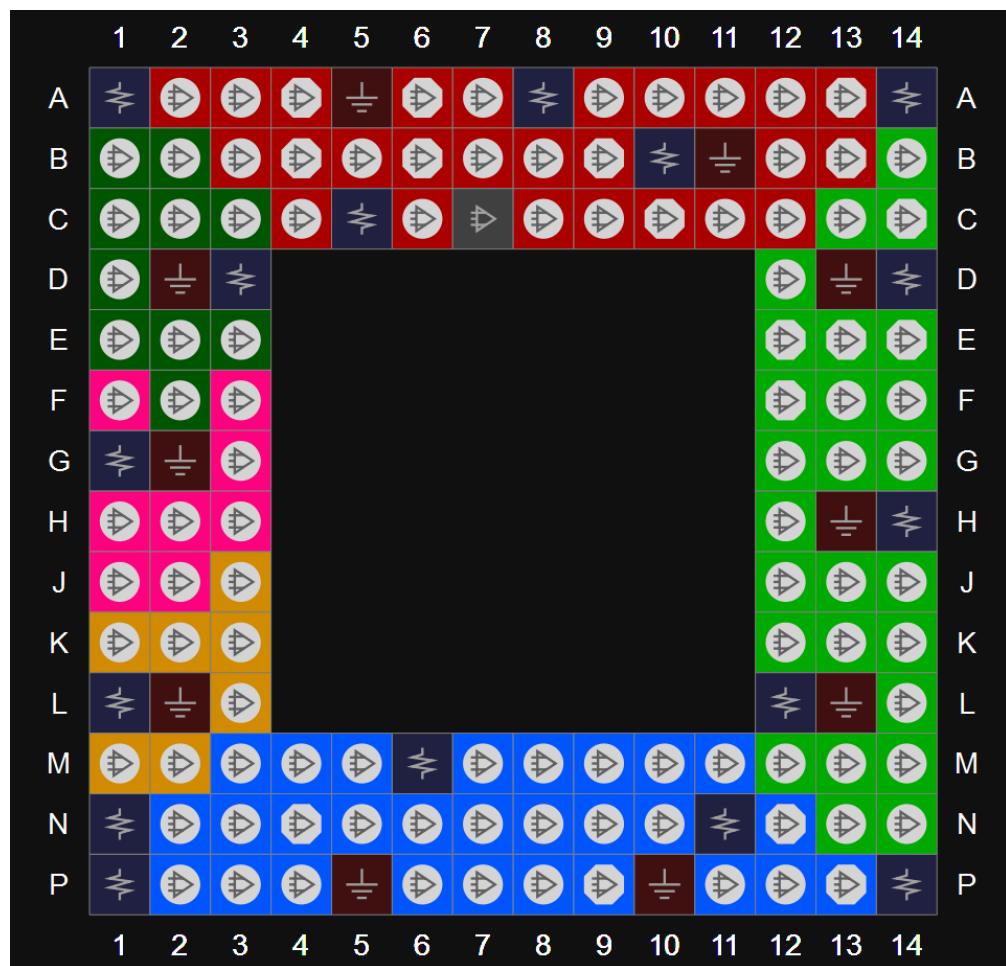


Table 3-21 Other Pins in GW1N-2 MG132 (LV Version)

VCC	A1,A14,N1,P14
VCCIO0	A8,B10,C5
VCCIO1/VCCX	D14,H14,L12
VCCIO2	M6,N11,P1
VCCIO3	L1
VCCIO4	G1
VCCIO5	D3
VSS	A5,B11,D2,D13,G2,H13,L2,L13,P5,P10
NC	C7

3.2.21 View of MG121 Pins Distribution (LV Version)

Figure 3-22 View of GW1N-2 MG121 Pins Distribution (LV Version, Top View)

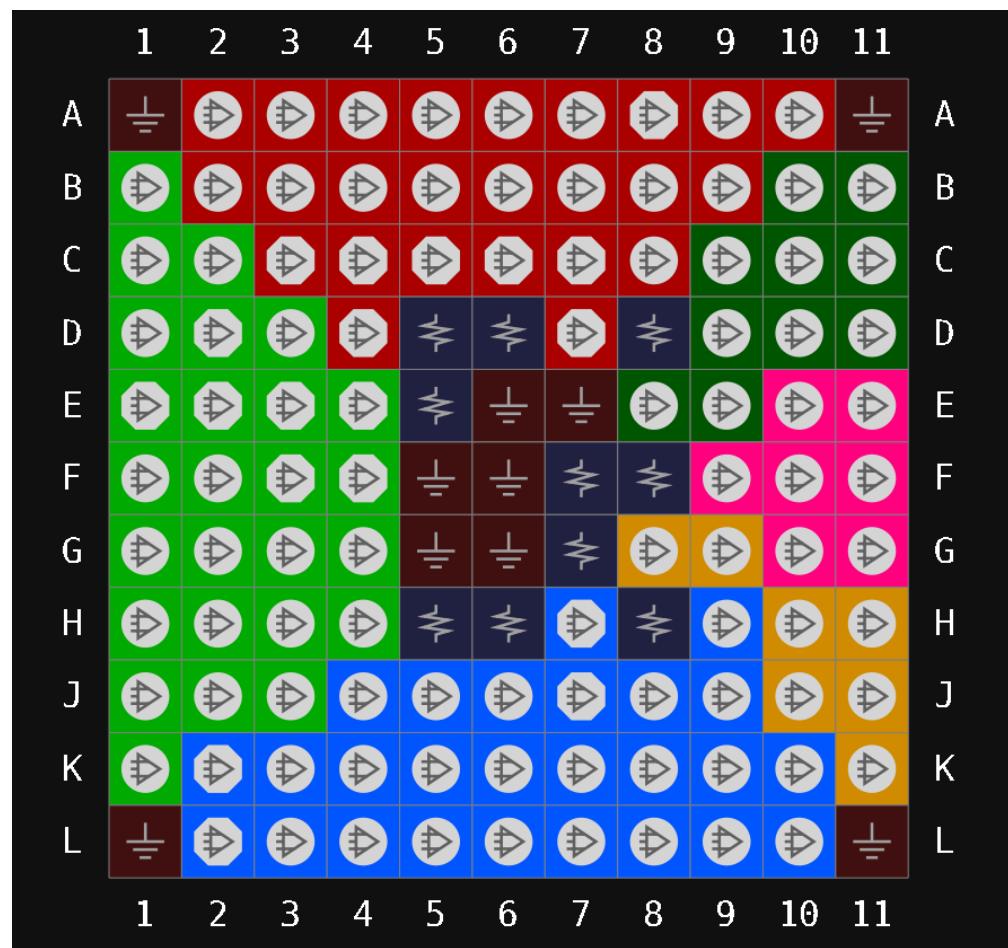


Table 3-22 Other Pins in GW1N-2 MG121 (LV Version)

VCC	F7,G7,D5,E5
VCCIO0	D6
VCCIO1/VCCX	H5
VCCIO2	H6
VCCIO3	H8
VCCIO4	F8
VCCIO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.2.22 View of MG121 Pins Distribution (UV Version)

Figure 3-23 View of GW1N-2 MG121 Pins Distribution (UV Version, Top View)

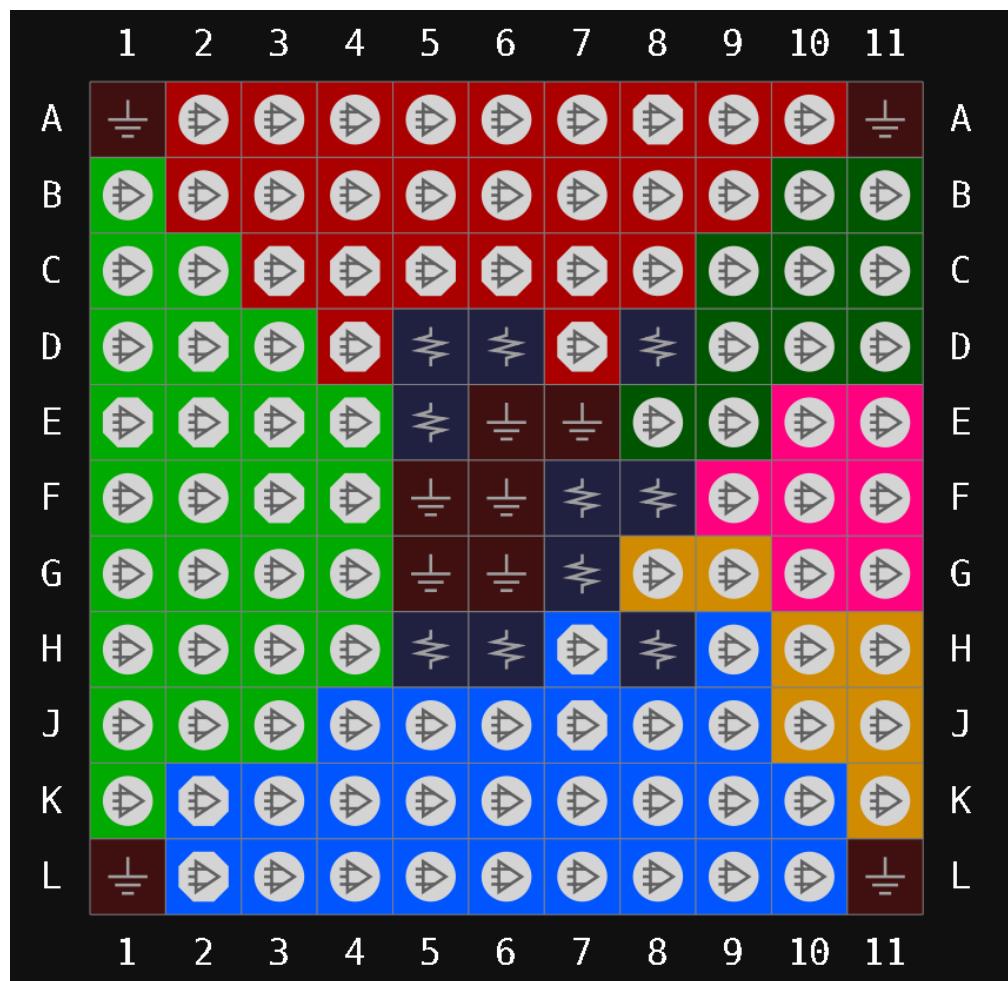


Table 3-23 Other Pins in GW1N-2 MG121 (UV Version)

VCC/VCCX	F7,G7,D5,E5
VCCIO0	D6
VCCIO1	H5
VCCIO2	H6
VCCIO3	H8
VCCIO4	F8
VCCIO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.2.23 View of MG121X Pins Distribution (LV Version)

Figure 3-24 View of GW1N-2 MG121X Pins Distribution (LV Version, Top View)

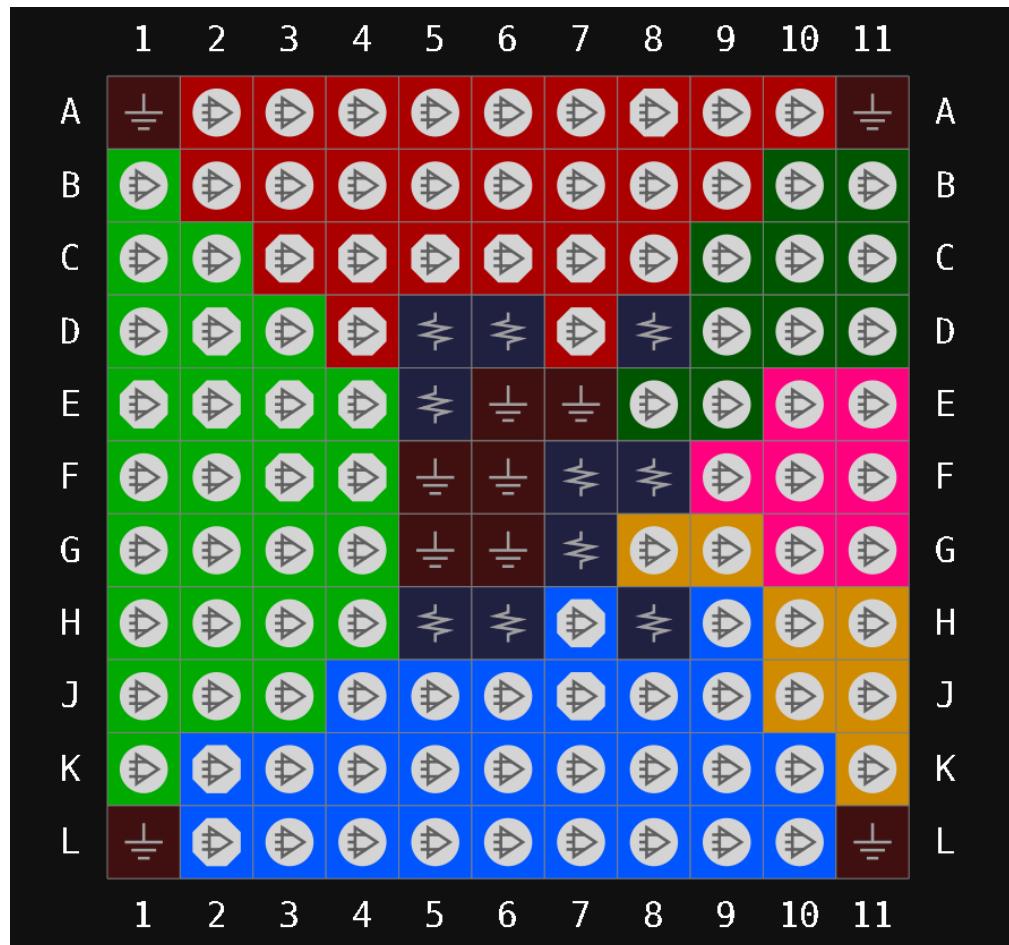


Table 3-24 Other Pins in GW1N-2 MG121X (LV Version)

VCC	F7,G7,D5,E5
VCCIO0	D6
VCCIO1/VCCX	H5
VCCIO2	H6
VCCIO3	H8
VCCIO4	F8
VCCIO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.2.24 View of MG121X Pins Distribution (UV Version)

Figure 3-25 View of GW1N-2 MG121X Pins Distribution (UV Version, Top View)

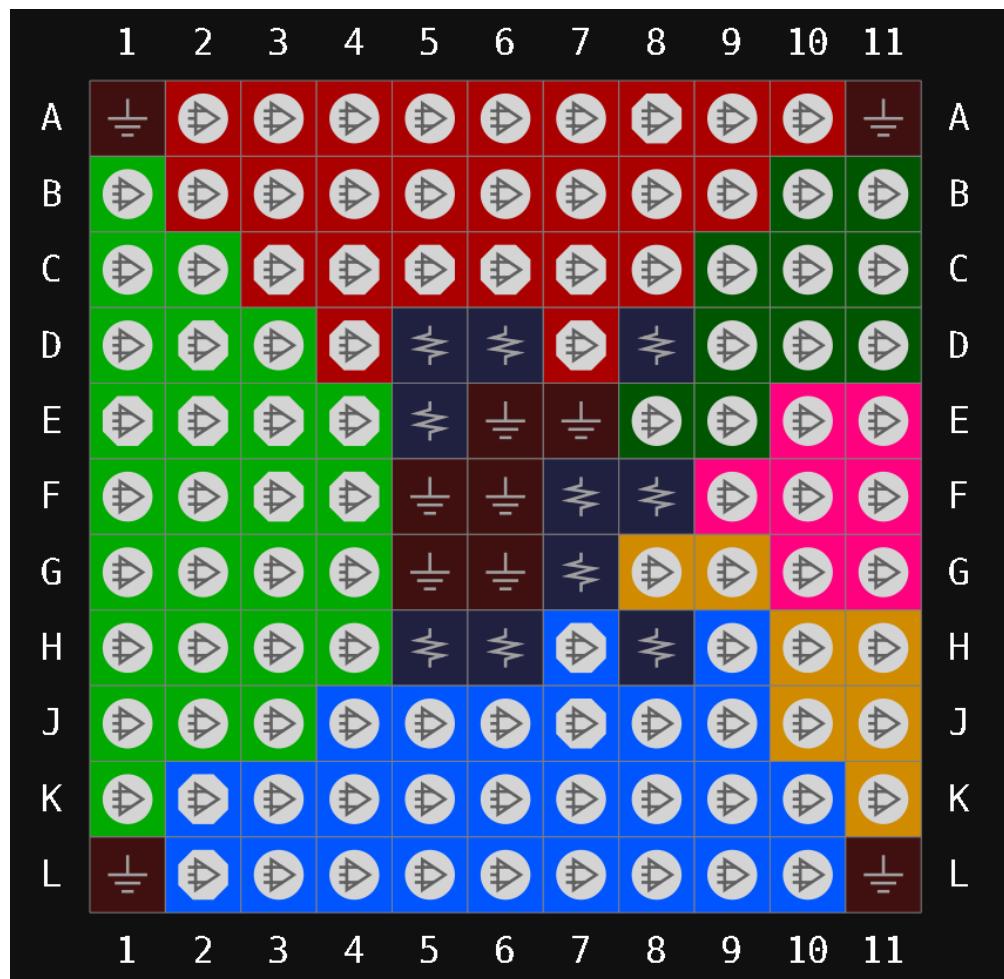


Table 3-25 Other Pins in GW1N-2 MG121X (UV Version)

VCC/VCCX	F7,G7,D5,E5
VCCIO0	D6
VCCIO1	H5
VCCIO2	H6
VCCIO3	H8
VCCIO4	F8
VCCIO5	D8
VSS	A1,A11,E6,E7,F5,F6,G5,G6,L1,L11

3.2.25 View of MG49 Pins Distribution

Figure 3-26 View of GW1N-2 MG49 Pins Distribution (Top View)

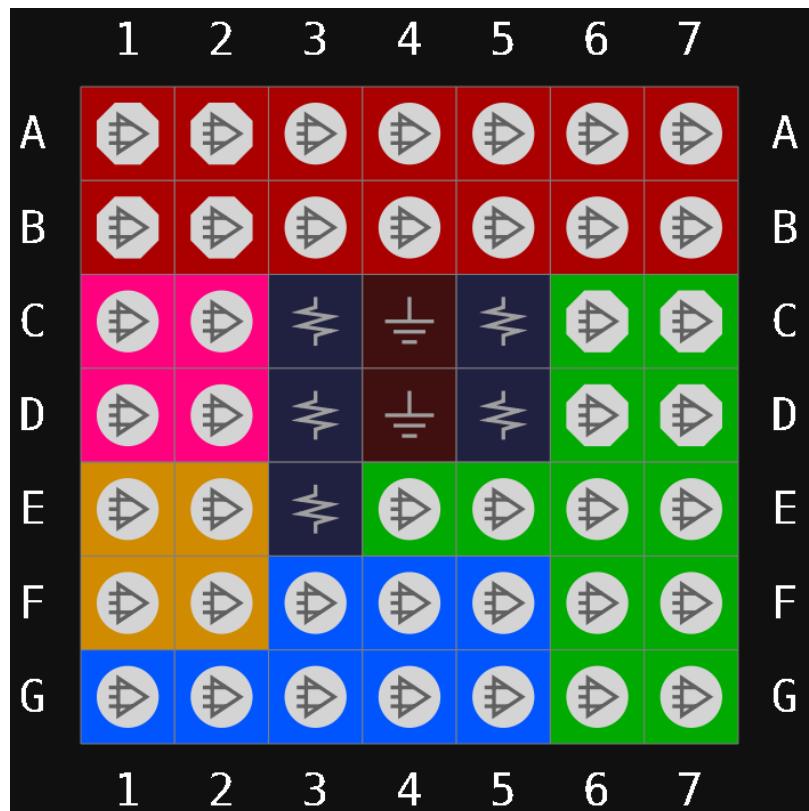


Table 3-26 Other Pins in GW1N-2 MG49

VCC	C3
VCCIO0	C5
VCCIO1	D5
VCCIO2/VCCIO3/VCCIO4/VCCIO5	D3
VCCX	E3
VSS	C4, D4

3.2.26 View of QN32 Pins Distribution (LV Version)

Figure 3-27 View of GW1N-2 QN32 Pins Distribution (LV Version, Top View)

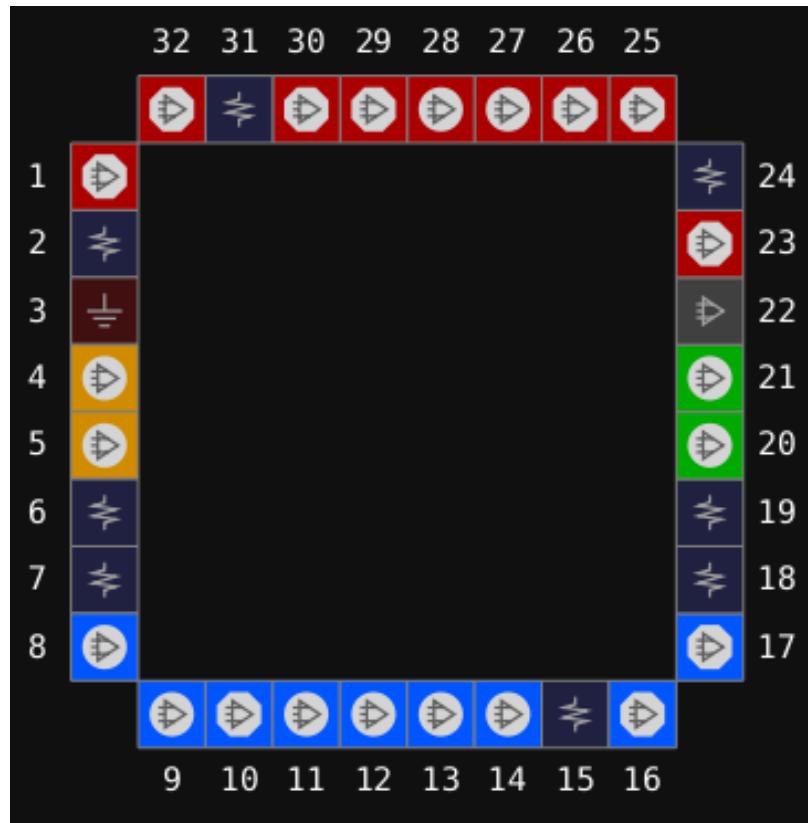


Table 3-27 Other Pins in GW1N-2 QN32 (LV Version)

VCCIO0/VCCX	24,31
VCC/VCCIO4/VCCIO5	18,2
VCCIO2	7,15
VCCIO3	6
VCCIO1	19
VSS	3

3.2.27 View of QN32 Pins Distribution (UV Version)

Figure 3-28 View of GW1N-2 QN32 Pins Distribution (UV Version, Top View)

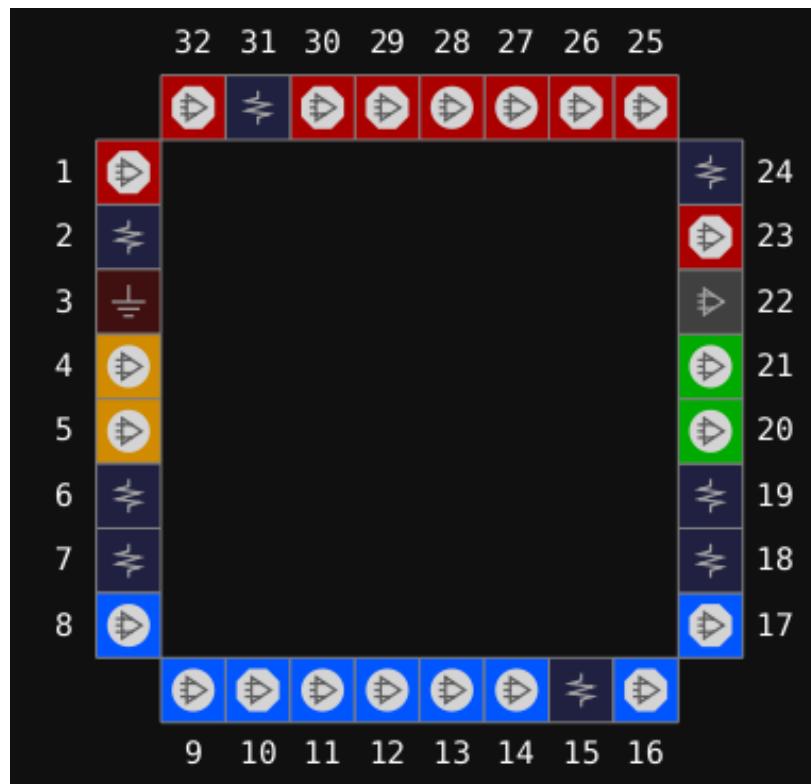


Table 3-28 Other Pins in GW1N-2 QN32 (UV Version)

VCCIO0	24,31
VCCIO1	19
VCCIO2	7,15
VCCIO3	6
VCC/ VCCIO4/VCCIO5/VCCX	18,2
VSS	3

3.2.28 View of QN32X Pins Distribution (LV Version)

Figure 3-29 View of GW1N-2 QN32X Pins Distribution (LV Version, Top View)

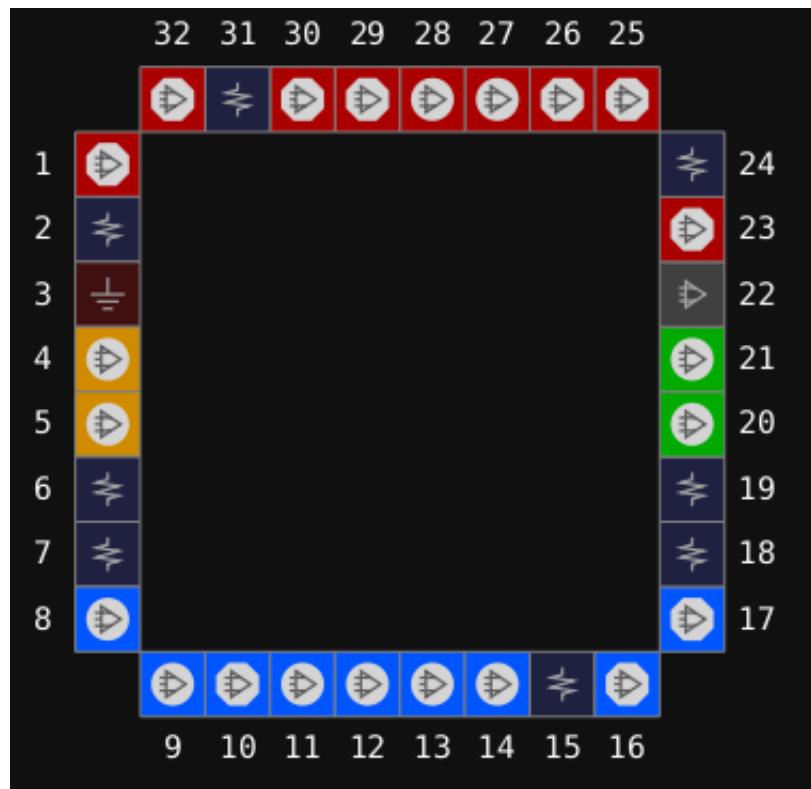
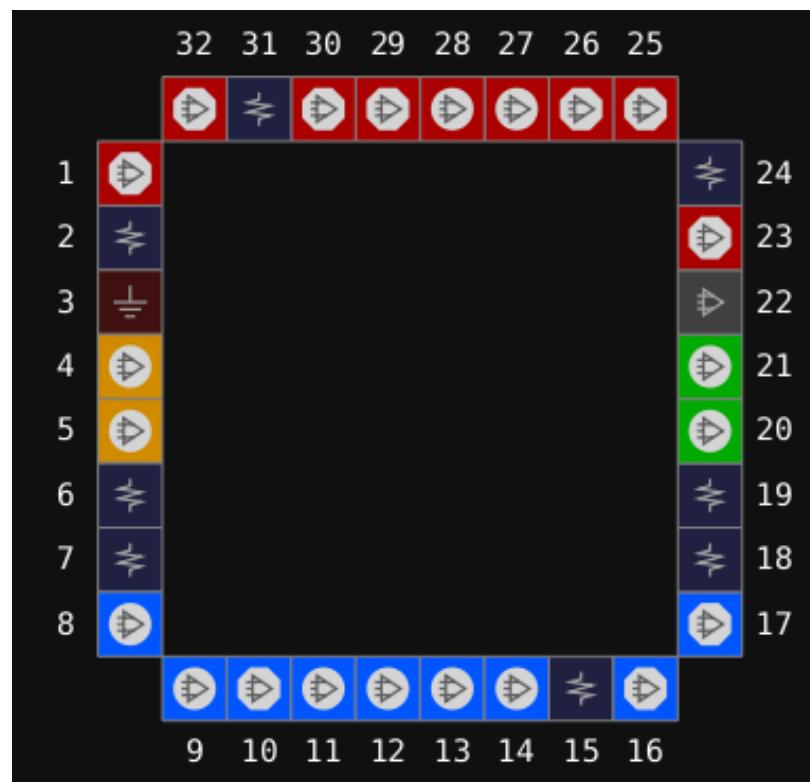


Table 3-29 Other Pins in GW1N-2 QN32X(LV Version)

VCCIO0/VCCX	24,31
VCC/VCCIO4/VCCIO5	18,2
VCCIO2	7,15
VCCIO3	6
VCCIO1	19
VSS	3

3.2.29 View of QN32X Pins Distribution (UV Version)

Figure 3-30 View of GW1N-2 QN32X Pins Distribution (UV Version, Top View)



VCCIO0	24,31
VCCIO1	19
VCCIO2	7,15
VCCIO3	6
VCC/VCCIO4/VCCIO5/VCCX	18,2
VSS	3

3.2.30 View of QN88 Pins Distribution (LV Version)

Figure 3-31 View of GW1N-2 QN88 Pins Distribution (LV Version, Top View)

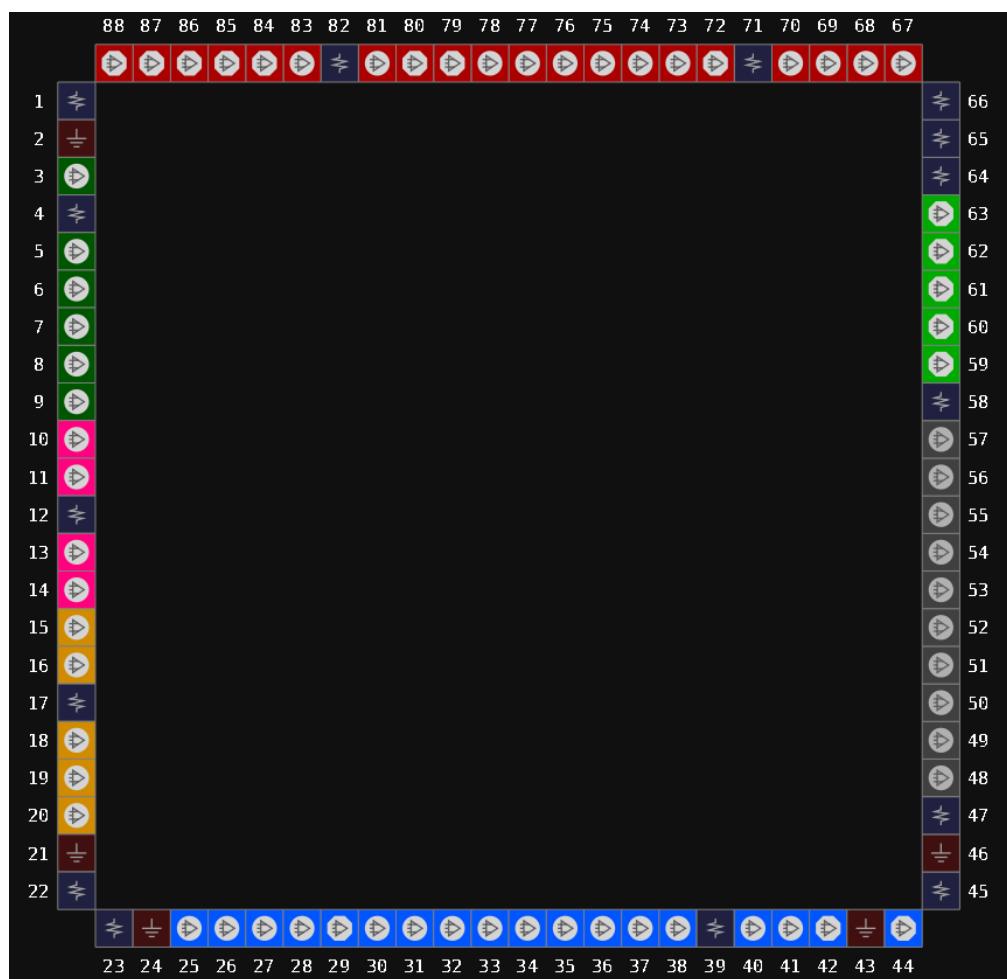


Table 3-31 Other Pins in GW1N-2 QN88(LV Version)

VCC	1,22,45,66
VCCIO0	71,82
VCCIO1	65
VCCIO2	23,39
VCCIO3	17
VCCIO4	12
VCCIO5	4
VCCX	47,64
VCCD/VCCIOD	58
VSS	2,21,24,43,46

3.2.31 View of QN88 Pins Distribution (UV Version)

Figure 3-32 View of GW1N-2 QN88 Pins Distribution (UV Version, Top View)

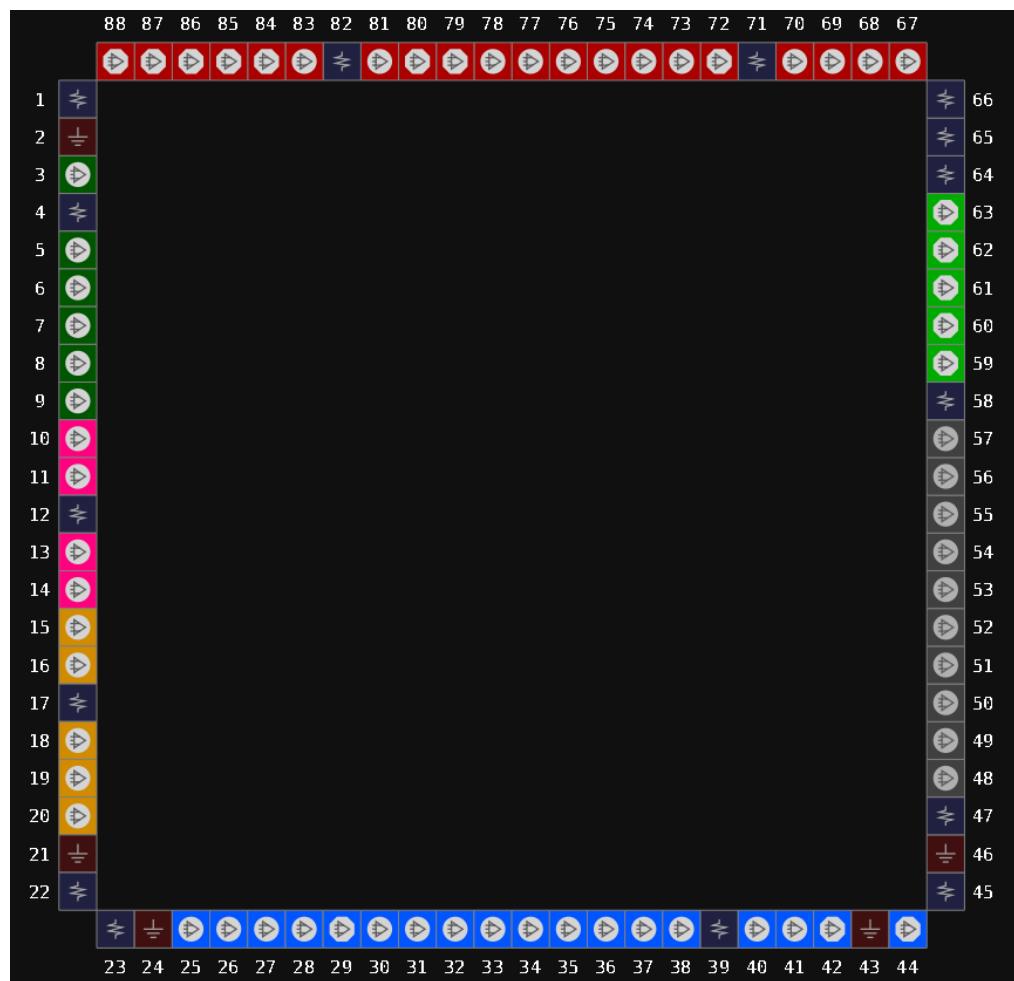


Table 3-32 Other Pins in GW1N-2 QN88(UV Version)

VCC	1,22,45,66
VCCIO0	71,82
VCCIO1	65
VCCIO2	23,39
VCCIO3	17
VCCIO4	12
VCCIO5	4
VCCX	47,64
VCCD/VCCIOD	58
VSS	2,21,24,43,46

3.3 View of GW1N-1P5 Pins Distribution

3.3.1 View of LQ100X Pins Distribution (LV Version)

Figure 3-33 View of GW1N-1P5 LQ100X Pins Distribution (LV Version, Top View)

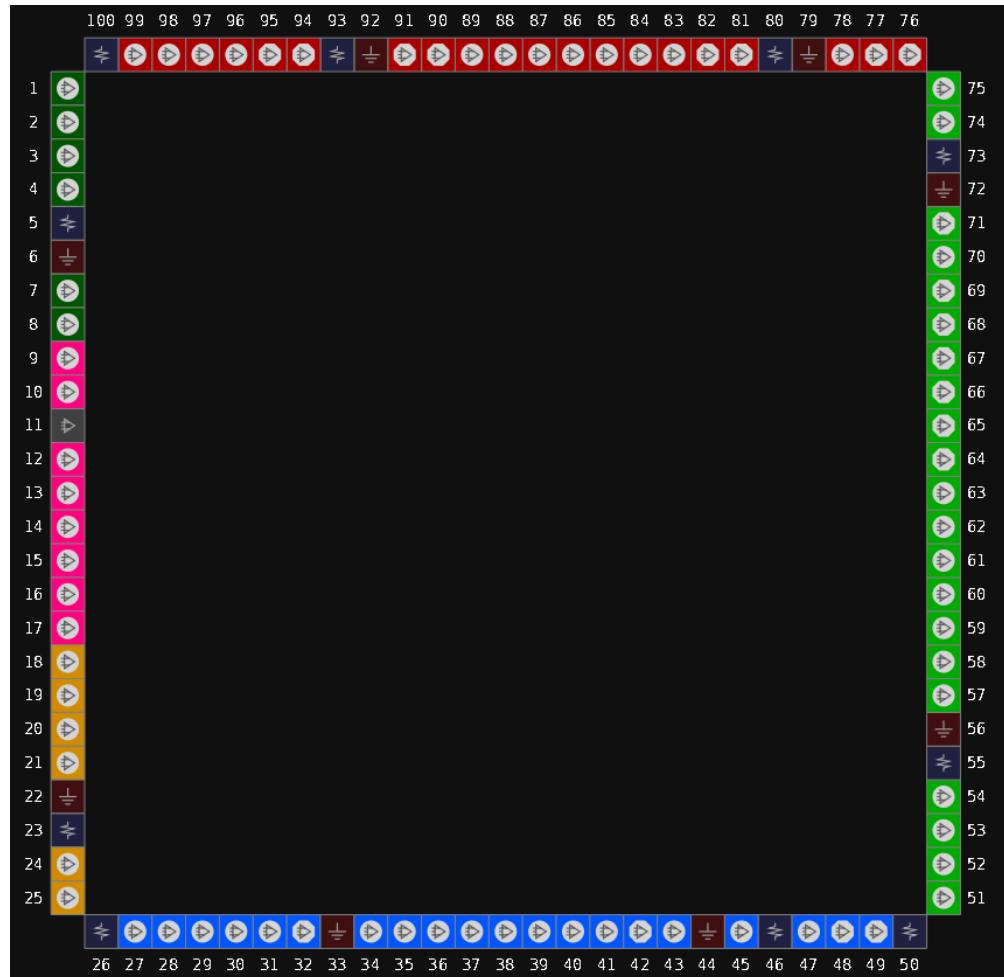


Table 3-33 Other Pins in GW1N-1P5 LQ100X (LV Version)

VCC	100,50
VCCIO0	80,93
VCCIO2	26,46
VCCIO3	23
VCCIO4/VCCIO5	5
VCCIO1/VCCX	55,73
VSS	6,22,33,44,56,72,79,92
NC	11

3.3.2 View of LQ100X Pins Distribution (UV Version)

Figure 3-34 View of GW1N-1P5 LQ100X Pins Distribution (UV Version, Top View)

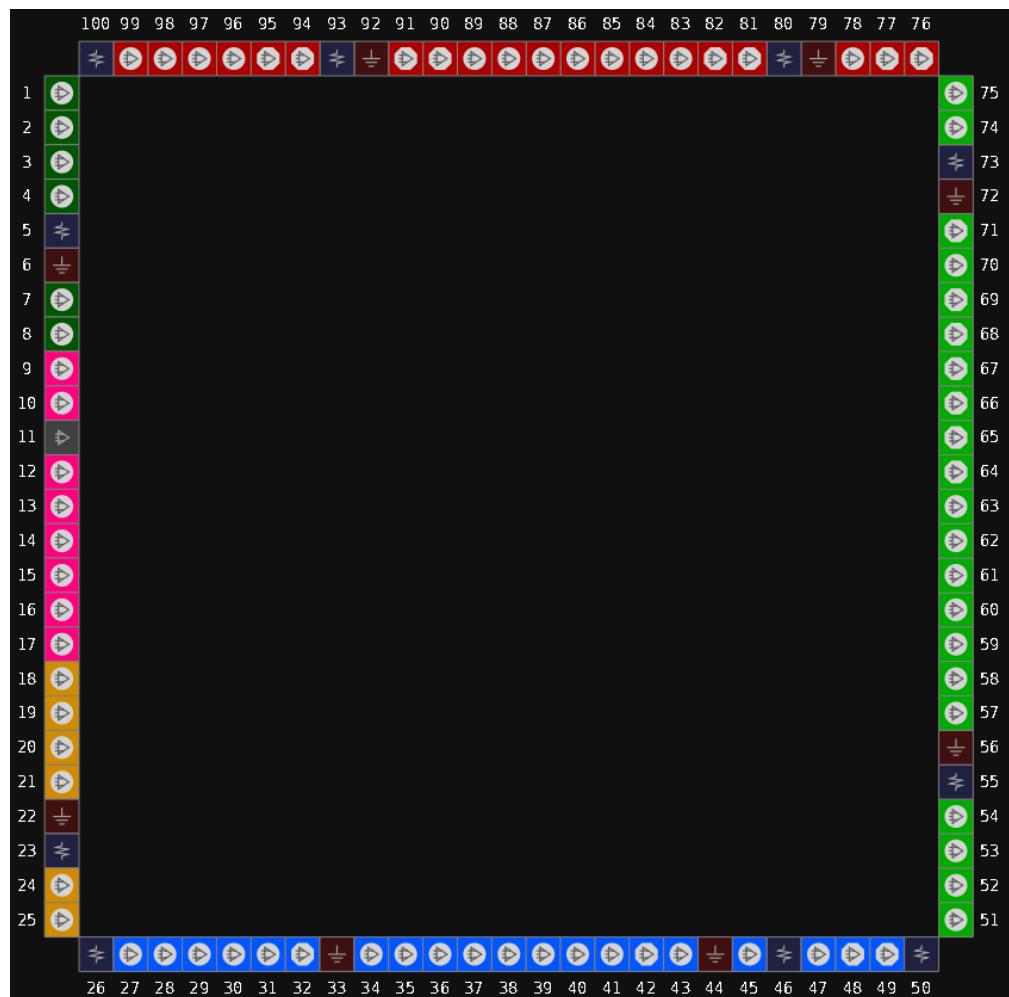


Table 3-34 Other Pins in GW1N-1P5 LQ100X (UV Version)

VCCIO0	80,93
VCCIO1	55,73
VCCIO2	26,46
VCCIO3	23
VCCIO4/VCCIO5	5
VCC/VCCX	100,50
VSS	6,22,33,44,56,72,79,92
NC	11

3.3.3 View of LQ100 Pins Distribution (LV Version)

Figure 3-35 View of GW1N-1P5 LQ100 Pins Distribution (LV Version, Top View)

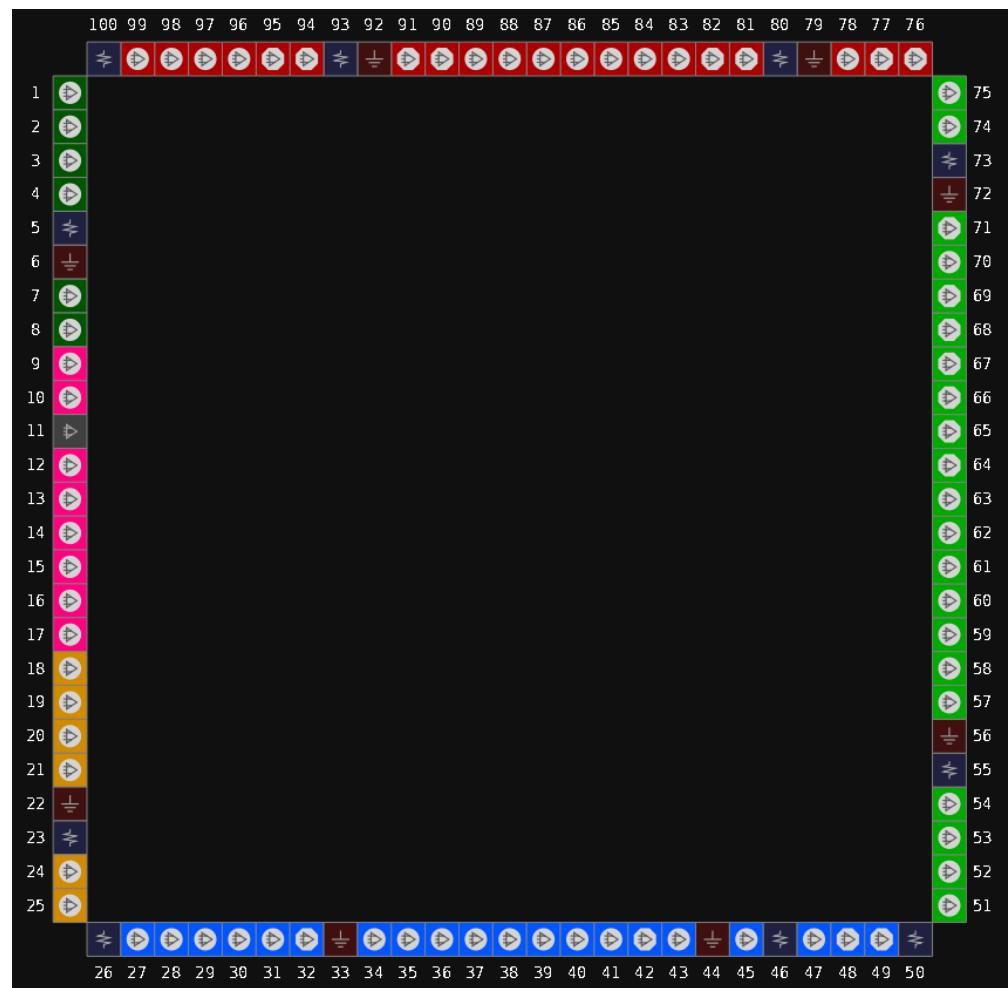


Table 3-35 Other Pins in GW1N-1P5 LQ100 (LV Version)

VCC	100,50
VCCIO0	80,93
VCCIO2	26,46
VCCIO3	23
VCCIO4/VCCIO5	5
VCCIO1/VCCX	55,73
VSS	6,22,33,44,56,72,79,92
NC	11

3.3.4 View of LQ100 Pins Distribution (UV Version)

Figure 3-36 View of GW1N-1P5 LQ100 Pins Distribution (UV Version, Top View)

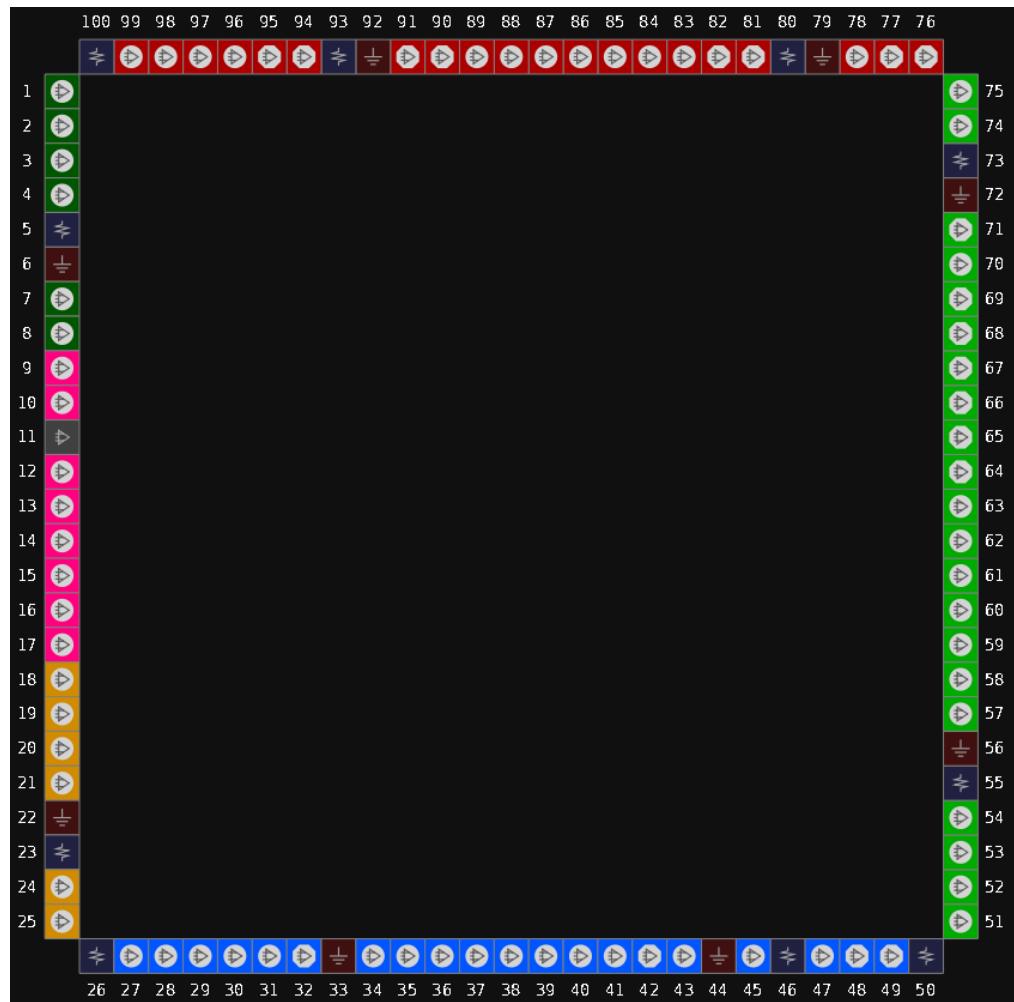


Table 3-36 Other Pins in GW1N-1P5 LQ100 (UV Version)

VCCIO0	80,93
VCCIO1	55,73
VCCIO2	26,46
VCCIO3	23
VCCIO4/VCCIO5	5
VCC/VCCX	100,50
VSS	6,22,33,44,56,72,79,92
NC	11

3.3.5 View of QN48X Pins Distribution (LV Version)

Figure 3-37 View of GW1N-1P5 QN48X Pins Distribution (LV Version, Top View)

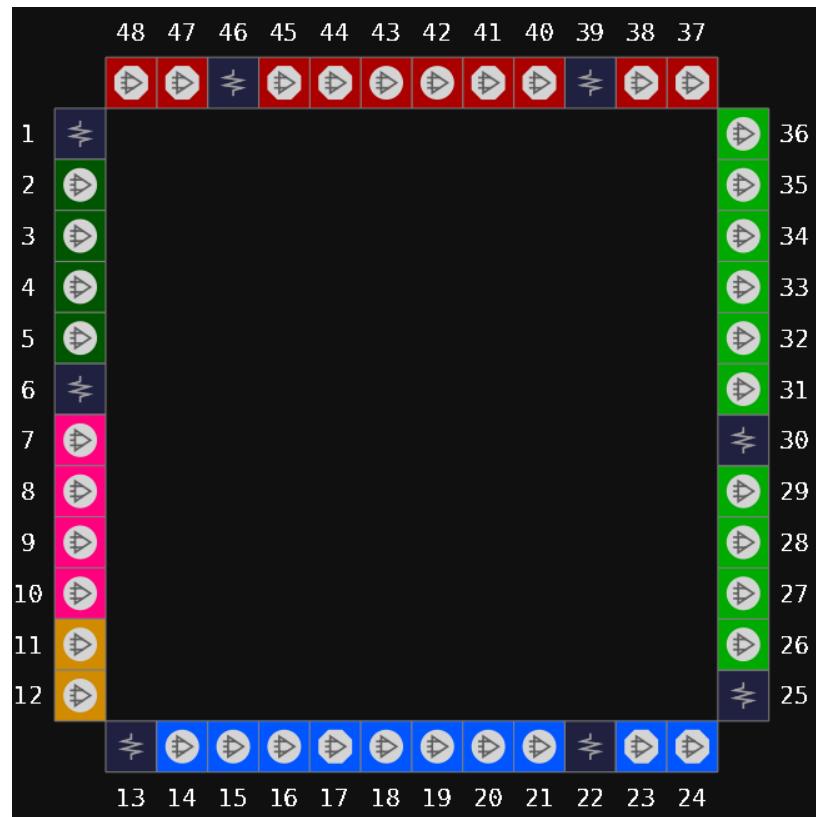


Table 3-37 Other Pins in GW1N-1P5 QN48X (LV Version)

VCC	1,25
VCCIO0	39,46
VCCIO2	13,22
VCCIO3/VCCIO4/VCCIO5	6
VCCIO1/VCCX	30

3.3.6 View of QN48X Pins Distribution (UV Version)

Figure 3-38 View of GW1N-1P5 QN48X Pins Distribution (UV Version, Top View)

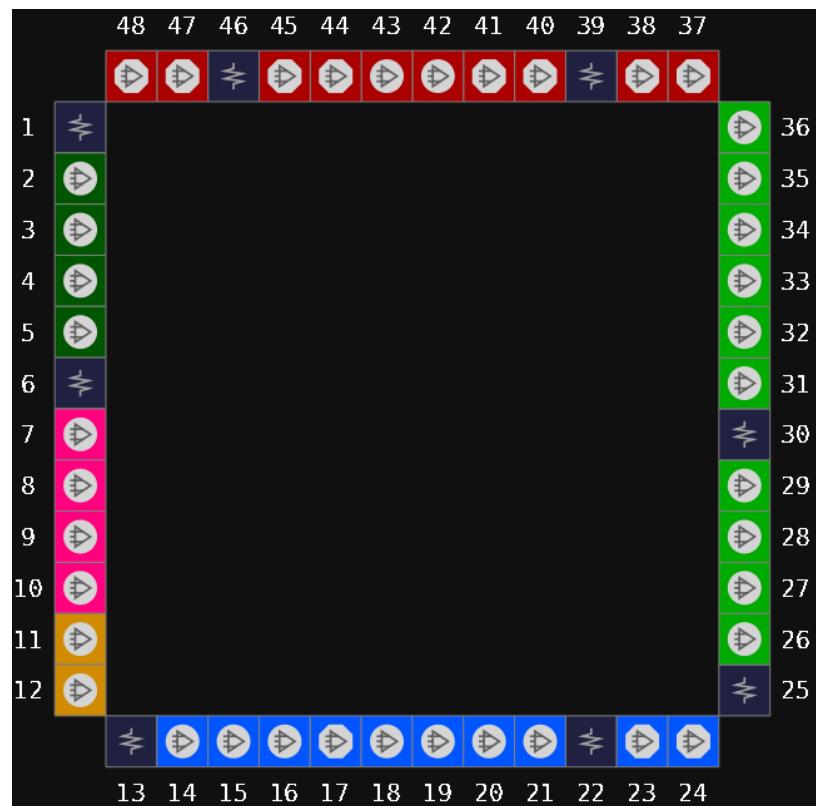


Table 3-38 Other Pins in GW1N-1P5 QN48X (UV Version)

VCC/VCCX	1,25
VCCIO0	39,46
VCCIO1	30
VCCIO2	13,22
VCCIO3/VCCIO4/VCCIO5	6

3.3.7 View of QN48XF Pins Distribution (LV Version)

Figure 3-39 View of GW1N-1P5 QN48XF Pins Distribution (LV Version, Top View)

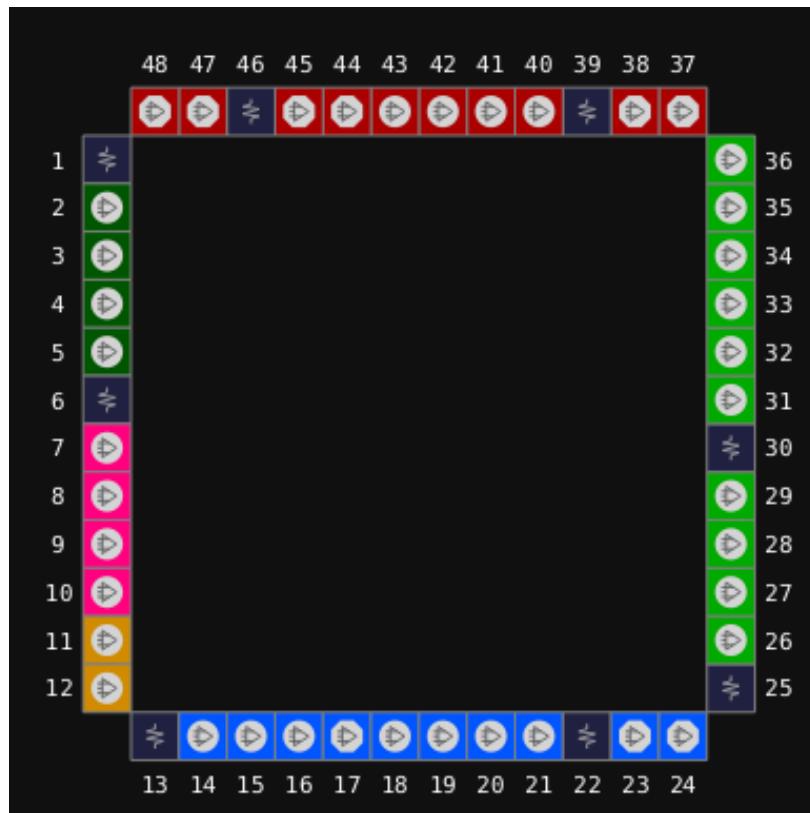


Table 3-39 Other Pins in GW1N-1P5 QN48XF (LV Version)

VCC	1,25
VCCIO0	39,46
VCCIO2	13,22
VCCIO3/VCCIO4/VCCIO5	6
VCCIO1/VCCX	30

3.3.8 View of QN48XF Pins Distribution (UV Version)

Figure 3-40 View of GW1N-1P5 QN48XF Pins Distribution (UV Version, Top View)

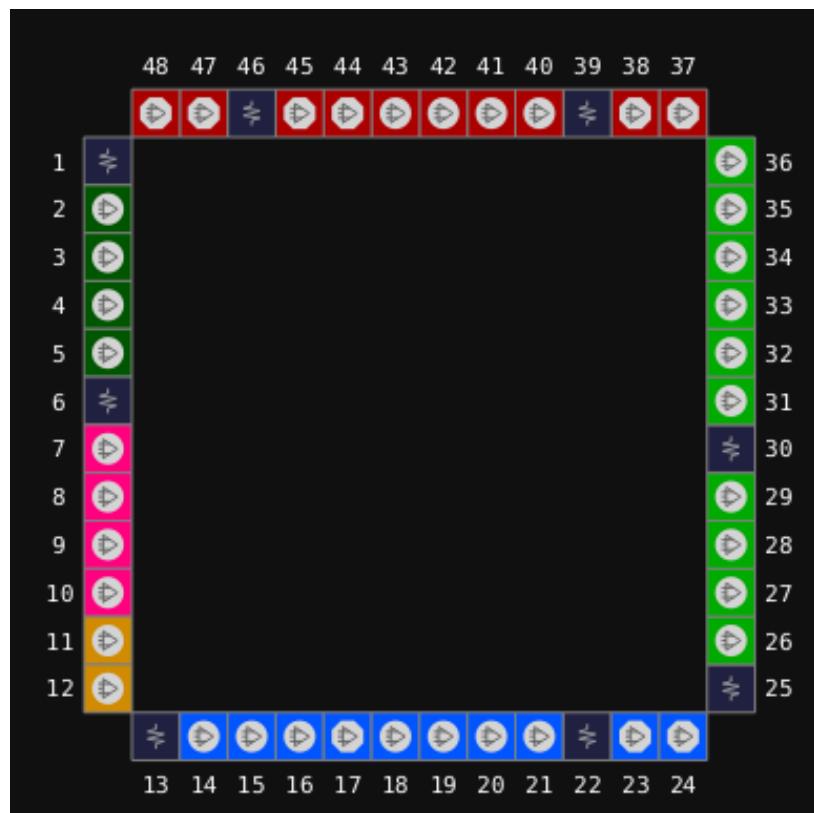


Table 3-40 Other Pins in GW1N-1P5 QN48XF (UV Version)

VCC/VCCX	1,25
VCCIO0	39,46
VCCIO1	30
VCCIO2	13,22
VCCIO3/VCCIO4/VCCIO5	6

3.4 View of GW1N-4 Pins Distribution

3.4.1 View of QN32 Pins Distribution

Figure 3-41 View of GW1N-4 QN32 Pins Distribution (Top View)

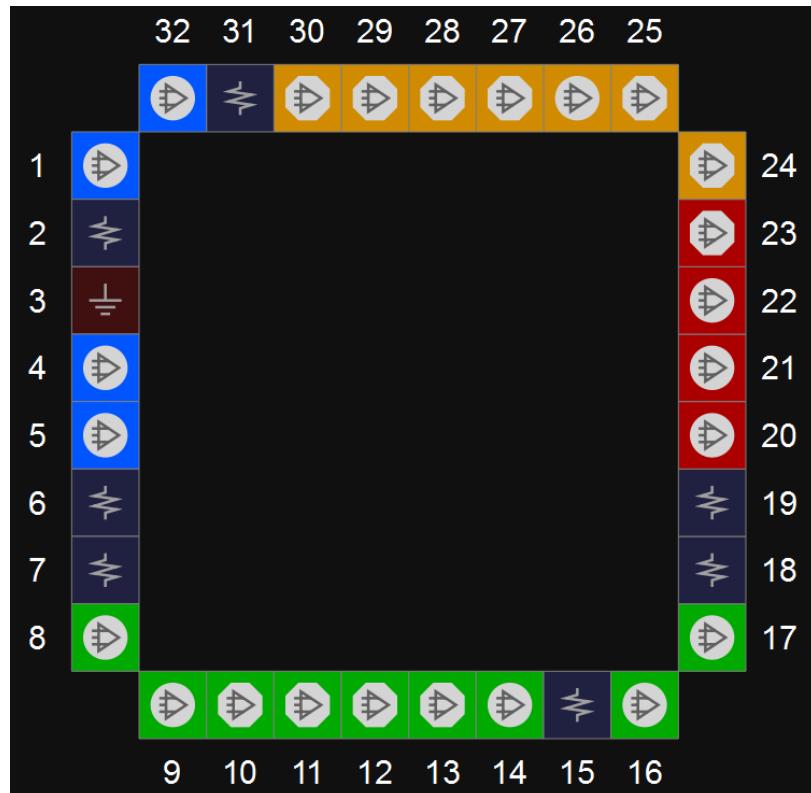


Table 3-41 Other Pins in GW1N-4 QN32

VCC	2, 18
VCCIO0	19
VCCIO1	7
VCCIO2	6
VCCIO3	31
VCCX	15
VSS	3

3.4.2 View of QN48 Pins Distribution

Figure 3-42 View of GW1N-4 QN48 Pins Distribution (Top View)

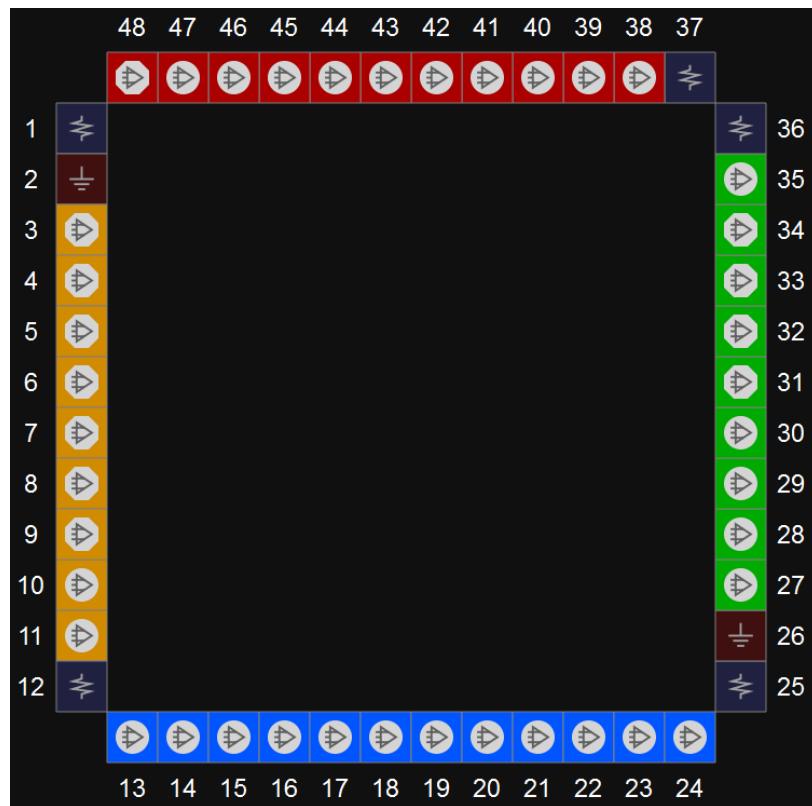


Table 3-42 Other Pins in GW1N-4 QN48

VCC	12, 37
VCCIO0/VCCIO3	1
VCCIO1/VCCIO2	25
VCCX	36
VSS	2, 26

3.4.3 View of CS72 Pins Distribution

Figure 3-43 View of GW1N-4 CS72 Pins Distribution (Top View)

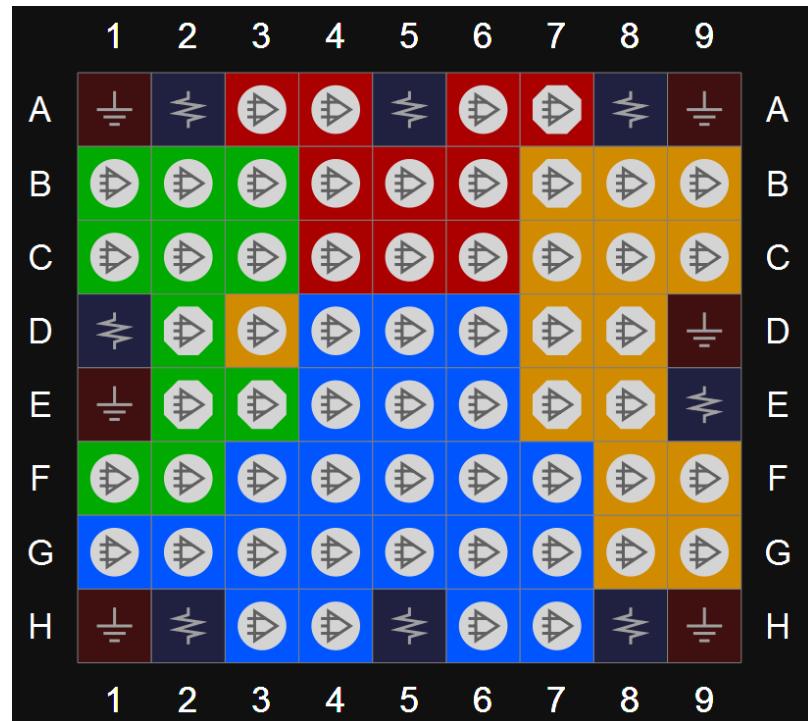


Table 3-43 Other Pins in GW1N-4 CS72

VCC	A2, A8, H8
VCCIO0	A5
VCCIO1	D1
VCCIO2	H5
VCCIO3	E9
VCCX	H2
VSS	A1, A9, D9, E1, H1, H9

3.4.4 View of QN88 Pins Distribution

Figure 3-44 View of GW1N-4 QN88 Pins Distribution (Top View)



Table 3-44 Other Pins in GW1N-4 QN48

VCC	1, 22, 45, 66
VCCIO0	67
VCCIO1	58
VCCIO2	23, 44
VCCIO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

3.4.5 View of LQ100 Pins Distribution

Figure 3-45 View of GW1N-4 LQ100 Pins Distribution (Top View)

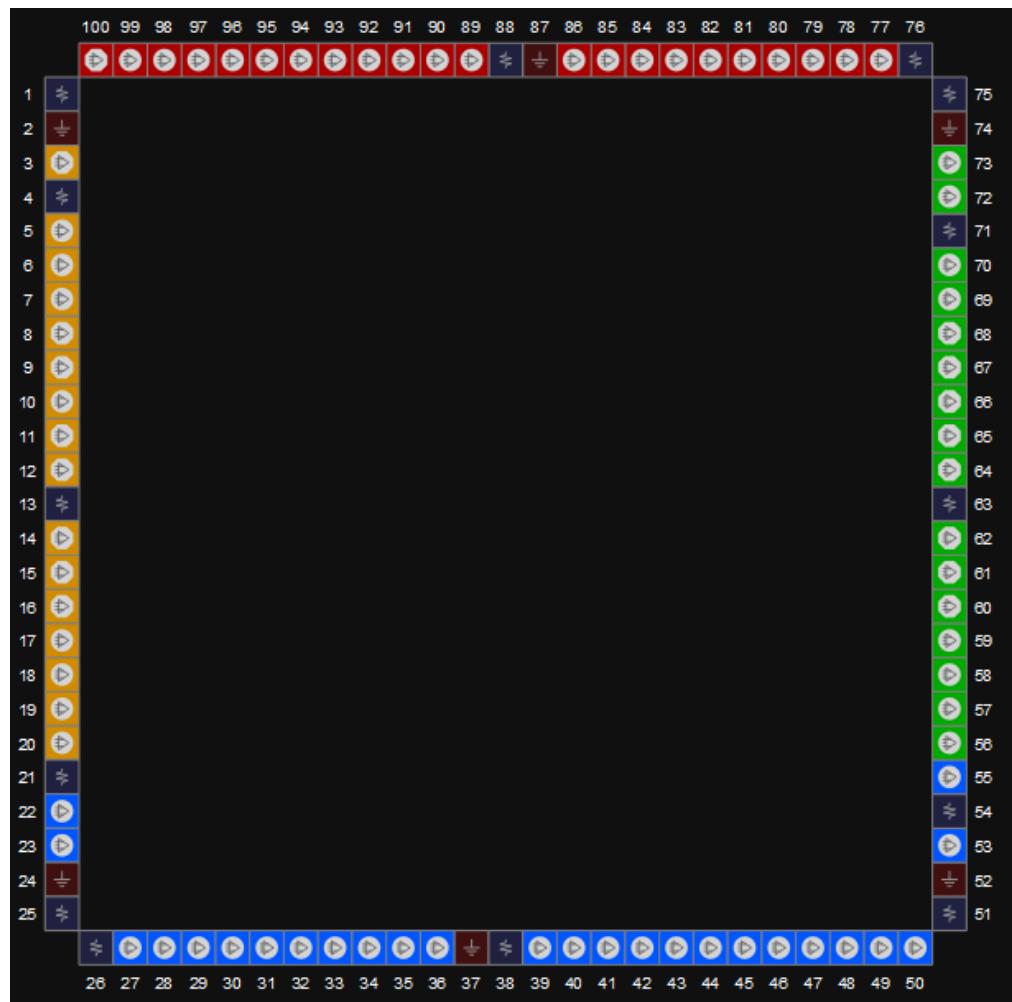


Table 3-45 Other Pins in GW1N-4 LQ100

VCC	1, 25, 51, 75
VCCIO0	76, 88
VCCIO1	54, 63
VCCIO2	26, 38
VCCIO3	4, 13
VCCX	21, 71
VSS	2, 24, 37, 52, 74, 87

3.4.6 View of MG132X Pins Distribution

Figure 3-46 View of GW1N-4 MG132X Pins Distribution (Top View)

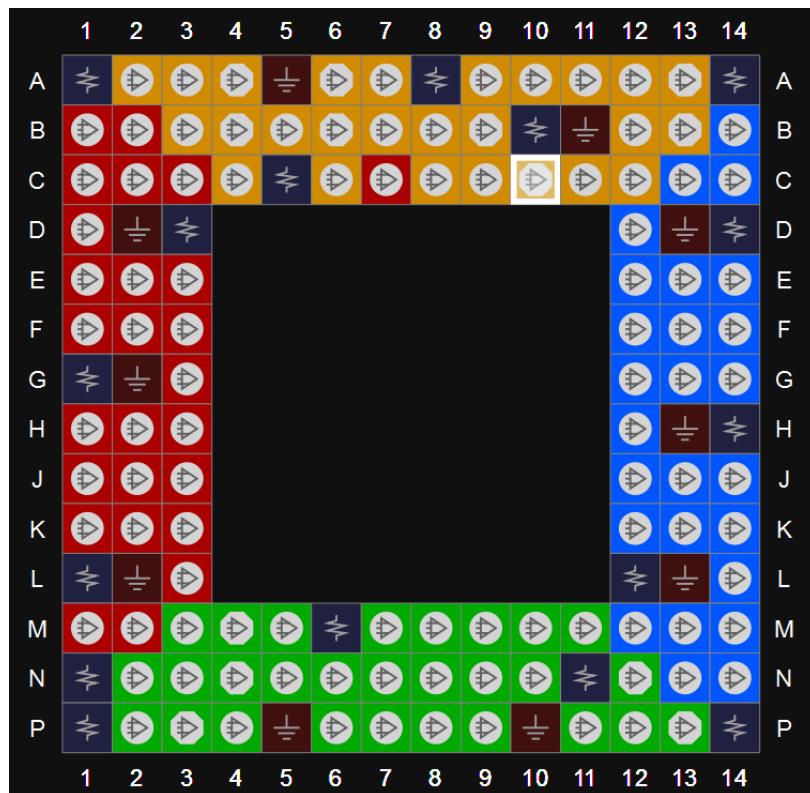


Table 3-46 Other Pins in GW1N-4 MG132X

VCC	A1,A14,N1,P14
VCCIO0	D3,G1,L1
VCCIO1	M6,N11,P1
VCCIO2	D14,H14,L2
VCCIO3	A8,B10,C5
VSS	A5,B11,D13,D2,G2,H13,L13,L2,P10,P5

3.4.7 View of LQ144 Pins Distribution

Figure 3-47 View of GW1N-4 LQ144 Pins Distribution (Top View)



Table 3-47 Other Pins in GW1N-4 LQ144

VCC	1, 36, 73, 108
VCCIO0	109, 127
VCCIO1	77, 91
VCCIO2	37, 55
VCCIO3	5, 19
VCCX	31, 103
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107, 125

3.4.8 View of MG160 Pins Distribution

Figure 3-48 View of GW1N-4 MG160 Pins Distribution (Top View)

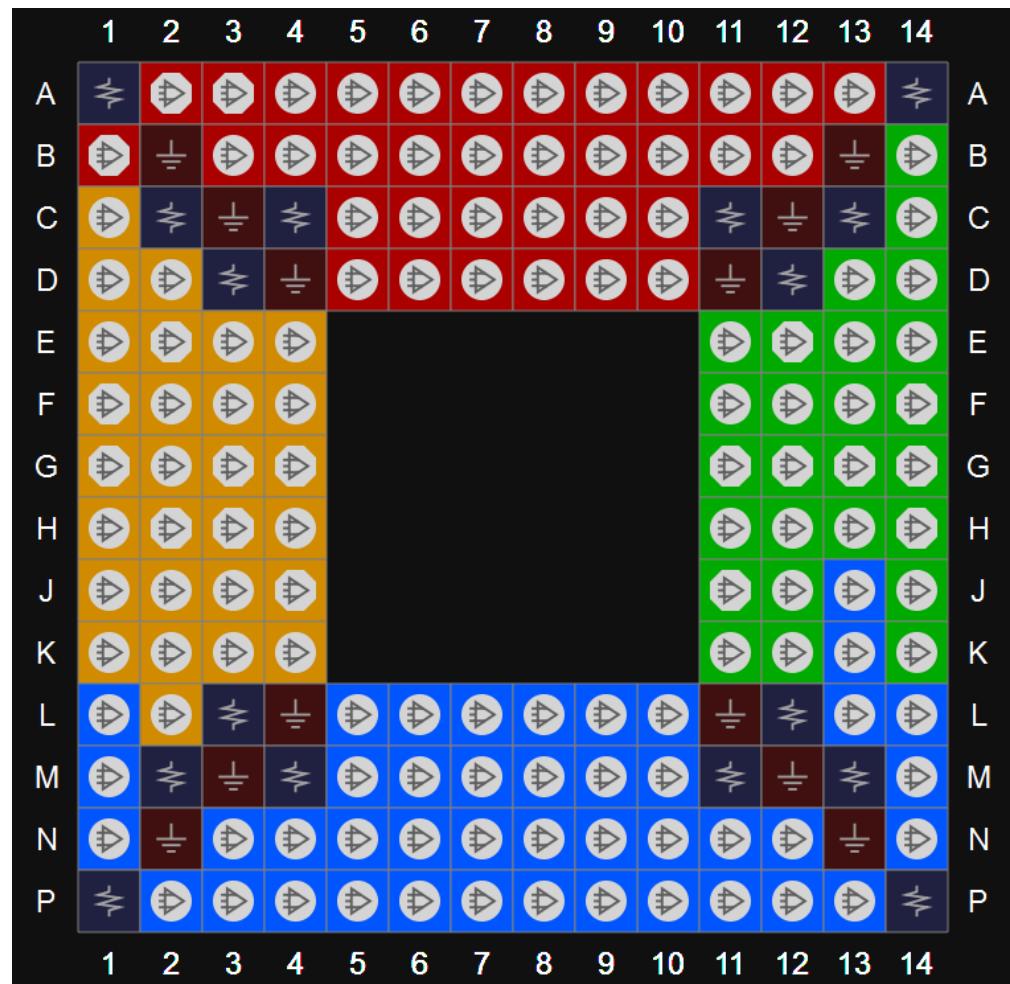


Table 3-48 Other Pins in GW1N-4/MG160

VCC	A1, A14, P1, P14
VCCIO0	C4, C11
VCCIO1	D12, L12
VCCIO2	M4, M11
VCCIO3	D3, L3
VCCX	C2, C13, M2, M13
VSS	B2, B13, C3, C12, D4, D11, L4, L11, M3, M12, N2, N13

3.4.9 View of UG169 Pins Distribution

Figure 3-49 View of GW1N-4 UG169 Pins Distribution (Top View)



Table 3-49 Other Pins for GW1N-4 UG169

VCC	F7, G6, G8, H7
VCCIO0	C6, C7, C8
VCCIO1	F11, G11, H11, J11
VCCIO2	L6, L7, L8
VCCIO3	F2, G3, J3, K3
VCCX	D3, D4, D10, K4, K9
VSS	A1, A13, B8, C3, D2, D5, E2, E11, F3, G7, H12, J4, L9, M6, N1, N13

3.4.10 View of PG256 Pins Distribution

Figure 3-50 View of GW1N-4 PG256 Pins Distribution (Top View)

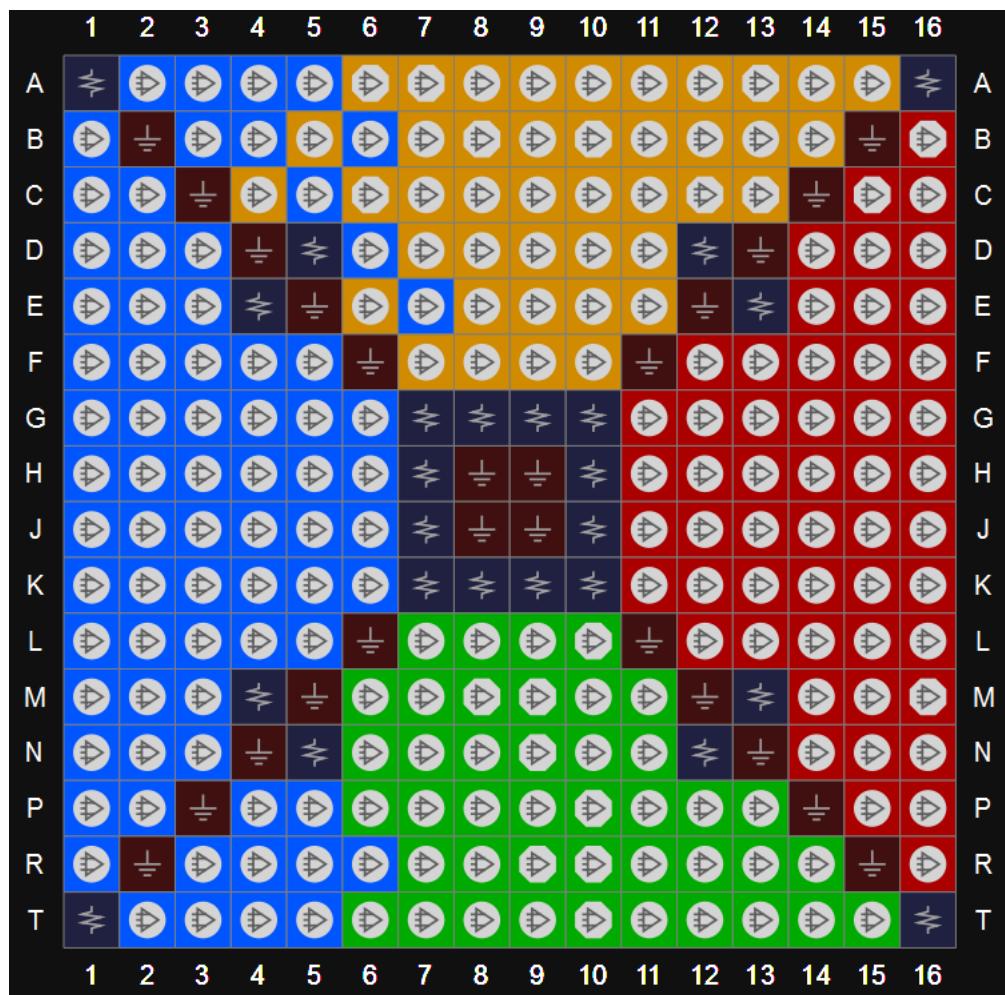


Table 3-50 Other Pins for GW1N-4 PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCCIO0	E13, J10, M13, H10
VCCIO1	K8, N5, N12
VCCIO2	E4, H7, M4, J7
VCCIO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9, J8, J9, L6, L11, M5, M12, N4, N13, P3, P14, R2, R15

3.4.11 View of PG256M Pins Distribution

Figure 3-51 View of GW1N-4 PG256M Pins Distribution (Top View)



Table 3-51 Other Pins in GW1N-4 PG256M

VCC	F10, G11, H10, H8, J7, J9, K6, L7
VCCIO0	A14, A3, F8, F9
VCCIO1	C16, J11, P16
VCCIO2	L8, L9, T3,T14
VCCIO3	C1, H6, P1
VCCX	H11, J6
VSS	A1, A16, B15, B2, F7, G10, G6, G7, G8, G9, K10, K11, K7, K8, K9, L10, R2, R15, T1, H9, H7, J10, J8

3.5 View of GW1N-9 Pins Distribution

3.5.1 View of QN48 Pins Distribution

Figure 3-52 View of GW1N-9 QN48 Pins Distribution (Top View)

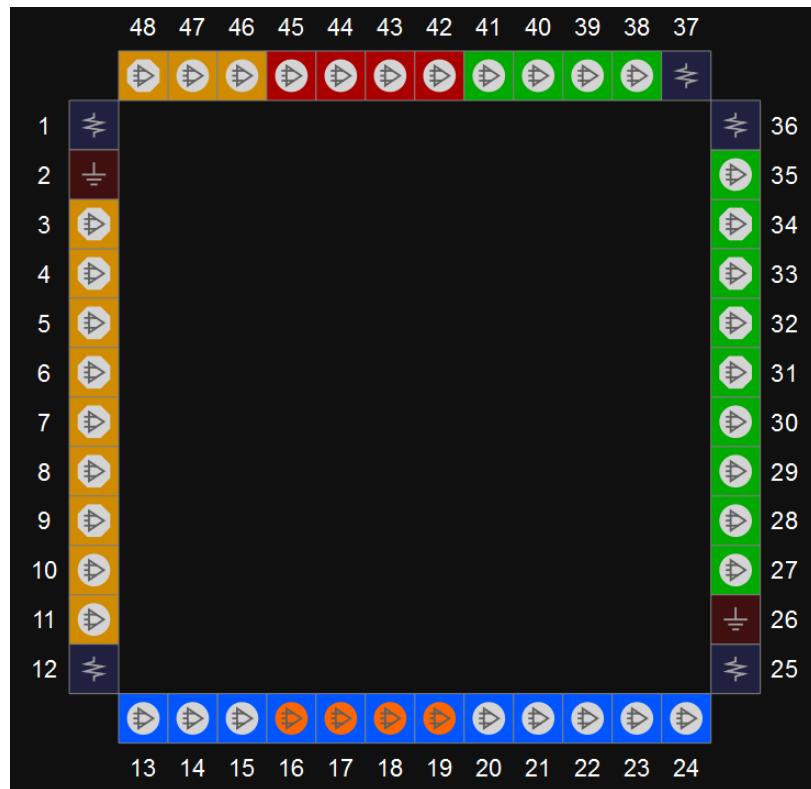


Table 3-52 Other Pins in GW1N-9 QN48

VCC	12, 37
VCCIO0/VCCIO3	1
VCCIO1/VCCIO2	25
VCCX	36
VSS	2, 26

3.5.2 View of CM64 Pins Distribution

Figure 3-53 View of GW1N-9 CM64 Pins Distribution (Top View)

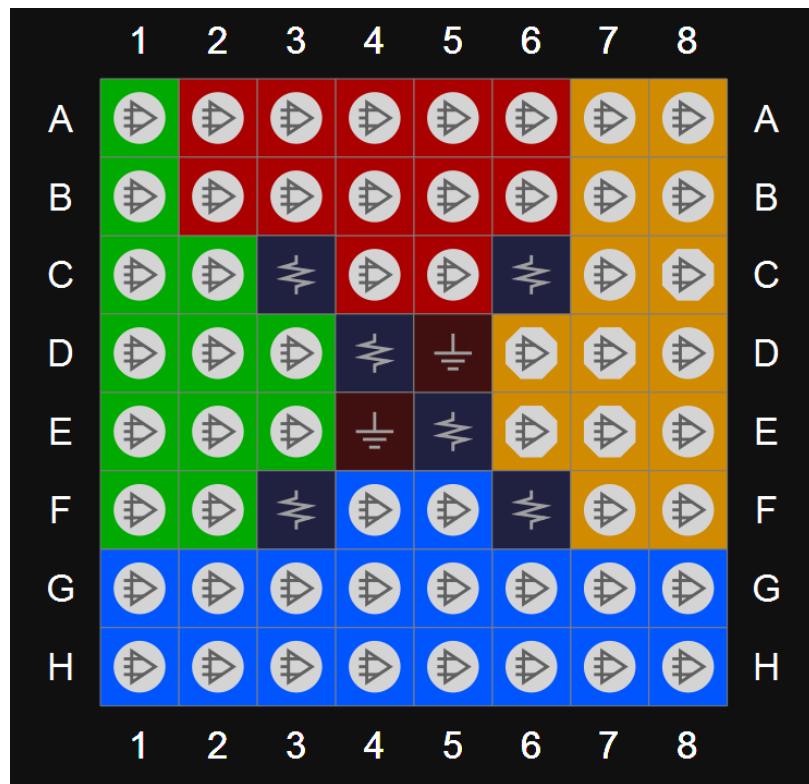


Table 3-53 Other Pins in GW1N-9 CM64

VCC	D4, E5
VCCIO0/VCCIO2	C6
VCCIO1/VCCIO3	F3
VCCX	C3, F6
VSS	D5, E4

3.5.3 View of CS81M Pins Distribution

Figure 3-54 View of GW1N-9 CS81M Pins Distribution (Top View)

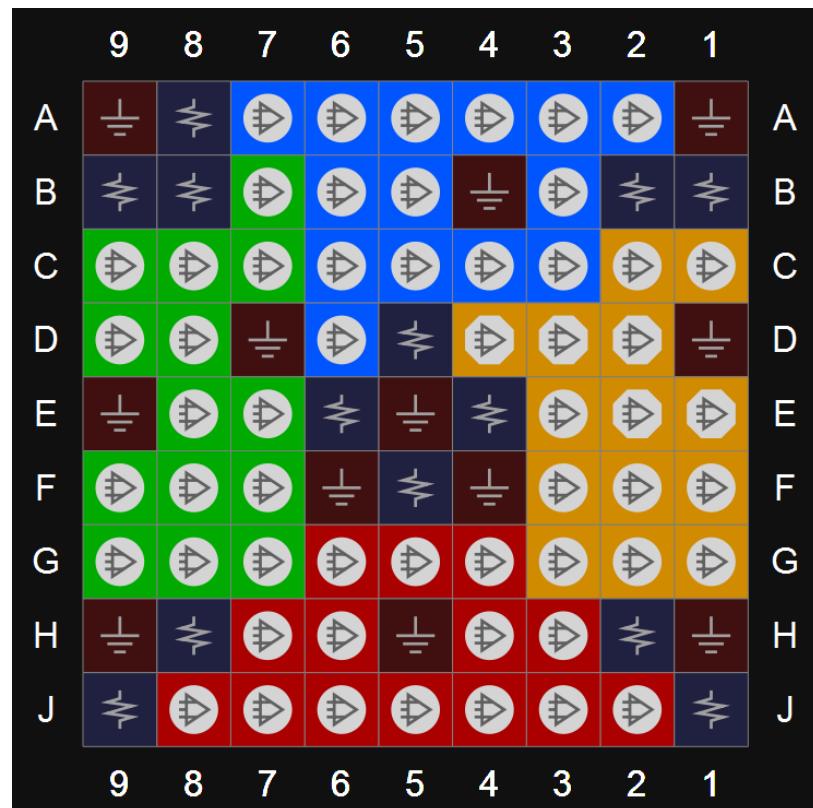


Table 3-54 Other Pins in GW1N-9 CS81M

VCC	A8、B2、B9、H2、H8
VCCIO0	F5
VCCIO1	E6
VCCIO2	D5
VCCIO3	E4
VCCX	B1、B8、J1、J9
VSS	A1、A9、B4、D1、D7、E5、E9、F4、F6、H1、H5、H9

3.5.4 View of QN88 Pins Distribution

Figure 3-55 View of GW1N-9 QN88 Pins Distribution (Top View)

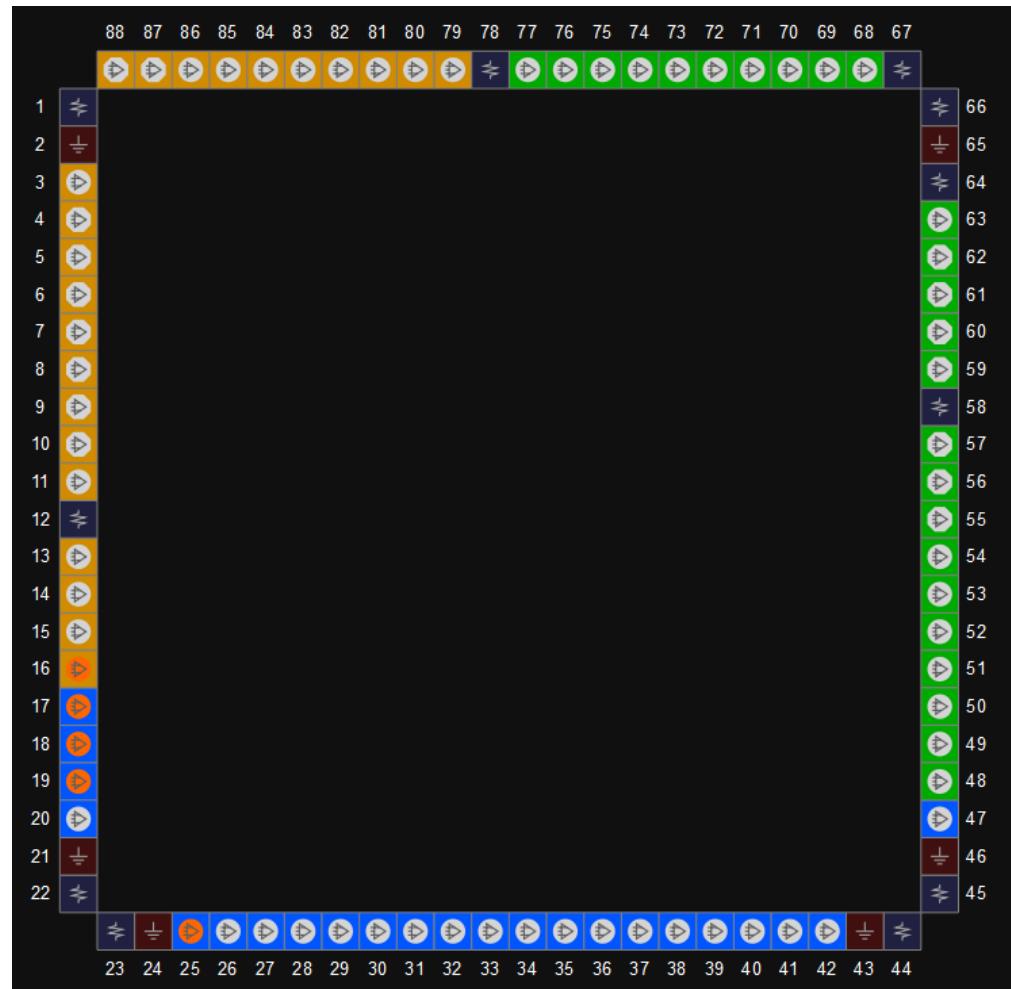


Table 3-55 Other Pins in GW1N-9 QN88

VCC	1, 22, 45, 66
VCCIO0	67
VCCIO1	58
VCCIO2	23, 44
VCCIO3	12
VCCX	64, 78
VSS	2, 21, 24, 43, 46, 65

3.5.5 View of LQ100 Pins Distribution

Figure 3-56 GW1N-9 LQ100 Pins Distribution View (Top View)

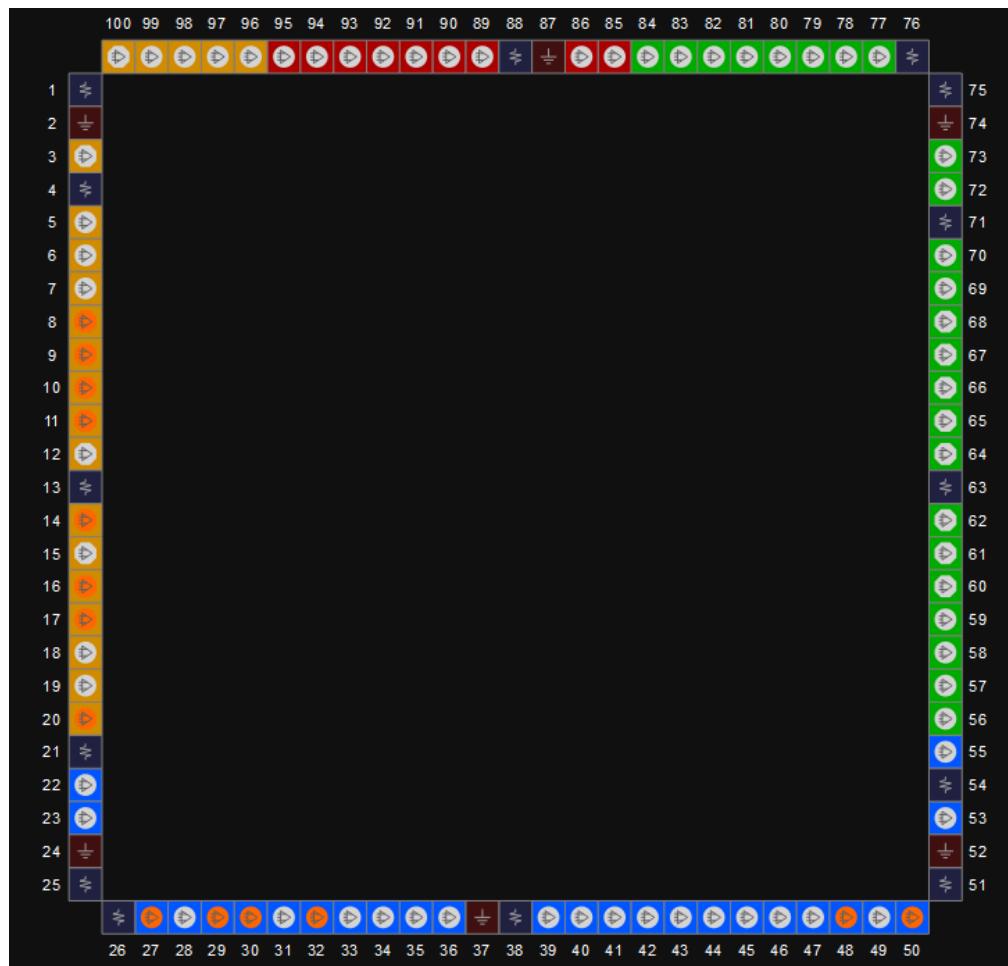


Table 3-56 Other Pins in GW1N-9 LQ100

VCC	1, 25, 51, 75
VCCIO0	76, 88
VCCIO1	63, 71
VCCIO2	26, 38
VCCIO3	4, 13
VCCX	21, 54
VSS	2, 24, 52, 74, 87, 37

3.5.6 View of MG100 Pins Distribution

Figure 3-57 View of GW1N-9 MG100 Pins Distribution (Top View)

	1	2	3	4	5	6	7	8	9	10	
A	±	±	±	±	±	±	±	±	±	±	A
B	±	±	±	±	±	±	±	±	±	±	B
C	±	±	±	±	±	±	±	±	±	±	C
D	±	±	±	±	±	±	±	±	±	±	D
E	±	±	±	±	±	±	±	±	±	±	E
F	±	±	±	±	±	±	±	±	±	±	F
G	±	±	±	±	±	±	±	±	±	±	G
H	±	±	±	±	±	±	±	±	±	±	H
J	±	±	±	±	±	±	±	±	±	±	J
K	±	±	±	±	±	±	±	±	±	±	K
	1	2	3	4	5	6	7	8	9	10	

Table 3-57 Other Pins in GW1N-9 MG100

VCC	A2,A8,J2
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
VSS	A1,A9,J1,J9

3.5.7 View of LQ144 Pins Distribution

Figure 3-58 View of GW1N-9 LQ144 Pins Distribution (Top View)



Table 3-58 Other Pins in GW1N-9 LQ144

VCC	1, 36, 73, 108
VCCIO0	109, 127
VCCIO1	103, 91
VCCIO2	37, 55
VCCIO3	5, 19
VCCX	31, 77
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107, 107, 125

3.5.8 View of EQ144 Pins Distribution

Figure 3-59 View of GW1N-9 EQ144 Pins Distribution (Top View)



Table 3-59 Other Pins in GW1N-9 EQ144

VCC	1, 36, 73, 108
VCCIO0	109, 127
VCCIO1	103, 91
VCCIO2	37, 55
VCCIO3	5, 19
VCCX	31, 77
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107

3.5.9 View of MG160 Pins Distribution

Figure 3-60 GW1N-9 MG160 Pins Distribution View (Top View)

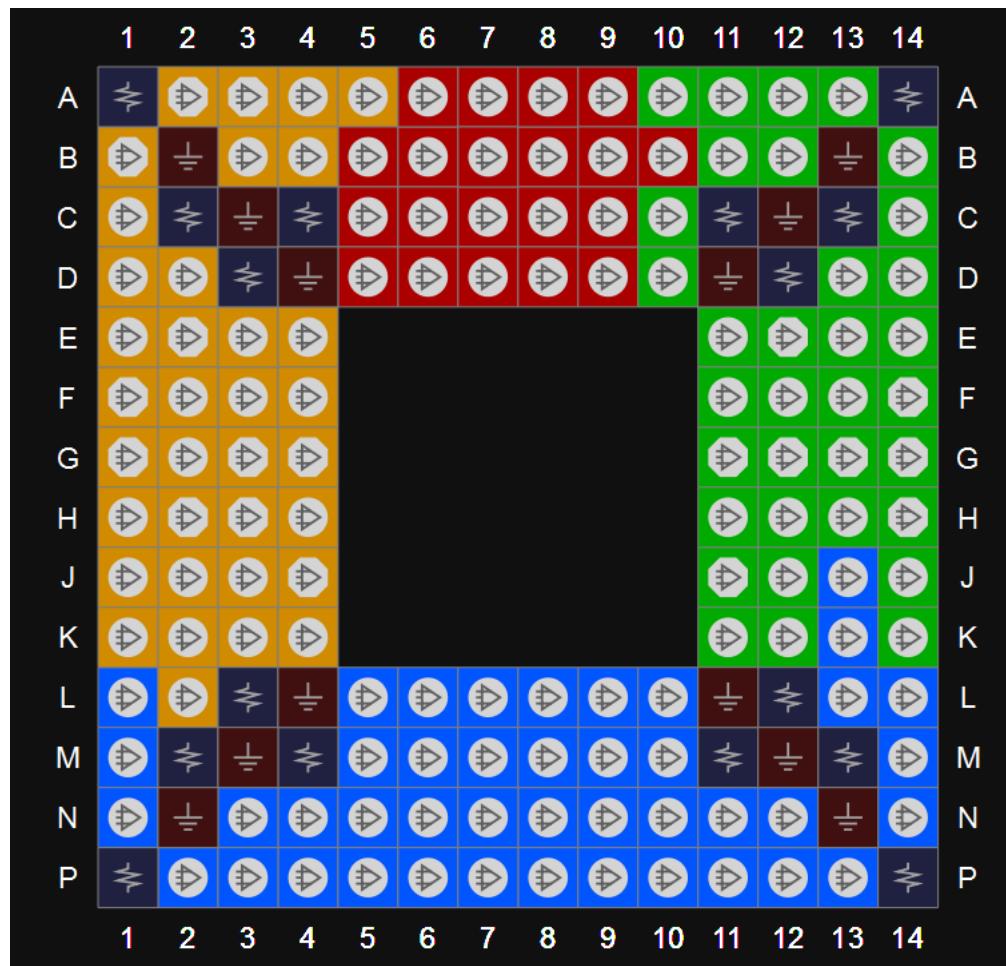


Table 3-60 Other Pins in GW1N-9 MG160

VCC	A1, A14, P1, P14
VCCIO0	C4, C11
VCCIO1	D12, L12
VCCIO2	M11, M4
VCCIO3	D3, L3
VCCX	C13, C2, M13, M2
VSS	B13, B2, C12, C3, D11, D4, L11, L4, M12, M3, N13, N2

3.5.10 View of UG169 Pins Distribution

Figure 3-61 View of GW1N-9 UG169 Pins Distribution (Top View)



Table 3-61 Other Pins for GW1N-9 UG169

VCC	F7,G6,G8,H7
VCCIO0	C6,C7,C8
VCCIO1	F11,G11,H11,J11
VCCIO2	L6,L7,L8
VCCIO3	F2,G3,J3,K3
VCCX	D10,D3,D4,K4,K9
VSS	A1,A13,B8,C3,D2,D5,E11,E2,F3,G7,H12,J4,L9,M6,N1,N13

3.5.11 View of LQ176 Pins Distribution

Figure 3-62 View of GW1N-9 LQ176 Pins Distribution (Top View)



Table 3-62 Other Pins for GW1N-9 LQ176

VCC	1, 44, 89, 132
VCCIO0	133, 155, 176
VCCIO1	95, 110, 115
VCCIO2	45, 65, 88
VCCIO3	13, 22, 34
VCCX	40, 66, 130, 154
VSS	2, 43, 46, 87, 90, 131, 134, 175

3.5.12 View of EQ176 Pins Distribution

Figure 3-63 View of GW1N-9 EQ176 Pins Distribution (Top View)



Table 3-63 Other Pins in GW1N-9 EQ176

VCC	1, 44, 89, 132
VCCIO0	133, 155, 176
VCCIO1	95, 110, 115
VCCIO2	45, 65, 88
VCCIO3	13, 22, 34
VCCX	40, 66, 130, 154
VSS	2, 43, 46, 87, 90, 131, 134, 175

3.5.13 View of MG196 Pins Distribution

Figure 3-64 View of GW1N-9 MG196 Pins Distribution (Top View)

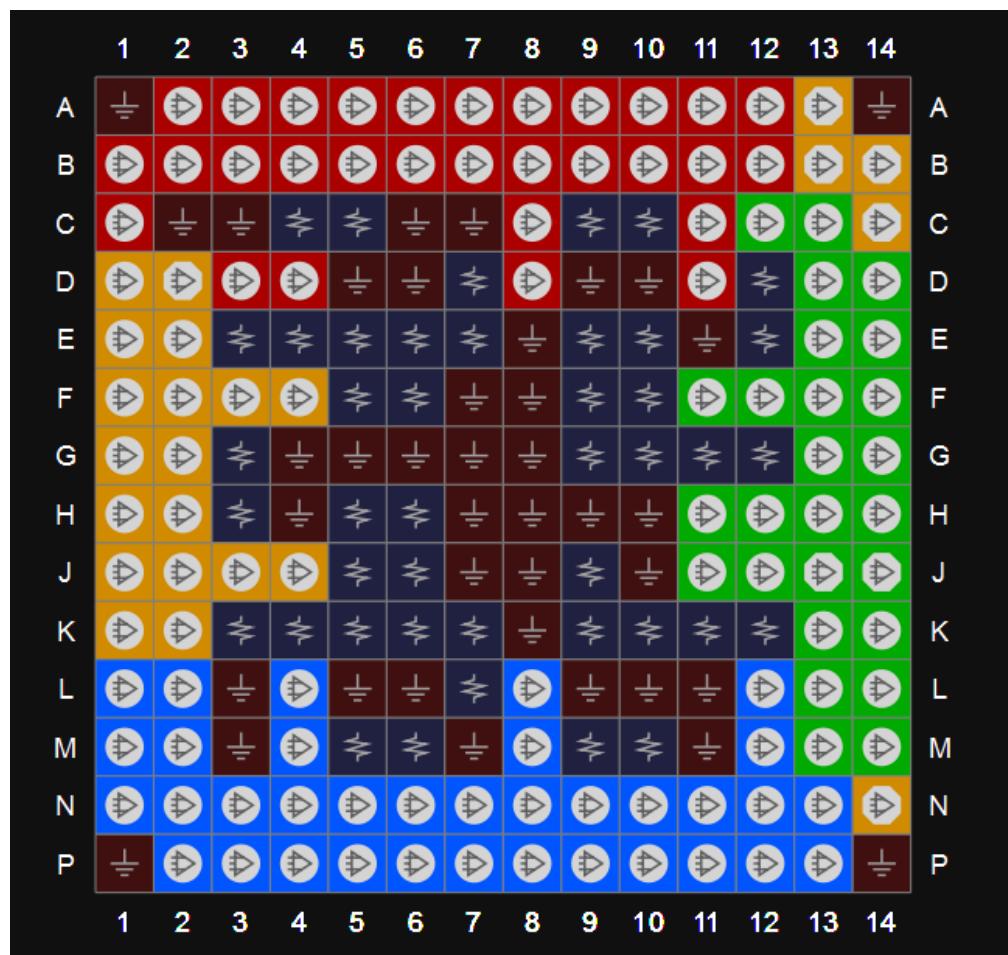


Table 3-64 Other Pins in GW1N-9 MG196

VCC	E10,E5,E6,E9,F10,F5,F6,F9,J5,J6,J9,K10,K5,K6,K9
VCCIO0	C4,C10,C5,C9
VCCIO1	D12,E12,G11,G12,K11,K12
VCCIO2	M5,M10,M6,M9
VCCIO3	E3,E4,G3,H3,K3,K4
VCCX	L7,K7,H6,H5,D7,E7,G10,G9
VSS	A14,A1,C3,C2,C7,C6,D5,D10,D9,D6,E8,E11,F7,F8,G4,G5,G6, G7,G8,H10,H4,H7,H8,H9,J10,J7,J8,K8,L10,L11,L3,L5,L6,L9,M 11,M3,M7,P1,P14

3.5.14 View of PG256 Pins Distribution

Figure 3-65 View of GW1N-9 PG256 Pins Distribution (Top View)

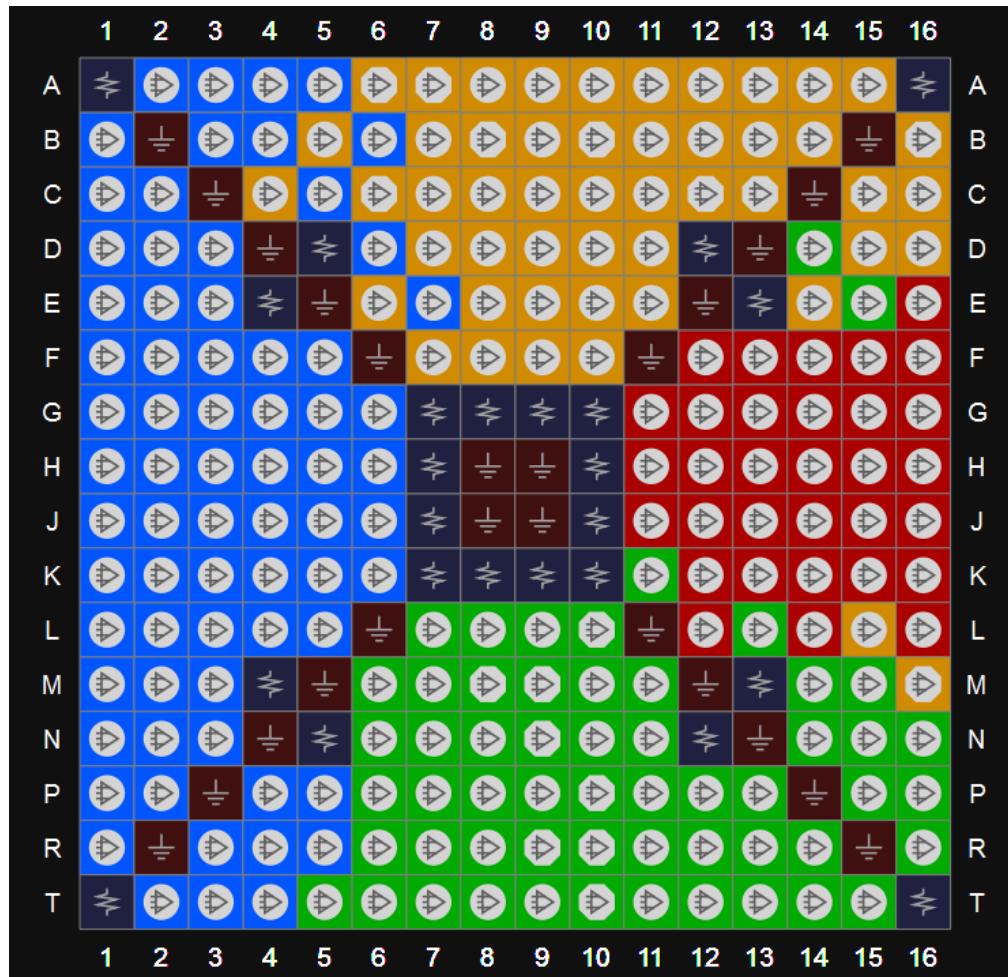


Table 3-65 Other Pins in GW1N-9 PG256

VCC	A1, A16, G7, G10, K7, K10, T1, T16
VCCIO0	E13, J10, M13, H10
VCCIO1	K8, N5, N12
VCCIO2	E4, H7, M4, J7
VCCIO3	D12, D5, G9
VCCX	G8, K9
VSS	B2, B15, C3, C14, D4, D13, E5, E12, F6, F11, H8, H9, J8, J9, L6, L11, M5, M12, N4, N13, P3, P14, R2, R15

3.5.15 View of UG256 Pins Distribution

Figure 3-66 View of GW1N-9 UG256 Pins Distribution (Top View)

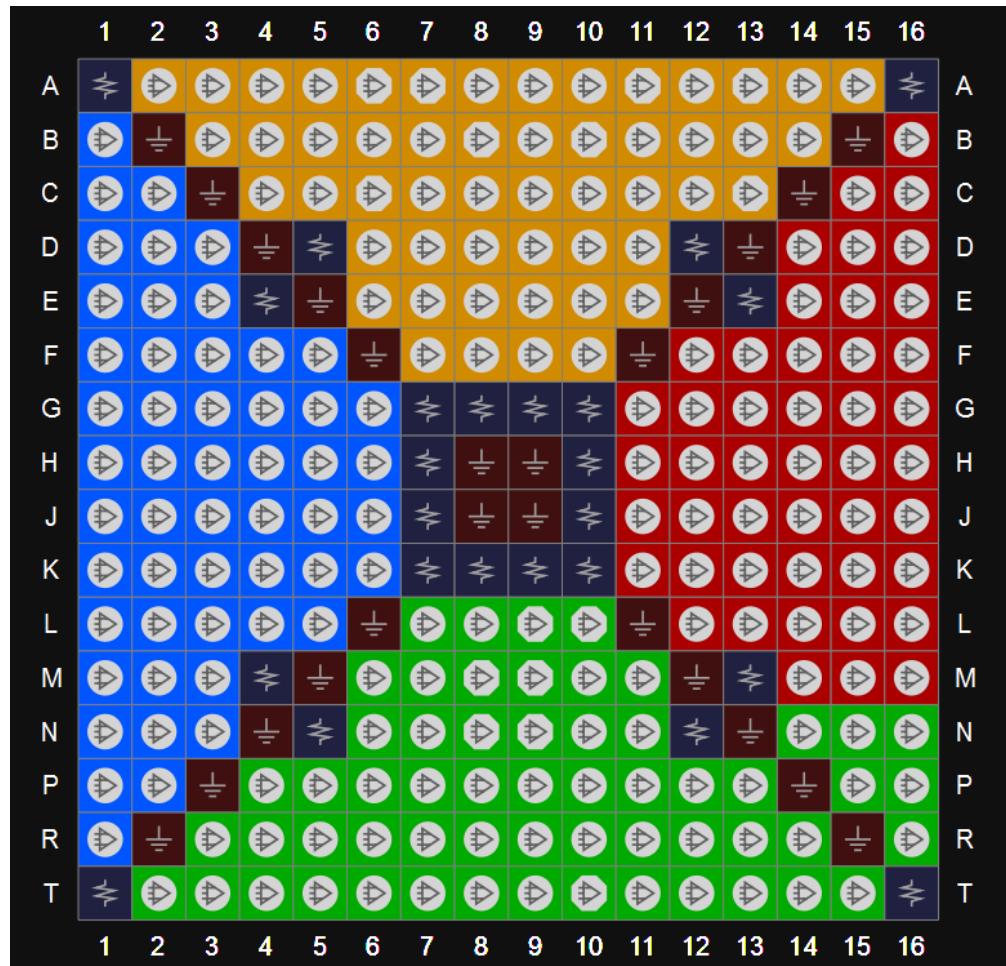


Table 3-66 Other Pins in GW1N-9 UG256

VCC	A1, A16, G10, G7, K10, K7, T1, T16
VCCIO0	E13, H10, J10, M13
VCCIO1	K8, K9, N12,N5
VCCIO2	E4, H7, J7, M4
VCCIO3	D12, D5, G9
VCCX	G8
VSS	B15, B2, C14, C3, D13, D4, E12, E5, F11, F6, H8, H9, J8, J9, L11, L6, M12, M5, N13, N4, P14, P3, R15, R2

3.5.16 View of UG332 Pins Distribution

Figure 3-67 View of GW1N-9 UG332 Pins Distribution (Top View)

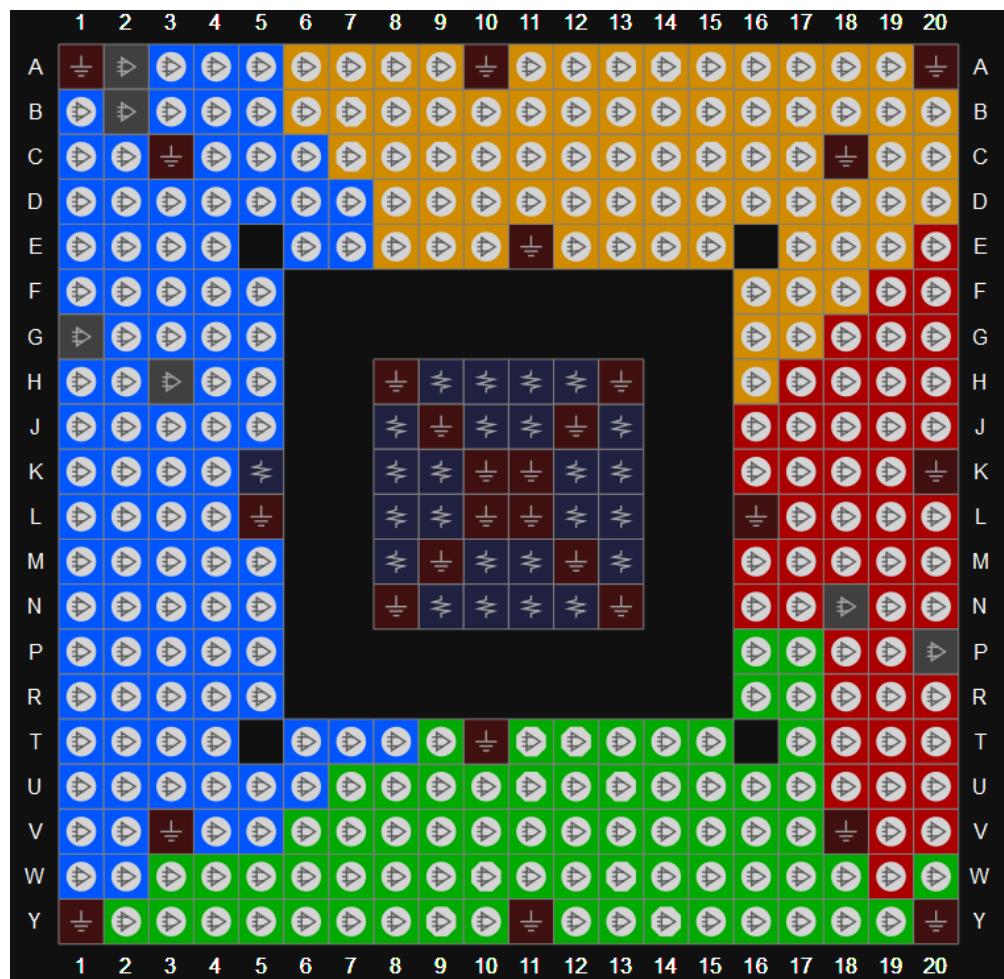


Table 3-67 Other Pins in GW1N-9 UG332

VCC	J10, J11, K9, K12, L9, L12, M10, M11
VCCIO0	J13, K13, L13
VCCIO1	N9, N10, N1, N12
VCCIO2	J8, K5, K8, L8, M8
VCCIO3	H11, H9, H12
VCCX	H10, M13
VSS	A1, A10, A20, C3, C18, E11, H8, H13, J9, J12, K10, K11, K20, L5, L10, L11, L16, M9, M12, N8, N13, T10, V3, V18, Y1, Y11, Y20
NC	N18, P20, G1, H3, A2, B2

3.5.17 View of QN48F Pins Distribution

Figure 3-68 View of GW1N-9 QN48F Pins Distribution (Top View)

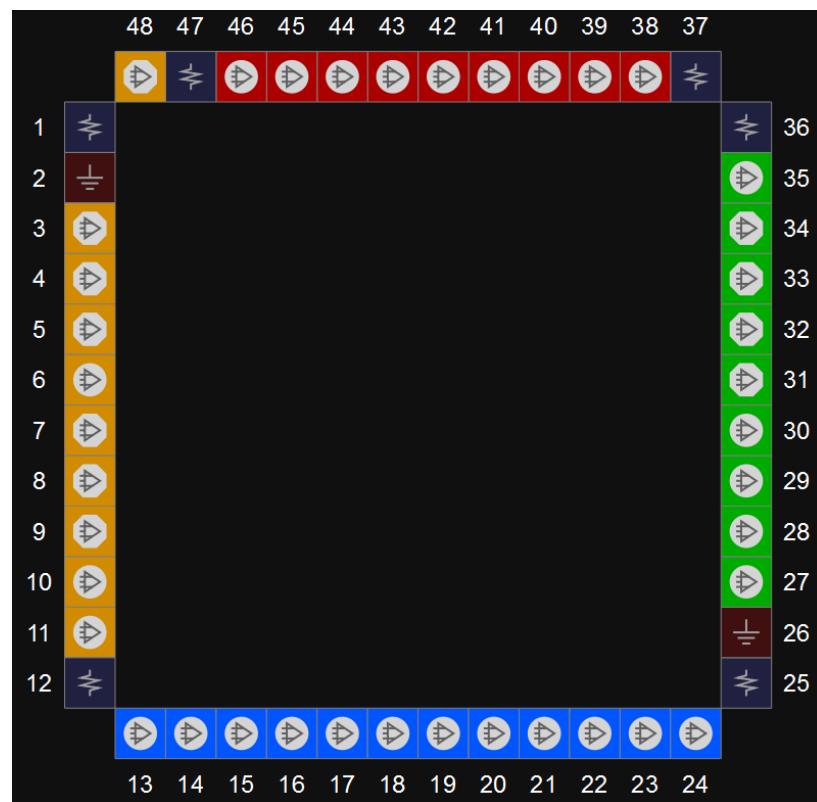


Table 3-68 Other Pins in GW1N-9 QN48F

VCC	12,37
VCCIO0	47
VCCIO3	1
VCCIO1/VCCIO2	25
VCCX	36
VSS	2,26

3.5.18 View of MG100T Pins Distribution

Figure 3-69 View of GW1N-9 MG100T Pins Distribution (Top View)

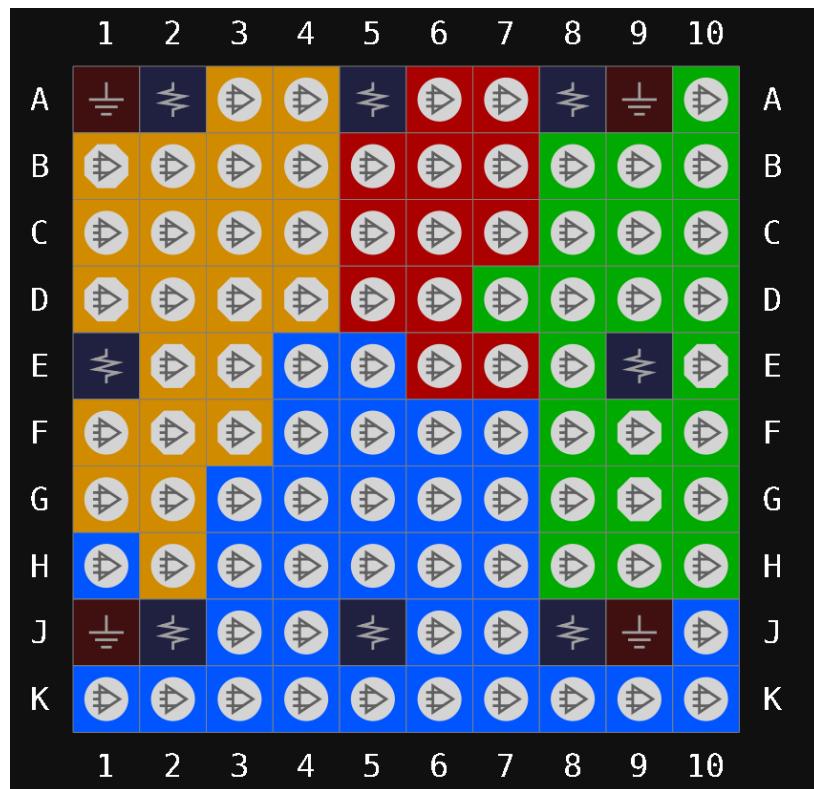


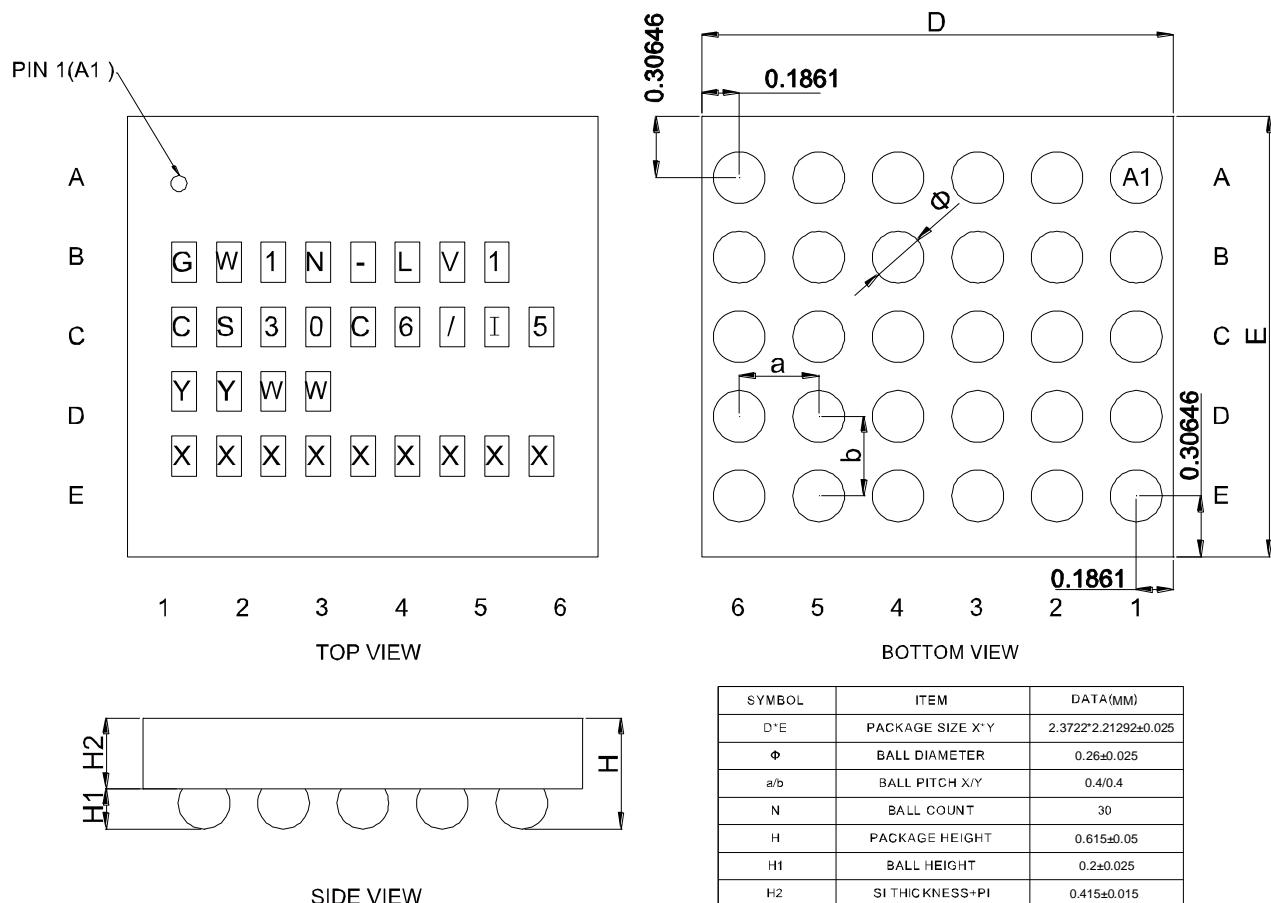
Table 3-69 Other Pins in GW1N-9 MG100T

VCC	J2,A8,A2
VCCIO0	A5
VCCIO1	E9
VCCIO2	J5
VCCIO3	E1
VCCX	J8
VSS	A1,A9,J1,J9

4 Package Diagrams

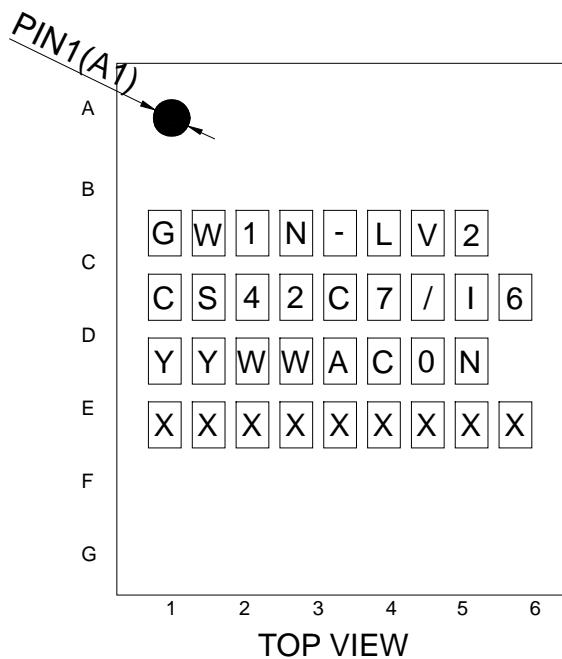
4.1 CS30 Package Outline (2.3mm x 2.4mm, GW1N-1)

Figure 4-1 Package Outline CS30 (GW1N-1)

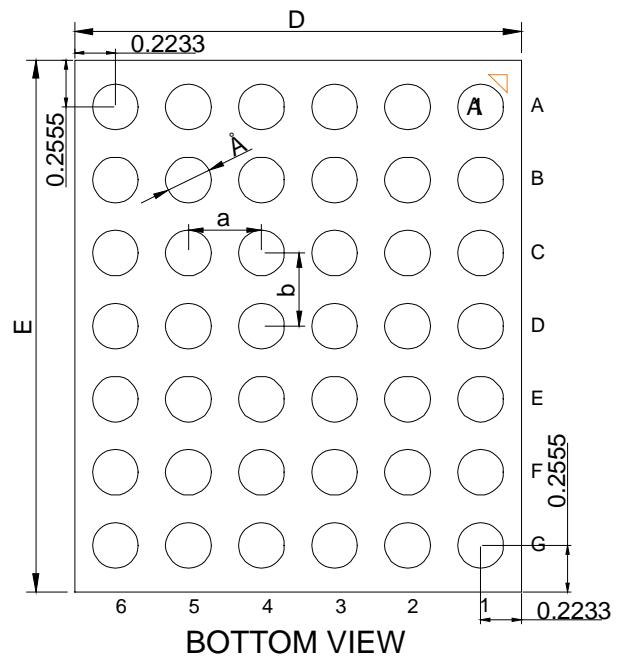


4.2 CS42 Package Outline (2.4mm x 2.9mm)

Figure 4-2 Package Outline CS42

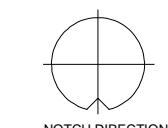
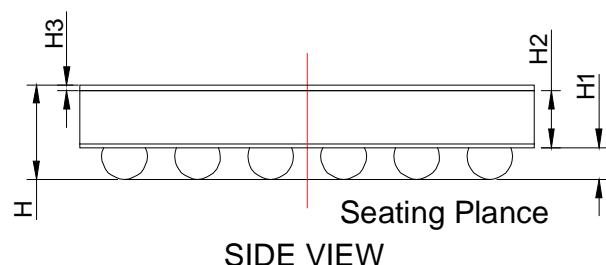


TOP VIEW



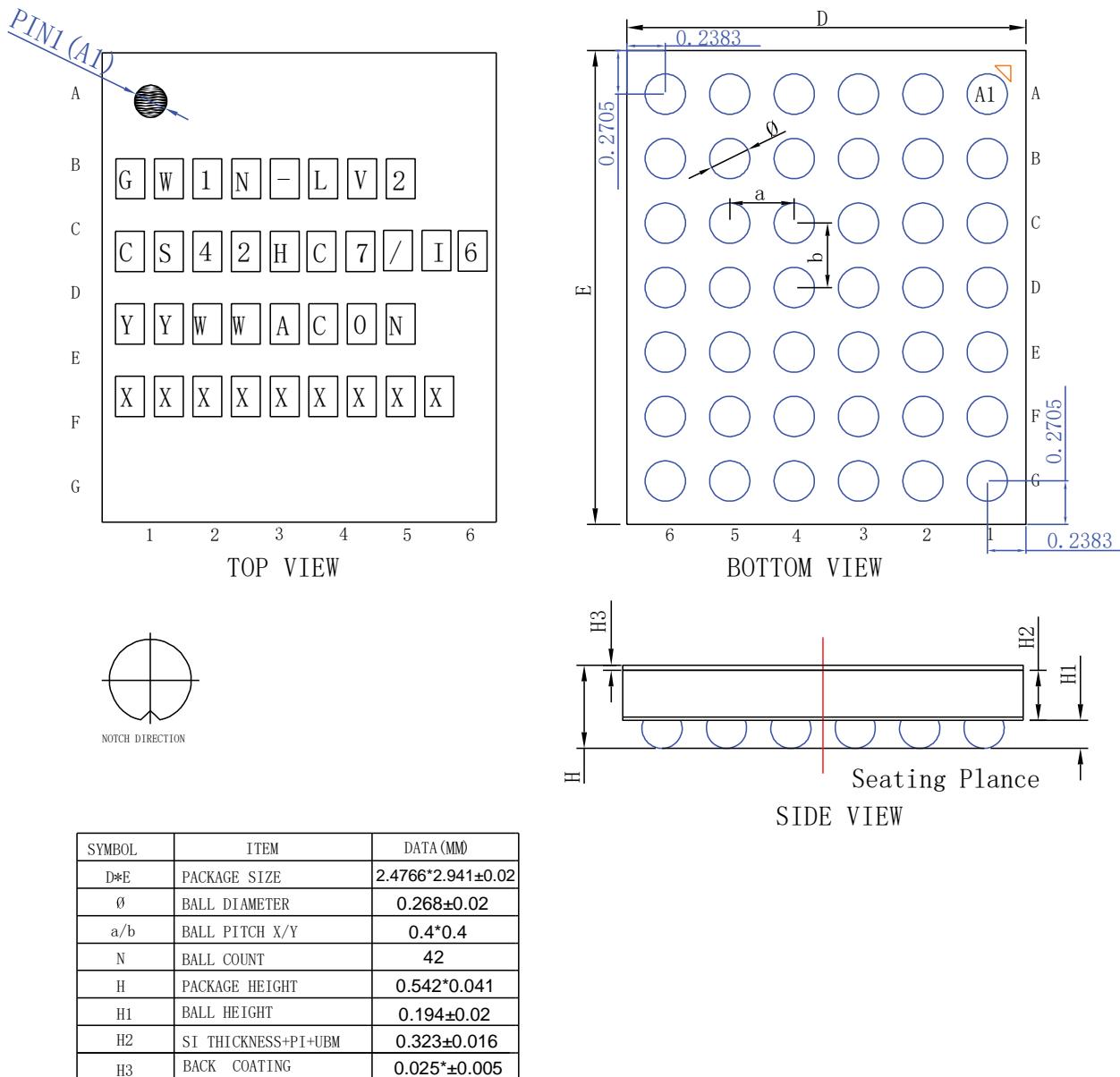
BOTTOM VIEW

SYMBOL	ITEM	DATA(MM)
<i>D*E</i>	PACKAGE SIZE	2.4466*2.9110±0.025
<i>A</i>	BALL DIAMETER	0.268±0.02
<i>a/b</i>	BALL PITCH X/Y	0.4/0.4
<i>N</i>	BALL COUNT	42
<i>H</i>	PACKAGE HEIGHT	0.542±0.041
<i>H1</i>	BALL HEIGHT	0.194±0.02
<i>H2</i>	SI THICKNESS+PI+UBM	0.323±0.016
<i>H3</i>	BACK COATING	0.025±0.005



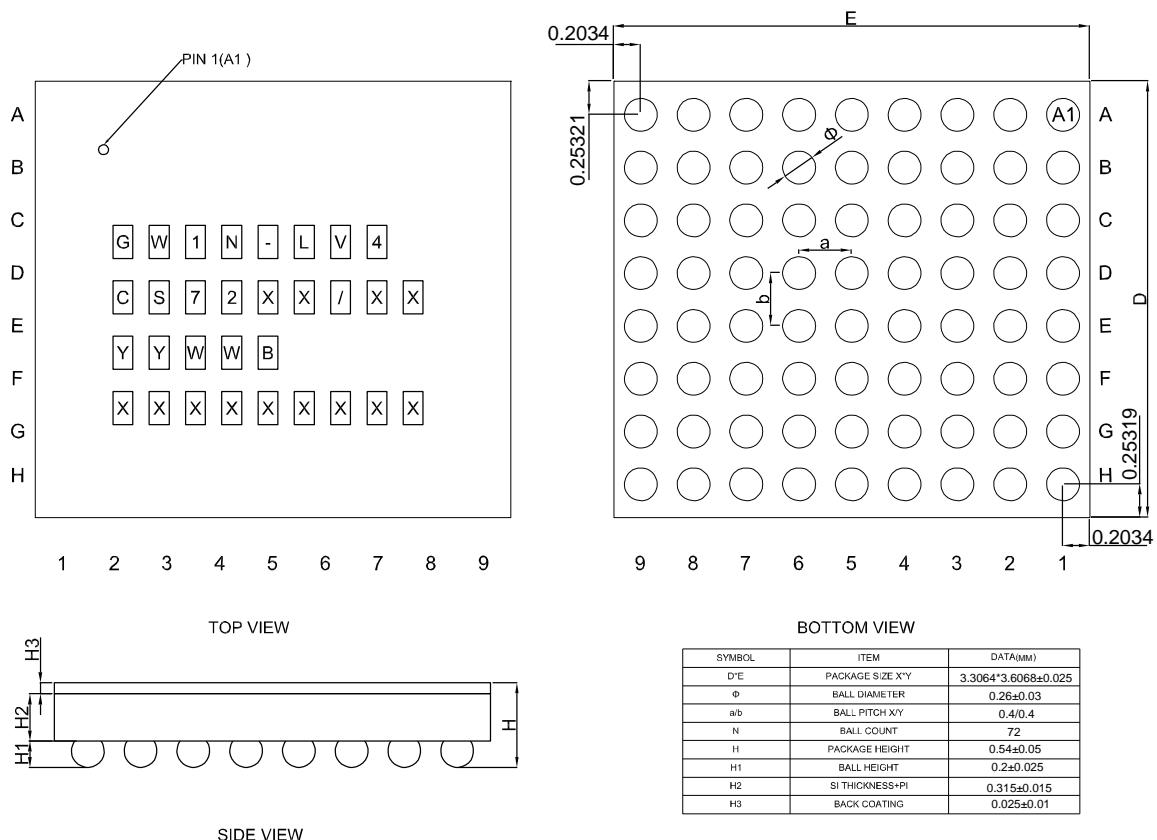
4.3 CS42H Package Outline (2.4mm x 2.9mm)

Figure 4-3 Package Outline CS42H



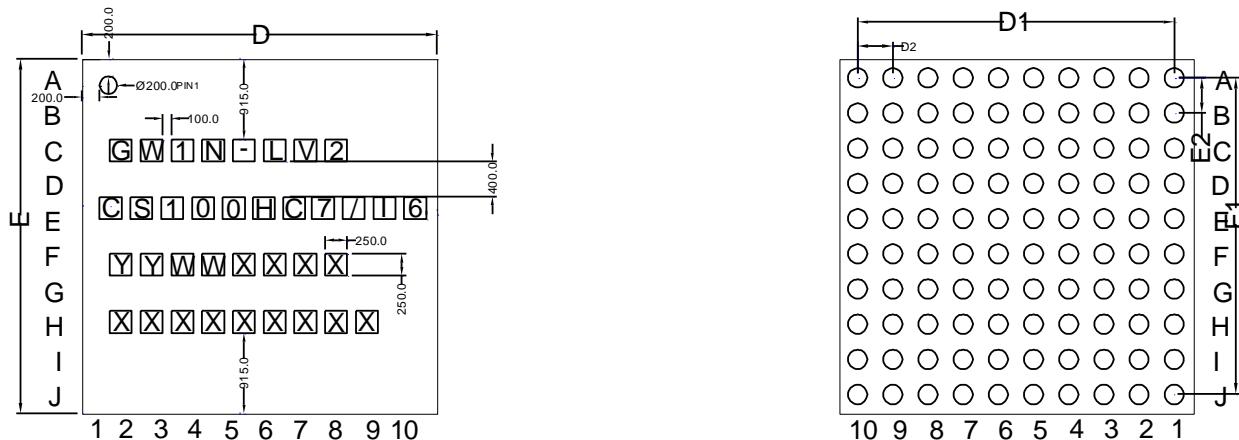
4.4 CS72 Package Outline (3.6mm x 3.3mm)

Figure 4-4 Package Outline CS72



4.5 CS100H Package Outline (4mm x 4mm)

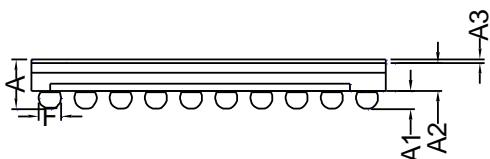
Figure 4-5 Package Outline CS100H



TOP VIEW
Ball Down

BOTTOM VIEW

Ball Up

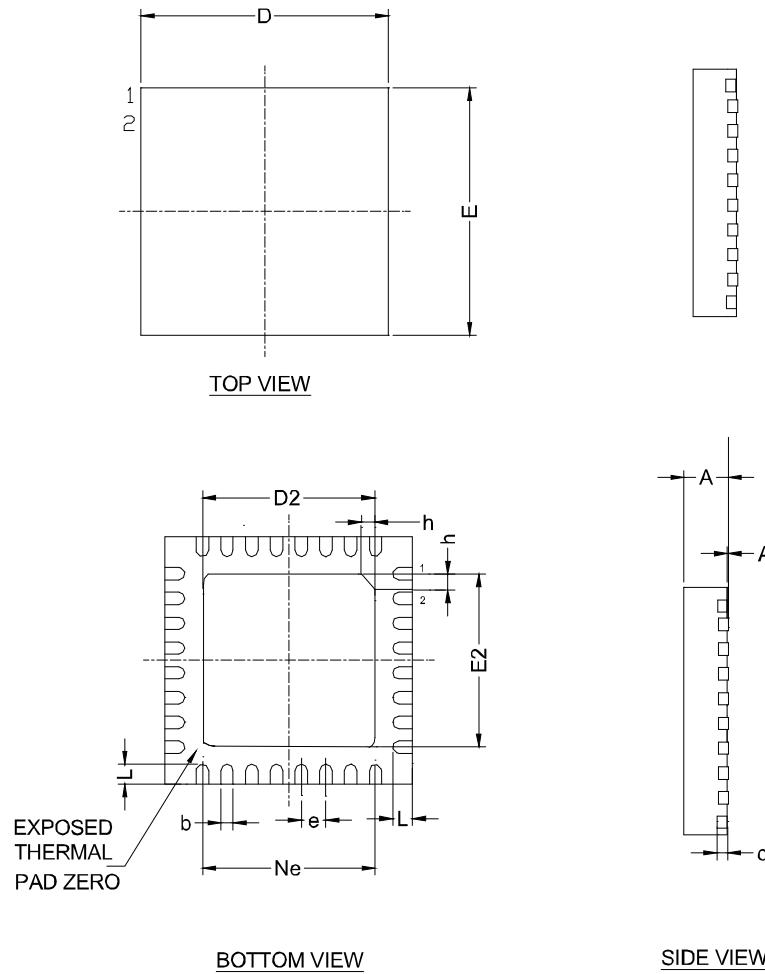


SIDE VIEW

		Unit:mm		
		NO.	Mean	Tolerance
Top Thickness	A		0.54	±0.0405
Ball Height+UEM Thickness	A1		0.2	±0.023
Wafer/Grinding Thickness	A2		0.3	±0.0125
Backside Coating Thickness	A3		0.04	±0.005
Pkg Die Size	X	D	4	±0.025
	Y	E	4	±0.025
Ball Size after reflow	F		0.262	±0.020
Ball Pitch		D1	3.6	NA
		D2	0.4	NA
		E1	3.6	NA
		E2	0.4	NA

4.6 QN32 Package Outline (5mm x 5mm, GW1N-4)

Figure 4-6 Package Outline QN32(GW1N-4)

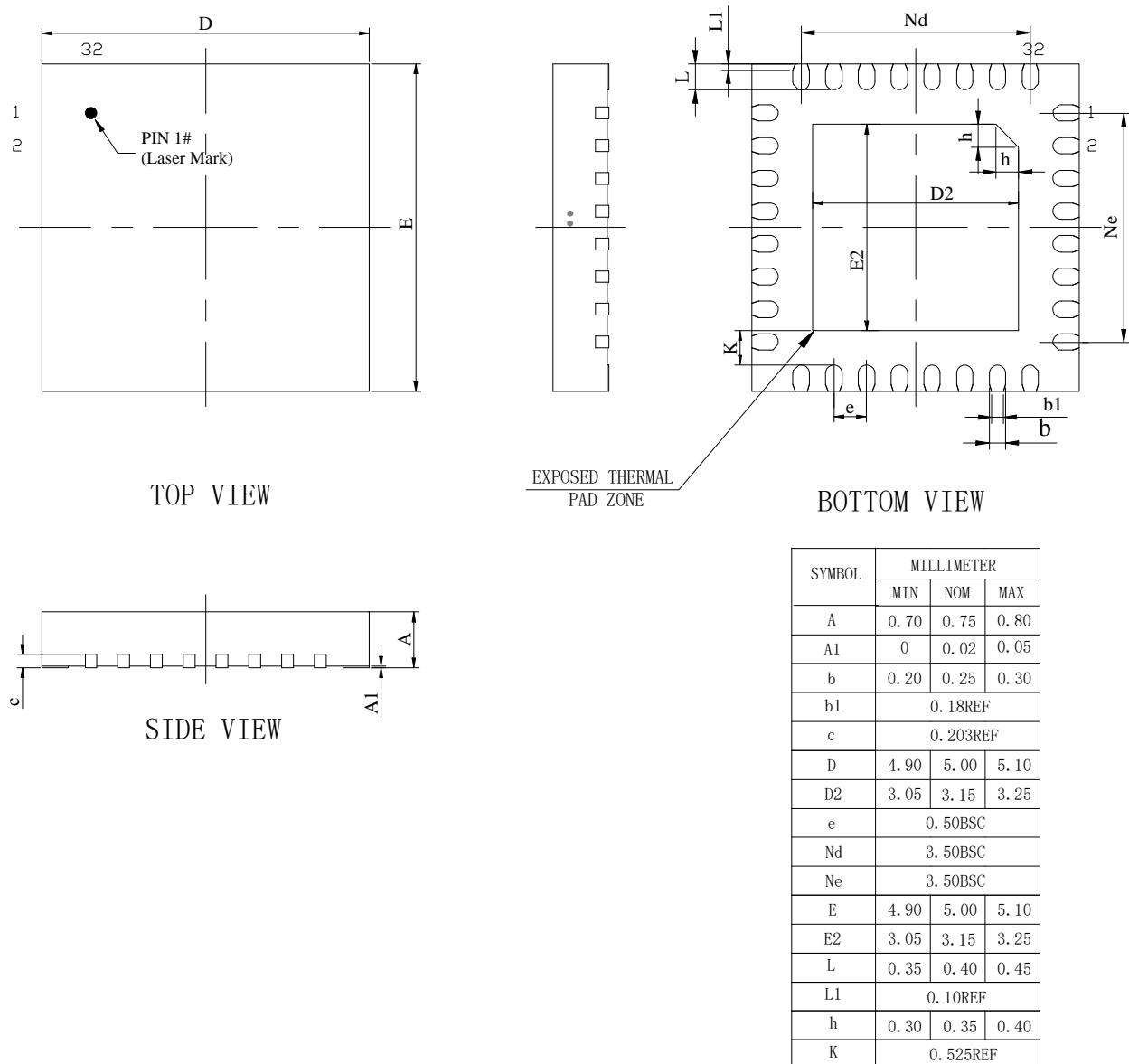


* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50 bsc		
Ne	3.50 bsc		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

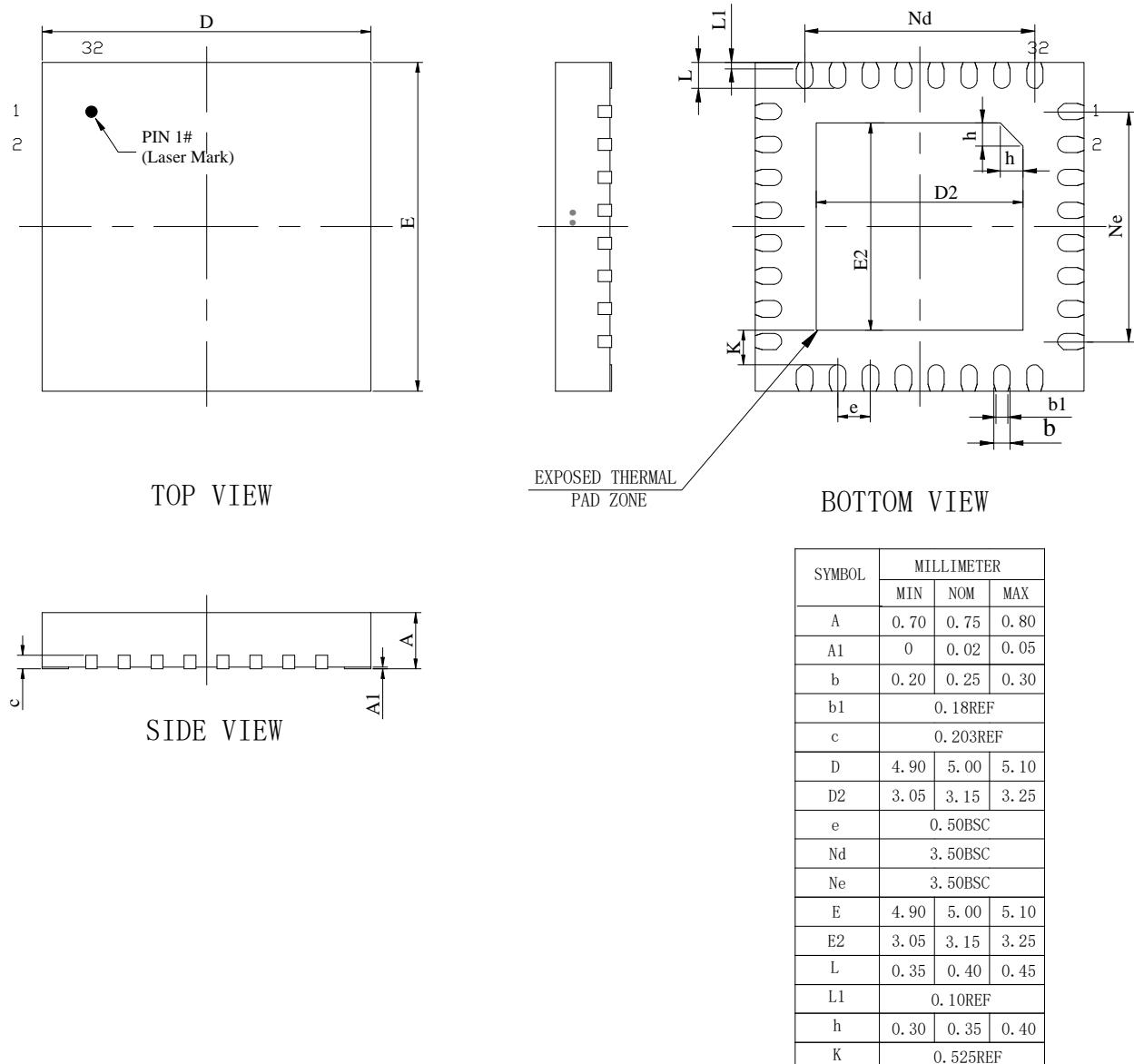
4.7 QN32 Package Outline (5mm x 5mm, GW1N-2)

Figure 4-7 Package Outline QN32(GW1N-2)



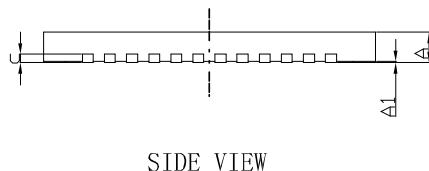
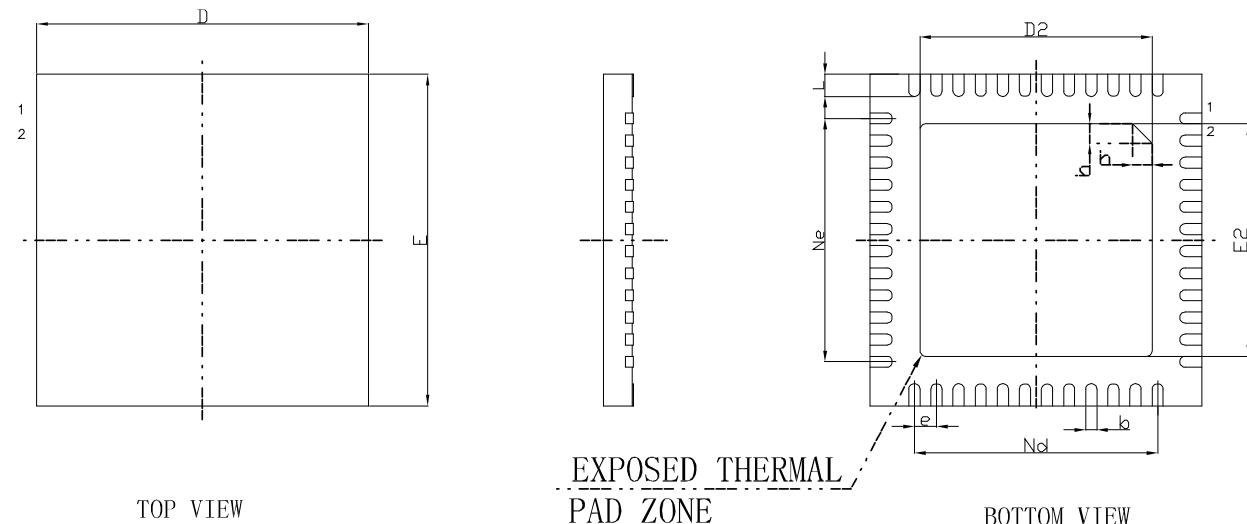
4.8 QN32X Package Outline (5mm x 5mm)

Figure 4-8 Package Outline QN32X



4.9 QN48/QN48H Package Outline (6mm x 6mm, GW1N-2/4)

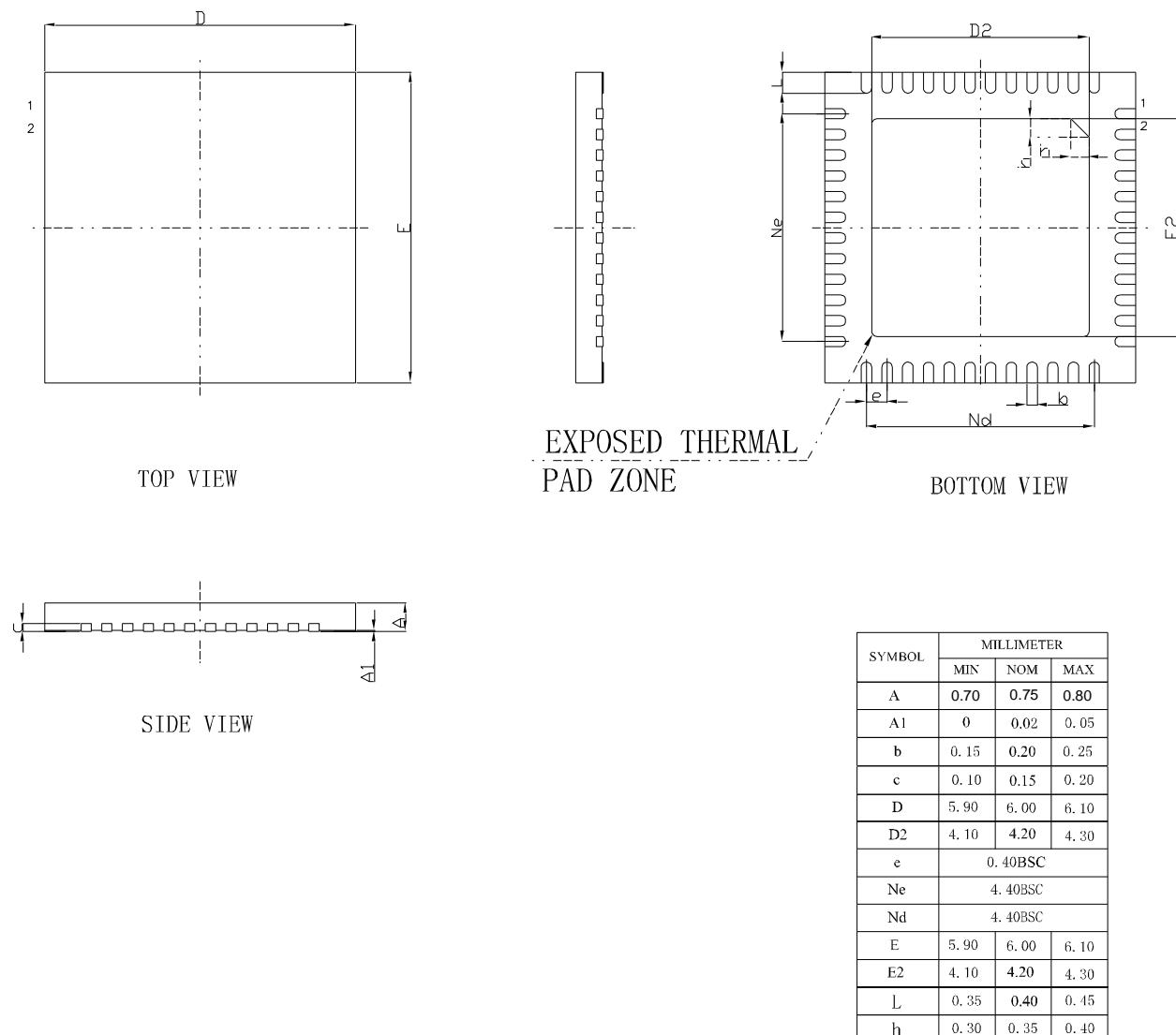
Figure 4-9 Package Outline QN48/QN48H(GW1N-2/4)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

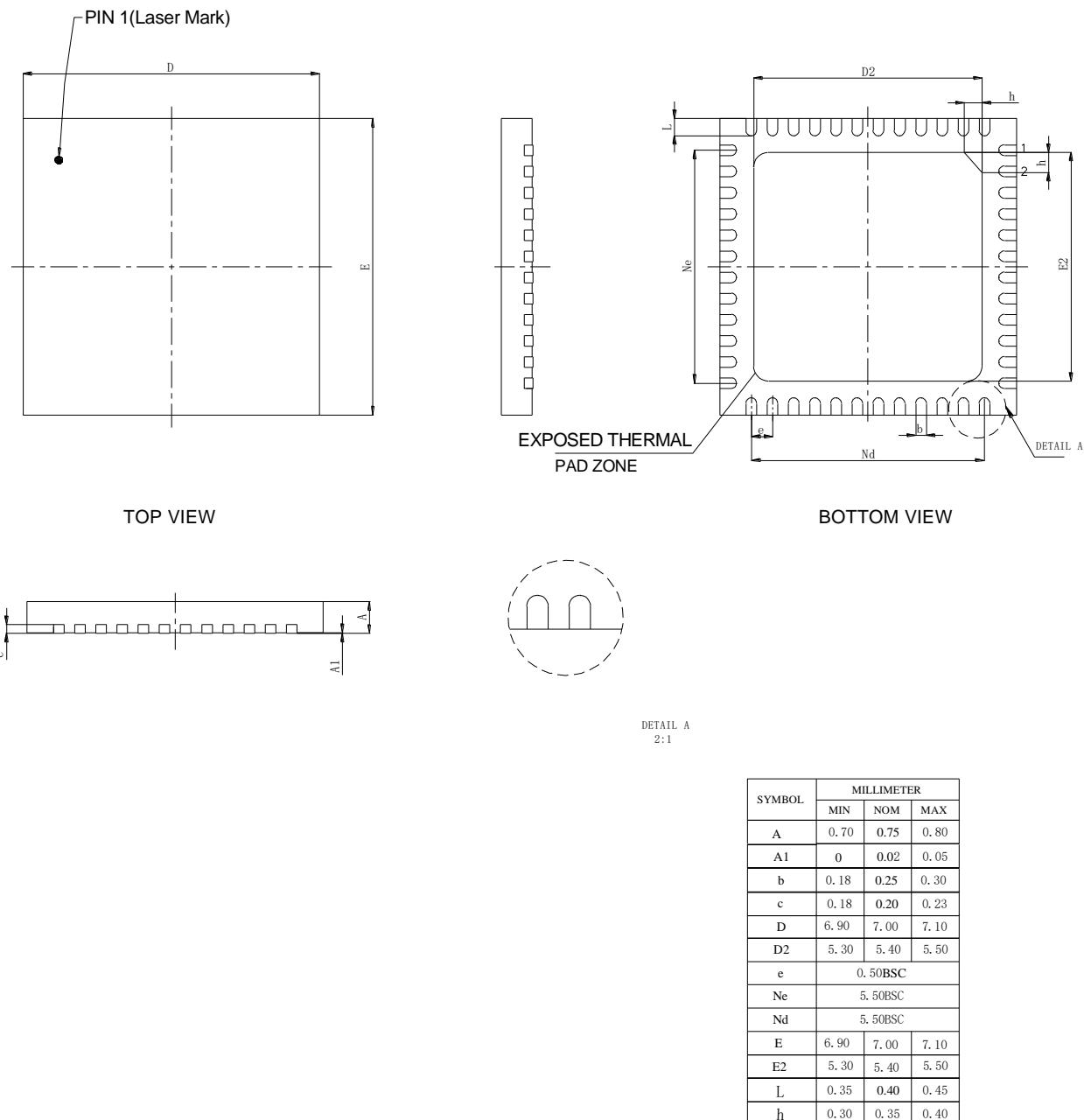
4.10 QN48/QN48F Package Outline (6mm x 6mm, GW1N-9)

Figure 4-10 Package Outline QN48/QN48F(GW1N-9)



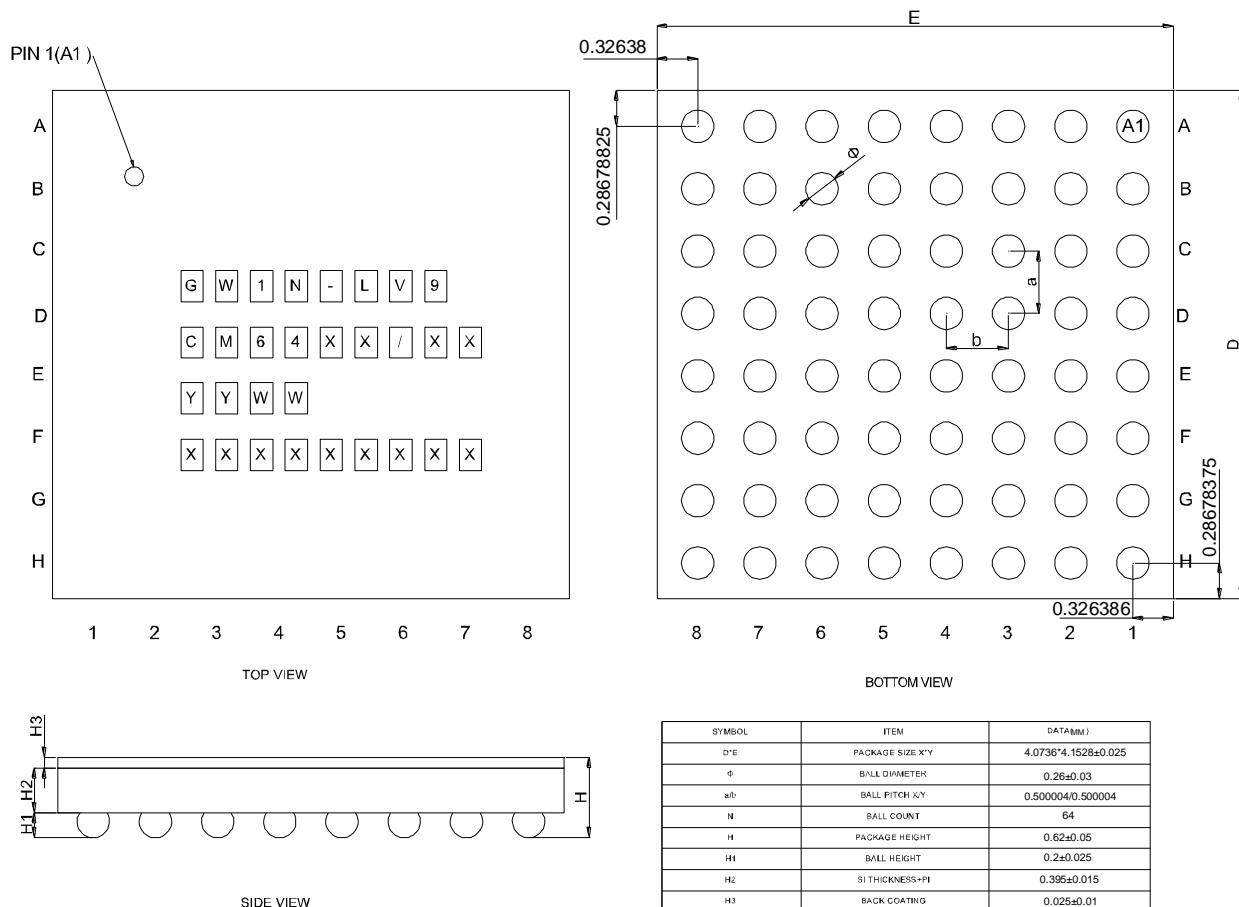
4.11 QN48X/QN48XF Package Outline (7mm x 7mm)

Figure 4-11 Package Outline QN48X/QN48XF



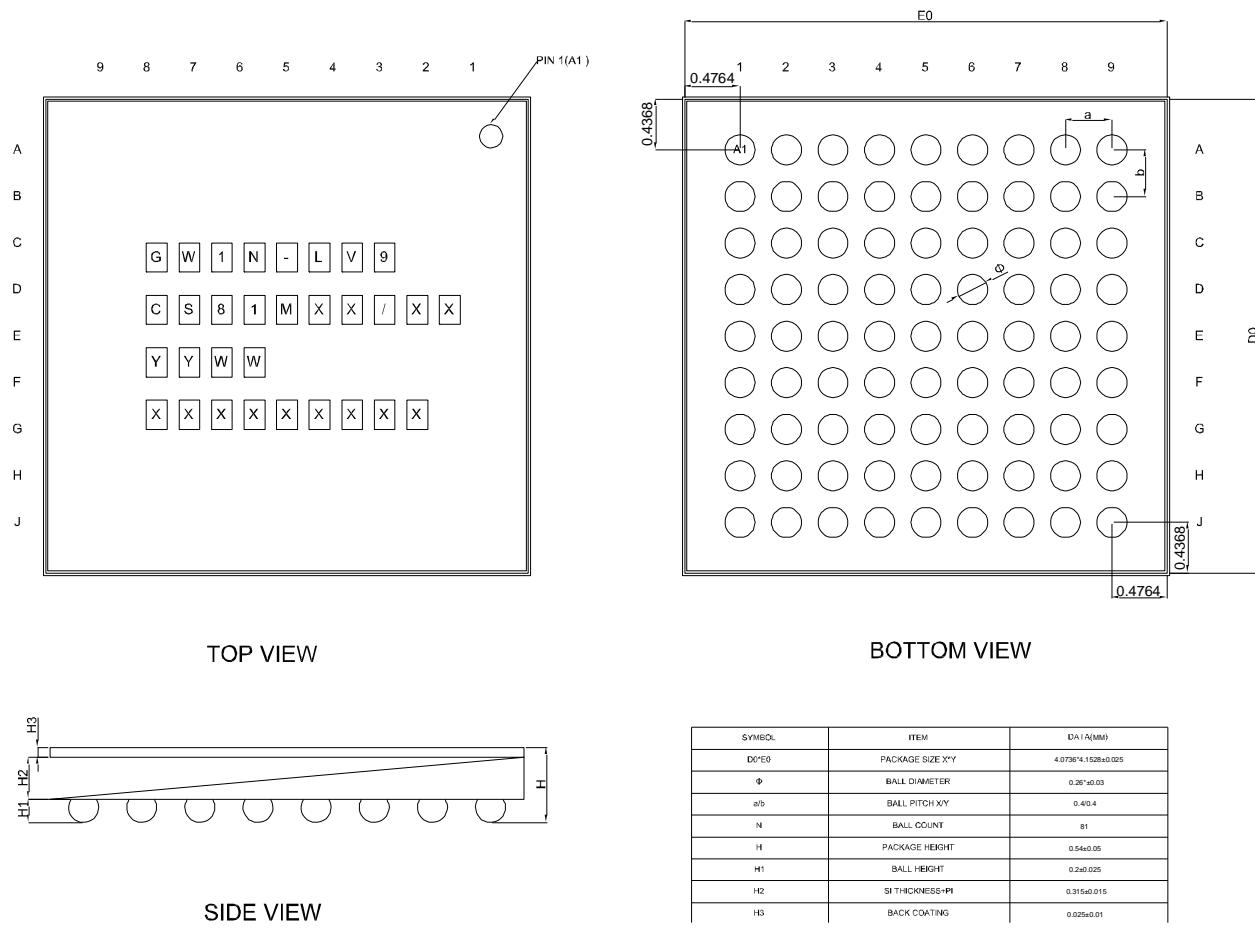
4.12 CM64 Package Outline (4.1mm x 4.1mm)

Figure 4-12 Package Outline CM64



4.13 CS81M Package Outline (4.1mm x 4.1mm)

Figure 4-13 Package Outline CS81M

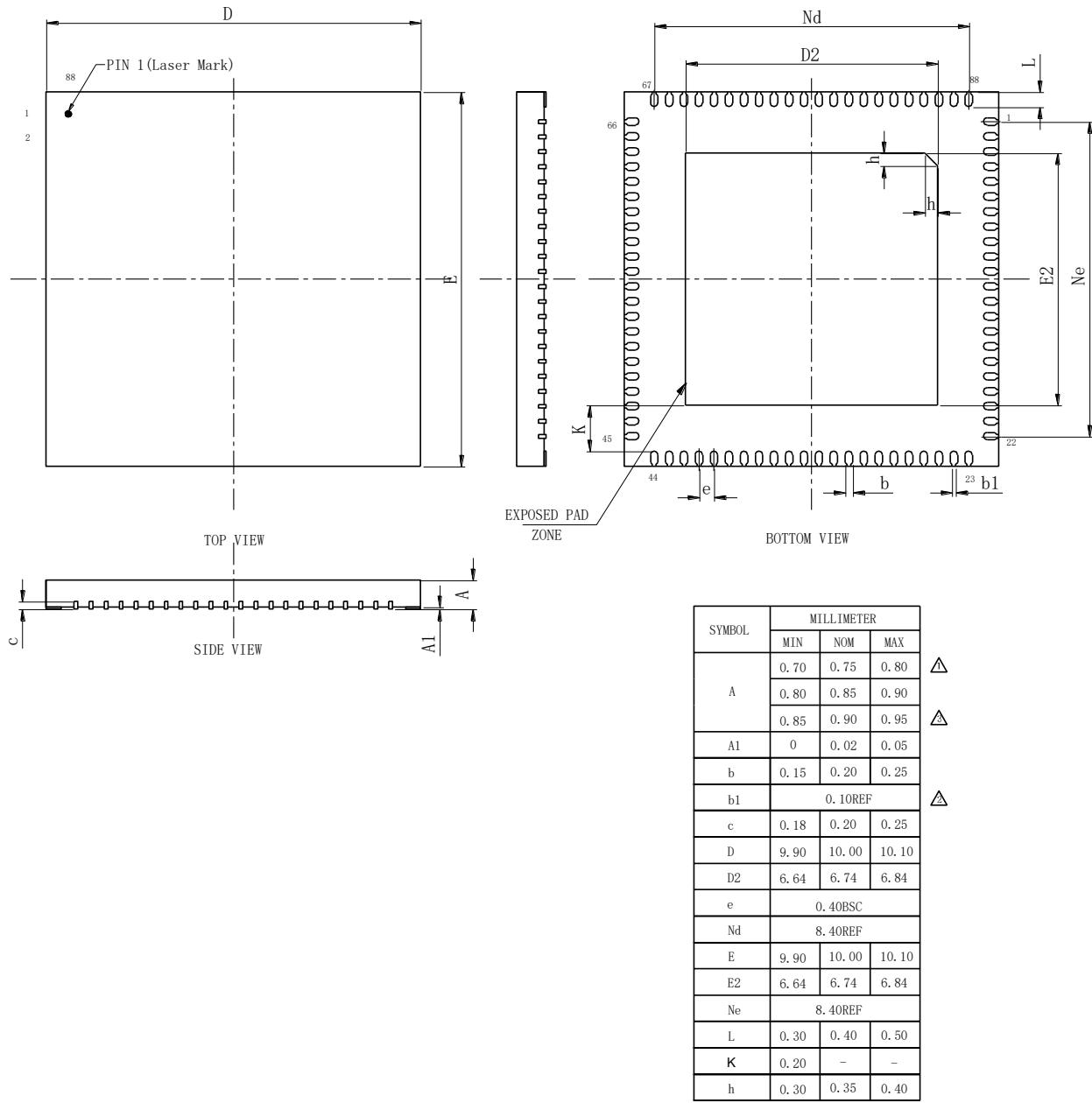


Note!

The sequence of pins 1-9 in the CS81M package outline is opposite to other WLCSP packages.

4.14 QN88 Package Outline (10mm x 10mm)

Figure 4-14 Package Outline QN88

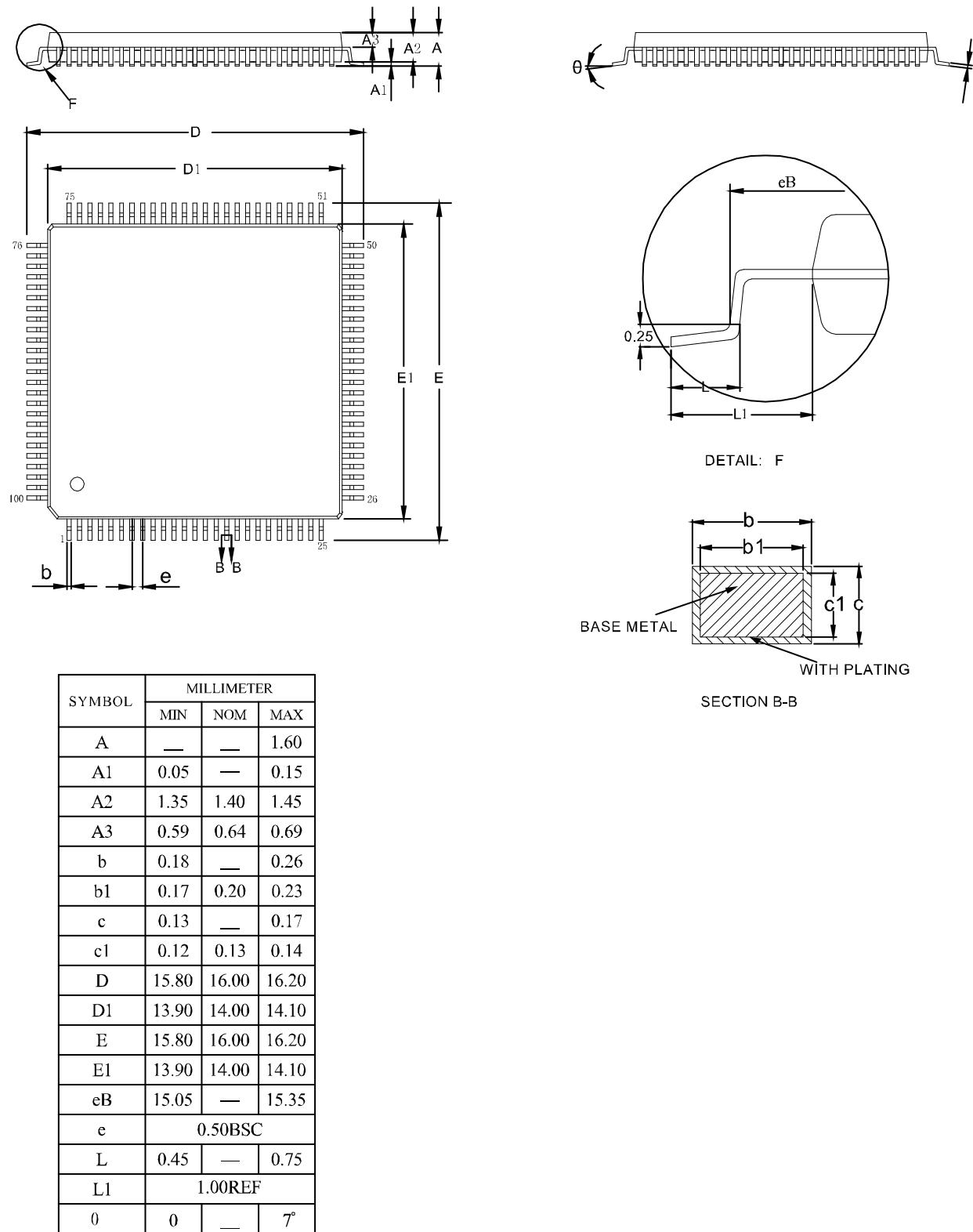


Note!

For GW1N-LV9QN88, GW1N-UV9QN88, GW1N-LV4QN88, GW1N-UV4QN88, GW1N-LV2QN88, and GW1N-UV2QN88, the value of A(NOM) is 0.85mm.

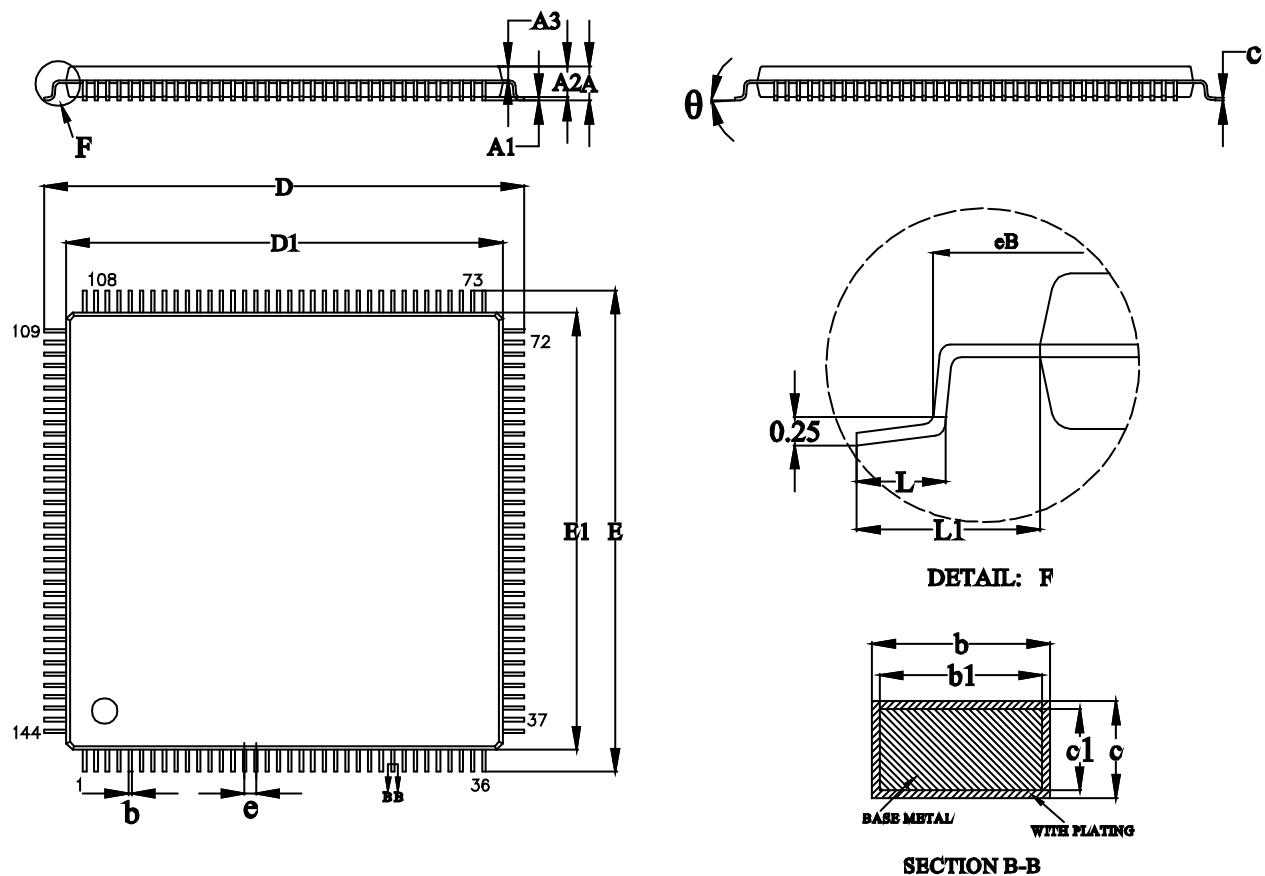
4.15 LQ100/LQ100X Package Outline (14mm x 14mm)

Figure 4-15 Package Outline LQ100/LQ100X



4.16 LQ144/LQ144X/LQ144F Package Outline (20mm x 20mm)

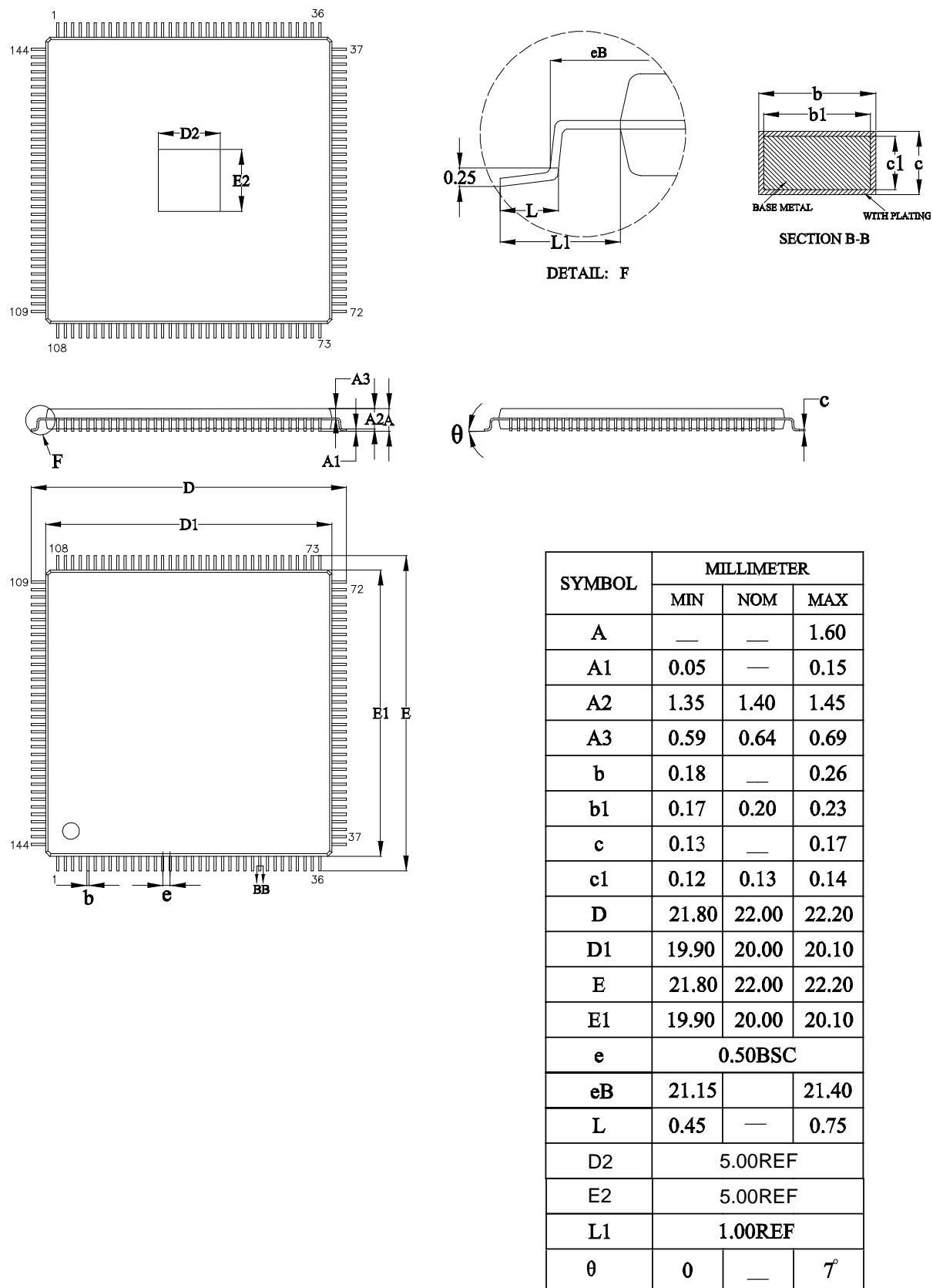
Figure 4-16 Package Outline LQ144 / LQ144X/LQ144F



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

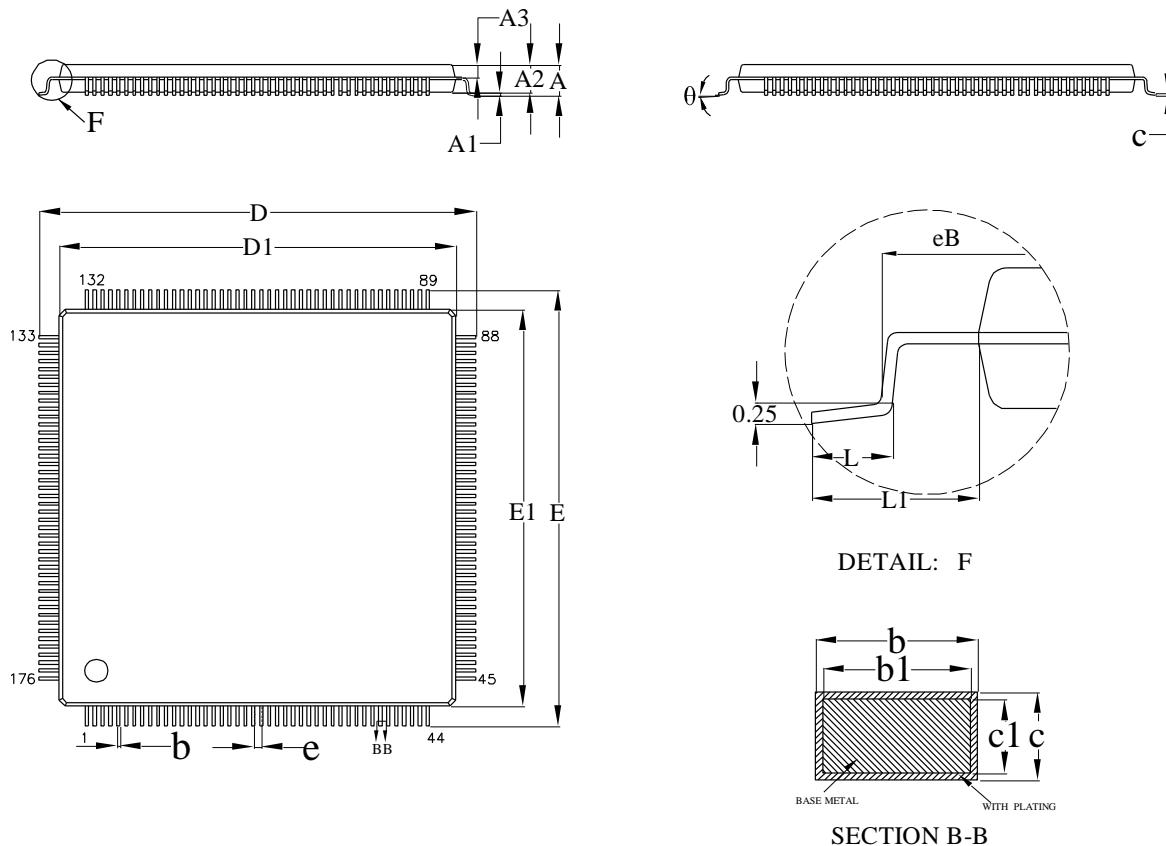
4.17 EQ144 Package Outline (20mm x 20mm)

Figure 4-17 Package Outline EQ144



4.18 LQ176 Package Outline (20mm x 20mm)

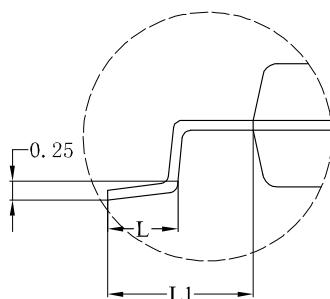
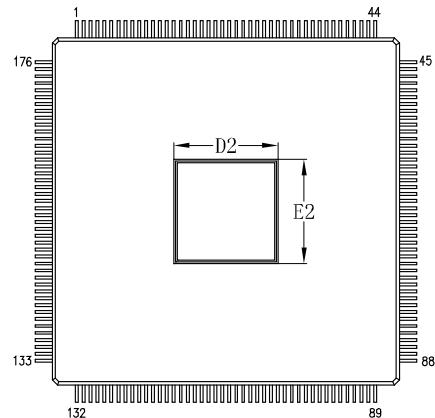
Figure 4-18 Package Outline LQ176



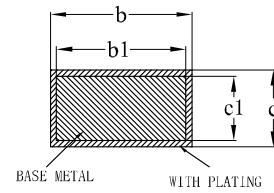
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
eB	21.15	—	21.40
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

4.19 EQ176 Package Outline (20mm x 20mm)

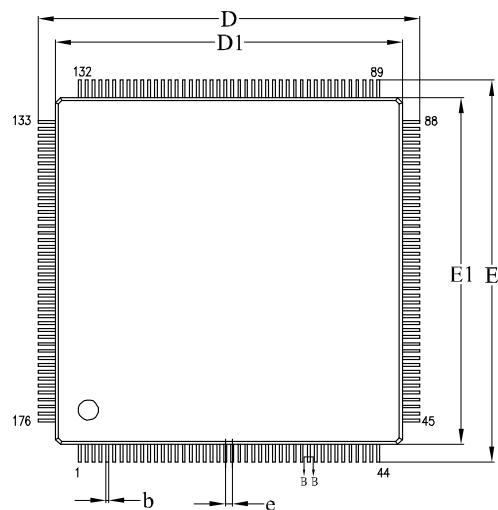
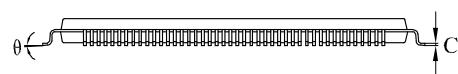
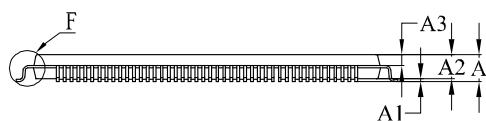
Figure 4-19 Package Outline EQ176



DETAIL: F



SECTION B-B

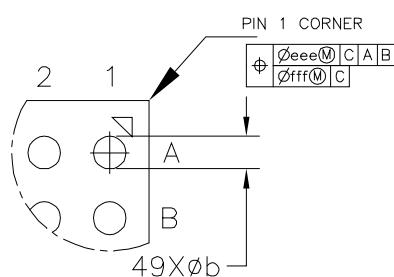
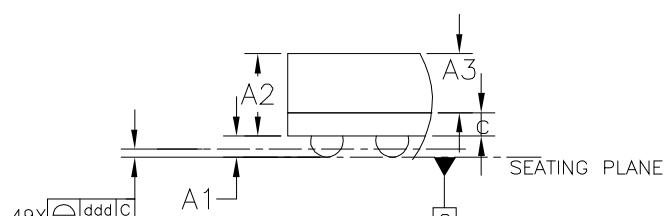
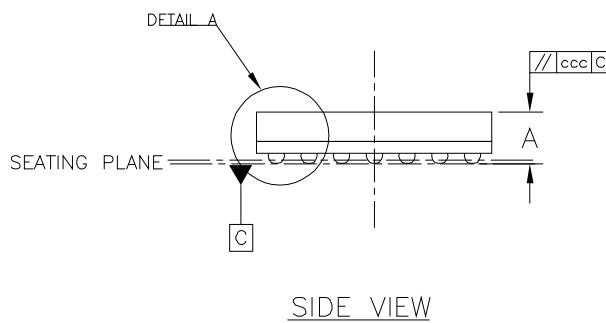
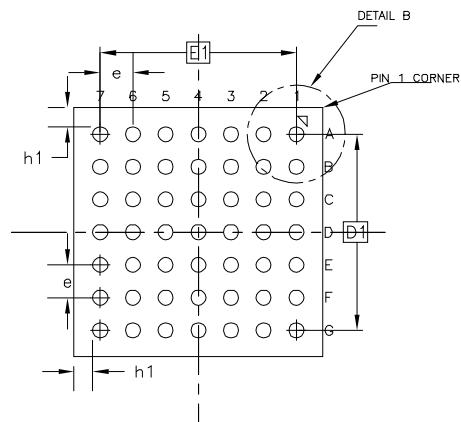
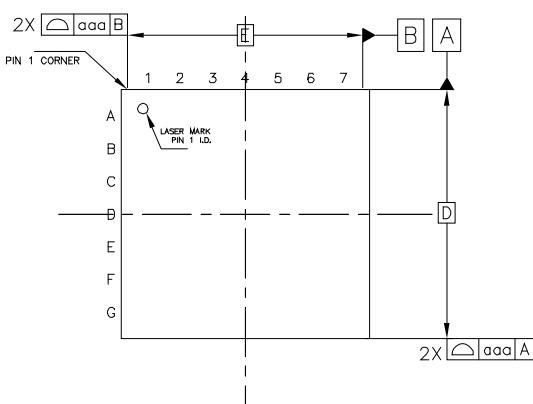


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.10	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.40BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	7°

D2	E2
6.00REF	6.00REF

4.20 MG49 Package Outline (3.8mm x 3.8mm)

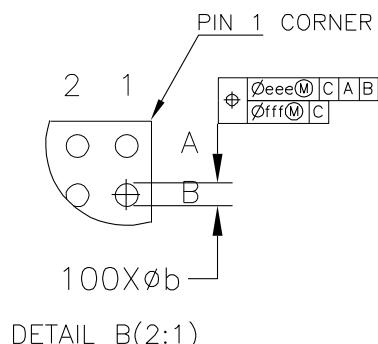
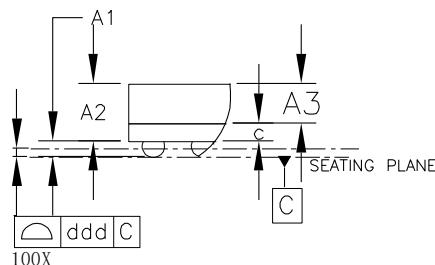
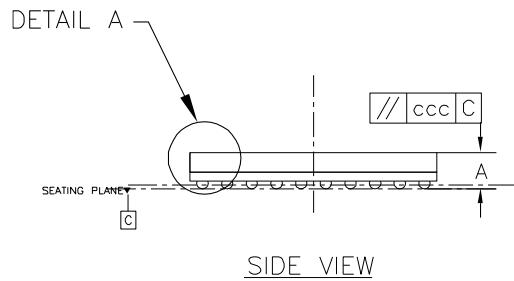
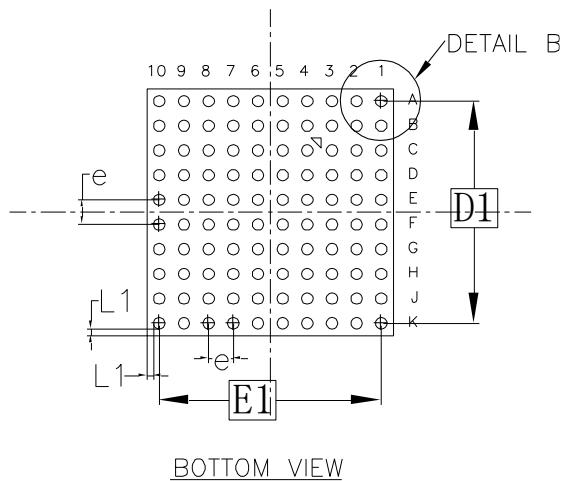
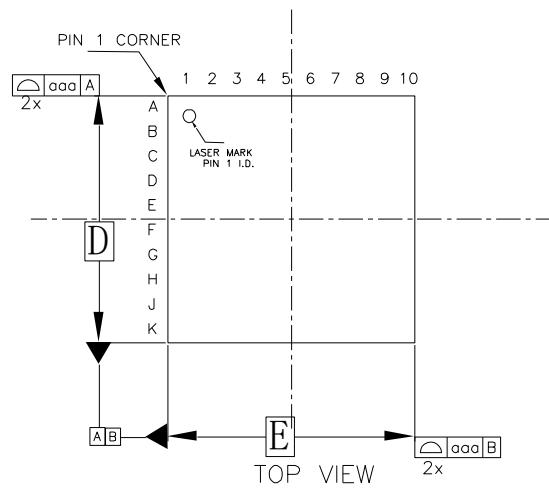
Figure 4-20 Package Outline MG49



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.71	0.79	0.87
A1	0.11	0.16	0.21
A2	0.58	0.63	0.68
A3	0.45 BASIC		
c	0.15	0.18	0.21
D	3.70	3.80	3.90
D1	3.00 BASIC		
E	3.70	3.80	3.90
E1	3.00 BASIC		
e	0.50 BASIC		
b	0.18	0.23	0.28
h1	0.285 REF		
aaa	0.10		
ccc	0.08		
ddd	0.08		
eee	0.15		
fff	0.05		

4.21 MG100/MG100T Package Outline (5mm x 5mm)

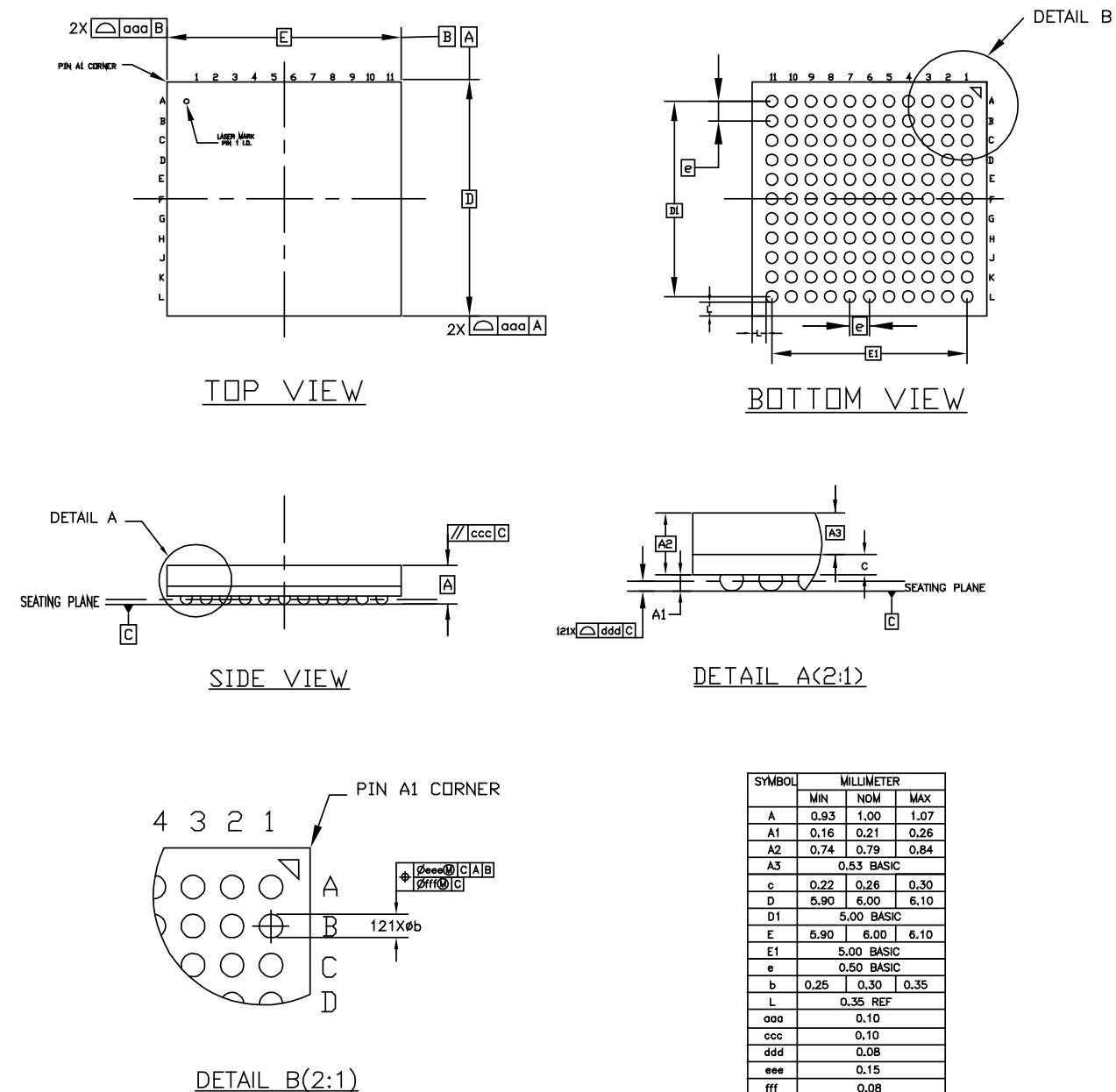
Figure 4-21 Package Outline MG100/MG100T



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.68	0.74	0.80
A1	0.11	0.16	0.21
A2	0.53	0.58	0.63
A3	0.40	BASIC	
c	0.15	0.18	0.21
D	4.90	5.00	5.10
D1	4.50	BASIC	
E	4.90	5.00	5.10
E1	4.50	BASIC	
e	0.50	BASIC	
b	0.18	0.23	0.28
L1	0.135	REF	
aaa	0.15		
ccc	0.08		
ddd	0.10		
eee	0.15		
fff	0.05		

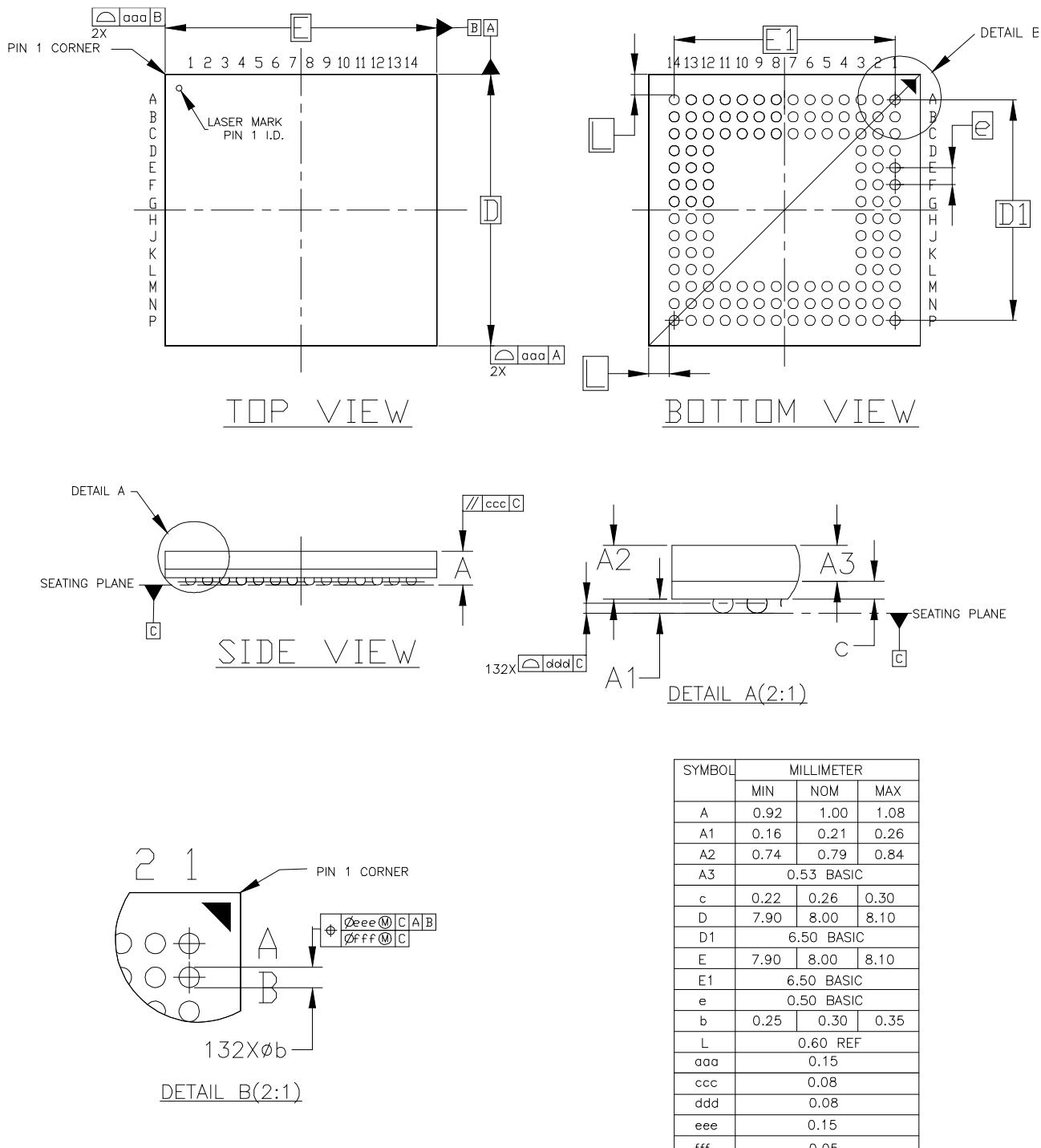
4.22 MG121/MG121X Package Outline (6mm x 6mm)

Figure 4-22 Package Outline MG121/MG121X



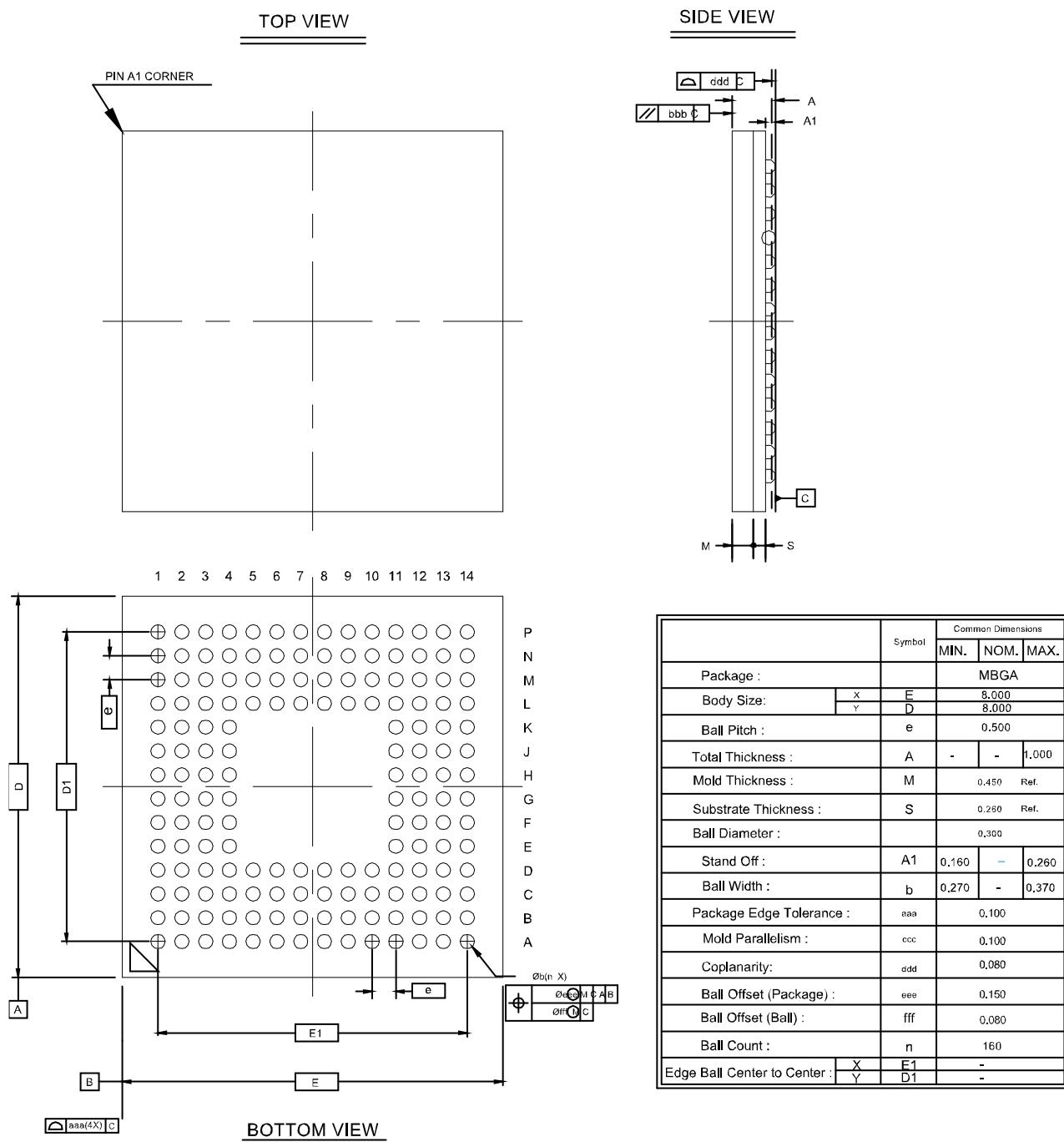
4.23 MG132/MG132X/MG132H Package Outline (8mm x 8mm)

Figure 4-23 Package Outline MG132/MG132X/MG132H



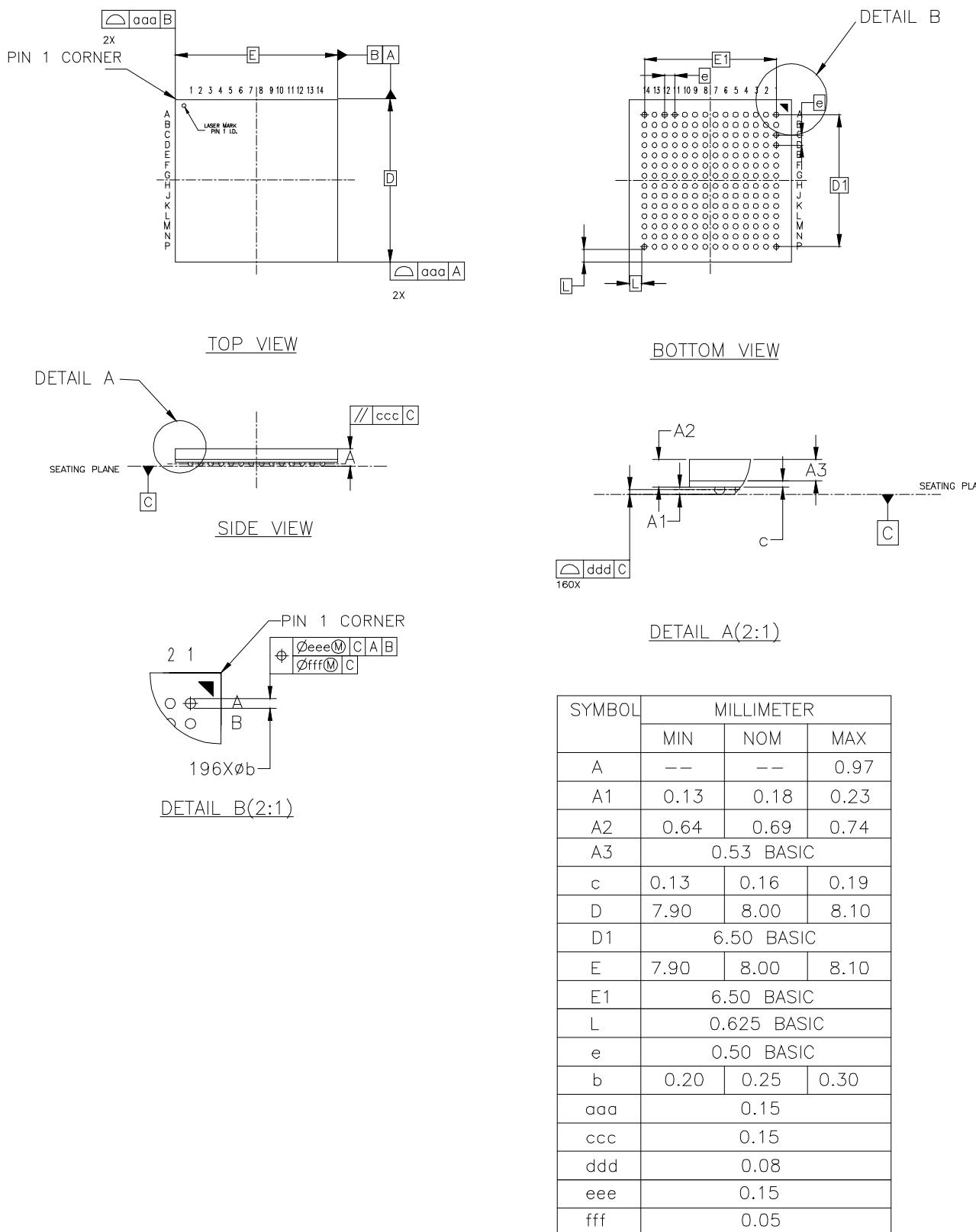
4.24 MG160 Package Outline (8mm x 8mm)

Figure 4-24 Package Outline MG160



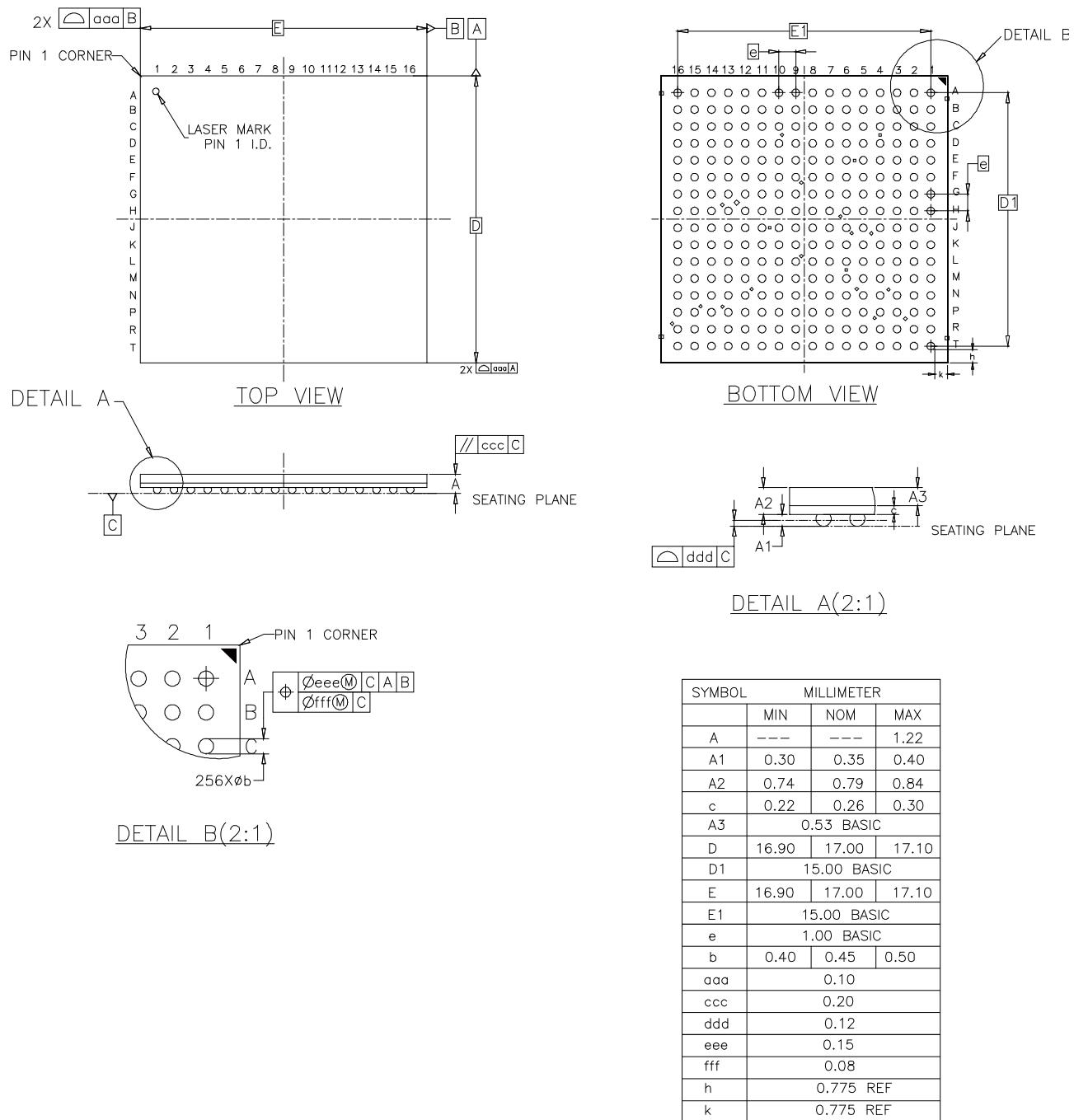
4.25 MG196 Package Outline (8mm x 8mm)

Figure 4-25 Package Outline MG196



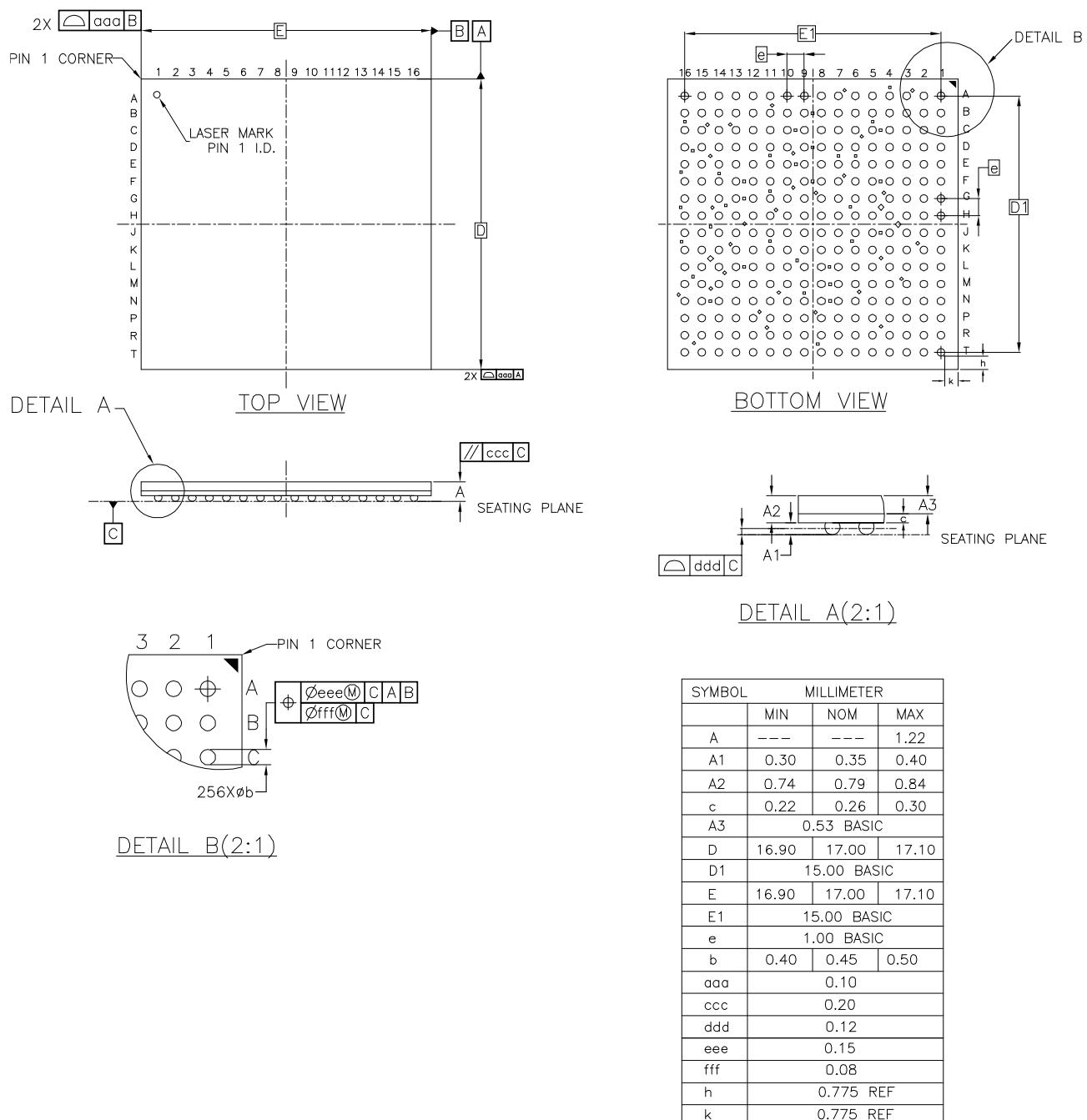
4.26 PG256M Package Outline (17mm x 17mm)

Figure 4-26 Package Outline PG256M



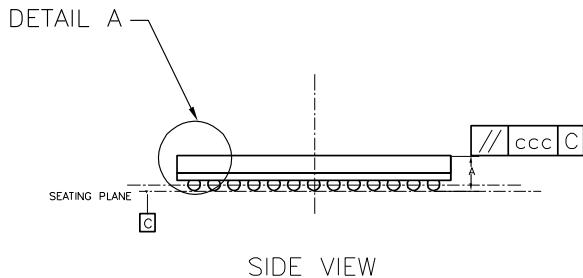
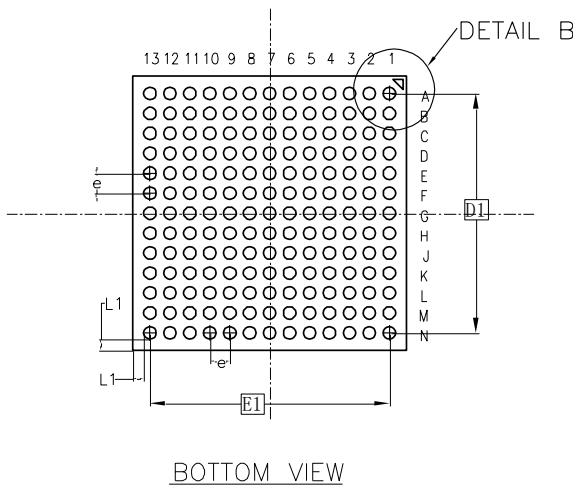
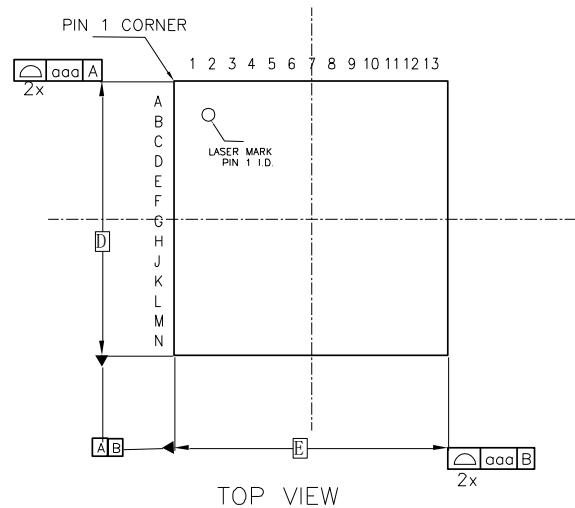
4.27 PG256 Package Outline (17mm x 17mm)

Figure 4-27 Package Outline PG256

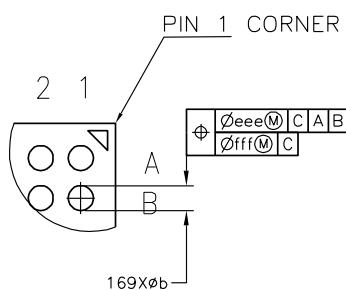
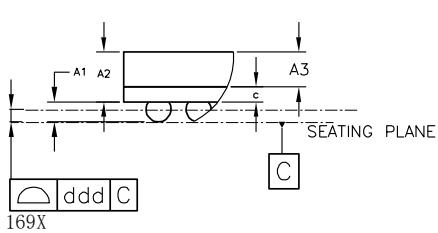


4.28 UG169 Package Outline (11mm x 11mm)

Figure 4-28 Package Outline UG169

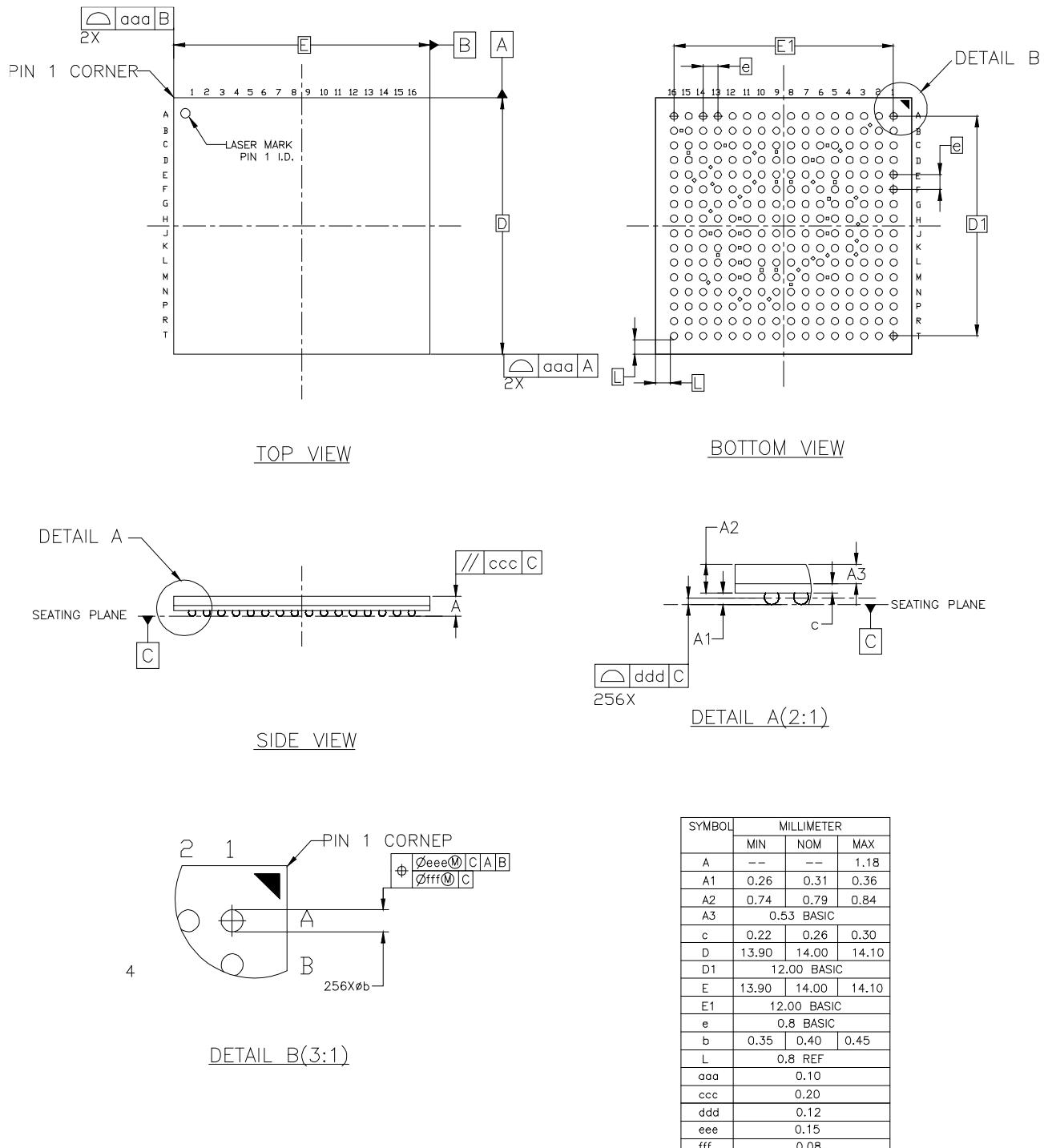


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.30	1.40	1.50
A1	0.35	0.40	0.45
A2	0.95	1.00	1.05
A3	0.70	BASIC	
c	0.26	0.30	0.34
D	10.90	11.00	11.10
D1	9.60	BASIC	
E	10.90	11.00	11.10
E1	9.60	BASIC	
e	0.80	BASIC	
b	0.45	0.50	0.55
L1	0.45	REF	
ooo	0.15		
ccc	0.15		
ddd	0.15		
eee	0.15		
fff	0.08		



4.29 UG256 Package Outline (14mm x 14mm)

Figure 4-29 Package Outline UG256



4.30 UG332 Package Outline (17mm x 17mm)

Figure 4-30 Package Outline UG332

