

pdp1

digital

*Walter Riva*

**MF11-U/UP  
memory system  
engineering  
drawings**

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# **DRAWING DIRECTORY**

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## **CUSTOMER PRINT SET INDEX**

## SEQUENCE

DRAWING DIRECTORY  
MODULE UTILIZATION  
TIMING DIAGRAM  
16K UNIBUS TIMING  
16K X-Y DRIVE  
16K SENSE MEMORY  
MEMORY STACK (16K X 16)  
PARITY CONTROL  
BACK PLANE  
OPTION HARNESS  
PARTS LIST  
CUSTOMER ACCEPTANCE PROC.  
UNIT ASSEMBLY  
AUTO. WIRE TEST REV. STAT.  
AUTO. WIRE TEST REV. STAT.

B-DD-MF11-U  
D-MU-MF11-U-MU  
D-TD-MF11-U-1  
D-CS-M8293-0-1  
D-CS-G235-0-1  
D-CS-G114-0-1  
D-CS-H217-0-1  
D-CS-M7259-0-1  
D-CS-5410345-0-1  
E-IA-7009535-0-0  
A-PL-MF11-U-0  
A-SP-MF11-U-3  
D-UA-MF11-U-0  
A-WT-7009295-3  
A-WT-7009295-4

ON-LINE TEST PROCEDURE A-SP-MF11-U-2  
MF11-U ENGINEERING SPECIFICATION A-SP-MF11-U-4

SEQUENCE

1

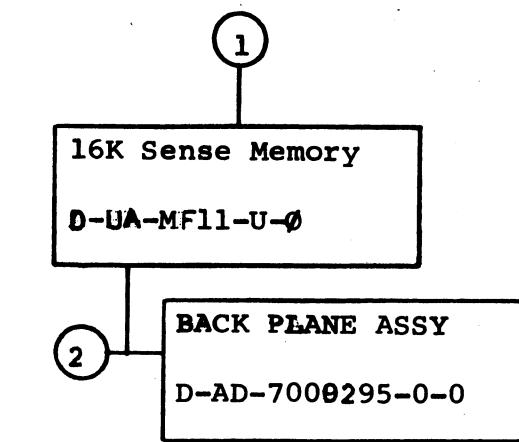
MFG. PRINT SET

# THIS IS PRINT SET

1

**NOTE:** TO INSTALL MF11-U OR MF11-UP IN 11/40 CPU WITH SERIAL NUMBER LESS THAN 6000 OR H960-D (OR-E) WITH SERIAL LESS THAN 7000 A FIELD MODIFICATION KIT (FM11-UA, -UB, OR -UC) IS REQUIRED.

REVISIONS	USED ON OPTION/MODEL	DRN. J. FLEMING	DATE 5/1/73	TITLE 16K SENSE MEMORY		
	CHK'D. W. MAJOR	DATE 5/11/73				
	PROJ ENG. D. SMELSER	DATE 5/15/73				
	PROD. R. SHOOP	DATE 6/13/73	SIZE B	CODE DD	NUMBER MF11-U	REV F
	FIELD SERV. WP RUBEE	DATE 1/8/74	DIST			
SHEET 1 OF 3						



TITLE

16K SENSE MEMORY

SHEET 2 OF 3



CUSTOMER PRINT SET		ELECTRICAL								CUSTOMER PRINT SET		MECHANICAL							
		SET	MFG.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE	SET	MFG.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE				
X	MF11-U	1	A-PL-MF11-U-0	D	1	16K SENSE MEMORY			X		1	A-PL-MF11-U-0	B	1	16K SENSE MEMORY				
X			D-CS-G114-0-1	#	9	16K SENSE INHIBIT						E-TA-7009535-0-0	#	1	OPTION HARNESS				
X			D-CS-G235-0-1	#	9	16K X-Y DRIVE						D-UA-MF11-U-0	D	1	MF11-U MEMORY				
X			D-CS-M8293-0-1	#	10	16K UNIBUS TIMING													
X			D-CS-H217-0-1	#	3	MEMORY STACK													
X			D-MU-MF11-U-MU	R	1	MODULE UTILIZATION													
X			D-TD-MF11-U-1	A	1	TIMING DIAGRAM													
X			D-CS-M7259-0-1	#	3	PARITY CONTROL													
X			A-SP-MF11-U-3	*	2	CUSTOMER ACCEPTANCE PROCEDURE													
X			A-SP-MF11-U-2	*	6	ONLINE TEST PROCEDURE													
X			A-SP-MF11-U-4	*	3	MF11-U ENG. SPEC.													
X			D-UA-MF11-U-0	D	1	MF11-U MEMORY													
X		2	D-AD-7009295-0-0	#	1	BACK PLANE ASSY													
X			D-CS-5410345-0-1	#	1	32K X 16,18 MEMORY BACKPLANE													
X		X	A-WT-7009295-3	#		AUTO WIRE TEST REV STAT													
X		X	A-WT-7009295-4	#		AUTO WIRE TEST REV STAT													
CUSTOMER PRINT SET CODES	X = PRINT OF DOCUMENT INCLUDED IN PRINT SET C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED								TITLE	16K SENSE MEMORY				SHEET 3 OF 3	SIZE DD	CODE MF11-U	NUMBER	REV	

8

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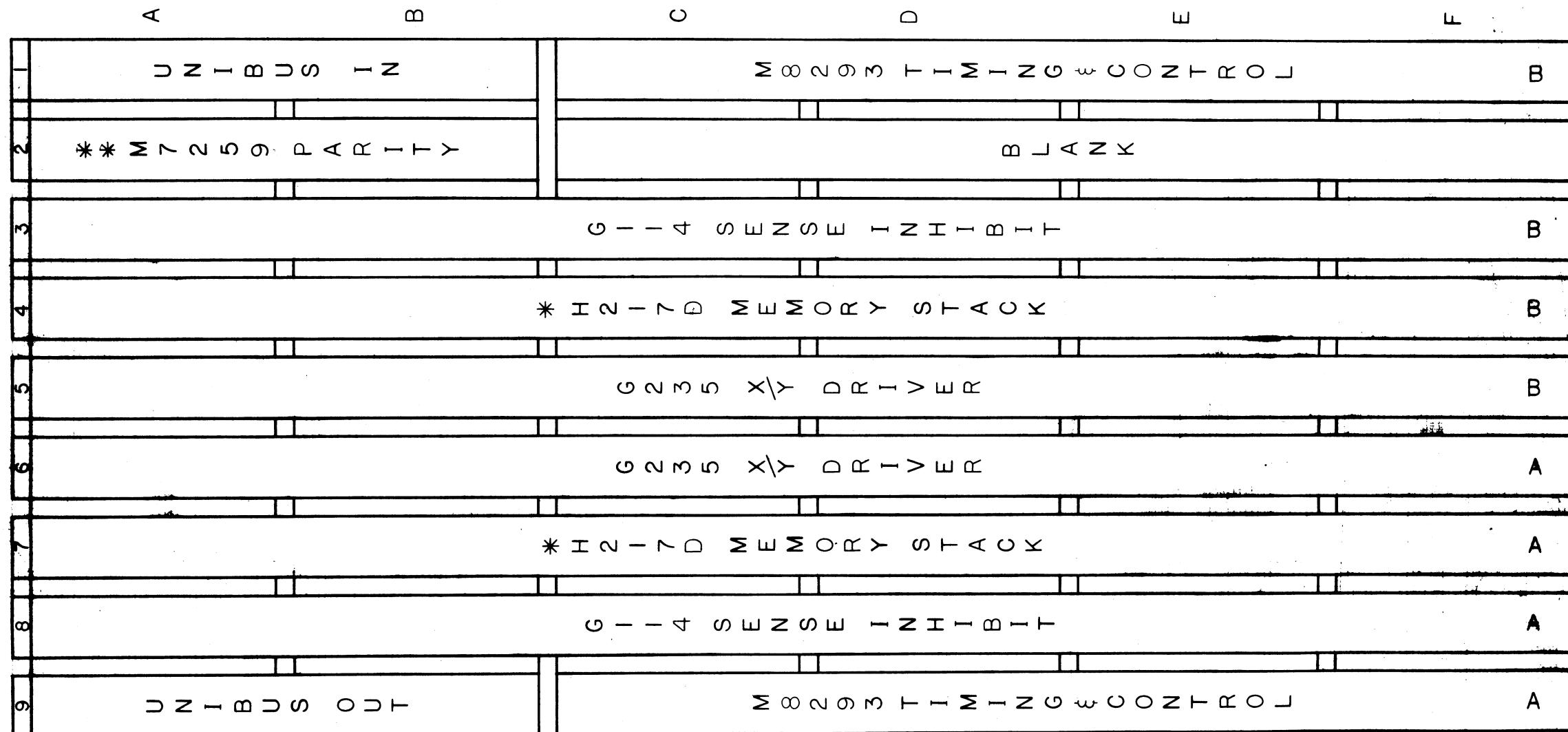
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## **NOTES**

- NOTES:**

  - \* 1. FOR MFII-UP (MEMORY WITH PARITY), USE H217C MEMORY STACK. THE H217C OR H217B MAY BE SUBSTITUTED FOR THE H217D IN NON PARITY SYSTEMS. THE H217B MAY BE SUBSTITUTED FOR THE H217C.
  - \* 2. M7259 IS USED WITH MFII-UP ONLY.
  - 3. INSTALL "A" MODULES FOR FIRST IGK; "B" MODULES FOR 2ND IGK.



VIEWED FROM MODULE SIDE OF BACKPLANE

A	IC TYPE	GND	+ 5V
<b>GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE</b>			
IC PIN LOCATIONS			
1	2	3	4
5	6	7	8
9	10	11	12
13	14	15	16
17	18	19	20

FIRST USED ON OPTION MODEL		QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.	
MFII-U			PARTS LIST				
			ETCH BOARD REV				
			DRN	DATE 4-17-73	digita EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
			CHK'D	DATE 4-13-73			
			ENG	DATE 5-15-73			
			PROL. ENG.	DATE 5-15-73			
			PROD.	DATE 6/11/73			
			NEXT HIGHER ASSY				
			B-DD-MFII-U				
			TITLE				
			MODULE UTILIZATION				
			REVISIONS				
			DEC NO.	EIA NO.	DEC NO.	EIA NO.	SIZE CODE
							NUMBER
							DMU MFII-U-MU
							REV.
							BL
							DIST.
SEMICONDUCTOR CONVERSION CHART							

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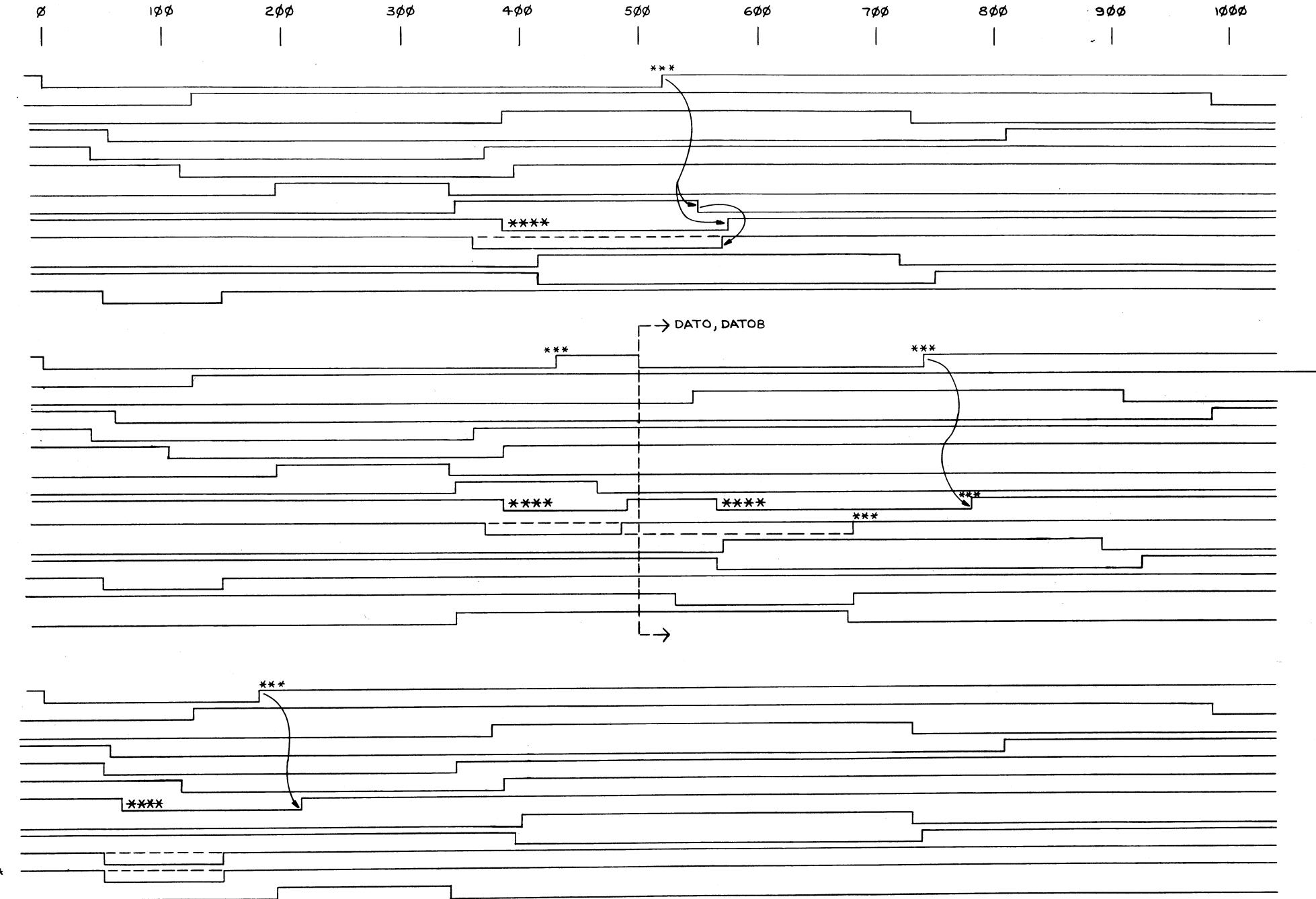
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2

1

n Sec



## NOTES:

1. \* IN THE DATOB MODE CLEAR MDR L ONLY OCCURS IN THE BYTE NOT BEING ADDRESSED.
2. \*\* IN THE DATOB MODE CLOCK MDR L ONLY OCCURS IN THE BYTE BEING ADDRESSED.
3. \*\*\* ACTUAL TIME DEPENDS ON BUS AND PROCESSOR DELAYS.
4. \*\*\*\* IN PARITY SYSTEMS BUS SSYN L WILL BE 20 NS LATER THAN SHOWN FOR DATO-DATOB BUSS MODES AND 150 NS LATER FOR DATI-DATIP MODES.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
<b>MFII-U</b>			PARTS LIST		
UNLESS OTHERWISE SPECIFIED			DRN. <i>H. Domanian</i>	DATE 4-19-73	
DIMENSION IN INCHES			CHKD. <i>J. Kirby</i>	DATE 4/30/73	
TOLERANCES			ENG. <i>D. Schuler</i>	DATE 5/29/73	
DECIMALS	ANGLES		PROJ. ENG. <i>D. Schuler</i>	DATE 5/29/73	
.xxx = .005	±0° 30'		REMOVED BY <i>D. Schuler</i>	DATE 5/29/73	
.xx = .02			PROD. <i>R. L. Ladd</i>	DATE 6/11/73	
.x = .1			NEXT HIGHER ASSY. <i>R. L. Ladd</i>	DATE 6/11/73	
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓			MATERIAL <b>B-DD-MFII-U</b>	SIZE CODE <b>D T D</b>	NUMBER <b>MFII-U-1</b>
FINISH	SCALE / /		REV. <b>A</b>	SHEET 1 OF 1	DIST.

REV.	CHANGE NO.	REV.
CHK	MFII-U-00001	A
REV	1-3-73	
CHANGE NO.	P. DIBANT	
REV	1-7-74	

DEC FORM NO. 102-C

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## PAGE REVISION CONTROL SHEET

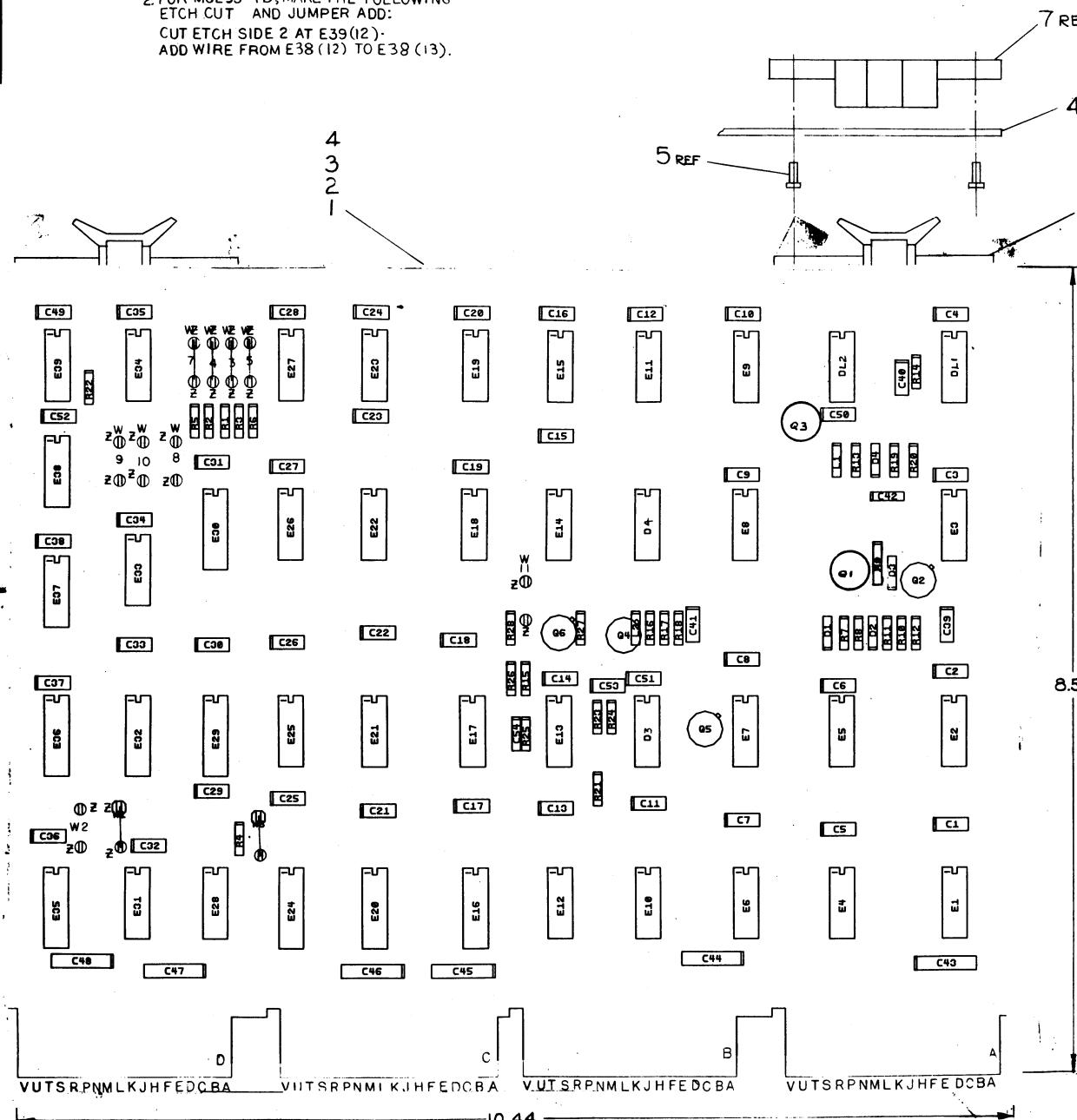
S/N.	PAGE REVISIONS							REMARKS	
	A	B	C	D	E	F	G		
1	A	B	C	D	E	F			
2	A	B	C	D	D	D			
3	A	B	C	D	D	D			
4	A	B	C	D	D	D			
5	A	B	C	D	D	D			
6	A	B	C	D	D	D			
7	A	B	C	D	D	D			
8	A	B	C	D	D	D			
9	A	B	C	D	D	D			
10	A	B	C	D	D	D			

DATE	ENG.	ETCH	ECO NO.	REV.						
9/27/73	R60d	B	00001	B	0R1G.					
11/16/73	R60d	B	00002	B	00003	C	00004	C	00005	20-Nov-76
11/4/74	R60d	C	00004	C	00005	C	00006	C	00007	4-6-75
11/16/75	R60d	B	00008	B	00009	C	00010	C	00011	20-Nov-76
12/19/75	R60d	C	00012	C	00013	C	00014	C	00015	20-Nov-76
12/20/75	R60d	B	00016	B	00017	C	00018	C	00019	20-Nov-76
12/21/75	R60d	C	00020	C	00021	C	00022	C	00023	20-Nov-76
12/22/75	R60d	B	00024	B	00025	C	00026	C	00027	20-Nov-76
12/23/75	R60d	C	00028	C	00029	C	00030	C	00031	20-Nov-76
12/24/75	R60d	B	00032	B	00033	C	00034	C	00035	20-Nov-76
12/25/75	R60d	C	00036	C	00037	C	00038	C	00039	20-Nov-76
12/26/75	R60d	B	00040	B	00041	C	00042	C	00043	20-Nov-76
12/27/75	R60d	C	00044	C	00045	C	00046	C	00047	20-Nov-76
12/28/75	R60d	B	00048	B	00049	C	00050	C	00051	20-Nov-76
12/29/75	R60d	C	00052	C	00053	C	00054	C	00055	20-Nov-76
12/30/75	R60d	B	00056	B	00057	C	00058	C	00059	20-Nov-76
12/31/75	R60d	C	00060	C	00061	C	00062	C	00063	20-Nov-76
1/1/76	R60d	B	00064	B	00065	C	00066	C	00067	20-Nov-76
1/2/76	R60d	C	00068	C	00069	C	00070	C	00071	20-Nov-76
1/3/76	R60d	B	00072	B	00073	C	00074	C	00075	20-Nov-76
1/4/76	R60d	C	00076	C	00077	C	00078	C	00079	20-Nov-76
1/5/76	R60d	B	00080	B	00081	C	00082	C	00083	20-Nov-76
1/6/76	R60d	C	00084	C	00085	C	00086	C	00087	20-Nov-76
1/7/76	R60d	B	00088	B	00089	C	00090	C	00091	20-Nov-76
1/8/76	R60d	C	00092	C	00093	C	00094	C	00095	20-Nov-76
1/9/76	R60d	B	00096	B	00097	C	00098	C	00099	20-Nov-76
1/10/76	R60d	C	00100	C	00101	C	00102	C	00103	20-Nov-76
1/11/76	R60d	B	00104	B	00105	C	00106	C	00107	20-Nov-76
1/12/76	R60d	C	00108	C	00109	C	00110	C	00111	20-Nov-76
1/13/76	R60d	B	00112	B	00113	C	00114	C	00115	20-Nov-76
1/14/76	R60d	C	00116	C	00117	C	00118	C	00119	20-Nov-76
1/15/76	R60d	B	00120	B	00121	C	00122	C	00123	20-Nov-76
1/16/76	R60d	C	00124	C	00125	C	00126	C	00127	20-Nov-76
1/17/76	R60d	B	00128	B	00129	C	00130	C	00131	20-Nov-76
1/18/76	R60d	C	00132	C	00133	C	00134	C	00135	20-Nov-76
1/19/76	R60d	B	00136	B	00137	C	00138	C	00139	20-Nov-76
1/20/76	R60d	C	00140	C	00141	C	00142	C	00143	20-Nov-76
1/21/76	R60d	B	00144	B	00145	C	00146	C	00147	20-Nov-76
1/22/76	R60d	C	00148	C	00149	C	00150	C	00151	20-Nov-76
1/23/76	R60d	B	00152	B	00153	C	00154	C	00155	20-Nov-76
1/24/76	R60d	C	00156	C	00157	C	00158	C	00159	20-Nov-76
1/25/76	R60d	B	00160	B	00161	C	00162	C	00163	20-Nov-76
1/26/76	R60d	C	00164	C	00165	C	00166	C	00167	20-Nov-76
1/27/76	R60d	B	00168	B	00169	C	00170	C	00171	20-Nov-76
1/28/76	R60d	C	00172	C	00173	C	00174	C	00175	20-Nov-76
1/29/76	R60d	B	00176	B	00177	C	00178	C	00179	20-Nov-76
1/30/76	R60d	C	00180	C	00181	C	00182	C	00183	20-Nov-76
1/31/76	R60d	B	00184	B	00185	C	00186	C	00187	20-Nov-76
2/1/76	R60d	C	00188	C	00189	C	00190	C	00191	20-Nov-76
2/2/76	R60d	B	00192	B	00193	C	00194	C	00195	20-Nov-76
2/3/76	R60d	C	00196	C	00197	C	00198	C	00199	20-Nov-76
2/4/76	R60d	B	00198	B	00199	C	00200	C	00201	20-Nov-76
2/5/76	R60d	C	00202	C	00203	C	00204	C	00205	20-Nov-76
2/6/76	R60d	B	00206	B	00207	C	00208	C	00209	20-Nov-76
2/7/76	R60d	C	00210	C	00211	C	00212	C	00213	20-Nov-76
2/8/76	R60d	B	00214	B	00215	C	00216	C	00217	20-Nov-76
2/9/76	R60d	C	00218	C	00219	C	00220	C	00221	20-Nov-76
2/10/76	R60d	B	00222	B	00223	C	00224	C	00225	20-Nov-76
2/11/76	R60d	C	00226	C	00227	C	00228	C	00229	20-Nov-76
2/12/76	R60d	B	00230	B	00231	C	00232	C	00233	20-Nov-76
2/13/76	R60d	C	00234	C	00235	C	00236	C	00237	20-Nov-76
2/14/76	R60d	B	00238	B	00239	C	00240	C	00241	20-Nov-76
2/15/76	R60d	C	00242	C	00243	C	00244	C	00245	20-Nov-76
2/16/76	R60d	B	00246	B	00247	C	00248	C	00249	20-Nov-76
2/17/76	R60d	C	00250	C	00251	C	00252	C	00253	20-Nov-76
2/18/76	R60d	B	00254	B	00255	C	00256	C	00257	20-Nov-76
2/19/76	R60d	C	00258	C	00259	C	00260	C	00261	20-Nov-76

**NOTES:**  
 1. UNLESS OTHERWISE SPECIFIED:  
 RESISTANCE IS IN OHMS,  
 CAPACITANCE IS IN MICROFARADS.  
 2. FOR M8293-YB, MAKE THE FOLLOWING  
 ETCH CUT AND JUMPER ADD:  
 CUT ETCH SIDE 2 AT E39(12).  
 ADD WIRE FROM E38 (12) TO E38 (13).

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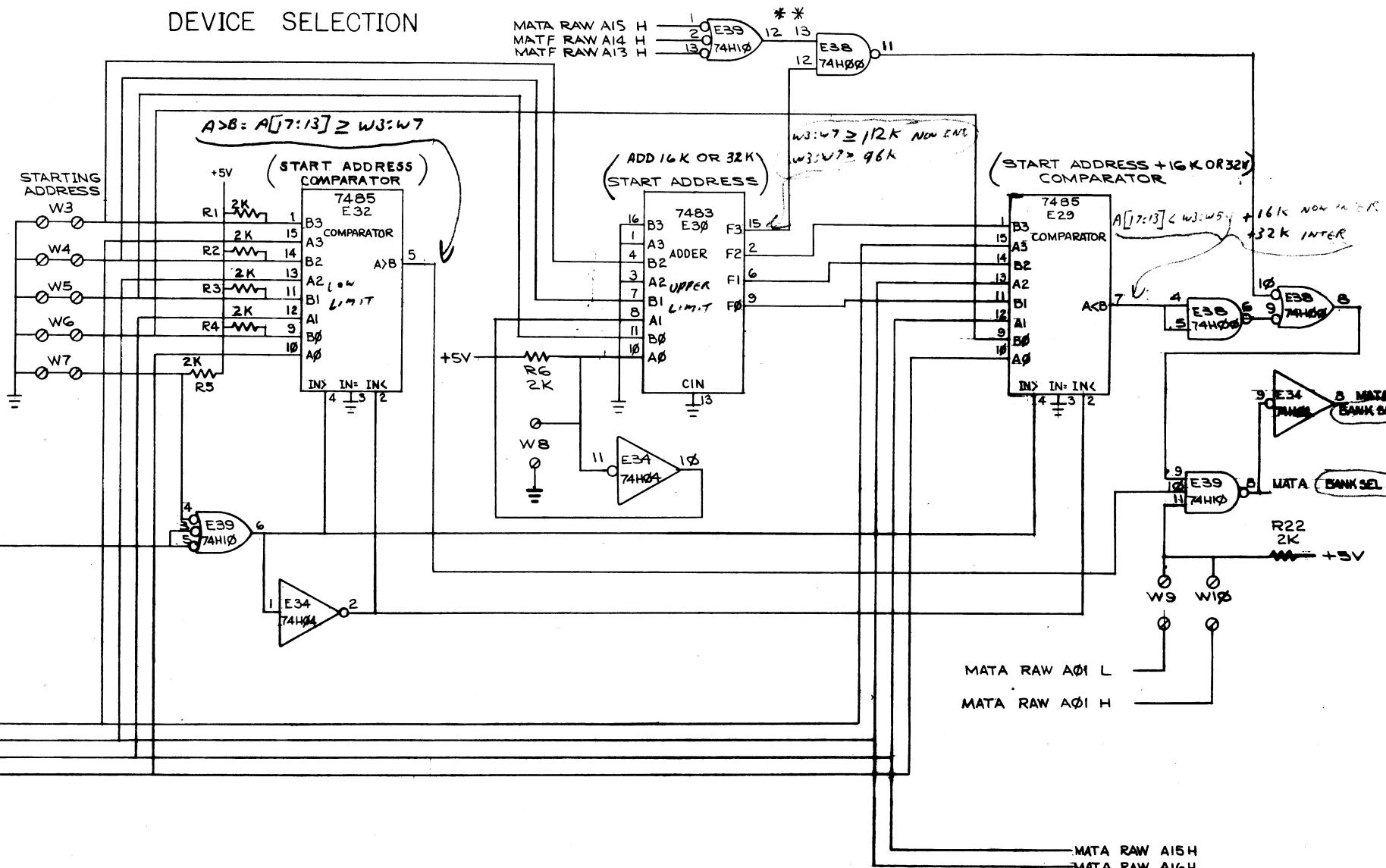
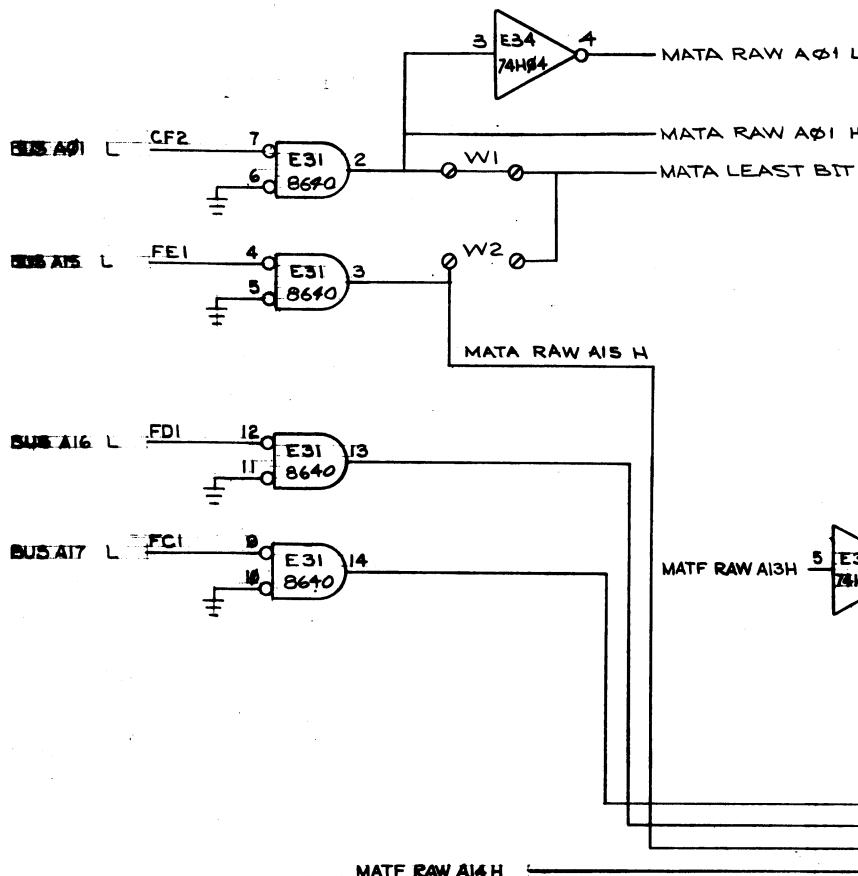
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DCS M8293-01

REV.



NOTE: INTERLEAVE CONTROL IS ACHIEVED AS FOLLOWS:

a) NON-INTERLEAVED

W1 IN  
W2, W8, W9 + W10 OUT

b) INTERLEAVED

W1 OUT  
W2, W8 IN

W9 IN → ONE MEMORY  
W10 OUT → THE OTHER MEMORY

STARTING ADDRESS FOR THE COMBINED INTERLEAVED MEMORY IS THE SAME AS FOR THE NON-INTERLEAVED CASE (W3 THRU W7 MUST BE CUT THE SAME FOR BOTH INTERLEAVED MEMORIES) BUT THE INTERLEAVED MAX ADDRESS IS INCREASED BY 16K (10000000)

0=IN 1=OUT						
NON-INTERLEAVED START ADDRESS	A <sub>17</sub> W <sub>3</sub>	A <sub>16</sub> W <sub>4</sub>	A <sub>15</sub> W <sub>5</sub>	A <sub>14</sub> W <sub>6</sub>	A <sub>13</sub> W <sub>7</sub>	NON-INTERLEAVED MAX ADDRESS
0000000 (8K)	0	0	0	0	0	077776
0200000 (4K)	0	0	0	0	1	117776
0400000 (8K)	0	0	0	1	0	137776
0600000 (12K)	0	0	0	1	1	157776
1000000 (16K)	0	0	1	0	0	177776
1200000 (20K)	0	0	1	0	1	217776
1400000 (24K)	0	0	1	1	0	237776
1600000 (28K)	0	0	1	1	1	257776
2000000 (32K)	0	1	0	0	0	277776
2200000 (36K)	0	1	0	0	1	317776
2400000 (40K)	0	1	0	1	0	337776
2600000 (44K)	0	1	0	1	1	357776
3000000 (48K)	0	1	1	0	0	377776
3200000 (52K)	0	1	1	0	1	417776
3400000 (56K)	0	1	1	1	0	437776
3600000 (60K)	0	1	1	1	1	457776
4000000 (64K)	1	0	0	0	0	477776

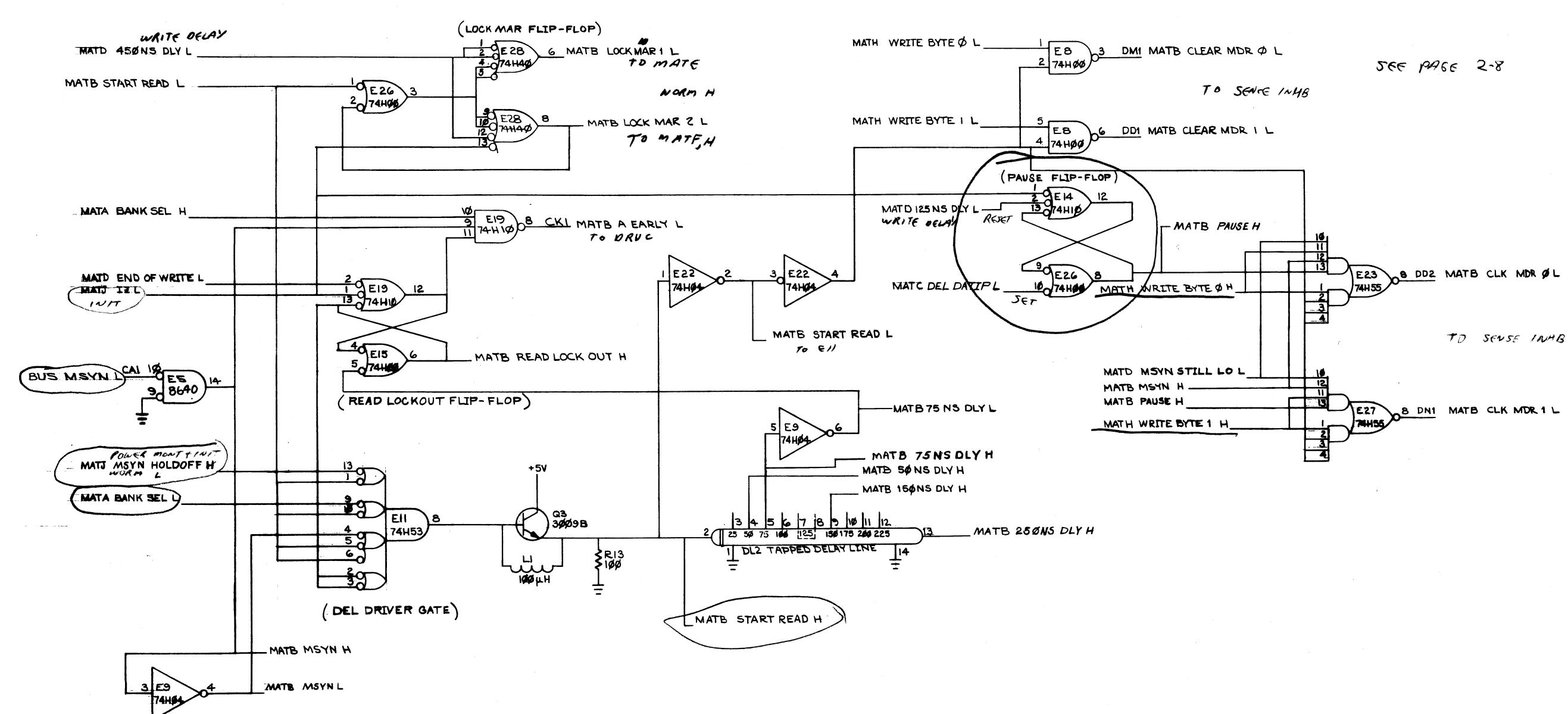
\*\* M8293-YB WILL RESPOND TO BUS ADDRESSES BETWEEN 124-128K.  
\* THE MEMORY WILL NOT RESPOND TO BUS ADDRESSES BETWEEN 124-128K

	W <sub>3</sub>	W <sub>4</sub>	W <sub>5</sub>	W <sub>6</sub>	W <sub>7</sub>
4200000 (8K)	1	0	0	0	1
4400000 (72K)	1	0	0	1	0
4600000 (76K)	1	0	0	1	1
5000000 (80K)	1	0	1	0	0
5200000 (84K)	1	0	1	0	1
5400000 (88K)	1	0	1	1	0
5600000 (92K)	1	0	1	1	1
6000000 (96K)	1	1	0	0	0
6200000 (100K)	1	1	0	0	1
6400000 (104K)	1	1	0	1	0
6600000 (108K)	1	1	0	1	1
7000000 (112K)	1	1	1	0	0
7200000 (116K)	1	1	1	0	1
7400000 (120K)	1	1	1	1	0

DEVICE SELECTION LOGIC

REVISIONS	CHANGE NO.	REV.
DCS	M8293-01	F2
SCALE	SHEET 3 OF 10	DIST.

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## READ START TIMING

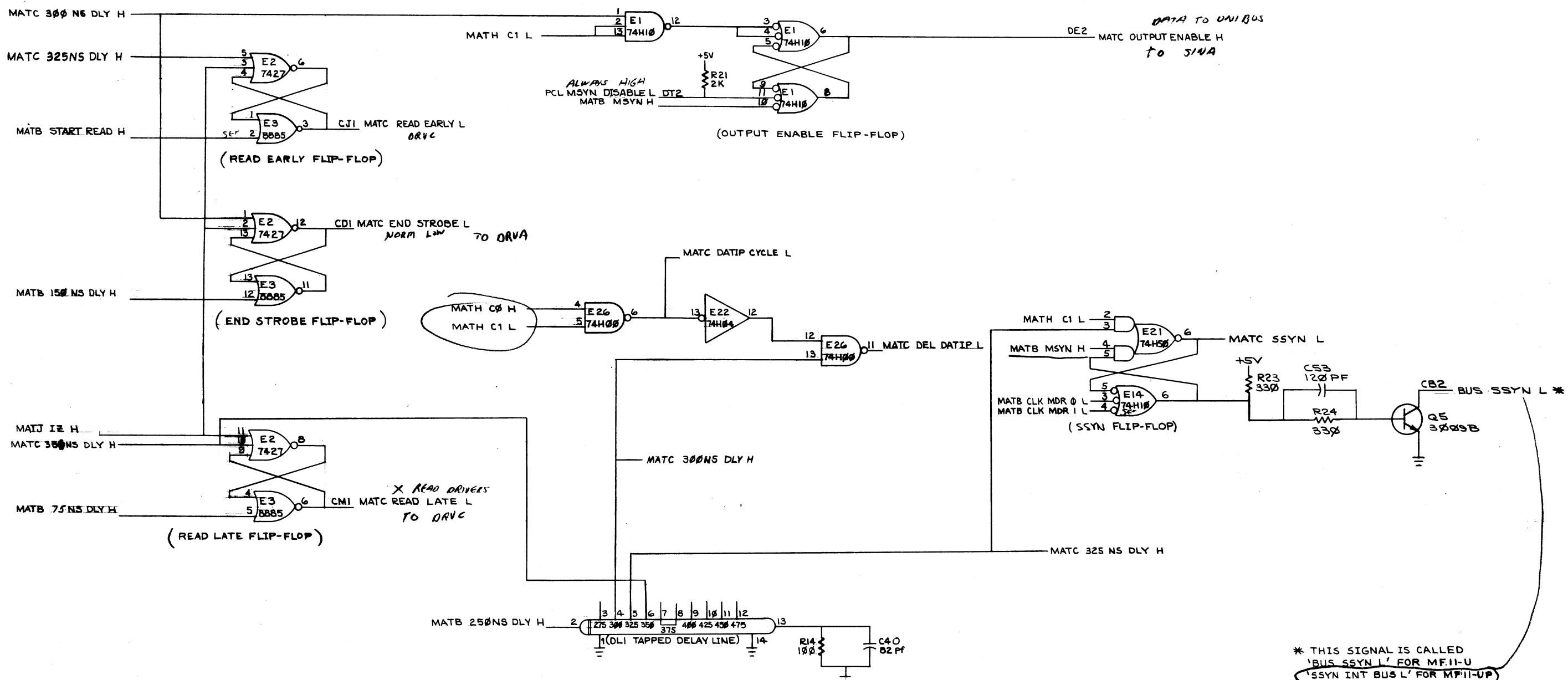
TITLE | 16K UNIBUS TIMING  
(MATB) |

SIZE CODE | DCS M 8293-0-1 | NUMBER | REV. |  
E | | | |

SCALE - # | SHEET 4 OF 10 | DIST. |

REVISIONS		
CHK	CHANGE NO.	REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. 100-128  
DRAFT

READ TIMING

TITLE 16K UNIBUS TIMING  
(MATIC)

SIZE CODE NUMBER REV.

DCS M8293-0-1 E

SCALE / SHEET 5 OF 10 DIST.

TYPE CODE M8293-0-1  
NUMBER M8293-0-1  
DATE 1/1/73

B

A

D

C

B

A

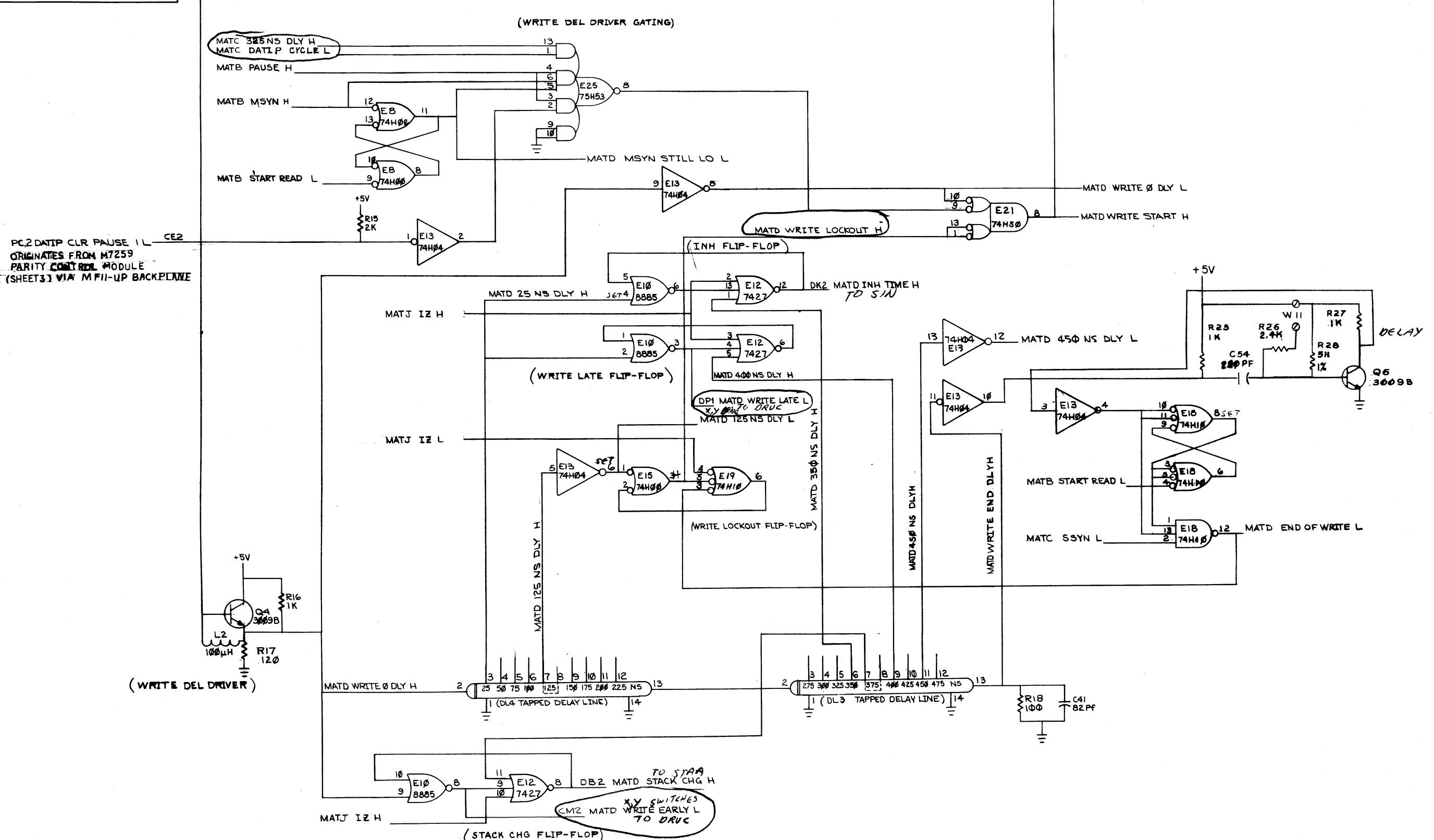
RWJ

REV.

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REVISIONS		
CHK	CHANGE NO.	REV.

## WRITE TIMING

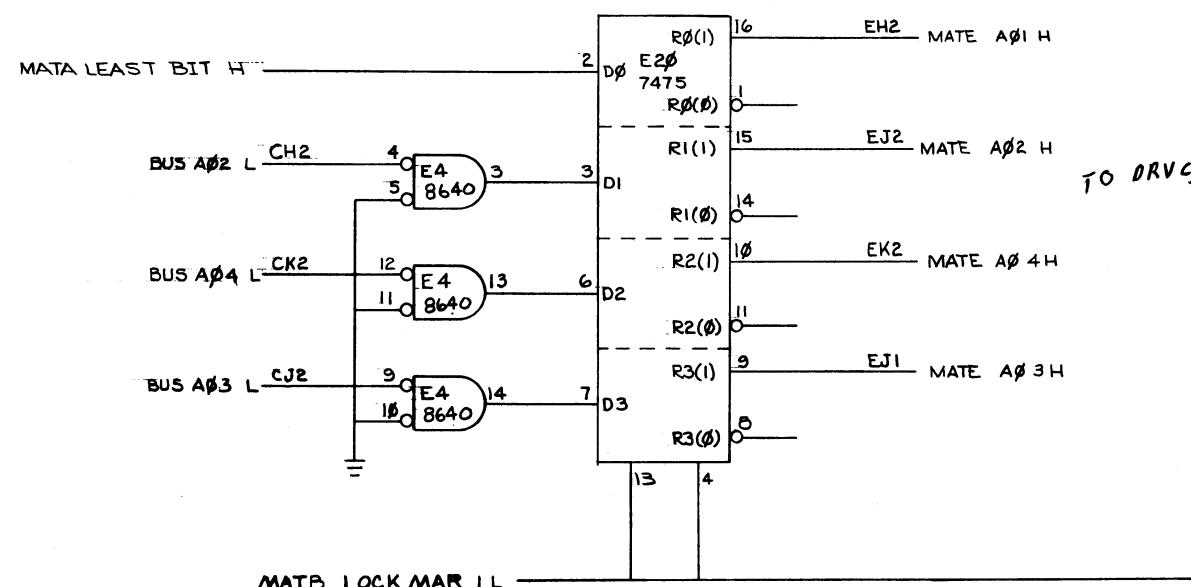
# KUNIBUS TIMING (MATD)

SHEET 6 OF 10

SIZE	CODE	NUMBER
D	CS	M8293-Ø-1

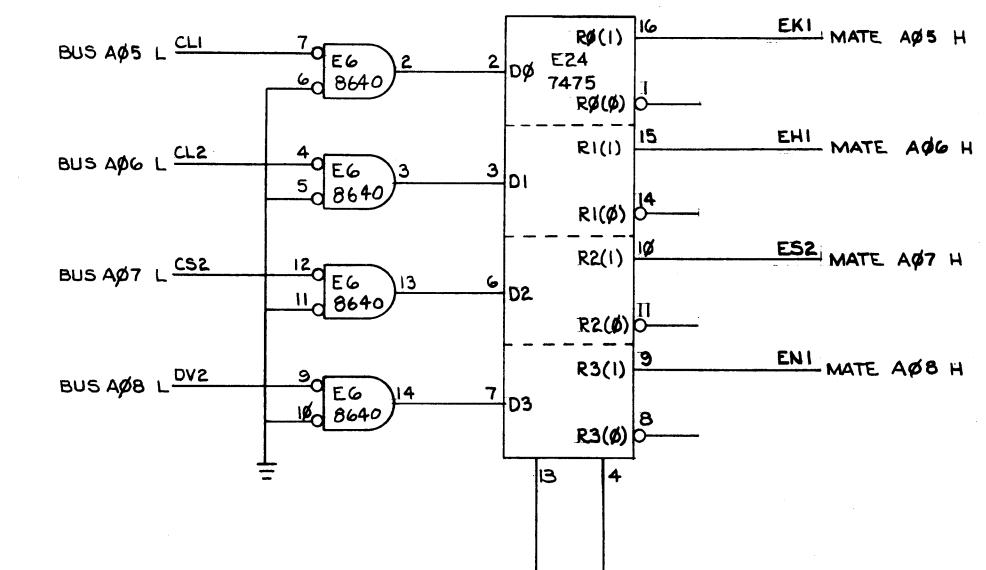
DIST.

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IF LOCK MAR 1 H  
 The input is passed to output

L inhibit input



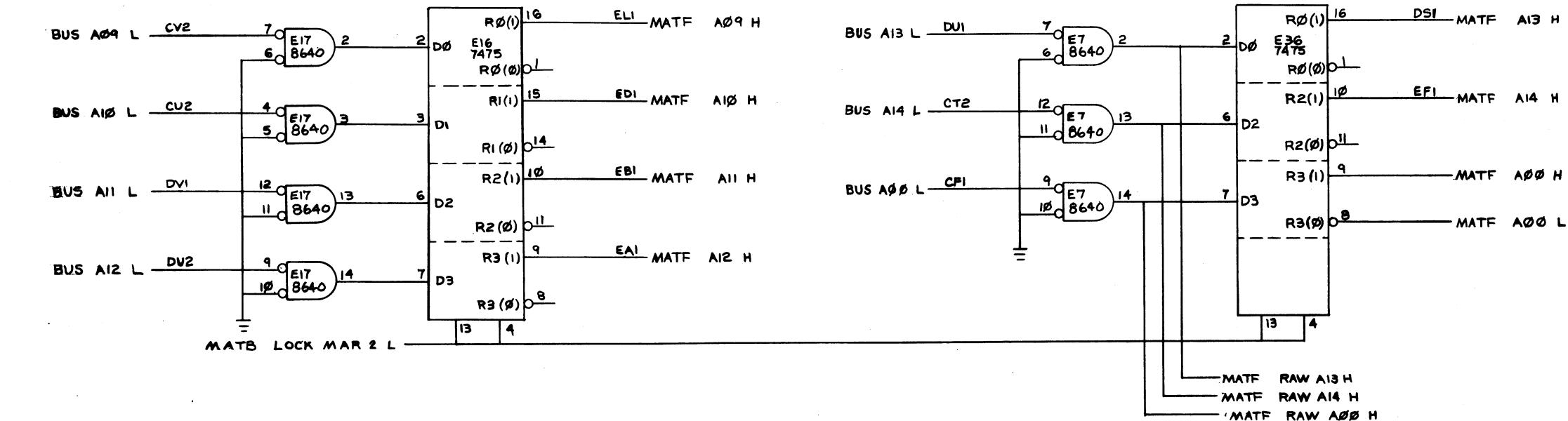
REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO.  
DRD 138

SIZE CODE DCS NUMBER MB293-0-1 REV. J

A01-A08 LATCHES  
 16K UNIBUS TIMING (MATE)  
 SIZE CODE DCS NUMBER M8293-0-1 REV. E  
 SCALE # SHEET 7 OF 10 DIST.

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REVISIONS		
CHK	CHANGE NO.	REV.

A00, A09 → A13 LATCHES  
TITLE 16K UNIBUS TIMING  
(MATF)  
SIZE CODE DCS NUMBER M8293-0-1  
REV. E

SCALE 1:1 SHEET 8 OF 10 DIST.

1

8

7

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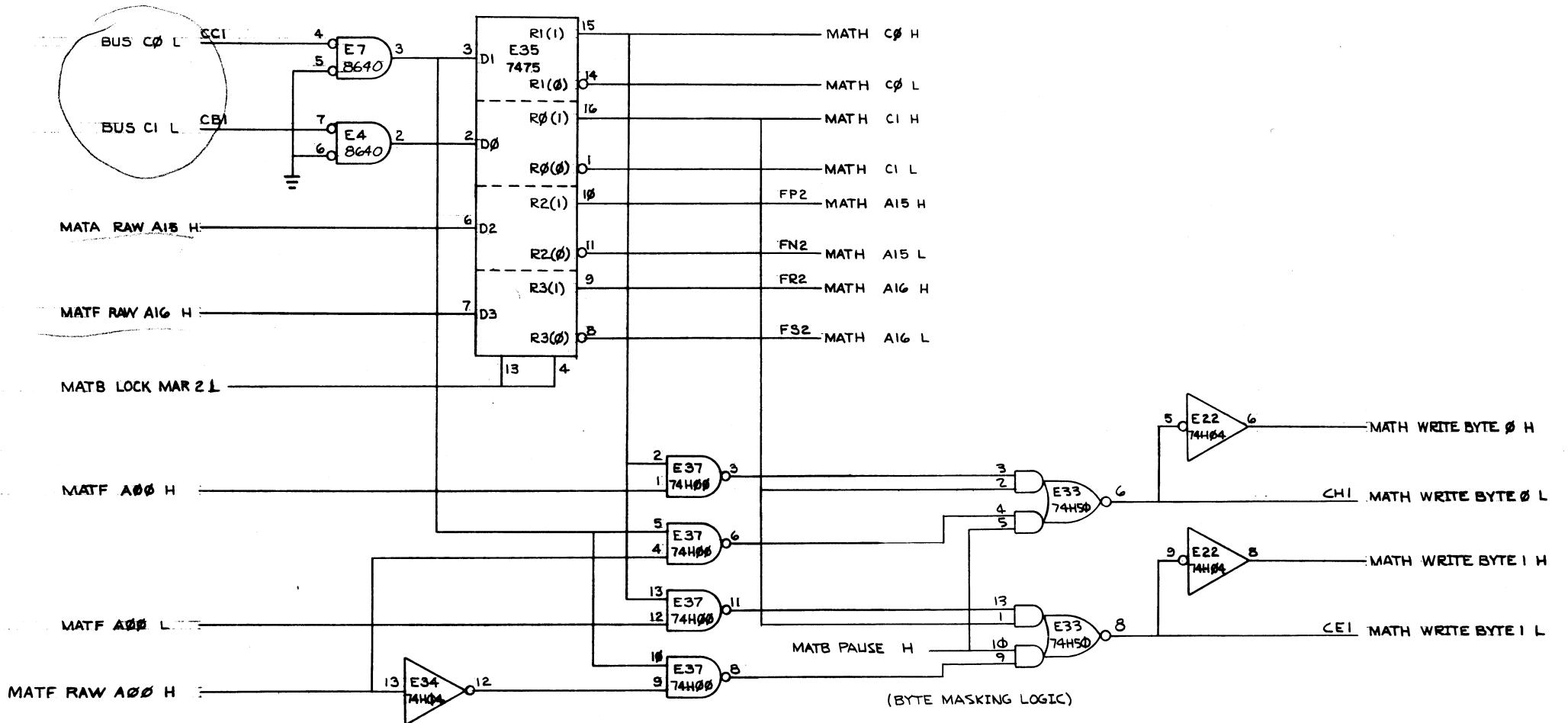
4

3

1

DCS M8293-0-1 E 2

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BYTE 0 = LOW BYTE  
BYTE 1 = HIGH BYTE

REVISIONS		
CHK	CHANGE NO.	REV.

1

DOC FORM NO.

GPO 128

8

7

6

5

4

3

1

## LATCHES &amp; BYTE MASKING

TITLE 16K UNIBUS TIMING  
(MATH)

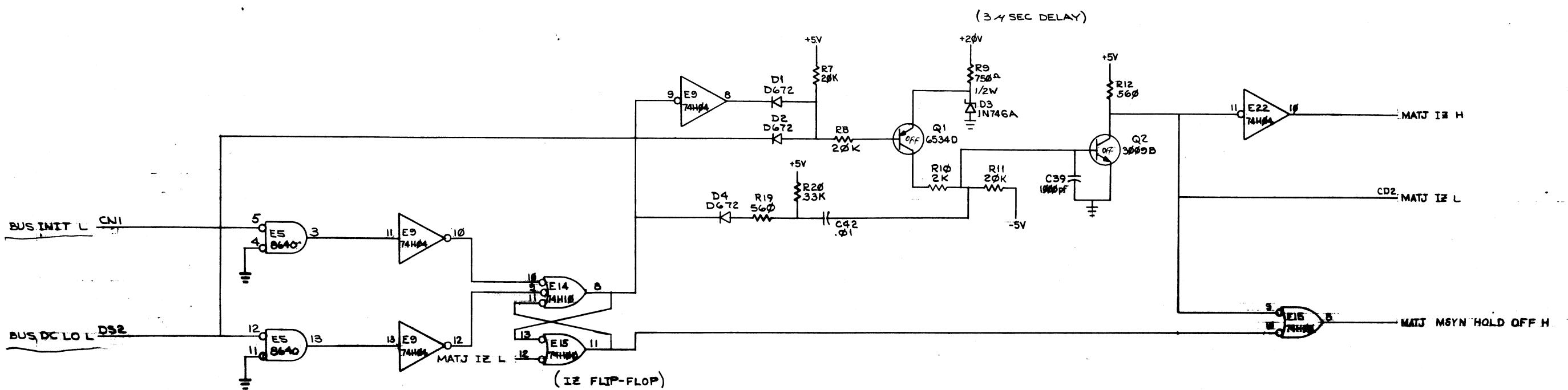
SCALE # SHEET 9 OF 10 DIST.

SIZE CODE DCS M8293-0-1 REV. E

SIZE CODE DCS M8293-0-1 REV. E

A

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REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO.  
DOD 120

8

7

6

5

4

3

2

1

TITLE	SIZE CODE	NUMBER	REV.
16K UNIBUS TIMING (MATJ)	DCS	M8293-0-1	E
SCALE	SHEET	10 OF 10	DIST.

PAGE REVISION CONTROL SHEET

PAGE REVISION CONTROL SHEET

SH. NO.	PAGE REVISIONS					REMARKS		
	DATE	ENG.	ETCH	REV.	ECO NO.	FIRST USED ON OPTION/MODEL	NUMBER	REV.
1	C	D	E	F	H	5/12/76	CS G235 - O-1	N
2	C	D	E	F	H	5-12-75		
3	C	D	E	F	H	11-23-75		
4	C	D	E	F	H	9-11-74		
5						3/13/74		
6						11-16-73		
7						8-15-73		
8						7/23/73		
9						1-1-73		
10						12-19-73		
11						11-16-73		
12						8-15-73		
13						7/23/73		
14						1-1-73		
15						12-19-73		
16						11-16-73		
17						8-15-73		
18						7/23/73		
19						1-1-73		
20						12-19-73		
21						11-16-73		
22						8-15-73		
23						7/23/73		
24						1-1-73		
25						12-19-73		
26						11-16-73		
27						8-15-73		
28						7/23/73		
29						1-1-73		
30						12-19-73		
31						11-16-73		
32						8-15-73		
33						7/23/73		
34						1-1-73		
35						12-19-73		
36						11-16-73		
37						8-15-73		
38						7/23/73		
39						1-1-73		
40						12-19-73		
41						11-16-73		
42						8-15-73		
43						7/23/73		
44						1-1-73		
45						12-19-73		
46						11-16-73		
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143						7/23/73		
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150						12-19-73		
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153						7/23/73		
154						1-1-73		
155						12-19-73		
156						11-16-73		
157						8-15-73		
158						7/23/73		
159						1-1-73		
160						12-19-73		
161						11-16-73		
162						8-15-73		
163						7/23/73		
164						1-1-73		
165						12-19-73		
166						11-16-73		
167						8-15-73		
168								

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### NOTES:

1. \* INDICATES NOT USED ON MFII-U & MFII-UP (2 PLACES).
2. \*\* INDICATES NOT USED ON MFII-U & MFII-UP, BUT ARE TIED TO UNUSED TERMINATORS ON THE GI14 MODULE, WHICH FORCES THEM TO +3V (5 PLACES).
3. 1 THERMISTOR LOCATED ON H217 STACK MODULE, 1 ON G235

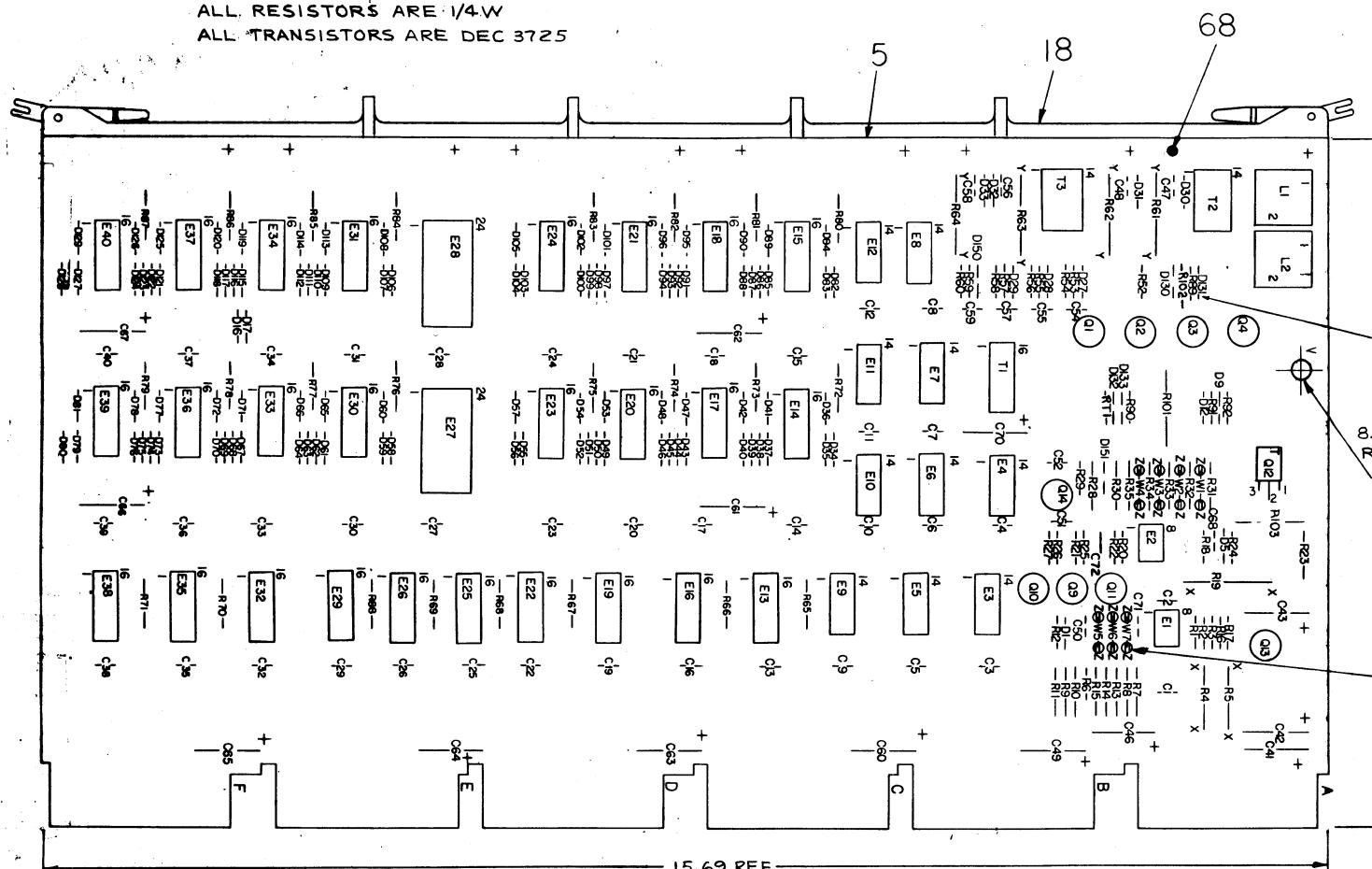
4. UNLESS OTHERWISE INDICATED;

ALL DIODES ARE D672

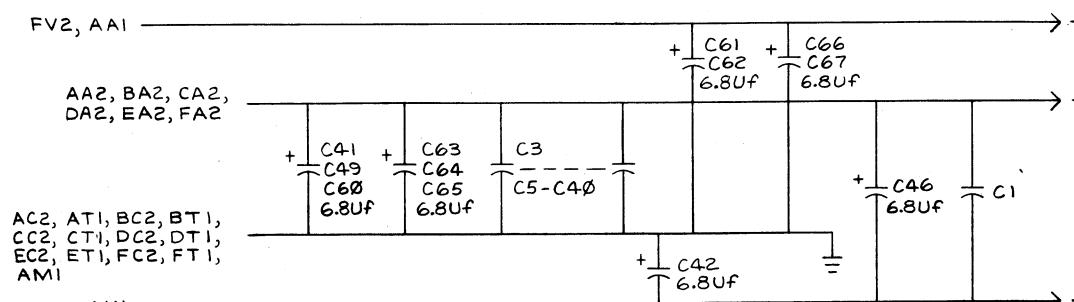
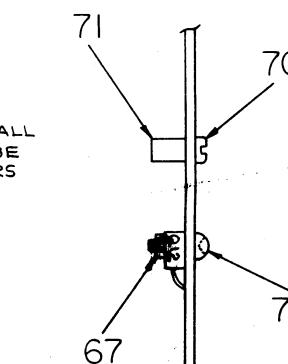
ALL CAPACITORS ARE .01 UF

ALL RESISTORS ARE 1/4W

ALL TRANSISTORS ARE DEC 3725



CATHODE END OF ALL  
DIODES SHALL BE  
TOWARD FINGERS



AC2, AT1, BC2, BT1,  
CC2, CT1, DC2, DT1,  
EC2, ET1, FC2, FT1,  
AM1

AK1

74121	7	—	—
741	—	—	—
75325	—	9	16
7442	8	16	—
74154	12	24	—
IC TYPE	GND	+ 5V	+20V

GND AND 5V ARE USUALLY PIN 7 AND 14  
RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE

### IC PIN LOCATIONS

CHG NO.	REV.	REVISIONS	ETCH BOARD REV.	PARTS LIST							
				QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.			
FIRST USED ON OPTION MODEL											
MFII-U & MFII-UP											
DRN. <i>[Signature]</i>	DATE 4-4-73	digital EQUIPMENT CORPORATION	CHK'D. <i>[Signature]</i>	DATE 4-4-73	MAINTAINANCE	ENG. <i>[Signature]</i>	DATE 4-4-73	TITLE			
PRO. ENG. <i>[Signature]</i>	DATE 4-4-73	MANUFACTURED BY MAYNARD, MASSACHUSETTS	PRO. ENG. <i>[Signature]</i>	DATE 4-4-73	PROD. <i>[Signature]</i>	PROD. <i>[Signature]</i>	DATE 4-4-73				
NEXT HIGHER ASSY											
DEC NO.	EIA NO.	DEC NO.	EIA NO.	SCALE 1/1	SHEET 2 OF 6	DIST. <i>[Signature]</i>	SIZE CODE DCS G235-0-1	NUMBER N			

SEMICONDUCTOR CONVERSION CHART

16K X-Y DRIVE

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REAR

The diagram illustrates the timing sequence of various control signals:

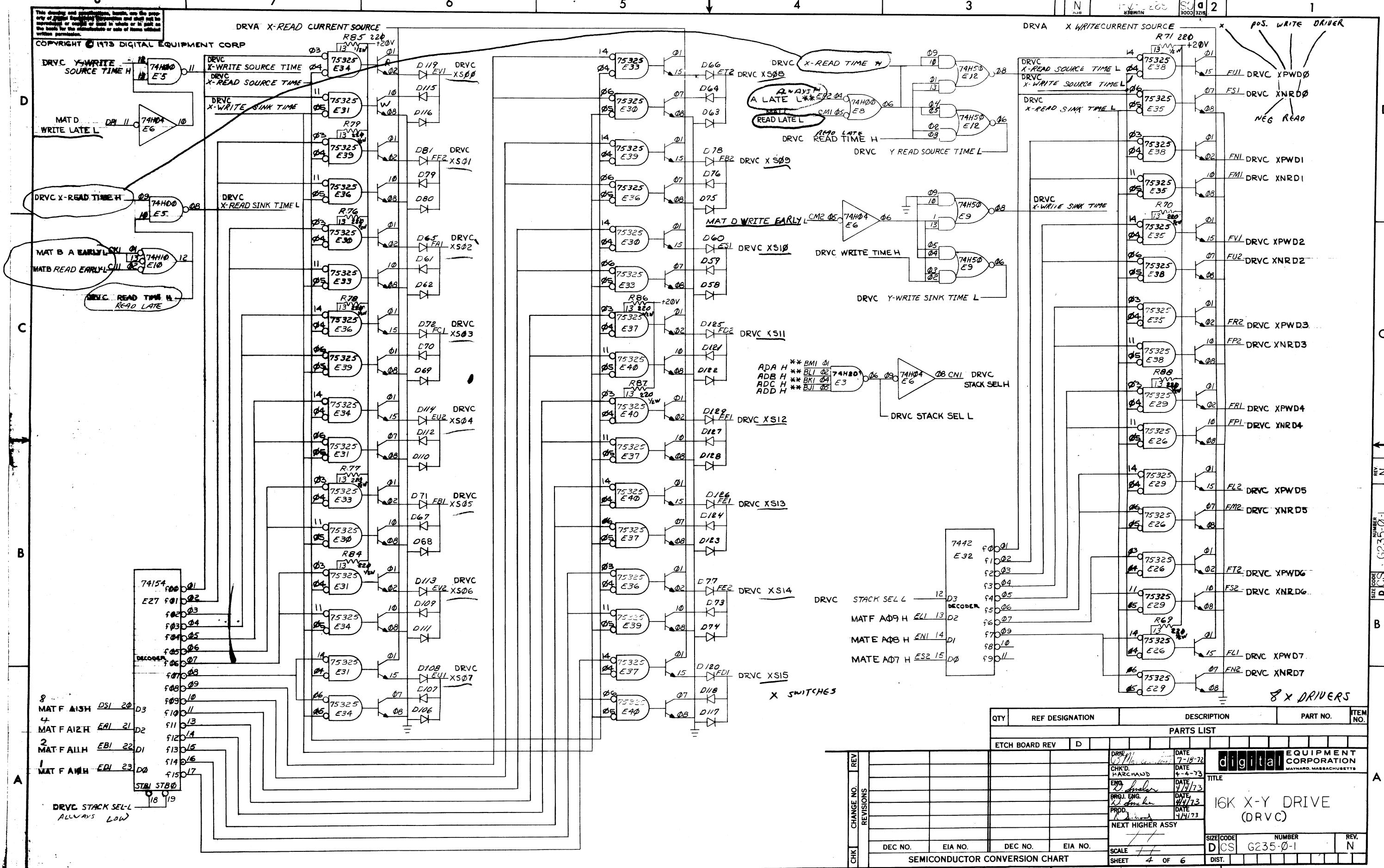
- msyn**: A pulse that triggers the start of the sequence.
- A EARLY**: A pulse occurring shortly after msyn.
- READ EARLY**: A pulse starting at time  $t = 0$ , labeled  $325 \text{ ns}$ .
- READ LATE**: A pulse starting at time  $t = 325 \text{ ns}$ , labeled  $275 \text{ ns}$ .
- XREAD SW TIME**: A pulse starting at time  $t = 325 \text{ ns}$ , labeled  $\times \text{RSW on}$ .
- XDRV**: A pulse starting at time  $t = 325 \text{ ns}$ , labeled  $\times \text{DRV}$ .
- SIRB ONE SHOT**: A pulse starting at time  $t = 325 \text{ ns}$ , labeled  $175 \text{ ns}$ .
- SSQ1**: A pulse starting at time  $t = 325 \text{ ns}$ , labeled  $190$  and  $370$ .

The diagram illustrates three timing signals relative to a reference time mark at 0 ns:

- WRITE**: A rectangular pulse starting at 0 ns and ending at 375 ns.
- WRITE EARLY**: A rectangular pulse starting at 0 ns and ending at 375 ns.
- WRITE LATE**: A rectangular pulse starting at 410 ns and ending at 375 ns.

SHEET 2 OF 6									
1	E6	IC DEC 74H04	1909931	62					
1	E10	IC DEC 74H10	1909057	63	REF	X-Y COORDINATE HOLE LOCATION	K-CO-G235-0-4	1	
2	E7,E11	IC DEC 74H40	1905586	64	REF	ASSY/DRILLING HOLE LAYOUT	D-AH-G235-0-5	2	
24	E13-E18,E20-E26,E29-E31, E33-E40	IC DEC 75325	1910960	65	REF	ECO MODULE HISTORY	B-MH-G235-0-6	3	
2	E9,E12	IC DEC 74H50	1909060	66	1 C71	ETCHED CIRCUIT BD.	5010145	4	
1		KEPNUT 4-40	9006557	67	46 CI-C40,C48,C50,C52, C58,C68,C72 C59,C54,C55,C57	CAP .01UF 50V 20%	1000011	5	
12		EYELET HANDLE	9006732	68	4	CAP .005 UF 100V 20% DISC	1001610	6	
14		SPLIT LUGS	9006735	69	1 C51	CAP 18 PF 100V 5% D.M.	1002608	7	
1		SCREW NYLON 6-32	9008212-1	70	1 C43	CAP 47 UF 20V 10% S. TANT	1004814	8	
1		STAND OFF 1/4 X 3/8	9008213	71	13 C41,C42,C46,C49,C60-C67,C70	CAP 6.8UF 35V 10% S. TANT	1005306	9	
1		SCREW (PHILLIPS PAN HEAD)4-40 X 5//6	900600-1	72	1 D1	DIODE ZENER IN753A 6.2V ± 5%	1102421	10	
1	R31	RES 10.6K 1/8W 1%	1309419	73	109 D9,D12,D17, D27-D130,D132,D150	DIODE D672	1105275	11	
AR	W1-W7	WIRE #22 AWG (SOLID)	9107560-1	74	1 D16	DIODE ZENER IN5248B 18V ± 10%	1110766	12	
1	R91,	RES 180Ω 1/4W 5%	1301322	75	1 D5	DIODE ZENER IN749A 4.3V ± 5%	1109977	13	
1	D133	DIODE ZENER IN752A 5.6V 5%	1102808	76	1 D131	DIODE ZENER IN754A 6.8V ± 5%	1109991	14	
1	R92	RES 150Ω 1/4W 5%	1300250	77	1 D151	DIODE ZENER IN750A 4.7V ± 5%	1100124	15	
2	C47, C56	CAP. 0.022UF 50V	1011683	78	1	HANDLE ASSY	1210711-2	16	
1	RT1	THERMISIER 300Ω 2%	1309785	79	2 R18,R24	RES 100 1/4W 5%	1300229	17	
1	R102	RES 330Ω 1/4W 5%	1300295	80	12 R69-R71,R76-R79,R84-R88	RES 220 1/2W 5%	1300274	18	
1	Q11	TRANS. DEC 4258	1505321	81	1 R101	RES 220 2W 10%	1300278	19	
1	E3	IC. DEC 74H2Φ	1905635	82	12 R65-R68,R72-R75,R80-R83	RES 270 1/2W 5%	1300285	20	
1	R7	RES. 9.09K 1/8W 1%	1304855	83	2 R21,R27	RES 470 1/4W 5%	1300316	21	
1	R103	RES. 75Ω 1W 5%	1305281	84	2 R3,R16,	RES 1K 1/4W 5%	1300365	22	
A/R		WIRE *30	9105740-55	85	1 R23	RES 1K 1/2W 5%	1300264	23	
				1 R2	RES 4.7K 1/4W 5%	1300447	24		
				1 R17	RES 10 1/4W 5%	1301317	25		
				1 R89	RES 82Ω 1/4W 5%	1301477	26		
				4 R61-R64	RES 10Ω 2W 10%	1300172	27		
				1 R22	RES 22K 1/4W 5%	1301808	28		
				1 R12	RES 270 1/4W 5%	1301972	29		
				4 R54,R56,R58,R60	RES 18 1/4W 5%	1302124	30		
				4 R53,R55,R57,R59	RES 75 1/4W 5%	1302379	31		
				4 R25,R26,R52,R20	RES 2K 1/4W 5%	1302388	32		
				2 R1,R6	RES 470K 1/4W 5%	1302398	33		
				1 R29	RES 120K 1/4W 5%	1300539	34		
				2 R32,R8	RES 10K 1/8W 1%	1302886	35		
				2 R28,R30	RES 14.7K 1/8W 1%	1302941	36		
				1 R9	RES 2871/8W 1%	1305124	37		
				1 R10	RES 198 1/8W 1%	1302956	38		
				1 R35	RES 3.16K 1/8W 1%	1302045	39		
				1 R34	RES 34.8K 1/8W 1%	1303156	40		
				1 R14,	RES 243K 1/8W 1%	1304843	41		
				1 R11	RES 2.61K 1/8W 1%	1305393	42		
				2 R15,R33,	RES 68.1K 1/8W 1%	1305252	43		
				1 R13	RES 121K 1/8W 1%	1305255	44		
				2 R4,R5	RES .25 3W 1%	1310219	45		
				1 R19	RES .08 5W 3%	1310983	46		
				1 R90	RES 56Ω 1/4W 5%	1302602	47		
				1 Q14	TRANS DEC 2904A	1501913	48		
				1 Q13	TRANS DEC 6534B	1503409-1	49		
				1 Q12	TRANS DEC 4920	1509605	50		
				6 Q1-Q4,Q9,Q10	TRANS DEC 3725	1510959	51		
				1 T1	PULSE TRANSFORMER (DIP)	1609651	52		
				2 T2,T3	SATURATING TRANSFORMER-XY	1610962	53		
				2 L1,L2	CHOKE 400 UH	1610963	54		
				2 E27,E28	IC DEC 74154	1909701	55		
				2 E19,E32	IC DEC 7442	1910046	56		
				1 E4	IC DEC 74121	1910230	57		
				2 E1,E2	IC DEC 741	1910298	58		
				2 E5,E8	IC DEC 74H00	1909056	59		
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.	REV.
					TITLE				
					16K X-Y DRIVE				
					SIZE CODE				
					DOS	G235-0-1			
					SCALE	/ - /			
					SHEET	3 OF 6			
					DIST.				

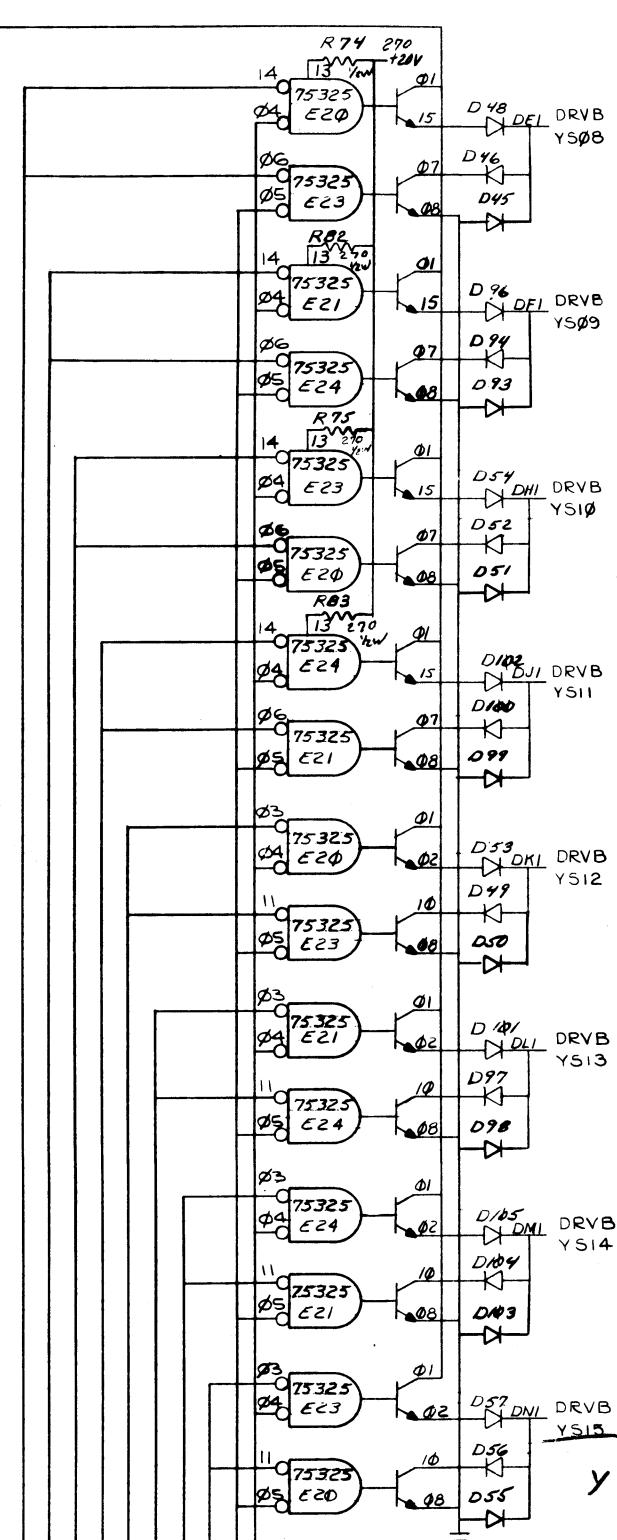
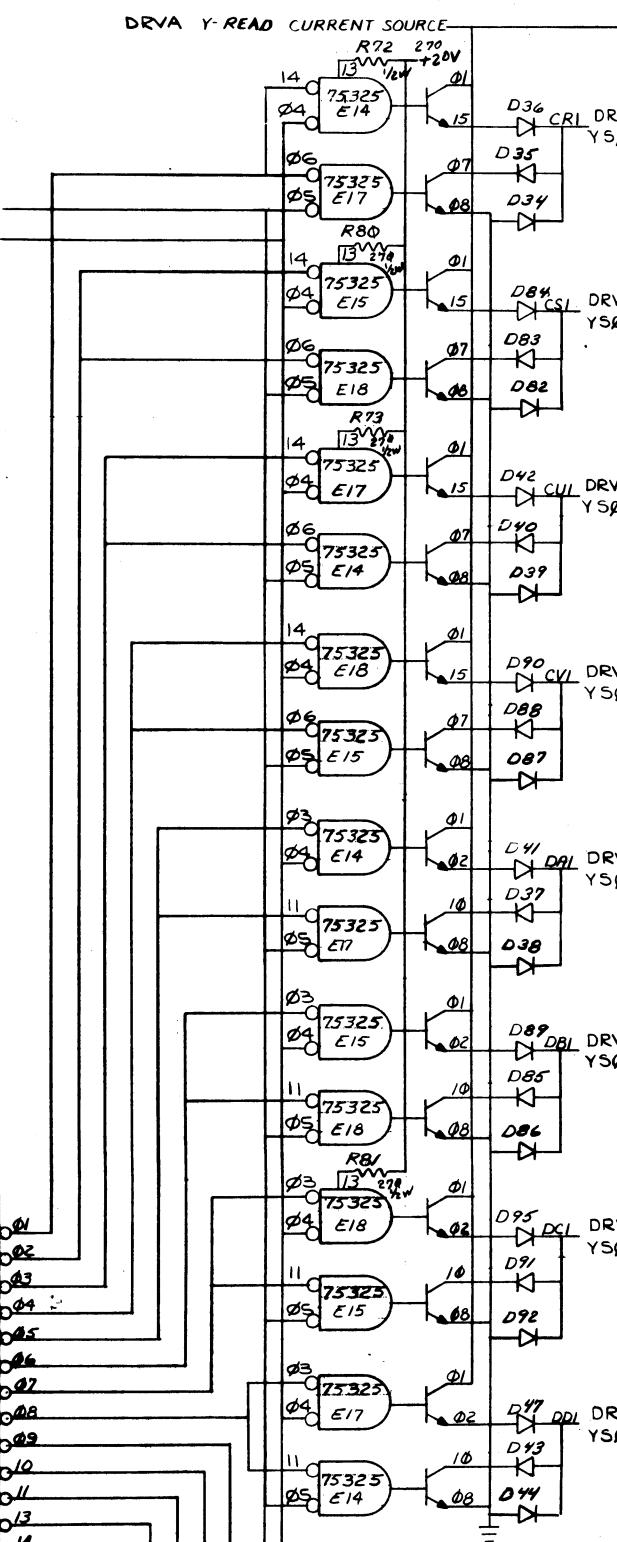
REVISIONS		
CHK	CHANGE NO.	REV



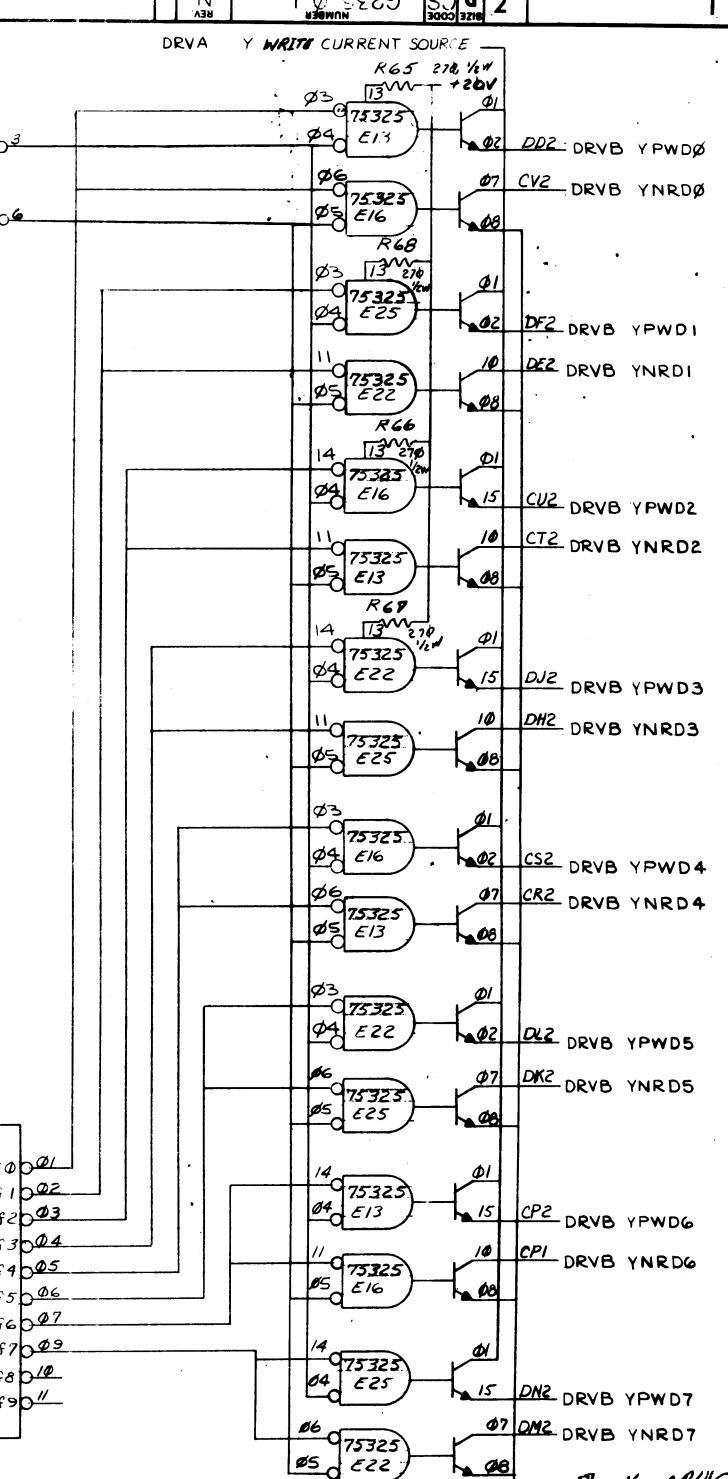
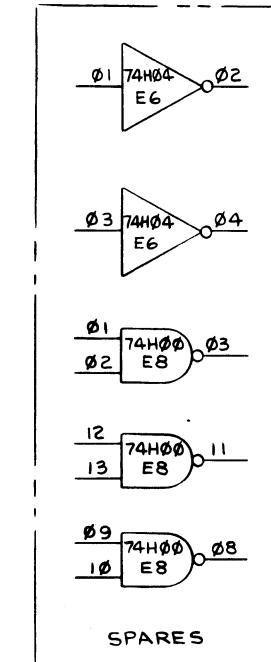
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DRVY Y-WRITE SINK TIME L  
DRVY READ SOURCE TIME L



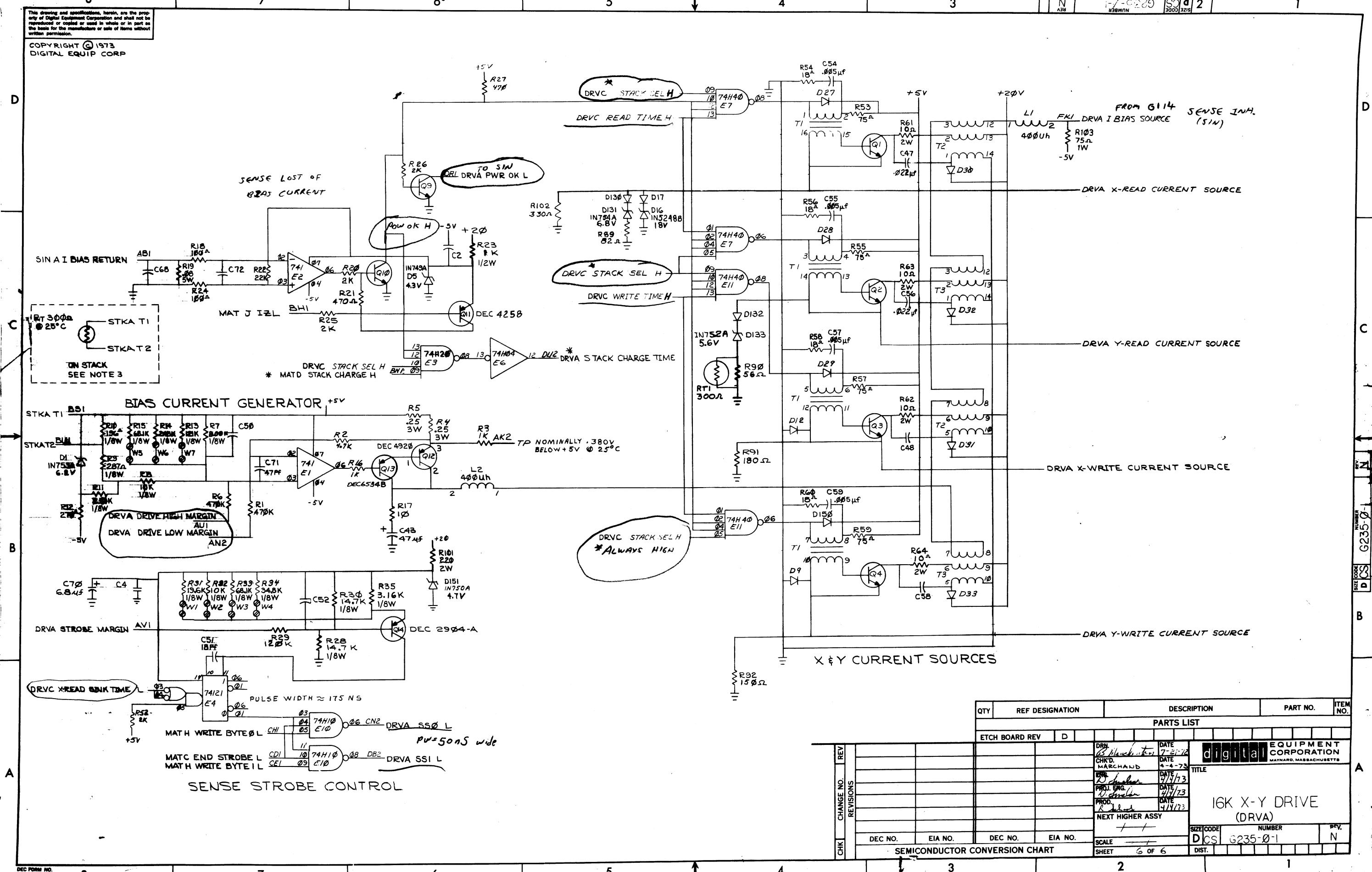
DRVC Y-WRITE SOURCE TIME H  
DRVC READ TIME H



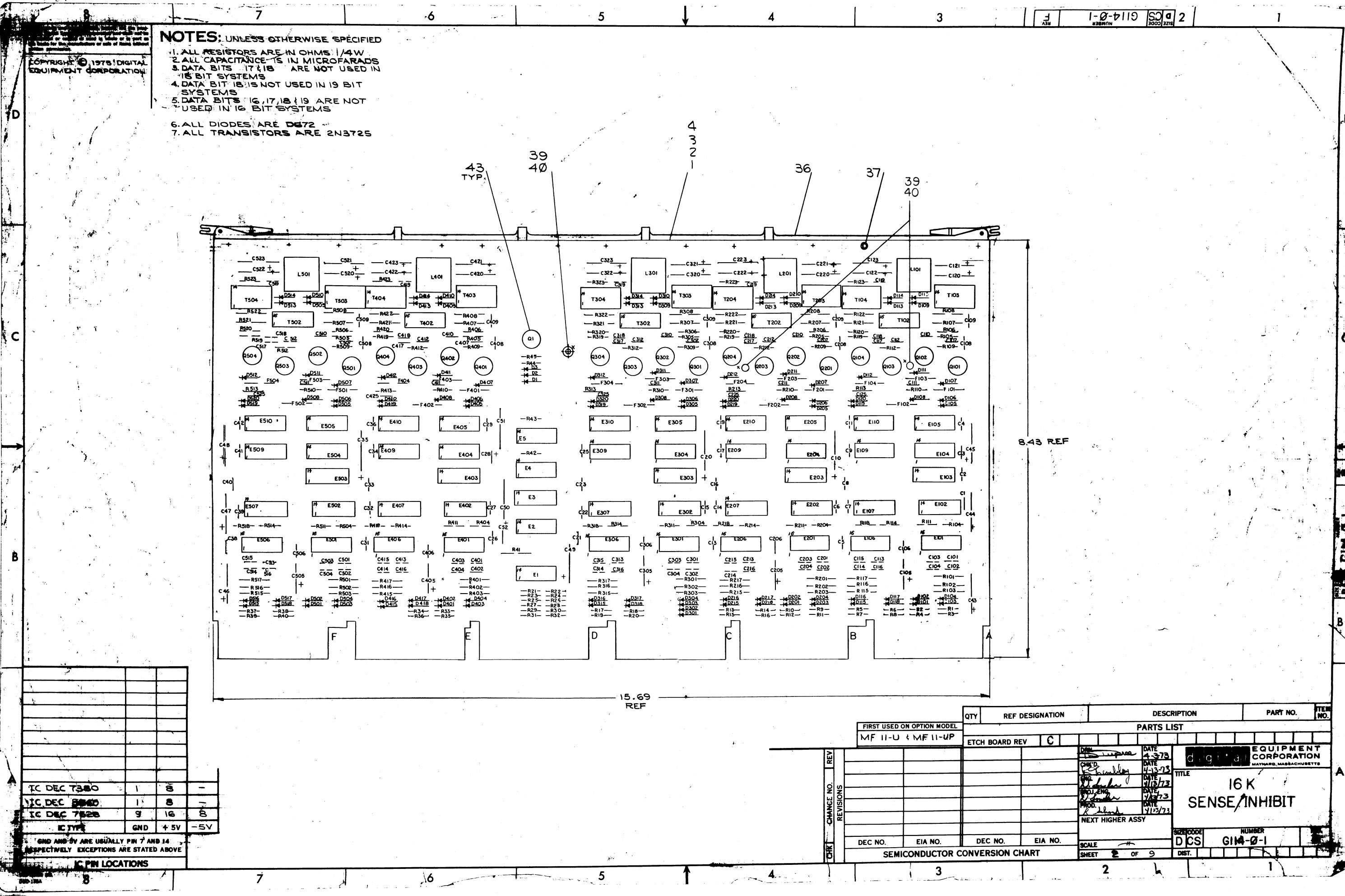
QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST				
ETCH BOARD REV	D			
CHK	CHANGE NO.	REV		
DRVR	Marshall	1/29/73	DATE	
CHK'D.	MARSHALL	4-4-73	DATE	
ENG.	D. Lander	7/1/73	DATE	
PROJ. ENG.	D. Lander	7/1/73	DATE	
PROD.	K. Lander	7/1/73	DATE	
NEXT HIGHER ASSY				
DEC NO.	EIA NO.	DEC NO.	EIA NO.	
SCALE	1/1	SHEET	5 OF 6	
SIZE CODE	D C S	NUMBER	G235-0-1	REV.
DIST.	N			

SEMICONDUCTOR CONVERSION CHART

16K X-Y DRIVE  
(DRVY)



PAGE REVISION CONTROL SHEET



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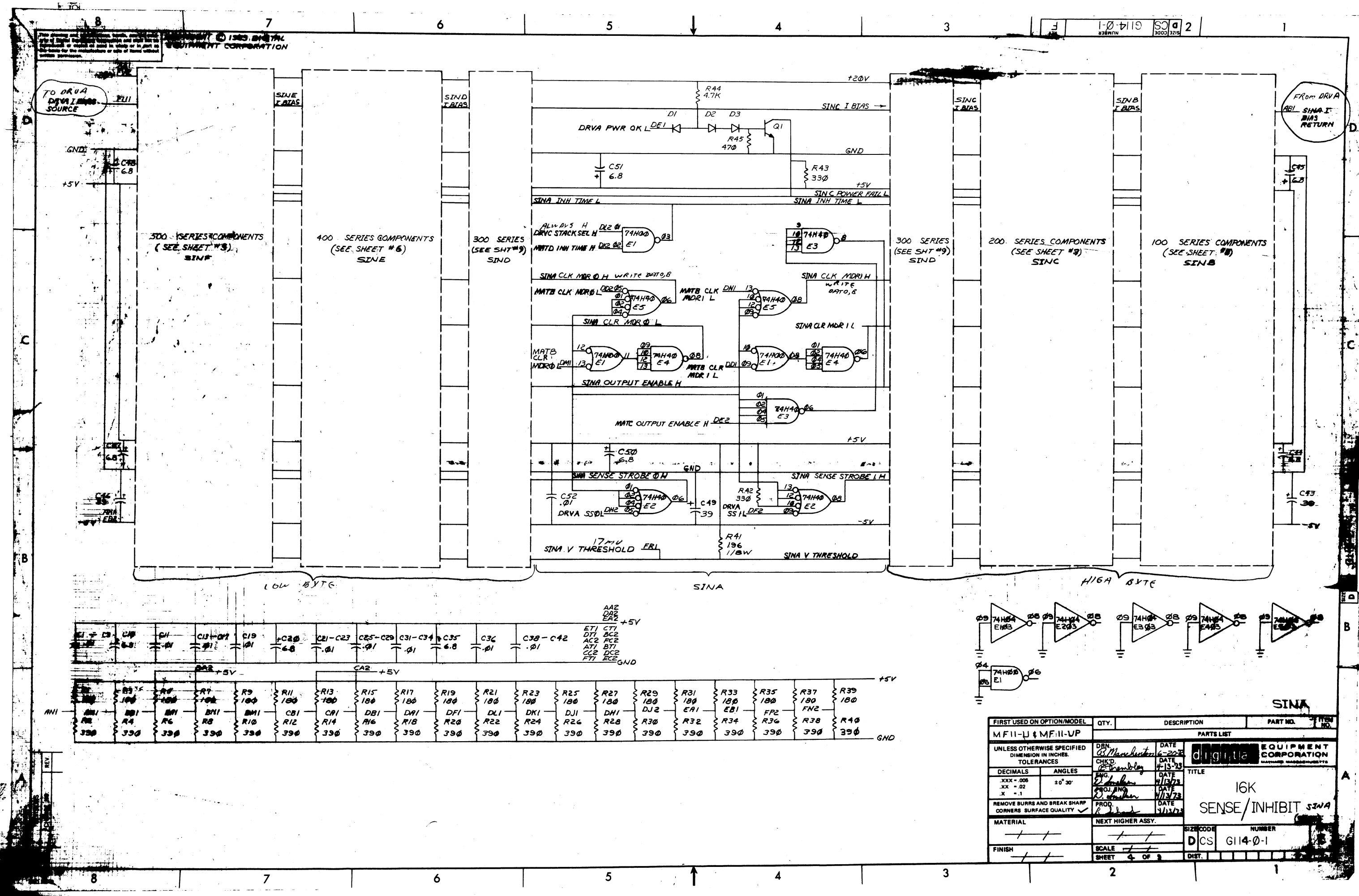
REVISIONS		
CHK	CHANGE NO.	RE

SENSE/INHIBIT DCS GI4-0-1  
SHEET 3 OF 9 DIST.

8  
7  
6  
5  
4  
3  
2  
1

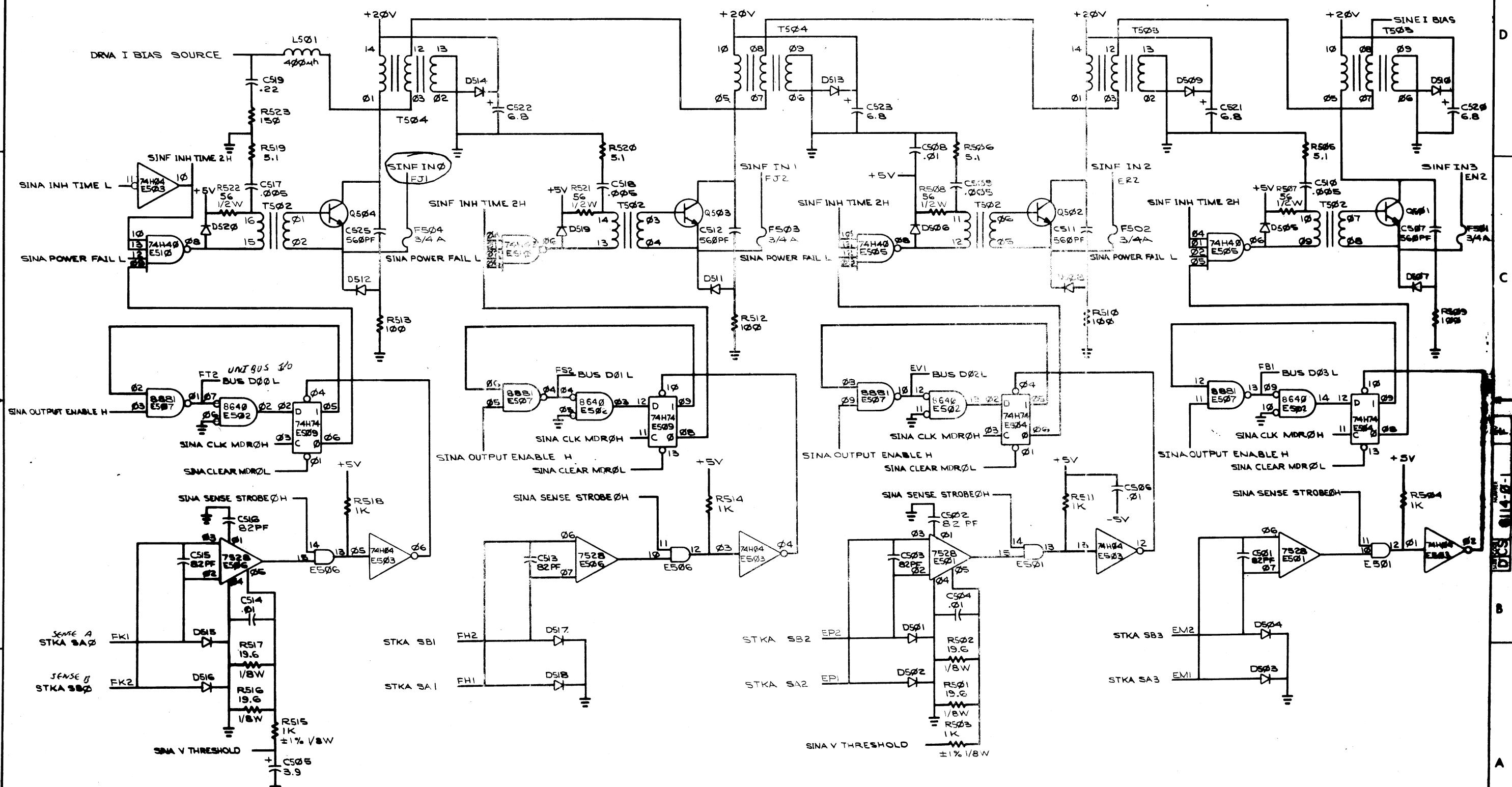
PRINTED ON ONE SIDE OF SHEET ONLY  
PRINTED ON ONE SIDE OF SHEET ONLY

NUMBER 6114-0-1  
CODE 32152000  
D C S G I I 4 - 0 - 1



## 500 SERIES SINF

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE/CODE	NUMBER	REV.
16K SENSE/INHIBIT (SINF)	DCS	G114-0-1	F
SCALE	SHEET	5 OF 9	DIST.

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7

6

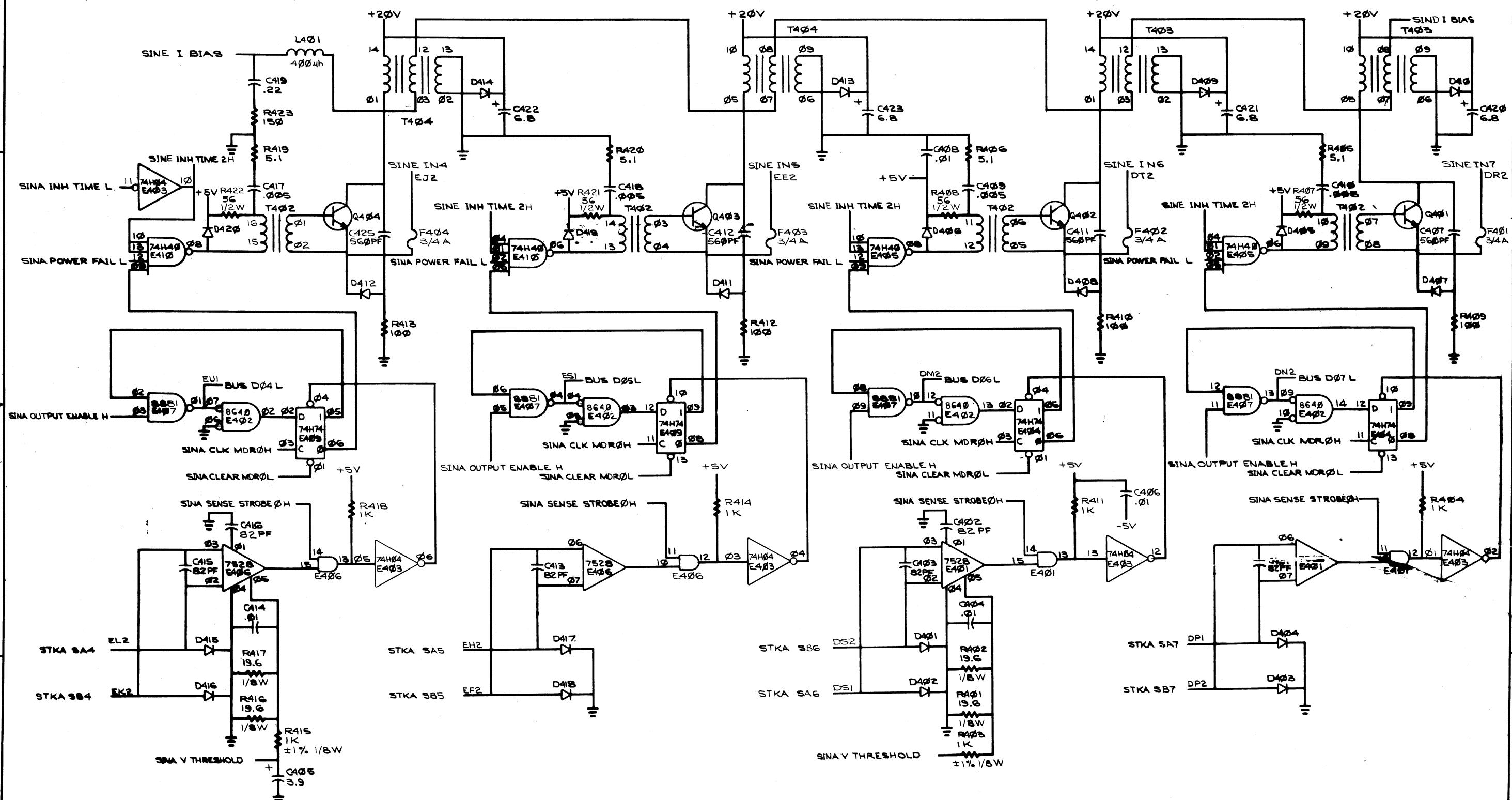
5

4

3

2

1



### 400 SERIES SINE

16K SENSE/INHIBIT (SINE)

DCS G114-0-1

SIZE CODE NUMBER REV.

REV. F

SCALE SHEET 6 OF 9 DIST.

1

REVISIONS		
CHK	CHANGE NO.	REV.

8

7

6

5

4

3

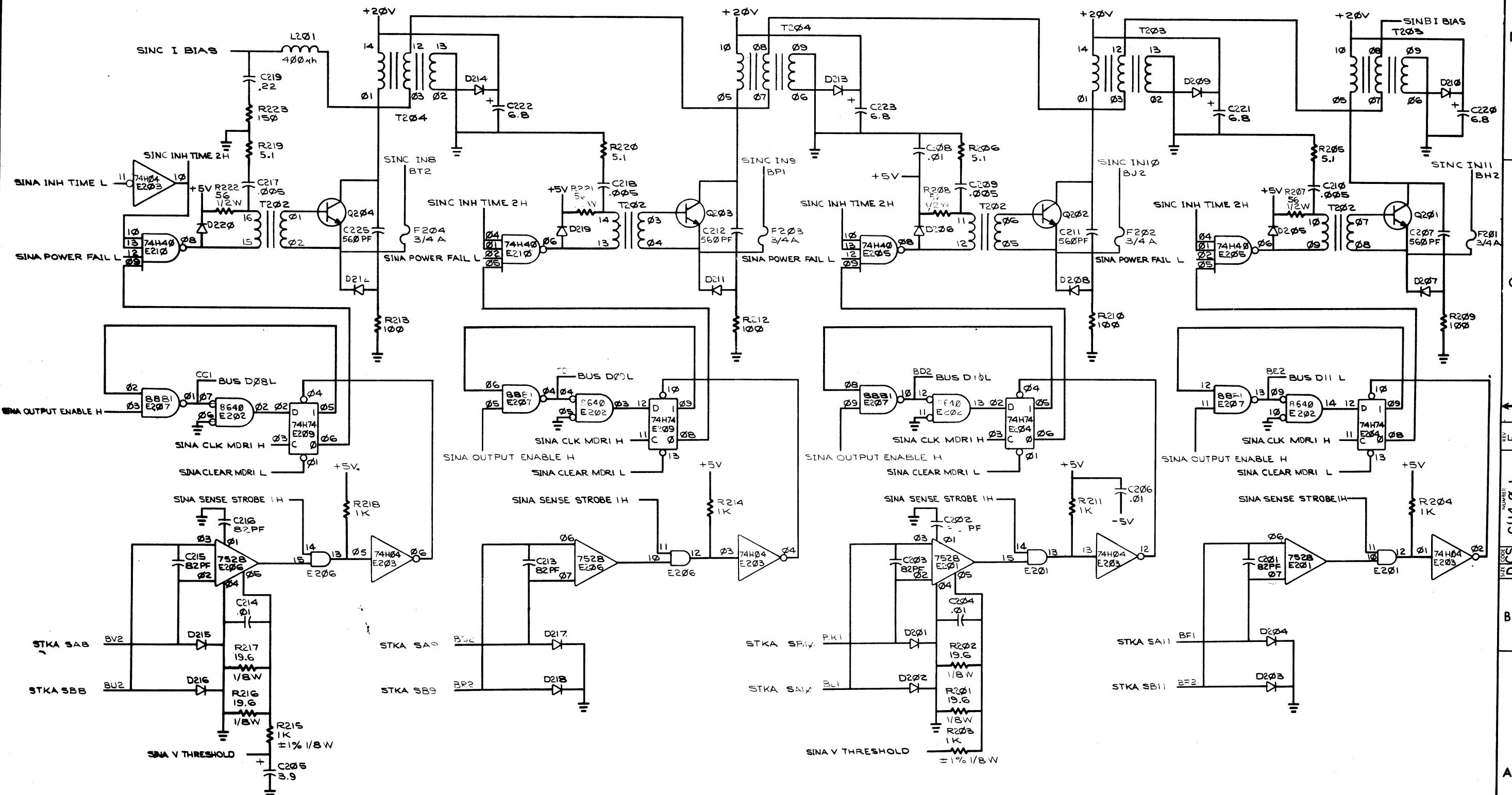
2

1

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7 6 5 4 3 2 1

DCS G114-0-1



REVISIONS	
CHANGE NO.	REV.

200 SERIES SINC

TITLE	16K SENSE/INHIBIT (SINC)	SIZE CODE	DCS	NUM	G114-2
SCALE	↔	SHEET	7	OF	9
DIST.					

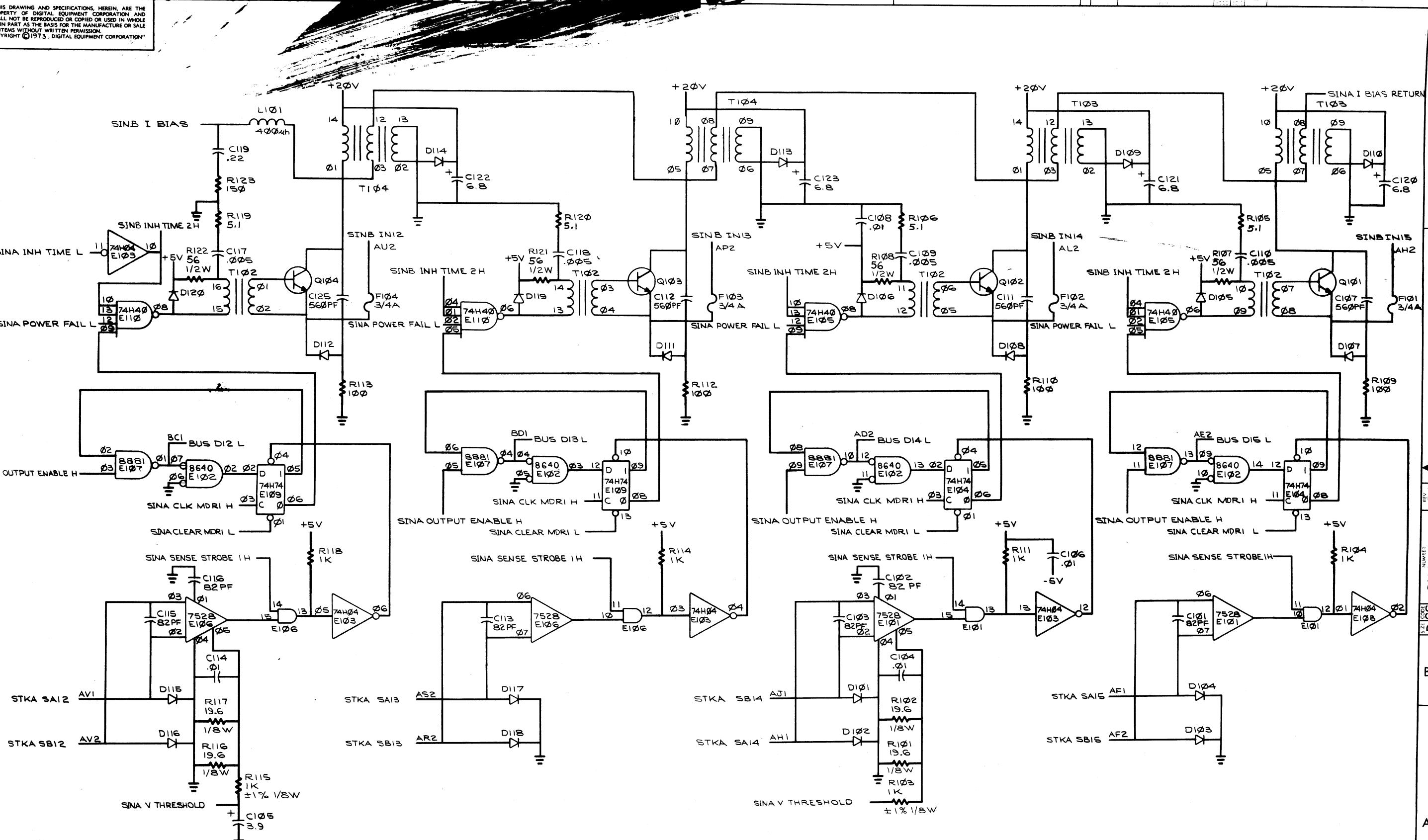
NUMBER: G114-0-1

SIZE CODE: DCS

BLOCK: B

A

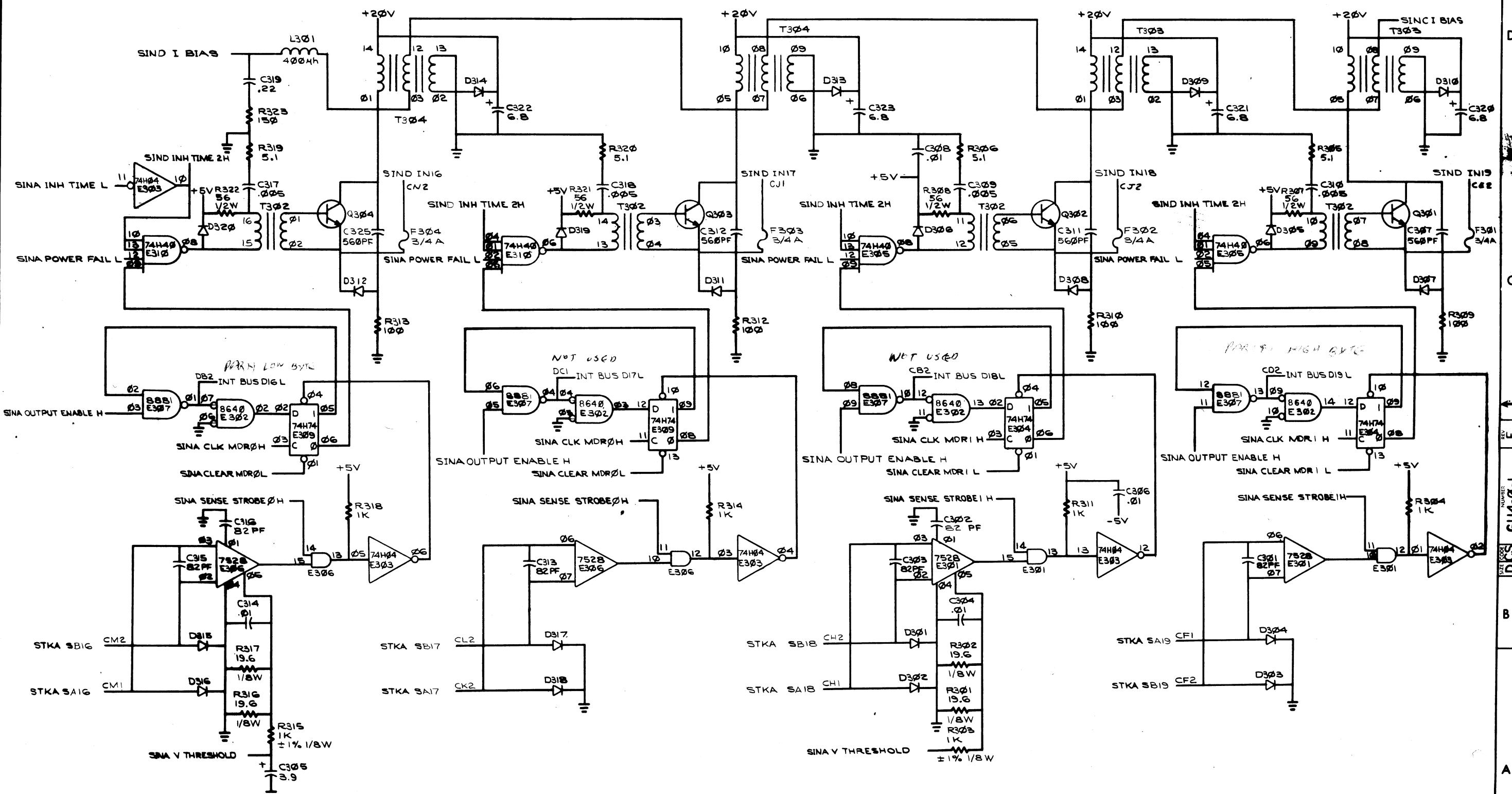
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
16K SENSE/INHIBIT (SINB)	DCS	G114-0-1		F
SCALE	SHEET	8 OF 9	DIST.	

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**REVISIONS**

ODD PARITY

## 300 SERIES SIND

TITLE <b>16K SENSE/INHIBIT (SIND)</b>	SIZE CODE <b>D CS</b>	NUMBER <b>G114-0-1</b>	REF <b>F</b>
SCALE <b>—</b>	SHEET <b>9</b> OF <b>9</b>	DIST.	

8                    7                    6                    5                    4                    3                    2

## NOTES

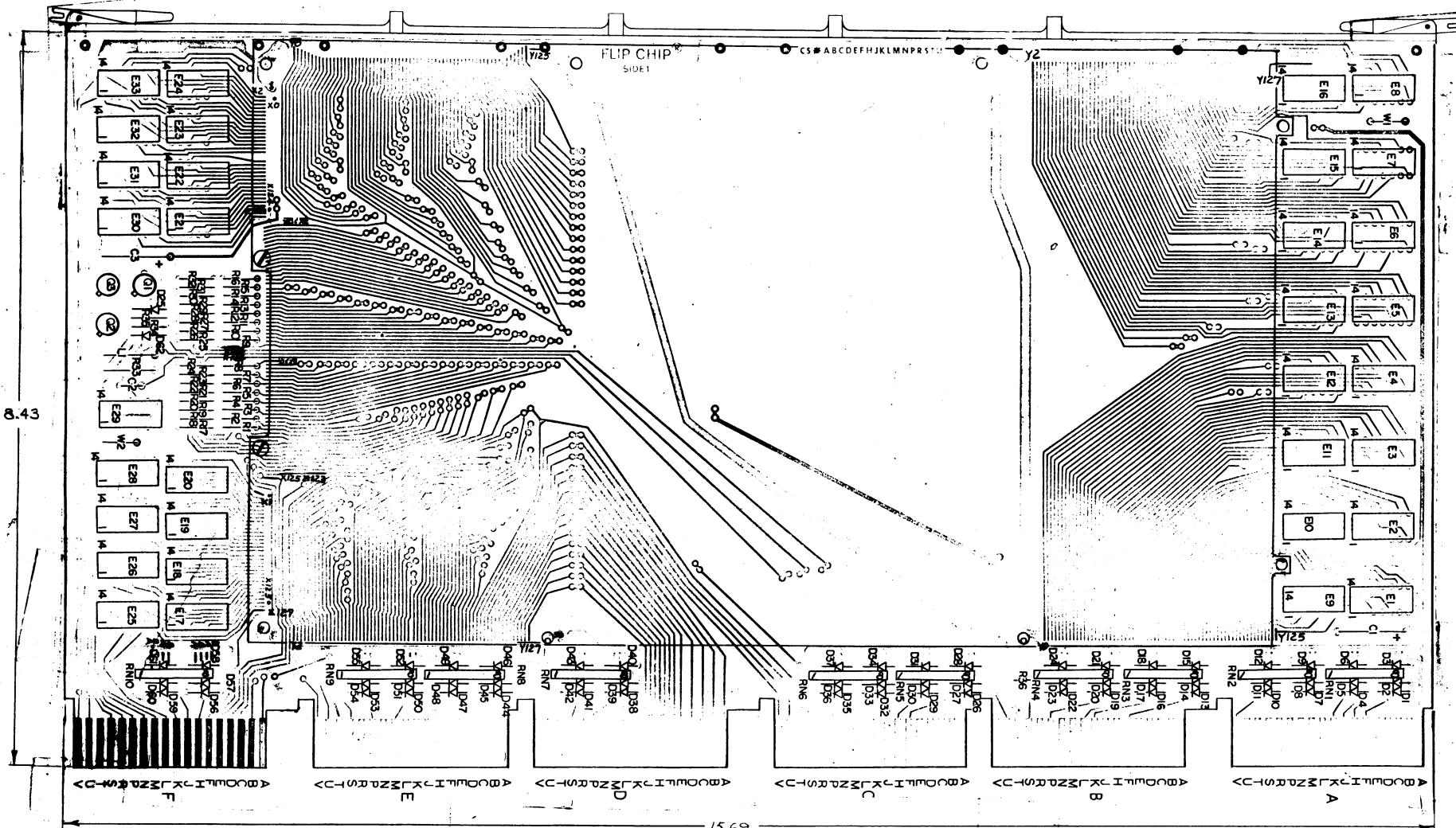
- NOTES:**

1. — X0 THRU X127 — & — Y0 THRU Y127 —  
INDICATES MAGNET WIRE TERMINATION  
(SOLDERED TO PRINTED CIRCUIT PAD).

2. FOR ASSEMBLY INFORMATION & PART NO'S.  
OF ITEMS NOT CALLED OUT ON THIS DRAWING  
REFER TO E-AD-9305680-0-0 (MEMORY  
STACK ASSY).

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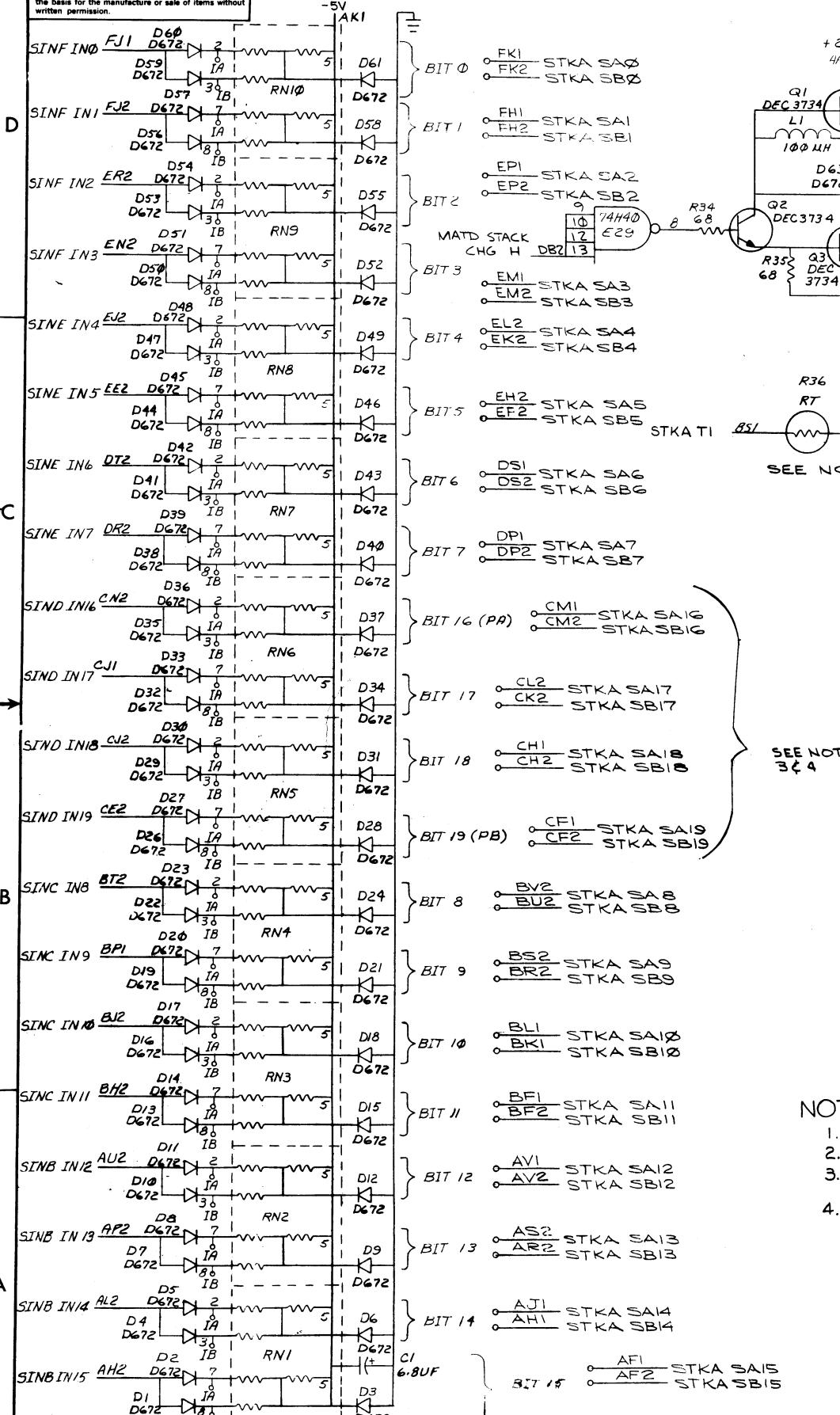
NUMBER	DEC	REFND PURCHASE SPEC.	DEC	PART NO.	STACK CONFIGURATION
9305680-1				H217-A	16K X 20
9305680-2				H217-B	16K X 19
9305680-3				H217-C	16K X 18
9305680-4				H217-D	16K X 16



	DEC 2501	N/A	N/A
A			
IC TYPE	GND	+ 5V	
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE			
IC PIN LOCATIONS			
SEARCHING 40-022 100000	8		
DEC FORM NO.			
DRD-135A			

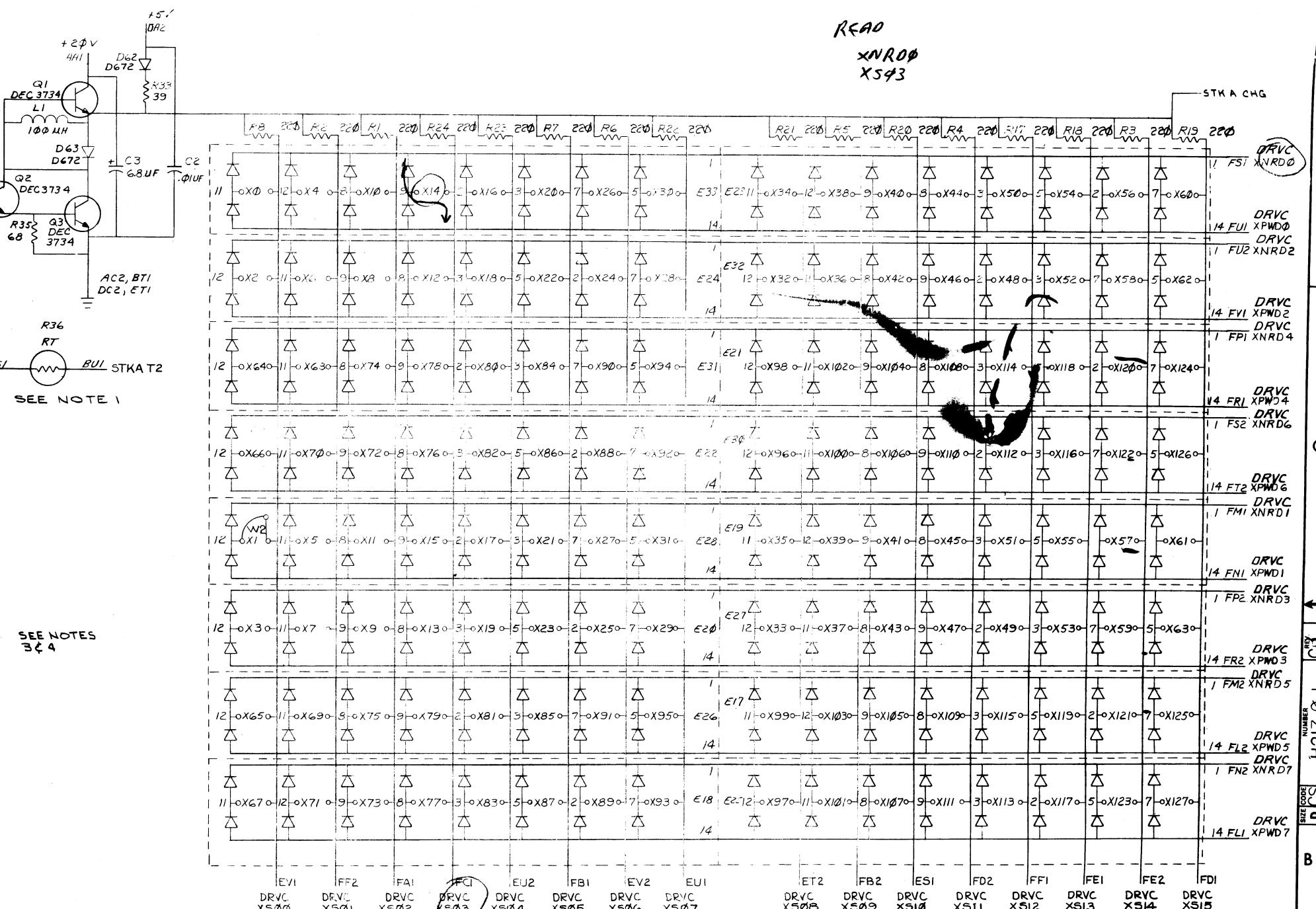
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### NOTES:

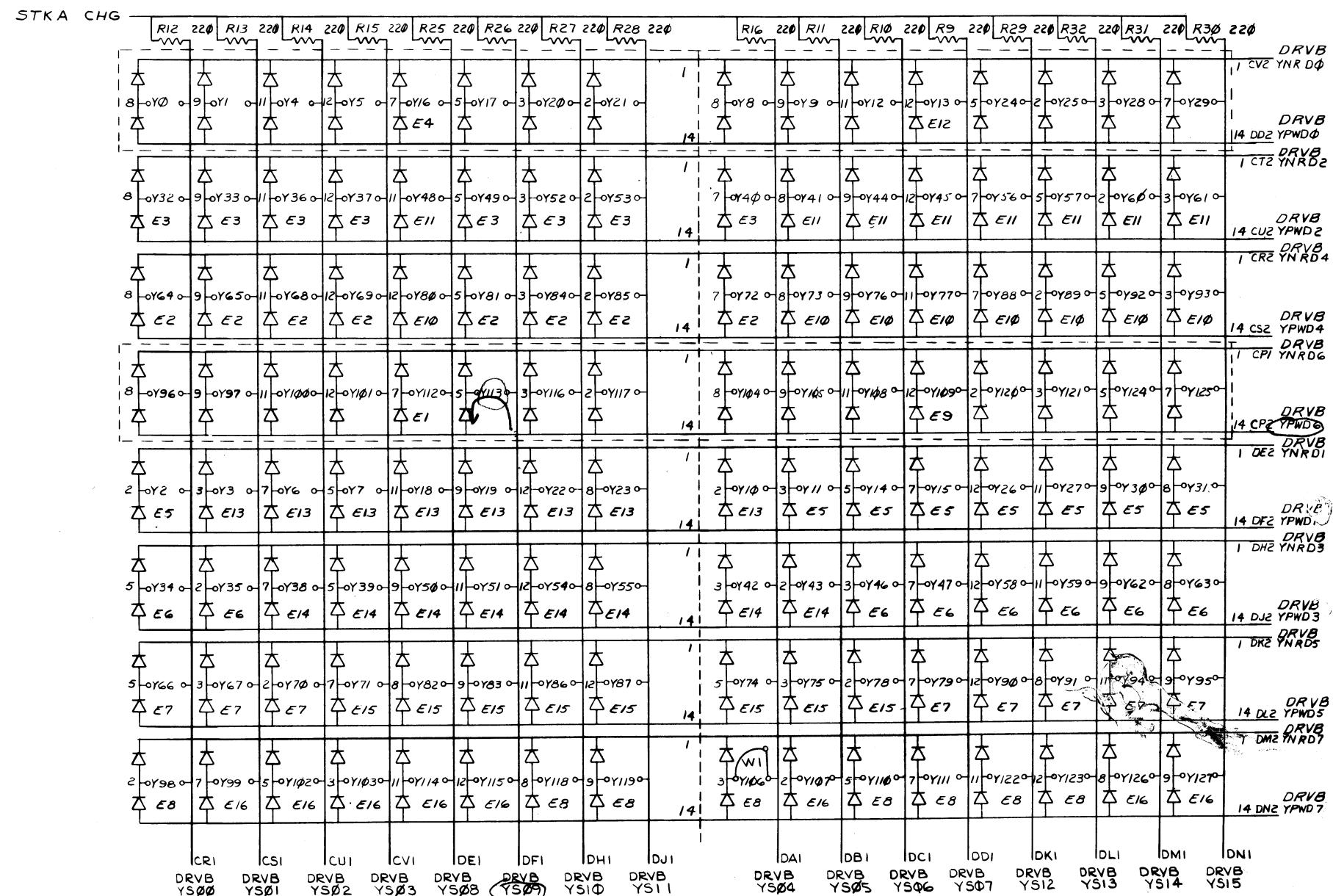
1. THERMISTOR FOR TEMPERATURE COMPENSATION
2. JUMPER W2 IS A CURRENT LOOP FOR TEST USE ONLY
3. FOR H217-D (16 BIT STACK) THE FOLLOWING COMPONENTS MUST BE DELETED; RN5, RNG, D2G THRU D37
4. FOR H217C (18 BIT STACK) THE FOLLOWING COMPONENTS MUST BE DELETED; D29, D30, D32, D33. FOR THE UNUSED BITS, THE FOUR MAGNET WIRE TERMINATION PADS (IA, IB, SA, SB) MUST BE SHORTED TOGETHER
- FOR H217B (19 BIT STACK) THE FOLLOWING COMPONENTS MUST BE DELETED; D29, D30. FOR THE UNUSED BIT THE FOUR MAGNET WIRE TERMINATION PADS (IA, IB, SA, SB) MUST BE SHORTED TOGETHER



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WHITE  
YRN06 YII-  
Y509



NOTE: JUMPER WI IS A CURRENT LOOP  
FOR TEST USE ONLY

FOR TEST USE ONLY

8721285 mem 0100

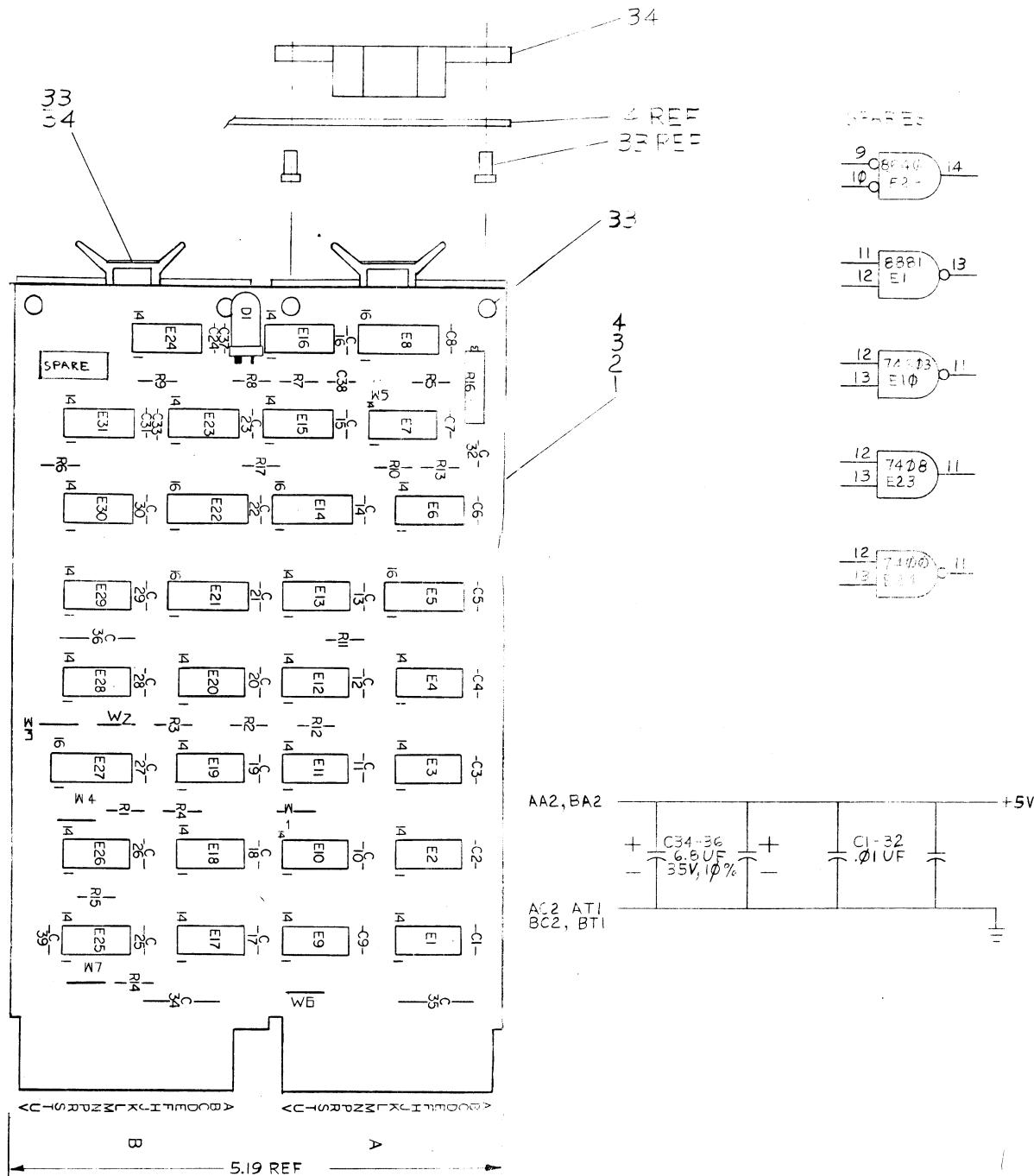
MF 11-01 UP  
EE Page 2-8

		QTY	REF DESIGNATION	DESCRIPTION		PART NO.	ITEM NO.
PARTS LIST							
	REV	ETCH BOARD REV	E				
CHCK	CHANGE NO.			DBN <i>B. Marchant</i>	DATE 7-10-72		
	REVISIONS			CMND <i>S. P. Belo</i>	DATE 2/10/73		
				ENCL <i>R. Marchant</i>	DATE 1/10/73		
				PROJ. ENG. <i>A. Marchant</i>	DATE 1/10/73		
				PROG. <i>J. Allegreto</i>	DATE 5/16/73		
				NEXT HIGHER ASSY		STACK BOARD (STKB)	
				<i>11</i>		SIZE D	CODE ICS
		DEC NO.	EIA NO.	DEC NO.	EIA NO.	NUMBER H217-0-1	REV. C
		SEMICONDUCTOR CONVERSION CHART		SCALE <i>11</i>	SHEET 3 OF 3	DIST.	

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## NOTES:

1. UNLESS OTHERWISE SPECIFIED:  
RESISTORS ARE 1/4 W, 5%  
CAPACITORS ARE 100V, 20%
2. JUMPERS CONTROL OPERATIONS  
AS FOLLOWS:  
W1-W4 SELECT CSR ADDRESS  
W5 CAPACITOR FOR SSYN DLY;  
NEVER USED  
W6 OUT FOR MFII-LP  
IN FOR MFII-UP  
W7 OUT TO HANG BUS ON PARITY  
ERROR.
3. DEC 8640 REPLACES THE  
OBSCURE DEC 380.

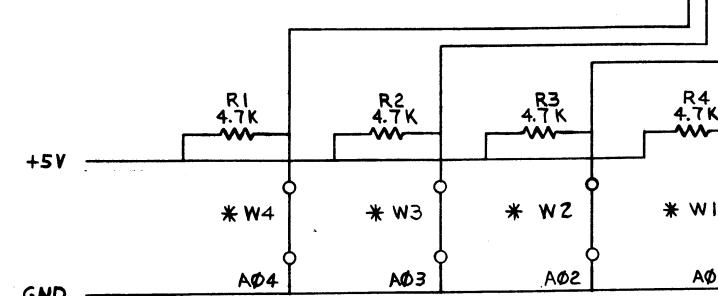
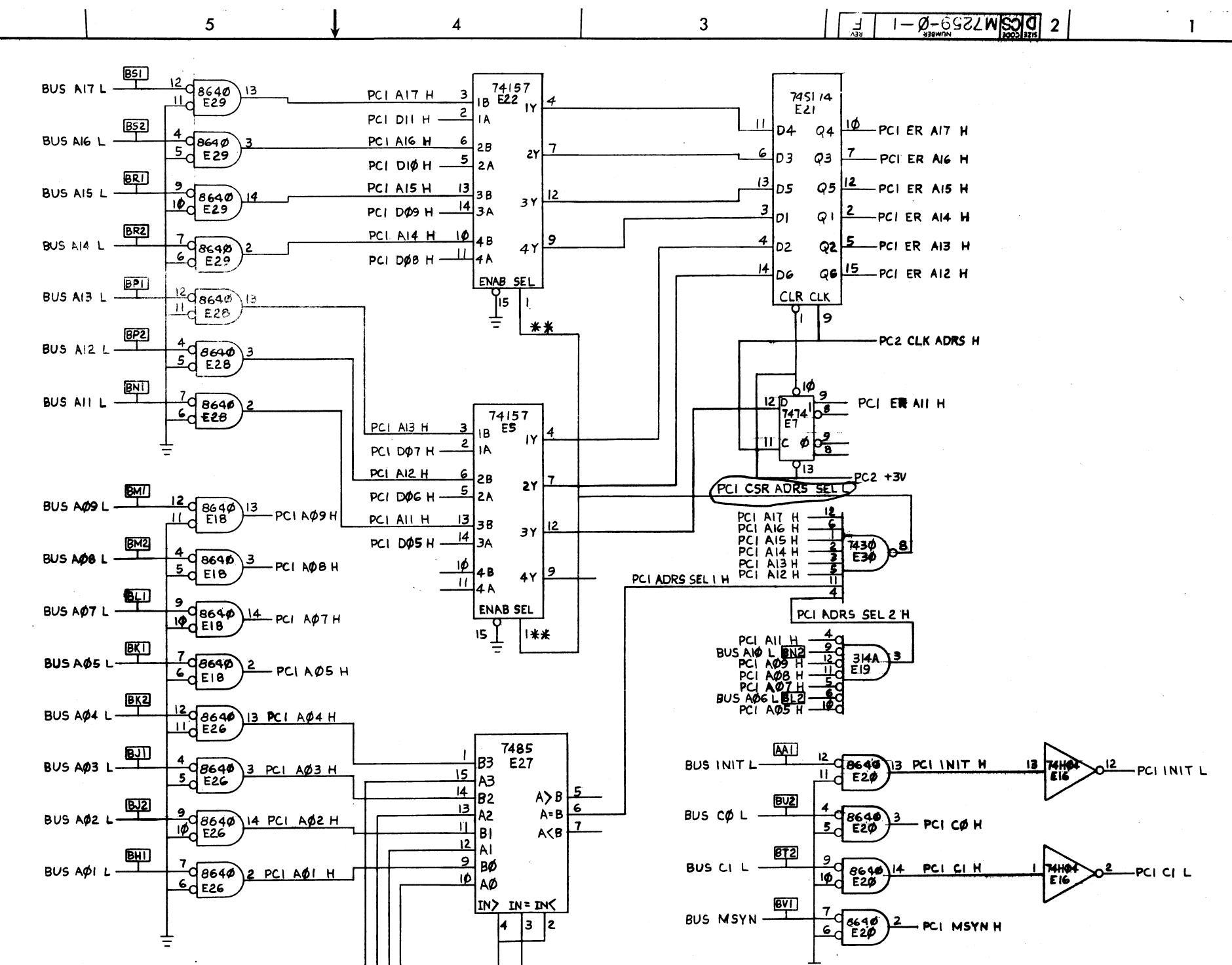
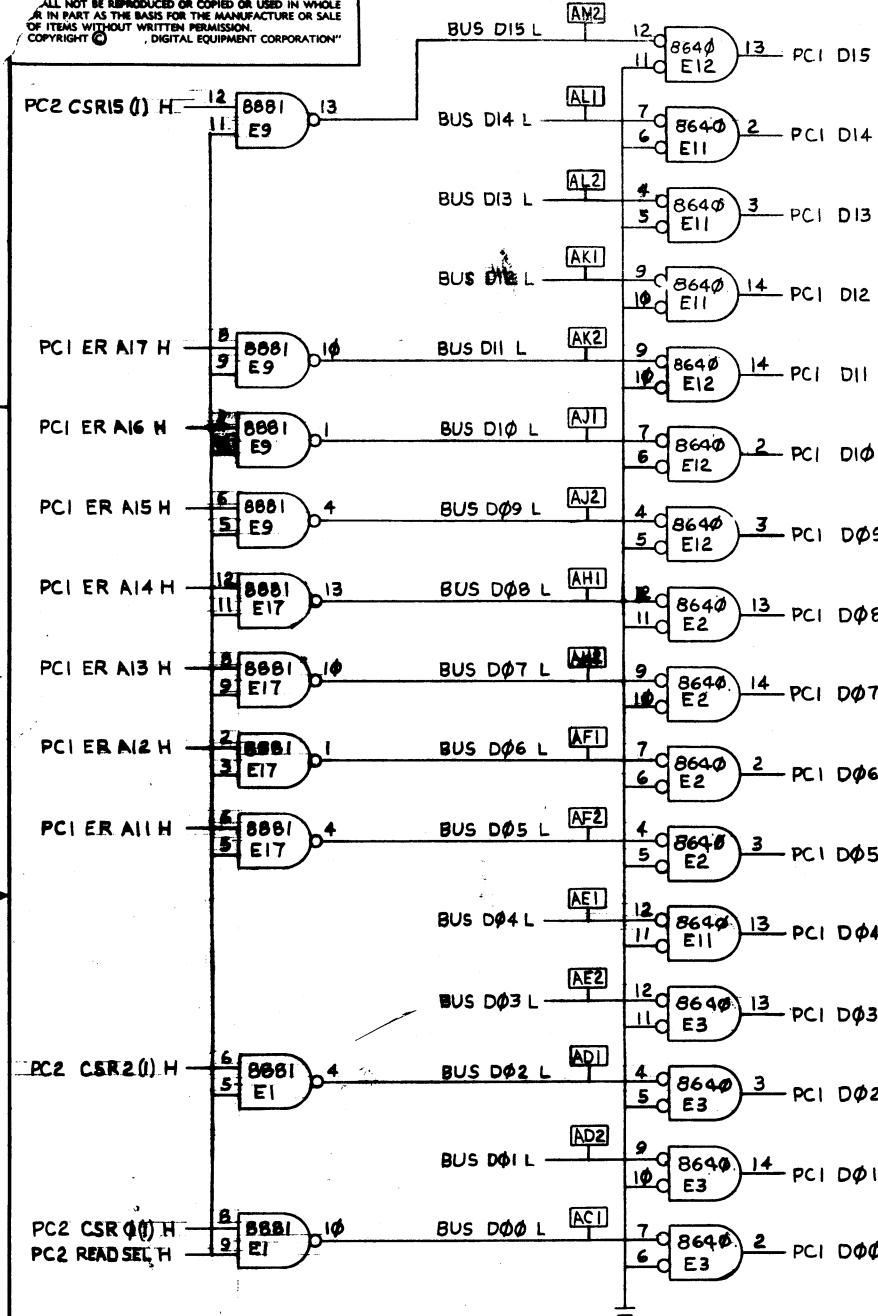


REF	X-Y COORDINATE HOLE LOCATION	K-CO-M7259-0-4
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M7259-0-5
REF	MODULE ECO HISTORY	B-MH-M7259-0-6
1	ETCHED CKT. BD.	5010314
1	C39	CAP 470 PF., 100V 5% D.M.
2	C33, C37	CAP 330 PF., 100V 5% DM
32	C1-C32	CAP .01UF., 100V 20% DISC
3	C34, C35, C36	CAP 6.8UF 35V 10% S.TA
1	C38	CAP 220PF, 100V, 5% DM
3	R8, R9, R15	RES 100Ω, 1W, 5%
6	R1-R4, R7, R14	RES 4.7K, 1W, 5%
5	R6, R10, R11, R12, R17	RES 470Ω, 1W, 5%
1	R13	RES 1K, 1W, 5%
1	R16	RES 20K 3/AW 1% 76 P.R. POT
1	E24	IC DEC 7400
1	E30	IC DEC 7436
1	E31	IC DEC 74B2
1	E13	IC DEC 314A
1	E2	IC DEC 7408
4	E1, E9, E17, E25	IC DEC 8881
1	E16	IC DEC 74H4
1	E27	IC DEC 7485
1	E8	IC DEC 74123
1	E10	IC DEC 74S13
1	E15	IC DEC 74S74
1	E21	IC DEC 74S174
2	E5, E22	IC DEC 74157
9	E2, E3, E11, E12, E18, E21, E26, E28	IC DEC 8640
2	E4, E13	DEC 82082
1	E14	IC DEC 8266
2	E6, E7	IC DEC 7474
6	W1-W4, W7, W6	JUMPER, INSULATED SETTING ENG L-2007-1
4		EYELET (GS-4-7)
2		HANDLE, FLIP CHIP (MAGENTA)
1	R5	RES 5.6K, 1/4 W, 5%
1	D1	LIGHT EMITTING DIODE

ITEM NO.	PART NO.	DESCRIPTION	QTY	REF DESIGNATION
PARTS LIST				
	DRN. M. PIERCE	DATE 12/16/72		
	CHK'D. K. GLEEZEN	DATE 1/17/73		
	ENG. M.	DATE 1/16/73		
	PROJ. ENG. M.	DATE 1/23/73		
	PROD. C.	DATE 1/24/73		
	NEXT HIGHER ASSY B-DD-MFII-LP			
	SCALE NONE			
	SHEET 1 OF 1			
	DIST.			

IC PIN LOCATIONS		
IC DEC 8640	1	8
IC DEC 8266	8	16
IC DEC 74123	8	16
IC DEC 74174	8	16
IC DEC 74157	8	16
IC DEC 7485	8	16
IC DEC 314A	1	8
IC TYPE	GND	+ 5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE		

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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	PARITY CONTROL-MFI-LP(PCI)	SIZE CODE	D	NUMBER	F
SCALE	NONE	SHEET	2	OF	3
DIST.					

SIZE CODE  
D  
NUMBER  
DCSM7259-0-1

REV.

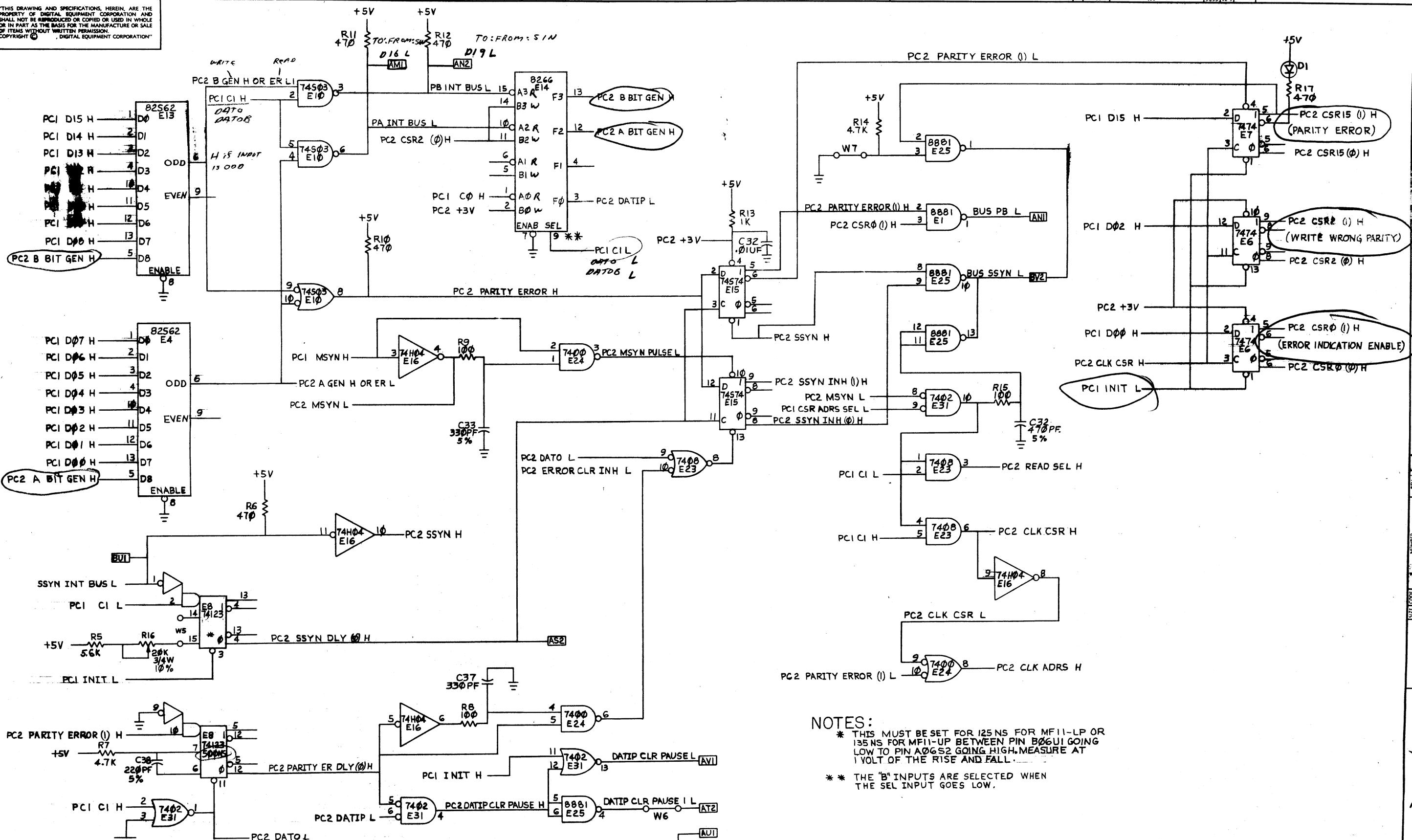
1

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#### NOTES:

\* THIS MUST BE SET FOR 125 NS FOR MFII-LP OR 135 NS FOR MFII-UP BETWEEN PIN B06UI GOING LOW TO PIN A06S2 GOING HIGH. MEASURE AT 1 VOLT OF THE RISE AND FALL.

\*\* THE 'B' INPUTS ARE SELECTED WHEN THE SEL INPUT GOES LOW.

REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. 100-104  
REV. D

TITLE: PARITY CONTROL-MFI-LP (PC2)  
SIZE CODE: D CS M7259-0-1  
NUMBER: F  
REV: E

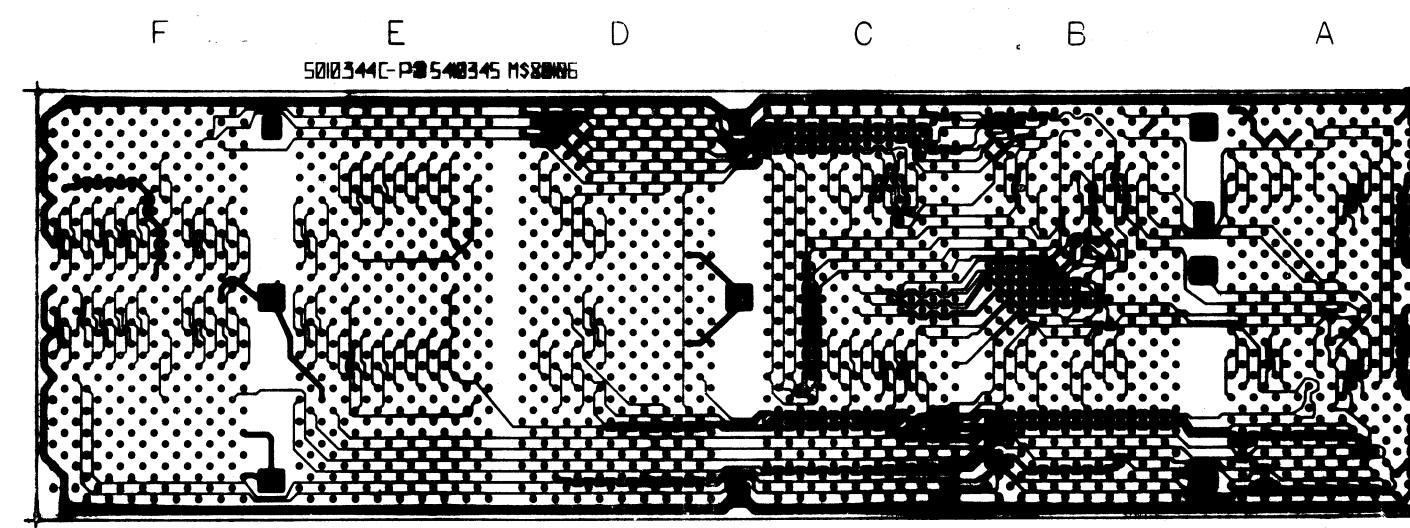
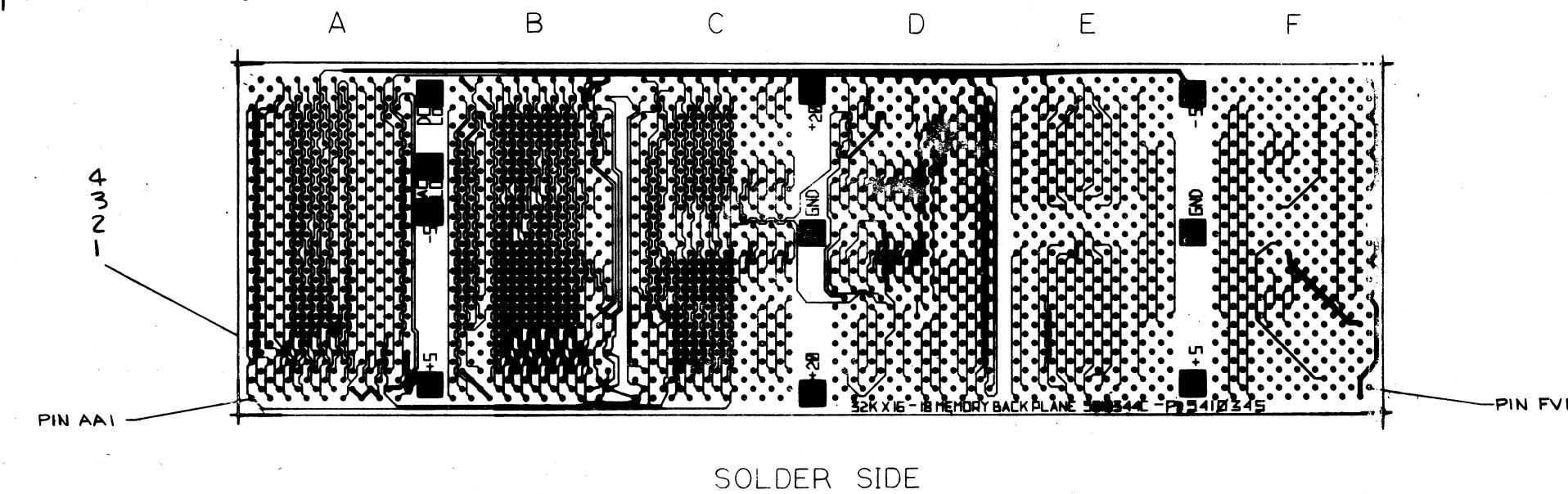
SCALE: NONE SHEET 3 OF 3 DIST. 1

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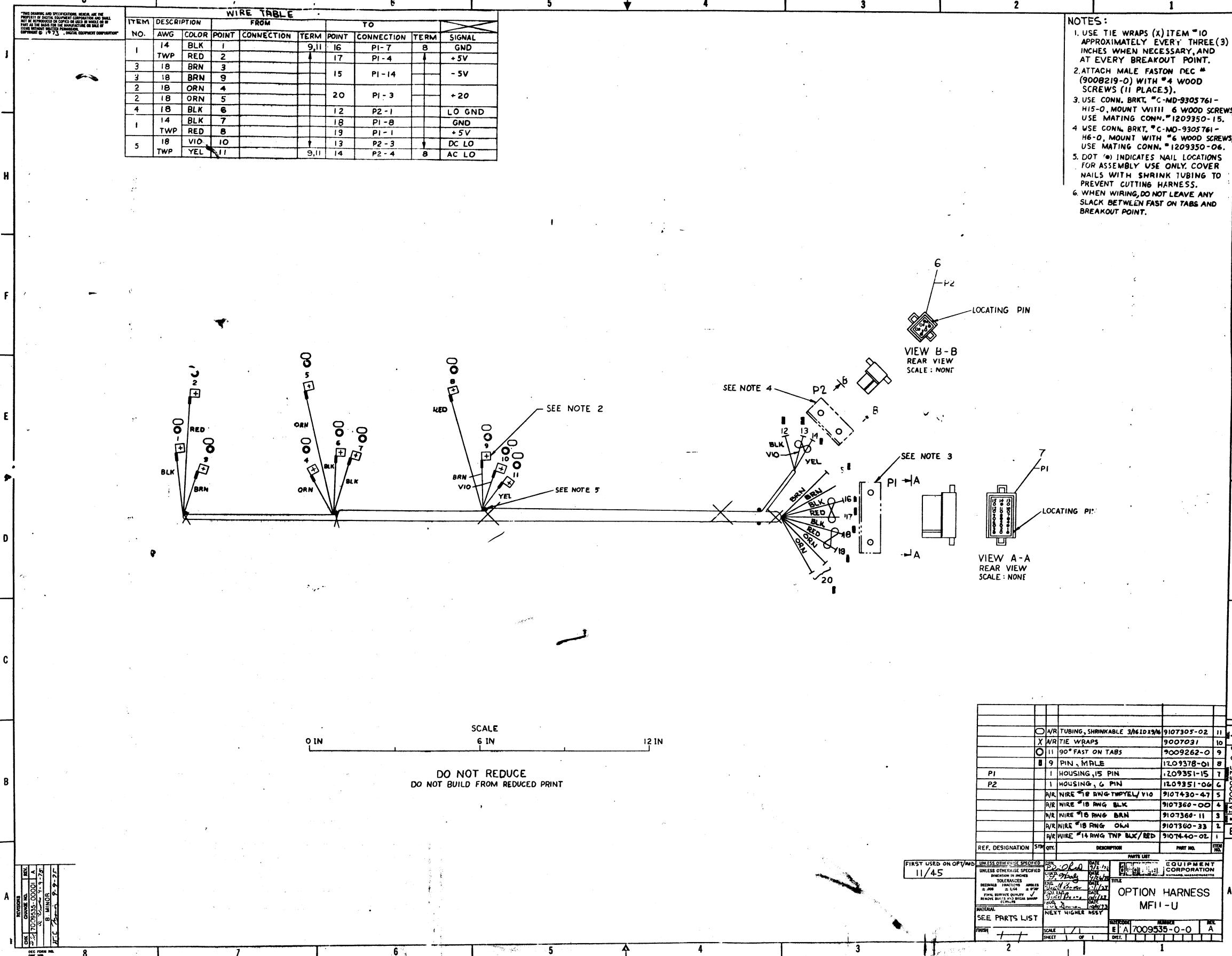
1. THIS IS A MULTILAYER BOARD
2. +5V PINS AA2, BA2, CA2, DA2, EA2, FA2 ARE CONNECTED TOGETHER THROUGH LAYER 3.
3. GND PINS AC2, AT1, BC2, BT1, CC2, CT1, DC2, DT1, FC2, ET1, FC2, FT1, ARE CONNECTED TOGETHER THROUGH LAYER 2



FIRST USED ON OPTION MODEL		PARTS LIST	
MM11-U	ETCH BOARD REV	C	
D-SMELSER 2/3/75	DRN W/Major	DATE 1/20/73	EQUIPMENT CORPORATION
D-SMELSER 2/3/75	CHK'D. W/Major	DATE 1/20/73	MAYNARD, MASSACHUSETTS
P. DURANT 9-1-73	ENG. J. Anderson	DATE 1/20/73	TITLE
P. DURANT 9-1-73	PROD. J. Schell	DATE 1/20/73	32K X 16-18
5410345-00001 B	NEXT HIGHER ASSY	D-AD-7009295-0-0	MEMORY BACK PLANE
CHG. NO. REV			
5410345-00001 B	DEC NO.	EIA NO.	SIZE CODE
CHG. NO. REV	DEC NO.	EIA NO.	NUMBER
			D 5410345-0-1
			C
		SCALE /	
		SHEET 1 OF 1	
		DIST. 1	

SEMICONDUCTOR CONVERSION CHART

IC TYPE	GND	+ 5V
GND AND BV ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		



**DIGITAL EQUIPMENT CORPORATION**  
**MAYNARD, MASSACHUSETTS**  
**PARTS LIST**

MADE BY W. MAJOR  
DATE 5/11/73  
ENG  
DATE 5/11/73

**CHECKED**  **MAILED**

SECTION

DATE 5/11/73  
ENG *D. Smoker*  
DATE 5

DATE	5/11/73
PROD	
DATE	8/2/73

ISSUED SEC  
13/73 1

ITEM NO.	DWG NO./ PART NO.	DESCRIPTION	M	M	M	M	M	M	M	
			F	M	M	M	M	M	M	
1	D-CS-G114-0-1	16K SENSE INHIBIT	1	1	1	1	2	4	2	4
2	D-CS-G235-0-1	16K X-Y DRIVE	1	1	1	1	2	4	2	4
3	D-CS-M8293-0-1	16K UNIBUS TIMING	1	1	1	1	2	4	2	4
4	D-AD-7009295-1	BACK PLANE ASSY	1	-	-	-	1	2	-	-
5	D-CS-H217-D-1 *	MEMORY STACK (16K X 16)	1	1	-	-	2	4	-	-
6	D-CS-H217-C-1 *	MEMORY STACK (16K X 18)	-	-	1	1	-	-	2	4
7	D-AD-7009295-2	BACK PLANE ASSY	-	-	1	-	-	+1	1	2
REF	D-MU-MF11-U-MU	MODULE UTILIZATION								
8	D-CS-M7259-0-1	Parity( SAME AS MF11-LP)	-	-	1	-	-	-	1	2
9	E-IA-7009535-0-0	OPTION HARNESS	1	-	1	-	1	2	1	2
10	D-IA-7010167-0-0	SUPPORT HARNESS	1	-	1	-	1	2	1	2
11	9006037-1	SCR PHIL PAN HD 8-32 + 3/8	4	-	4	-	4	8	4	8
12	9008072	EXTERNAL TOOTH LOCK WASHER #8	4	-	4	-	4	8	4	8
13	D-CS-H217-B-1 *	MEMORY STACK (16K X 19)								
*	THE H217B MAY BE SUBSTITUTED FOR THE H217C OR H217D AND THE H217C MAY BE SUBSTITUTED FOR THE H217D IN NON PARITY SYSTEMS									
TITLE	16K SENSE MEMORY	ASSY NO. D-UAMF11-U-0	SIZE	CODE	NUMBER			REV.	ECO NO.	
			A	PL	MF11-U-0			B	MU- 60005	
		SHEET 1 OF 1			DIST.					

**DEC FORM DEC 16-(325)-1031-N870  
DRA 110**

ASSY NO.  
D-~~UA~~MFII-U-O

SHEET 1 OF 1

**SIZE COD**

DIST.

**NUMBER**  
**MF11-U-8**

— — —

**REV. B** **ECO NO.** **MTRU-  
68887**

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DIGITAL EQUIPMENT CORPORATION  
MAYNARD, MASSACHUSETTS

DATE 9/7/73

TITLE MF11-U/UP CUSTOMER ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG *P. Durant*

APPD *J. Sharrow* 12-5-73

SIZE  
A  
SP

CODE  
NUMBER  
MF11-U-3

REV

DEC FORM NO.  
DRA 107A

SHEET 1 OF 2

ENGINEERING SPECIFICATION

CONTINUATION SHEET

TITLE MF11-U/UP CUSTOMER ACCEPTANCE PROCEDURE

1.0 Overview

- 1.1 This procedure contains directions pertaining to field assurance of the correct operation of an MF11-U/UP.
- 1.2 Prior to this acceptance, the option will have been installed, inspected, and connected and have power applied. Generally the memories shipped as add ons will have been configured and tested at the factory with their addresses beginning at 000000. Prior to running diagnostics, these memories must be re-configured for the customers system, as directed in the MF11-U/UP Customer Print Set. (See M8293 MAT A)
- 1.3 If this option is part of a PDP-11/40-11/45 installation, as opposed to an add on, then the system acceptance procedures provided with those systems should be utilized in place of this procedure.

2.0 Inspection

2.1 Assure presence of the following documentation:

- 2.1.1 Customer Acceptance Form
- 2.1.2 Keysheets (2)
- 2.1.3 Accessory Checklist
- 2.1.4 LIBKIT list for MF11-U/UP
- 2.1.5 ECO Status Sticker (for mounting in expansion box)
- 2.1.6 Waiver Sheet (if applicable)
- 2.1.7 Documentation Update Card (if applicable).

2.2 Utilize the accessory checklist, and LIBKIT list to verify that all items are present.

3.0 Diagnostic Testing:

3.1 The following tests must be run without error for the times specified:

\*Maindec-11-DZQMA Memory I/O 5 min/MF11-U/UP  
Maindec-11-DZQMB Memory Exerciser 5 min/MF11-U/UP  
Maindec-11-DCMFA Parity Test 2 passes/MF11-U/UP  
(MF11-UP Memory Only)

\*Only for add-on memories in systems with NPR devices

	SIZE A	CODE SP	NUMBER MF11-U-3	REV

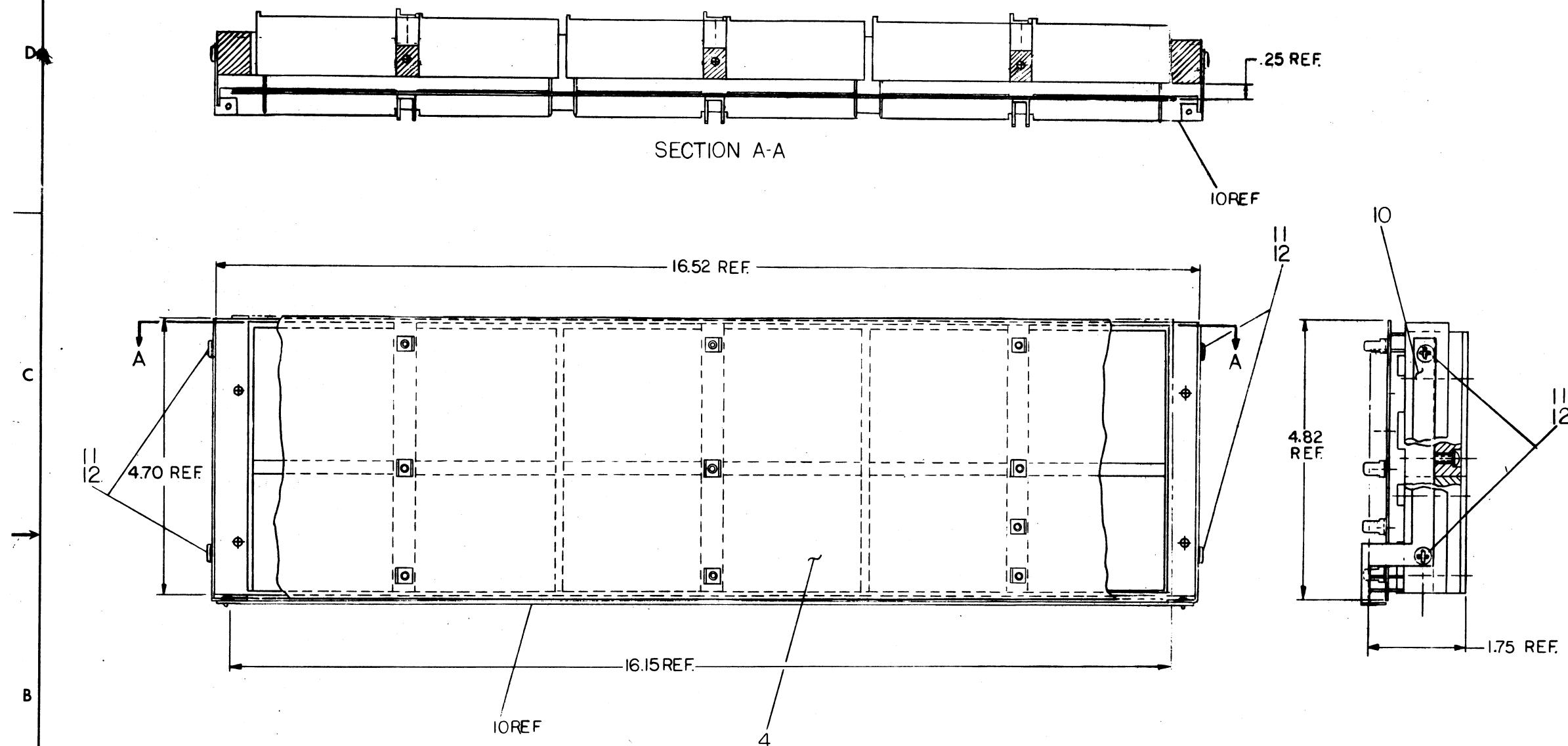
DEC FORM NO DEC 16-(381)-1022-N370  
DRA 108

SHEET 2 OF 3

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1979

2 D UJA MFII-U-0 2 SIZE CODE NUMBER 1

NOTES:



REVISIONS		REV.	CHG NO.	CHANGE NO.
		B		MFIIU-00003
		D		MFIIU-00004
		C		MFIIU-00004
		A		G Change 2-26-75
		D		D Snelser
				Change 2-26-75
				D Snelser
				Change 2-26-75

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
MFII-U				
<b>PARTS LIST</b>				
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES. TOLERANCES				
DECIMALS	ANGLES	DRW. G. Charles	DATE 2-25-75	EQUIPMENT CORPORATION
XX - .006	± 0° 30'	CHKD G. Charles	DATE 2-25-75	digital HANOVER MASSACHUSETTS
XX - .02		PPOL. SNG. G. Charles	DATE 2-26-75	
X - .1		REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓	DATE 2/26/75	
		MATERIAL	NEXT HIGHER ASSY.	
			B-DD-MFII-U	SIZE CODE
				NUMBER
				REV.
				D
			D UJA MFII-U-0	
			SHEET 1 OF 1	DIST.

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DRAWING NUMBER	INIT REL	AUTOMATIC WIRE TESTER (AWT) REVISION STATUS											
		T4	C										
D-CS-5410345-0-1	C	C											
D-AD-7009295-0-0	C	D											
REVISIONS		CHANGE NO.	REV.										
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CHK'D.		J. Gilbert		DATE		26 Nov 75		MAYNAPD, MASSACHUSETTS					
ENG				DATE		12-1-75		digital					
PROD/ENG.				DATE		12-1-75		TITLE					
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