Arora V Analog to Digital Converter (ADC)

User Guide

UG299-1.0.2E, 12/08/2023

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Revision History

Date	Version	Description
05/08/2023	1.0E	Initial version published.
07/31/2023	1.0.1E	The description of “2.3.1 ADC Conversion Timing” optimized.
12/08/2023	1.0.2E	ADC parameter descriptions updated.

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1 About This Guide

1.1 Purpose

Arora V Analog to Digital Converter (ADC) User Guide is to help you quickly learn the features and usage of Arora V ADC by introducing to the functions, ports, configuration, etc.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI website. You can find the related documents at www.gowinsemi.com:

- DS981E, GW5AT series of FPGA Products Data Sheet
- DS1103E, GW5A series of FPGA Products Data Sheet
- DS1104E, GW5AST series of FPGA Products Data Sheet
- DS1108E, GW5AR series of FPGA Products Data Sheet
- DS1115E, GW5AS-25 Data Sheet
- DS1114E, GW5AS-138 Data Sheet
- SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ADC	Analog to Digital Converter
CIC Filter	Cascaded Integrator–comb Filter
FPGA	Field Programmable Gate Array
IP	Intellectual Property
OSC	Oscillator
SRAM	Static Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

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2 Overview

Arora V series of FPGA products integrate eight-channel 10 bits Delta-sigma ADC. It is an ADC with low power, low-leakage current, and high dynamic performance. When combined with the programmable logic capability of the FPGA, the sensor can address the data acquisition and monitoring requirements for by chip internal temperature and power monitoring. FPGA also provides rich and freely configurable GPIO interfaces and ADC analog signal interfaces to connect to the ADC voltage channels, which can meet the voltage data sampling and monitoring requirements.

2.1 Features

The main features of Arora V ADC are as follows:

- Number of ADC:
  - GW5A-25/ GW5AR-25/ GW5AS-25: 1
  - GW5A-138/ GW5AT-138/ GW5AT-75/ GW5AST-138: 2
- Reference voltage source: Built-in
- Number of channels per ADC: 8
- Bit width accuracy: 10 bits
- Sampling Clock: < 2MHz
- ADC unipolar input voltage: 0~1V
- Temperature sensor accuracy: +/-2□
- Voltage sensor accuracy: +/-5mV

2.2 Functional Description

2.2.1 Overview

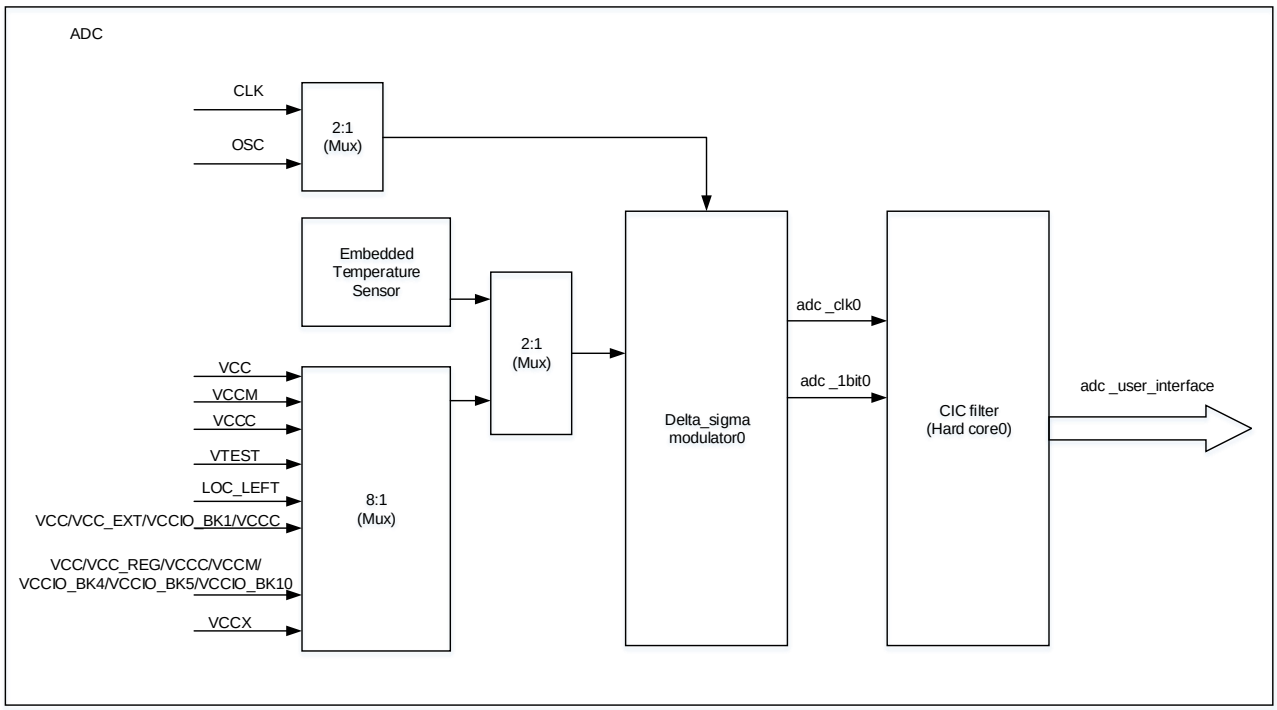
Arora V ADC provides analog Delta-sigma modulators to meet the requirements of on-chip temperature and voltage detection in multiple regions, and also provides abundant input interfaces to meet off-chip voltage and temperature input, supporting single-ended and differential signal input. (Positive input voltage > Negative input voltage)

Arora V ADC has embedded reference voltage source with high accuracy, and it does not require off-chip voltage reference source; Arora V ADC features low power and high accuracy for temperature and supply voltage detection. Arora V ADC has an internally integrated voltage signal processing module, so no external voltage reference source is required. It meets the accuracy of voltage signal measurements and helps to reduce user costs.

2.2.2 Architecture

Figure 2-1 shows the structure diagram of GW5A-25 / GW5AR-25 / GW5AS-25 ADC.

Figure 2-1 GW5A-25 ADC Structure Diagram



GW5A-25 / GW5AR-25 / GW5AS-25 ADC supports on-chip temperature and voltage detection. Through the control signal, you can

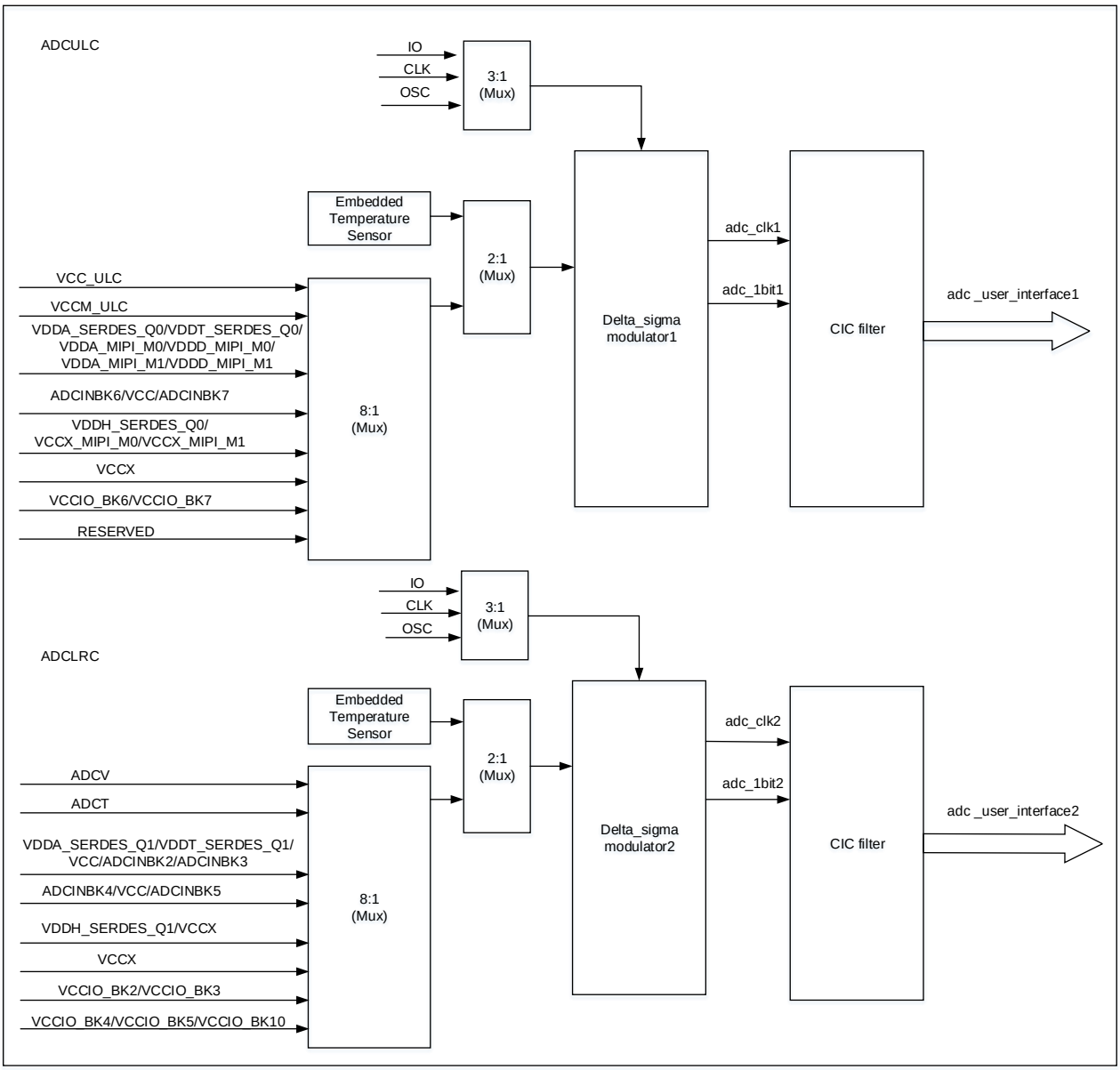
select the voltage from the on-chip temperature sensor to enter the on-chip temperature detection mode; or you can select another path to monitor the power supply voltage of IP modules in the FPGA, including Bank1/4/5/10 voltage, core voltage, and SRAM voltage, etc.

For GW5A-25 / GW5AR-25 / GW5AS-25 ADC, you can select UserLogic clock or OSC clock to obtain a better balance between power and performance.

The voltage signal into the Delta sigma modulator0 is quantized and noise-shaped to output adc_1bit0 and adc_clk0, which can be sent to the embedded CIC hard core or CIC soft core for further processing to obtain the digital characterization of temperature and voltage.

GW5A-138/GW5AT-138/GW5AT-70/GW5AST-138 offers two ADCs. Figure 2-2 shows the structure diagram.

Figure 2-2 GW5A-138/GW5AT-138/GW5AT-70 /GW5AST-138 ADC Structure Diagram



GW5A-138/GW5AT-138/GW5AT-70/GW5AST-138 supports on-chip temperature and voltage detection. Through the control signal, you can select the voltage from the on-chip temperature sensor to enter the on-chip temperature detection mode; or you can select another path to monitor the power supply voltage of IP modules in the FPGA, including Bank2/3/4/5/6/7/10 voltage, core voltage, MIPI and SERDES voltage, etc. Off-chip voltage signals can be sent to ADC for ADC quantization via Bank2/3/4/5/6/7 GPIO pins.

For GW5A-138/GW5AT-138/GW5AT-70/GW5AST-138 ADC, you can select user logic clock IO, GPIO clock or OSC clock to obtain a better balance between power and performance.

The voltage signal into the Delta_sigma modulator1/Delta_sigma modulator2 is quantized and noise-shaped to output adc_1bit1/adc_1bit2 and adc_clk1/adc_clk2. They can be sent to the embedded CIC hard core for further processing to obtain the digital characterization of temperature and voltage.

In addition, the 138K ADC supports two differential pairs: adcvp/adcvn, adctp/adctn, providing users with a low-latency, low-noise differential voltage input channel.

2.3 ADC Characteristics

2.3.1 ADC Conversion Timing

There are N clock cycles needed for the ADC to sample analog input signals, convert them to output digital signals, and then generate the output signals. When the rising edge of the sensor_req signal comes, and the sensor_en signal is enabled (active-high), the ADC will be triggered to sample once; when the sensor measurement is finished, it will pull the sensor_rdy signal high to indicate the completion of sampling and output the sampling value of sensor_value[13:0].

In voltage measurement mode, the output value of sensor_value is an unsigned number (sensor_value [13:11] for the integer part and sensor_value [10:0] for the fractional part), which needs to be divided by 2048 to get the actual measured value in V.

In temperature mode, the output value of sensor_value is a signed number (sensor_value [13] for the sign bit, sensor_value [12:2] for the integer part and sensor_value [1:0] for the fractional part), which needs to be divided by 4 to get the actual measured value in℃.

Figure 2-3 ADC Conversion Timing

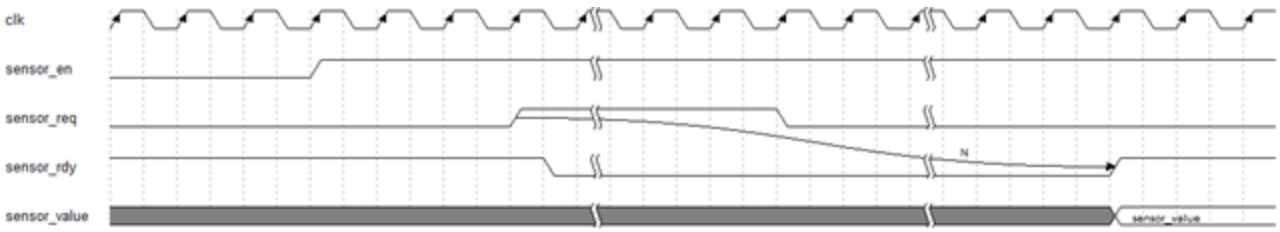


Table 2-1 ADC Timing Parameters

Symbol	Description	Spec.		Unit
		Min.	Max.	
CLK	Clock cycle	TBD	TBD	ns
T_S	SOC setup time	TBD	TBD	ns
T_H	SOC hold-up time	TBD	TBD	ns
T_{D_EOC}	EOC delay time	TBD	TBD	ns
T_{D_B}	Data-out delay time	TBD	TBD	ns

2.3.2 Electrical Characteristic Parameters

Table 2-2 ADC Electrical Parameters

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
DC precision					
Output	Digital output bits	-	10	-	Bit
INL	Integral nonlinearity	-	TBD	-	LSB
DNL	Differential nonlinearity	-	TBD	-	LSB
Offset error	Offset error	-	TBD	-	%FS
Gain error	Gain error	-	TBD	-	%FS
Analog Input					
CH[7：0]	Single-ended input range	-	TBD	-	V
CIN	Input capacitance	-	TBD	-	pF
Slew Rate					
SoC	Sample frequency	-	TBD	-	MHz
CLK	Master Clock	-	TBD	-	MHz
Date-out delay	Date-out delay	-	TBD	-	Clock cycle
Dynamic Characteristic Parameters					
SINAD	Signal Noise Ratio	-	TBD	-	DB
		-	TBD	-	DB
SFDR	Spurious-free dynamic range	-	TBD	-	DB
		-	TBD	-	DB
ENOB	Valid output data bits	-	TBD	-	Bit
		-	TBD	-	Bit

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
Digital Input					
V_{IH}	Input high level	-	TBD	-	V
V_{IL}	Input low level	-	TBD	-	V
Digital output B[9：0]					
V_{OH}	Output high level	-	TBD	-	V
V_{OL}	Output low level	-	TBD	-	V
Supply voltage					
V_{dd_a}	Analog core voltage	-	TBD	-	V
V_{dd_dig}	Digital voltage	-	TBD	-	V
Vddx	Analog voltage	-	TBD	-	TBD
I_{vdd_a}	Analog bitstream	-	TBD	-	uA
I_{vdd_dig}	Digital current	-	TBD	-	uA
I_{vddx}	Analog current	-	TBD	-	TBD
I_{pd}	Turn-off current	-	TBD	-	mA

3 ADC

3.1 ADC

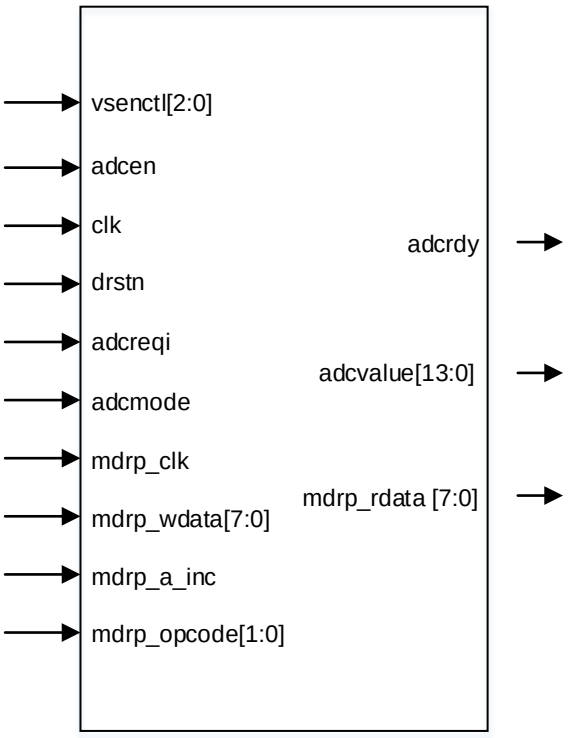
3.1.1 Devices Supported

Table 3-1 Terminology and Abbreviations

Family	Series	Device
Arora®	GW5A	GW5A-25A
	GW5AR	GW5AR-25A
	GW5AS	GW5AS-25A

3.1.2 Port Diagram

Figure 3-1 ADC Port Diagram



3.1.3 Port Description

Table 3-2 ADC Port Description

Port	I/O	Description
clk	input	clk input
drstn	input	digital part reset signal, active low
adcmode	input	mode selection 1’b0: temperature mode 1’b1:voltage mode
vsenctl	input	input source selection bit [2:0] 3’b000: glo_left 3’b001:glo_right 3’b010:loc_left（Corresponding to Bank1 GPIO） 3’b011: vtest 3’b100:vcc 3’b101:vccc 3’b110:vccm 3’b111:vccx_buf

Port	I/O	Description
adcen	input	enable signal, active high
adcreqi	input	measurement request signal, valid rising edge
adcrdy	output	measurement completion signal, active high
adcvalue	output	bit[13:0] the measurement result output
mdrp_rdata	output	bit[7:0] mdrp_rdata
mdrp_clk	input	mdrp clock
mdrp_wdata	input	bit[7:0] mdrp_wdata
mdrp_a_inc	input	mdrp_a_inc
mdrp_opcode	input	bit[1:0] mdrp_opcode
tlvds_ibuf_adc_i	input	The adcvp signal from bank1
tlvds_ibuf_adc_ib	input	The adcvn signal from bank1
tlvds_ibuf_adc_adcen	input	The adc enable signal from bank1

3.1.4 Parameter Description

Table 3-3 ADC GUI Parameters

Parameter	Default Value	Description
ADC Select	ADC	ADC
ADC Mode	Temperature	Temperature/Voltage
Division Factor	1	clock division 0: /1, 1: /2, 2: /4, 3: /8 Clock after frequency division, 500kHz~8MHz
Clock Select	OSC	clk source osc (2.5MHz) or CLK
Sample Rate	64	sample rate configuration 4/8/16/32/64/128
Sample Count	1024	sample count configuration 64/128/256/512/1024/2048
Fscal Value	730(Temperature) 623(Voltage)	temperature mode: 510~948 voltage mode: 452~840
Offset	-1180(Temperature) 0(Voltage)	temperature mode: -1560~-760 voltage mode: -410~410
Dynamic Bank Enable (Voltage mode)	Unchecked	If checked, the tlvds_ibuf_adc ADC input interface (Bank1 input) will be enabled.
glo_left	vcc	vcc/vcc_ext/vccio_bk1/vccc/pad The pad

Parameter	Default Value	Description
(Voltage mode)		corresponds to the bank0/6/7 IOs, referred to as bus0. When using the IOs of these banks as ADC inputs, it is necessary to add the physical constraints as follows: USE_ADC_SRC_bus0 loc.
glo_right (Voltage mode)	vcc_reg	vcc/vcc_reg/vccc/vccm/vccio_bk4/ vccio_bk5/vccio _bk10/pad The pad corresponds to the bank2/3/4/5 IOs, referred to as bus0. When using the IOs of these banks as ADC inputs, it is necessary to add the physical constraints as follows: USE_ADC_SRC_bus1 loc.
vccx_buf (Voltage mode)	vccx	vccx

3.1.5 ADC Instantiation

Verilog Instantiation:

```
Gowin_ADC    Gowin_ADC_inst (
    .adcrdy(adcrdy_o),
    .adcvalue(adcvalue_o),
    .mdrp_rdata(mdrp_rdata_o),
    .vsenctl(vsenctl_i),
    .adcen(adcen_i),
    .clk(clk_i),
    .drstn(drstn_i),
    .adcreqi(adcreqi_i),
    .adcmode(adcmode_i),
    .mdrp_clk(mdrp_clk_i),
    .mdrp_wdata(mdrp_wdata_i),
    .mdrp_a_inc(mdrp_a_inc_i),
    .mdrp_opcode(mdrp_opcode_i)
);
```

Vhdl Instantiation:

```
component Gowin_ADC
    port (
        adcrdy: out std_logic;
        adcvalue: out std_logic_vector(13 downto 0);
        mdrp_rdata: out std_logic_vector(7 downto 0);
        vsenctl: in std_logic_vector(2 downto 0);
        adcen: in std_logic;
        clk: in std_logic;
        drstn: in std_logic;
        adcreqi: in std_logic;
        adcmode: in std_logic;
        mdrp_clk: in std_logic;
        mdrp_wdata: in std_logic_vector(7 downto 0);
        mdrp_a_inc: in std_logic;
        mdrp_opcode: in std_logic_vector(1 downto 0)
    );
end component;

Gowin_ADC_inst: Gowin_ADC
    port map (
        adcrdy => adcrdy_o,
        adcvalue => adcvalue_o,
        mdrp_rdata => mdrp_rdata_o,
        vsenctl => vsenctl_i,
        adcen => adcen_i,
        clk => clk_i,
        drstn => drstn_i,
        adcreqi => adcreqi_i,
        adcmode => adcmode_i,
        mdrp_clk => mdrp_clk_i,
        mdrp_wdata => mdrp_wdata_i,
        mdrp_a_inc => mdrp_a_inc_i,
```

```
        mdrp_opcode => mdrp_opcode_i
    );
```

3.2 ADC

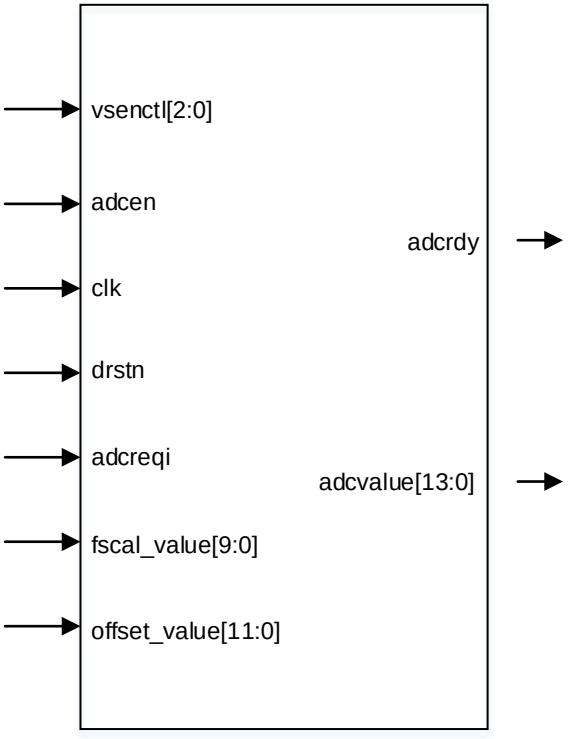
3.2.1 Devices Supported

Table 3-4 Terminology and Abbreviations

Family	Series	Device
Arora®	GW5A	GW5A-138B
	GW5AS	GW5AS-138B
	GW5AT	GW5AT-138 / GW5AT-138B / GW5AT-75B
	GW5AST	GW5AT-138B

3.2.2 Port Diagram

Figure 3-2 ADC Port Diagram



3.2.3 Port Description

Table 3-5 ADCULC Port Description

Port	I/O	Description
clk	input	clk input

Port	I/O	Description
drstn	input	digital part reset signal, active low
vsenctl	input	input source selection bit[2:0] 3'b000:vtest 3'b001:vdd09_0 3'b010:vdd09_1 3'b011:vdd09_2 3'b100:vdd18_0 3'b101:vdd18_1 3'b111:vdd33
adcen	input	enable signal, active high
adcreqi	input	measurement request signal, valid rising edge
adcrdy	output	measurement completion signal, active high
adcvalue	output	bit[13:0] the measurement result output
fscal_value	input	bit[9:0] temperature mode: 510~948 voltage mode: 452~840
offset_value	input	bit[11:0] emperature mode: -1560~-760 voltage mode: -410~410
tlvds_ibuf_adc_i	input	The adcvp signal from bank6/7
tlvds_ibuf_adc_ib	input	The adcvn signal from bank6/7
tlvds_ibuf_adc_adcen	input	The adc enable signal from bank6/7
adcinbk6a	input	adcvp from Bank6 GPIO
adcinbk6b	input	adcvn from Bank6 GPIO
adcinbk7a	input	adcvp from Bank7 GPIO
adcinbk7b	input	adcvn from Bank7 GPIO

Table 3-6 ADCLRC Port Description

Port	I/O	Description
CLK	input	clk input
DRSTN	input	digital part reset signal, active low
VSENCTL	input	input source selection bit[2:0] 3'b000: adcv 3'b001: adct 3'b010: vdd09_0

Port	I/O	Description
		3’b011: vdd09_1 3’b100: vdd18_0 3’b101: vdd18_1 3’b110: vdd33_0 3’b111: vdd33_1
ADCEN	input	enable signal, active high
ADCREQI	input	measurement request signal, valid rising edge
ADCRDY	output	measurement completion signal, active high
ADCVALUE	output	bit[13:0] the measurement result output
FSCAL_VALUE	input	bit[9:0] temperature mode: 510~948 voltage mode: 452~840
OFFSET_VALUE	input	bit[11:0] emperature mode: -1560~-760 voltage mode: -410~410
TLVDS_IBUF_ADC_I	input	The adcvp signal from bank2/3
TLVDS_IBUF_ADC_IB	input	The adcvn signal from bank2/3
TLVDS_IBUF_ADC_ADCEN	input	The adc enable signal from bank2/3
ADCINBK2A	input	adcvp from Bank2 GPIO
ADCINBK2B	input	adcvn from Bank2 GPIO
ADCINBK3A	input	adcvp from Bank3 GPIO
ADCINBK3B	input	adcvn from Bank3 GPIO
ADCINBK4A	input	adcvp from Bank4 GPIO
ADCINBK4B	input	adcvn from Bank4 GPIO
ADCINBK5A	input	adcvp from Bank5 GPIO
ADCINBK5B	input	adcvn from Bank5 GPIO

3.2.4 Parameter Description

Table 3-7 ADCULC GUI Parameters

Parameter	Default Value	Description
ADC Select	ADCULC	ADCULC/ADCLRC
ADC Mode	Temperature	Temperature/Voltage
Division Factor	1	clock division 0: /1, 1: /2, 2: /4, 3: /8 Clock after frequency division, 500kHz~8MHz

Parameter	Default Value	Description
Clock Select	OSC	clk source osc(2.5MHz) /CLK/IO
VSEN Control	Unchecked	vsenctl control port If checked, the ADC IP generated has no vsenctl signal.
Sample Rate	64	sample rate configuration 4/8/16/32/64/128
Sample Count	1024	sample count configuration 64/128/256/512/1024/2048
Fscal Value	730(Temperature) 623(Voltage)	temperature mode: 510~948 voltage mode: 452~840
Offset	-1180(Temperature) 0(Voltage)	temperature mode: -1560~-760 voltage mode: -410~410
Dynamic Bank Enable (Voltage mode)	Unchecked	If checked,the tlvds_ibuf_adc ADC input port will be enabled. (Bank6/7 input)
vtest (Voltage mode)	vcc	vcc
vdd09_0 (Voltage mode)	vccm	vccm
vdd09_1 (Voltage mode)	vdda_serdes_q0	vdda_serdes_q0/vddt_serdes_q0/vdda_mipi_m0/ vddd_mipi_m0/ vdda_mipi_m1/ vddd_mipi_m1
vdd09_2 (Voltage mode)	ADCINBK6	ADCINBK6/vcc/ ADCINBK7
Vdd18_0 (Voltage mode)	vddh_serdes_q0	vddh_serdes_q0/vccx_mipi_m0/ vccx_mipi_m1
Vdd18_1 (Voltage mode)	vccx	vccx
Vdd33 (Voltage mode)	vccio_bk6	vccio_bk6/vccio_bk7

Table 3-8 ADCLRC GUI Parameters

Parameter	Default Value	Description
ADC Select	ADCULC	ADCULC/ADCLRC
ADC Mode	Temperature	Temperature/Voltage
Division Factor	1	clock division 0: /1, 1: /2, 2: /4, 3: /8 Clock after frequency division, 500kHz~8MHz
Clock Select	OSC	clk source osc(2.5MHz) /CLK/IO
VSEN Control	Unchecked	vsenctl control port If checked, the ADC IP generated has no vsenctl signal.
Sample Rate	64	sample rate configuration 4/8/16/32/64/128
Sample Count	1024	sample count configuration 64/128/256/512/1024/2048
Fscal Value	730(Temperature) 623(Voltage)	temperature mode: 510~948 voltage mode: 452~840
Offset	- 1180(Temperature) 0(Voltage)	temperature mode: -1560~-760 voltage mode: -410~410
Dynamic Bank Enable (Voltage mode)	Unchecked	If checked,the tlvds_ibuf_adc ADC input port will be enabled. (Bank2/3 input)
vdd09_0 (Voltage mode)	vdda_serdes_q1	vdda_serdes_q1/vddt_serdes_q1/vcc/ADCINBK2/ADCINBK3
vdd09_1 (Voltage mode)	ADCINBK4	ADCINBK4/vcc/ ADCINBK5
vdd18_0 (Voltage mode)	vddh_serdes_q1	vddh_serdes_q1/ vccx
vdd18_1 (Voltage mode)	vccx	vccx
vdd33_0 (Voltage mode)	vccio_bk2	vccio_bk2/vccio_bk3
vdd33_1 (Voltage mode)	vccio_bk4	vccio_bk4/ vccio_bk5/vccio_bk10

3.2.5 ADC Instantiation (Take ADCULC as an Example)

Verilog Instantiation:

```
Gowin_ADC Gowin_ADC_inst(
    .adcrdy(adcrdy_o), //output adcrdy
    .adcvalue(adcvalue_o), //output [13:0] adcvalue
    .adcinbk6a(adcinbk6a_i), //input adcinbk6a
    .adcinbk6b(adcinbk6b_i), //input adcinbk6b
    .adcinbk7a(adcinbk7a_i), //input adcinbk7a
    .adcinbk7b(adcinbk7b_i), //input adcinbk7b
    .vsenctl(vsenctl_i), //input [2:0] vsenctl
    .adcen(adcen_i), //input adcen
    .clk(clk_i), //input clk
    .drstn(drstn_i), //input drstn
    .adcreqi(adcreqi_i) //input adcreqi
);
```

Vhdl Instantiation:

```
component Gowin_ADC
    port (
        adcrdy: out std_logic;
        adcvalue: out std_logic_vector(13 downto 0);
        adcinbk6a: in std_logic;
        adcinbk6b: in std_logic;
        adcinbk7a: in std_logic;
        adcinbk7b: in std_logic;
        vsenctl: in std_logic_vector(2 downto 0);
        adcen: in std_logic;
        clk: in std_logic;
        drstn: in std_logic;
        adcreqi: in std_logic
    );
end component;
```

```
Gowin_ADC_inst: Gowin_ADC
    port map (
        adcrdy => adcrdy_o,
        adcvalue => adcvalue_o,
        adcinbk6a => adcinbk6a_i,
        adcinbk6b => adcinbk6b_i,
        adcinbk7a => adcinbk7a_i,
        adcinbk7b => adcinbk7b_i,
        vsenctl => vsenctl_i,
        adcen => adcen_i,
        clk => clk_i,
        drstn => drstn_i,
        adcreqi => adcreqi_i
    );
```

4 ADC Configuration and Call

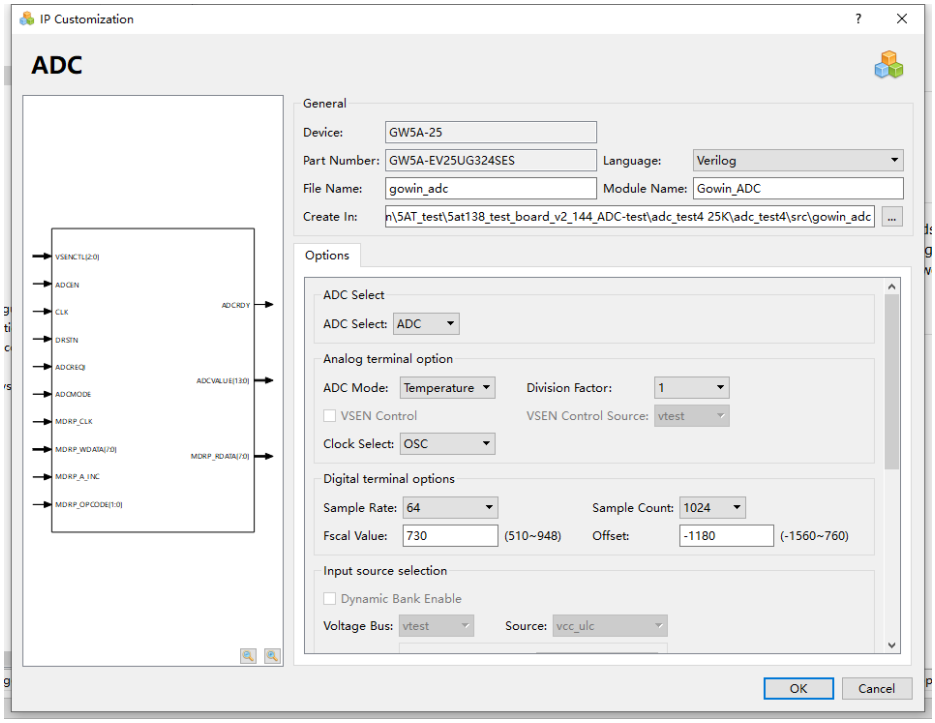
You can click “Tools > IP Core Generator” in Gowin Software to call and configure ADC.

The following description takes the GW5A-25 ADC call as an example.

4.1 ADC Configuration

The ADC configuration interface is shown in Figure 4-1.

Figure 4-1 ADC Configuration



4.2 Generation Files

After ADC configuration, it will generate three files that are named after the "File Name". Take the default configuration as an example:

- “gowin_adc.v” file is a complete Verilog module to generate instance Gowin_ADC;
- “gowin_adc_tmp.v” is a template file for IP designs;
- “gowin_adc.ipc” file is an IP configuration file for users to load and configure the IP.

Note!

If VHDL is selected as the hardware description language, the first two files will be named with .vhd suffix.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