Gowin B-SRAM

User Guide

UG285-1.09E, 5/31/2018

Disclaimer

Revision History

Date	Version	Description
05/31/2018	1.09E	Initial version published.

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1 About This Guide

1.1 Purpose

This Gowin B-SRAM user guide describes the GOWINSEMI B-SRAM features, operation modes, timing, operation notes, etc.

1.2 Supported Products

The information in this guide applies to the following products:

1. GW1N series of FPGA products: GW1N-1, GW1N-2, GW1N-4, GW1N-6, and GW1N-9.
2. GW1NR series of FPGA products: GW1NR-4, GW1NR-9;
3. GW2A series of FPGA products: GW2A-55, GW2A-18;
4. GW2AR series FPGA products: GW2AR-18

1.3 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series of Products Data Sheet
2. GW1NR series of FPGA Products Data Sheet
3. GW2A series of FPGA Products Data Sheet
4. GW2AR series of FPGA Products Data Sheet
5. Gowin FPGA Primitives Guide
6. Gowin IP Core Generator User Guide

1.4 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name	Meaning
B-SRAM	Block SRAM	Block SRAM
SP	Single Port	Single Port
DP	Dual Port	Dual Port
SDP	Semi Dual Port	Semi Dual Port
CFU	Configurable Function Unit	Configurable Function Unit
CST	Constraint Text	Physical Constraints File

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: +86 755 8262 0391

2 Overview

GOWINSEMI FPGA products provide abundant block static random access memories, B-SRAM for short. B-SRAM is embedded as a row in GOWINSEMI FPGA products. In the FPGA array, each B-SRAM occupies three columns of CFU. The number of B-SRAM depends on the device family. For the detailed capacity, please refer to *GW1N series of FPGA Products Data Sheet*, *GW1NR series of FPGA Products Data Sheet*, *GW2A series of FPGA Products Data Sheet*, and *GW2AR series of FPGA Products Data Sheet*.

Data width and address depth can be configured for each B-SRAM. Each B-SRAM can be configured with up to 18 Kbits. Each B-SRAM has two ports: Port A and Port B. Either port can be a read or write port. They have independent clocks, addresses, data, and control signals, but they share the same storage memory. Each B-SRAM has four operation modes: Single Port, Dual Port, Semi-dual Port, and ROM. In the semi-dual Port, Port A can only write, and Port B can only read.

B-SRAM supports the data initialization operation. You can opt to set the related parameters or read the initialization file using the IP core generator. The B-SRAM write operation and read operation is clock synchronous. The B-SRAM input port and output port have registers, and the input port register supports clock synchronization between writing data and control signal. The output register supports the pipeline mode to increase system timing and performance. It also supports the bypass mode. In comparison with the bypass mode, the pipeline mode adds one clock cycle latency; however, the pipeline mode is recommended. B-SRAM write operation supports normal-write mode, write-through mode, and read-before-write mode.

The IP Core Generator that is integrated into the Gowin YunYuan software supports the generation of the B-SRAM Single Port mode, Dual Port mode, Semi-dual Port mode, and ROM mode.

2.1 Features

- Each B-SRAM can store up to 18Kbits of data
- Supports Single Port mode (SP)
- Supports Dual Port Mode (DP)
- Supports Semi-dual Port mode (SDP)

- Supports Read Only mode (ROM)
- Data width ranges from 1 bit to 36 bits
- Dual Port and Semi-dual Port support independent clocks and independent data width
- 16 bits or above data width supports byte enable
- Asynchronous reset with optional synchronous release
- Supports Pipeline Mode and Bypass Mode.
- Write operation supports Normal-write Mode, Write-through Mode, and Read-before-write Mode

2.2 Configuration

Each B-SRAM can be configured as 16 Kbits or18 Kbits. Data width and address depth can be configured as shown in Table 2-1.

Table 2-1 Configuration

Capacity	Single Port Mode		Dual Port Mode		Semi-dual Port Mode		Read Only	
16Kbits	SP	16 K x 1	DP	16K x 1	SDP	16K x 1	ROM	16K x 1
		8K x 2		8K x 2		8K x 2		8K x 2
		4K x 4		4K x 4		4K x 4		4K x 4
		2K x 8		2K x 8		2K x 8		2K x 8
		1K x 16		1K x 16		1K x 16		1K x 16
		512 x 32		–		512 x 32		512 x 32
18Kbits	SPX9	2K x 9	DPX9	2K x 9	SDPX9	2K x 9	ROMX9	2K x 9
		1K x 18		1K x 18		1K x 18		1K x 18
		512 x 36		–		512 x 36		512 x 36

Each B-SRAM has 14 address lines, that is AD[13:0], and the maximum address depth is 16,384. Different data widths use different address line, as shown in Table 2-2.

Table 2-2 Data Width and Address Width

Type	Configuration	Data Depth	Address Depth	Address Width
SP SDP DP ROM	16K x 1	[0:0]	16,384	[13:0]
	8K x 2	[1:0]	8,192	[13:1]
	4K x 4	[3:0]	4,096	[13:2]
	2K x 8	[7:0]	2,048	[13:3]
	1K x 16	[15:0]	1,024	[13:4]
	512 x 32	[31:0]	512	[13:5]
SPX9 SDPX9 DPX9 ROMX9	2K x 9	[8:0]	2,048	[13:3]
	1K x 18	[17:0]	1,024	[13:4]
	512 x 36	[35:0]	512	[13:5]

Dual Port and Semi-dual Port support independent read/write clocks

and independent read/write data width. In Dual Port mode, the data widths supported by Port A and Port B are as shown in Table 2-3. In Semi-dual Port mode, the data widths supported by Port A and Port B are as shown in Table 2-4.

Table 2-3 Data Width Configuration in Dual Port Mode

Type	Port B	Port A						
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
DP	16K x 1	*	*	*	*	*		
	8K x 2	*	*	*	*	*		
	4K x 4	*	*	*	*	*		
	2K x 8	*	*	*	*	*		
	1K x 16	*	*	*	*	*		
DPX9	2K x 9						*	*
	1K x 18						*	*

Note!

"*"denotes the modes supported.

Table 2-4 Data Width Configuration in Semi Dual Port Mode

Type	Port B	Port A								
		16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512 x 36
SDP	16K x 1	*	*	*	*	*	*			
	8K x 2	*	*	*	*	*	*			
	4K x 4	*	*	*	*	*	*			
	2K x 8	*	*	*	*	*	*			
	1K x 16	*	*	*	*	*	*			
	512 x 32	*	*	*	*	*	*			
SDPX9	2K x 9							*	*	*
	1K x 18							*	*	*

Note!

"*"denotes the modes supported.

2.2.1 Single Port Mode

Single port mode supports the operations as follows:

- Read/write at a clock edge
- Supports normal-write mode, write-through mode, and read-before-write mode
- Supports Pipeline Mode and Bypass Mode
- Supports Synchronous Reset and Asynchronous Reset

2.2.2 Dual Port Mode

Dual port mode supports the following operations:

- Two independent reads
- Two independent writes
- Independent clock
- Supports normal-write mode, write-through mode, and read-before-write mode
- Supports pipeline mode and bypass mode

- Supports synchronous reset and asynchronous reset

2.2.3 Semi-Dual Port Mode

Semi Dual port mode supports the operations as follows:

- Port A writes, Port B reads
- Independent clock
- Supports normal mode
- Supports pipeline mode and bypass mode
- Supports synchronous reset and asynchronous reset

2.2.4 Read Only

Read only mode supports the operations as follows:

- Supports pipeline mode and bypass mode
- Supports synchronous reset and asynchronous reset

3 Ports and Parameters

3.1 Structure View

Each B-SRAM can store up to 18 Kbits of data. It includes Port A and Port B.

Figure 3-1 Structure View

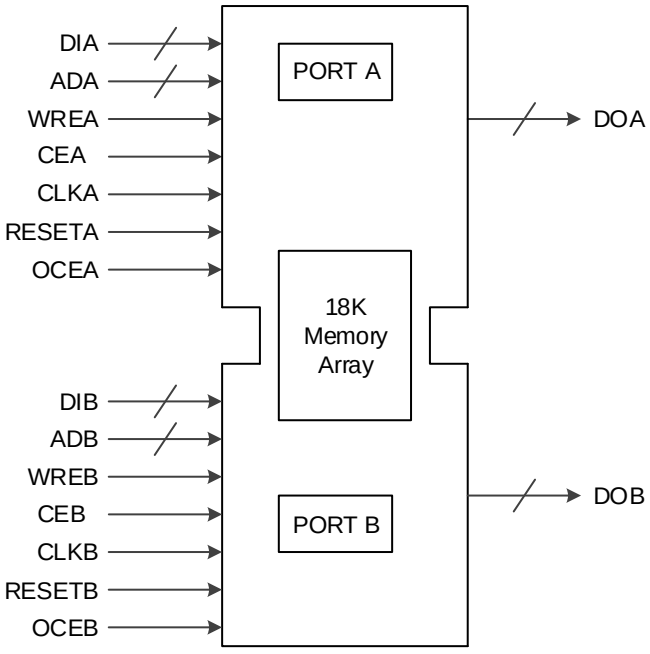


Table 3-1 Ports List

Port Name	I/O	Description
DIA/ DIB	I	Port A/B data input
ADA/ ADB	I	Address signal for port A/B, including byte enable signal[1]
CEA/ CEB	I	Clock Enable, Port A/B
RESETA/ RESETB	I	Output reset signal, Port A/B
WREA/ WREB	I	Read/Write Enable, Port A/B
BLKSEL	I	Block select
CLKA/ CLKB	I	Read/Write Clock for Port A/B

Port Name	I/O	Description
OCEA/ OCEB	I	Clock enable for Port A/B output registers
DOA/ DOB	O	Port A/B data output

3.2 Ports Signal Description

CLKA, CLKB

The clock signals of Port A/B are active at rising edge by default. B-SRAM read/write operations synchronize with the clock signals. The clock signals of the two ports are independent. Single port mode has only one CLK. Dual Port mode and Semi-dual Port mode have CLKA and CLKB. Read/write operations can be performed at different clocks.

CEA, CEB

The clock enable signals of Port A/B are active-high by default. Ports with an inactive enable signals do not write data to the memory cells. Unexpected write operation may occur when the clock enable signal is used to write. For further details, please refer to Appendix A. Ports with an inactive enable signals do not read data from the memory cells. Unexpected read operation may occur when the clock enable signal is used to read. For further details, please refer to Appendix A.

WREA, WREB

Single port mode only has one signal: WRE. The port writes when the signal is high and the clock enable signal is active. The port reads when the signal is low and the clock enable signal is active.

Dual port mode REA/WREB controls the read/write operation of Port A/B. The Port A/B write when the signal is high and the clock enable signal is active. The Port A/B read when the signal is low and the clock enable signal is active.

Semi-dual port WREA only controls write operation. The write operation is valid when the clock enable signal is active and WREA is high. WREB only controls read operation. The write operation is valid when the clock enable signal is active and WREB is low.

Unexpected write operation may occur when WREA is employed to control write. For further details, please refer to Appendix A. Unexpected write operation may occur when WREB is employed to control read. For further details, please refer to Appendix A.

ADA, ADB

The address signal of Port A/B, ADA and ADB, can be employed to select the read/write operation address or a range of address. Note that the

address ranges of the read operation and write operation can not exceed the allowed max. data depth, no matter the storage memory is 16 Kbits or 18 Kbits.

AD is write operation and read operation of the single port mode. Dual-port ADA/ADB is the read/write operation address of Port A/B. The two ports share a same storage address. The Semi-dual port ADA is the write operation address. ADB is the read operation address.

BYTE_ENA, BYTE_ENB

BYTE_ENA and BYTE_ENB are used to realize 16bits/18bits and 32bits/36bits data widths byte enable. They are active-high. If the data is required to write to the storage cell, the corresponding byte needs to be set to high.

When users call the library primitives to realize the storage, this signal is assigned to the low-bit of the address signal. When users generate B-SRAM using IP Core Generator, the software automatically assigns byte_en to the low-bit of the address signal.

Table 2-2 lists the corresponding relationship between data width and address width. When the data width is 16/18 or 32/36, the lower-bit of the address signal is the byte-enable signal, as shown in Table 3-2.

The byte-enable signals and the corresponding data signals are shown in Table 3-3.

Table 3-2 Byte-enable and Address Signals

Data Depth	Address Width	Byte Enable Width	Address Value AD[13:0]
1	14	–	ad1[13:0]
2	13	–	{ad1 [12:0],1’b0}
4	12	–	{ad1 [11:0],2’b00}
8/9	11	–	{ad1 [10:0],3’b000}
16/18	10	2	{ad1[9:0],2’b00,byte_en[1:0]}
32/36	9	4	{ad1[8:0],1’b0,byte_en[3:0]}

Note!

- [1] ad is the user input address.

Table -3-3 Byte-enable and Data Signals

Byte Enable Signal	Data Signal /32	Data Signal /36
byte_en[0]	DI[7:0]	DI[8:0]
byte_en[1]	DI[15:8]	DI[17:9]
byte_en[2]	DI[23:16]	DI[26:18]
byte_en[3]	DI[31:24]	DI[35:27]

Read-in Data: DIA, DIB

Single Port and Semi-dual Port only have one data-input port: DI. For

Dual Port, DIA is the data-input Port A and DIB is the data-input Port B.

Clock enable for output registers: OCEA, OCEB

These two signals are high-active. They are valid for the register output mode in read mode and invalid for pipeline output. If register mode is employed in read mode, the read-out data is output when the read operation is valid and the signal is high.

Single Port and Semi-dual Port only have one clock enable signal, OCE, for output registers. For Dual Port mode, OCEA is the clock enable signal of Port A for output registers and OCEB is the clock enable signal of Port B for output registers.

Read-out Data: DOA, DOB

Single Port and Semi-dual Port only have one data output port: DO. For Dual Port mode, DOA is the data output of Port A and DOB is the data output of Port B.

Reset Signals: RESETA, RESETB

These two signals are high-active. RESETA and RESETB can be used to reset the output registers of Port A and Port B. Synchronous reset and asynchronous reset are supported. They can be configured by the parameter "RESET_MODE", and the default value is synchronous reset. When register output mode is used, the RESET signal is required to be set to high. Output the reset data 0.

Please note that set the RESET signal to high when the port writes data normally.

Expansion Signal: BLKSEL

This signal is used for storage capacity expansion. It supports multiple B-SRAM cascading to support greater storage capacity. There is no expansion by default. Used together with BLK_SEL. The software will handle expansion automatically when IP Core Generator is used to expand storage capacity.

3.3 Parameter Attributes

You can configure the parameters in the B-SRAM modules generated by IP Core Generator or in the B-SRAM primitive library. These parameter attributes are described as below.

READ_MODE

It can be used to set the read mode parameters for B-SRAM Port A/B. "0" denotes the bypass mode; "1" denotes the register output mode. The default value is READ_MODE = 1'b0.

WRITE_MODE

It can be used to set the write mode parameters for B-SRAM Port A/B. The bit width is 2. If the value is 2'b00, it denotes Normal Mode; if the value is 2'b01, it denotes Write-through Mode; if the value is 2'b10, it denotes Read before Write Mode. The default value is WRITE_MODE0 = 2'b00.

BIT_WIDTH

It can be used to set the data width for B-SRAM Port A/B. The B-SRAM with a capacity of 16 Kbits supports x1/x2/x4/x8/x16/x32 bits and the B-SRAM with a capacity of 16 Kbits supports x9/x18/x36 bits, in accordance with the B-SRAM configuration modes. The data width is the max. value supported by default. IP Core Generator configures this parameter automatically according to users' data width.

Block Select Signal: BLK_SEL

BLK_SEL is the B-SRAM cascading signal. To expand storage capacity, it is required to be used in combination with the port signal - BLKSEL. There is no expansion by default. The software will handle expansion automatically when IP Core Generator is used to expand storage capacity.

RESET_MODE

It is used to set the reset mode of Port A/B. It supports SYNC reset and ASYNC reset. The default is that RESET_MODE = "SYNC".

Block Initialization: INIT_RAM_xx

It is used to set the initialization data of B-SRAM. If users do not set the initialization data of B-SRAM, the default value will be set to 0 in bitstream by default. INIT_RAM_00 to INIT_RAM_3F are used for block initialization. For 16 Kbits B-SRAM, each INIT_RAM_xx contains the initialization data for 256 addresses. For 18 Kbits B-SRAM, each INIT_RAM_xx contains the initialization data for 288 addresses. Users can select to initialize partial or all of the block data. The parameter values are all 0 by default.

The B-SRAM addresses those correspond to the 256 bit of INIT_RAM_xx can be calculated by the following formula. "y" denotes the decimal data converted by hexadecimal data.

- Start address: [(y+1) x 256] -1
- End address: y x 256
  For example, the 256 data of INIT_RAM_1A corresponds to the following B-SRAM address:
- “1A” correspind to the decimal data 26
- Start address: [(26+1) x 256] -1 = 6911
- End address: 26 x 256 = 6656

Table 3-4 16Kbits B-SRAM Initialization - Addresses Correspondence

Parameter	Storage Block	
	Start Address	End address
INIT_RAM_00	255	0
INIT_RAM_01	511	256
INIT_RAM_02	767	512
…	…	…
INIT_RAM_1F	8191	7936
…	…	…
INIT_RAM_2F	12287	12032
…	…	…
INIT_RAM_3F	16383	16128

Note! The addresses correspondence of 18 Kbits is the same with that of 16 Kbits.

4 IP Generation

The IP core generator that is integrated in the Gowin YunYuan software can be used to generate IP cores. Users can set data width, address depth, and write/read modes to generate the corresponding IP modules. Besides that, there are two more ways to generate B-SRAM. Users can call the library file of Gowin YunYuan software and set the port and parameters to generate the required IP modules. Synplify Pro can be used to synthesize B-SRAM automatically during code synthesis.

For further details about generating and calling B-SRAM using the IP core generator, please refer to the *Gowin IP Core Generator user guide*.

5 Storage Expansion

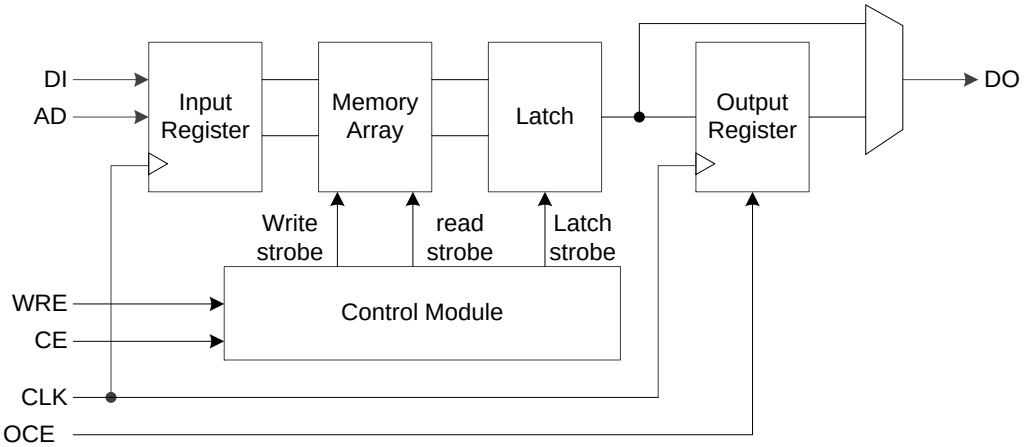
The B-SRAM in GOWINSEMI FPGA devices supports storage expansion. Users can call the primitives to expand the storage capacity by themselves or use the IP Core Generator that is integrated in Gowin YunYuan software to expand automatically.

6Operation Modes

6.1 Read Mode

B-SRAM supports two read modes: Pipeline mode and bypass mode. Users are advised to employ the output registers to help increase system performance and timing.

Figure 6-1 B-SRAM Logic Structure View



6.2 Write Mode

The write operation requires a clock cycle. The write port data enters input register at the clock edge, and then the data is stored in the memory array.

The write mode supports the following modes:

- Normal mode
- Write-through mode
- Read-before-write mode

6.2.1 Normal mode

Note!

In normal mode, a dummy read cycle is required to change the write operation to a read operation (WRE is changed from 1 to 0). After the dummy cycle, the read data is consistent with the written data.

- By default, when writing to one port, the outputs on that port will not

change, and no data appears on the read port in a write cycle.

- If repeatedly written to the same address, the previously written data will be overwritten.
- In comparison to the bypass mode, the pipeline mode adds one clock cycle latency.

Figure 6-2 Normal Mode - Bypass Mode Timing

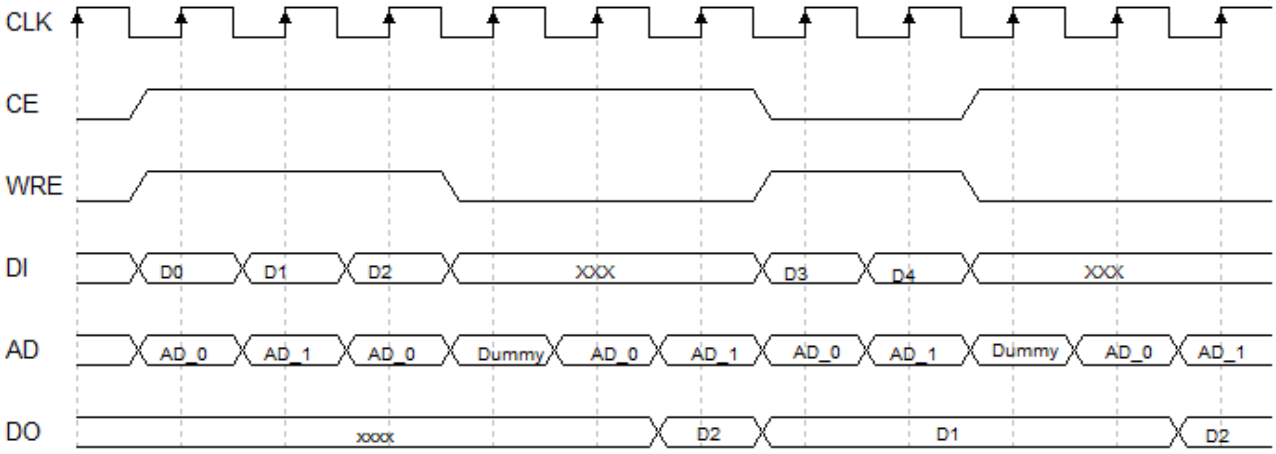
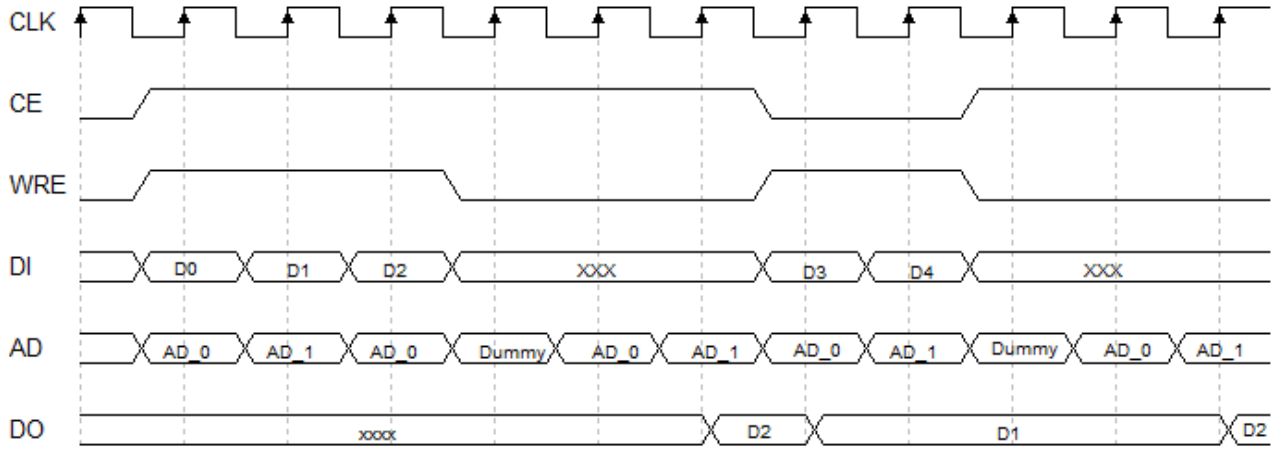


Figure 6-3 Normal Mode - Pipeline Mode Timing



6.2.2 Write-through Mode

In write-through mode, during a write, the output data of the port is updated with the input data. In comparison to the bypass mode, the pipeline mode adds one clock cycle latency.

Figure 6-4 Write Through Mode - Bypass Mode Timing

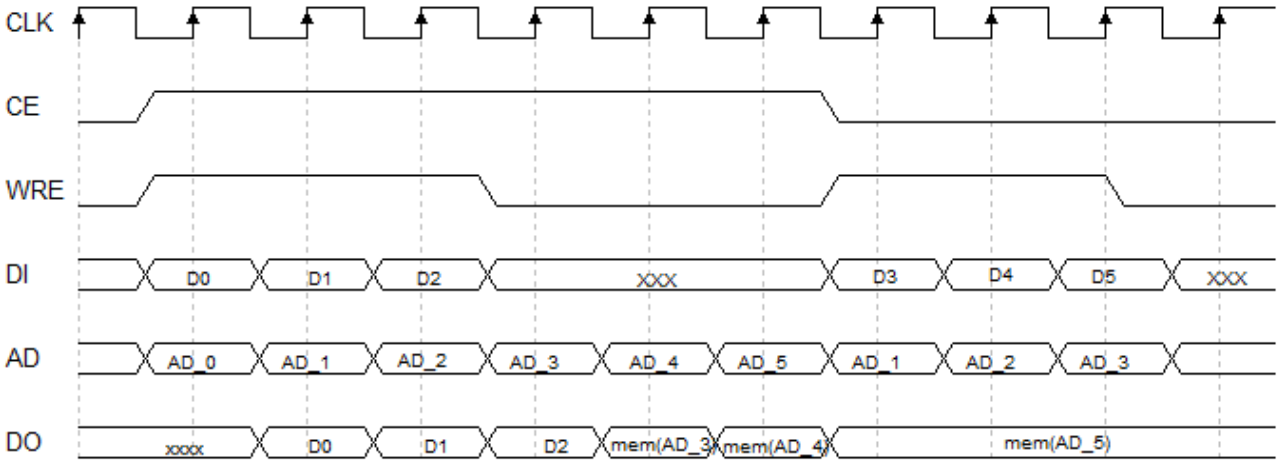
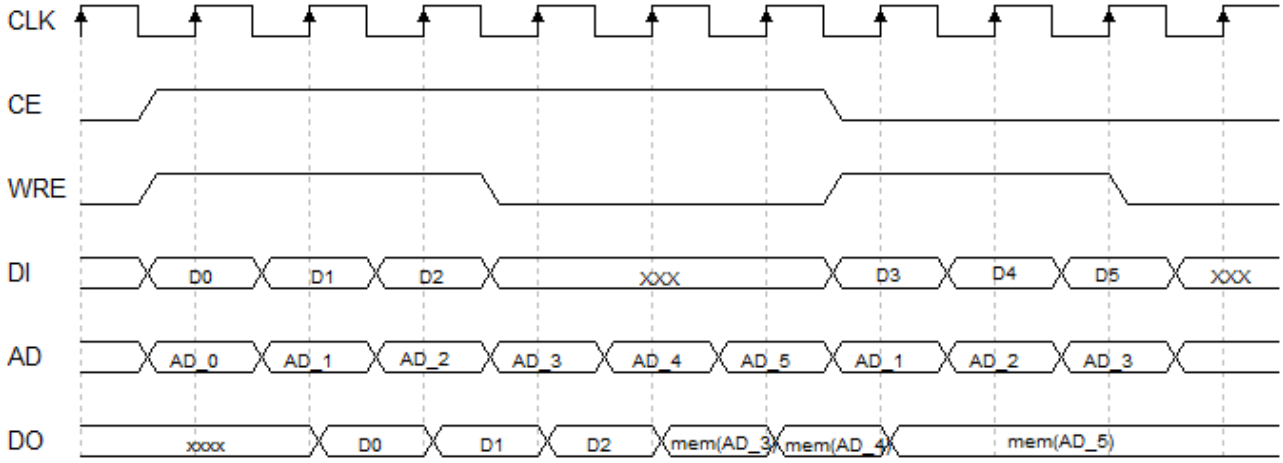


Figure 6-5 Write Through Mode - Pipeline Mode Timing



6.2.3 Read-before-write mode

In the read-before-write mode, during a write, the output data of the port is updated with the existing data stored in the write-address. The new data is then written into the address.

Figure 6-6 Read-before-write Mode - Bypass Mode Timing

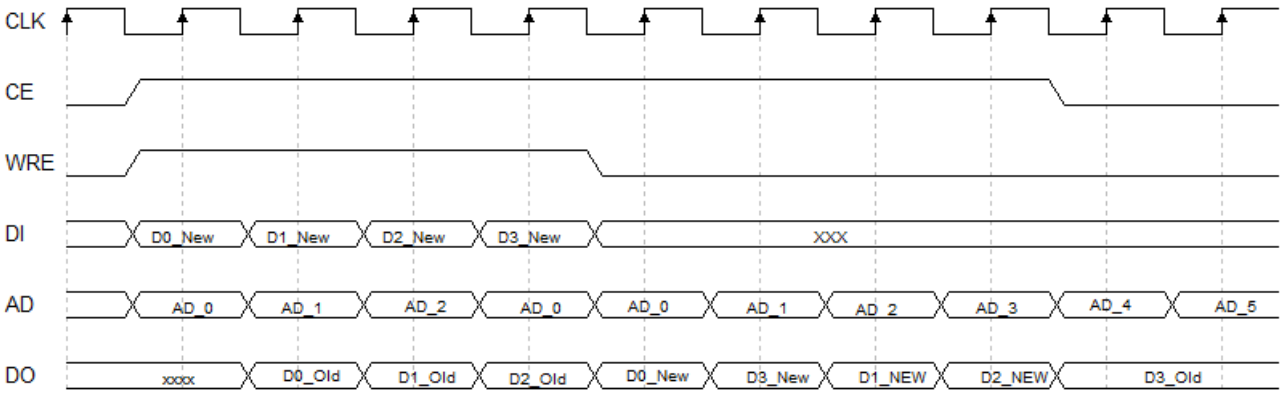
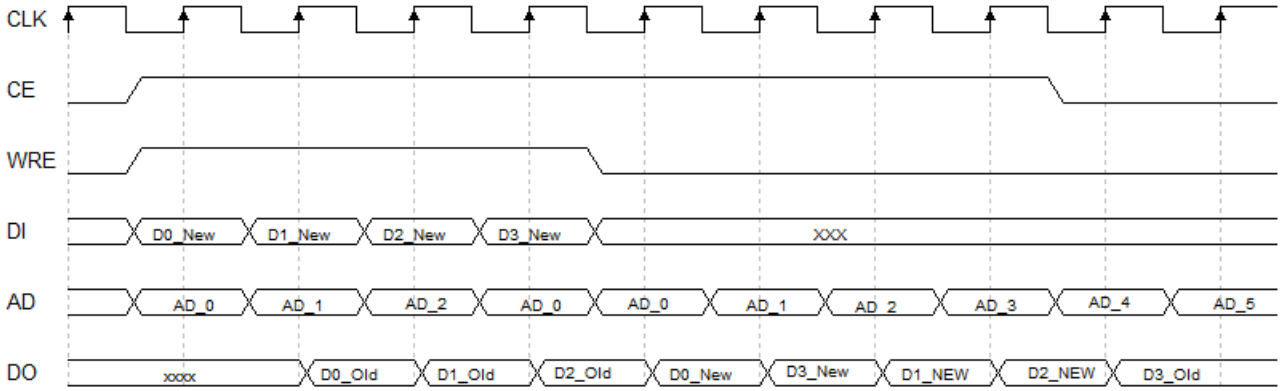


Figure 6-7 Read-before-write Mode - Pipeline Mode Timing



6.3 Conflict Avoidance

Conflict avoidance may occur in the following cases:

- In the Semi-dual port mode and dual port mode, one port reads while the other port writes at the same address;
- In Dual-port mode, port A and port B writes different data to the same address.

Note!

In Dual-port mode, Port A and Port B can read from or write to at the same address.

Please note conflicts and ignore the invalid data, or avoid reading from or writing to the same address at the same time.

6.4 Byte Enable

B-SRAM supports byte-enable, which masks the input data so that only specific bytes of data are written. It is active-high by default. The data can be written if this option is enabled. If not, the data cannot be written.

The low address supports byte-enable. The correspondence between byte-enable, data width, and address depth is shown in Table 6-1.

Table 6-1 Correspondence between Byte-enable, Data Width, and Address Depth

Capacity	Configuration	Address Value	Byte Enable Signal	Data
16K	16K x 1	ad[13:0]	–	DI[0]
	8K x 2	{ad[12:0],1'b0}	–	DI[1:0]
	4K x 4	{ad[11:0],2'b00}	–	DI[3:0]
	2K x 8	{ad[10:0],3'b000}	–	DI[7:0]
	1K x 16	{ad[9:0],2'b00,byte_en[1:0]}	byte_en[0] byte_en[1]	DI[7:0] DI[15:8]
	512 x 32	{ad[8:0],1'b0,byte_en[3:0]}	byte_en[0] byte_en[1] byte_en[2] byte_en[3]	DI[7:0] DI[15:8] DI[23:16] DI[31:24]
18K	2K x 9	{ad[10:0],3'b000}	–	DI[8:0]
	1K x 18	{ad[9:0],2'b00,byte_en[1:0]}	byte_en[0] byte_en[1]	DI[8:0] DI[17:9]

Capacity	Configuration	Address Value	Byte Enable Signal	Data
	512 x 36	{ad[8:0],1'b0,byte_en[3:0]}	byte_en[0] byte_en[1] byte_en[2] byte_en[3]	DI[8:0] DI[17:9] DI[26:18] DI[35:27]

When calling the primitives library directly, refer to Table 6-1 for the address value. When using the IP Core Generator, B-SRAM generates byte-enable port "byte_en" with the user value "byte_en" according to requirements. The software assigns the value to the lower address automatically; please refer to *Gowin IP Core Generator User Guide* for further details.

6.5 Parity Bit Support

All B-SRAMs have built-in parity-bit support. The ninth bit associated with each byte of 18 Kbit B-SRAM, SPX9, SDPX9, and DPX9 can store a parity bit or serve as an additional data bit.

Note!

No parity function is performed on the ninth bit.

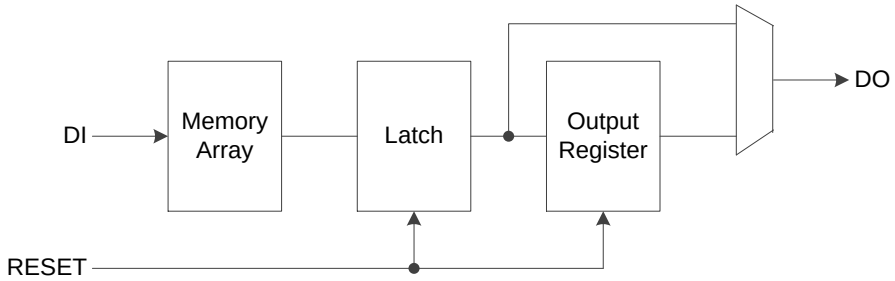
6.6 Power-up Conditions

B-SRAM supports power-on conditions for memory initialization. During power on, the B-SRAMs are in an idle state, and data outputs are always set to 0.

6.7 Output Reset

The output module supports reset and output reset data 0. Figure 6-8 shows the structure view.

Figure 6-8 Output Reset Structure View



The RESET output is 0 when active-high.

RESET supports synchronous reset and asynchronous reset. When you call the primitives library directly, set the parameter "RESET_MODE", please refer to *Gowin FPGA Primitives User Guide* for the details. Select “Reset Mode” on "Customize IP" page using IP Core Generator; please refer to *Gowin IP Core Generator user guide* for the details.

RESET is valid for both latch and output register, so when RESET is enabled, port outputs 0 in both pipeline mode and bypass mode.

Note!

- During the write operation, RESET should be set to 0 (invalid state); Regardless of whether the OCE is valid or not, DO outputs "DO_RAM".
- DO outputs "DO_RAM" regardless of whether OCE is valid or not.

Figure 6-9、Figure 6-10 and Figure 6-11 show the reset timing in different modes. DO_RAM refers to the data in the memory array; DO refers to the output port data.

In pipeline mode:

- When synchronous reset is enabled, DO is reset to 0 at CLK riding edge
- When asynchronous reset is enabled, DO is reset to 0 accordingly.
- When OCE is valid, DO outputs "DO_RAM"
- When OCE is invalid, DO retains the previous output data.

In bypass mode:

- When RESET is valid, DO is reset to 0
- DO outputs "DO_RAM" regardless of whether OCE is valid or not.

Figure 6-9 Reset Timing - Pipeline Mode

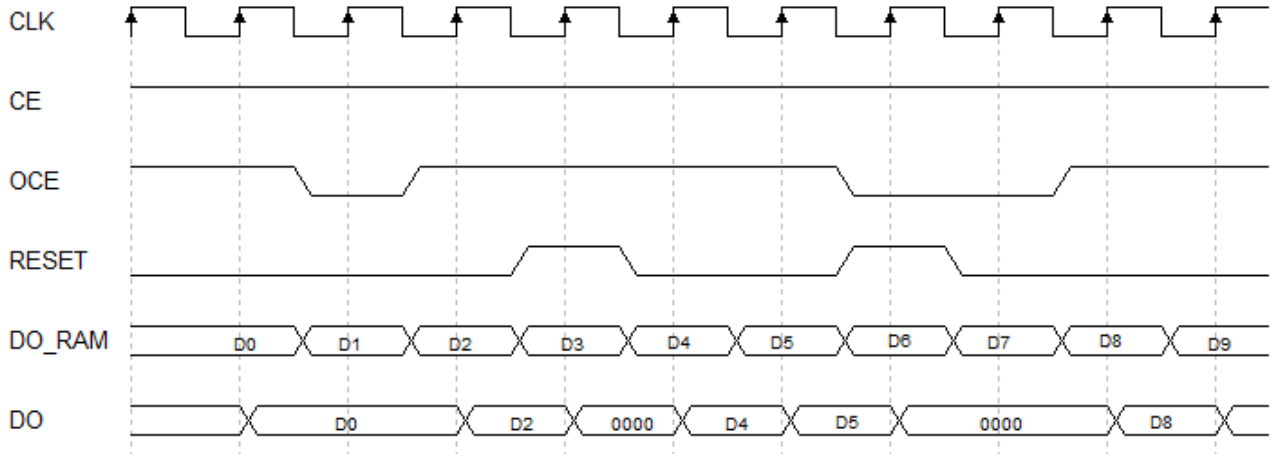


Figure 6-10 Reset Timing - Bypass Mode

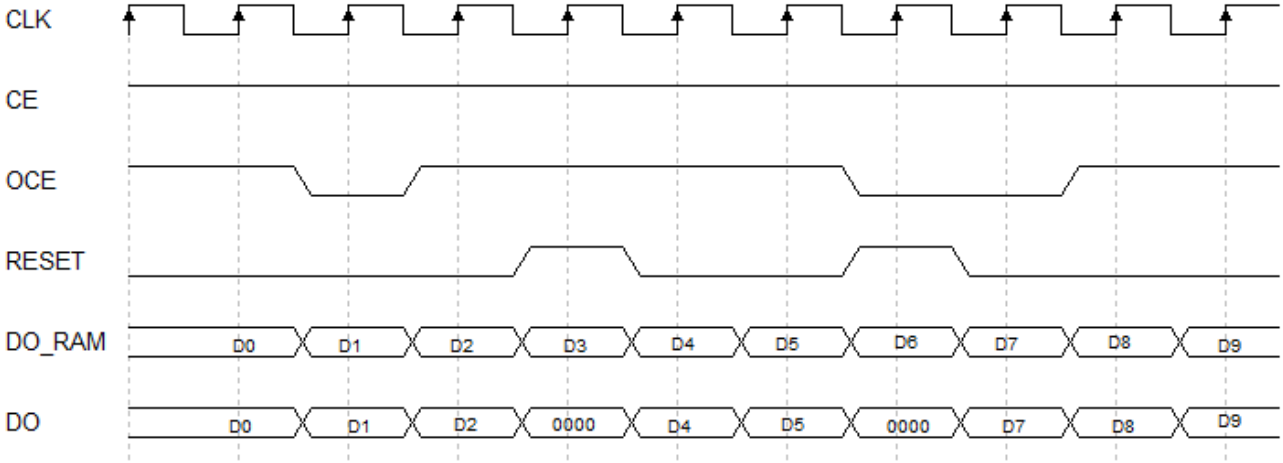
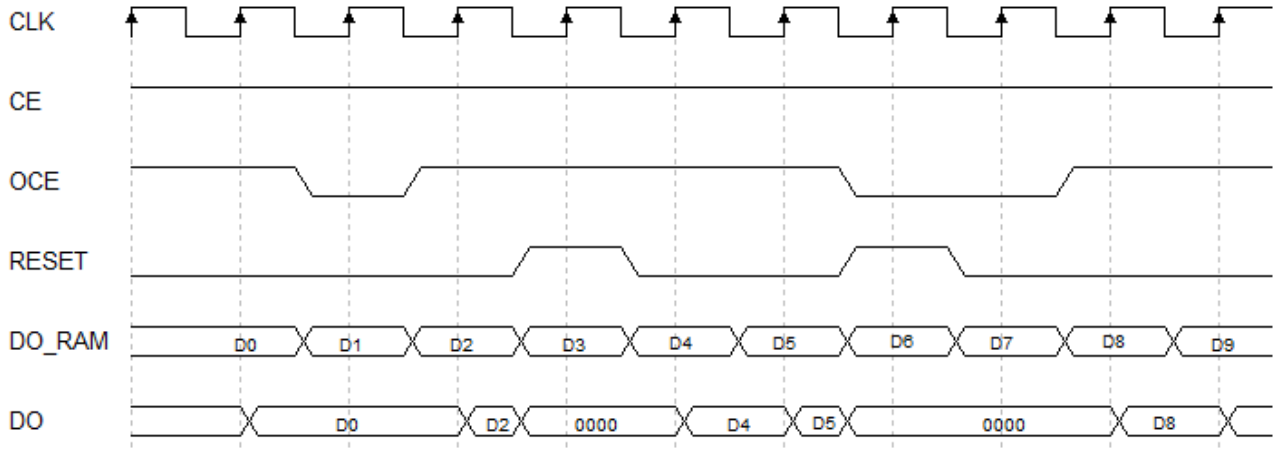


Figure 6-11 Asynchronous Reset Timing - Pipeline Mode



6.8 B-SRAM Location Constraint

Gowin YunYuan software supports B-SRAM location constraint, including the two methods detailed below:

- Gowin Floor Planner drag-on GUI. Please refer to *Gowin Design Constraints Guide* for the details.
- Set in the Physical constraints file CST as follows:

  INS_LOC "sdp_16/bram_sdp_0" R10C23;

  INS_LOC "sdp_16/bram_sdp_0" R10C26;

For the B-SRAM physical location, please refer to the Gowin Floor Planner GUI.

7 B-SRAM Primitives

The B-SRAM primitives file is available in the Gowin YunYuan software installation directory: GOWIN/1.5/Pnr/lib/gwxx. "1.5" is the software version, and "gwxx" indicates the device series, such as gw1n and gw2a.

For further details about B-SRAM primitives, please refer to *Gowin FPGA Primitives User Guide*.

8 Timing Model

To read from or write to the B-SRAM, setup time, hold time, and register output time of the read/write operation of the data/address/control signals is required. Different FPGA products have different timing parameters. For more details about the timing parameters, please refer to the *GW1N series of FPGA Products DataSheet*, *GW1NR series of FPGA Products DataSheet*, *GW2A series of FPGA Products DataSheet*, and *GW2AR series of FPGA Products DataSheet*.

8.1 Timing Parameters

Name	Description
t_{COAD_BSRAM}	Clock to output from read address/data
t_{COOR_BSRAM}	Clock to output from output register

8.2 Timing Features

TBD

Appendix A Operation Notes

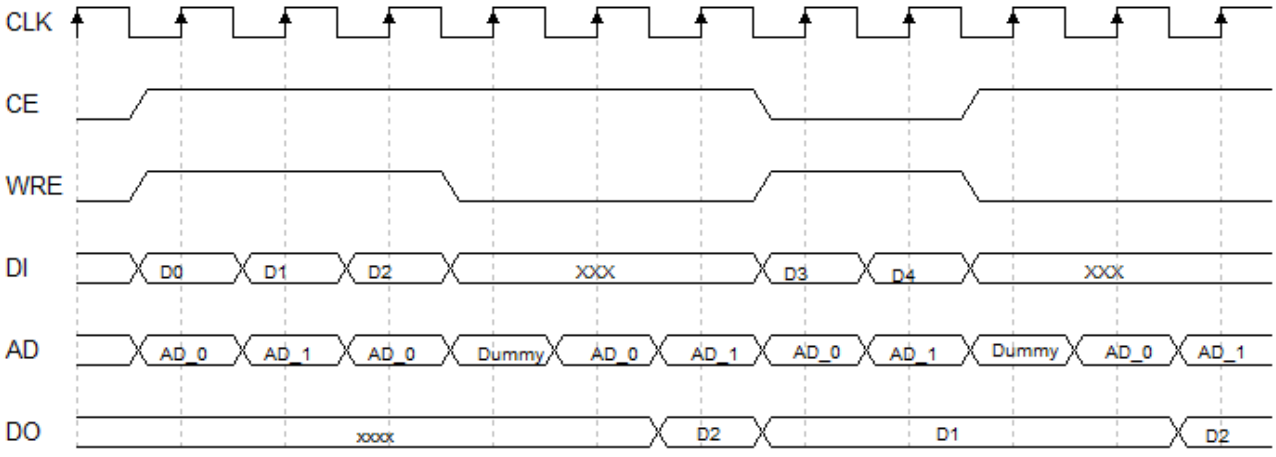
Please refer to the following notes during B-SRAM operation. In the event of improper operation or product limitations, the result may differ.

A.1 Dummy Clock Cycle

In normal mode, when reading from or writing to the same port of B-SRAM, including SP, SPX9, DP, and DPX9, a dummy read cycle is required to change the write operation to a read operation (WRE goes from 1 to 0), as shown in Figure A -1.

In write-through mode and read-before-write mode, no dummy read cycle is required.

Figure A -1Normal Mode - Bypass Mode Timing



A.2 Synchronous Reset

RESET has an effect on the write operation in synchronous reset mode; as such, RESET must not be enabled during the write operation.

The write operation is not affected in asynchronous reset mode.

A.3 Read/write Notes

A.3.1 Write Operation Notes

Table A.1 Write Operation Notes

Mode	Condition	Notes	Remark
SP/SPX9/ SDP/SDPX9/ DP/DPX9	Write port: WRE is 1, when CE changes from 1 to 0	Data will be written to the first address since CE is invalid	CE signal prolongs for one active clock cycle
SDP/SDPX9	Write port: CE is 1, when WREA changes from 1 to 0	Data will be written to the first address since WREA is invalid	WREA signal prolongs for one active clock cycle

A.3.2 Read Operation Notes

Table2 Read Operation Notes

Mode	Data Width	Condition	Notes	Remark
SP/SDP/ DP/ROM	16/32	Read port: WRE is 0, when CE changes from 1 to 0	Data will be read out from the first address since CE is invalid	CE signal prolongs for one active clock cycle
SPX9/SDPX9/ DPX9/ROMX9	18/36			
SDP/ROM	16/32	Read port: CE is 1, when WREB changes from 0 to 1	Data will be read out from the first address since WREB is invalid	WRE signal prolongs for one active clock cycle
SDPX9/ROMX9	18/36			
SP/SDP/ DP/ROM	1/2/4/8	Read port: WRE is 0, when CE changes from 1 to 0	The data that changes with the valid lower-four bit read/write addresses gets on the output port.	The data will be output continuously.
SPX9/SDPX9/ DPX9/ROMX9	9			
SDP/ROM	1/2/4/8	Read port: CE is 1, when WREB changes from 0 to 1		
SDPX9/ROMX9	9			
SP/DP	1/2/4/8	Normal operation mode, read port: CE is 1, WRE changes from 0 to 1	Read the data that changes with the valid lower-four bit read/write addresses and retain it when WRE is invalid	WRE signal prolongs for one active clock cycle
SPX9 / DPX9	9			
SP/DP	1/2/4/8	Read before write and write through operation modes, write port: WRE is 1, when CE changes from 1 to 0	The data that changes with the valid lower-four bit read/write addresses gets on the output port.	The data will be output continuously.
SPX9 / DPX9	9			
SP/DP	16/32	Read before write	Data will be read	CE signal

Mode	Data Width	Condition	Notes	Remark
SPX9/DPX9	18/36	and write through operation modes, write port: WRE is 1, when CE changes from 1 to 0	out from the first address and be retained since CE is invalid	prolongs for one active clock cycle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