Design of Optimized Reversible Binary Adder/Subtractor and BCD Adder

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***Abstract*—Reversible logic has gained the interest of many researchers due to its applicability in emerging low power technologies such as Quantum computing, QCA, optical computing etc., Adders/Subtractors are basic design components of any processor. Optimized design of these adders results in efficient processors. In this work we propose optimized Binary adders/subtractors and BCD adders. The adders/subtractors designed in this work are optimized for Quantum cost and Delay. We also propose a generic design of n-bit adders and subtractors. In this work, we explore the use of Negative control lines for detecting overflow logic of BCD adder which considerably reduces Quantum cost, delay and gate count which result in high speed BCD adder with optimized area which give way to lot of scope in the field of reversible computing in near future.**

Keywords—Negative controlled Toffoli, Reversible logic, Binary adder/subtractor, BCD adder

I. INTRODUCTION

In any digital system, adder/subtractor block is the most essential one. Ripple carry adder and BCD adder are very commonly used in digital systems. Combinational logic circuits dissipate heat in an order of kTln2 joules for every bit of information that is lost [1]. Bennet showed that kTln2 energy dissipation would not occur, if a computation were carried out in a reversible way [2]. An operation is said to be physically reversible if it converts no energy to heat and produces no entropy [3]. A logic circuit is said to be reversible if it computes a bijective (one-to-one and onto) logic functions [4] and has neither feedback nor fan-out allowed [5].

In present day world as the size of the technology is scaling down for the purpose of miniaturization and portability, there is a need for a low power consumption circuits with optimized area. n*n Toffoli is a commonly used reversible gate in digital circuits with positive control lines. In this work, we are using negative controlled Toffoli gates to implement adder block. Incorporating negative control lines leads to smaller circuits with respect to the number of gates i.e., reduction with respect to gate count as well as quantum cost and the run-time of the synthesis can be improved [6, 7].

In this paper, we have designed a 1-bit reversible binary full adder and subtractor using positive and negative controlled Toffoli gates with zero garbage output and have extended the same to 4-bit reversible binary full adder and subtractor with optimized Quantum cost compared to previous works. On the same line, a BCD reversible adder design has been proposed with Quantum cost much lesser than the previous work using negative controlled Toffoli gates and proposed binary full adder circuit.

II. PRELIMINARIES

A. Reversible Logic

A Reversible gate has same number of input and output lines i.e., for each input pattern there should be a unique output pattern [5, 8]. A reversible circuit consists only of reversible gates with no fan-out or feedback. Reversible hardware computation is very much essential in areas such as quantum computing, low power design, nanotechnology, optical information processing, and bioinformatics. If a reversible gate has n-inputs, and hence n-outputs, then we call it an n*n reversible gate.

Some of the reversible gates are NOT gate, CNOT / FEYNMAN gate, TOFFOLI gate, FREDKIN gate and PERES gate. Among them the most popular one is the TOFFOLI gate. An n*n Toffoli gate given in Fig 1, maps the input vector [n_1, n_2, n_3… n_k] to the output vector [O_1,O_2,O_3…O_k], where $O_j=n_j$ (for j=1, 2... k-1) and $O_k=n_1n_2….n_{k-1} \oplus n_k$. The first (n-1) bits are called control lines and last bit is called target line. Here the target bit is toggled only when all control lines are 1. The Quantum Cost of Positive controlled Toffoli gate is 5 and the delay associated with it is 5Δ.

A negative controlled Toffoli gate has one or more negative control lines. In this case toggling happens at target bit if all negative control lines are at logic 0 and if any positive control, it should be at logic 1. The Quantum Cost of Negative controlled Toffoli gate is 6 with a delay of 6Δ. A 3-bit negative controlled Toffoli is as shown in Fig 2.

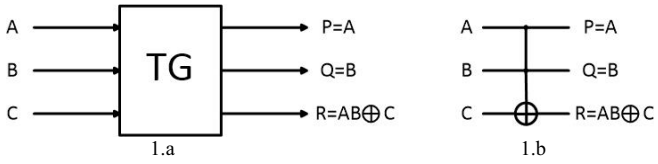

Fig. 1. a: Positive Controlled Toffoli gate (TG)
b: TG Symbol

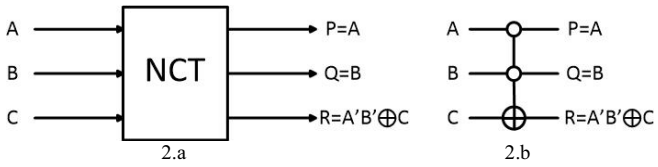

Fig. 2. a: Negative controlled Toffoli (NCT) gate
b : NCT symbol

B. Literature Survey

Design of combinational block using the concept of negative control lines is an emerging trend in VLSI domain. This is because of its capability of replacing series of gates and thereby reducing the area, gate count and as well as power consumption. Various synthesis and design techniques have been proposed using negative control lines. [6] proposes a post-synthesis DD based optimization technique using negative control lines.

Exact synthesis algorithms give minimal circuit for a given function. Negative control lines are used in [7] to optimize this algorithm. But computational time is large and applicable only to small functions. Optimization based on template matching technique is another method proposed in [9] which defines set of rules to efficiently replace NCT in place of series of PCT, thus reducing gate count, area and power consumption. [10] proposes a reversible binary and BCD adder circuit with optimized Ancilla inputs and garbage outputs.

Design of reversible binary adder/subtractor and BCD adders have been proposed in [15] with a goal of optimizing number of ancilla input bits and the garbage outputs. [13] proposes a modular synthesis method to realize a reversible BCD adder circuit. But delay of the circuit is not taken into account. In [17] BCD adder has been designed using New gates and FG gates. They have considered only the garbage outputs. Quantum cost, delay and ancilla inputs have not been discussed. Another BCD adder design has been proposed in [15] using five HNG gates, one Peres gate, one Feynman gate and one SCL gate. They have also not considered quantum cost into account.

In this paper, we have proposed a new 1-bit reversible adder and subtractor with optimized quantum cost consisting of only Toffoli gates. The proposed design is then used further to construct a 4-bit binary full adder/subtractor and BCD adder. The parameters such as quantum cost, delay, ancilla inputs and garbage outputs has been considered and compared with the existing designs. All the designs have been generalized to n-bits and compared with the previous works.

III. DESIGN

A. 1-bit Reversible Full Adder

A 1-bit reversible full adder has been designed using only n*n positive controlled Toffoli gates as shown in Fig 3. 2*2 Toffoli gate is generally called CNOT gate / Feynman gate. The proposed design is simple and has a gate count of 4 with 0 garbage output.

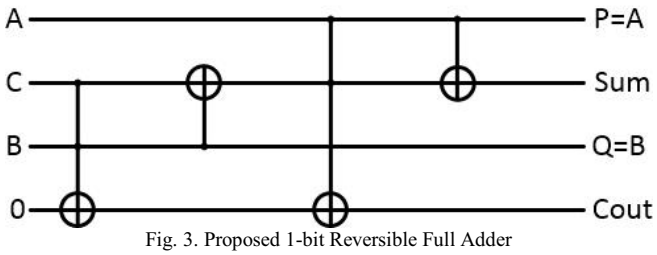

Fig. 3. Proposed 1-bit Reversible Full Adder

B. 4-bit Reversible Full Adder

4-bit reversible ripple carry adder has been designed using four 1-bit reversible adders as shown in Fig 4. For each stage of input, 1 ancilla input is required producing no garbage output. The quantum cost of the proposed design is 48 with a delay of 40Δ. This is better than the previous works that has been done. When compared to [15, 19], the quantum cost has been reduced by 18.75% for an 8-bit adder. The block diagram representation of the proposed 4-bit reversible full adder design is as shown in Fig 5 and in the rest of the paper it will be called by the name 'NAFA'.

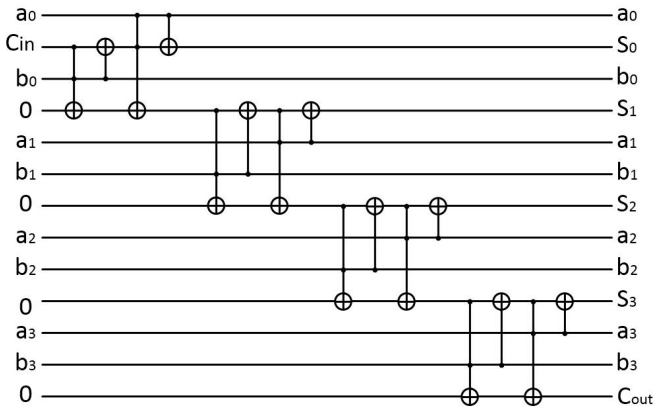

Fig. 4. Proposed 4-bit Reversible Full Adder Design

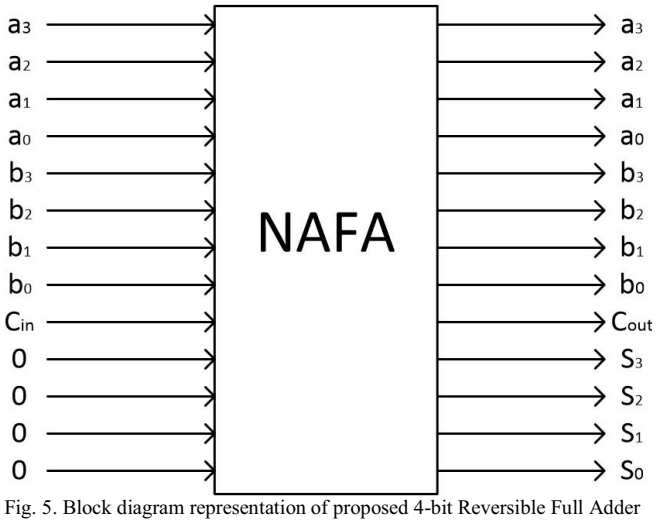

Fig. 5. Block diagram representation of proposed 4-bit Reversible Full Adder

C. 4-bit BCD Adder Design using NAFA

Conventionally BCD adders are constructed using Full Adder circuit with an overflowing detector circuit. In this design we have proposed a 4-bit reversible BCD adder using NAFA as shown in Fig 6. The overflowing detector circuit has been designed using two 3*3 negative controlled Toffoli gates and a positive controlled Toffoli gate. The use of negative logic reduces the gate count and hence aids the requirement. In this design 2 NAFA full adders are used to realize the reversible BCD adder.

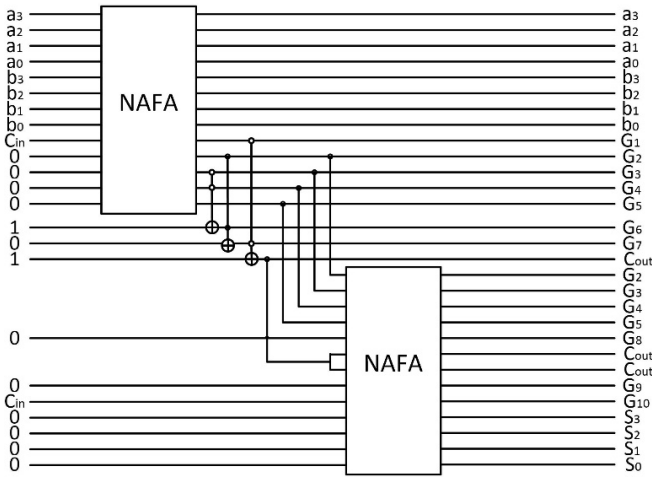

Fig. 6. Proposed 4-bit Reversible BCD adder design

D. 1-bit Reversible Full Subtractor

A 1-bit reversible full subtractor is designed using n*n positive and negative controlled Toffoli gates as shown in Fig 7. The circuit flow remains same when compared to proposed reversible full adder. All parameters such as ancilla inputs, garbage outputs, QC, delay and the gate count remains the same. The only change is that, we replace positive controlled Toffoli gate in 2nd stage by a Toffoli gate consisting of both positive and negative control lines. This gate has the same quantum cost as positive Toffoli.

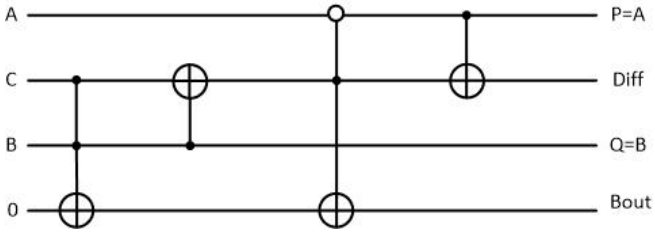

Fig. 7. Proposed 1-bit Reversible Full Subtractor

E. 4-bit Reversible Full Subtractor

4-bit reversible full subtractor has been designed using four 1-bit reversible subtractors as shown in Fig 8. For each stage of input, 1 ancilla input is required producing no garbage output. The quantum cost of the proposed design is 48 with a delay of 40Δ, which is same as that of adder design. Hence, there is no overhead for reversible subtractor when compared to reversible adder design. QC of the proposed design is better than the existing works. When compared to [15], the quantum cost has been reduced by 20.83% for a 4-bit subtractor. The block diagram representation of the proposed 4-bit reversible full subtractor design is as shown in Fig 8 and in the rest of the paper it will be called by the name 'NAFS'.

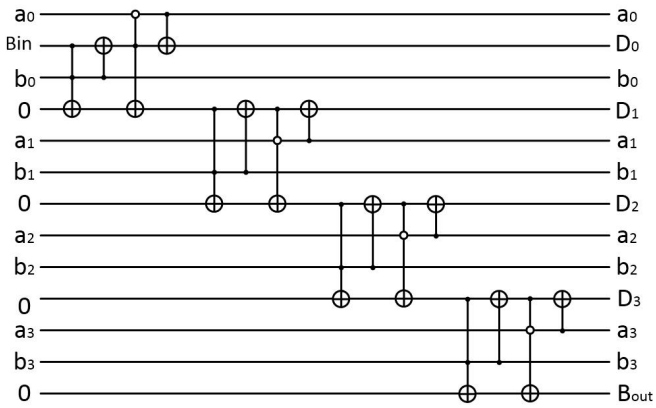

Fig. 8. Proposed 4-bit Reversible Full Subtractor Design

IV. METHODOLOGY

A. Binary Full Adder

The methodology adapted is to ripple the carry through each stage of full adder circuit. The proposed 1-bit full adder circuit has been cascaded to work as a 4-bit reversible full adder with a Quantum cost of 48 and delay of 40Δ. The delay calculation process has been shown diagrammatically shown in Fig 7. According to the design, for each group of 2*2 and 3*3 Toffoli gate, delay is found to be

$$\Delta = \max(1\Delta, 5\Delta) = 5\Delta$$

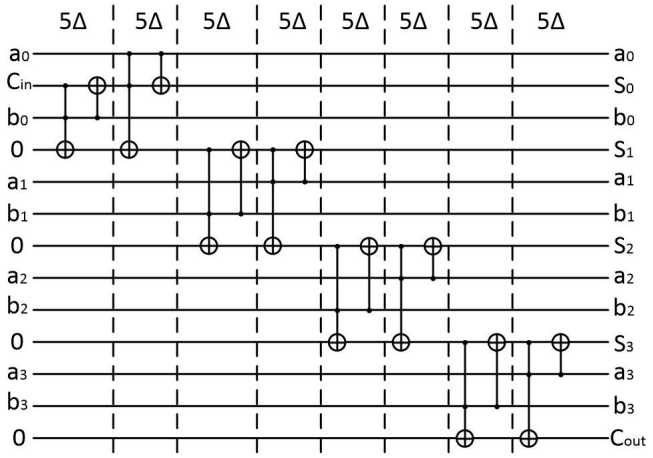

Fig. 9. Delay Calculation in 4-bit Reversible Full Adder design

Since there are 8 such pairs, the total delay for a 4-bit reversible full adder is found to be 40Δ. The general expression to find delay for an n-bit reversible binary adder is as shown below:

$$\Delta_{\text{total}} = \sum_{i=1}^{2n} \max\,(1\Delta, 5\Delta)$$

B. BCD Adder

BCD adder using reversible logic has been designed using binary full adders and the Toffoli gates with positive and negative control lines. A binary coded decimal is a form of number system in which every four bits of a number is represented by its equivalent value. For example, a decimal number 45 is represented as 0100 0101 in BCD system. This makes things simple and facilitates the logic designer to understand the logic. While designing a combinational circuit using BCD logic, we may need to perform different operations on it such as addition, subtraction, etc. While performing any operation, there may be chances of overflowing the range of the number system. In such a case, a detector and corrector circuit needs to be present. During BCD addition if there is any overflow, the logic to correct is to add 6 (0110) to the resulting data. In this proposed design, we have used cascade of two negative controlled Toffoli and a positive controlled Toffoli gate to detect the overflow and have used another 4-bit reversible binary adder (NAFA) to correct it by adding 6 (0110) to the output of first NAFA. By this the quantum cost has been found to be 113 with gate count of 35 and delay of 97Δ.

C. Binary Full Subtractor

The methodology adapted is similar to ripple carry adder. Here borrow is propagated through each stage of full subtractor circuit. The proposed 1-bit full subtractor has no overhead when compared to proposed adder. QC and delay remains same i.e., a Quantum cost of 48 and delay of 40Δ. Here we utilize the property of negative controlled Toffoli gate to implement full subtractor with no overhead.

V. RESULTS AND DISCUSSIONS

A. Binary Full Adder

Proposed n-bit reversible binary full adder has the quantum cost of 12n, delay of 10n, 4n ancilla inputs and 0 garbage outputs. When compared to [15, 19], the quantum cost of the proposed design has been reduced by 18.75% for an 8-bit adder. The delay has been improved by 7.5% when compared to [18]. Table I gives the comparison of n-bit full reversible binary full adder. Table II gives the percentage improvement in quantum cost for different bits.

TABLE I. COMPARISON OF N-BIT REVERSIBLE FULL ADDER

	Ancilla Inputs	***Garbage Outputs***	***Quantum Cost***	***Delay Δ***
[18]	0	0	17n-6	10n+6
[19]	0	0	17n-22	15n-6
[15]	0	0	15n-6	9n+1
Proposed	4n	0	12n	10n

TABLE II. QUANTUM COST COMPARISON OF N-BIT REVERSIBLE FULL ADDER

Bits	***[19]***	***[15]***	***Proposed***	***% Improvement. w.r.t [19]***	***%Improvement w.r.t [15]***
8	114	114	96	18.75	18.75
16	250	234	192	30.20	21.87
32	522	474	384	35.93	23.43
64	1066	954	768	38.80	24.21
128	2154	1914	1536	40.23	24.61
256	4330	3834	3072	40.95	24.80
512	8682	7674	6144	41.30	24.90

B. Reversible BCD Adder

TABLE III. COMPARISON OF 4-BIT REVERSIBLE BCD ADDER

	Ancilla Inputs	***Garbage Outputs***	***Quantum Cost***	***Delay Δ***
[10]	68	72	440	Not Mentioned
[11]	28	24	220	Not Mentioned
[12]	16	16	676	Not Mentioned
[13]	56	64	336	Not Mentioned
[14] (Design 3*)	8	24	412	Not Mentioned
[15] (Work 3*)	4	3	280	228
[16]	6	10	Not Mentioned	Not Mentioned
[17]	17	22	Not Mentioned	Not Mentioned
Proposed	13	10	113	97

* In [14] 6 designs and in [15], 4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here.

The proposed BCD adder using reversible binary full adder has better quantum cost when compared to previous works. The results of all the previous works and our proposed

design have been summarized in Table III. The percentage improvement in quantum cost when compared to [11] is 94.69% and delay improvement is 135.05% compared to [15]. Though the ancilla inputs and garbage outputs are more compared to [15], the quantum cost and delay has been optimized to a greater extent. Table IV gives the comparison of n-bit reversible BCD adder.

TABLE IV. COMPARISON OF N-BIT REVERSIBLE BCD ADDER

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[10]	17n	18n	110n	Not Mentioned
[11]	7n	6n	55n	Not Mentioned
[12]	4n	4n	169n	Not Mentioned
[13]	14n	16n	84n	Not Mentioned
[14] (Design 3*)	2n	6n	103n	Not Mentioned
[15] (Work 3*)	n	n-1	70n	57n
Proposed	$3n+\frac{n}{4}$	$2n+\frac{n}{2}$	$28n+\frac{n}{4}$	$24n+\frac{n}{4}$

*In [14] 6 designs and in [15], 4 works on BCD adders are proposed based on varying parameters such as Ancilla inputs, garbage outputs, quantum cost and the delay. Among them, the design with minimum Ancilla inputs and garbage outputs are compared here.

C. Binary Full Subtractor

n-bit reversible binary full subtractor proposed in this paper has the quantum cost of 12n, delay of 10n, 4n ancilla inputs and 0 garbage outputs with a gate count of 4n. The quantum cost has been reduced by 27.08% when compared to [15] for an 8-bit subtractor. The delay has been improved by 20% when compared to [20]. Table V gives the comparison of 4-bit reversible binary full subtractor, followed by an n-nit comparison in table VI. Table VIII gives the percentage improvement in quantum cost for different bits.

TABLE V. COMPARISON OF 4-BIT REVERSIBLE FULL SUBTRACTOR

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[15]	1	1	58	38
[20]	1	1	68	48
[21]	0	0	87	77
[22]	0	0	63	53
Proposed	16	0	48	40

TABLE VI. COMPARISON OF N-BIT REVERSIBLE FULL SUBTRACTOR

	Ancilla Inputs	*Garbage Outputs*	*Quantum Cost*	*Delay Δ*
[15]	1	1	16n-6	9n+2
[20]	1	1	20n-12	12n
[21]	0	0	29n-29	26n-27
[22]	0	0	18n-9	15n-7
Proposed	4n	0	12n	10n

TABLE VII. QUANTUM COST COMPARISON OF N-BIT REVERSIBLE FULL SUBTRACTOR

Bits	*[15]*	*[22]*	*Proposed*	*% Improvement. w.r.t [15]*	*%Improvement w.r.t [22]*
8	122	135	96	27.08	40.62
16	250	279	192	30.20	45.31
32	506	567	384	31.77	47.65
64	1018	1143	768	32.55	48.82
128	2042	2295	1536	32.94	49.41
256	4090	4599	3072	33.13	49.70
512	8186	9207	6144	33.23	49.85

VI. CONCLUSIONS

In this work, we have proposed a reversible binary adder and subtractor design with optimized quantum cost and delay compared to previous work in literature and using this adder, an optimized reversible BCD adder in terms of Quantum cost, delay and garbage outputs have been designed using reversible gate libraries made in Verilog model and functionally verified using Xilinx ISE tool. The use of negative control lines in the design for detecting overflow logic of BCD adder has considerably reduced delay and gate count which result in high speed BCD adder with optimized area. Thus we conclude that the use of Negative control lines reduces the gate count and hence area, which gave way to lot of scope in the field of reversible computing in near future.

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