EE 2361 - Final Exam
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1. a. True
   b. False, only math, logic, & bit shifts change status bits
   c. False, PC contains the address of instruction at current time
   d. False, 2 if true, 1 if false.
   e. False, W15 is used for SP.
   f. False, high prescaler = lower resolution.
   g. False, ISR occurs synchronously, but an interrupt is asynchronous.
   h. False, ISR's don't take parameters / return values.
   i. False, the default priority lvl is 4 of 7.
   j. True
   k. False, PIC24 architectures are usually 16-bit.
   l. False, I2C is synchronous.
   m. True
   n. False, address frame contains slave address.
   o. False, I2C supports multiple masters but they can't communicate directly.
   p. True
   q. True
   r. True
   s. False, not global variables
   t. True

2. a. MOV W4, W2

b. MOV.B [W6++], [W7]

3. a. #1: Sums even numbers between 20 to 0 by multiplying each number by 2 before it sums.

#2: Does the same but sums the numbers first, then multiplies everything by 2 after.

b. #1: $(5 \cdot 10) - 1 = 49$

#2: $(4 \cdot 10) - 1 + 1 = 40$

c. The second loop takes less cycles, so #2.

4. a. Copies all values from Bar to Aar arrays

b.

```
.bss
Barr: .space 20
Aarr: .space 20
.text
_main:
    MOV #10, W3
    MOV #Bar, W10
    MOV #Aar
LOOP:
    MOV [W10++], [W11++]
    DEC WREG3
    BRA NZ, LOOP
END_LOOP:
    MOV...
```

5. a. W3 [0x00AA]
W4 [0x00AA]
W5 [0x0810]
W15 [0x0812]
0x0810 [0x0A07]
0x0812 [0x5678]
0x0814 [0x9ABC]

b. PC [0x01120A]
W3 [0x00AB]
W15 [0x0814]
0x0814 [0x120A]
0x0816 [0x0001]
0x0818 [0x00AB]
0x081A [0x00CD]

C. MSEC @ 0x01200A
PC [0x01200A]
W1 [0x081A]
W3 [0x5678]
W15 [0x081C]
0x0818 [0x100A]
0x081A [0x0001]
0x081C [0x9ABC]

6. 64 PRE

$\left[\frac{1}{8\text{MHz}} \cdot 64\right] \times 16{,}000 = \boxed{128\ \text{ms}}$

7. a.

$U1BRG = \frac{Fcy}{16 \cdot BR}$ when BRGH = 0

$= \frac{1}{16 \cdot BR}$

≈ 2.25

$= 2 \rightarrow$ 8.59% error

U1BRG when BRGH = 1

$= \frac{1 \cdot 10^6}{16 \cdot 19200} = 12 \rightarrow$ 0.159% error

$\boxed{U1BRG = 12}$

$\boxed{BRGH = 1}$

b.