

EXAMPLE: SCOREBOARDING (in-order issue, out-of-order completion)

i1: $R4 \leftarrow R0 * R2$
i2: $R6 \leftarrow R4 * R8$ RAW with i1
i3: $R8 \leftarrow R2 + R12$ WAR with i2
i4: $R4 \leftarrow R14 + R16$ WAW with i1

Pipeline architecture

mult1 six cycle latency
mult2 six cycle latency
add one cycle latency
shift one cycle latency

cycle 1

instruction status

i1

i2

i3

i4

issue

functional unit status

shift

mult1

mult2

add

Ua

op

Fi

Fj

Fk

Qj

Qk

Rj

Rk

0

1

i1

R4

R0

R2

?

?

1

1

0

0

register result status

R0

R2

R4

R6

R8

R10

R12

R14

R16

0

0

mult1

0

0

0

0

0

0

cycle 2

instruction status

i1

i2

i3

i4

dispatch

issue

functional unit status

shift

mult1

mult2

add

Ua

op

Fi

Fj

Fk

Qj

Qk

Rj

Rk

0

1

i1

R4

R0

R2

?

?

1

1

1

i2

R6

R4

R8

mult1

?

0

1

0

register result status

R0

R2

R4

R6

R8

R10

R12

R14

R16

0

0

mult1

mult2

0

0

0

0

0

cycle 3

instruction status	i1	exec(1)
	i2	issue
	i3	issue
	i4	

functional unit status	Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	1	i1	R4	R0	R2	?	?	1	1
mult2	1	i2	R6	R4	R8	mult1	?	0	1
add	1	i3	R8	R2	R12	?	?	1	1

register result status	R0	R2	R4	R6	R8	R10	R12	R14	R16
	0	0	mult1	mult2	add	0	0	0	0

cycle 4

instruction status

i1

i2

i3

i4

exec(2)

issue

dispatch

functional unit status

shift

mult1

mult2

add

Ua

op

Fi

Fj

Fk

Qj

Qk

Rj

Rk

0

1

i1

R4

R0

R2

?

?

1

1

1

i2

R6

R4

R8

mult1

?

0

1

1

i3

R8

R2

R12

?

?

1

1

register result status

R0

R2

R4

R6

R8

R10

R12

R14

R16

0

0

mult1

mult2

add

0

0

0

0

cycle 5

instruction status	i1	exec(3)
	i2	issue
	i3	exec
	i4	

functional unit status	Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	1	i1	R4	R0	R2	?	?	1	1
mult2	1	i2	R6	R4	R8	mult1	?	0	1
add	1	i3	R8	R2	R12	?	?	1	1

register result status	R0	R2	R4	R6	R8	R10	R12	R14	R16
	0	0	mult1	mult2	add	0	0	0	0

cycle 6 no change

cycle 7 no change

cycle 8 no change

cycle 9

instruction status	i1	write
	i2	dispatch
	i3	write
	i4	issue

functional unit status	Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	0								
mult2	1	i2	R6	R4	R8	mult1	?	1	1
add	1	i4	R4	R14	R16	?	?	1	1

register result status	R0	R2	R4	R6	R8	R10	R12	R14	R16
	0	0	add	mult2	0	0	0	0	0