cycle 4

instruction status

i1	exec(2)
i2	issue
i3	dispatch
i4	

functional unit status

	Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	1	i1	R4	R0	R2	?	?	1	1
mult2	1	i2	R6	R4	R8	mult1	?	0	1
add	1	i3	R8	R2	R12	?	?	1	1

register result status

R0	R2	R4	R6	R8	R10	R12	R14	R16
0	0	mult1	mult2	add	0	0	0	0

i1 continues exec.
i2 is stalled
i3 is executed
i4 blocked

cycle 5

instruction status

i1	exec(3)
i2	issue
i3	exec
i4	

functional unit status

	Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	1	i1	R4	R0	R2	?	?	1	1
mult2	1	i2	R6	R4	R8	mult1	?	0	1
add	1	i3	R8	R2	R12	?	?	1	1

register result status

R0	R2	R4	R6	R8	R10	R12	R14	R16
0	0	mult1	mult2	add	0	0	0	0

i1 continues exec.
i2 is stalled
i3 cannot write because $F_k(i2) = F_i(i3)$ => WAR

cycle 6 no change
cycle 7 no change
cycle 8 no change

cycle 9

instruction status

i1	write
i2	dispatch
i3	write
i4	issue

functional unit status

	Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	0								
mult2	1	i2	R6	R4	R8	mult1	?	1	1
add	1	i4	R4	R14	R16	?	?	1	1

register result status

R0	R2	R4	R6	R8	R10	R12	R14	R16
0	0	add	mult2	0	0	0	0	0

After cycle 8:

i1 completes exec and starts write
- mult1 is cleared
- $R_j(i2)$ is set to 1

=> i2 is dispatched
i3 starts write
- add is replaced with i4
- P_8 is reset

i4 is issued