EXAMPLE: SCOREBOARDING (in-order issue, out-of-order completion)

i1: R4<-R0*R2

i2: R6<-R4*R8 RAW with i1

i3: R8<-R2+R12 WAR with i2

i4: R4<-R14+R16 WAW with i1

Pipeline architecture

mult1 six cycle latency mult2 six cycle latency add one cycle latency shift one cycle latency

cycle 1										
nstruction status	i1	issue]							
	i2		1							
	i3		1							
	i4		1							
			•							
functional unit status		Ua	op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	shift	0						1.5		
	mult1	1	i1	R4	RO	R2	?	3	(1	1)
	mult2	0				Ĭ				
	add	0								
register result status	RO	R2	R4	R6	R8	R10	R12	R14	R16	
	0	0	mult1	0	0	0	0	0	0	

which can be dispatched

Moreover R = 0 = is can be

ssued

and P4=0 => is an 4e

			1 1						
i1	dispatch	-> Was	Jopa.						
i2	issue	1							
i3		1							
i4									
		-							
	Ua	oρ	F	Fj	Fk	Qj	Qk	Rj	Rk
shift	0								
mult1	1	11	R4	RO	R2	?	?	1_	1
mult2	1	12	R6	R4	R8	mult1	1.7	(0	1)
add	0								
RO	R2	R4	R6	R8	R10	R12	R14	R16	
0	0	mult1	mult2	0	0	0	0	0	
	i2 i3 i4 shift mult1 mult2 add	i2 issue i3 i4 Ua shift 0 mult1 1 mult2 add 0 R0 R2	i2 issue i3 i4 Ua op shift 0 mult1 1 i1 mult2 add 0 R0 R2 R4	i2 issue i3 i4 Ua op Fl shift 0 Fl Rd	12	12	12	13	12

P8=0 => i3 1s issued

i1 stents execution

cycle 3										
nstruction status	(1	exec(1)	1							
	i2	issue								
	i3	issue	1							
	14									
functional unit status		Ua	ор	Fi	Fj	Fk	Qj	Qk	Rj	Ak
	shift	0			,					-
	mult1	1	i1	R4	RO	R2	?	?	1	1
	mult2	1	12	R6	R4	R8	mult1	?	0_	1
	add	1	i3	R8	R2	R12	?	7	(1	1
register result status	RO	R2	R4	R6	R8	R10	R12	R14	R16	
	0	0	mult1	mult2	add	0	0	0	0	1

is continues exec.

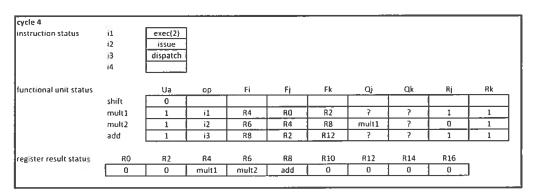
is is still stalled, as R; = O(RAW)

is is obspatched

is count be issued for two

reasons:

1) A to (no unit fee)



cycle 5	•									
instruction status	11	exec(3)								
	12	issue								
	i3	exec								
	i4									
functional unit status		Ua	ор	Fi	Fji	Fk	Qj	Qk	Rj	Rk
	shift	0								
	mult1	1	i1	R4	RO	R2	?	?	1	1
	mult2	1	i2	R6	84	(R8)	mult1	?	0	1
	add	1	+3	R8 /	R2	R12	?	?	1	1
				-						
register result status	RO	R2	₽4	R6	R8	R10	R12	R14	R16	
	0	0	mult1	mult2	add	0	0	0	0	1

cycle 6 no change cycle 7 no change cycle 8 no change

cycle 9		<u> </u>								
instruction status	īI	write	1							
	i2	dispatch	1							
	i3	write	1							
	14	issue								
			_							
functional unit status		Ua	ор	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	shift	0								
	mult1	0								
	mult2	1	12	R6	R4	R8	mult1	?	(1)	~ 1.
	add	1	14	R4	R14	R16	?	.?	1	1
register result status	RO	R2	R4 -	R6	RS	R10	R12	R14	R16	
,	0	0	add	mult2	0	G	0	0	0	Ì
			1		1 Cod					•

is continues exec. iz is stalled is is executed in blocked

is continues exec. 13 comet write because $F_{K}(i2) = F_{i}(i3) = > WAR$

After cycle 8:

i1 completes exect and stants write

(... mult 1 is cleared
... R; (i2) is set to 1

i2 is dispatched
i3 stants write
... add is replaced will is
... P8 is reset

i4 is issued