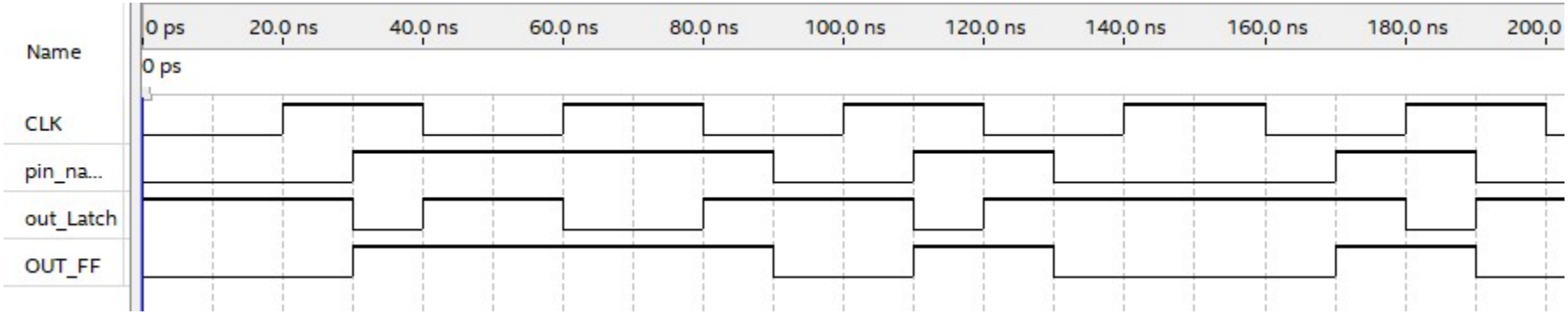
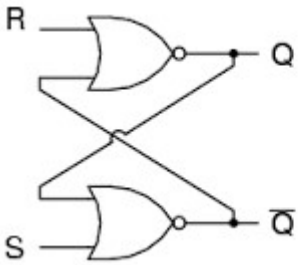
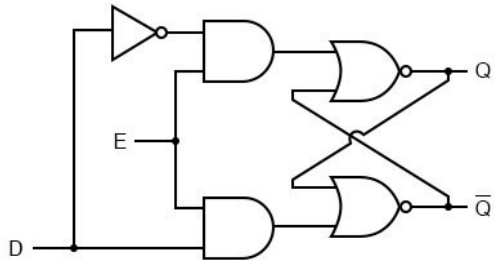
Guião 9_10_2022
Problema 1





S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

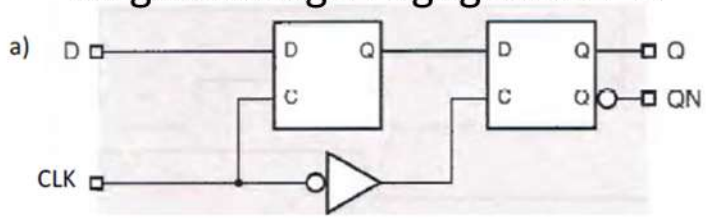


E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

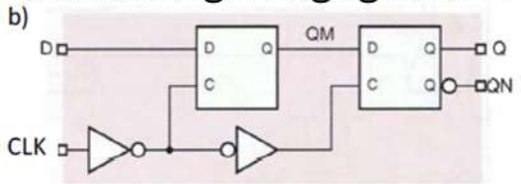
Guião 11_2021
Problema 2

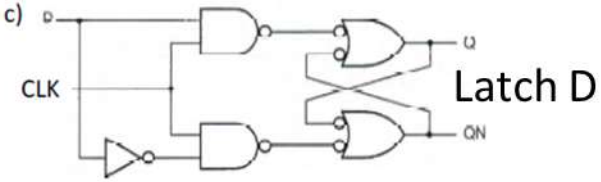
2. *[Paper and pencil]*. Analyze the circuits in Fig. 2 and indicate the location of a D latch, a positive-edge-triggered D flip-flop, and a negative-edge-triggered D flip-flop.

Negative Edge Trigegered FF D



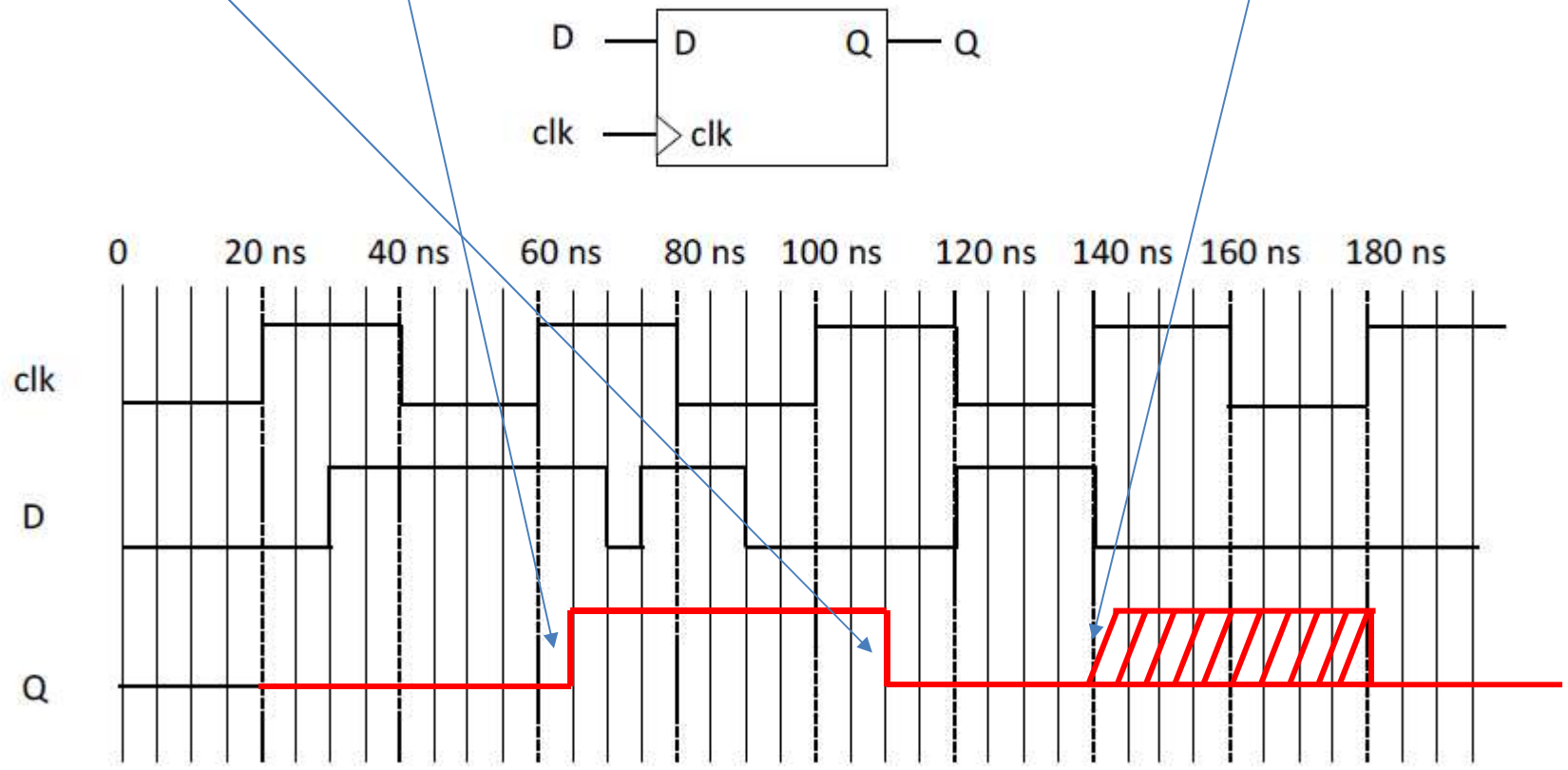
Positive Edge Trigegered FF D





Latch D

3. *[Paper and pencil]*. Complete the timing diagram of a positive edge-triggered flip-flop, illustrated in Fig. 3, with the following timing specifications: $t_{setup} = 5$ ns, $t_{hold} = 3$ ns, $t_{pHL} = 10$ ns, $t_{pLH} = 5$ ns.



4. *[Paper and pencil]*. Analyze the circuit in Fig. 4 and complete the following timing diagram (for now, assume that all delays are 0). What is the function of this circuit? Determine the period, frequency, and duty cycle of both the `clk` signal and `Q` output. Do not forget to indicate the correct units.

Assuming that the flip-flop has the following timing specifications: $t_{setup} = 5$ ns, $t_{hold} = 3$ ns, $t_{pHL} = 15$ ns, $t_{pLH} = 10$ ns, determine the maximum operating frequency of the circuit.

$T_{min} > t_{setup} + \max(t_{pHL}, t_{pLH})$

$T_{min} > 5ns + 15ns > 20ns$

$F_{max} = 50MHz$

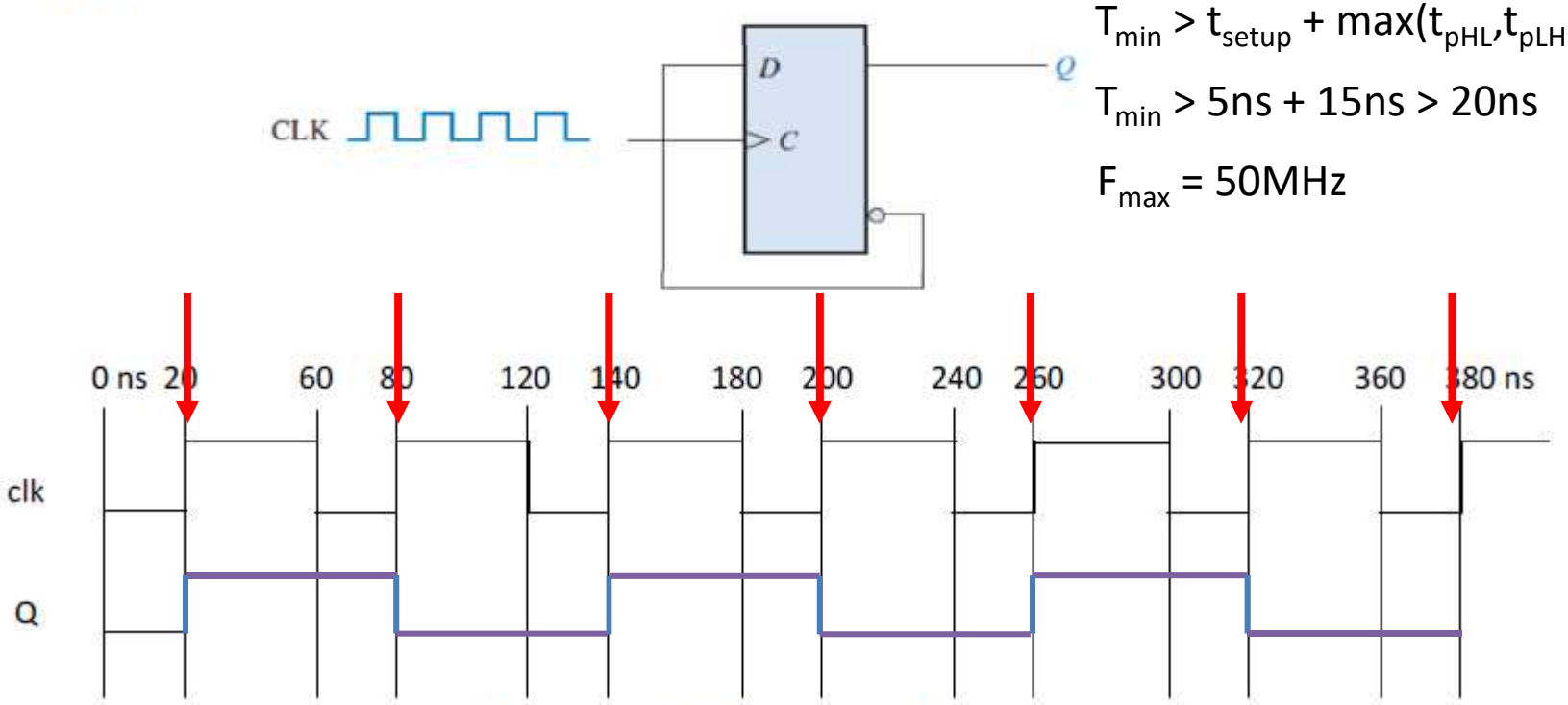


Fig. 4 – A circuit based on a D flip-flop and its timing diagram.

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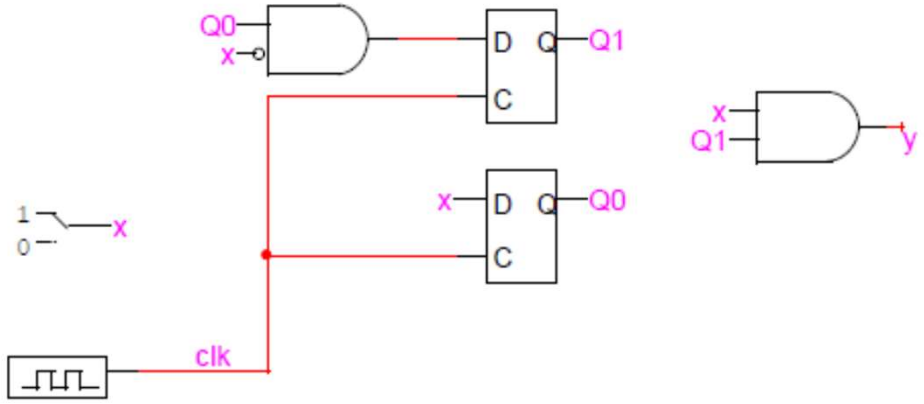
Problema 5



a. What are the circuit inputs and outputs? → Input : x output : y
b. What is the output function? → $y = xQ_1$
c. What is the next state function? → $Q_1^* = D_1 = Q_0\bar{x}$ $Q_0^* = D_0 = x$
d. What is the type of this finite state machine: Mealy ~~or Moore~~?

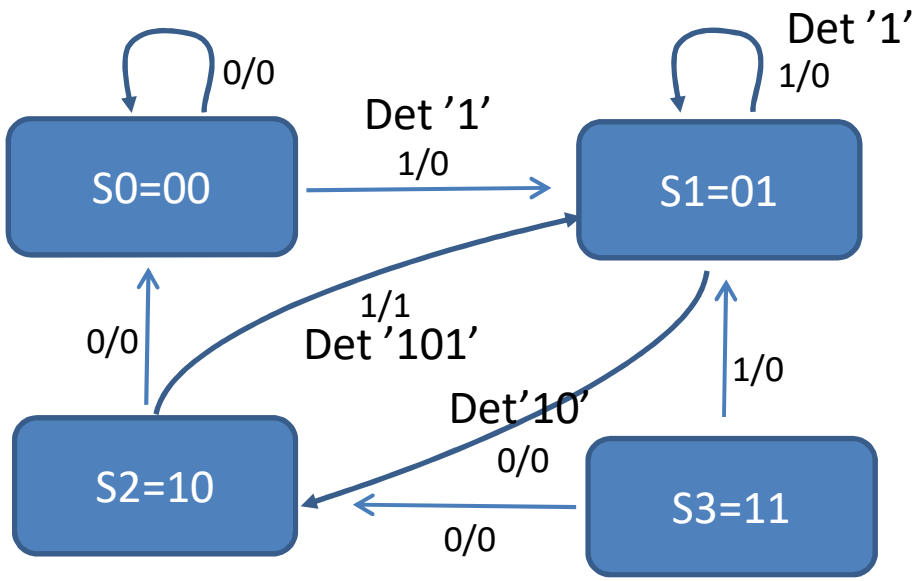
Guião 9_10_2022
Problema 5

Construct the transition/output table.
Draw the state diagram.
What is the function performed by the circuit?

$$Q_1^* = D_1 = Q_0\bar{x}$$

$$Q_0^* = D_0 = x$$

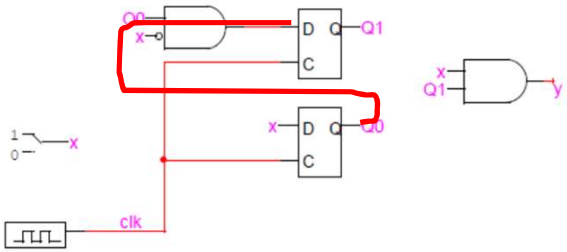
$$y = xQ_1$$



Entrada	Estado Atual	Estado seguinte	saída
x	S	S*	y
0	S0	S0	0
0	S1	S2	0
0	S2	S0	0
0	S3	S2	0
1	S0	S1	0
1	S1	S1	0
1	S2	S1	1
1	S3	S1	0

Guião 9_10_2022
Problema 5

What is the function performed by the circuit?
Assume that the flip-flops in Fig. 5 have the following timing specifications: t_{setup} = 15 ns, t_{hold} = 5 ns, t_{pHL} = 25 ns, t_{pLH} = 20 ns. What is the maximum delay that an elementary logic gate t_{gate} could have so that the circuit would function correctly at 20 MHz?



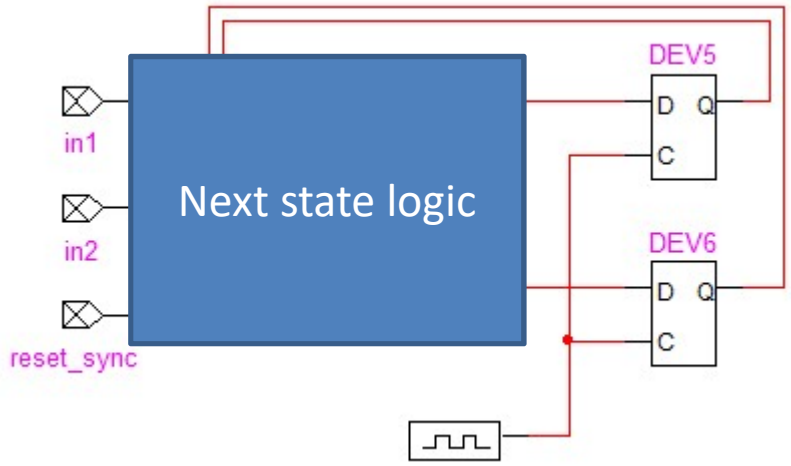
$T_{min} > max(t_{pHL},t_{pLH}) + t_{pgate} + t_{setup}$

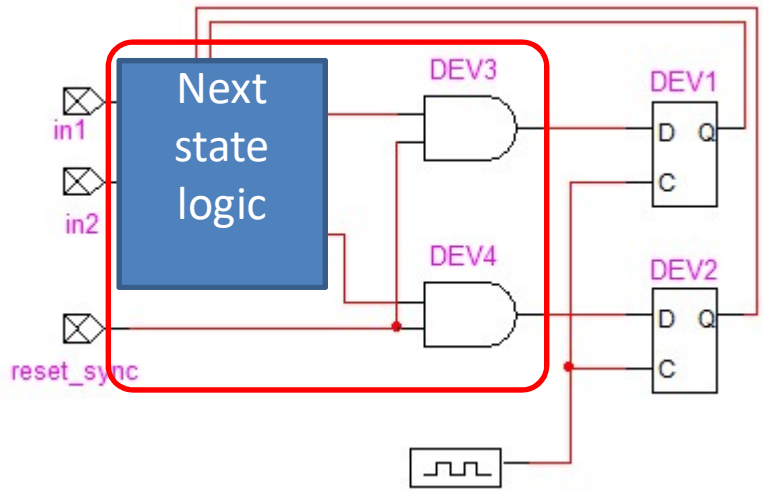
$50ns > 25ns + t_{pgate} + 15ns$

$t_{pgate} < 10ns$

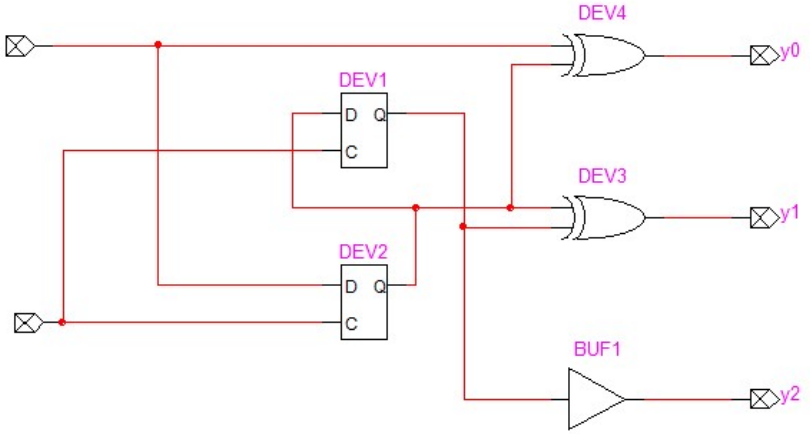
Entrada	Estado atual	Estado seguinte	Saída	Estado atual		Estado seguinte		Saída
x	**S**	**S+**	**y**	**Q1**	**Q0**	**Q1+=D1**	**Q0+=D0**	**y**
0	**S0**	**S0**	**0**	**0**	**0**	**0**	**0**	**0**
0	**S1**	**S2**	**0**	**0**	**1**	**1**	**0**	**0**
0	**S2**	**S0**	**0**	**1**	**0**	**0**	**0**	**0**
0	**S3**	**S2**	**0**	**1**	**1**	**1**	**0**	**0**
1	**S0**	**S1**	**0**	**0**	**0**	**0**	**1**	**0**
1	**S1**	**S1**	**0**	**0**	**1**	**0**	**1**	**0**
1	**S2**	**S1**	**1**	**1**	**0**	**0**	**1**	**1**
1	**S3**	**S1**	**0**	**1**	**1**	**0**	**1**	**0**

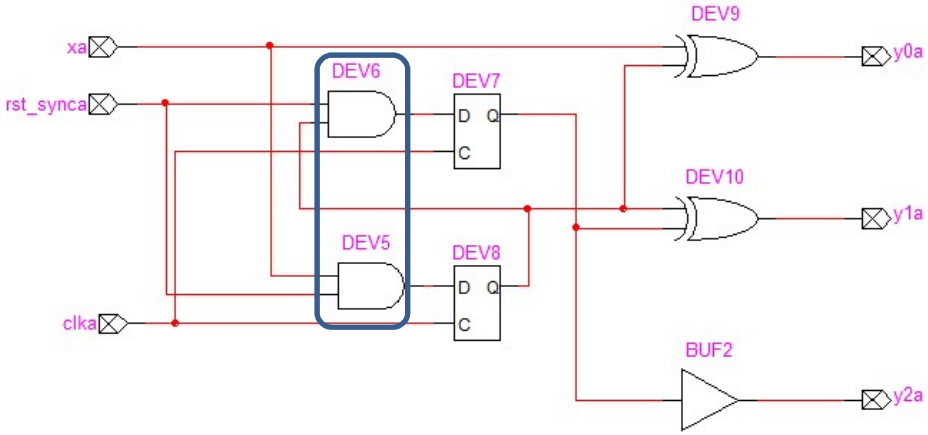
Guião 9_10_2022
Problema 6



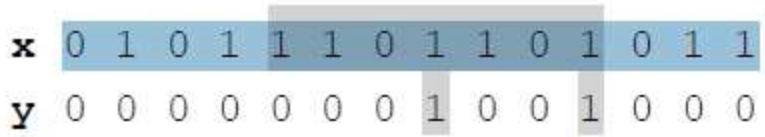


Guião 9_10_2022
Problema 6

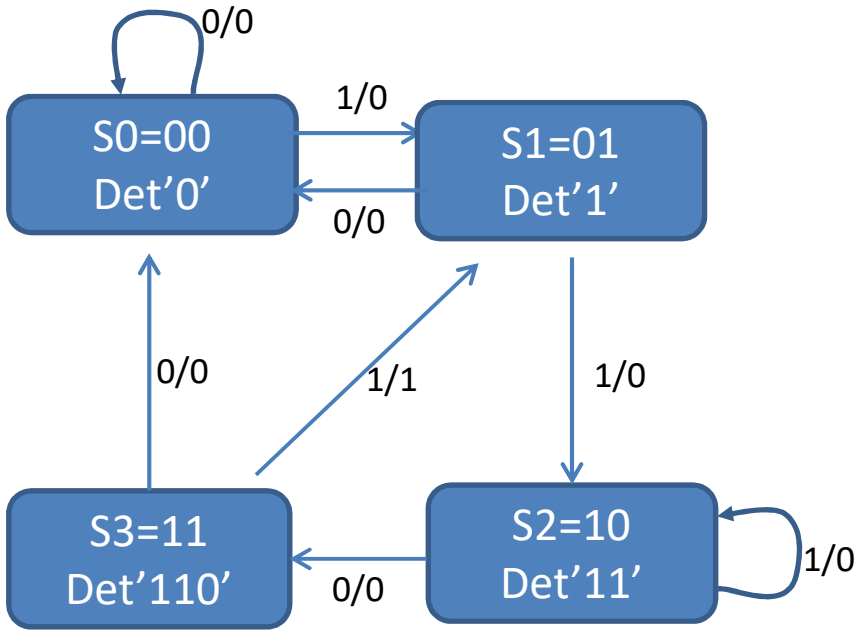




Guião 11_13_2022
Problema 1

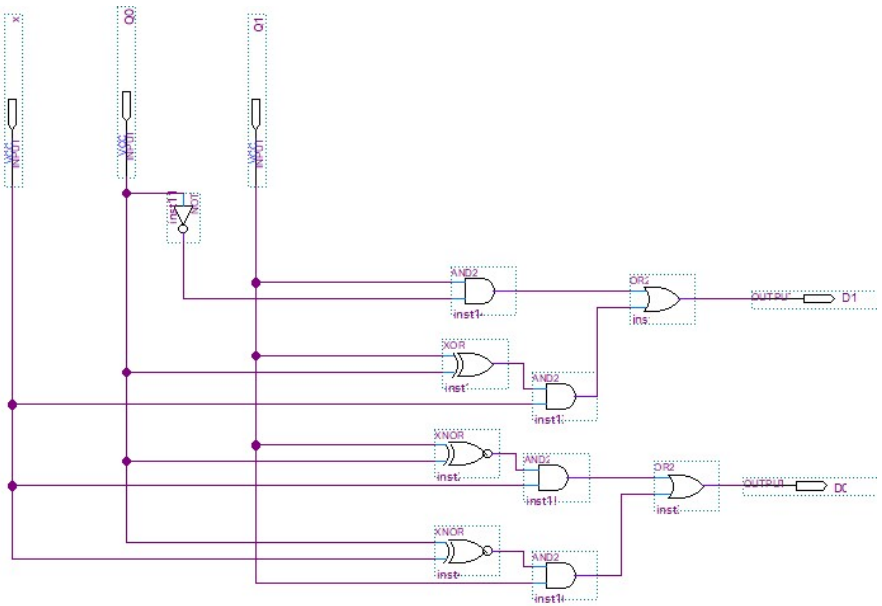


x/y



x	Q1	Q0	D1	D0	y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	0	1	1

Guião 11_13_2022
Problema 1

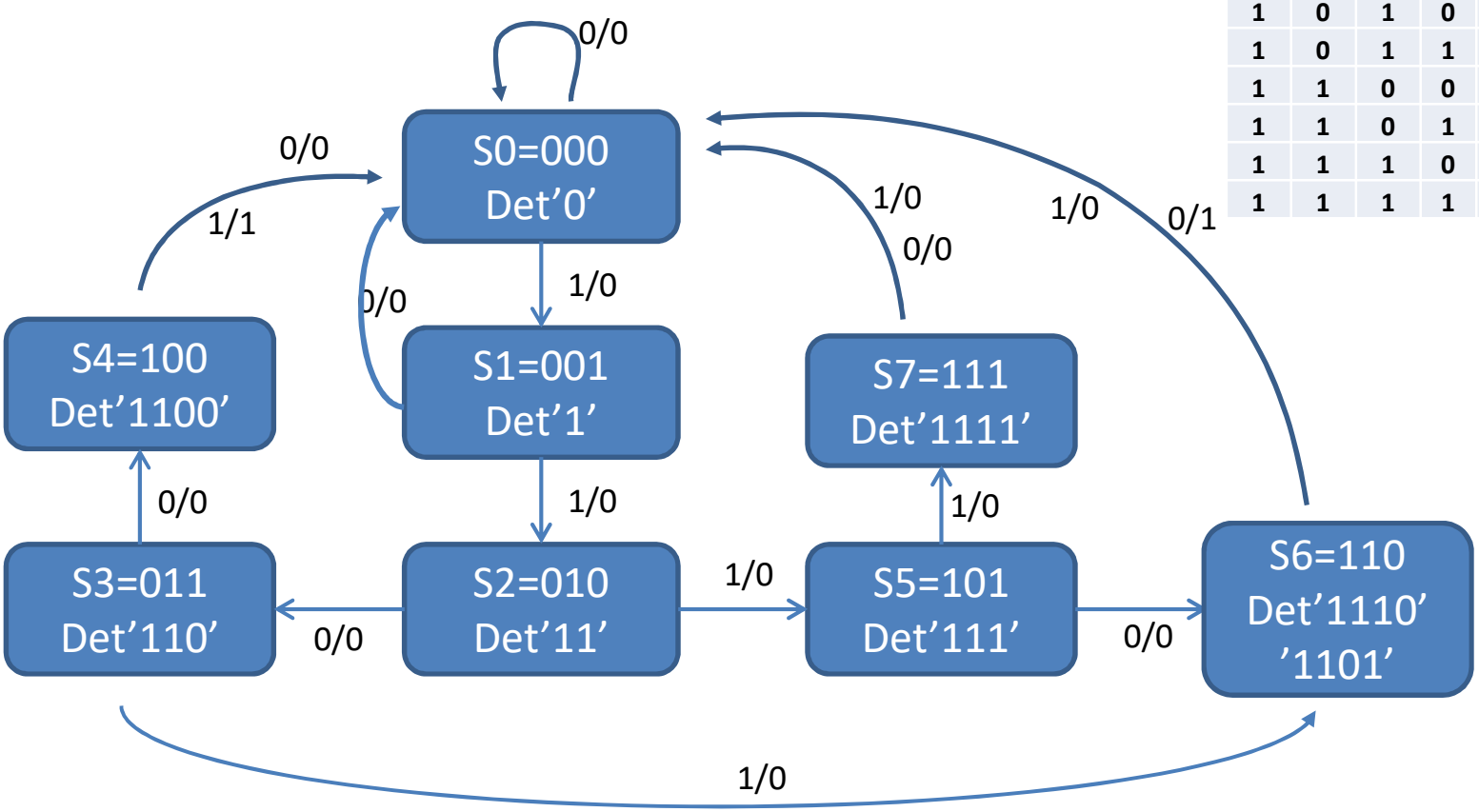


x	Q1	Q0	D1	D0	y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	0	0
1	1	1	0	1	1

D1	Q1 Q0							
X	00	01	11	10				
0				1		D1=Q1.Q0'+x.Q1'. Q0		
1		1		1				
D0	Q1 Q0							
X	00	01	11	10				
0				1		D0=Q1.(x xor Q0)' +x.(Q1 xor Q0)'		
1	1		1					

Guião 11_13_2022
Problema 2

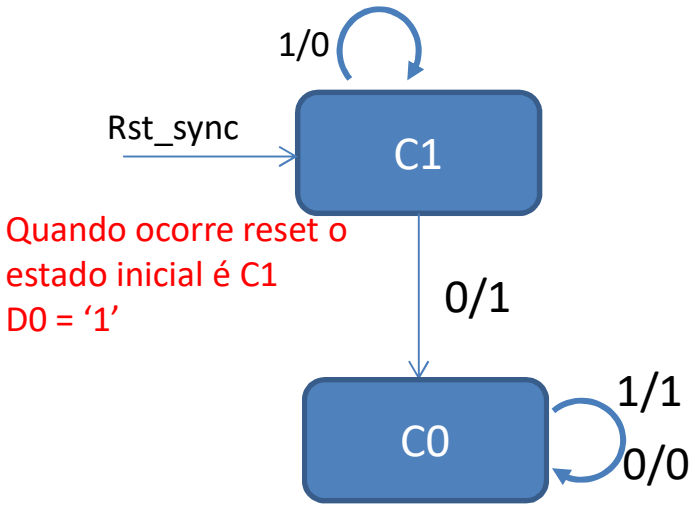
x	Q2	Q1	Q0	D2	D1	D0	y
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	1	1	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	1	1	0	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	0	0
1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	0	1	0
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	0
1	1	1	1	0	0	0	0



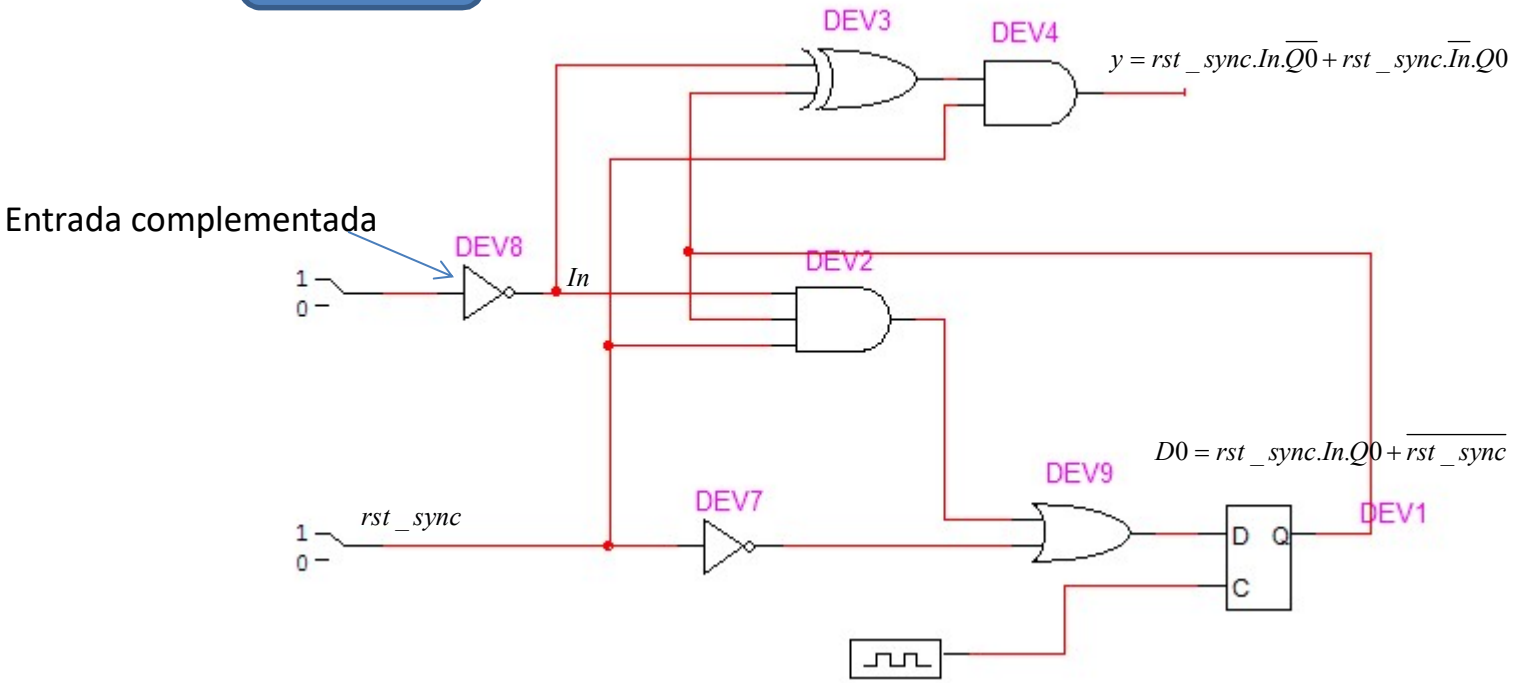
Guião 2019_2020
Problema 3 FSM Mealy

C1 estado carry out = ‘1’
C0 estado carry out = ‘0’

rs_sync	In	Q0	D0	y
1	0	0	0	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0
0	*	*	1	0

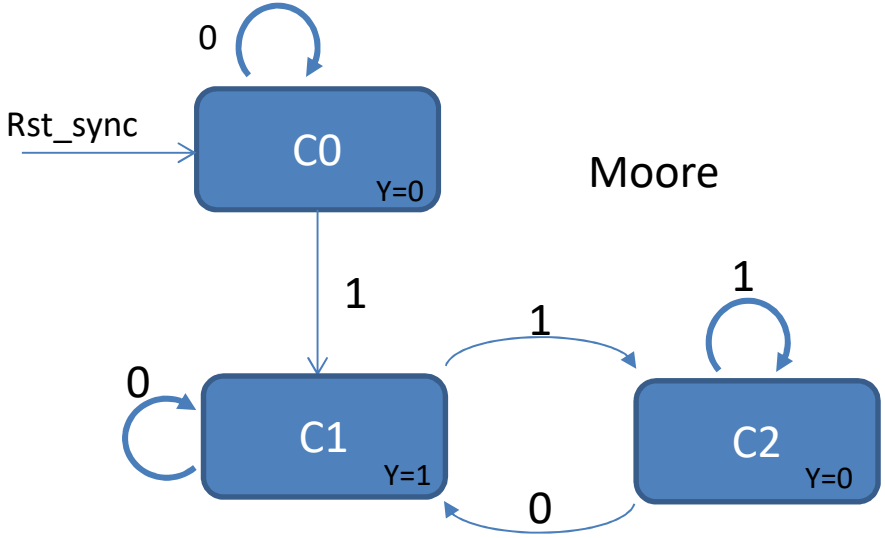


Quando ocorre reset o estado inicial é C1
D0 = ‘1’

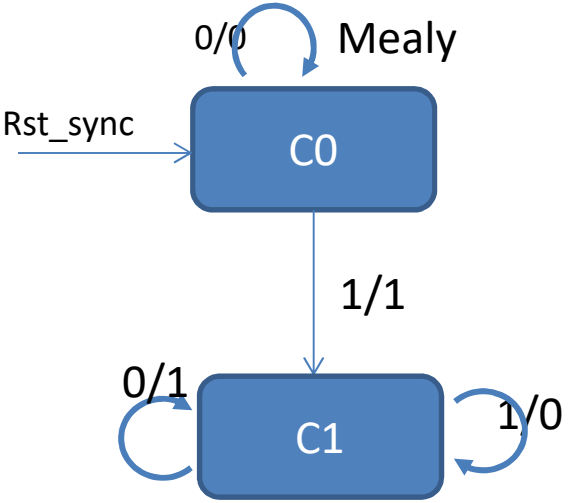


Guião 11-13_2022

Problema 3 FSM Moore



Moore



		X=0		X=1		
Q1	**Q0**	**D1**	**D0**	**D1**	**D0**	**out**
0	0	0	0	0	1	0
0	1	0	1	1	0	1
1	0	0	1	1	0	0
1	1	*	*	*	*	*

Q2	Q1	Q0	Q2+	Q1+	Q0+
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Guião 11

Problema 4 Gray counter

Next state truth table

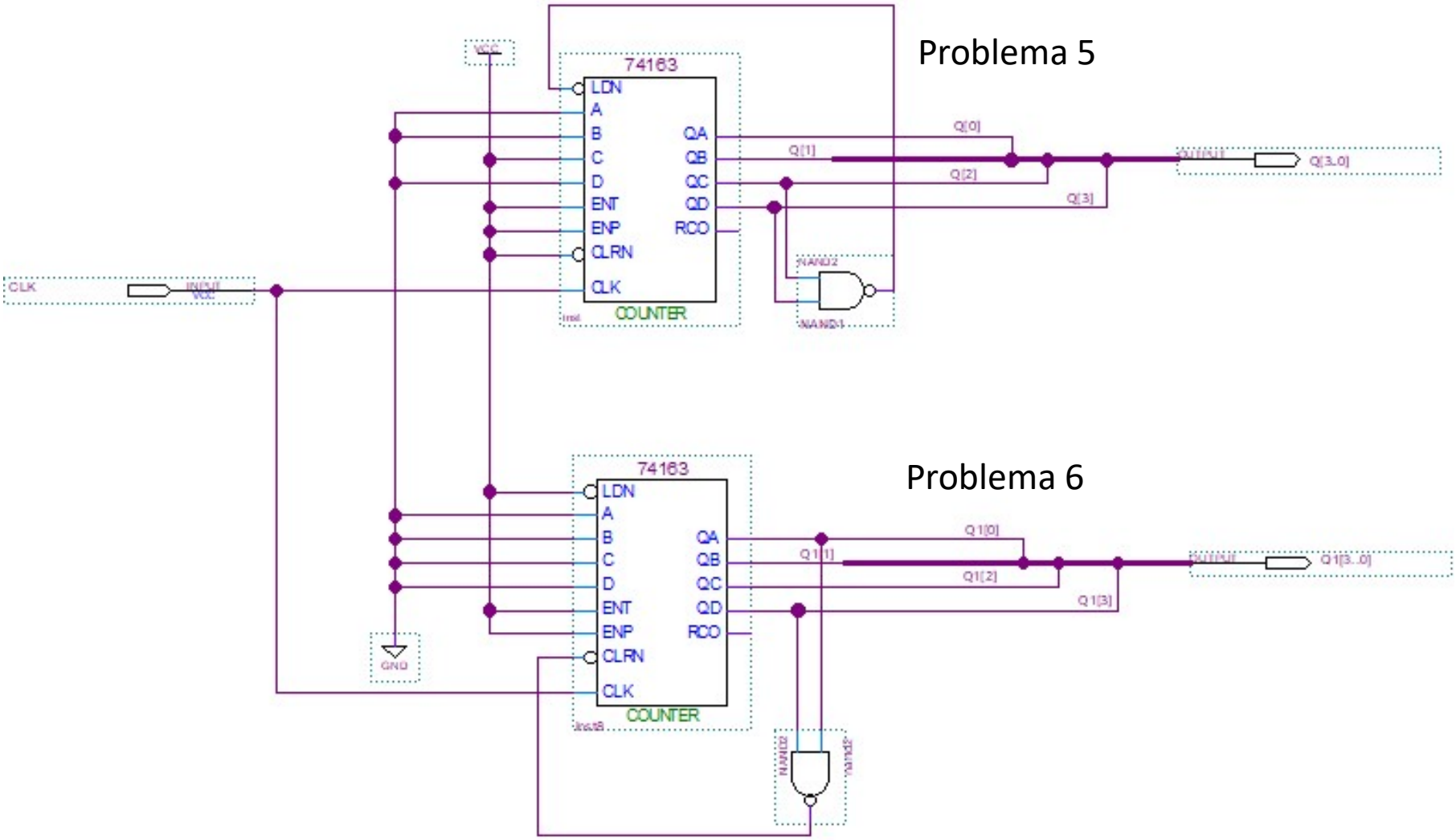
Q0/Q2Q1	00	01	11	10	
0		1	1		Q2+=Q0'.Q1+Q0.Q2
1			1	1	

Q0/Q2Q1	00	01	11	10	
0		1	1		Q1+=Q0'.Q1+Q0.Q2'
1	1	1			

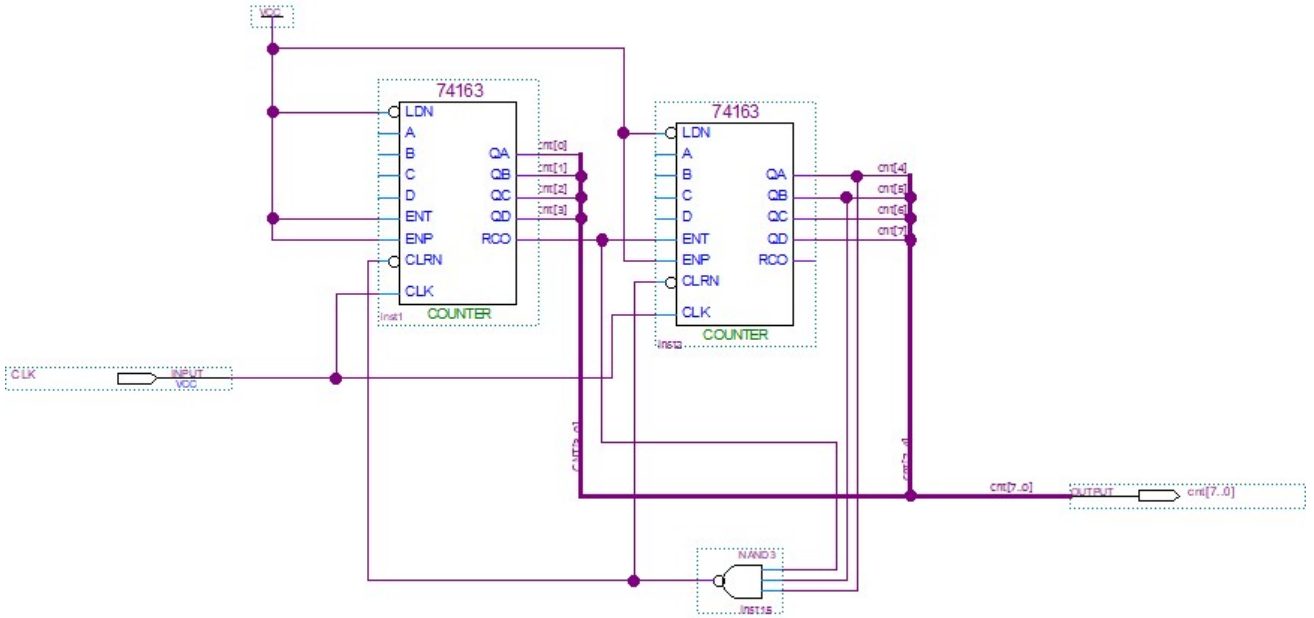
Q0/Q2Q1	00	01	11	10	
0	1		1		
1	1		1		Q0+=Q2'.Q1'+Q2.Q1

Guião 11-13

Problema 5 -6 counters

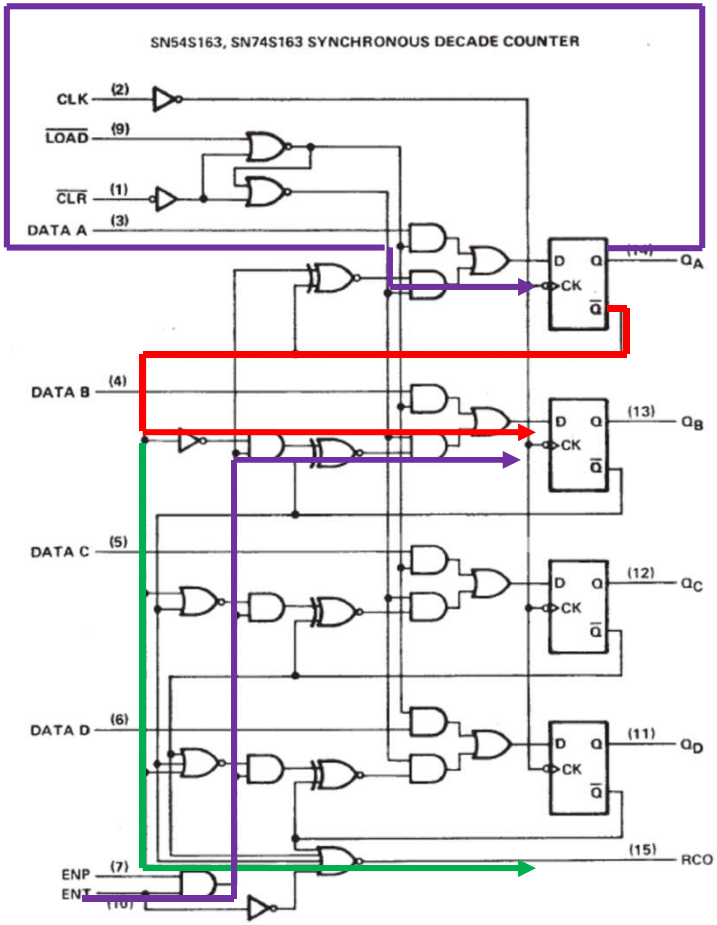


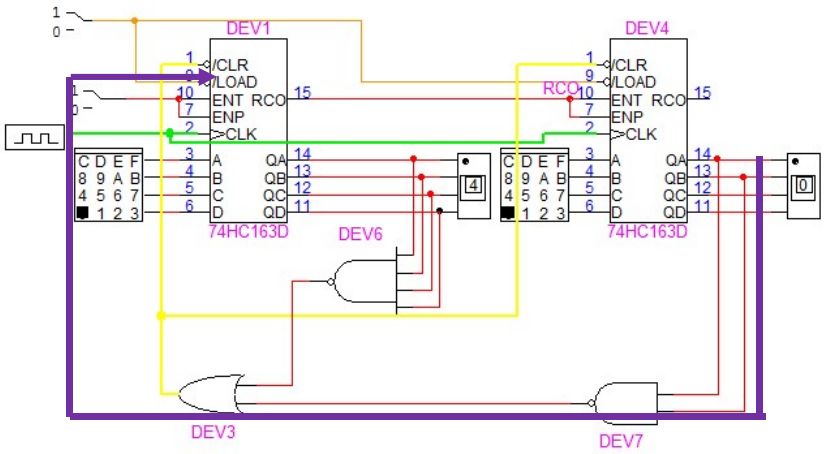
Guião 11-13
Problema 7 counter mod 64



Com base nos componentes 74x163 crie um contador módulo 64. Determine, justificando a máxima frequência de funcionamento do circuito tendo em conta as seguintes especificações temporais:

a. flip-flops que compõem o contador: t_{setup}=10 ns, t_{hold}=4 ns, t_{pHL}=20 ns, t_{pLH}=15 ns;
b. tempo de atraso de uma porta lógica elementar (se usada): t_{porta} = 5 ns.



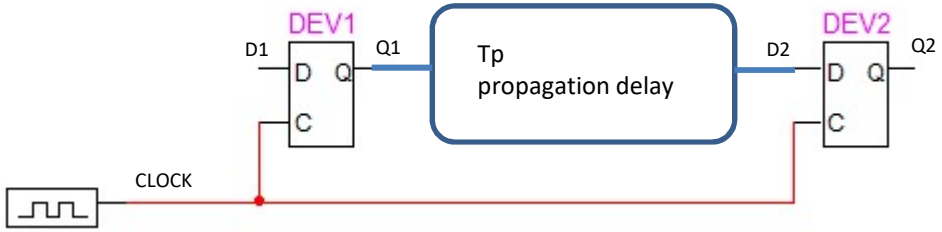


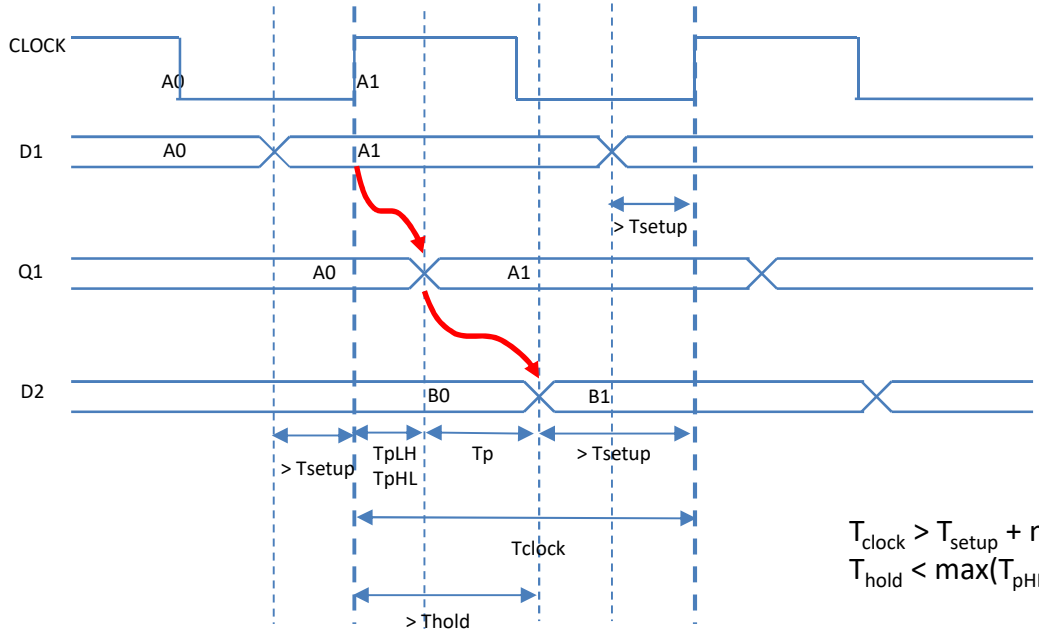
6 gates

5 gates

6 gates

Análise temporal de um circuito síncrono





$T_{clock} > T_{setup} + \max(T_{pHL},T_{pLH}) + T_p$

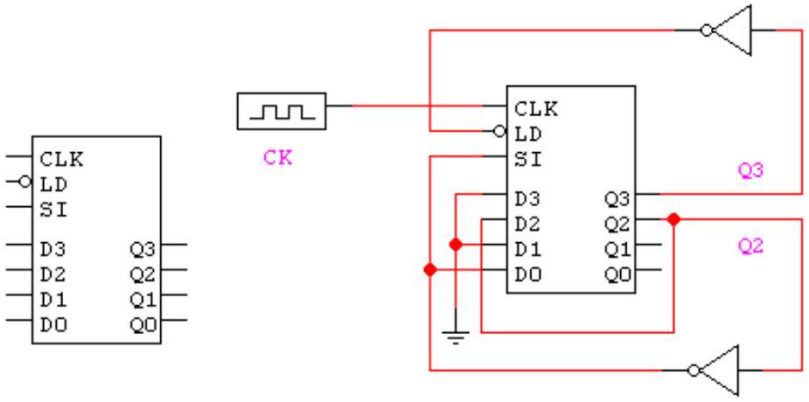
$T_{hold} < \max(T_{pHL},T_{pLH}) + T_p$

O problema das limitações temporais de um circuito digital resumem-se à análise da propagação dos sinais entre saídas e entradas, do mesmo ou de outro de Flip Flop, consoante se trata de um circuito com *feedback* ou sem *feedback*.

Guião 11-13_2022

Prob 8: Shift_register

1 – 3 – 7 – 14 – 4 – 8 - 1



a) b)

Q3	Q2	Q1	Q0	D3	D2-Q2	D1	D0-Q2’	Si- Q2’	LD-Q3’
0	0	0	0	0	0	0	1	1	1
0	0	0	1	0	0	0	1	1	1
0	0	1	1	0	0	0	1	1	1
0	1	1	1	0	1	0	0	0	1
1	1	1	0	0	1	0	0	0	0
0	1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	1	0
0	0	0	1	0	0	0	1	1	1

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** Nios® II EDS requires you to install an Eclipse IDE manually.

Devices

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cyclone-20.1.1.720.qdz

Size: 466 MB
SHA1: 5447aa416749edf5bae5f68dcc734c43e8db6a67