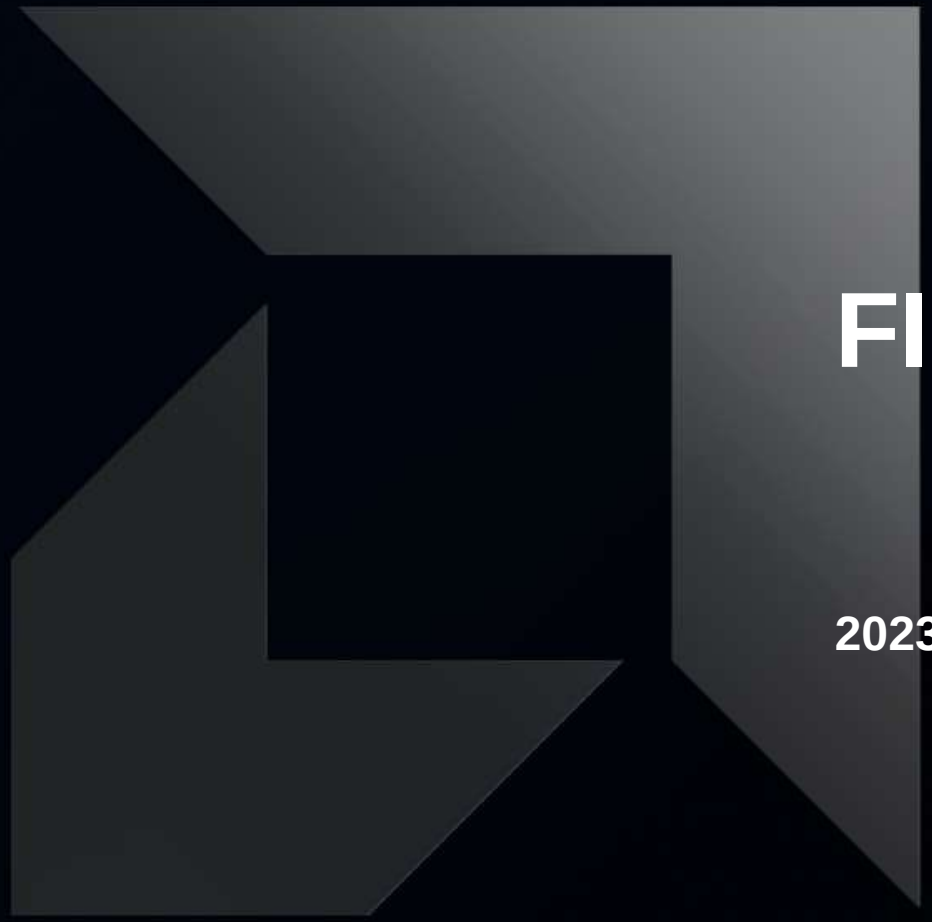


FIFO Exam

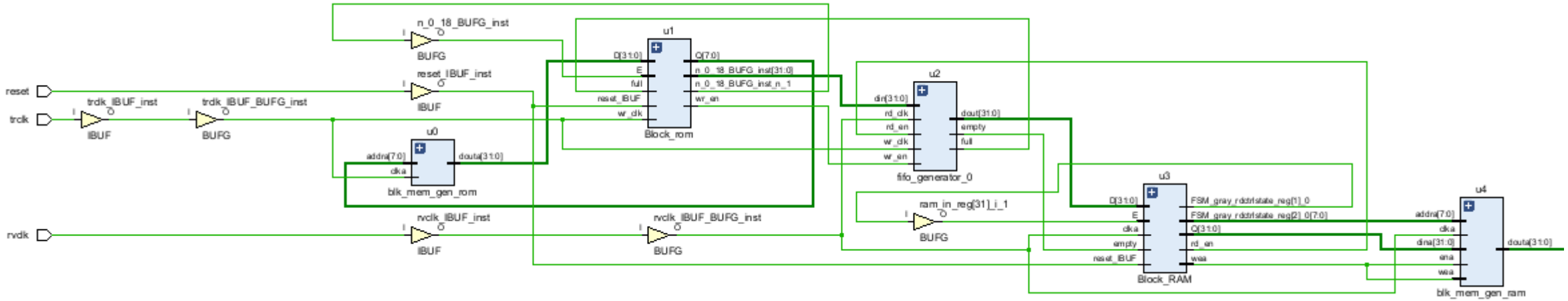
2023.11

AMD
together we advance_

Agenda

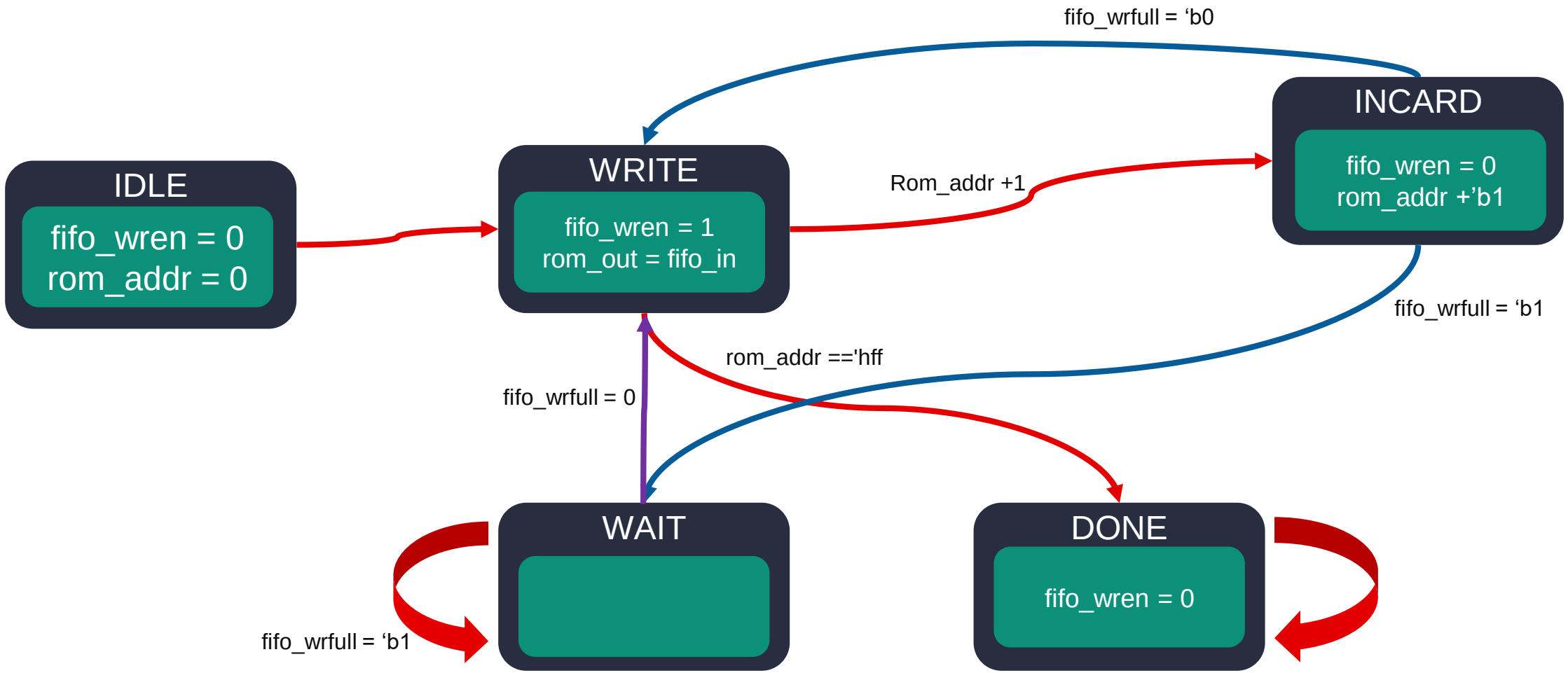
- Structure of Circuit
- Finite-State Machine
- Simulation
- Timing Constraints
- Results of Synthesis

Finite-State Machine



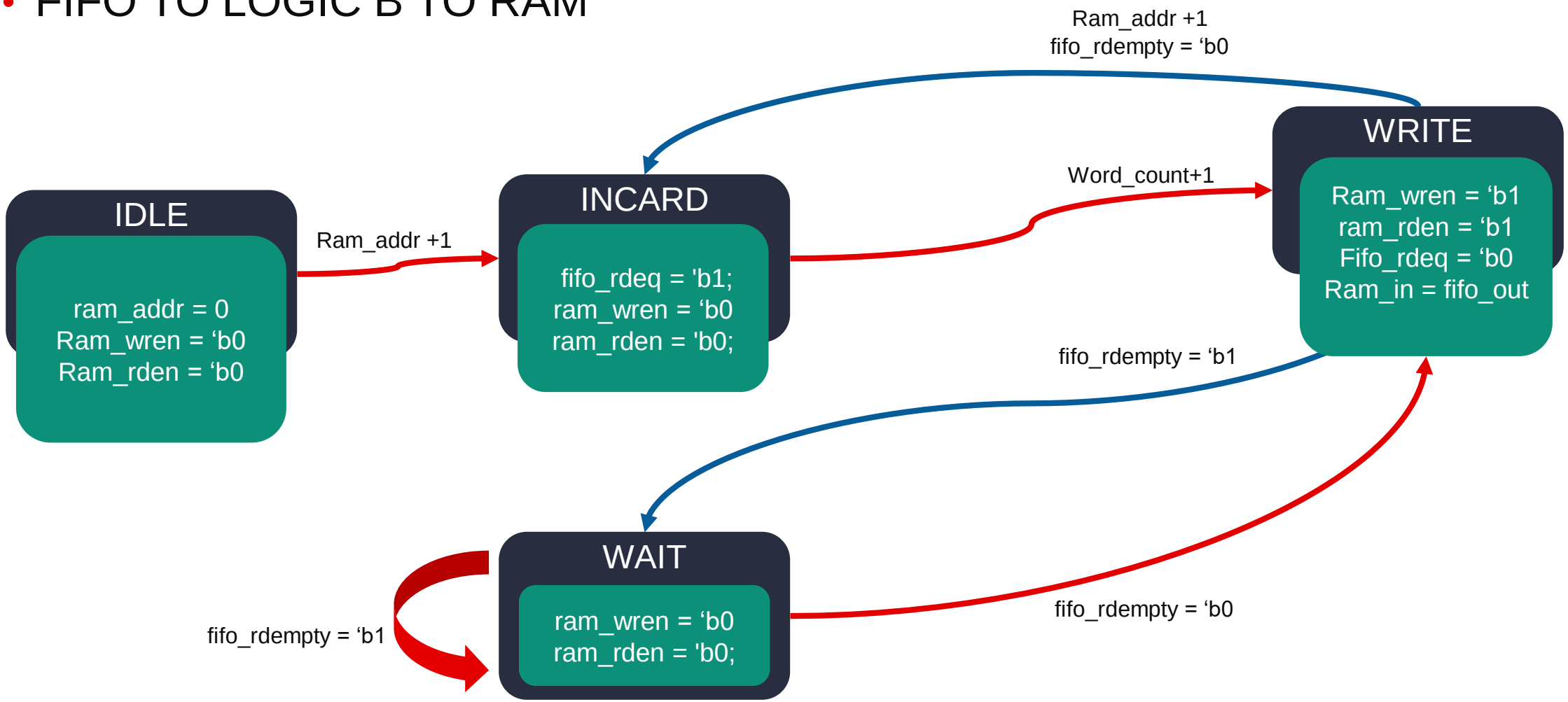
Finite-State Machine

- ROM TO LOGIC A TO FIFO



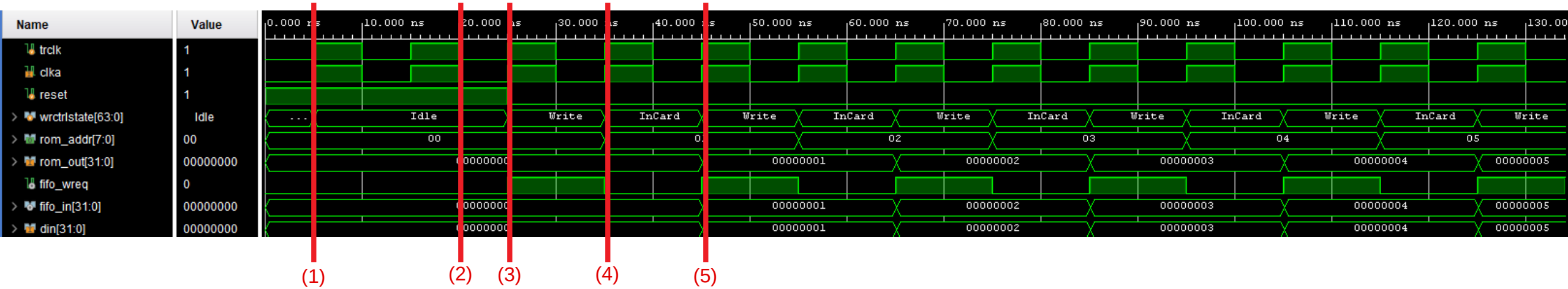
Finite-State Machine

- FIFO TO LOGIC B TO RAM



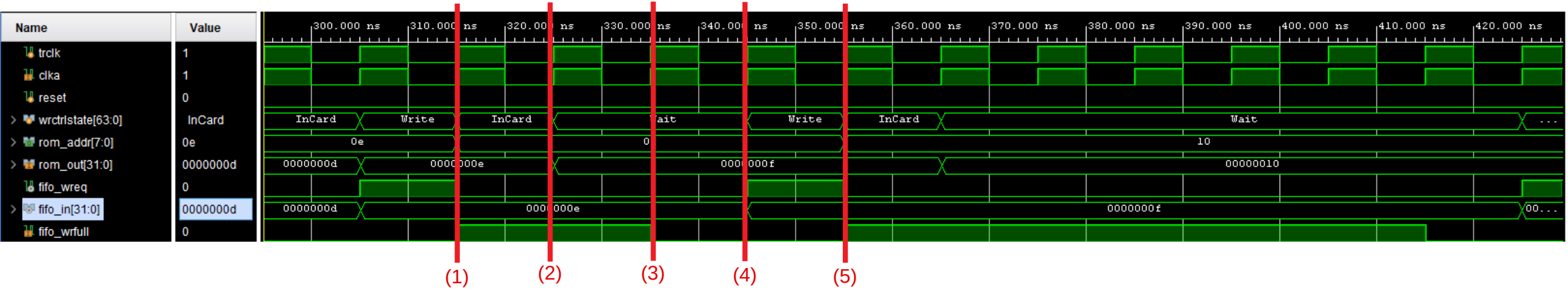
Simulation

- Transmitting Domain



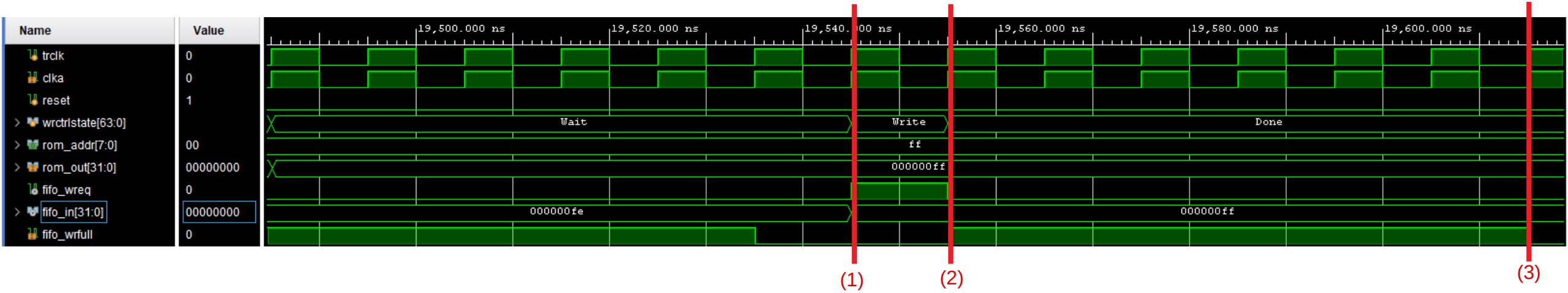
Simulation

- wire operation when FIFO is Full



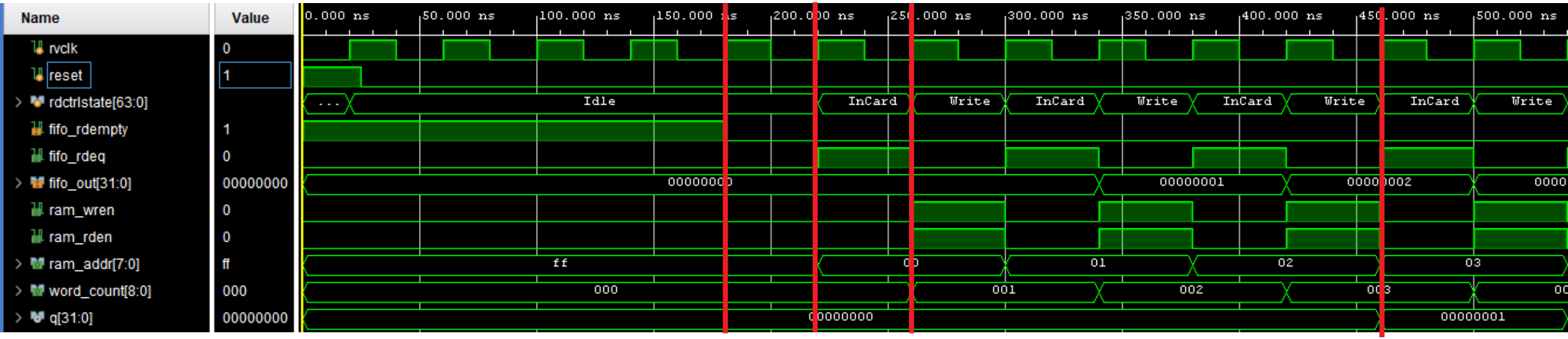
Simulation

- completion of data transfer form ROM to FIFO



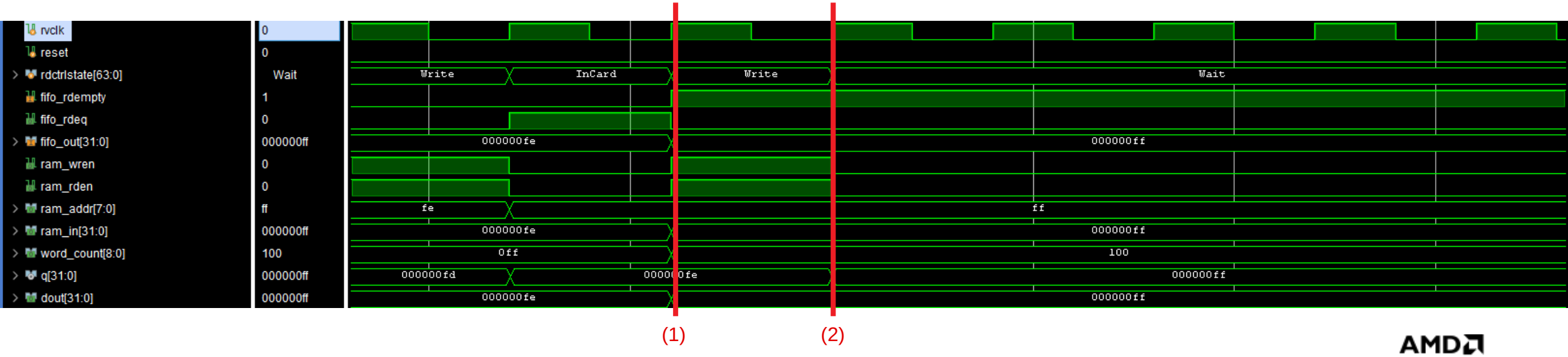
Simulation

- Receiveing Domain



Simulation

- completion of data transfer form FIFO to RAM



Please tell me what the WNS of your design is under the default synthesis strategy?

Setup

Worst Negative Slack (WNS):	998.975 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	8

All user specified timing constraints are met.

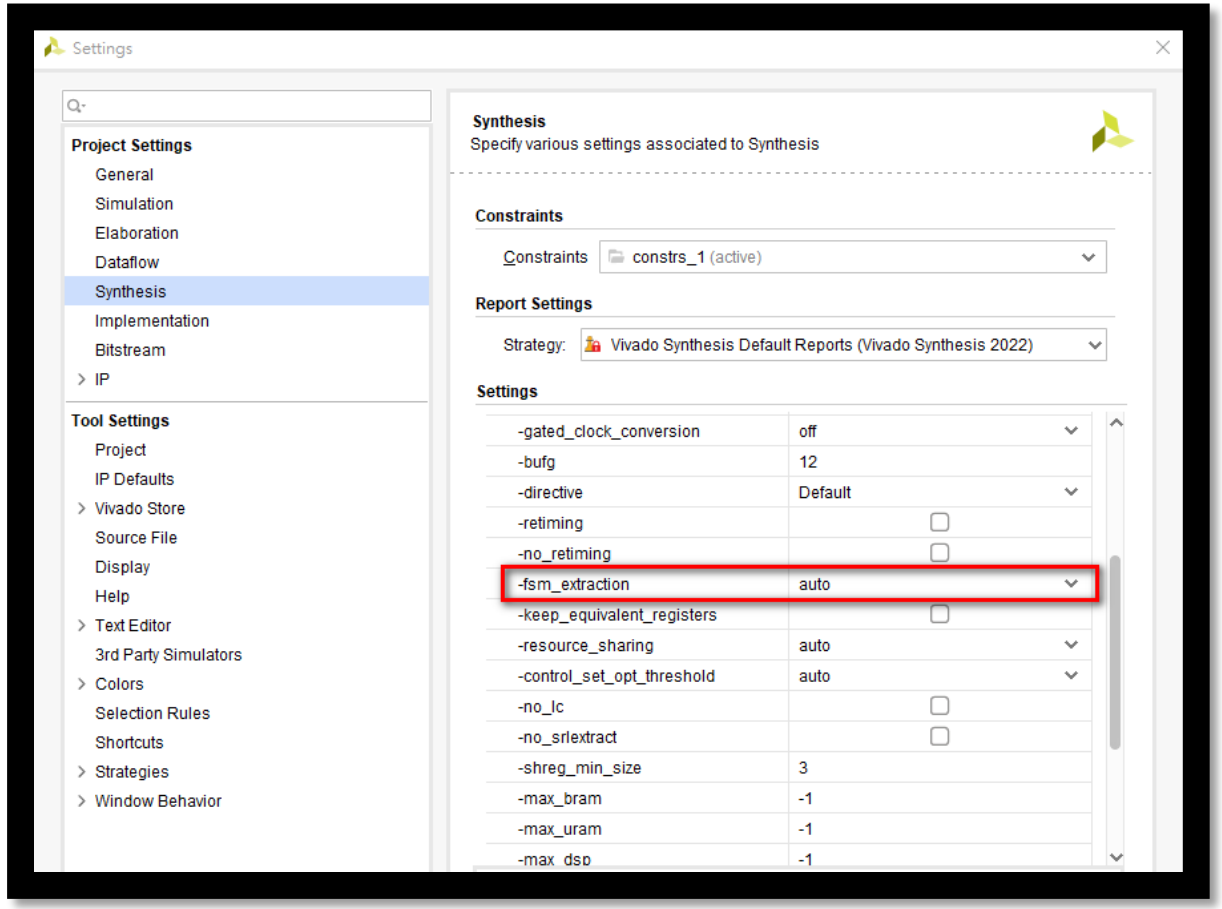
Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
5	trclk	5.000	0.000	2.500	☐	[get_ports trclk]	gray.xdc		
6	rvclk	20.000	0.000	10.000	☐	[get_ports rvclk]	gray.xdc		

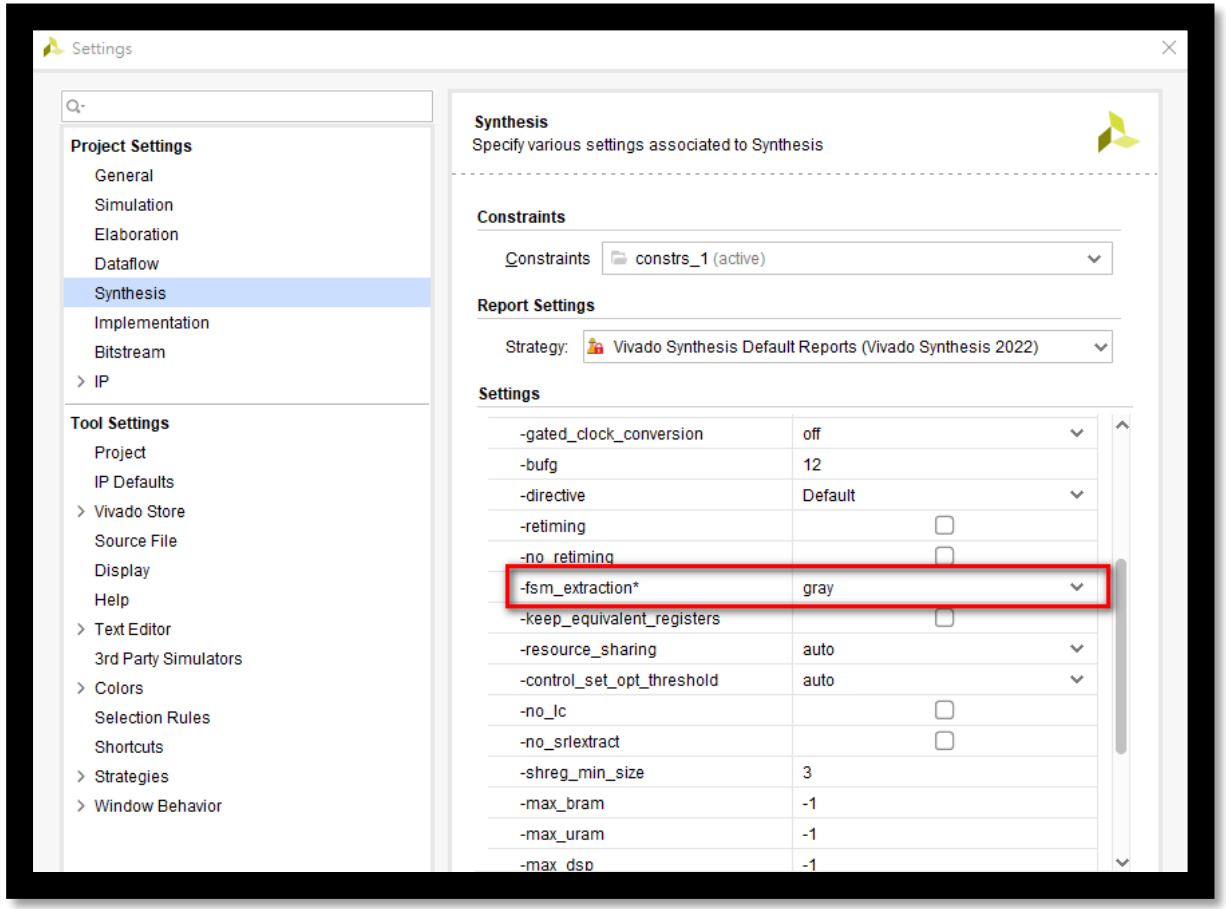
Setup

Worst Negative Slack (WNS):	2.320 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	90

All user specified timing constraints are met.

What method is used for the FSM of the default strategy? What will be the difference if the report is changed to Gray-code mode?





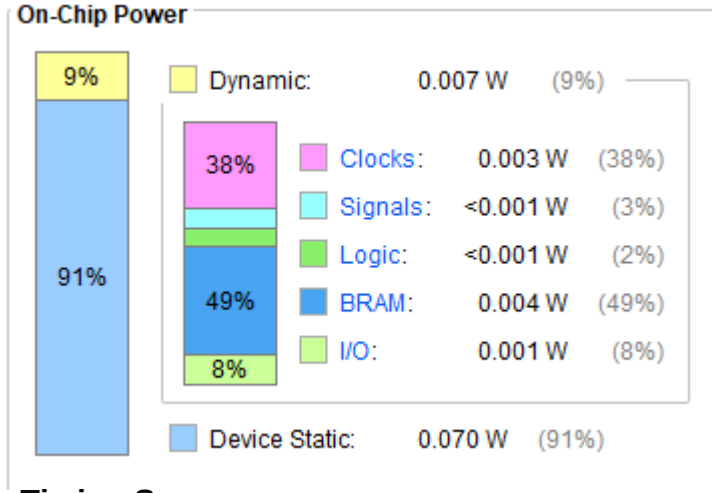
Report different between the Strategy of FSM Extraction(AUTO/GRAY)

AUTO

Utilization

Name	Slice LUTs (32600)	Slice Registers (65200)	Block RAM Tile (75)	Bonded IOB (210)	BUFGCTRL (32)
TOP	47	156	1.5	35	4
u0 (blk_mem_gen_rom)	0	0	0.5	0	0
u1 (Block_rom)	11	50	0	0	0
u2 (fifo_generator_0)	27	56	0.5	0	0
u3 (Block_RAM)	9	50	0	0	0
u4 (blk_mem_gen_ram)	0	0	0.5	0	0

Power



Timing Summary

Setup

Worst Negative Slack (WNS):	2.320 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	90

Hold

Worst Hold Slack (WHS):	0.007 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	82

Pulse Width

Worst Pulse Width Slack (WPWS):	2.000 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	73

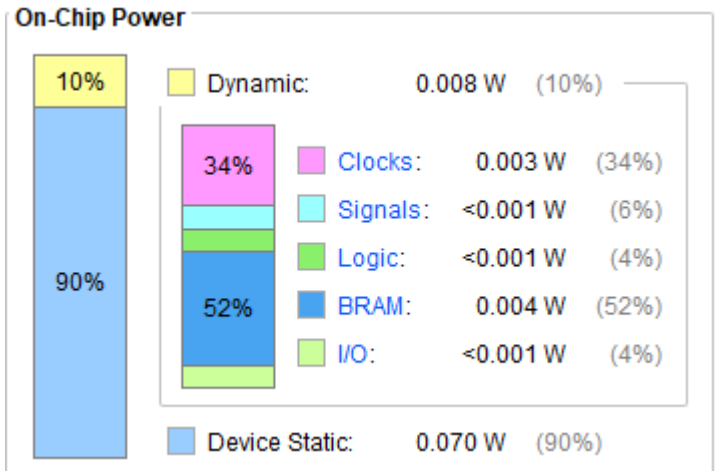
All user specified timing constraints are met.

GRAY

Utilization

Name	Slice LUTs (32600)	Slice Registers (65200)	Block RAM Tile (75)	Bonded IOB (210)	BUFGCTRL (32)
TOP	51	151	1.5	35	4
u0 (blk_mem_gen_rom)	0	0	0.5	0	0
u1 (Block_rom)	12	47	0	0	0
u2 (fifo_generator_0)	27	56	0.5	0	0
u3 (Block_RAM)	12	48	0	0	0
u4 (blk_mem_gen_ram)	0	0	0.5	0	0

Power



Timing Summary

Design Timing Summary

Setup

Worst Negative Slack (WNS):	2.320 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	90

Hold

Worst Hold Slack (WHS):	0.007 ns
Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	82

Pulse Width

Worst Pulse Width Slack (WPWS):	2.000 ns
Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	70

All user specified timing constraints are met.

Please provide your Timing constrain file

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
5	trclk	5.000	0.000	2.500	☐	[get_ports trclk]	gray.xdc		
6	rvclk	20.000	0.000	10.000	☐	[get_ports rvclk]	gray.xdc		

```
create_clock -period 5.000 -name trclk -waveform {0.000 2.500} [get_ports trclk]
create_clock -period 20.000 -name rvclk -waveform {0.000 10.000} [get_ports rvclk]
```