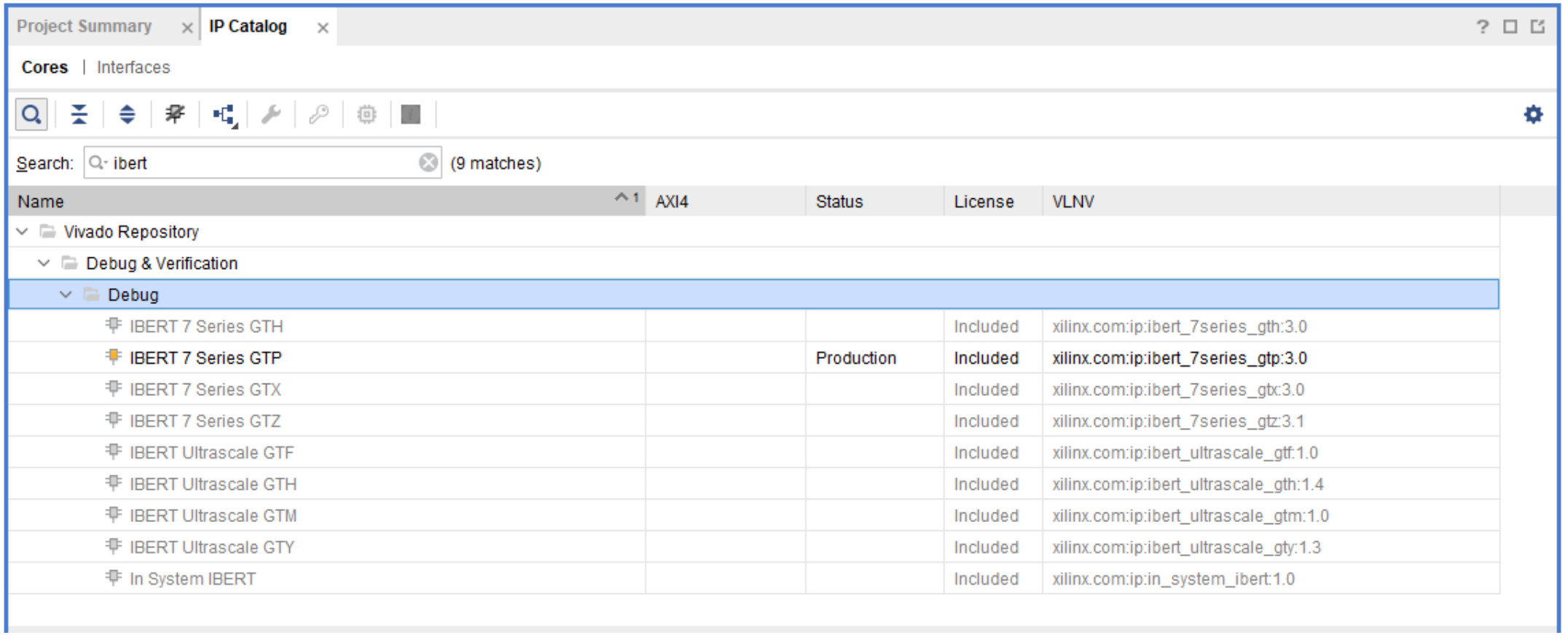
Xilinx IBERT usage

AMD
together we advance_

IBERT

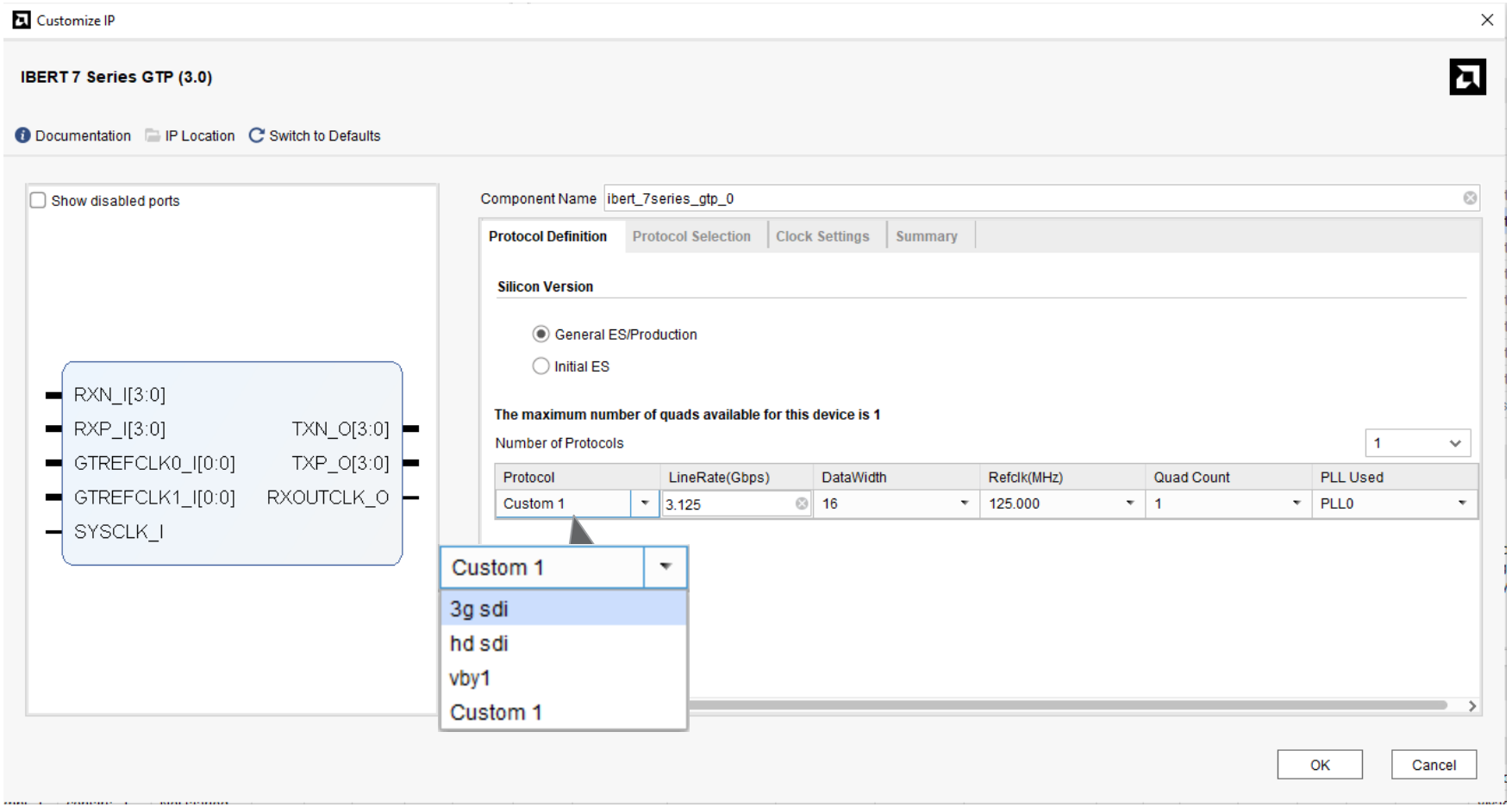
IBERT Catalog

Based on different transceivers, you can generate the corresponding IBERT IP.
The differences in configurations between various IPs are not significant. Here, we will use GTP as an example



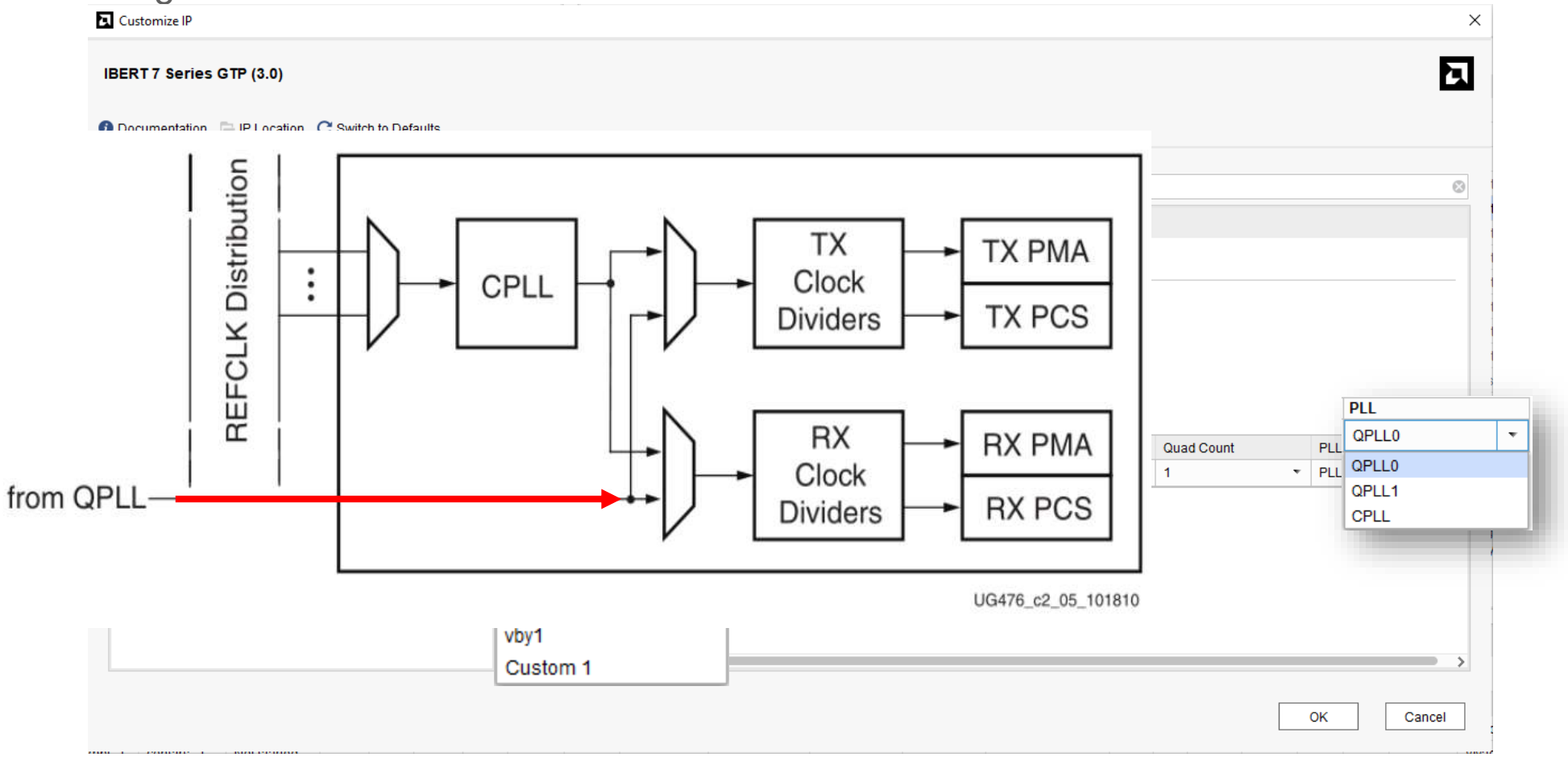
IBERT IP Setting

In the IP settings, there are default Protocol templates available for selection. However, you can also modify them according to your specific requirements.



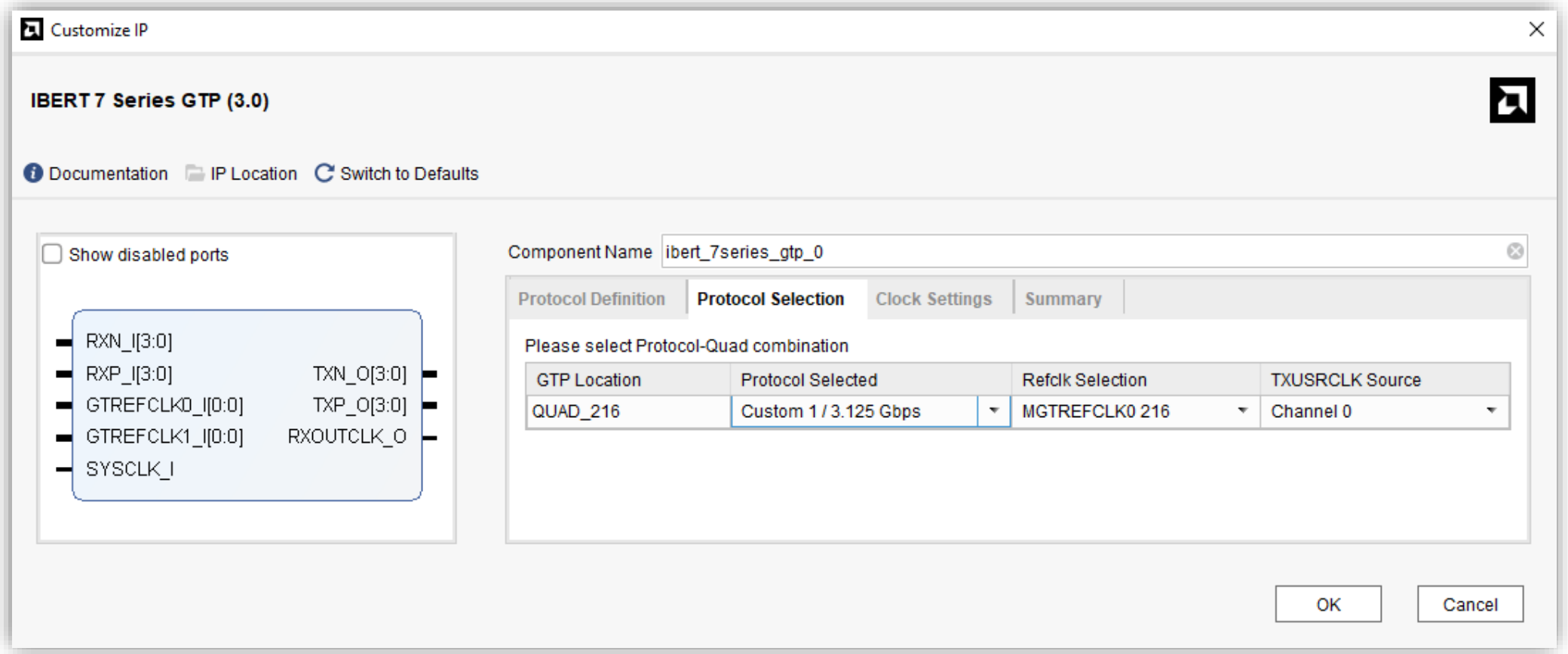
IBERT PLL Used

In certain types of transceivers, there may be a shared PLL for the entire Quad and individual PLLs for each channel. The most significant difference between them is the LineRate they can achieve. Generally, the QPLL rate is higher than the CPLL rate.



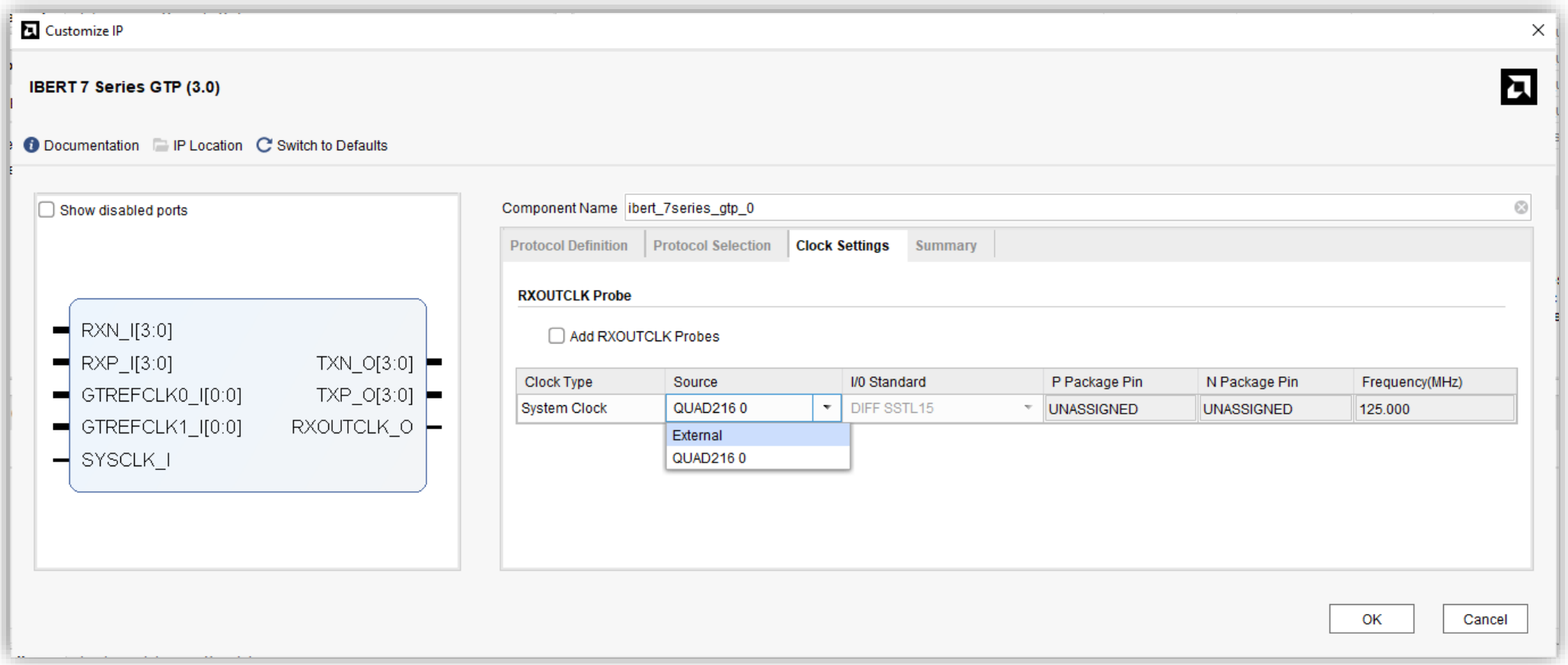
IBERT Refclk Selection

In IBERT, the reference clock is uniformly provided by the transceiver.



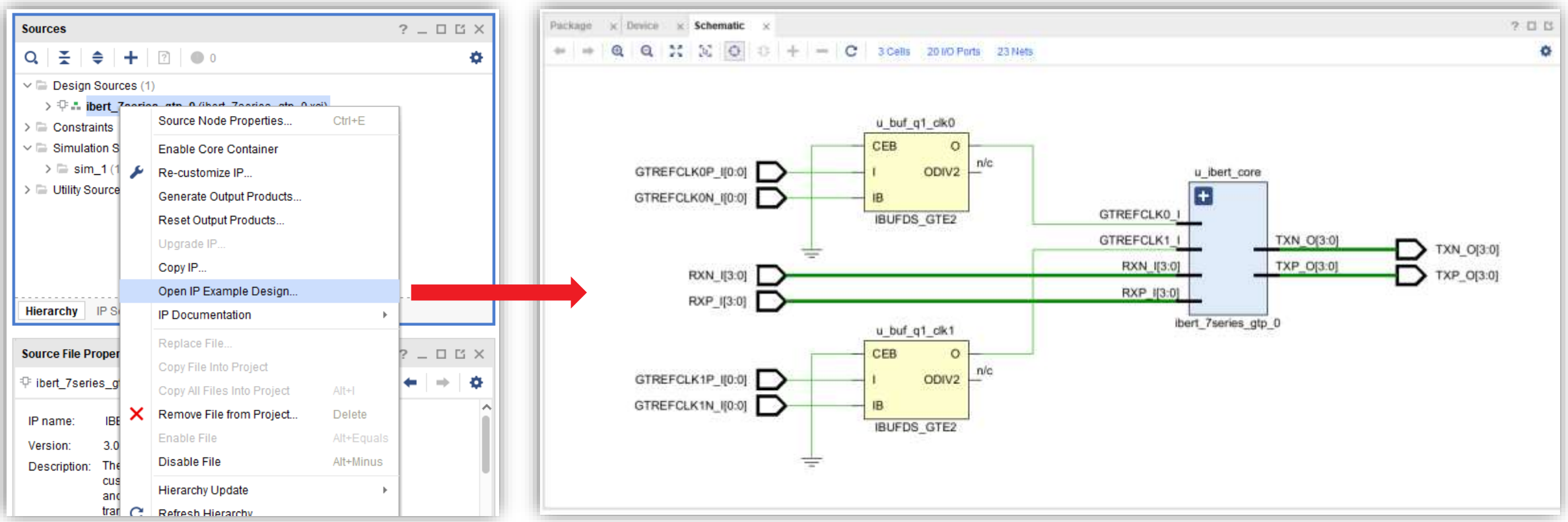
IBERT Refclk Selection

The system clock can be selected to be provided either externally or by the transceiver. Subsequent example designs can make pin assignments based on IP settings.



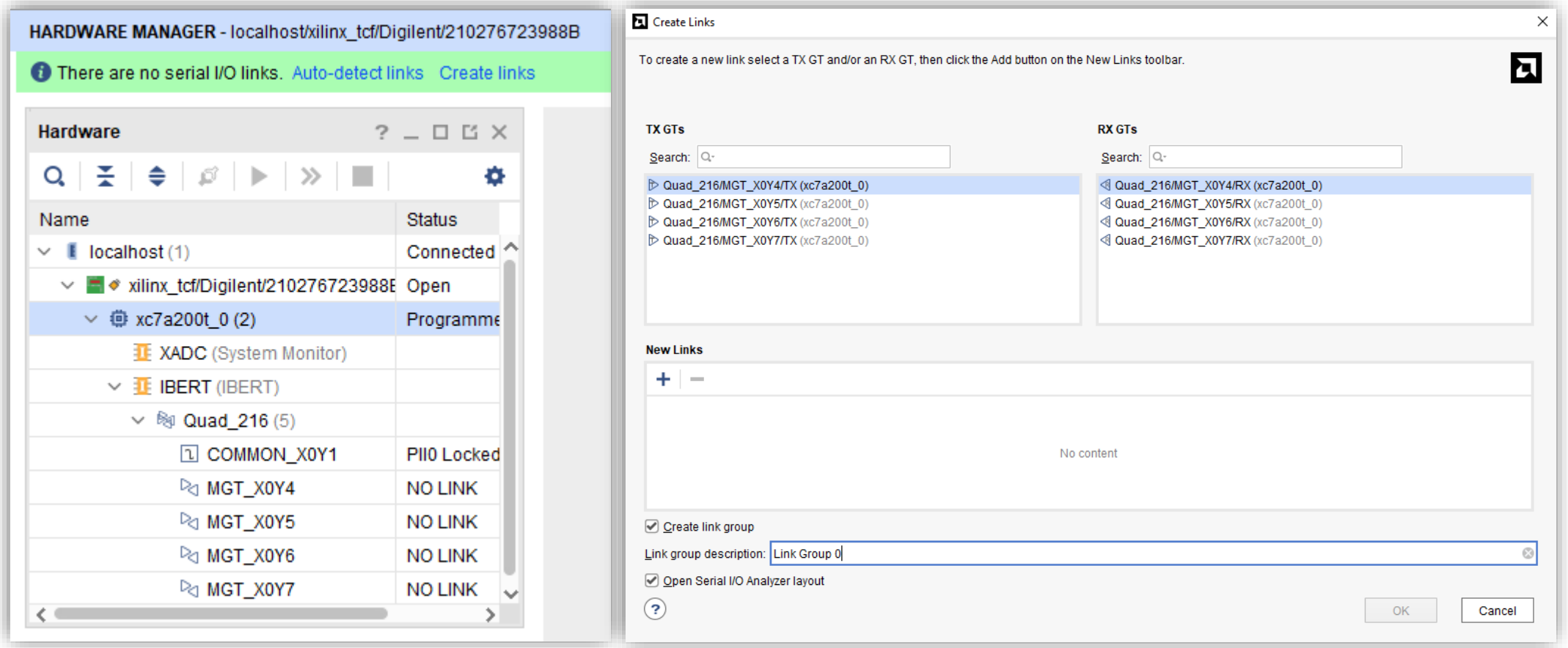
Open IBERT Example Design

You can generate an example design by right-clicking on the IP.



IBERT Links

The next step is to generate the bitstream file and program it into the FPGA for testing.
After programming, you can let VIVADO automatically detect or manually add the channels you want to observe.



IBERT Status & Parameter

You can use the status to determine whether the linking process was successful.
If the linking is not successful, first check whether the PLL has locked (if not, recheck the reference and system clock).
In addition, you can adjust various parameters and patterns or enable loopback modes for testing.

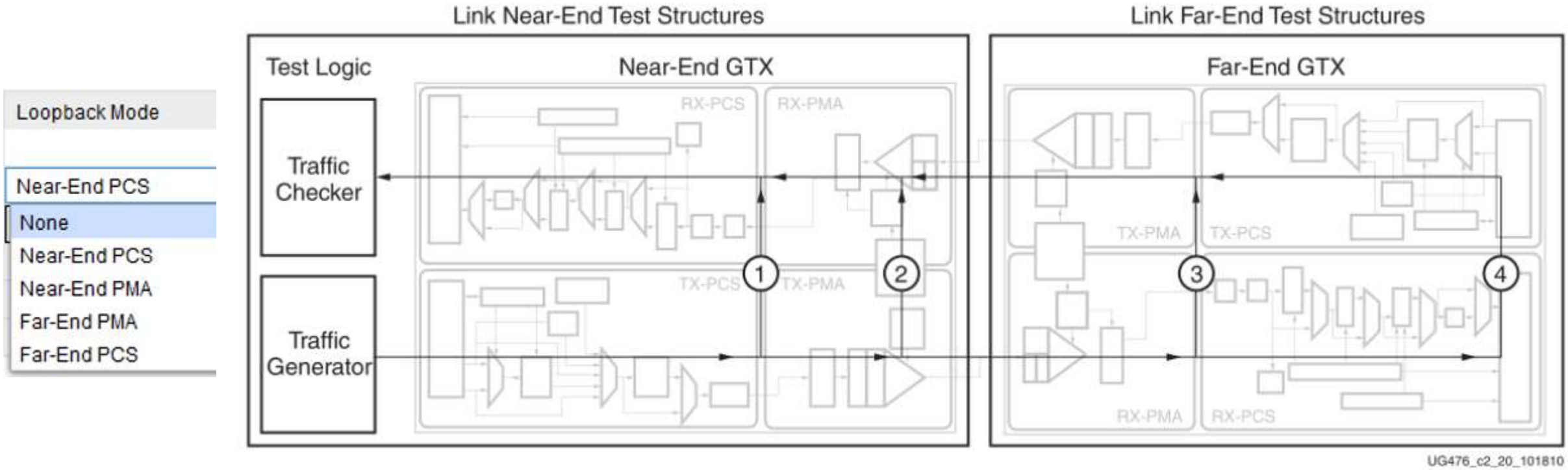
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset
Ungrouped Links (0)							
Link Group 0 (4)							Reset
Link 0	Quad_216/MGT_X0Y4/TX (xc7a200t_0)	Quad_216/MGT_X0Y4/RX (xc7a200t_0)	3.131 Gbps	1.953E11	1.539E9	7.882E-3	Reset
Link 1	Quad_216/MGT_X0Y5/TX (xc7a200t_0)	Quad_216/MGT_X0Y5/RX (xc7a200t_0)	3.118 Gbps	1.944E11	1.567E9	8.062E-3	Reset
Link 2	Quad_216/MGT_X0Y6/TX (xc7a200t_0)	Quad_216/MGT_X0Y6/RX (xc7a200t_0)	3.131 Gbps	1.953E11	1.538E9	7.878E-3	Reset
Link 3	Quad_216/MGT_X0Y7/TX (xc7a200t_0)	Quad_216/MGT_X0Y7/RX (xc7a200t_0)	3.131 Gbps	1.953E11	1.538E9	7.878E-3	Reset

TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)

RX PLL Status	TX PLL Status	Loopback Mode
		Near-End PCS
Locked	Locked	None
Locked	Locked	Near-End PCS
Locked	Locked	Near-End PMA
Locked	Locked	Far-End PMA
		Far-End PCS

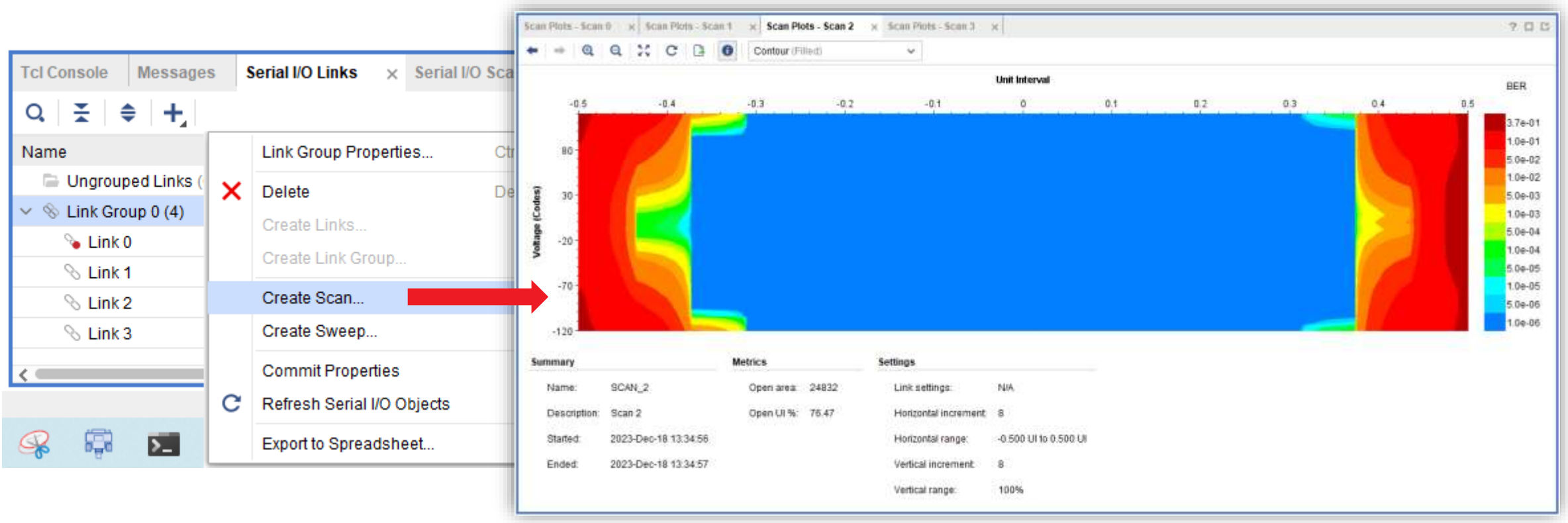
IBERT Loopback Mode

Loopback modes can be selected based on the diagram; for example, if you want to perform single-ended transmit and receive tests, choose Near-end. For remote testing, choose Far-end for the testing end.



Versal IBERT Example Design

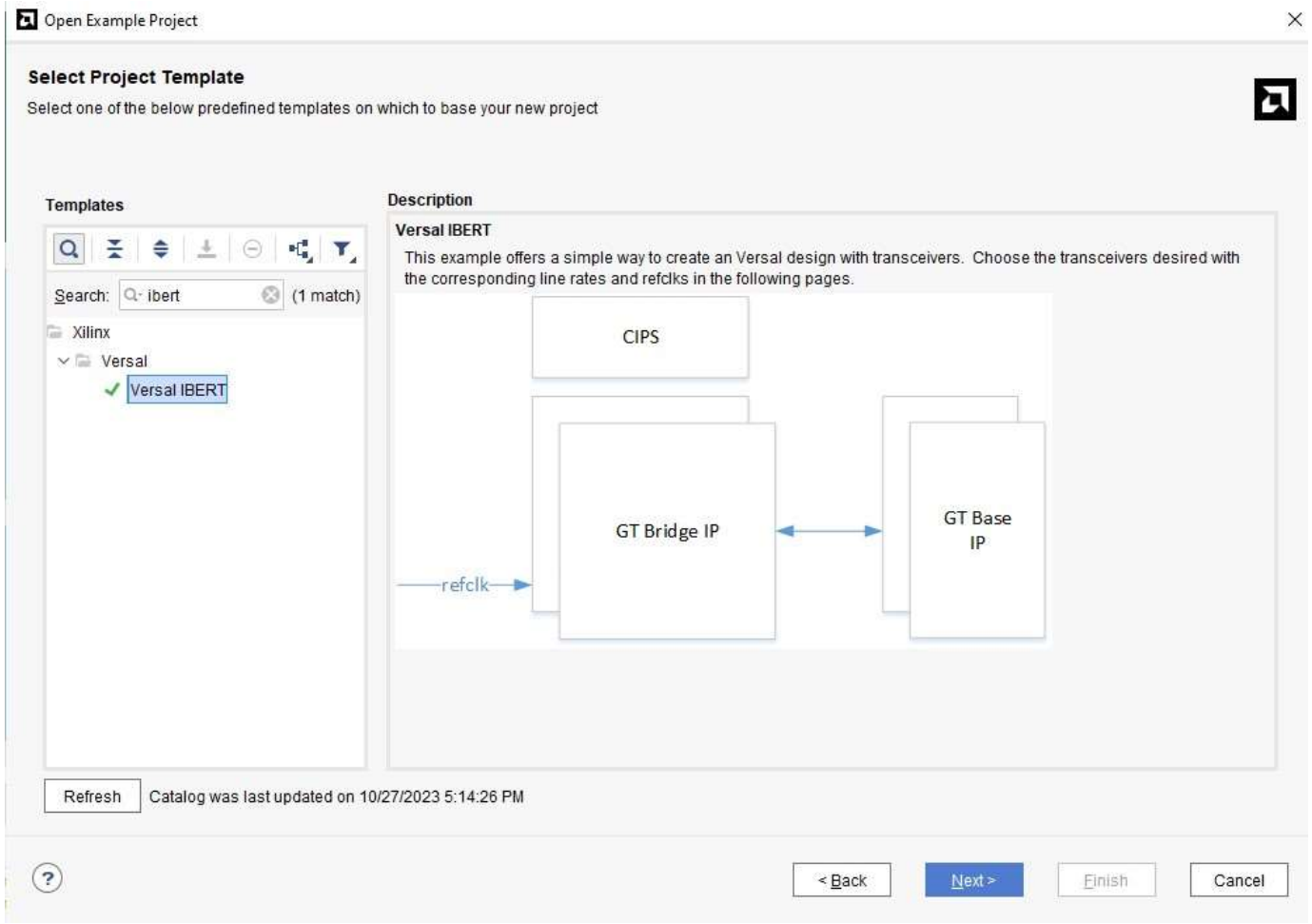
After adjusting all the settings, right-click to generate an eye diagram.
You can see the values on the right side, and when the color is closer to blue, it indicates a stronger signal.



Versal IBERT

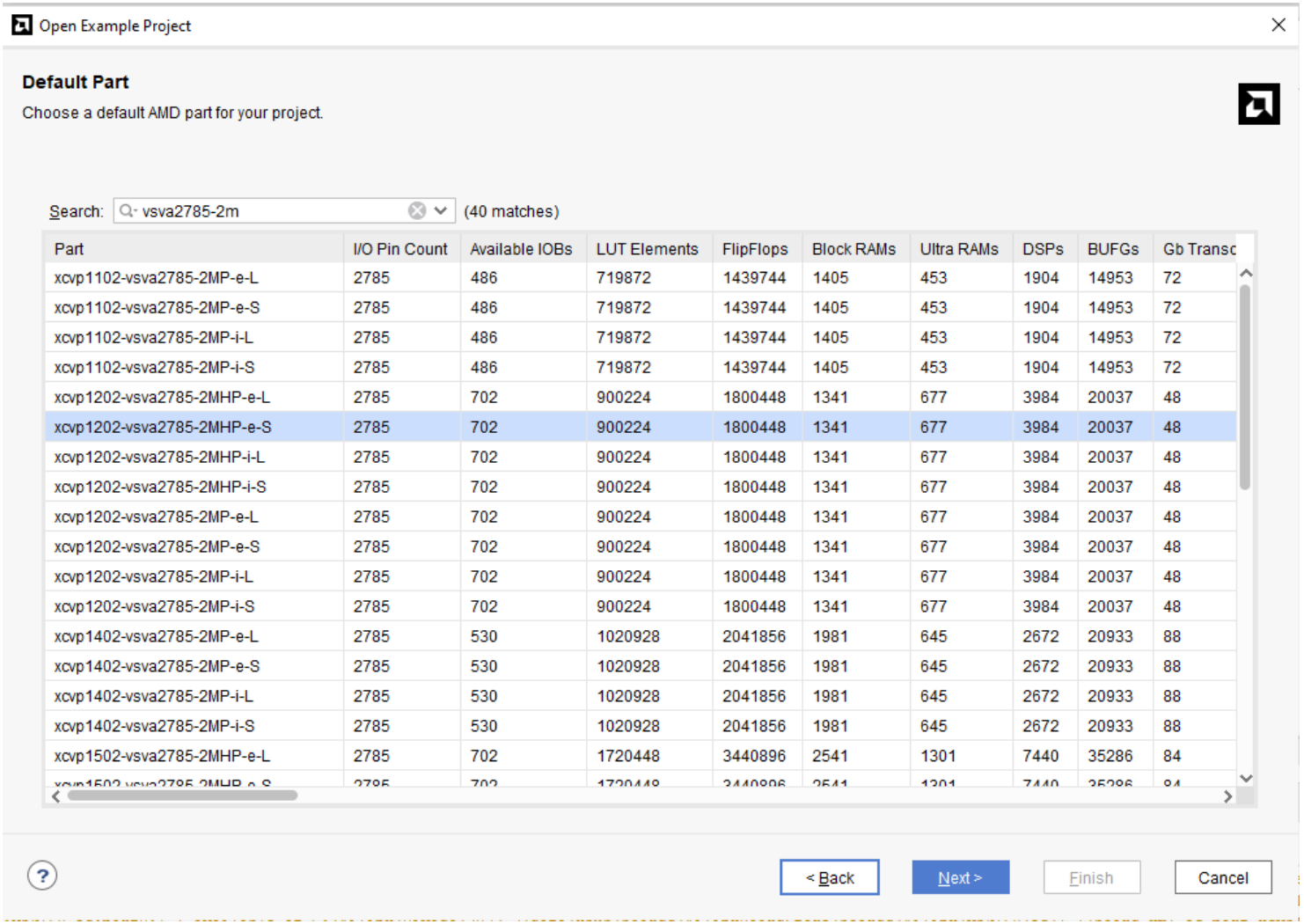
Versal IBERT Example Design

The design consists of a specific flow that will ensure success and repeatability by leveraging built in Vivado example designs and flows. This same flow can be used with deviations later, in order to test different bandwidths, GTs or other board capabilities. The design can be simply explained with the following block diagram



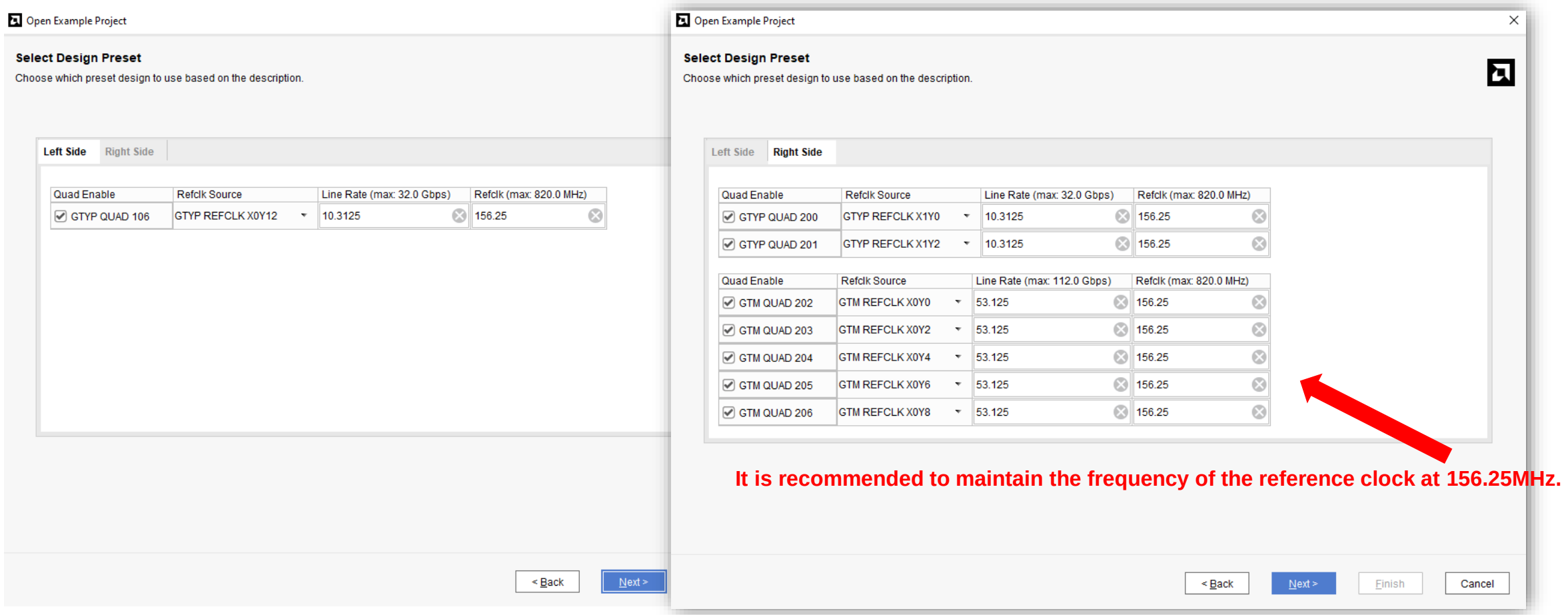
Versal IBERT Example Design

In the Default Part selection, click on the Part column header, which will sort the parts repeatably13. Scroll nearly 5/6 of the way down and select xcvp1202-vsva2785-2MP(or2MHP)-e-S



Versal IBERT Example Design

Here we can select the GTYP/GTM for our IBERT design.
The GTs are broken up into a left and right side well as broken into QUADs



Versal Transceiver Mapping

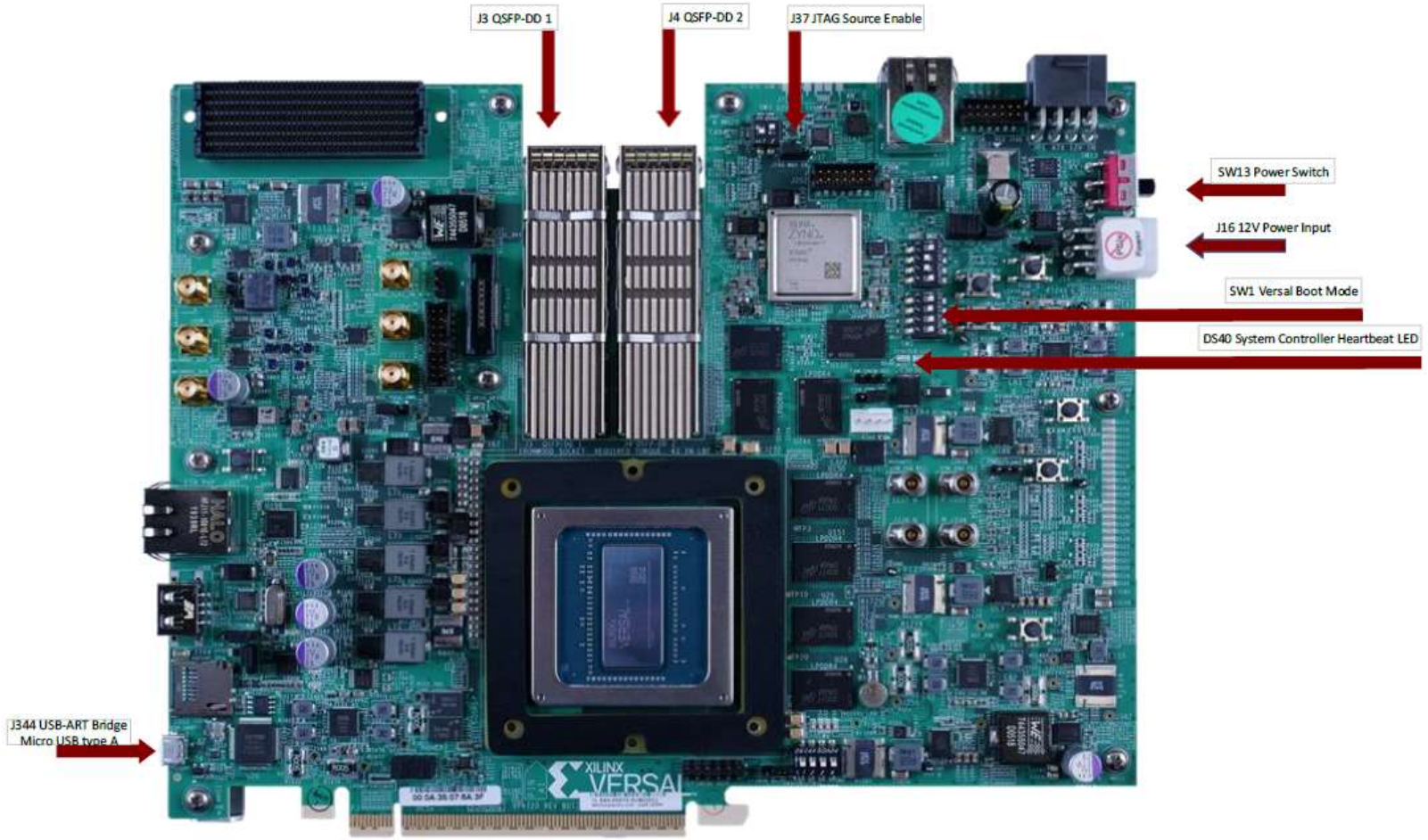
- In the User Guide, the Transceiver Mapping table has more detail as the included hardened IP blocks associated with specific transceiver quads are mapped out including which clocks are associated with each quad
- This might be used if testing and tuning specific QUADs to be used with specific hardened IP is necessary for future designs
- The default value of 156.25 MHz has already been programmed at the factory for the clock source. This mean the 8A34001 (U219).
- If a different frequency is desired, refer to the BoardUI programming tool as well as Renesas programming instructions.

Table: Transceiver Mapping

VPK120 XCVP1202 VSVA2785 GTY/GTM Mapping								
[Unused]	ch3	GTYP Quad 106 X0Y6	PCIe X0Y1		MRMAC X0Y1	GTM Quad 206 X0Y4	ch3	GTM SMA
[Unused]	ch2						ch2	8A34001 1PPS Clocks
[Unused]	ch1						ch1	[Unused]
[Unused]	ch0						ch0	[Unused]
[Unused]	refclk1						refclk1	8A34001 CLK6 IN
[Unused]	refclk0						refclk0	8A34001 Q7 OUT
PCIe Lane 0	ch3	GTYP Quad 105 X0Y5	CPM5			GTM Quad 205 X0Y3	ch3	QSFPDD1 Lane 1
PCIe Lane 1	ch2						ch2	QSFPDD1 Lane 5
PCIe Lane 2	ch1						ch1	QSFPDD1 Lane 2
PCIe Lane 3	ch0						ch0	QSFPDD1 Lane 6
[Unused]	refclk1						refclk1	[Unused]
PCIe Edge Clock 0	refclk0						refclk0	8A34001 Q8 BUF0
					DCMAC X0Y0			
PCIe Lane 4	ch3	GTYP Quad 104 X0Y4	CPM5 (HSDP)			GTM Quad 204 X0Y2	ch3	QSFPDD1 Lane 3
PCIe Lane 5	ch2						ch2	QSFPDD1 Lane 7
PCIe Lane 6	ch1						ch1	QSFPDD1 Lane 4
PCIe Lane 7	ch0						ch0	QSFPDD1 Lane 8
[Unused]	refclk1						refclk1	8A34001 CLK5 IN MUX1
PCIe Edge Clock 1	refclk0						refclk0	8A34001 Q8 BUF1

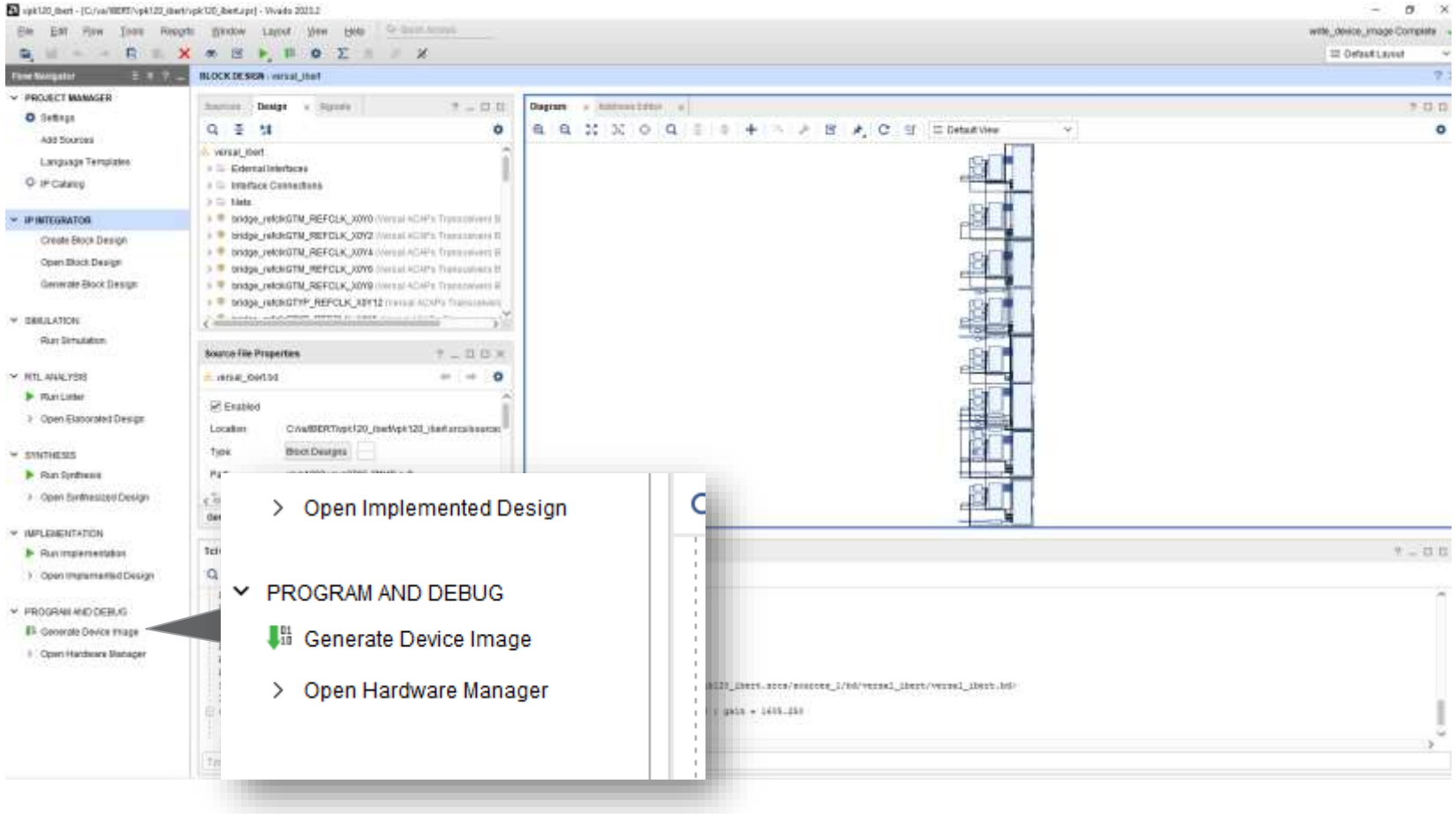
Board Component Location

Ensure the included loopback adapter (Multilane ML4062-LB-112) is inserted and FULLY seated in the QSFPDD-1 (J3) cage / connector(If you are using the official PDI file provided in RDF0636,)



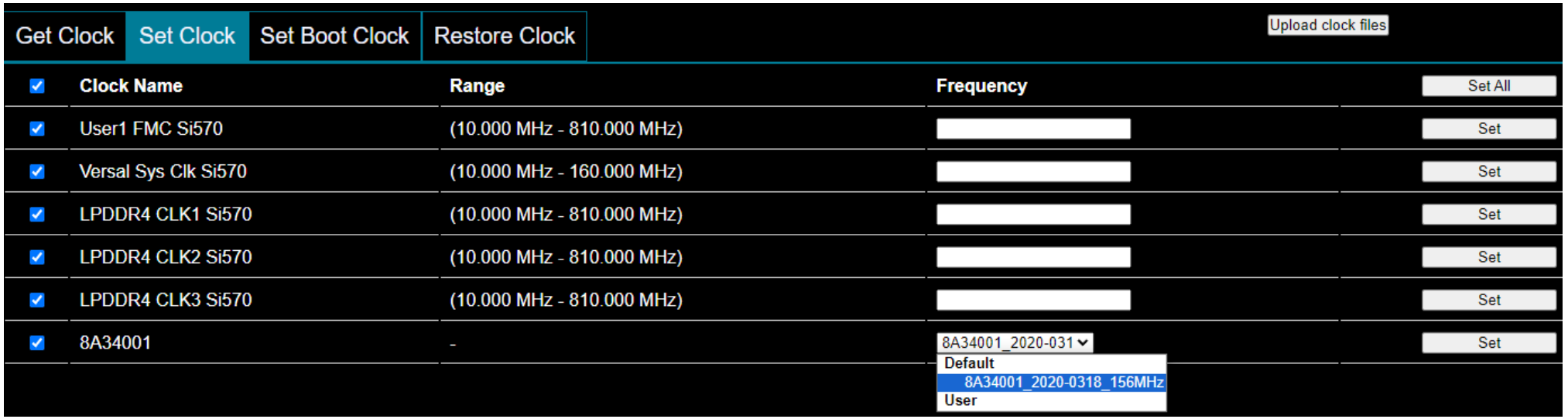
Generate Device Image

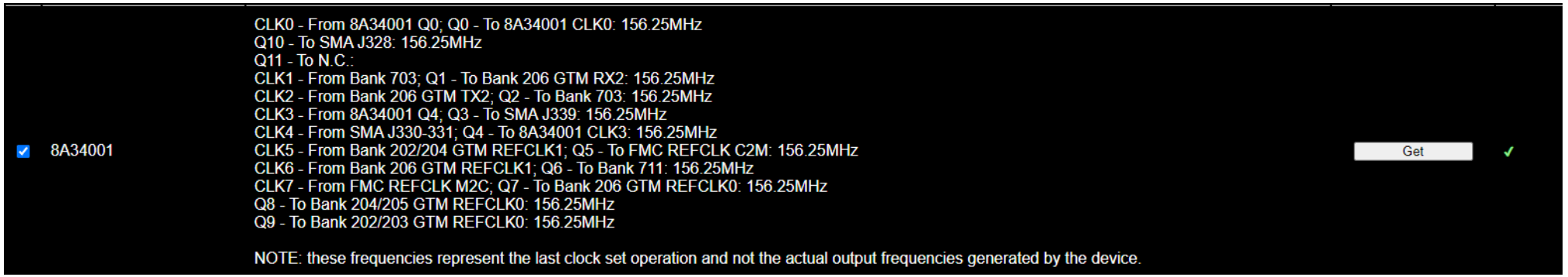
Once the project is initialized, as mentioned in the beginning overview, now is the time to review settings, by opening the Block Design and then opening the details of the various IP generated for you
Once satisfied, or if you do not wish to review, select Generate Device Image from the Flow Navigator



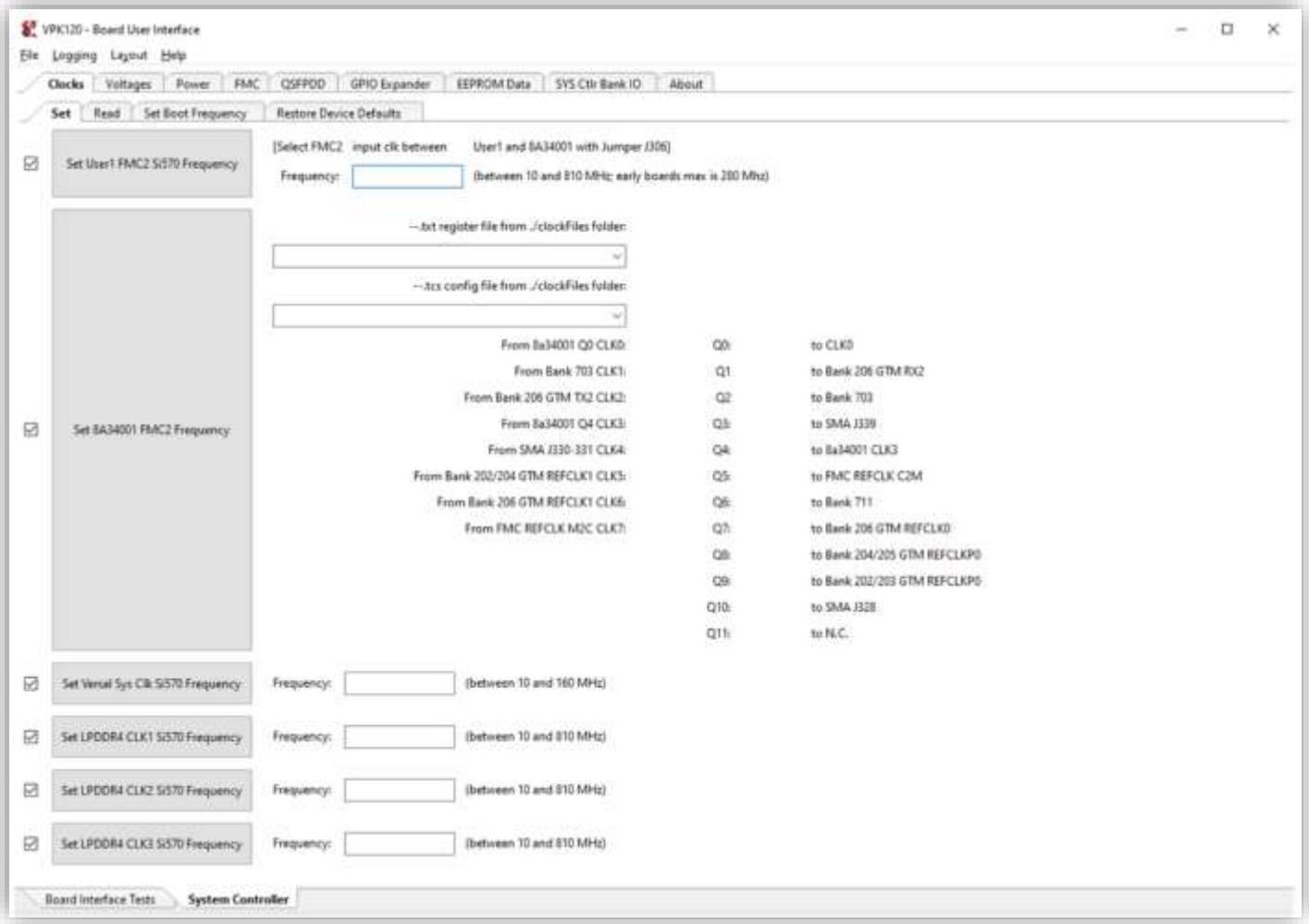
Modify Refclk Frequency

Before programming, it is necessary to adjust the frequency of 8A34001 to 156.25.
You can use either BoardUI or BEAM to utilize the System Controller for adjustment.





Modify Refclk Frequency



A brief summary is provided here.

1.Ensure the Skyworks/Silicon Labs VCP USB-UART drivers are installed. See the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).

2.Download the board user interface host PC application from the VPK120 Evaluation Board website.

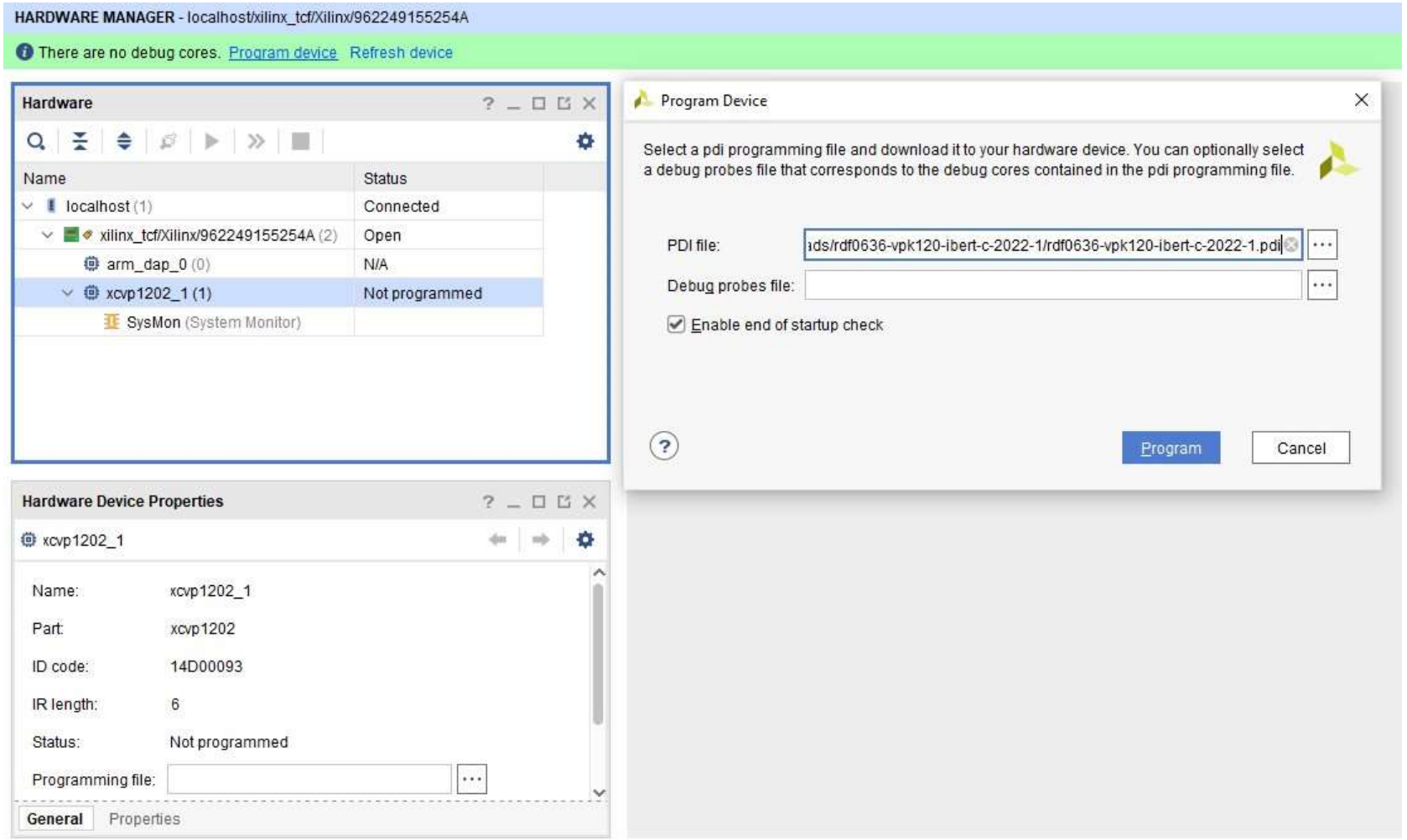
3.Connect a USB cable to VPK120 USB-UART USB-A connector (J344).

4.Power-cycle the VPK120.

5.Launch the board user interface application.

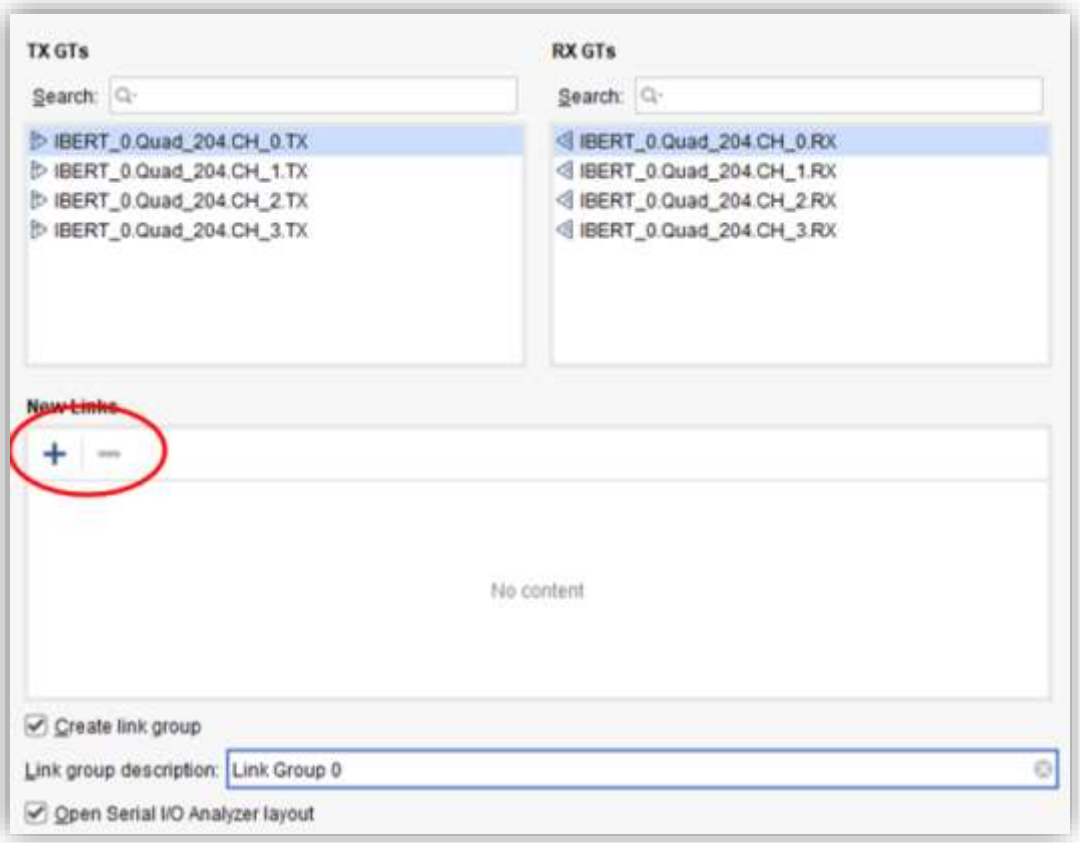
Program Device

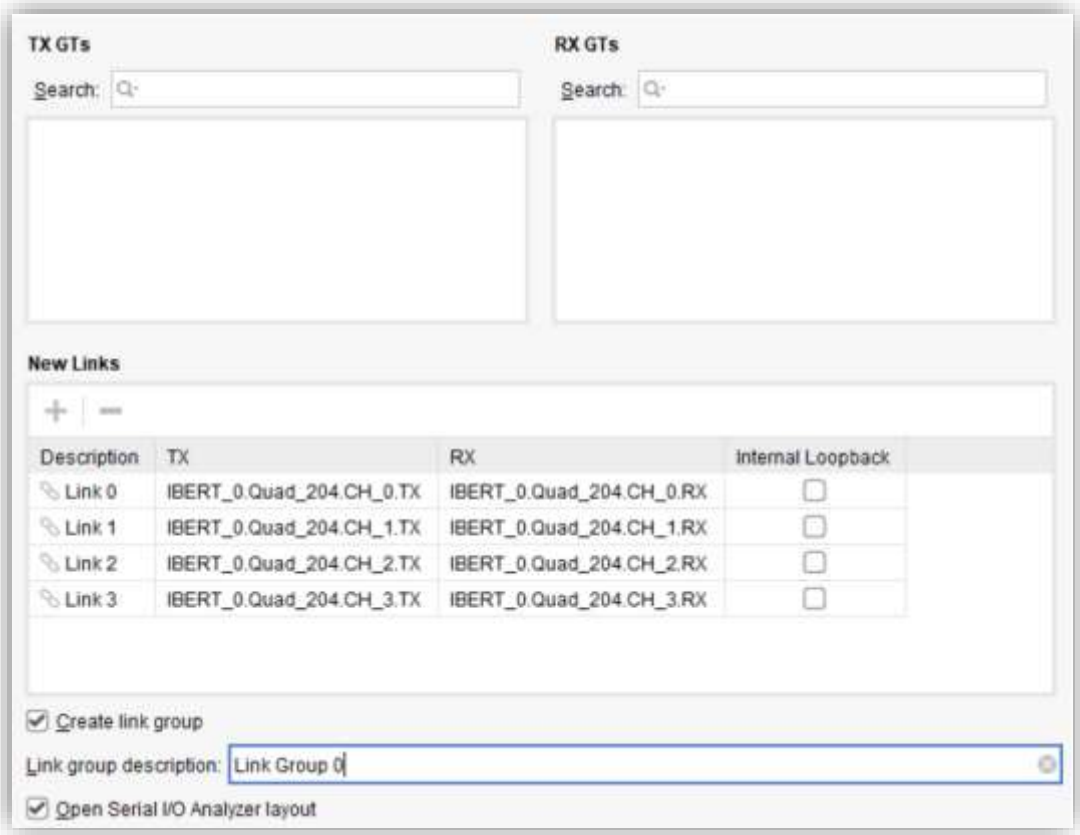
If you are programming the prebuilt PDI, select the file here and program.
Once completed, the IBERT Real-Time Scan Plots are opened



Create Links

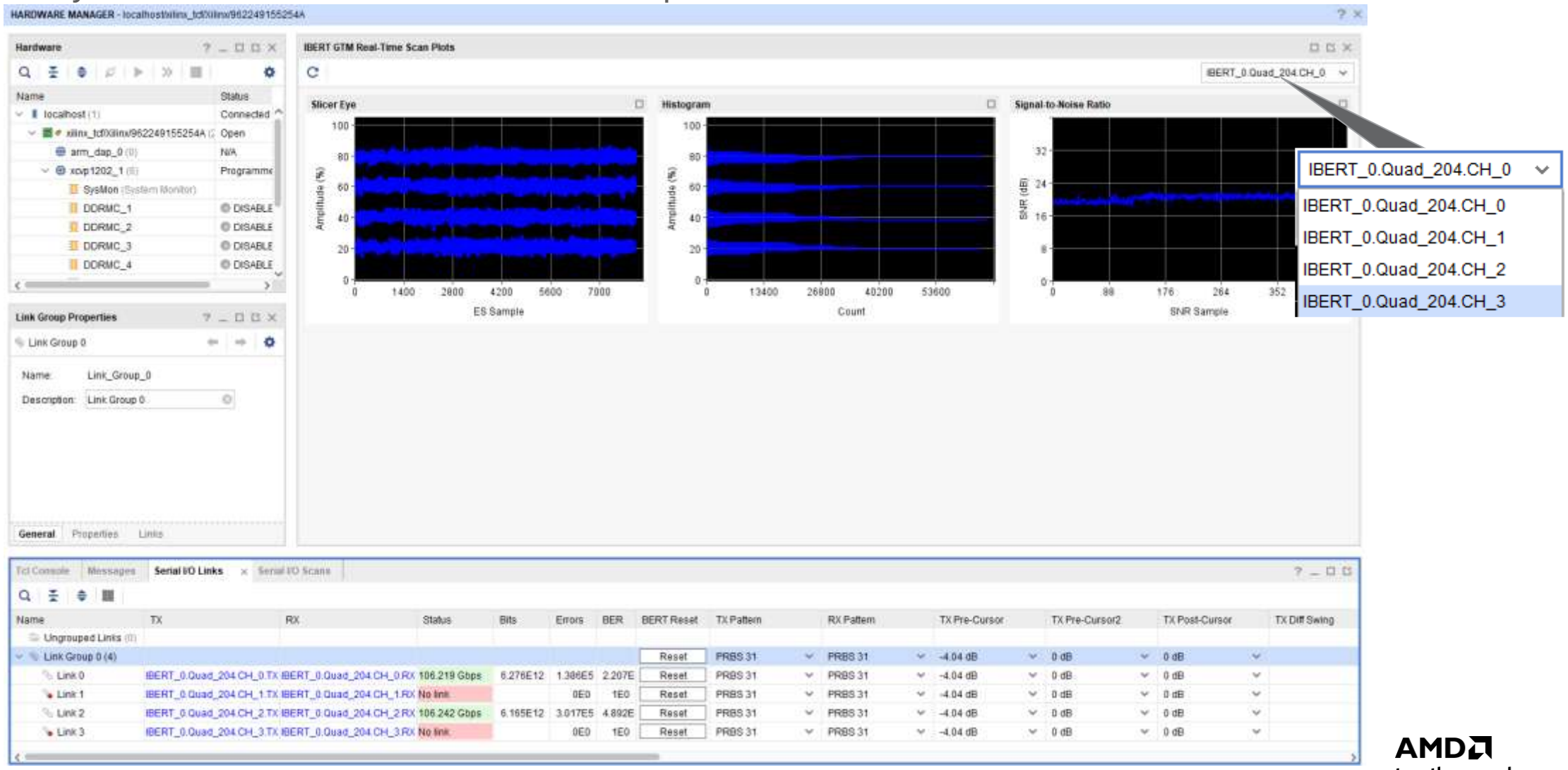
In the Serial I/O Links tab, select Create Links.
Note: Depending on configuration, it can be prohibitively long to run “Auto-detect links”
• In the following pop-up dialog, select a 1:1 for each channel such that the New Links area is populated as shown. This is done by clicking the large + while you have two channels selected





Versal IBERT View

Using this, you can view each individual channel's plots.



PLL Status

- Verify is that the PLLS are locked. Scroll the tab to the right and locate the PLL columns

- If the PLL does not show lock, please review whether the refclk is set correctly.

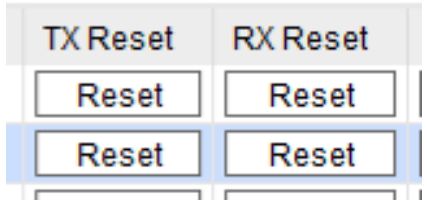
RX PLL Status	TX PLL Status
Locked	Locked
Locked	Locked
Locked	Locked
Locked	Locked

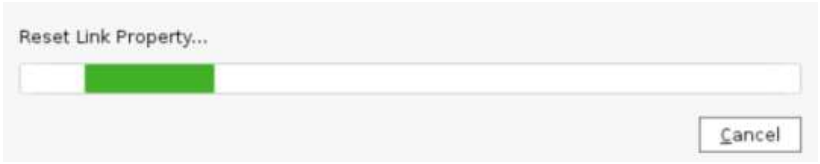
Parameter adjustment.

For the VPK120, example performance tuning has been completed and it is suggested to change the TX Pre-Cursor, TX Pre-Cursor2, TX Post-Cursor and TX Main-Cursor for Link 0 as suggested in the following image

TX Pre-Cursor	TX Pre-Cursor2	TX Post-Cursor	TX Main-Cursor
Multiple	Multiple	Multiple	Multiple
-4.04 dB	0 dB	0 dB	0.998 Vdd
User Design	User Design	User Design	User Design
User Design	User Design	User Design	User Design
User Design	User Design	User Design	User Design

As these are critical tunes, we will now need to reset the link

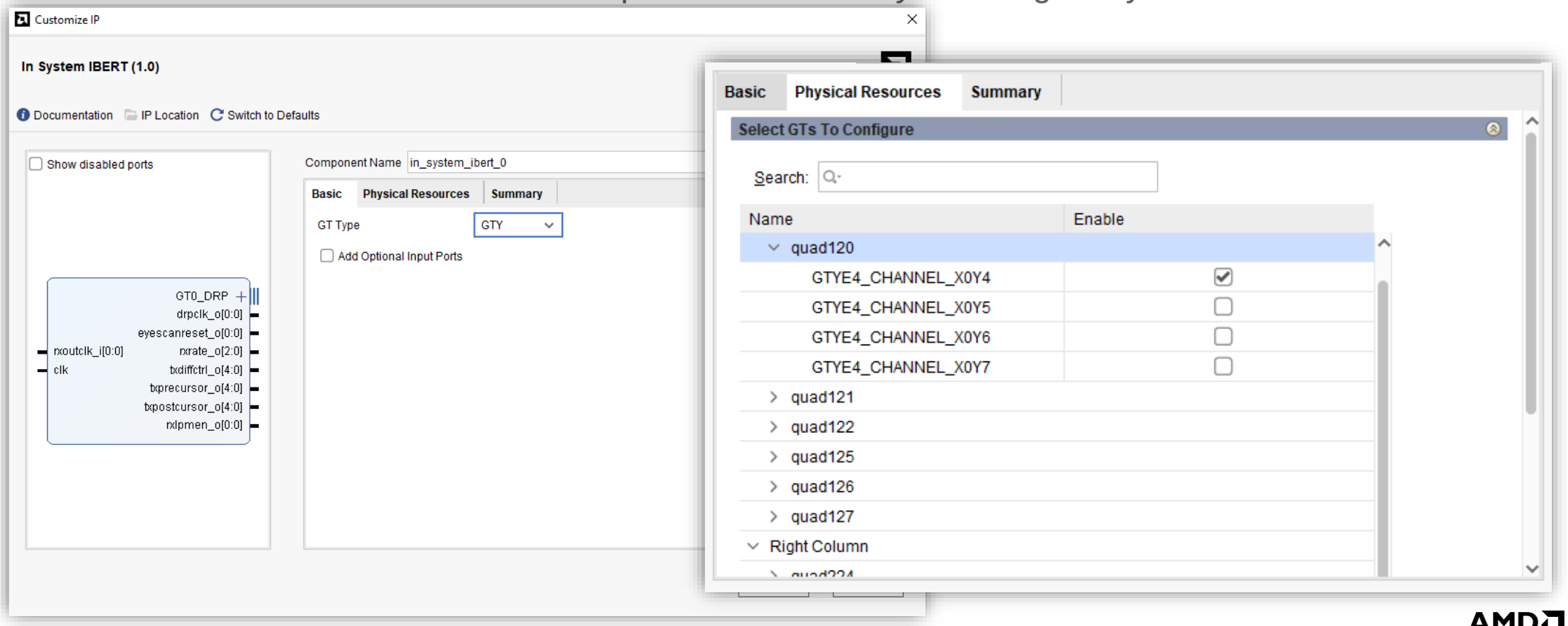




System IBERT

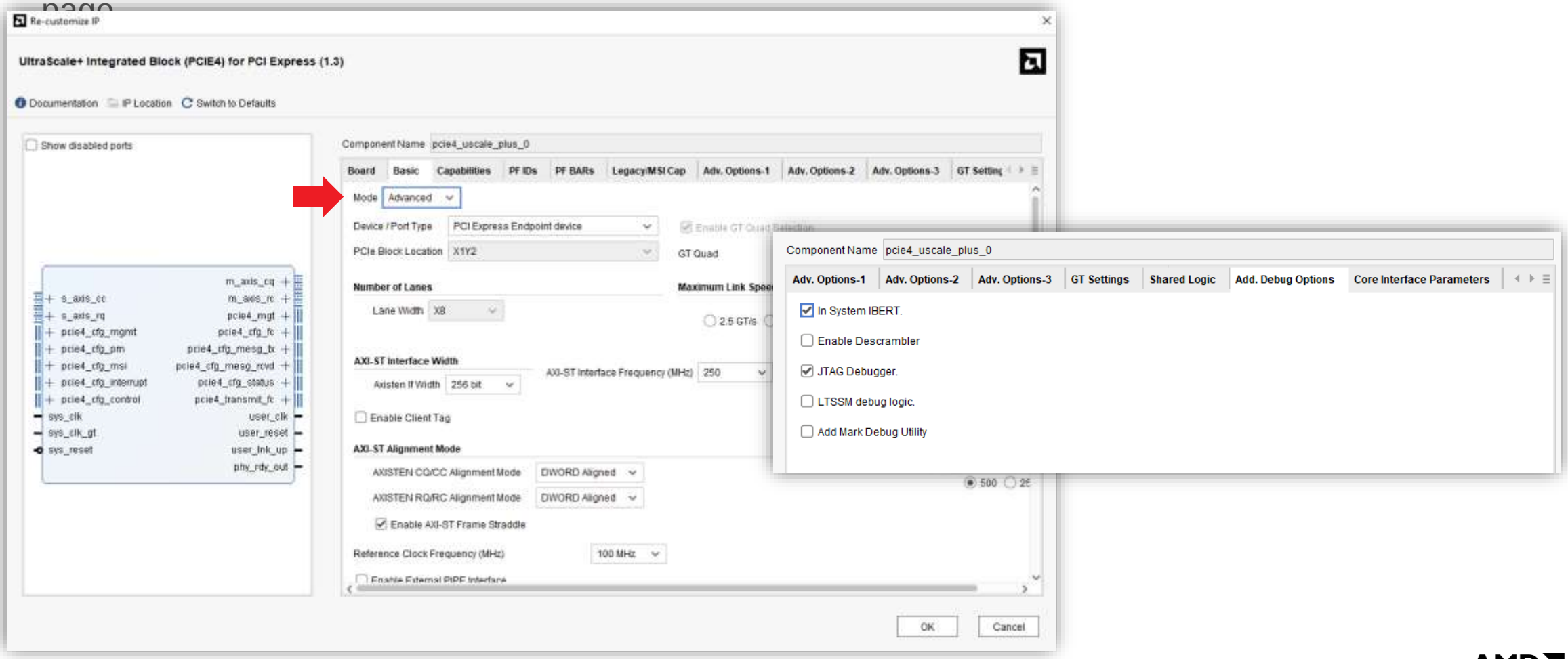
System IBERT

If you want to test the eye diagram of signals transmitted through the transceiver for a specific protocol (such as PCIe), you can choose to use System IBERT. There are two ways to add it. One is to connect it directly to the transceiver. However, when adding it in this way, vivado does not provide an example design. You will need to refer to the documentation to incorporate IBERT into your design on your own.



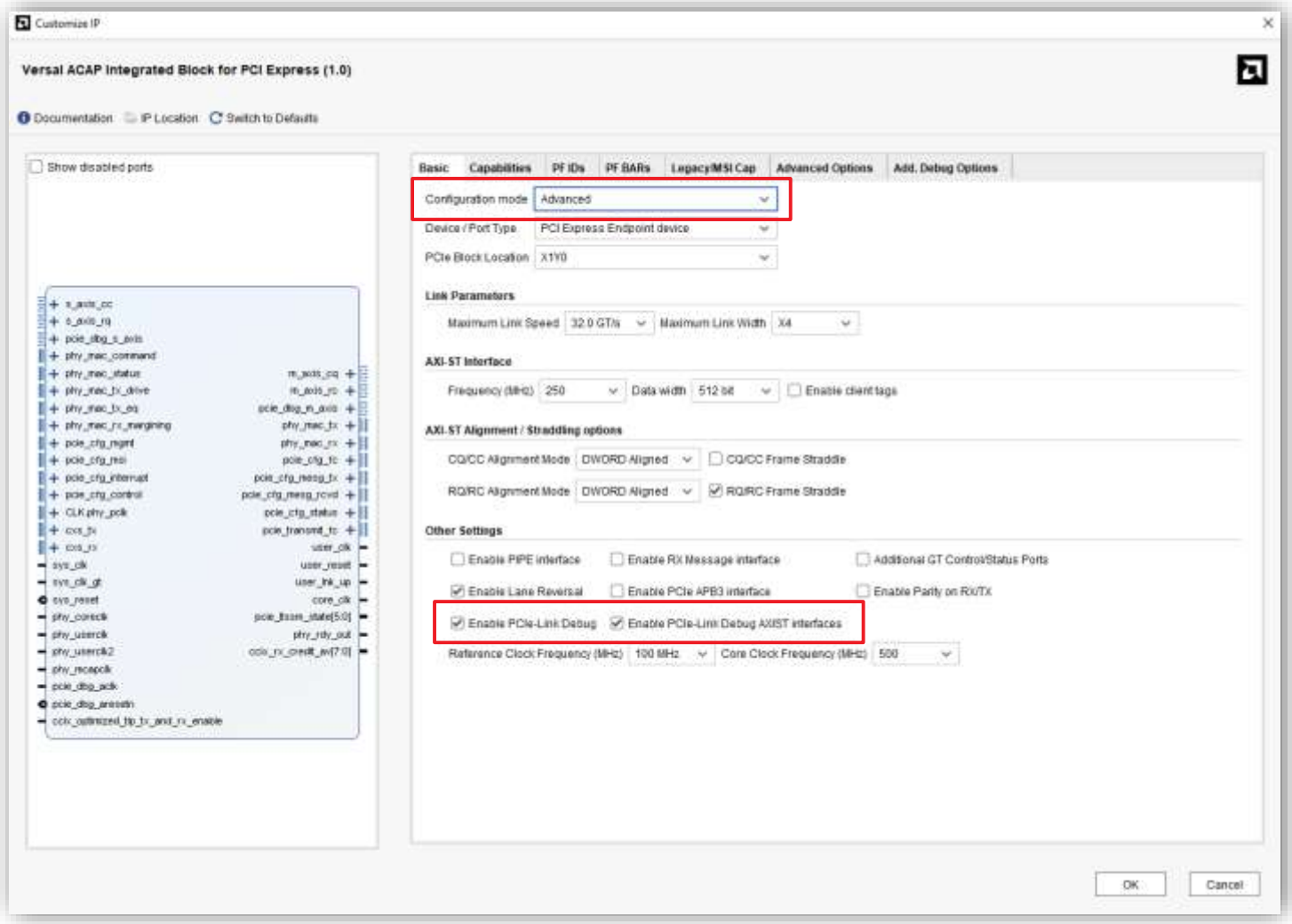
System IBERT

Another way is, if you are using our IP (here using PCIe as an example), you can directly add IBERT in the IP settings. Select advanced mode on the Basic page, and then you can directly add it in the Add. Debug page



Versal System IBERT

System IBERT



For Versal's System IBERT, this is the only
method provided, and the rest is not significantly different from before.

The only difference is the location of the adjustments in the IP Setting. Adjust according to the red box.