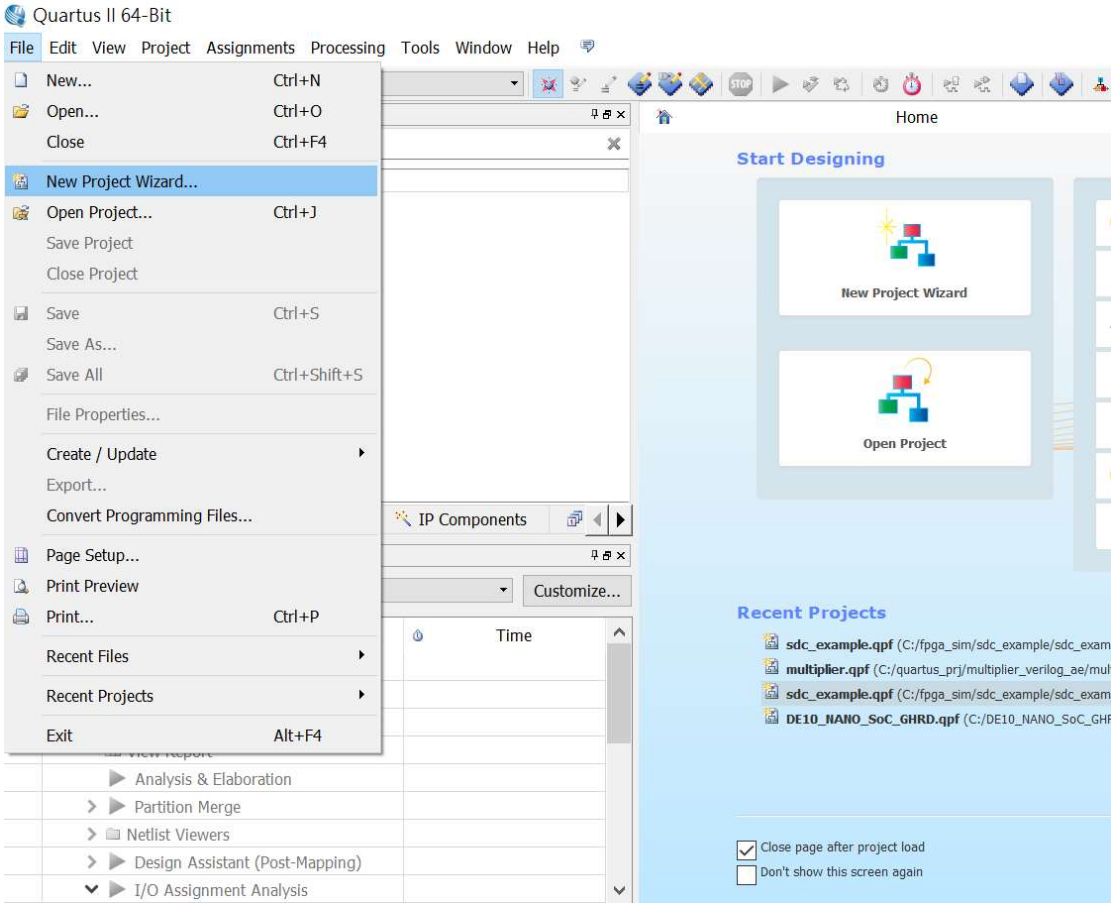
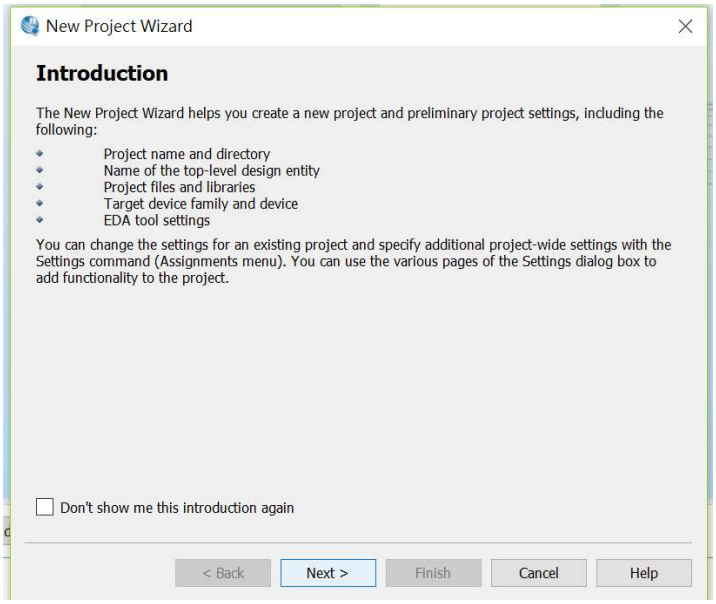
Intel® Quartus 操作流程

- Create Project Flow

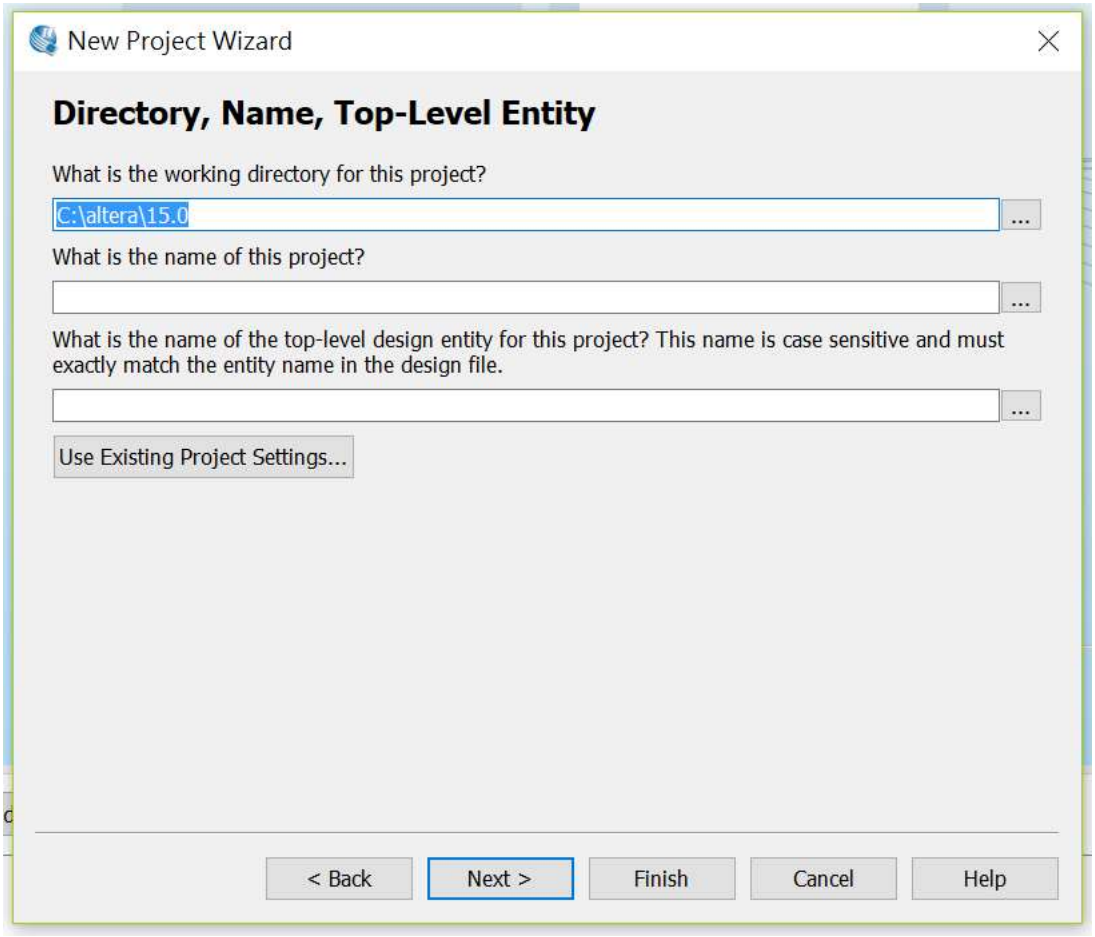
1. 用滑鼠左鍵點選 File -> New Project Wizart



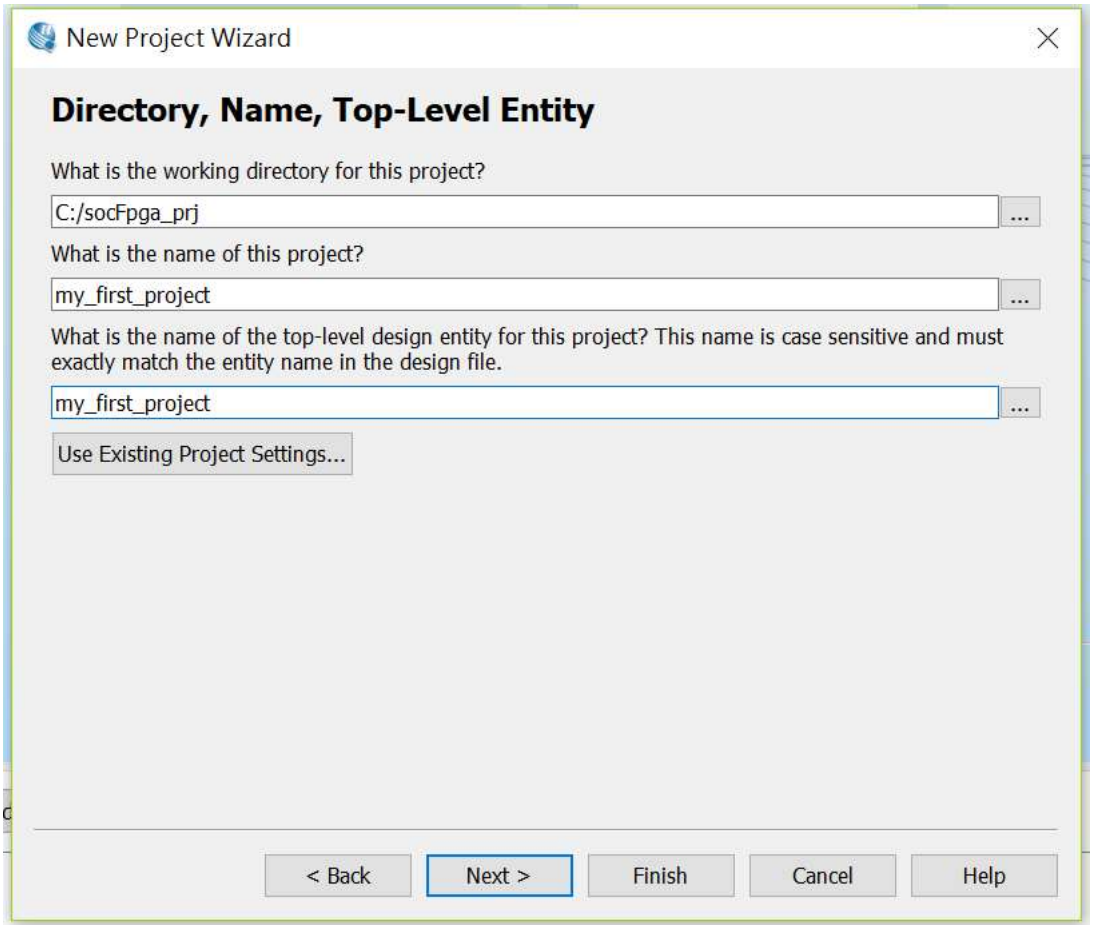
會出現如下的圖示



用滑鼠左鍵點選”Next”,接下去會出現下圖

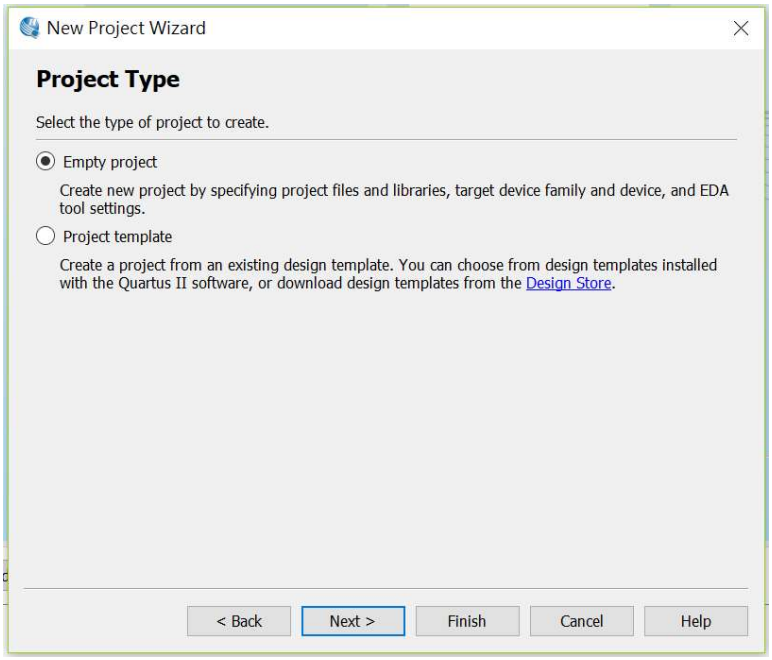


在上圖中的”What is the working directory for this project?”填入你想要放置專案的工作目的.在”What is the name of this project”寫入你想要的專案名稱.如下例所示:

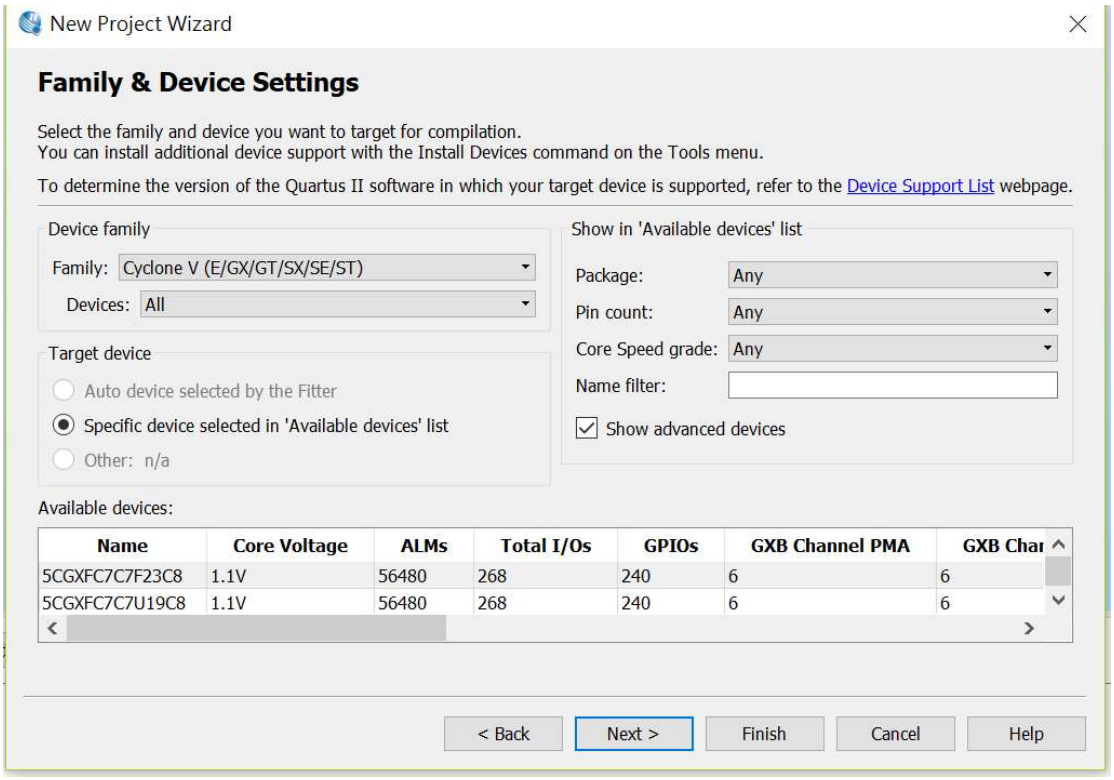


上圖例子所示即為工作目錄在 c:/socfpga_prj.工作專案名稱為 my_first_project

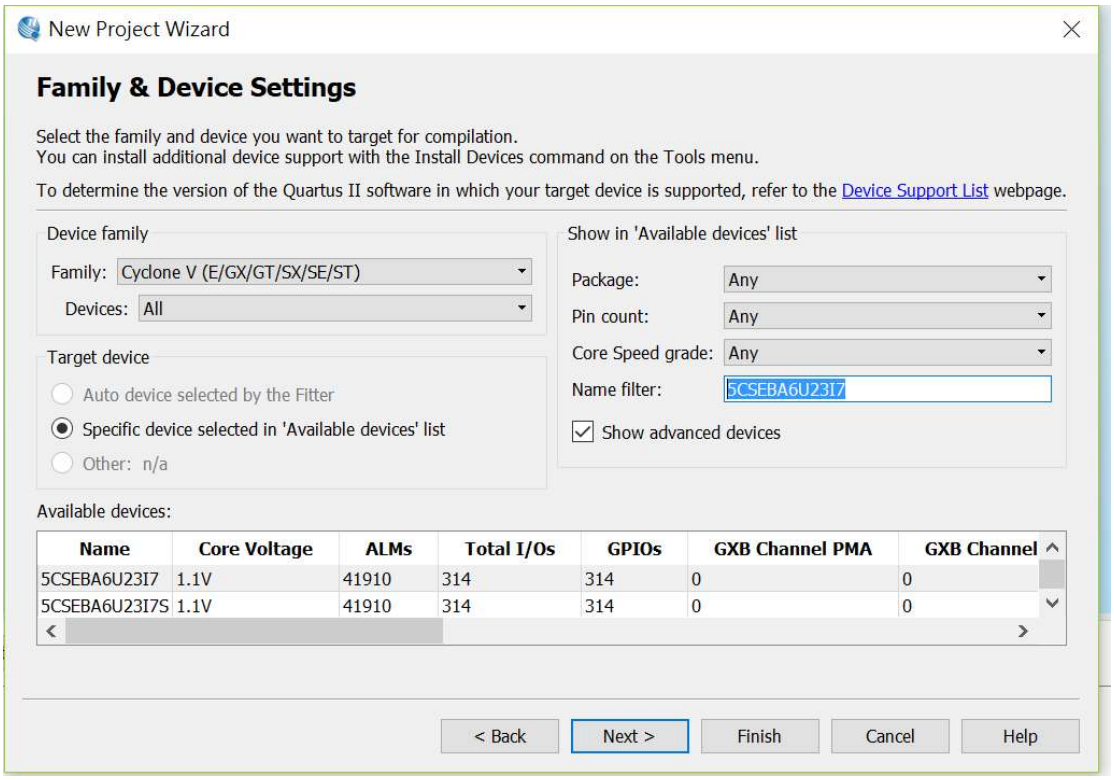
待設定完成後,再用滑鼠左鍵點選”Next”.即會出現下圖.



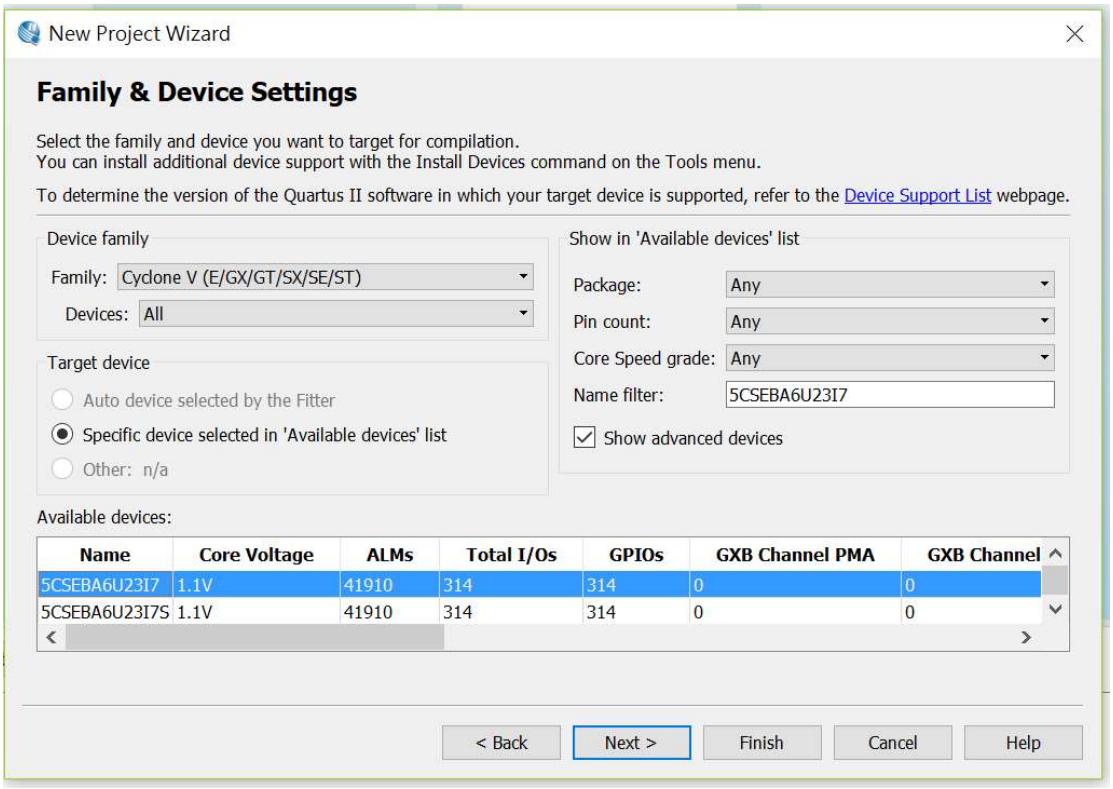
再用滑鼠左鍵點”Empty project”,後再選”Next”,會出現下面的視窗



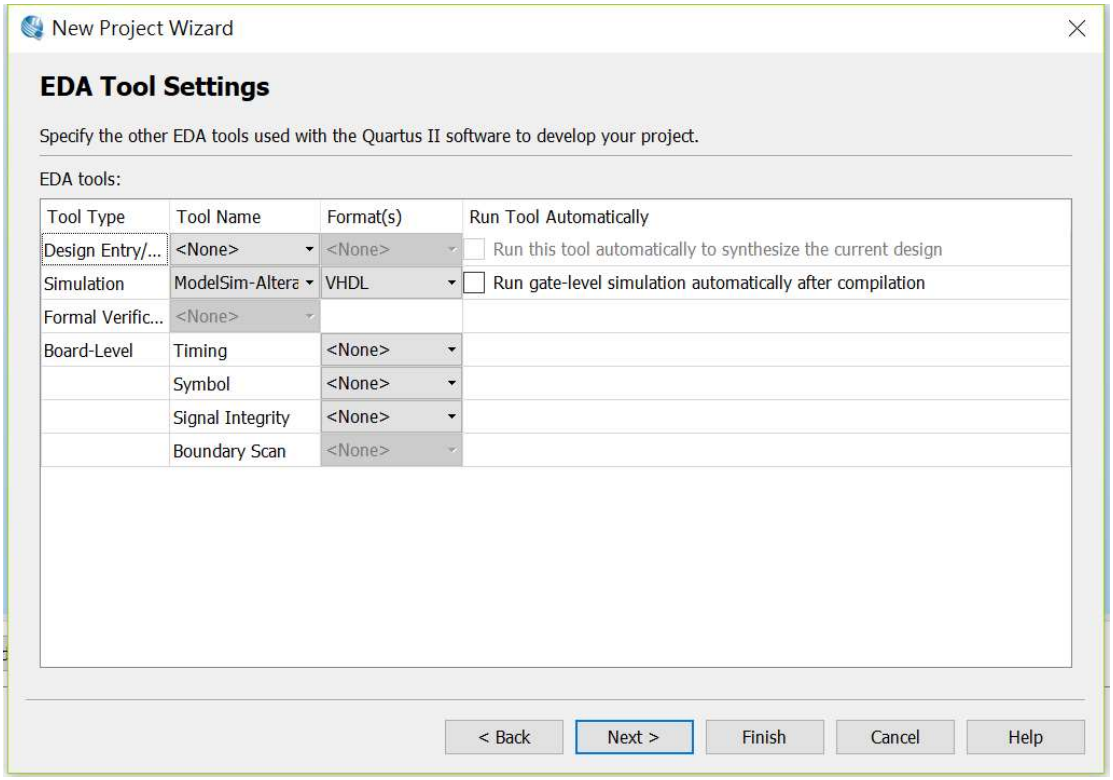
此視窗是用來選取工作專案預計要燒錄的FPGA型號.目前是使用Cyclone V SoC FPGA 5CSEBA6U23I7.所以在”Name filter”欄位填入5CSEBA6U23I7,即可以在Available devices中找到該型號.如下圖所示:



用滑鼠左錄在 Available device 中點選 5CSEBA6U23I7,即會看到該型號 FPGA 反白顯示,即代表已經選取.如下圖所示:

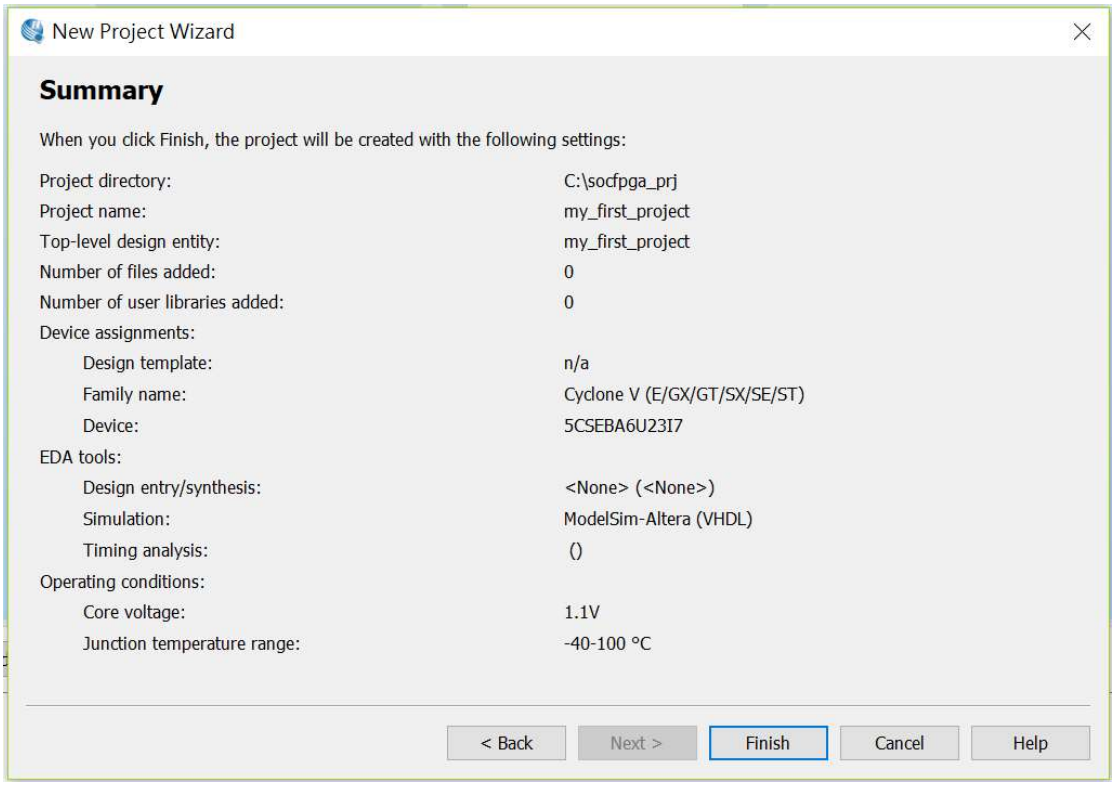


再用滑鼠左鍵點選”Next”,即會出現如下視窗.



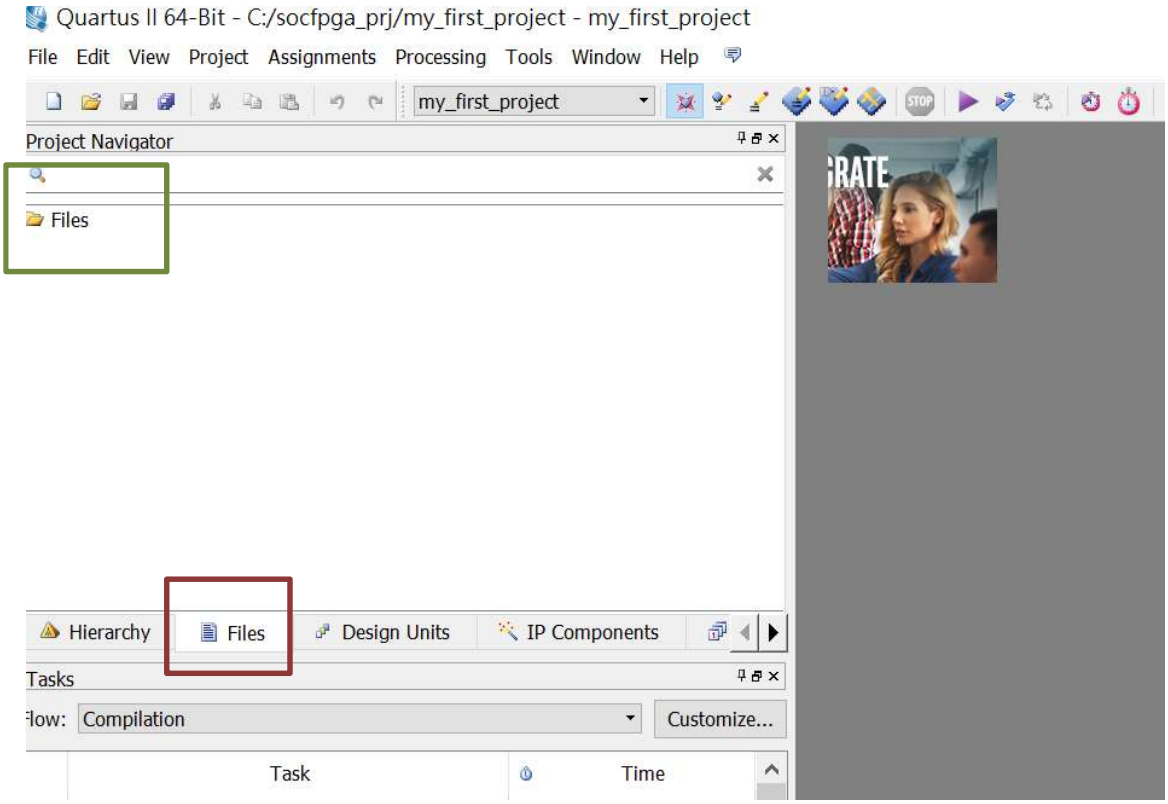
再用滑鼠左鍵點選”Next”,即會出現如下視窗.

確認出現視窗中的 Device 型號是否為 5CSEBA6U23I7.若是再用滑鼠左鍵點選”Finish”,即完成專案的建立.

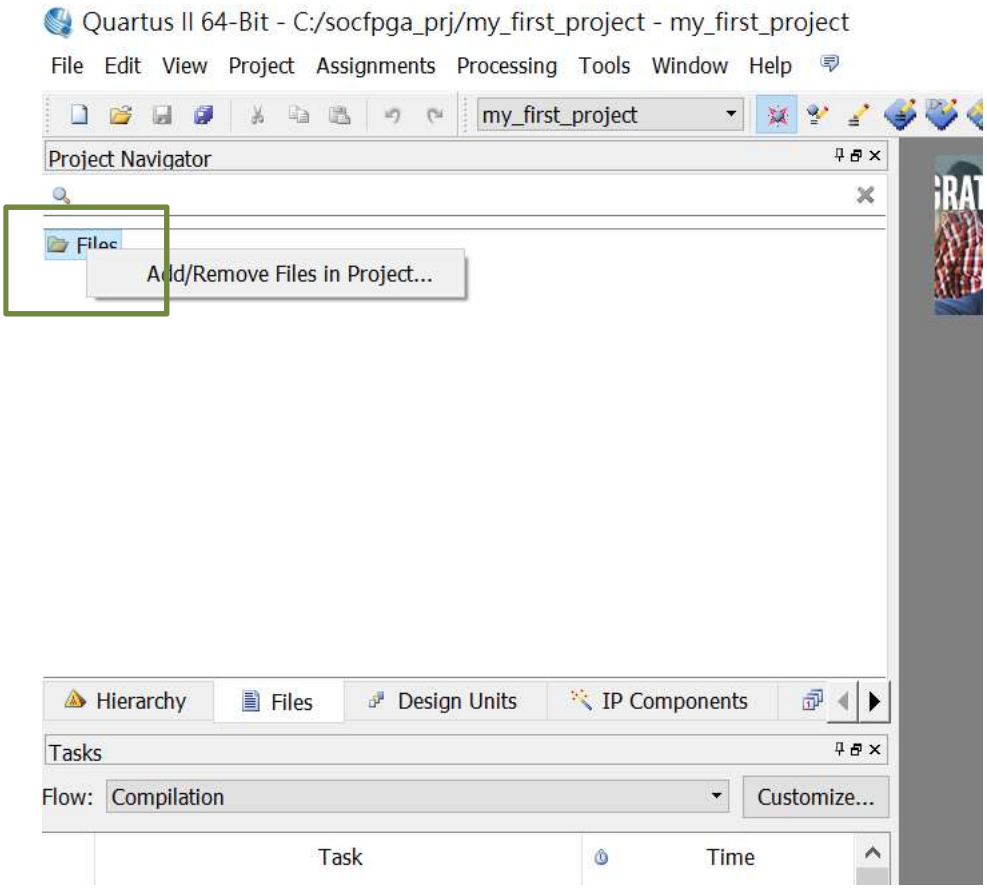


- **如何匯入檔案至專案中**

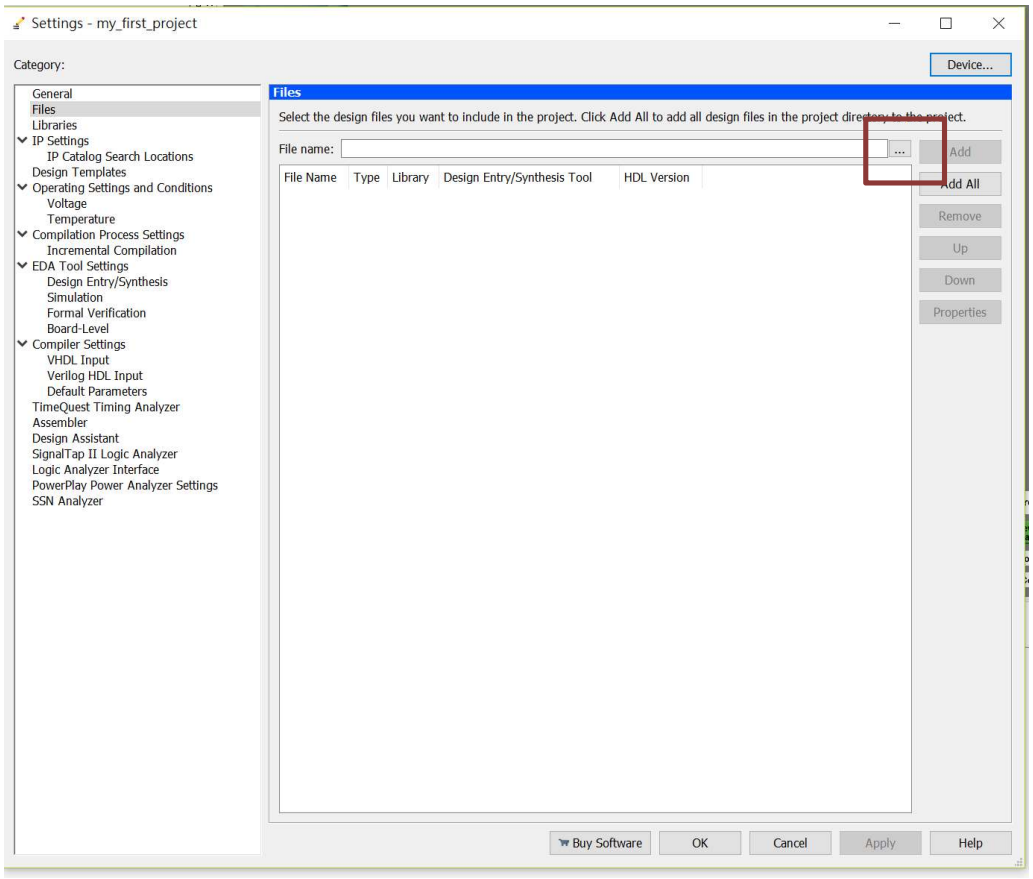
1.利用滑鼠左鍵點選 Project Navigator 中的 Files.如下圖紅方框所示,即會在 Project Navigator 中出現 Files 如綠方框所示:



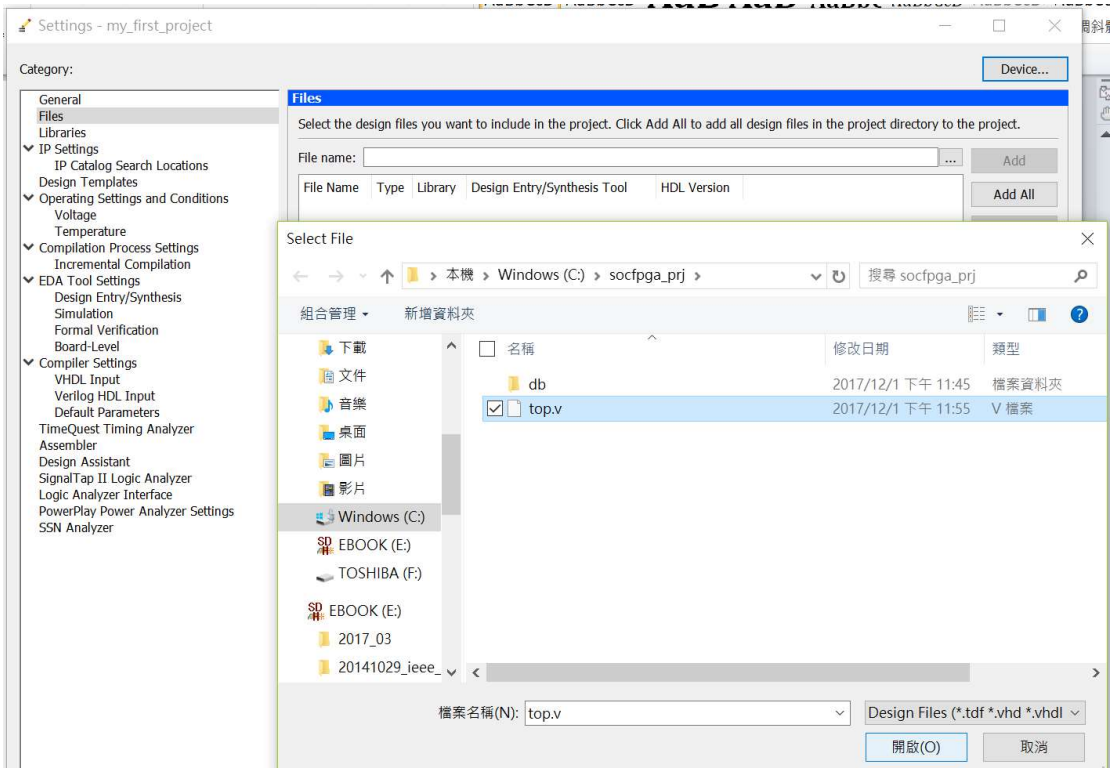
2.利用滑鼠右鍵點選 Project Navigator 中的 Files 如下圖綠框所示,即會跳出”Add/Remove Files in Project”的視窗,再用滑鼠左鍵點選.



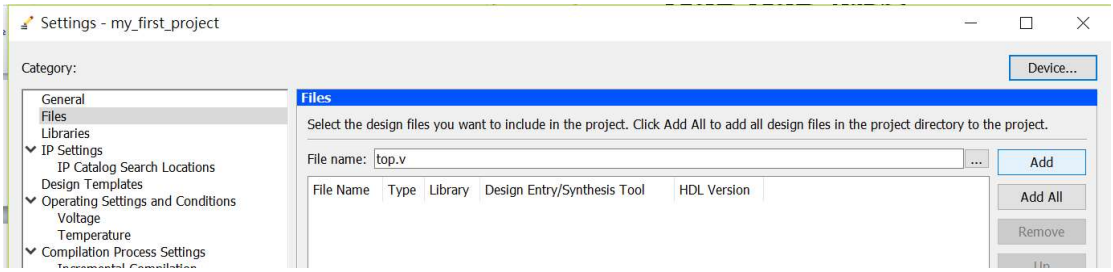
點選完後即會出現下列的視窗.再用滑鼠右鍵點說下圖紅框所示的位置



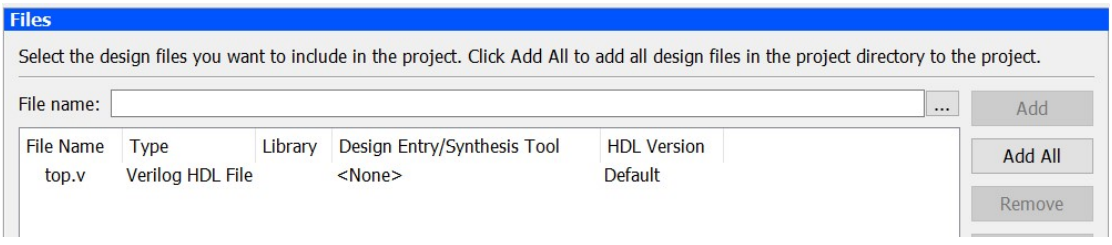
即會跳出如下的視窗,即可以選取想要加入的專案設計檔案(Verilog).再按”開啟”.注意此視窗可以一次點取多個檔案.



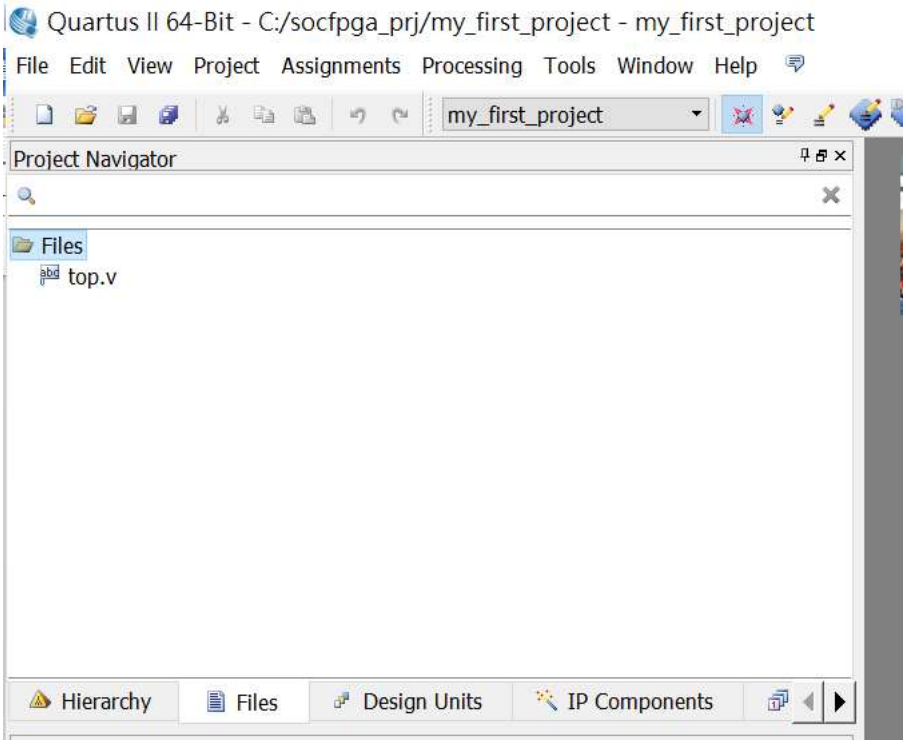
點選”開啟”之後,視窗即會出現如下圖所示.



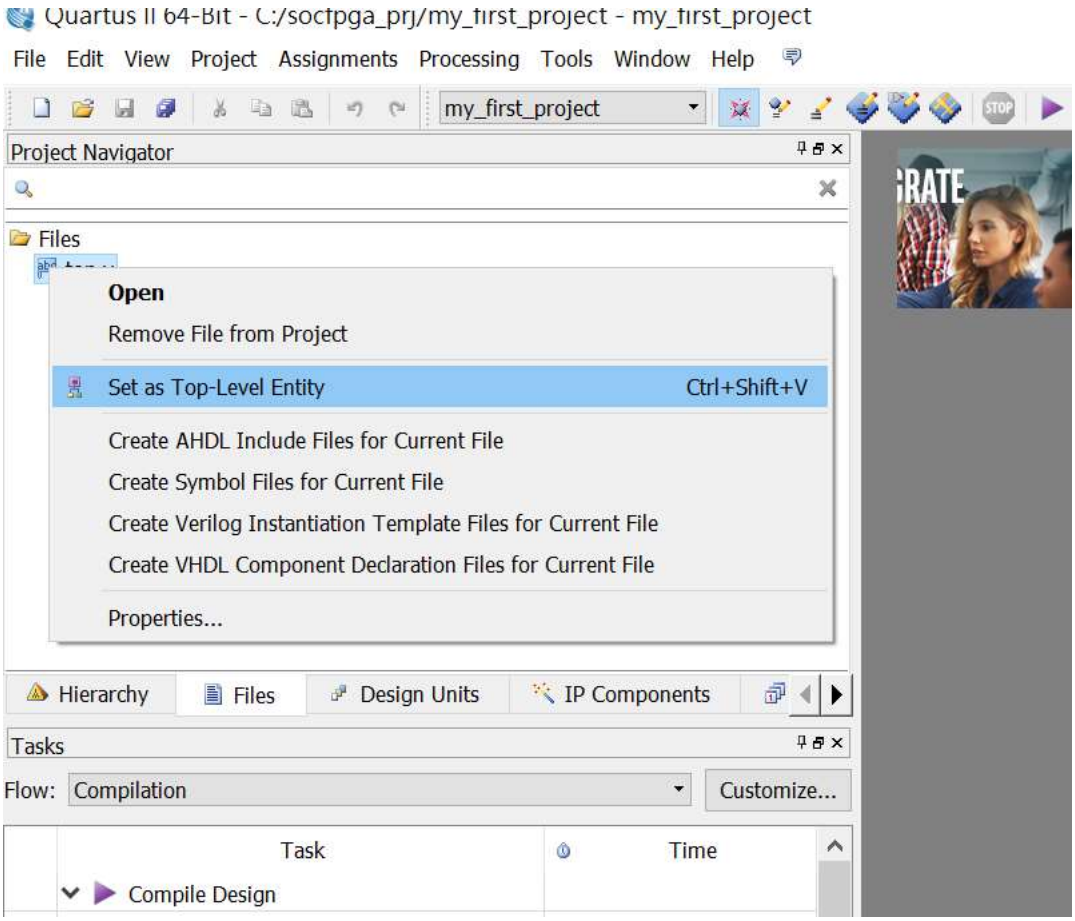
記得要再點按”Add”,所選取的檔案才算是真正地加入專案中.如下圖所示.



再點選”OK”.如果成功,則會在 Project Natigator 中看到專案的檔案.



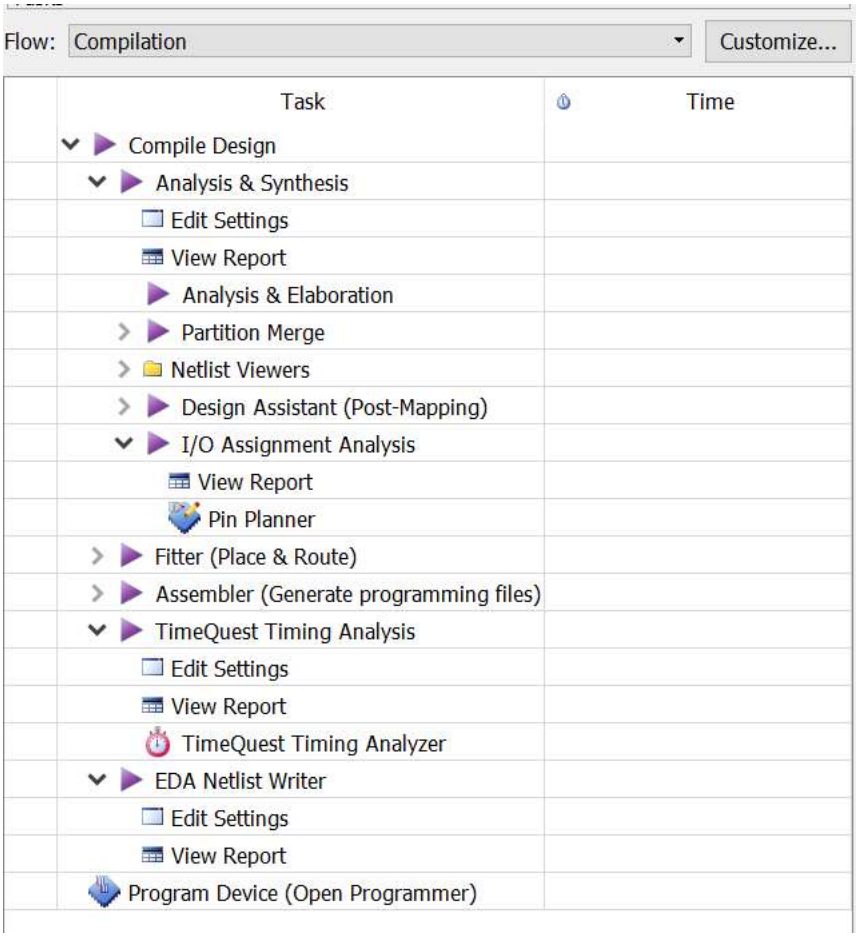
再將滑鼠的右鍵點選整個專案檔案的 Top Module Verilog File.此處是 top.v 如下圖所示:



再用滑鼠左鍵點選”Set as Top-Level Entity”.即完成將設計檔案加入專案的工作

- **<u>如何利用 Quartus 來設計體電路</u>**

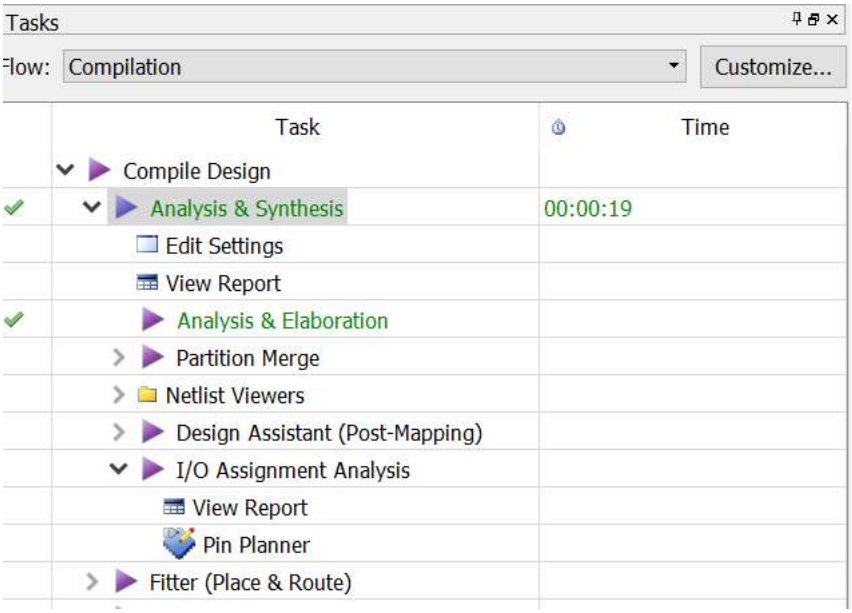
下圖是 Quartus compilation Flow 會執行的工作項目.



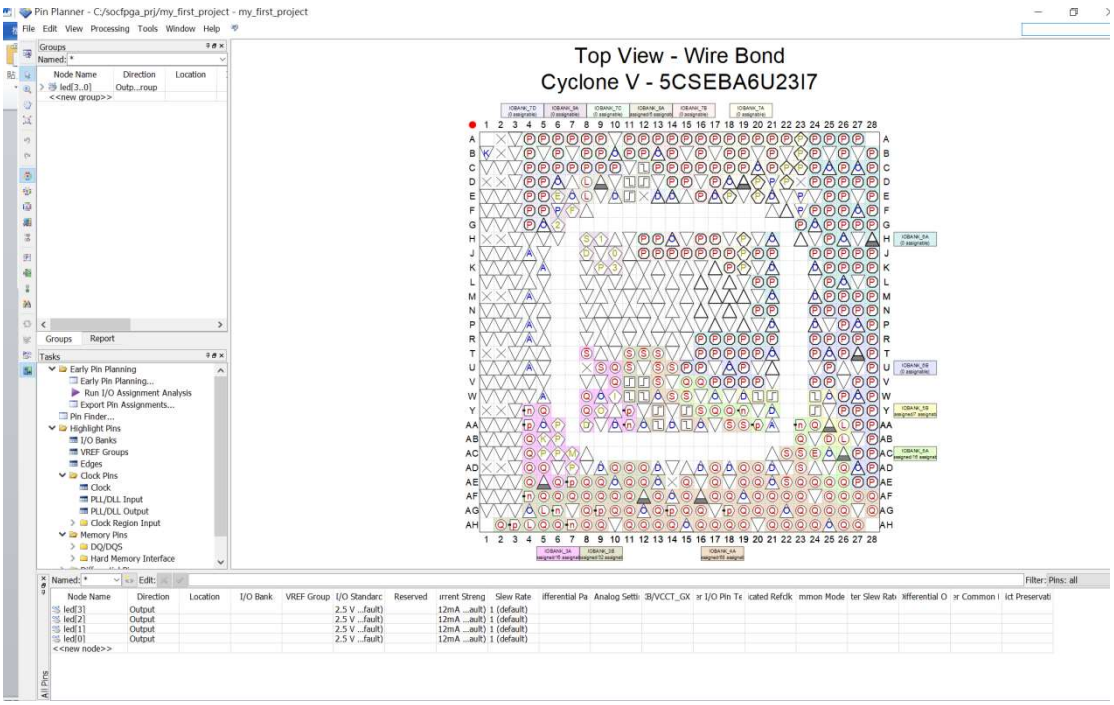
1. Analysis & Synthesis:
   甲、執行電路的語法檢查及電路合成
2. Filter(Place & Route:
   甲、執行電路元件的擺放及繞錄
3. Assembler
   甲、產生 FPGA Code 燒錄檔
   i. rbf: Cyclone V SoC SD Card 使用
   ii. pof:燒至 SPI Flash
   iii. sof:燒至 FPGA 中的 SRAM(for debug),關電即消失.
4. TimingQuest Timing Analyzer
   甲、根據 Timing Constraint 對電路做 Timing 分析

如何做 pin assignment

先用滑鼠左鍵點選”Analysis & Synthesis”二下,讓 Quartus 先執行 Analysis & synthesis.此時 Quartus 即會開始做電路的語法檢查和電路合成的動作,待完成後,視窗會如下圖所示.若看到”Analysis & Synthesis”前有小綠勾產生,即是完成.

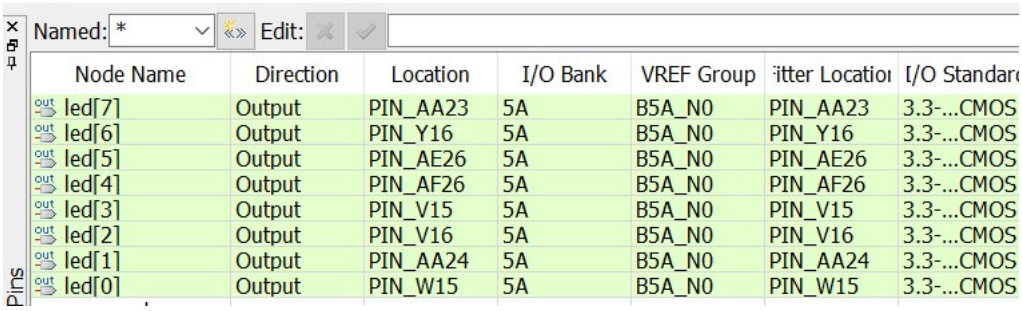


此時再用滑鼠點選”Pin Planner”二下,即會出現如下的視窗,



再根據 data sheet,將相對應的 pin assign 填入,如下圖所示,即完成 pin assignment 的工作.

待輸入完成後,應如下圖所示:



即完成 pin assignment 的工作.

然後關閉 pin assignment 的工作視窗.

rstn pin assignment 則是選用下列二個中的一個。

Table 3-7 Pin Assignment of Push-buttons

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY[0]	PIN_AH17	Push-button[0]	3.3V
KEY[1]	PIN_AH16	Push-button[1]	3.3V

clk pin 的 assignment 則是選用 PIN_V11. 此 clock 的頻率為 50MHz.

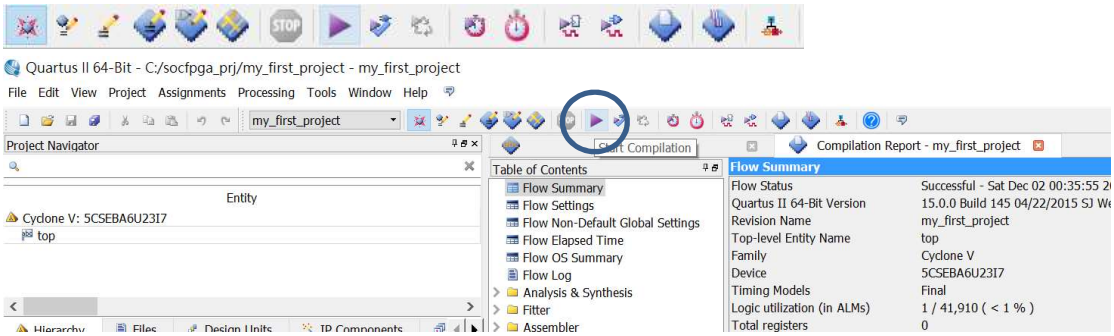
Table 3-5 Pin Assignment of Clock Inputs

Signal Name	FPGA Pin No.	Description	I/O Standard
FPGA_CLK1_50	PIN_V11	50 MHz clock input	3.3V
FPGA_CLK2_50	PIN_Y13	50 MHz clock input	3.3V
FPGA_CLK3_50	PIN_E11	50 MHz clock input (share with FPGA_CLK1_50)	3.3V
HPS_CLK1_25	PIN_E20	25 MHz clock input	3.3V
HPS_CLK2_25	PIN_D20	25 MHz clock input	3.3V

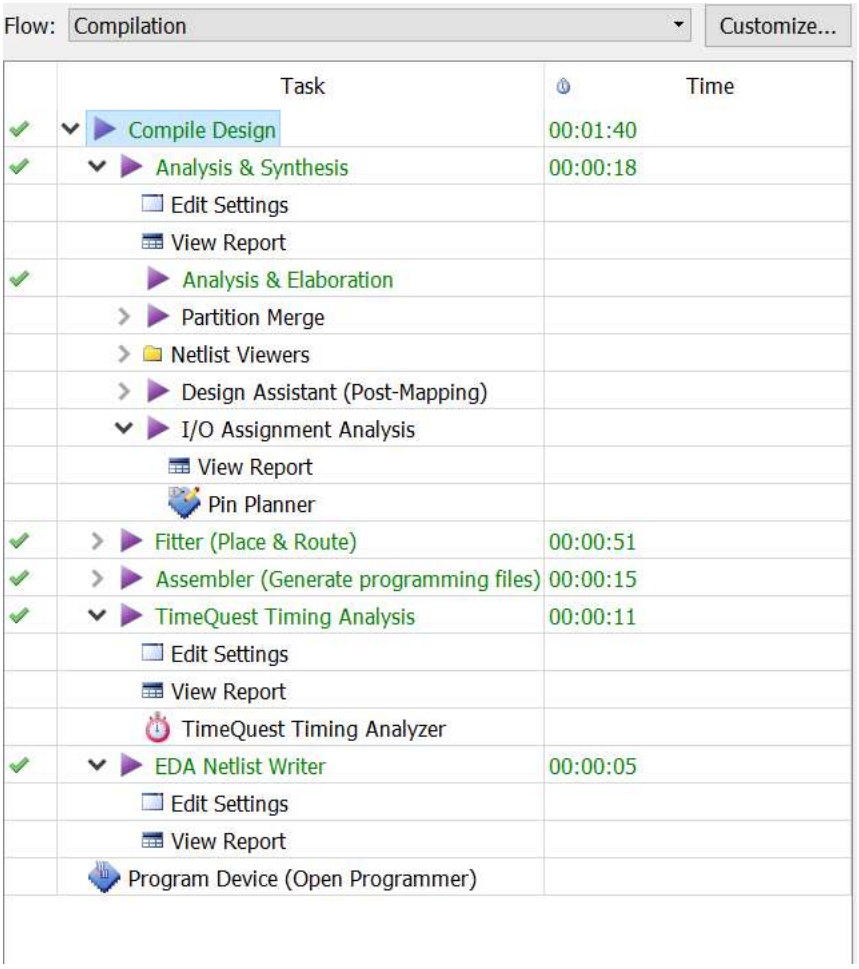
整個 PIN assignment 應會如下圖所示:

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	ırrent Streng	Slew Rate
altera_...ved_tms	Input				2.5 V (default)		12mA ...ault)	
clk	Input	PIN_V11	3B	B3B_N0	3.3-V LVCMOS		2mA (...ault)	
led_o[3]	Output	PIN_AA23	5A	B5A_N0	3.3-V LVCMOS		2mA (...ault)	1 (default)
led_o[2]	Output	PIN_Y16	5A	B5A_N0	3.3-V LVCMOS		2mA (...ault)	1 (default)
led_o[1]	Output	PIN_AE26	5A	B5A_N0	3.3-V LVCMOS		2mA (...ault)	1 (default)
led_o[0]	Output	PIN_AF26	5A	B5A_N0	3.3-V LVCMOS		2mA (...ault)	1 (default)
rstn	Input	PIN_AH16	4A	B4A_N0	3.3-V LVCMOS		2mA (...ault)	
<<new node>>								

點選如下圖中的藍色圖示的 icon  ,Quartus 即開始做電路的 compilation.



待全部做完之後,全部正確無誤的話,將會如下圖所示:



- 如何燒錄 FPGA Code 至 FPGA Board.

請參考 DE10-Nano_User_manual.pdf P.15.節錄如下:

■ Configure the FPGA in JTAG Mode

There are two devices (FPGA and HPS) on the JTAG chain. The following shows how the FPGA is programmed in JTAG mode step by step.

Open the Quartus II programmer, please Choose **Tools** > **Programmer**. The Programmer window opens. Please click "**Hardware Setup**", as circled in Figure 3-3.

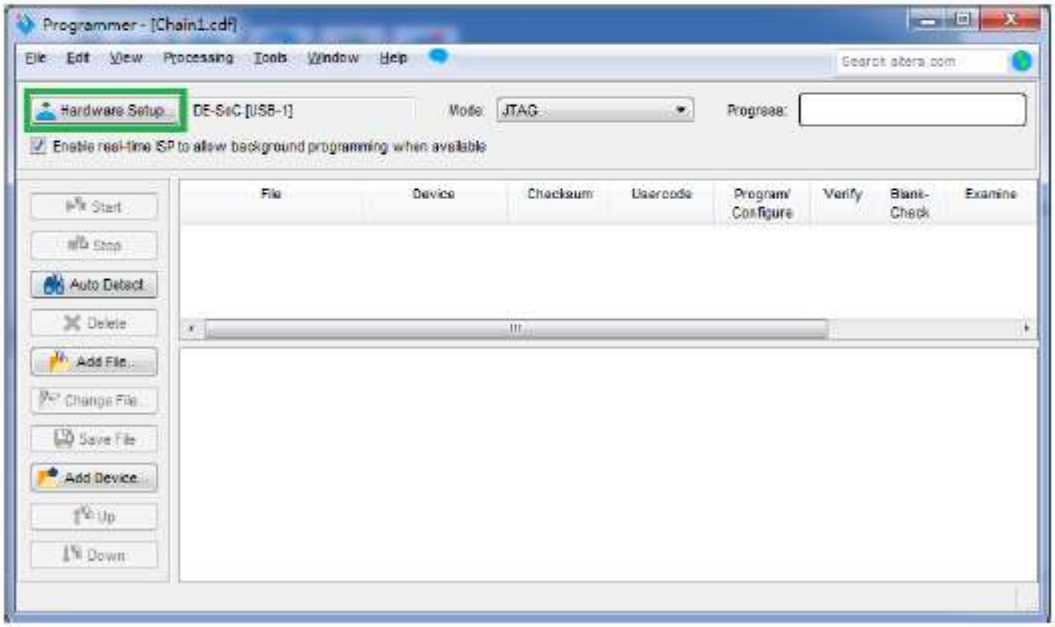


Figure 3-3 Programmer Window

If it is not already turned on, turn on the DE-SoC [USB-1] option under currently selected hardware and click "Close" to close the window. See Figure 3-4.

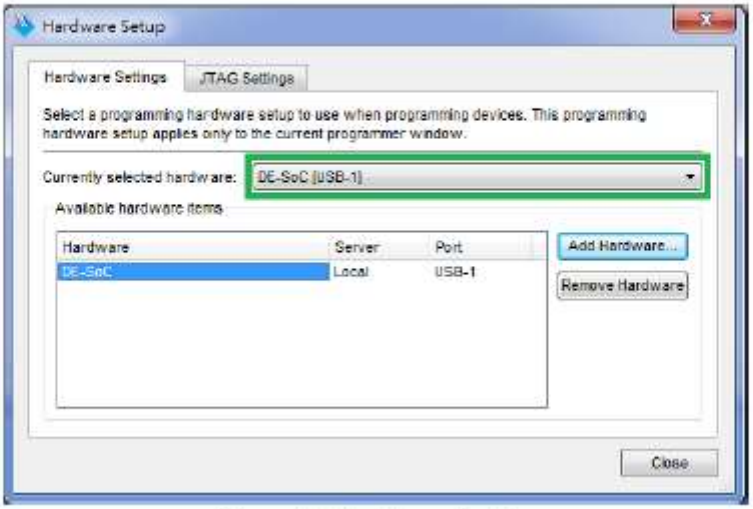


Figure 3-4 Hardware Setting

Return to the Quartus II programmer and click "Auto Detect", as circled in Figure 3-5

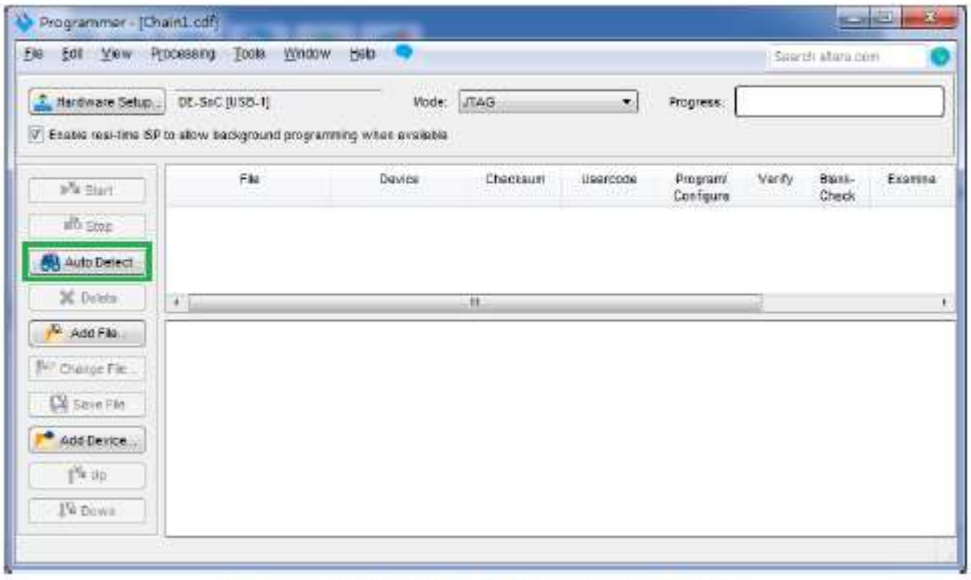


Figure 3-5 Detect FPGA device in JTAG mode

If the device is detected, the window of the selection device is opened, Please select detected device associated with the board and click "OK" to close the window, as circled in Figure 3-6.

Figure 3-6 Select 5CSEBA6 device

Both FPGA and HPS are detected, as shown in Figure 3-7.

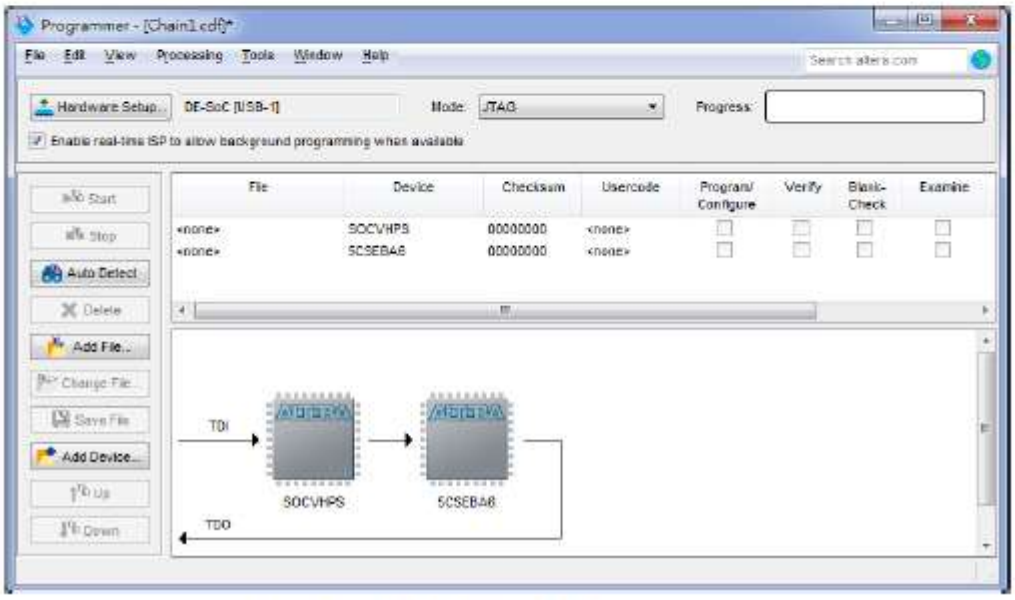


Figure 3-7 FPGA and HPS detected in Quartus programmer

Right click on the FPGA device and open the .sof file to be programmed, as highlighted in Figure 3-8.

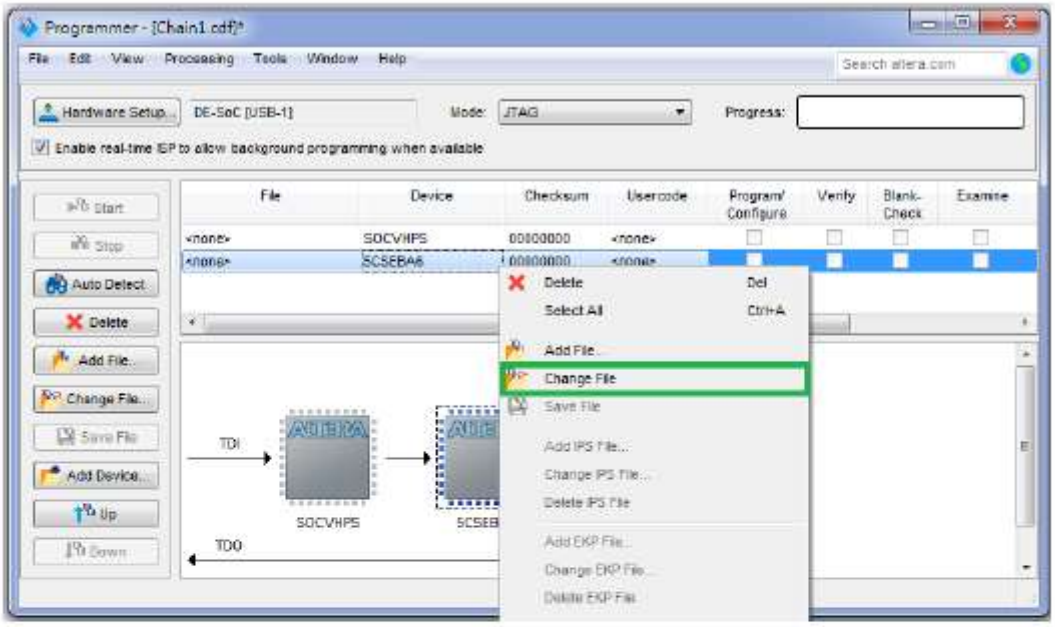


Figure 3-8 Open the .sof file to be programmed into the FPGA device

Select the .sof file to be programmed, as shown in Figure 3-9.

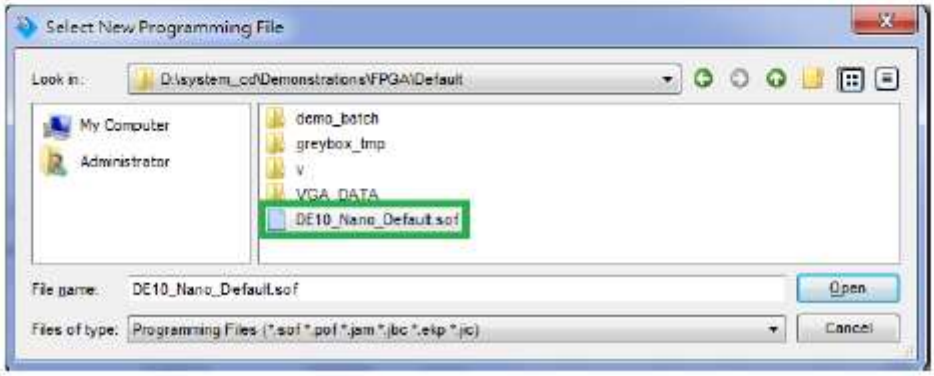


Figure 3-9 Select the .sof file to be programmed into the FPGA device

Click “Program/Configure” check box and then click “Start” button to download the .sof file into the FPGA device, as shown in Figure 3-10.

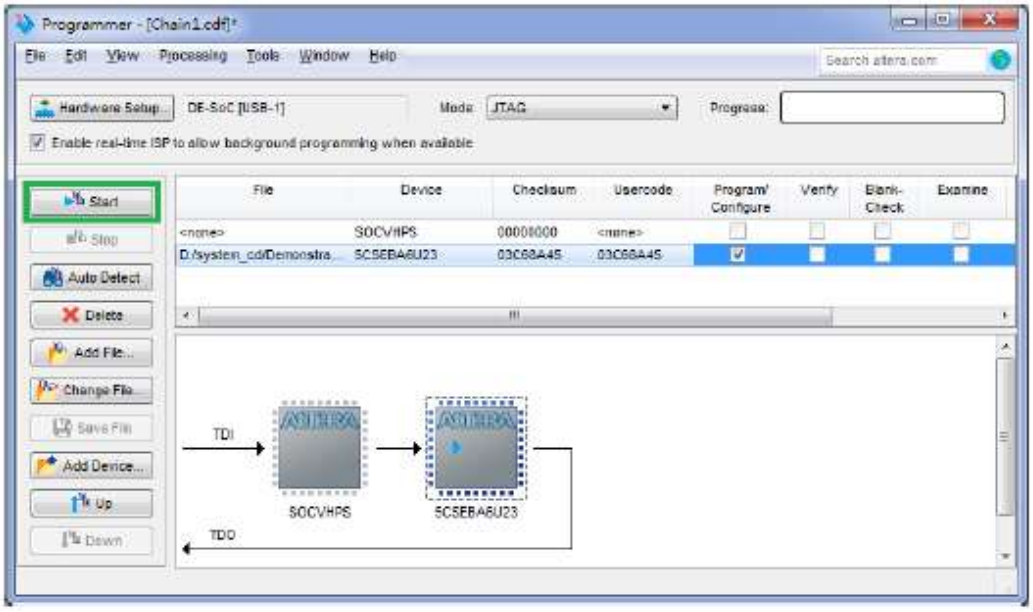


Figure 3-10 Program.sof file into the FPGA device