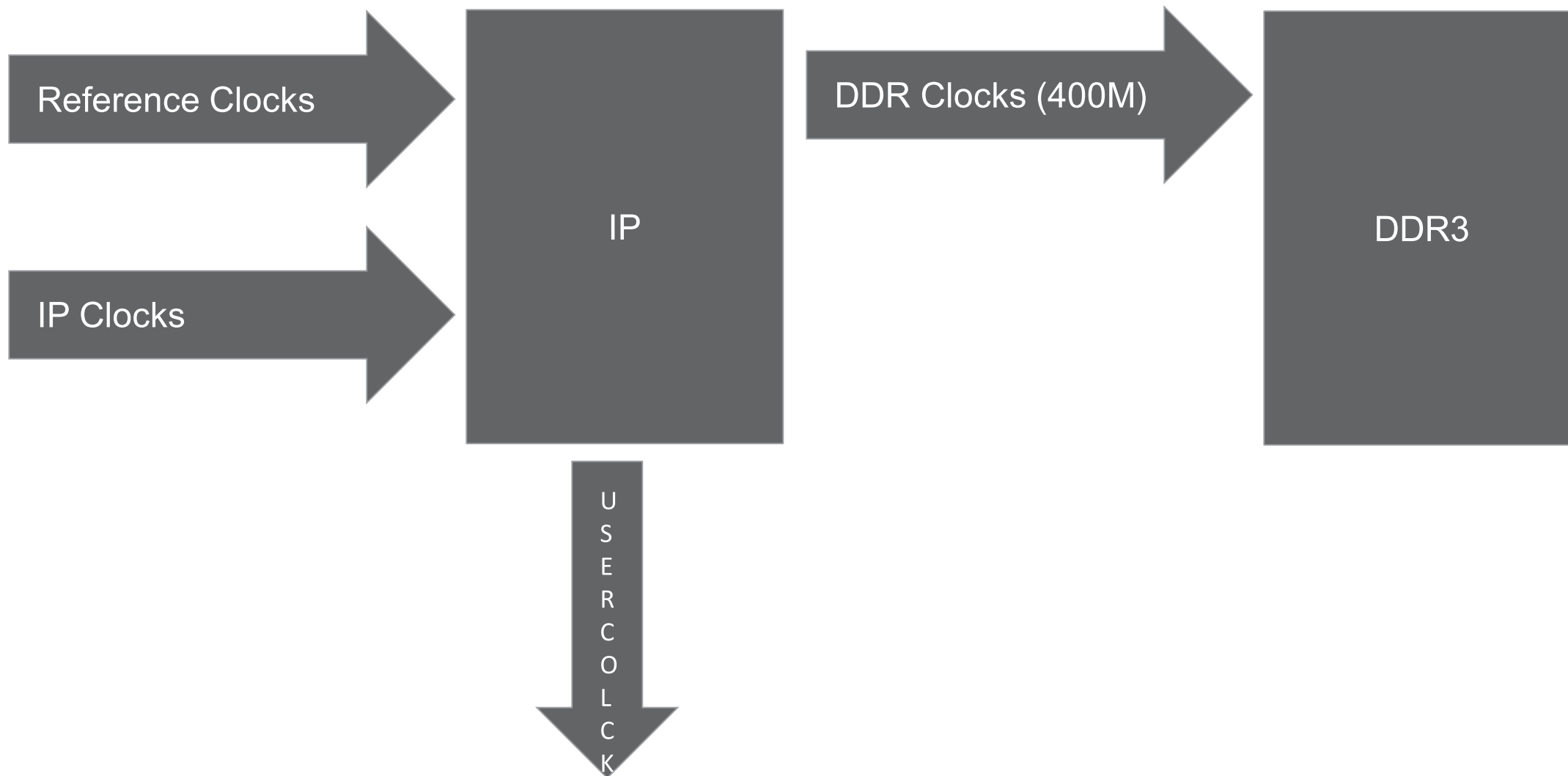




MIG 7 Series IP Overview

Agenda

- Customizing the IP
- Simulating the Example Design
- Simulating Read / Write with AXI VIP
- Connecting the MIG to a Custom Design
- Connecting the MIG to two AXI Master VIP using AXI Smart Connect



Customizing the IP Step 1

Project Summary ? □ ↗

Overview | Dashboard

Settings Edit

Project name: MIG_lab_example_design

Project location: C:/Users/User/Desktop/vince/0.meself/0.Agenda_vince/3.Basic Environment Infrastructure/MIG_lab_example_design/MIG_lab_example_design

Product family: Zynq-7000

Project part: Zynq 7000 ZC702 Evaluation Board (xc7z020clg484-1)

Top module name: Not defined

Target language: Verilog

Simulator language: Mixed

Board Part

Display name: Zynq 7000 ZC702 Evaluation Board

Board part name: xilinx.com:zc702:part0:1.4

Board revision: 1.0

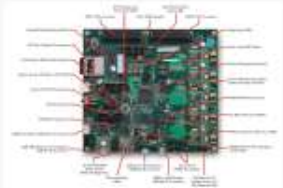
Connectors: No connections

Repository path: C:/Xilinx/Vivado/2022.2/data/xhub/boards

URL: www.xilinx.com/zc702

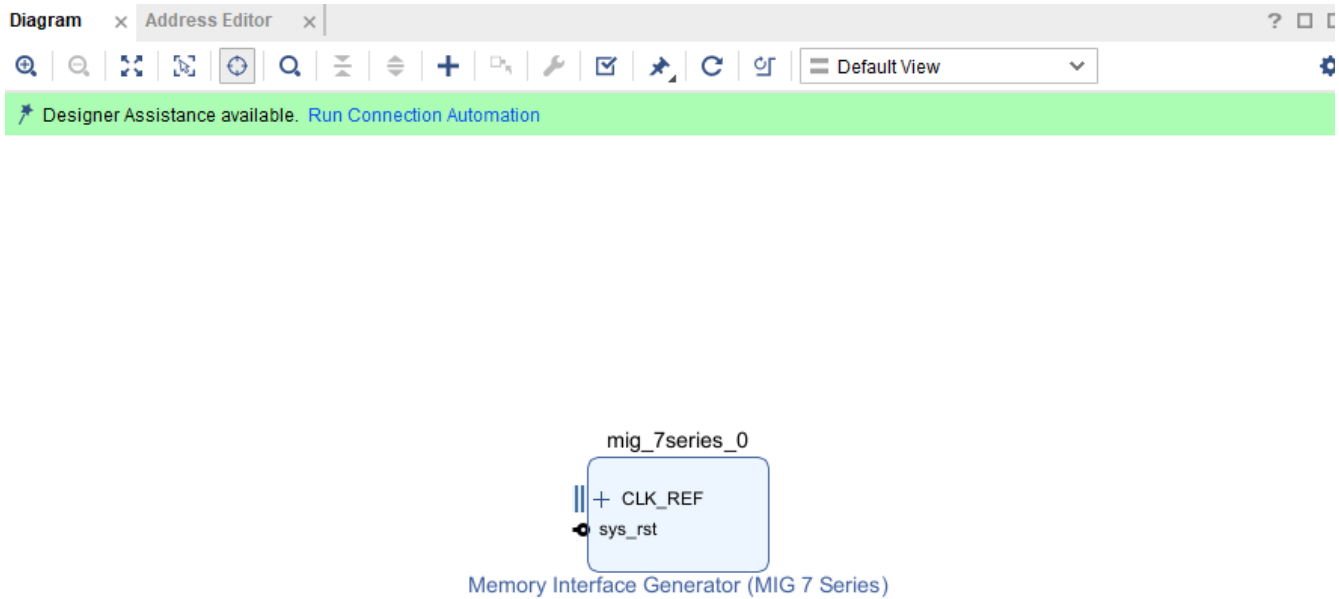
Board overview: Zynq 7000 ZC702 Evaluation Board

[Changes](#)



Customizing the IP

Create a new block diagram (BD) and use the IP catalog to add a new IP to the BD - in this case, the “Memory Interface Generator (MIG 7 Series)” core. If using a board, a prepackaged MIG may be available. We can customize it by double clicking it.



Memory Interface Generator



The screenshot shows the 'MIG Output Options' window in Vivado ML Editions. The 'Create Design' radio button is selected. Below it, the 'Component Name' field is set to 'MIG_lab_mig_7series_0_0'. The 'Multi-Controller' section shows 'Number of controllers' set to 1. The 'AXI4 Interface' section has the 'AXI4 Interface' checkbox checked. At the bottom, there are buttons for 'User Guide', '< Back', 'Next >', and 'Cancel'.

MIG Output Options

☒ **Create Design**
Select this option to generate a memory controller. Generating a memory controller will create RTL, XDC, implementation and simulation files.

☐ **Identify Pin Changes and Update Design**
Selecting this feature verifies the modified XDC for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input XDC file to be compatible with the current version of MIG. While updating the XDC it preserves the pin outs of the input XDC. This option will also generate the new design with the Component Name you selected in this page.

Component Name

Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design", "user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.

Component Name:

Multi-Controller

Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDDR® SDRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information.

Number of controllers:

AXI4 Interface

Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and QDDR SDRAM controllers with Verilog design entry.

☒ AXI4 Interface

[User Guide](#)

Select the “Create Design”

Click “Next”

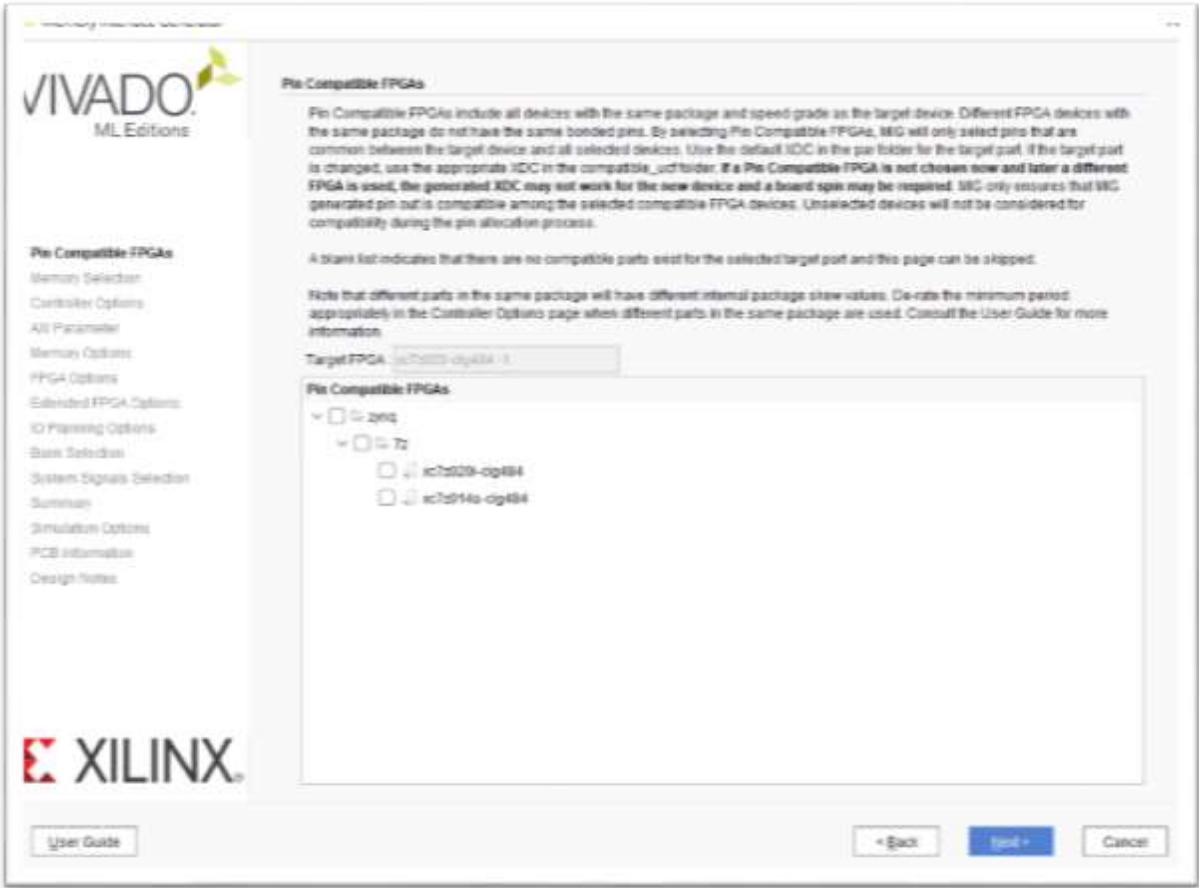
(“Number of Controllers” mean is numbers of controller you need)

“AXI4 Interface” MIG using AXI4 Interface.

- Make sure the AXI4 interface is enabled and select DDR3 SDRAM.

Memory Interface Generator

Pin Compatible FPGAs



Memory selection



Memory Interface Generator - Option for Controller

Memory Interface Generator

VIVADO

ML Editions

Pin Compatible FPGAs

Memory Selection

Controller Options

AXI Parameter

Memory Options

FPGA Options

Extended FPGA Options

IO Planning Options

Bank Selection

System Signals Selection

Summary

Simulation Options

PCB information

Design Notes

Options for Controller 0 - DDR3 SDRAM

Clock Period: Choose the clock period for the desired frequency. The allowed period range(2500 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.

2,500ps400.0 MHz

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.

4:1

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.

Components

Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLD RAM II.

MT41J128M8XX-125

Create Custom Part

Memory Voltage: Select the Voltage of the Memory part selected.

1.5V

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.

8

ECC: MIG supports ECC for 72 bit data width configuration. To be able to select ECC, select a data width that has ECC supported.

Disabled

Data Mask: Enable or disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part selected has DM pins. Uncheck this box to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs (DDR3 SDRAM, DDR2 SDRAM) will not use Data Mask.

☒

Number of Bank Machines: This parameter defines the number of bank machines. A given bank machine manages a single DRAM bank at any given time. Note: Setting a lower value will result in lower resource utilization, but may effect controller efficiency for certain traffic patterns.

4

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.

Normal

Memory Details: 1Gb, x8, row:14, col:10, bank:3, data bits per strobe:8, with data mask, single rank, 1.5V

XILINX

8

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AMD
together we advance_

Memory Interface Generator - Option for Controller

Clock Period: Choose the clock period for the desired frequency. The allowed period range(2500 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.

2,500

ps

400.0 MHz

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.

4:1

1

2

1.
- The desired clock period must be between 2500 and 3300ps. For now, use 2500ps (400 MHz), as this is the speed of the actual physical DDR3 RAM transactions.
2.
- Make sure the PHY to Controller Clock Ratio is **4:1 (ensuring that the physical DDR RAM will operate at 400 MHz, but the controller stays at 100 MHz i.e., ui_clk = 100 MHz).**
- The ui_clk using by User want to reading the MIG controller address.

Memory Interface Generator - Option for Controller

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.	Components	1
Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLD RAM II.	MT41J128M8XX-125 Create Custom Part	2
Memory Voltage: Select the Voltage of the Memory part selected.	1.5V	3
Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.	8	4

- Memory Type – This feature selects the type of memory parts used in the design.
- Memory Part – This option selects a memory part for the design. Selections can be made from the list or a new part can be created. Note: For a complete list of memory parts available, see Answer Record: 54025.
- Data Width – The data width value can be selected here based on the memory type selected earlier. The list shows all supported data widths for the selected part. One of the data widths can be selected. These values are generally multiples of the individual device data widths. In some cases, the width might not be an exact multiple. For example, 16 bits is the default data width for x16 components, but eight bits is also a valid value.
- Data Mask – This option allocates data mask pins when selected. This should be deselected to deallocate data mask pins and increase pin efficiency. Also, this is disabled for memory parts that do not support data mask.

Memory Interface Generator - Option for Controller

Create Custom Part

Create custom part

This option create a new memory part. Note that the new memory part will be modification of the 'Base Part' selected below. The timing parameters and density can be changed

Select base part: MT41J128M8XX-125

Enter new memory part name:

Change the required Timing Parameters. "Value" is the only field that can be edited.

Parameter	Value	Range	Unit	Description
tcke	5	5-20	ns	CKE minimum pulse width
tfaw	30	25-55	ns	Four Address Width
tras	35	33-37.5	ns	Active to Precharge command
trcd	13.75	10-15	ns	Active to Read or write delay
trfll	7.8	3.9-7.8	us	Average periodic refresh interval
trfc	110	90-350	ns	Refresh to Active or Refresh to Refresh
trp	13.75	10-15	ns	Precharge command period
trrd	8	5-20	ns	Activate minimum command period
trtp	7.5	7.5-20	ns	Read following a Write to the same de
twtr	7.5	7.5-20	ns	Read following a Write to the same de

Row address: 14

Column address: 10

Bank address: 3

SaveDeleteClose

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.

Components

Memory Part: Select the memory part. Part(s) marked with a warning symbol are not compatible with the frequency selection above. Find an equivalent part or create a part using the "Create Custom Part" button if the part needed is not listed here. The "Create Custom Part" feature is not supported for RLD RAM II.

MT41J128M8XX-125

Create Custom Part

1. On the Controller Options page select the appropriate frequency. Either use the spin box or enter a valid value using the keyboard. Values entered are restricted based on the minimum and maximum frequencies supported.
2. Select the appropriate memory part from the list. If the required part or its equivalent is unavailable, a new memory part can be created. To create a custom part, click the Create Custom Part below the Memory Part pull-down menu. A new page appears, as shown in Figure.
3. Select the suitable base part from the Select Base Part list.
4. Enter the appropriate memory part name in the text box.
5. Edit the value column as needed.
6. Select the suitable values from the Row, Column, and Bank options as per the requirements.
7. After editing the required fields, click Save. The new part is saved with the selected name. This new part is added in the Memory Parts list on the Controller Options page. It is also saved into the database for reuse and to produce the design.
8. Click Next to display the Memory Options page (or the AXI Parameter Options page if AXI Enable is checked on the Memory Type selection page).

Memory Interface Generator - Option for Controller

Number of Bank Machines: This parameter defines the number of bank machines. A given bank machine manages a single DRAM bank at any given time.
Note: Setting a lower value will result in lower resource utilization, but may effect controller efficiency for certain traffic patterns.

4

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.

Normal

Memory Details: 1Gb, x8, row:14, col:10, bank:3, data bits per strobe:8, with data mask, single rank, 1.5V

- Number of Bank Machines – The list shows the number of bank machines that are supported for the selected design configuration.
- Ordering – This feature allows the Memory Controller to reorder commands to improve the memory bus efficiency.
- Memory Details – The bottom of the Controller Options Figure displays the details for the selected memory configuration Figure.

Memory Interface Generator – AXI Parameter

Memory Interface Generator



- Pin Compatible FPGAs
- Memory Selection
- Controller Options
- AXI Parameter**
- Memory Options
- FPGA Options
- Extended FPGA Options
- IO Planning Options
- Bank Selection
- System Signals Selection
- Summary
- Simulation Options
- PCB information

Axi Parameter Options C0 - DDR3 SDRAM

Data Width

AXI DATA WIDTH: Data width of AXI read & write channels. The data width is less than or equal to user interface data width with the possible values 32, 64, 128, 256 & 512.

128

Arbitration Scheme

Select the arbitration scheme between the read and write address channels

RD_PRI_REG

Narrow Burst Support

Enables logic to support narrow bursts on the AXI4 slave interface. Can be set to zero if no masters in the system issue narrow bursts and all the data widths are equal. (1-Enable, 0-Disable)

0

Address Width

AXI4 address width of read and write address channels.

28

ID Width

AXI4 ID width for read and write channels. AXI4 ID is used as the identification tag for write or read address group of signals

4

MIG Pin Definition

1,DDR3 level standard

DDR3 level standard is SSTL15, 1.5V+- 0.075V

2,DDR3 electrical interface parameters

Pin definition : inout [31:0] ddr3_dq;

Pin description : Data input and output, bidirectional data.

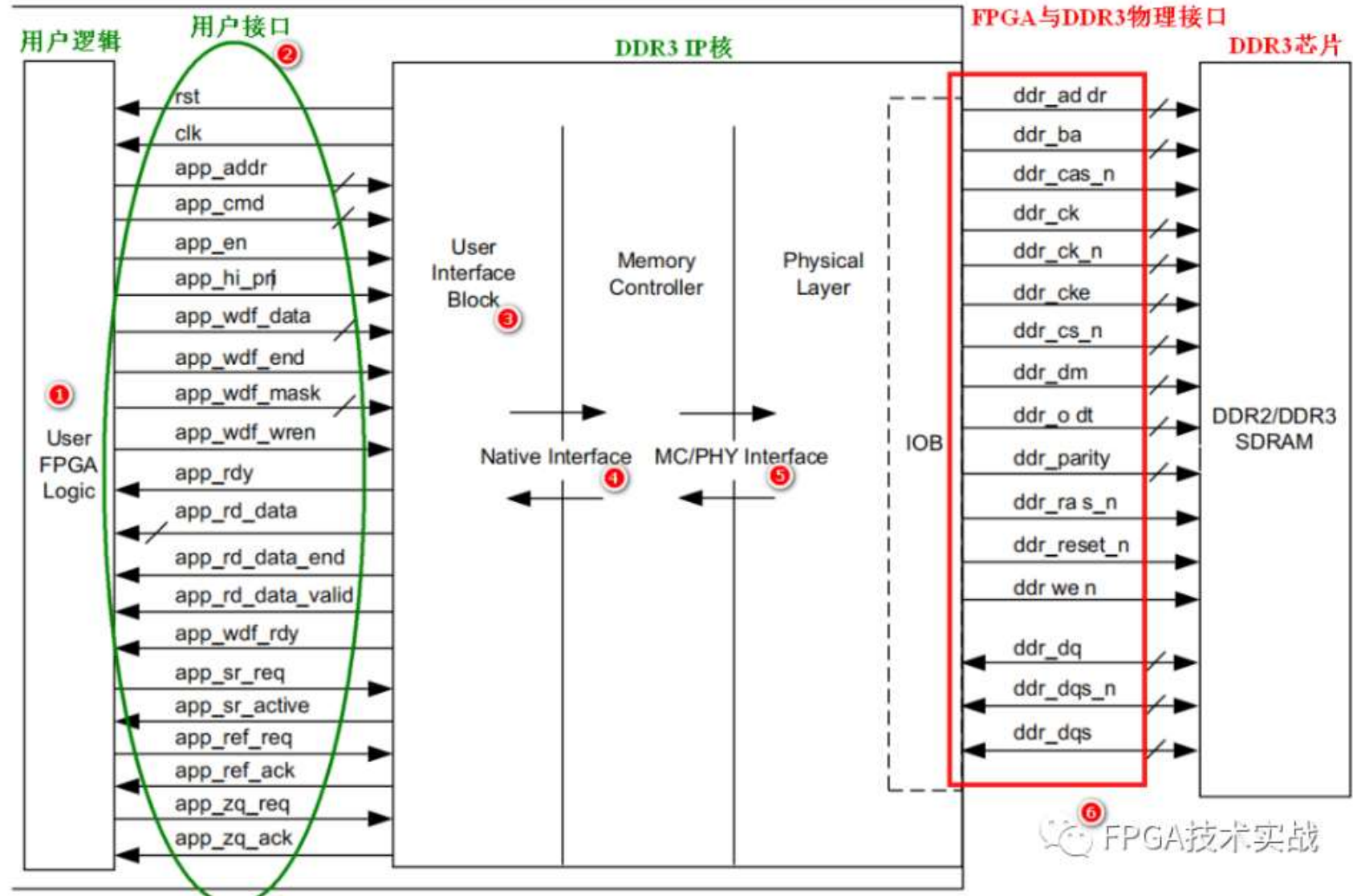
3, ddr3_dps_p & ddr3_dps_n

Pin definition : inout [3:0] ddr3_dps_n/p

Pin description : Data strobe when data is read, is the output for DDR3, and the edges are aligned with the data being read. When writing data, for DDR3 it is the input and the center is aligned with the write data.

4,

Solution Design



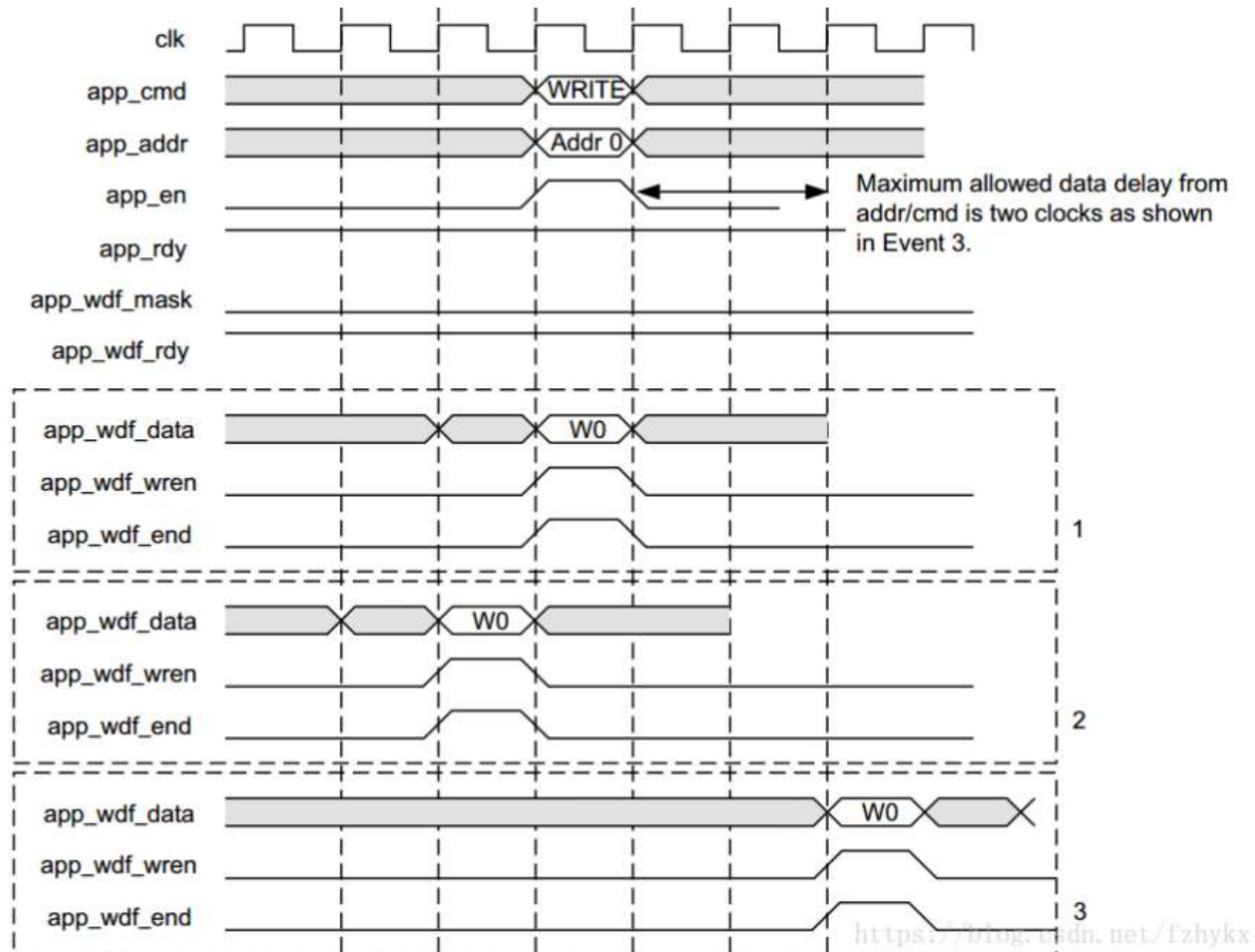
Pin	Direction	Note
ddr3_addr	Output	
ddr3_ba	Output	
ddr3_cas_n	Output	
ddr3_ck_n	Output	
ddr3_ck_p	Output	
ddr3_cke	Output	
ddr3_ras_n	Output	
ddr3_reset_n	Output	復位狀態信號
ddr3_we_n	Output	
ddr3_dq	inout	
ddr3_dps_n	inout	
ddr3_dps_p	inout	
Init_calib_complete	Output	初始化完成信號
ddr3_cs_n	Output	
ddr3_dm	Output	
ddr3_odt	Output	

sys_clk_i	input	The clk for board
clk_ref_i	input	The clk for board
sys_rst	Input	The clk for reset of board

Pin	Direction	Note
app_addr	input	要操作地址每次step 為8
app_cmd	input	寫000 讀001
app_en	input	Enable single
app_wdf_data	input	Write data [255:0]
app_wdf_end	input	Last data single
app_wdf_wren	input	Write enable single
app_rd_data	output	Read data [255:0]
app_rd_data_end	output	Last data single()
app_rd_data_valid	output	Read enable
app_rdy	output	
app_wdf_rdy	output	
app_sr_req	Input	Set 0
app_ref_req	Input	Set 0
app_zq_req	Input	Set 0
app_sr_active	Output	
app_ref_ack	Output	
app_zq_ack	Output	
ui_clk	Output	Users clk
ui_clk_sync_rst	Output	Users reset
app_wdf_mask	input	Keep single

Time analyze

- Write the timing (wr_en high) , we can perform operations when the **app_rdy** and **app_wdf_ready** all are **high**, The command pull **app_en high** and **write the data and address at the same time.**(DDR allows the WR_EN signal to lag within two CMD and two CLOCK, but it is still recommended to write within the same cycle.)



Read timing

- read the timing (rd_en high) , we can perform operations when the **app_en** and **app_addr** all are **high**,than waiting valid single (valid data), **How many commands were issued (CLK) and how many commands were responded to (CLK).**

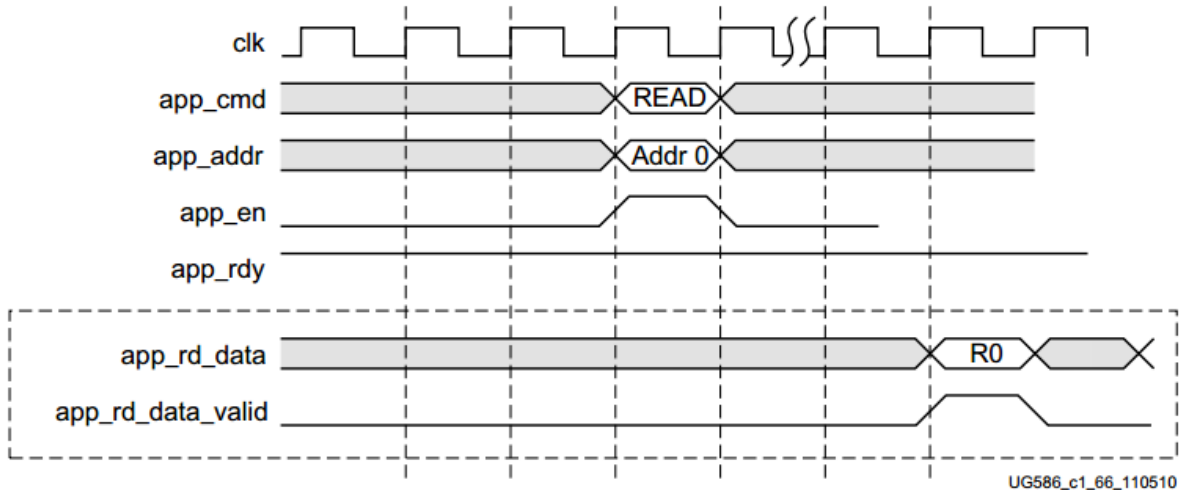


Figure 1-81: 4:1 Mode UI Interface Read Timing Diagram (Memory Burst Type = BL8)

