Button Debounce 電路設計

下圖為 Button Debounce 電路的 Waveform 圖

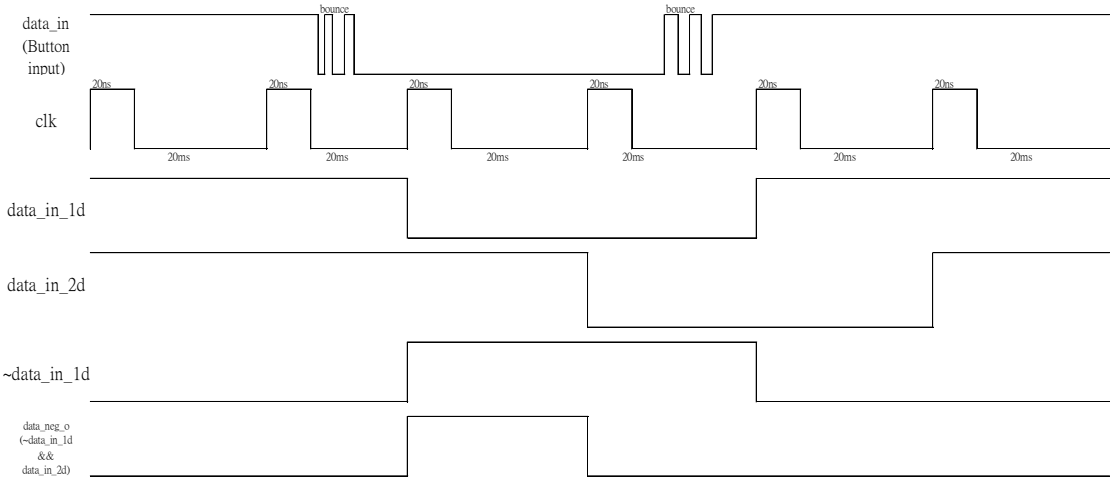

Fig. Button Debounce Waveform

其電路原理為利用 50MHz(20ns)的 system clock 產生間隔為 20ms 的 pulse 訊號，並以此訊號來 capture 按鈕的訊號，並避開按鈕 bounce 的時間，再利用 Edge detector 的電路設計方式產生一個 Pulse 訊號(data_neg_o)。所以每當按鈕(button)被按下時，即會產生一個 pulse 訊號。

完整的 Verilog Code 如下所示:

```
module debounce (
  clk,           // 50MHz
  reset_n,
  data_in,
  data_neg_o,
  data_out
);
input     clk,reset_n;
input     data_in;
output    data_out;
output    data_neg_o;
parameter time_20ms = 32'd49999 * 20;    // 20ms
reg [31:0]  cnt;         // counter to generate 20ms
reg         data_in_1d,data_in_2d;
wire        time_20ms_cap;

// 20ms counter
always@(posedge clk or negedge reset_n)
begin
    if(~reset_n)
            cnt <= 32'h0;
    // generate one clock pulse based on 50MHz every 20ms.
    else if(cnt == time_20ms)
            cnt <= 'h0;
    else
            cnt <= cnt + 1'b1;
end
// generate one pulse every 20ms
assign time_20ms_cap = (cnt == time_20ms) ? 1'b1 : 1'b0;


always@(posedge clk or negedge reset_n)
begin
    if(~reset_n) begin
        data_in_1d <= 1'b0;
        data_in_2d <= 1'b0;
    end
    else if(time_20ms_cap) begin
        data_in_1d <= data_in;
        data_in_2d <= data_in_1d;
    end
    else begin
        data_in_1d <= data_in_1d;
        data_in_2d <= data_in_2d;
    end
end

// negedge detector base on 20ms clock
assign data_neg_o = ~data_in_1d && data_in_2d;
assign data_out = data_in_2d;

endmodule
```