Efficient Implementation of a High-Performance In-production Weather Model on FPGA

Task description of the Bachelor thesis, ETH Zurich, supervised by Johannes de Fine Licht, Professor Torsten Hoefler

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Introduction

Accurate and reliable weather forecast is of vital importance for a broad field of industries, as well as the general public. Highly regular and statically analyzable stencil operators [1] on structured grids are used to numerically solve the partial differential equations of such weather prediction models. This allows optimizations for data re-use while minimizing the high demand of memory bandwidth [2, 3] on the FPGA (field-programmable gate array) platform. Our collaboration with MeteoSwiss [4] enables us to apply our theoretical optimization findings to the numerical weather prediction and regional climate model COSMO [5, 6]. By cooperating closely with the University of Paderborn [7], we gain access to a clustered heterogeneous supercomputer containing 32 interconnected Stratix 10 FPGAs [8] whereby we intend to figure out if FPGAs [9] are the optimal choice for future high-performance weather prediction simulations.

Research questions to answer (Q) / Development tasks to perform (D)

1. Manual analysis and formalization of the problem. (Q)
2. Defining a suitable input representation. (Q)
3. Automatic analysis of the input including computation of important characteristics such as latency, buffer requirements, etc. (D)
4. Feasibility estimate. (Q)
5. Formulation of optimization goals and constraints. (Q)

6. Automatic optimization of the input according to the goals/constraints using a suitable solver. (D)

7. Formalization of a FPGA simulation model and implementation of the software simulation for testing, debugging and performance metric measures. (Q,D)

8. Manual implementation of the stencil chains on (single/multiple) FPGAs including performance optimizations in HLS [10]. (Q,D)

9. Automatic code generation. (D)

10. [Optional] Porting and testing of the complete dynamical core of COSMO to the FPGA platform. (D)

References

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