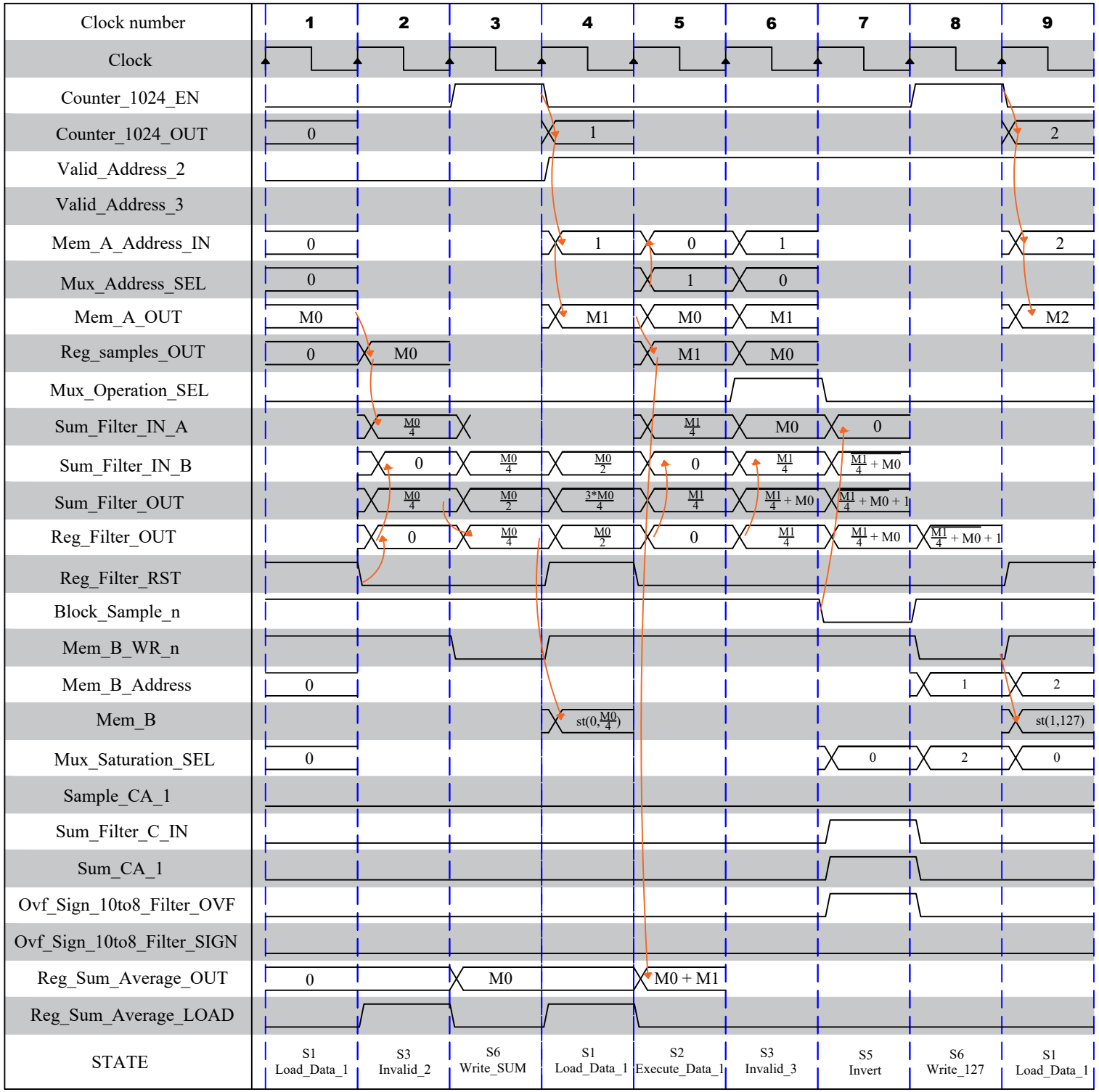
Clock number
1
2
3
4
5
6
7
8
9
Clock
Counter_1024_EN
Counter_1024_OUT
0
1
2
Valid_Address_2
Valid_Address_3
Mem_A_Address_IN
0
1
0
1
2
Mux_Address_SEL
0
1
0
Mem_A_OUT
M0
M1
M0
M1
M2
Reg_samples_OUT
0
M0
M1
M0
Mux_Operation_SEL
Sum_Filter_IN_A
M0/4
M1/4
M0
0
Sum_Filter_IN_B
0
M0/4
M0/2
0
M1/4
M1/4 + M0
Sum_Filter_OUT
M0/4
M0/2
3*M0/4
M1/4
M1/4 + M0
M1/4 + M0 + 1
Reg_Filter_OUT
0
M0/4
M0/2
0
M1/4
M1/4 + M0
M1/4 + M0 + 1
Reg_Filter_RST
Block_Sample_n
Mem_B_WR_n
Mem_B_Address
0
1
2
Mem_B
st(0,M0/4)
st(1,127)
Mux_Saturation_SEL
0
0
2
0
Sample_CA_1
Sum_Filter_C_IN
Sum_CA_1
Ovf_Sign_10to8_Filter_OVF
Ovf_Sign_10to8_Filter_SIGN
Reg_Sum_Average_OUT
0
M0
M0 + M1
Reg_Sum_Average_LOAD
STATE
S1 Load_Data_1
S3 Invalid_2
S6 Write_SUM
S1 Load_Data_1
S2 Execute_Data_1
S3 Invalid_3
S5 Invert
S6 Write_127
S1 Load_Data_1