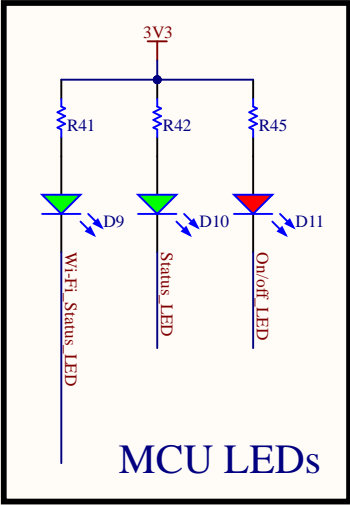
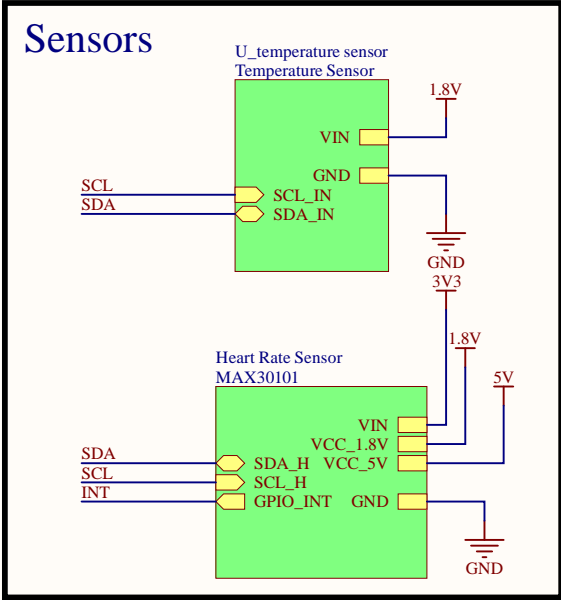
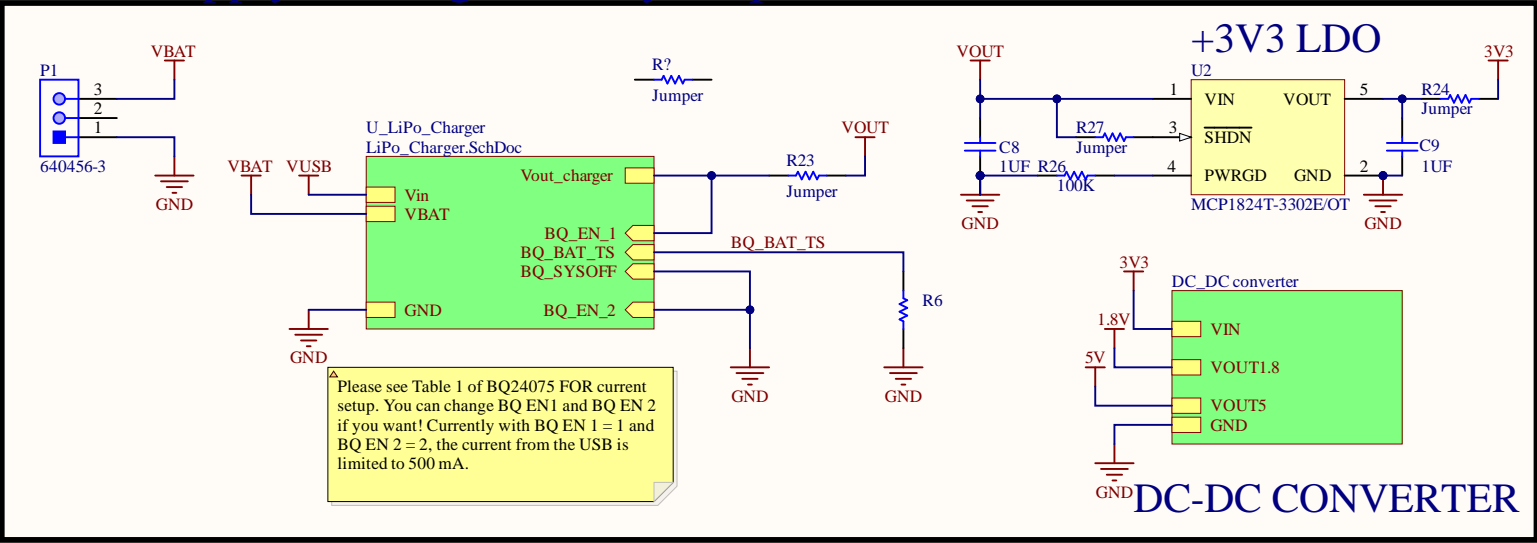
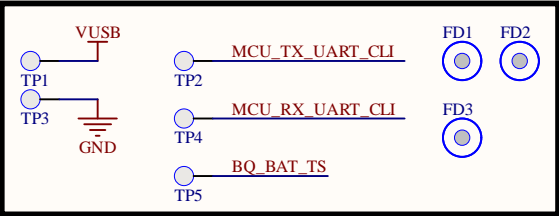


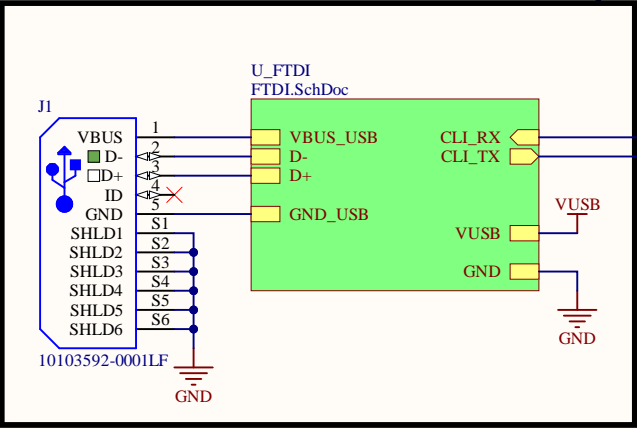
Power Supply - Change me to your power architecture



Test Points + Fiducials

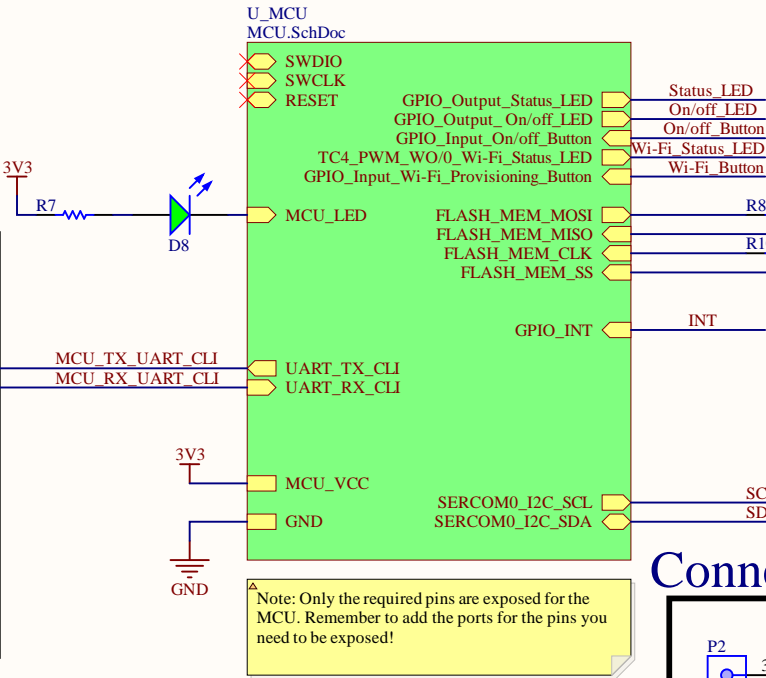


USB Connector + FTDI Chip

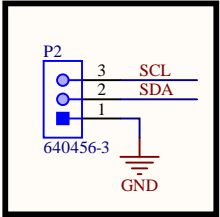


NOTE:
The FTDI Chip is an useful chip that allows us to convert USART cmessages into USB signals. It allows us to connect the MCU directly to the USB port of a computer and use the serial terminal (it is the same bridge used on the SAMW25 Xplained Board).The FTDI device also contains protection circuitry for the USB.

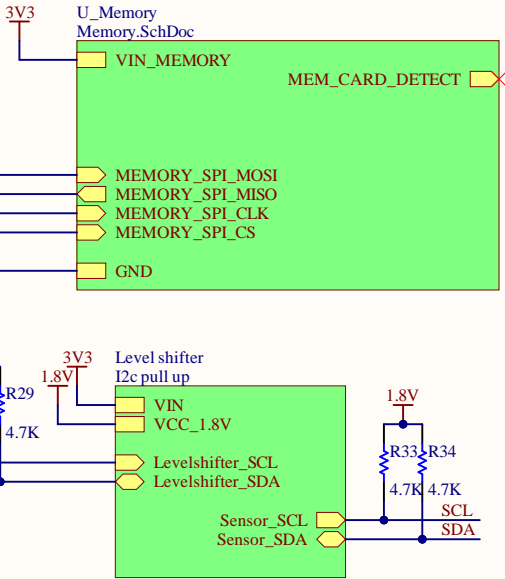
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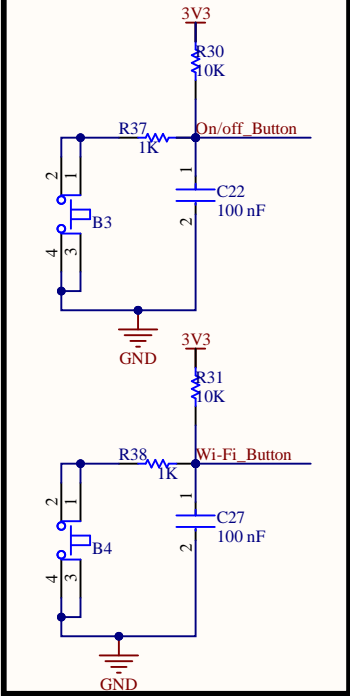
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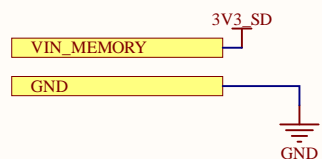
SD Card Memory



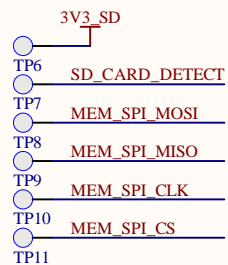
MCU Test Buttons



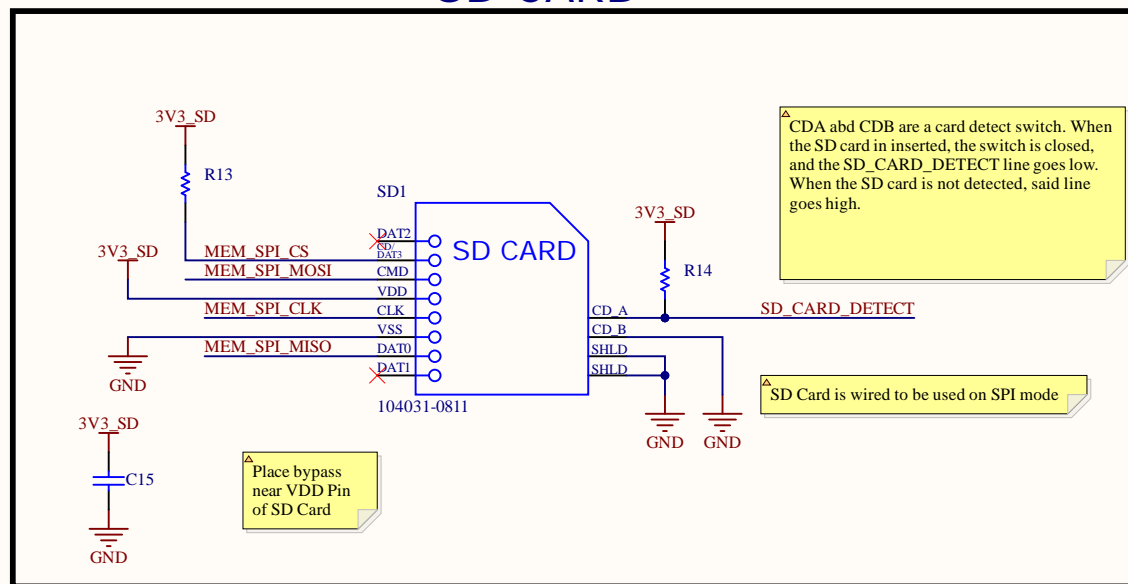
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MEMORY_SPI_CLK	MEM_SPI_CLK
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MEM_CARD_DETECT	SD_CARD_DETECT



TESTPOINTS



SD CARD



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Size: Letter

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AD Ver. 23.1.1.15

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Sheet

2

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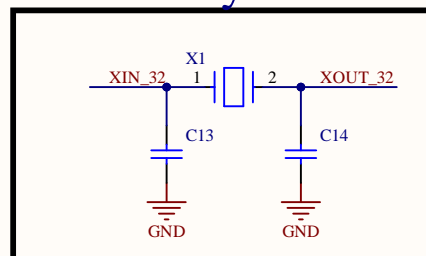
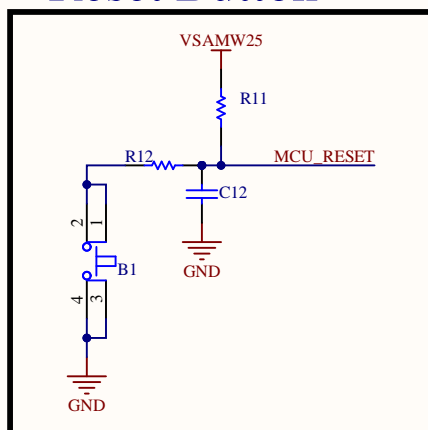
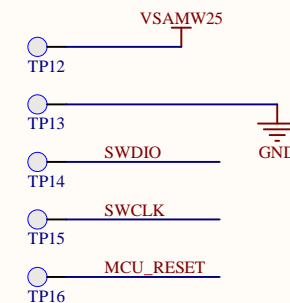
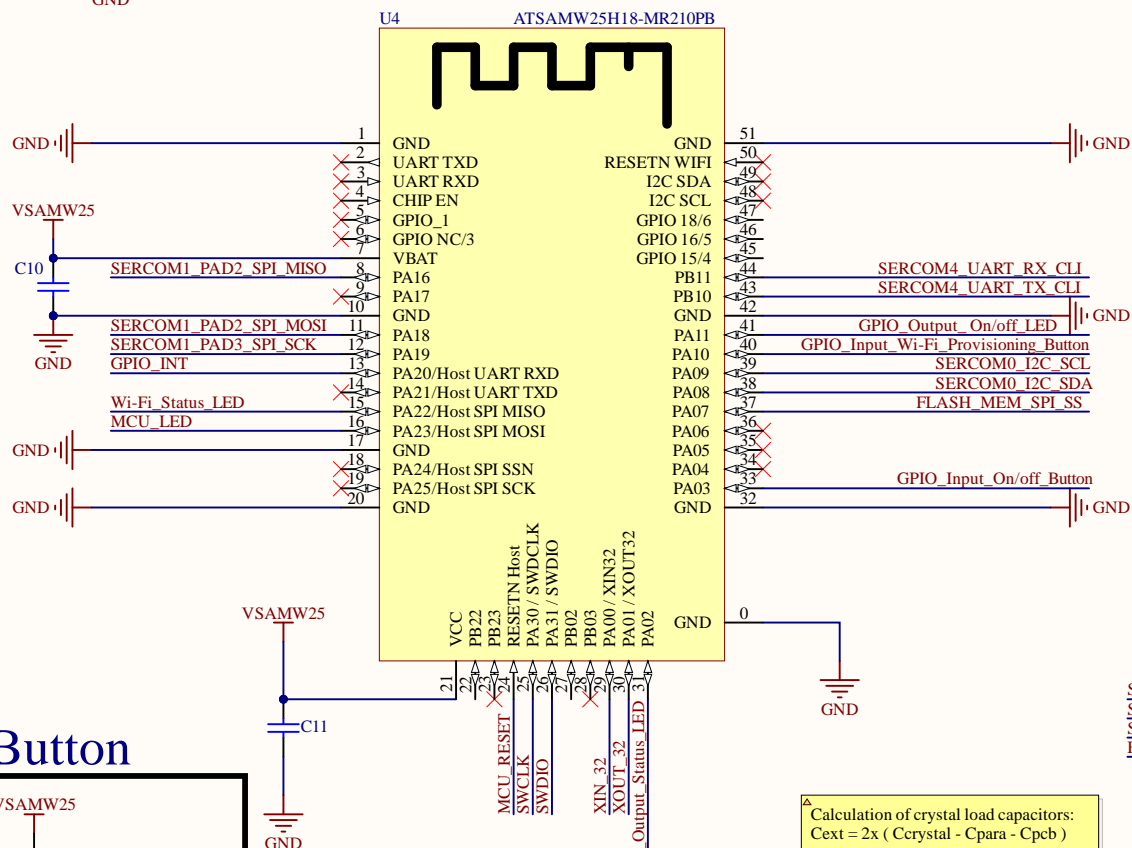
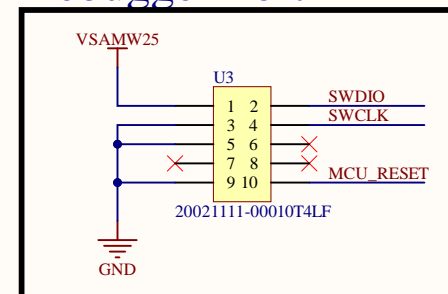
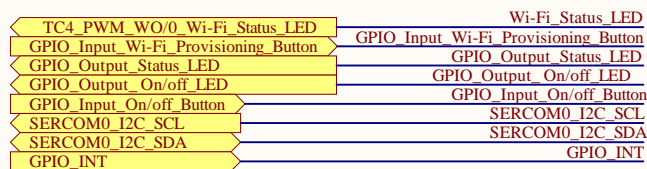
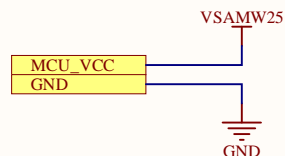
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Electrical and Systems Engineering

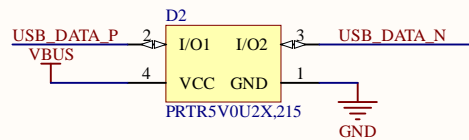
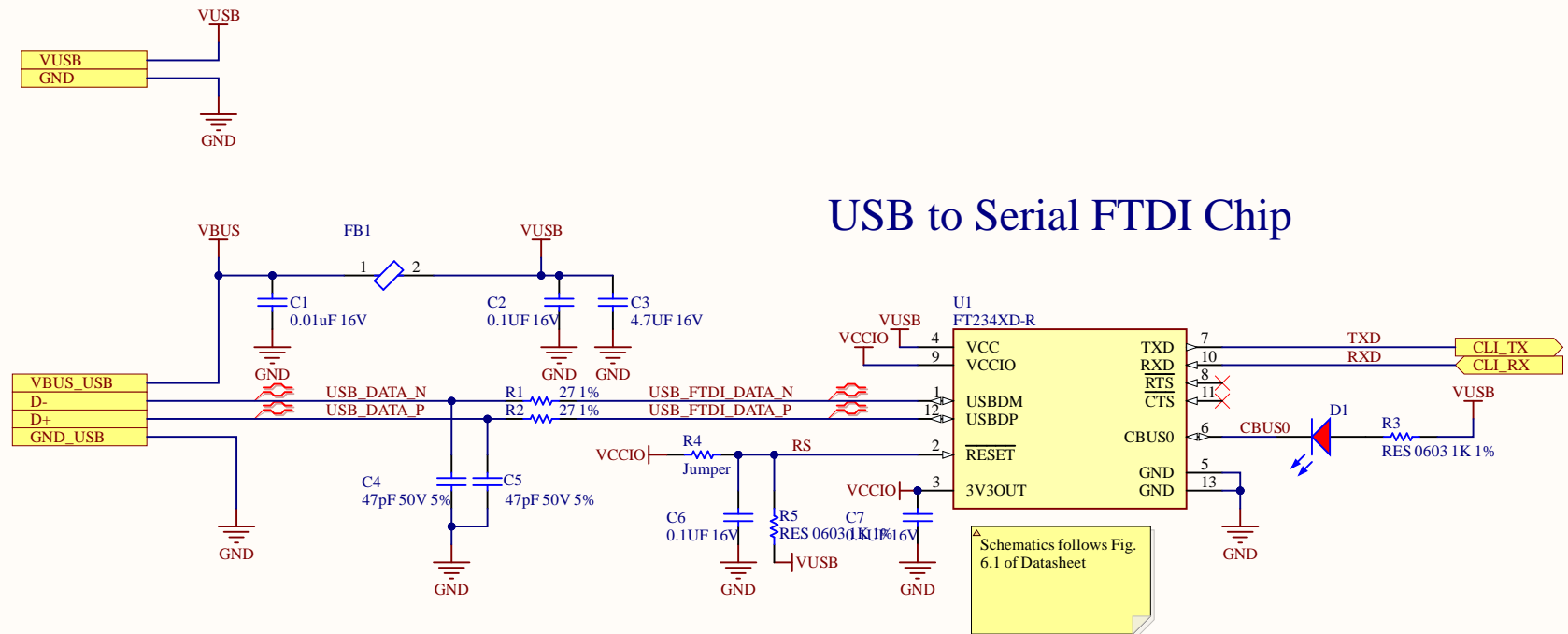



Calculation of crystal load capacitors:
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$

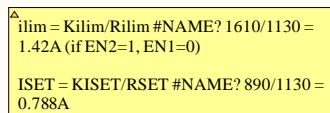
Ccrystal = 12.5pF (from crystal datasheet)
Cpara = 3.15pF (from MCU datasheet)
Cpcb = 0.5pF (estimate)
Cext = 2x(12.5pF - 3.15pF - 0.5pF) = 17.7pF

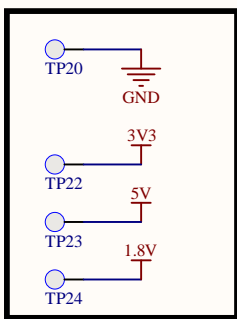
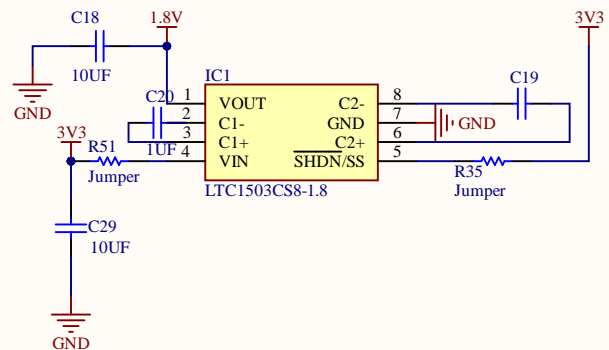
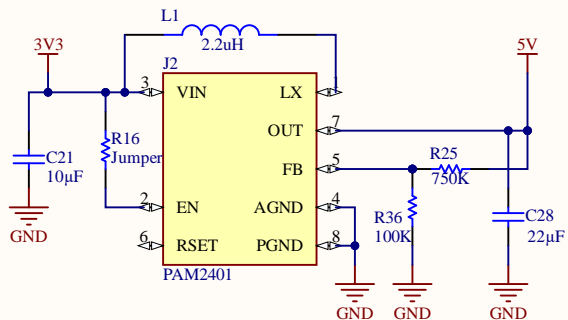
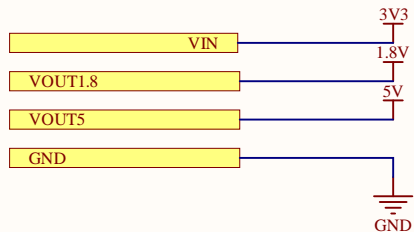
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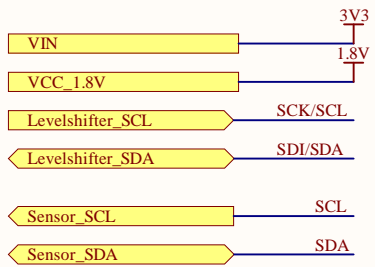




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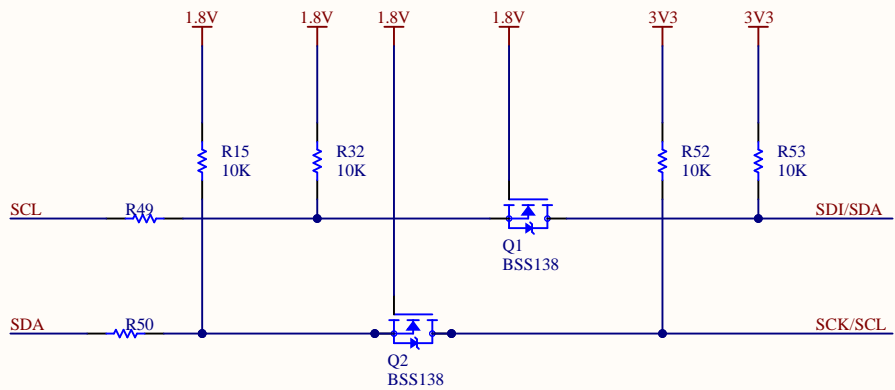
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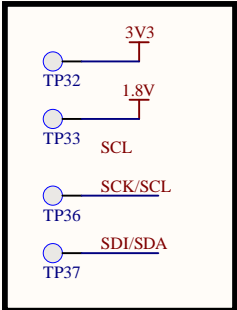
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C

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I2C Pullups & Shift

D

D

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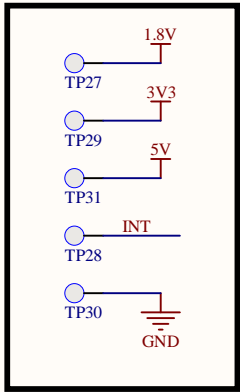
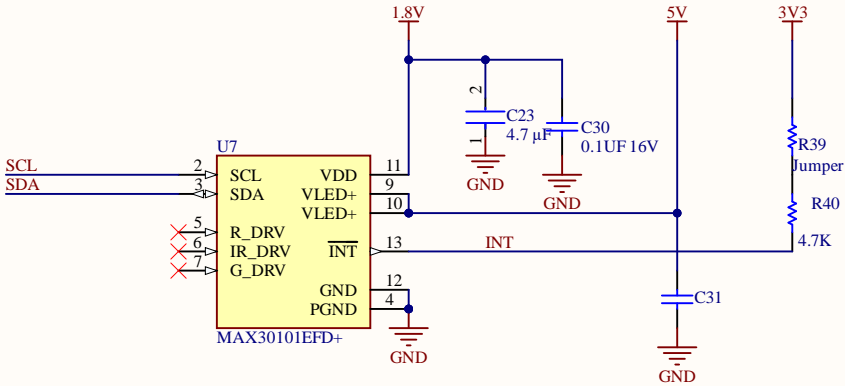
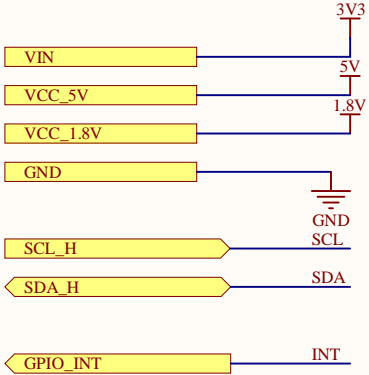
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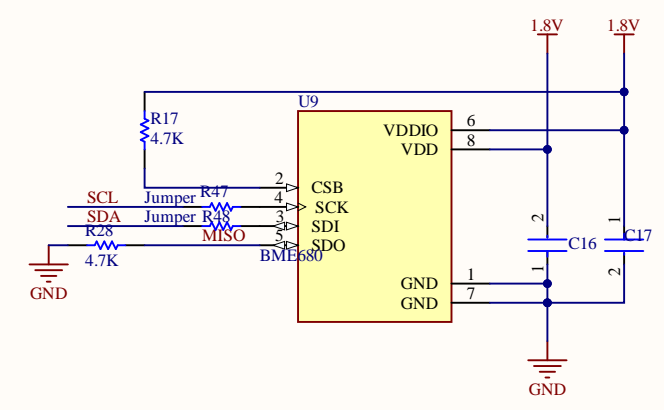
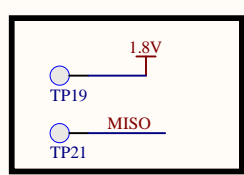
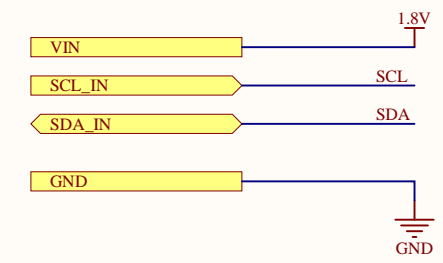
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Manufacturing Notes

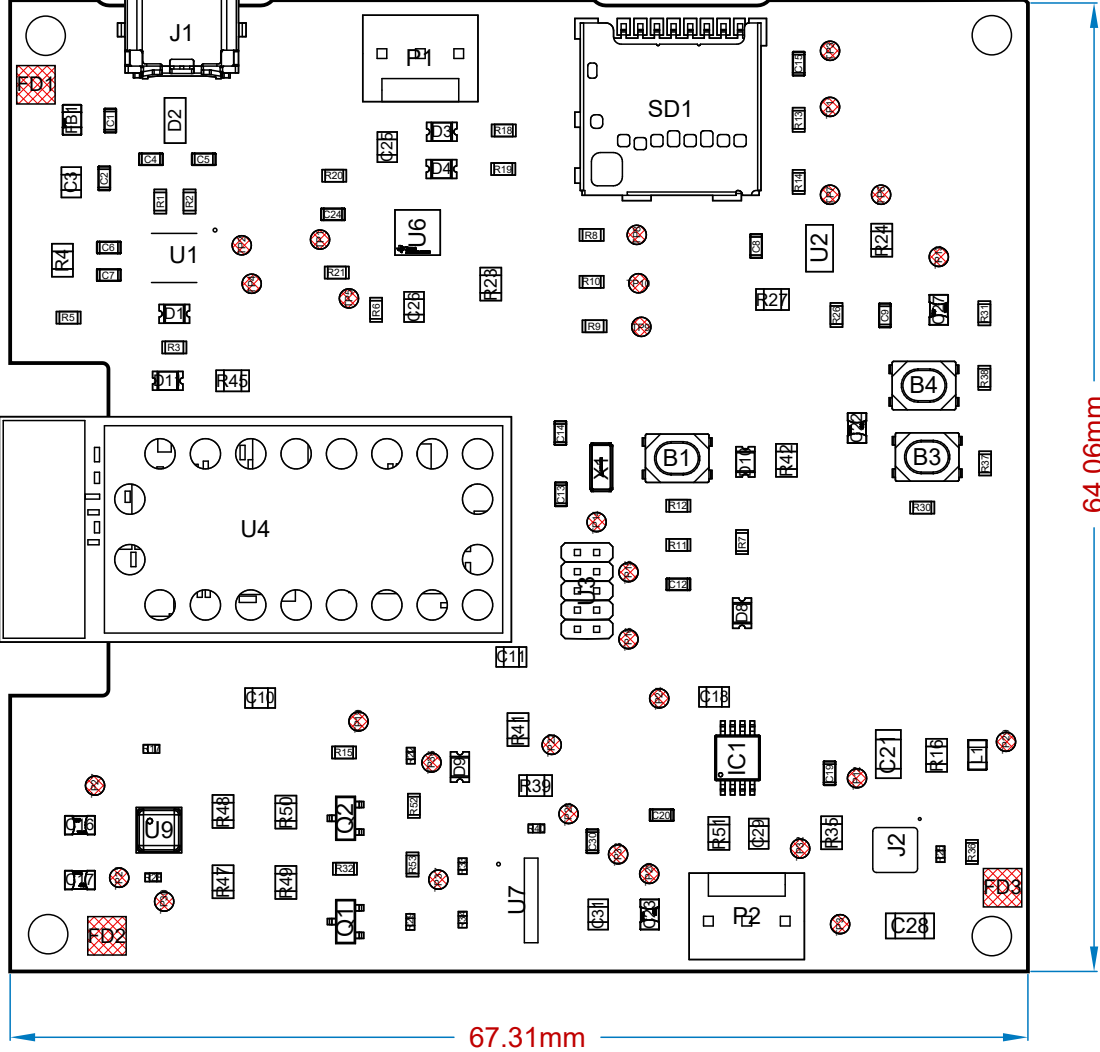
Four(4) Layers
Dimensions: 67.31mm x 64.32mm
Thickness: 1.53mm
Material: FR4
All layers are unmirrored - shoule be able to "see straight through"
Scoring: none

Finished Thickness: 0.062 inches
Surface Finish: ENEPIG
Gold Fingers: No
Outer Layer Finish Copper: 1 Oz
Inner Copper: 0.5 oz inners
Number of Holes Per Board: 193
Minimum Hole Size: 0.008 inches or more
Minimum Trace(Out layer): 0.006 inches
Minimum Space(Out layer): 0.006 inches
Minimum Trace(Inner layer): 0.006 inches
Minimum Space(Inner layer): 0.006 inches
Solder Mask: Yes
Solder Mask Sides: Top and Bottom
Solder Mask Color: Green
Solder Mask Type: LPI
Solder Mask Finish: Standard(Semi-Gloss)
Silk Screen: Yes
Silk Screen Sides: Both
Silk Screen Color: White
Internal Slots: None
Counter Sink: No
Counter Bore: No
Edge Plating: No
Route and Retain: Yes
Scoring: Yes
Controlled Impedance: None
Controlled Dielectric: None
Thru-Hole Via in Pad: No
Thickness Tolerance: Plus or Minus 10%
Logo Allowed: In copper or silk screen
UL Marking Required: Yes
Rohs Marking: Yes
ITAR?: No

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
Surface Material	Top Overlay			Legend	GTO
	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.04mm		Signal	GTL
Prepreg		0.33mm	PP-006	Dielectric	
CF-004	GroundPlane	0.02mm		Signal	G1
Core		0.71mm	Core-009	Dielectric	
CF-004	PowerPlane	0.02mm		Signal	G2
Prepreg		0.33mm	PP-006	Dielectric	
Copper	Bottom Layer	0.04mm		Signal	GBL
Surface Material	Bottom Solder	0.03mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.53mm					

View from Top side (Scale 2:1)

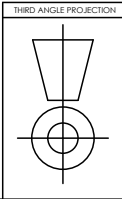
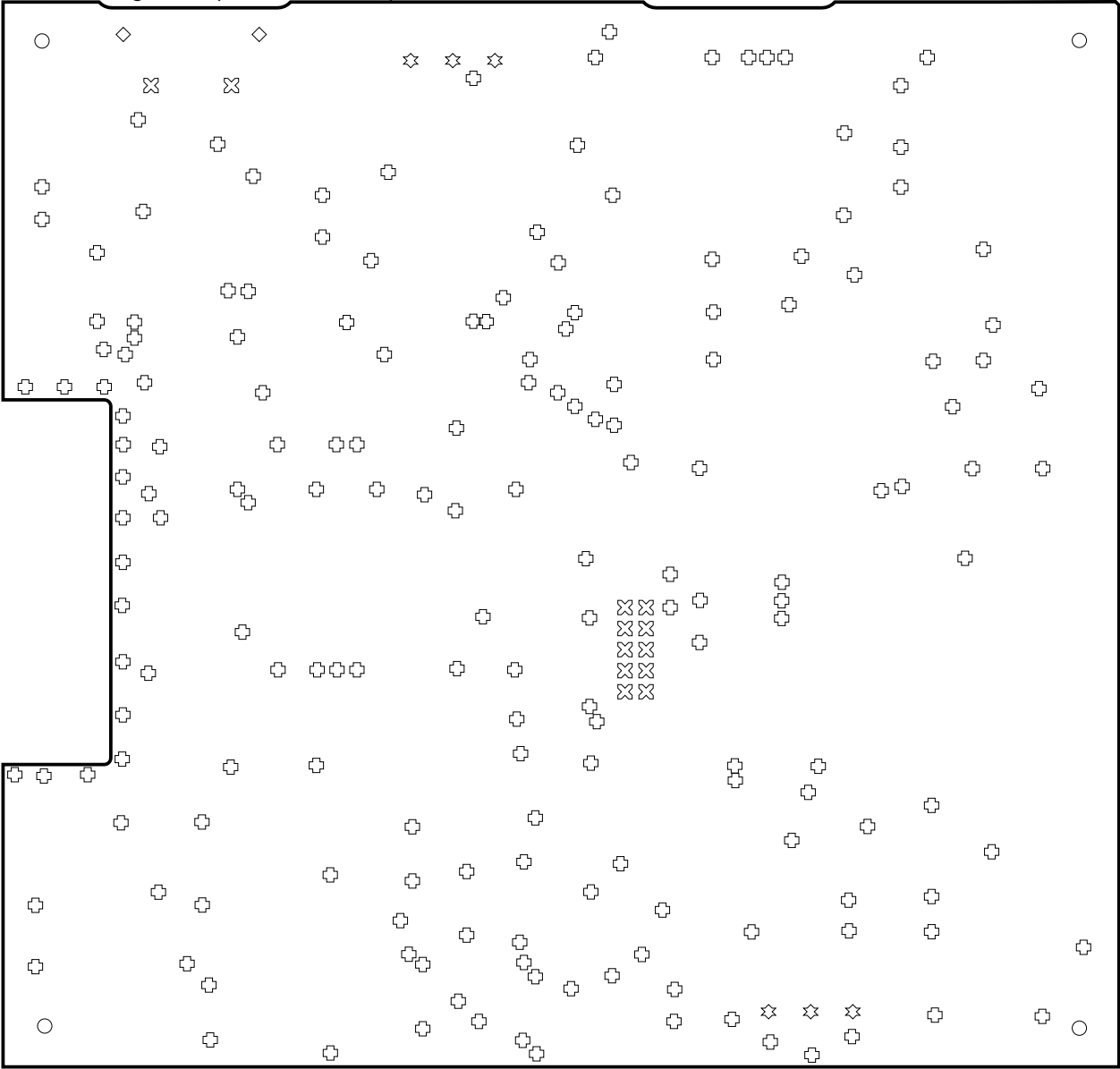


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Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊕	181	0.20mm	Plated	
⊗	12	0.65mm	Plated	
◇	2	0.70mm	Plated	
☆	6	1.27mm	Plated	
○	4	2.70mm	Plated	
	205 Total			

Drill Drawing View (Scale 2.4513:1)

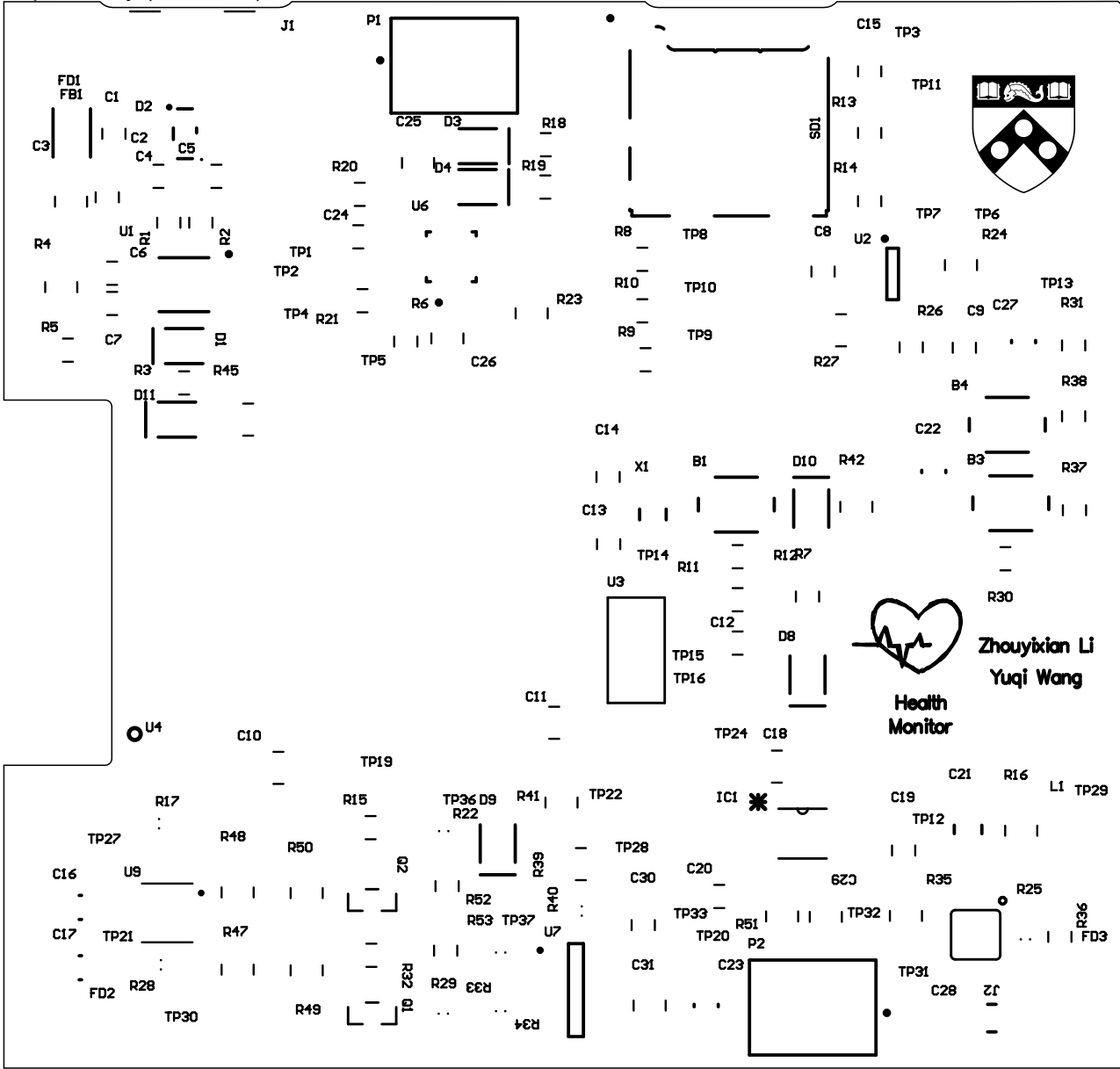



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DESIGNER: YUQI WANG;	YUQI WANG;
CHECKER: YUQI WANG;	YUQI WANG;
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ASSY DOC: StarterBoardFabrication	
SCH DOC: MAIN	
PCB DOC: =PCB_DWG_NO	
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DESIGN ITEM REVISION: .ItemRevision	
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SHEET: 2 OF 11	

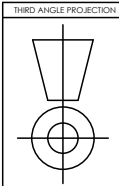
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	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED	

Top Overlay (Scale 5:2)



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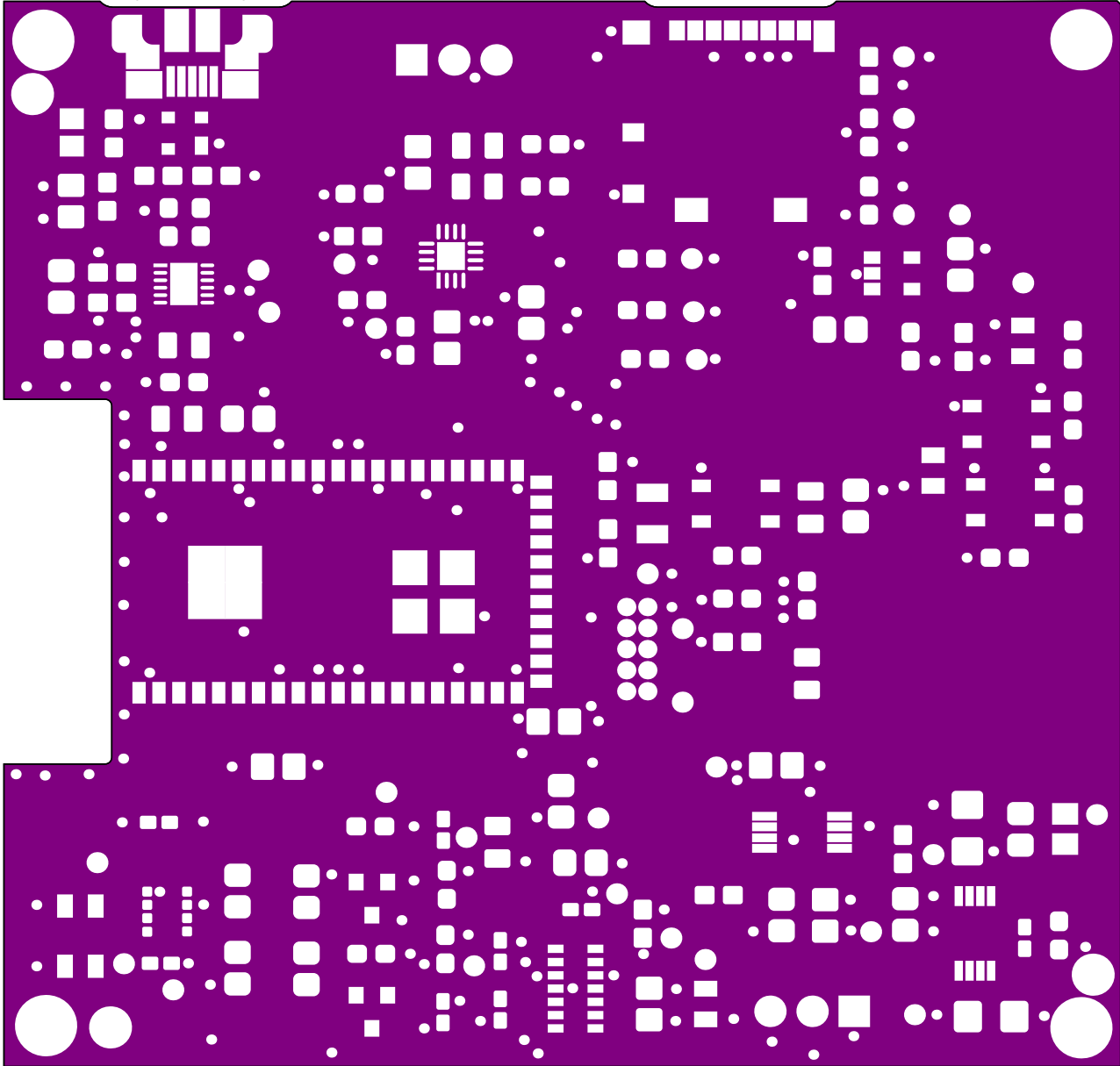


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TOP SOLDER MASK

Top Solder (Scale 5:2)

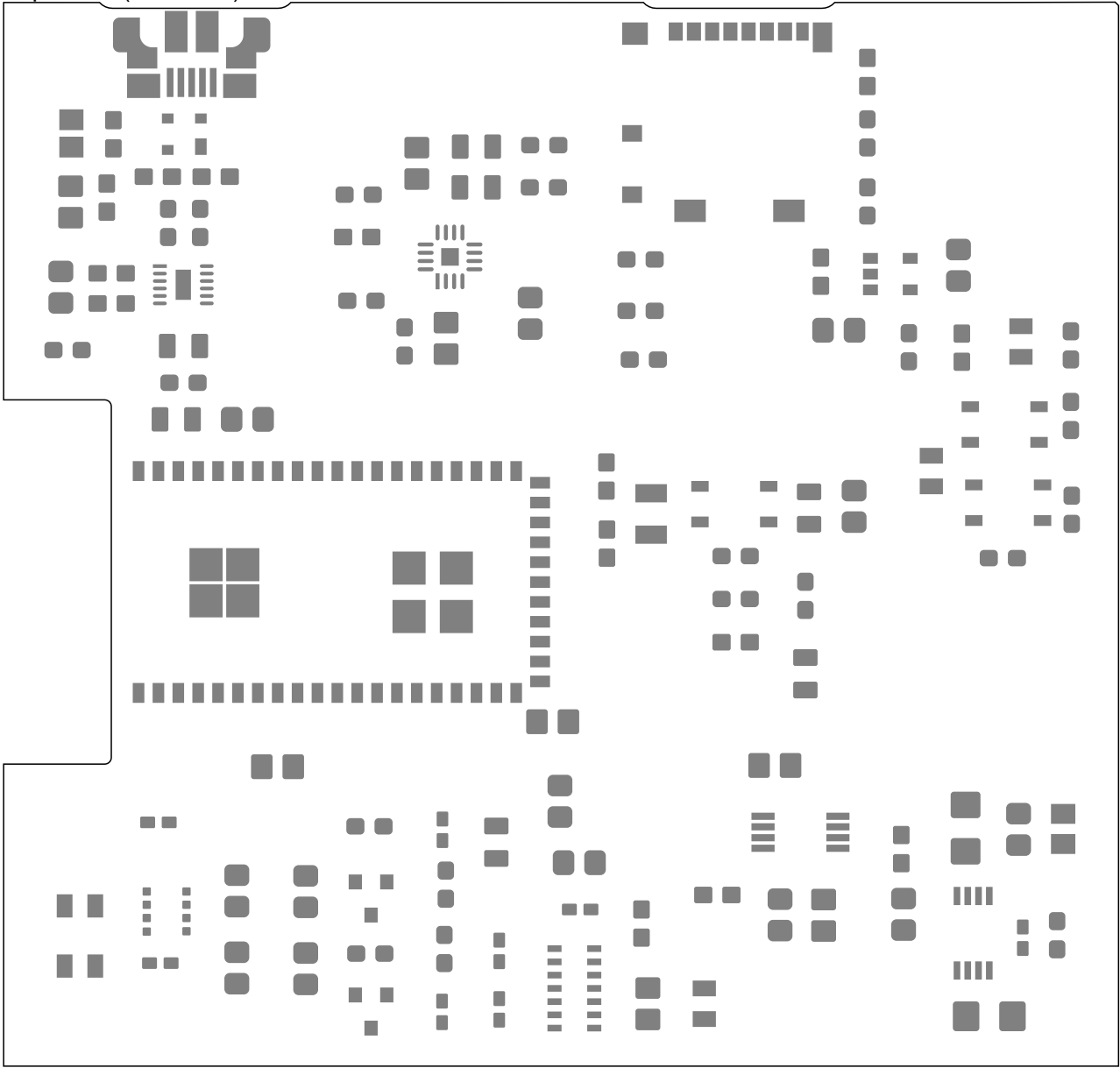


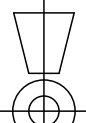
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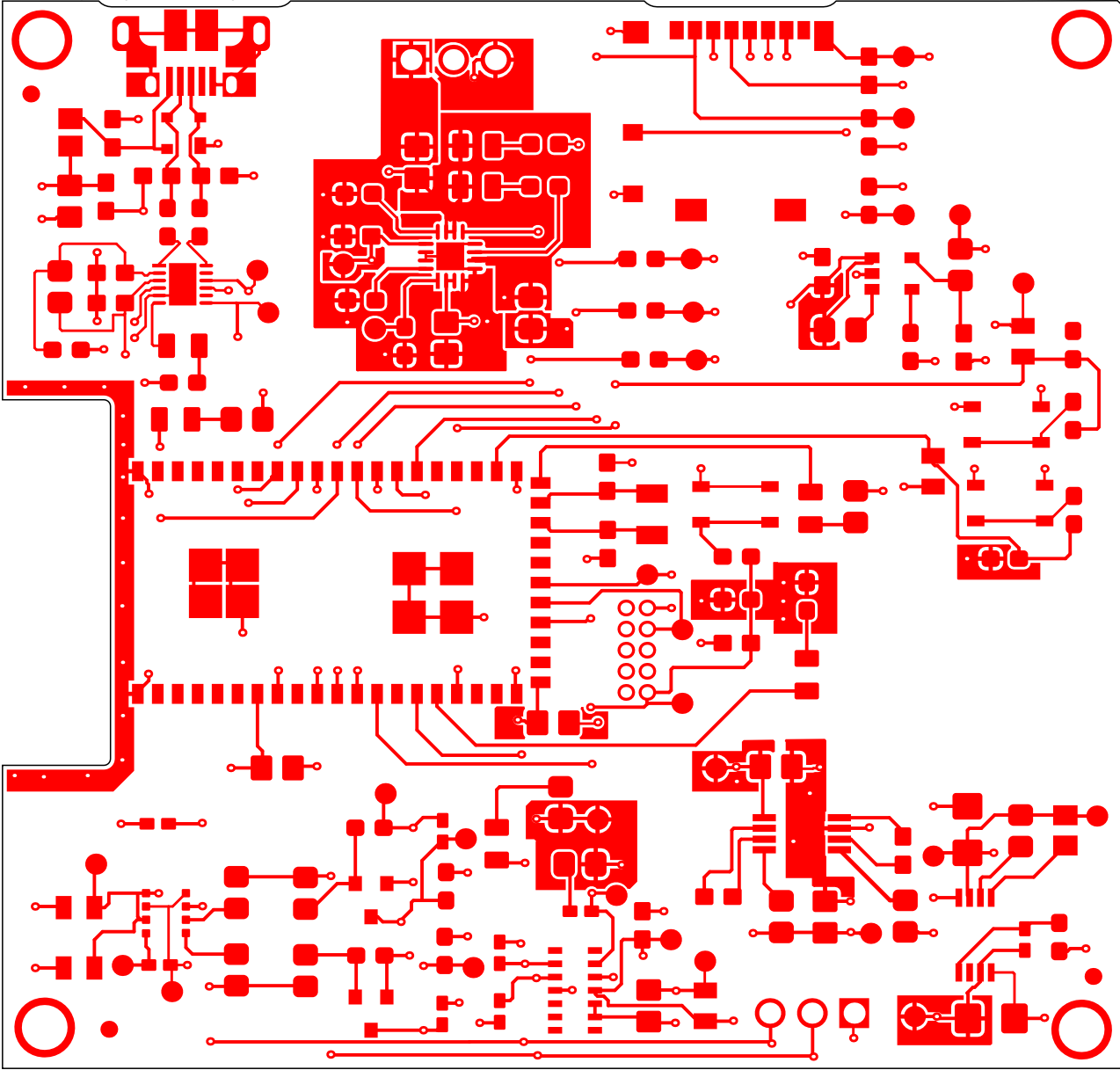


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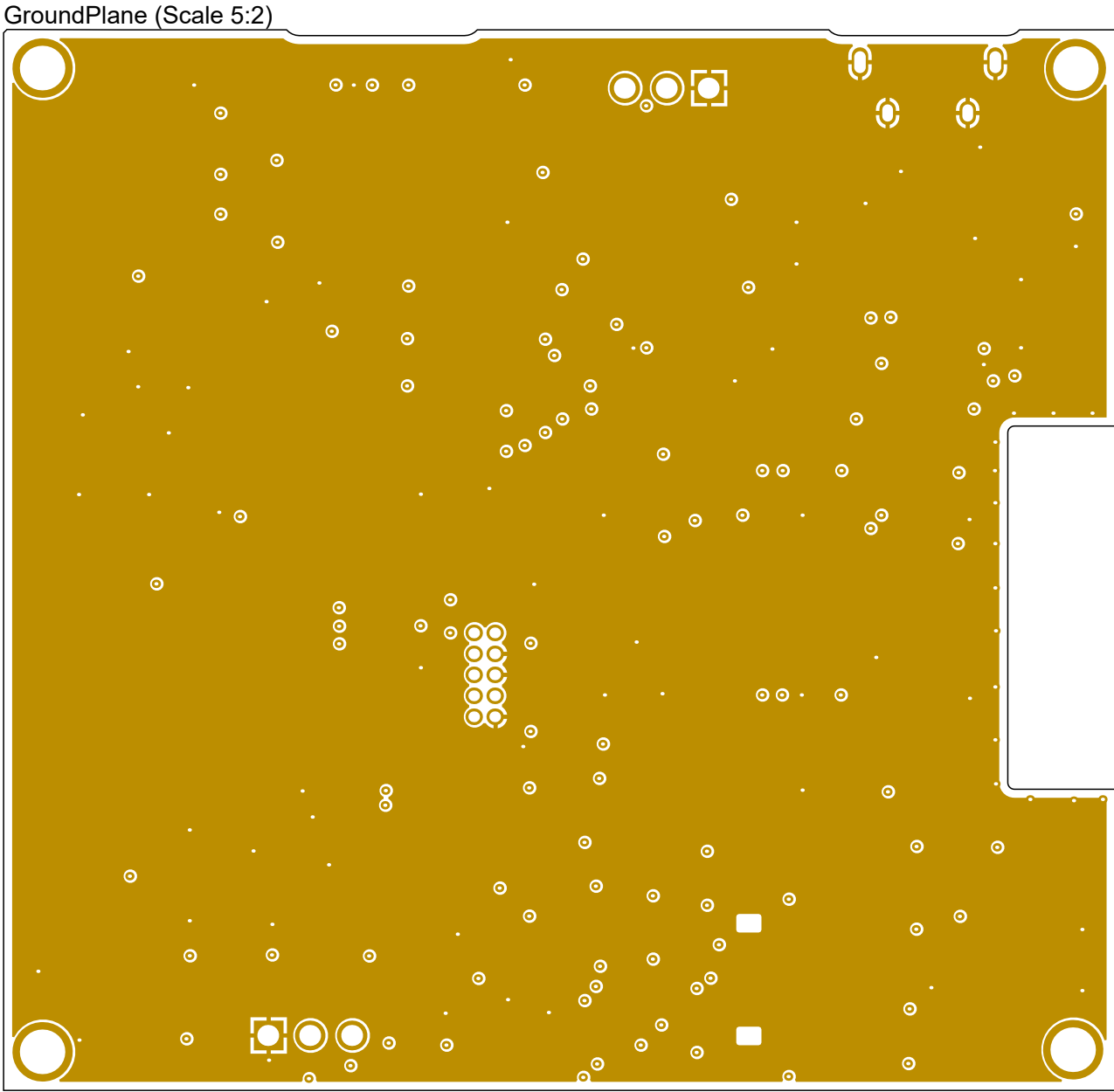
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Top Layer (Scale 5:2)



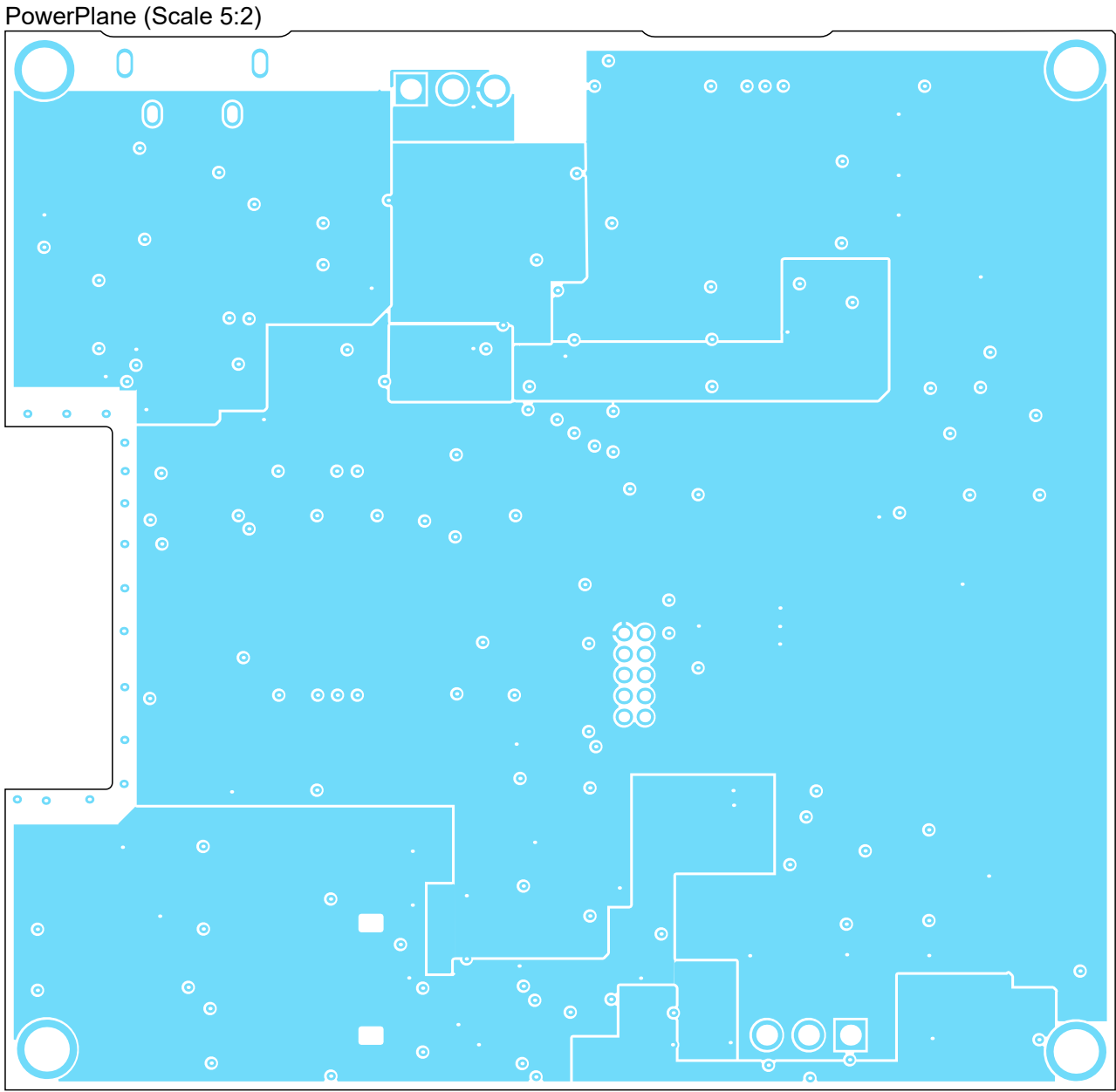
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APPLICATION				SCALE:	FILE NAME: StarterBoardFabrication.PCBDef	SHEET: 8 OF 11	

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1

2

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A

B

C

D

E

F

Bottom Paste (Scale 5:2)

THIRD ANGLE PROJECTION

NEXT ASSY

USED ON

APPLICATION

PART NO: =PCB_PART_NUMBER

APPROVALS

ENGINEER: ZHOUYIXIAN LI; YUQI

DESIGNER: YUQI WANG;

CHECKER: YUQI WANG;

DATE

ZHOUYIXIAN LI;

YUQI WANG;

YUQI WANG;

Reference Documents

BOM DOC: ESE516_PCB

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SCH DOC: MAIN

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FILE NAME: StarterBoardFabrication.PCBDwf

APPROVED

DATE

REVISIONS

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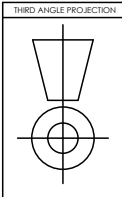
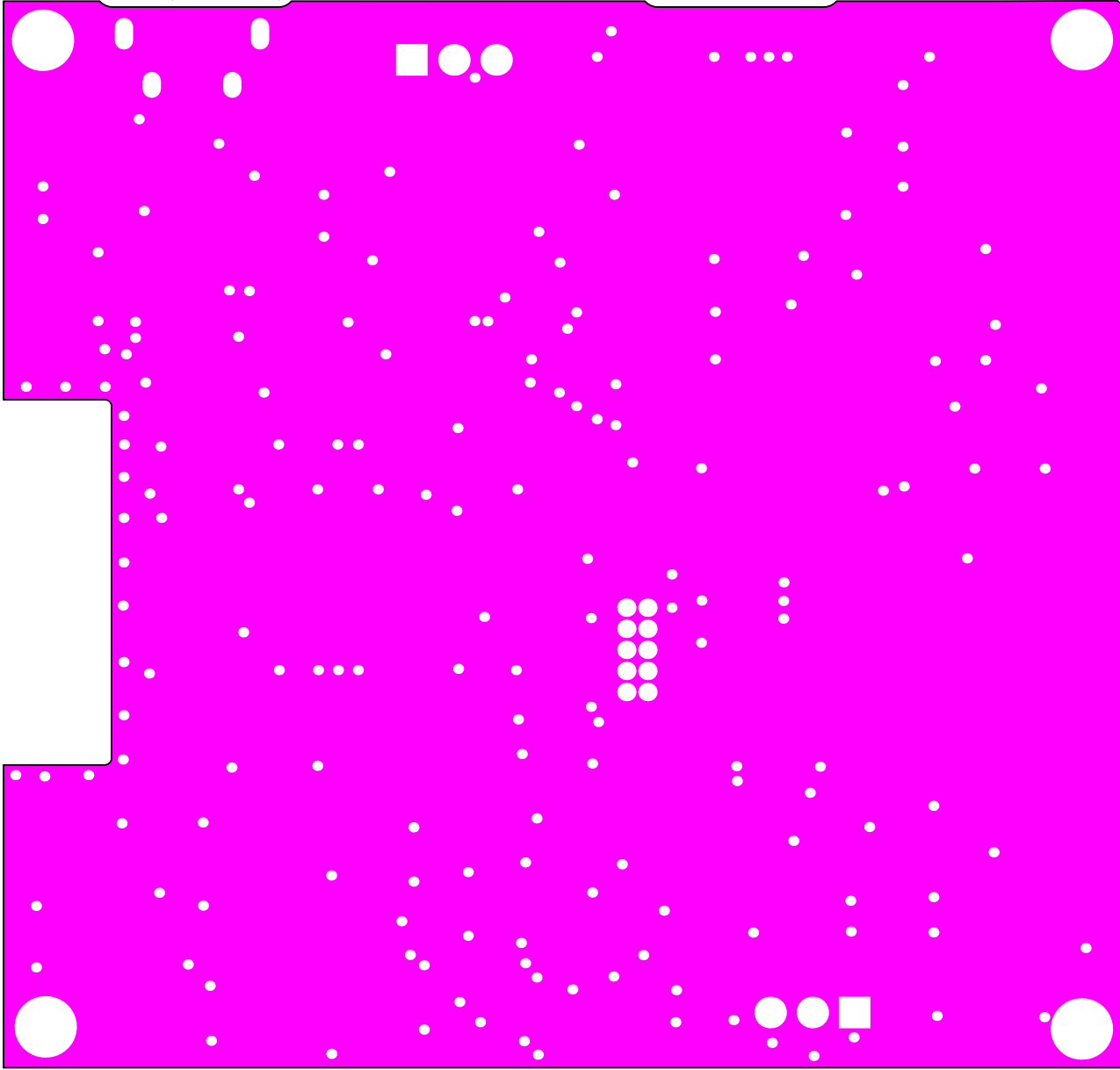
OF 11

SHEET:

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REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED

Bottom Solder (Scale 5:2)



THIRD ANGLE PROJECTION	
NEXT ASSY	USED ON
APPLICATION	

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DESIGNER: YUQI WANG;		YUQI WANG;			
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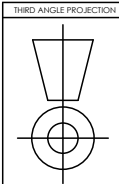
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Bottom Overlay (Scale 5:2)

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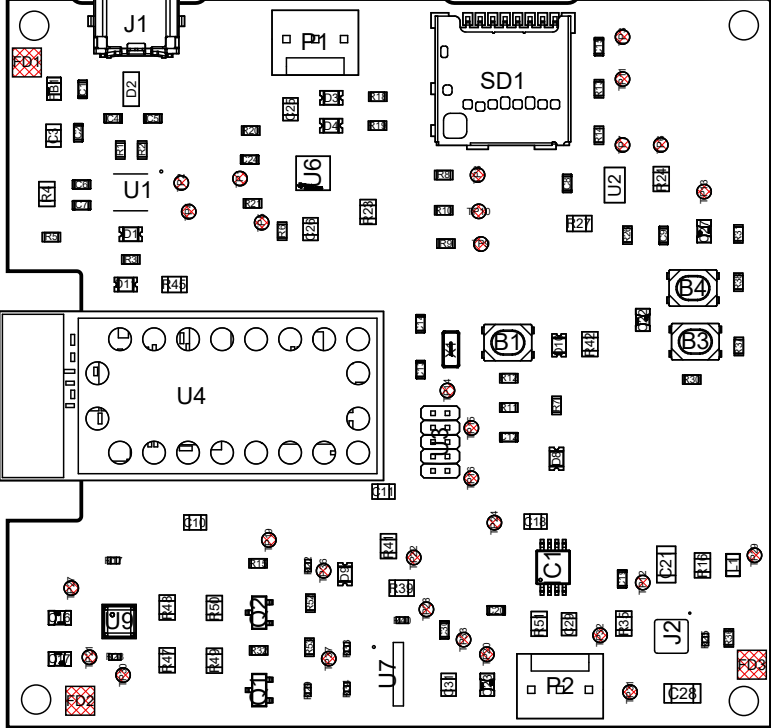


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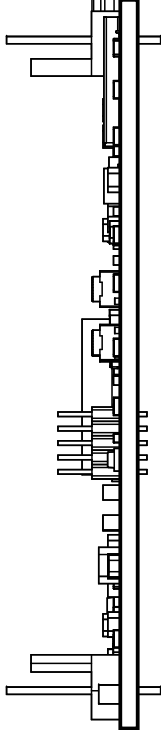
Notes :

1. THIS ITEM IS ELECTROSTATIC SENSITIVE
AND SHALL BE HANDLED ACCORDINGLY

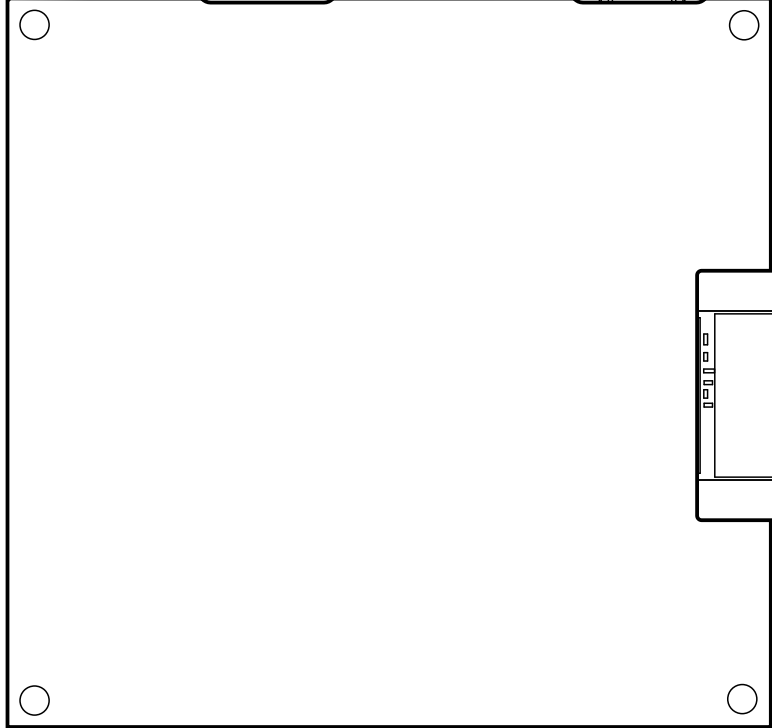
View from Top side (Scale 3:2)



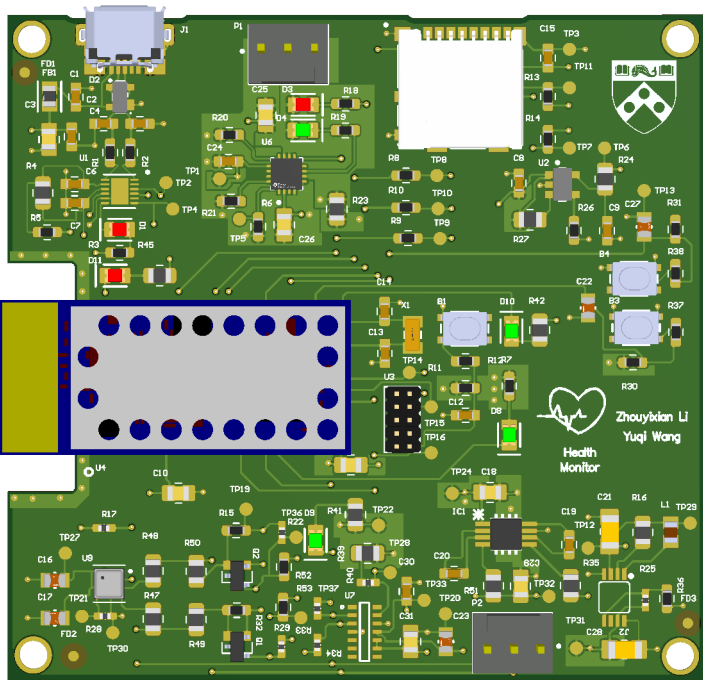
View from Right side (Scale 3:2)




View from Bottom side (Scale 3:2)

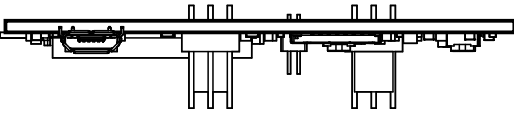


Realistic View



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