OCD - Resumo

→ Portas lógicas:

1. AND = $p \wedge q \iff r$

Símbolo:

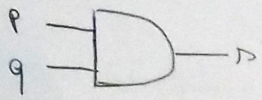


Tabela verdade:

p	q	r
0	0	0
0	1	0
1	0	0
1	1	1

2. OR = $p \vee q \iff r$

Símbolo:

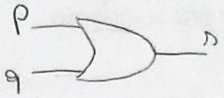


Tabela Verdade:

p	q	r
0	0	0
0	1	1
1	0	1
1	1	1

3. NOT / INVERSOR = $\neg p \iff \bar{p} \iff r$

Símbolo:

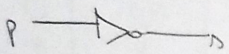


Tabela Verdade:

p	r
0	1
1	0

4. XOR / OU EXCLUSIVO = $p \veebar q \iff r$

Símbolo:

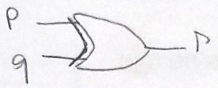


Tabela Verdade:

p	q	r
0	0	0
0	1	1
1	0	1
1	1	0

Obs.: Todas as portas lógicas podem ser descritas utilizando AND, OR e NOT.

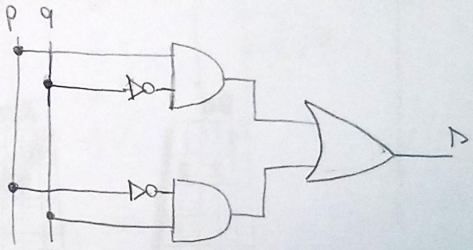
Ex.: As seguintes equivalências são válidas para o XOR:

1. $(p \wedge \neg q) \vee (\neg p \wedge q) \iff r$:

Tabela Verdade:

p	q	¬p	¬q	p∧¬q	¬p∧q	(p∧¬q)∨(¬p∧q)	XOR
0	0	1	1	0	0	0	0 ✓
0	1	1	0	0	1	1	1 ✓
1	0	0	1	1	0	1	1 ✓
1	1	0	0	0	0	0	0 ✓

Circuito:

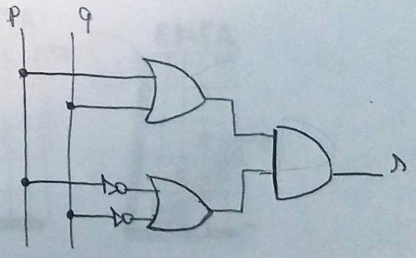


2. $(p \vee q) \wedge (\neg p \vee \neg q) \iff r$:

Tabela Verdade:

p	q	¬p	¬q	p∨q	¬p∨¬q	(p∨q)∧(¬p∨¬q)	XOR
0	0	1	1	0	1	0	0 ✓
0	1	1	0	1	1	1	1 ✓
1	0	0	1	1	1	1	1 ✓
1	1	0	0	1	0	0	0 ✓

Circuito:

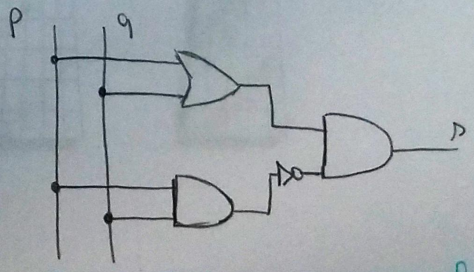


3. $(p \vee q) \wedge \neg(p \wedge q) \iff r$:

Tabela Verdade:

p	q	p∨q	p∧q	¬(p∧q)	(p∨q)∧¬(p∧q)	XOR
0	0	0	0	1	0	0 ✓
0	1	1	0	1	1	1 ✓
1	0	1	0	1	1	1 ✓
1	1	1	1	0	0	0 ✓

Circuito:



Obs.: As equivalências são obtidas aplicando as leis de DeMorgan nas exp. lógicas.

5. NAND = $\neg(p \wedge q) \iff \wedge$

Símbolo:

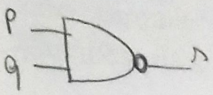


Tabela Verdade:

p	q	p∧q	∧
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

6. NOR = $\neg(p \vee q) \iff \wedge$

Símbolo:

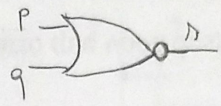


Tabela Verdade:

p	q	p∨q	∧
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Obs.: As portas NAND e NOR são chamadas portas universais, pois podem ser combinadas para implementar o AND, OR e NOT.

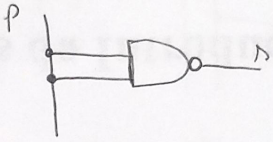
→ Universalidade do NAND:

I. Inversor = $\neg(p \wedge p) \iff \neg p \iff \wedge$

Tabela Verdade:

p	p∧p	¬(p∧p)	¬p	
0	0	1	1	✓
1	1	0	0	✓

Circuito:

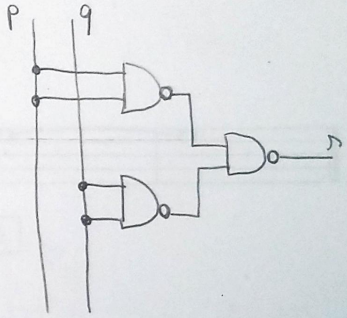


II. OR = $\neg(\neg(p \wedge p) \wedge \neg(q \wedge q)) \iff p \vee q \iff \wedge$

Tabela Verdade:

p	q	p∧p	¬(p∧p)	q∧q	¬(q∧q)	a = ¬(p∧p) ∧ ¬(q∧q)	¬a	p∨q	
0	0	0	1	0	1	1	0	0	✓
0	1	0	1	1	0	0	1	1	✓
1	0	1	0	0	1	0	1	1	✓
1	1	1	0	1	0	0	1	1	✓

Circuito:

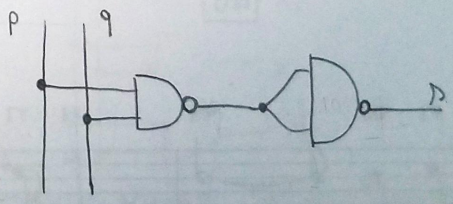


III. AND = $\neg(\neg(p \wedge q) \wedge \neg(p \wedge q)) \iff p \wedge q \iff \wedge$

Tabela Verdade:

p	q	p∧q	¬(p∧q)	a = ¬(p∧q) ∧ ¬(p∧q)	¬a	p∧q	
0	0	0	1	1	0	0	✓
0	1	0	1	1	0	0	✓
1	0	0	1	1	0	0	✓
1	1	1	0	0	1	1	✓

Circuito:



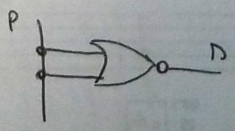
→ Universalidade do NOR:

I- Inversor = $\neg(p \vee p) \iff \neg p \iff \wedge$

Tabela Verdade:

p	p∨p	¬(p∨p)	¬p	
0	0	1	1	✓
1	1	0	0	✓

Circuito:

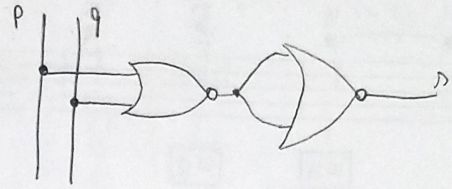


II - OR = $\neg(\neg(p \vee q) \vee \neg(p \vee q)) \Leftrightarrow p \vee q \Leftrightarrow \wedge$

Tabela Verdade:

p	q	p∨q	¬(p∨q)	a = ¬(p∨q)∨¬(p∨q)	¬a	p∨q	
0	0	0	1	1	0	0	✓
0	1	1	0	0	1	1	✓
1	0	1	0	0	1	1	✓
1	1	1	0	0	1	1	✓

Circuito:

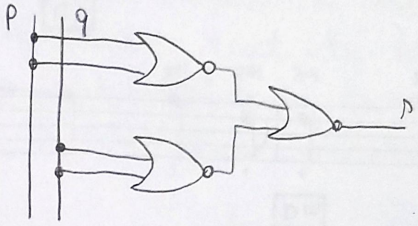


III - AND = $\neg(\overbrace{\neg(p \vee p) \vee \neg(q \vee q)}^{a}) \Leftrightarrow p \wedge q \Leftrightarrow \wedge$

Tabela Verdade:

p	q	p∨p	¬(p∨p)	q∨q	¬(q∨q)	a	¬a	p∧q	
0	0	0	1	0	1	1	0	0	✓
0	1	0	1	1	0	1	0	0	✓
1	0	1	0	0	1	1	0	0	✓
1	1	1	0	1	0	0	1	1	✓

Circuito:



7. XNOR = $\neg(p \dot{\vee} q) \Leftrightarrow \wedge$

Símbolo:

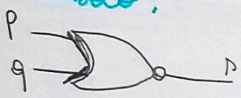
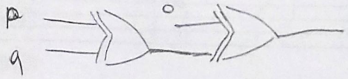


Tabela Verdade:

p	q	p∨̇q	∧
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

NOT com XNOR:

OR com XNOR:



Descodificador

a	b	x_1	x_2	x_3	x_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

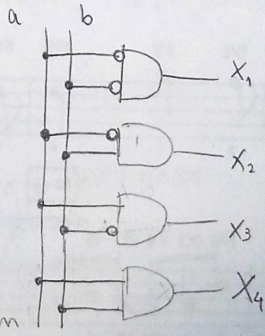
$x_1 = \neg a \wedge \neg b$

$x_2 = \neg a \wedge b$

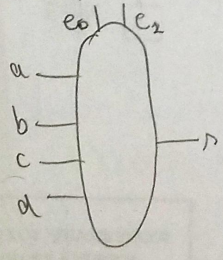
$x_3 = a \wedge \neg b$

$x_4 = a \wedge b$

→

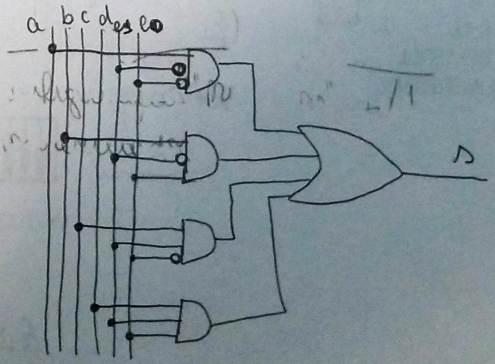


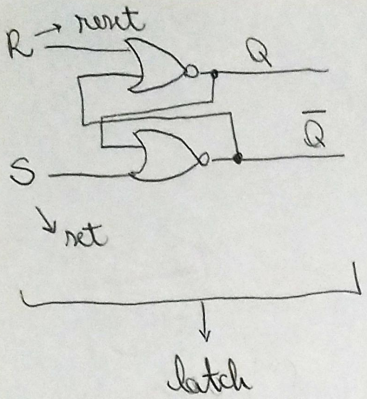
Multiplexador



(X) = don't care → indicam em quem vamos "prestar atenção"

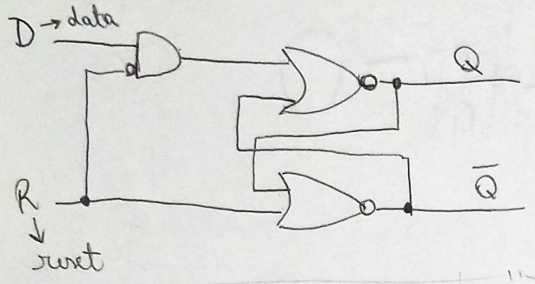
a	b	c	d	e_1	e_0	S
0	X	X	X	0	0	0
1	X	X	X	0	0	1
X	0	X	X	0	1	0
X	1	X	X	0	1	1
X	X	0	X	1	0	0
X	X	1	X	1	0	1
X	X	X	0	1	1	0
X	X	X	1	1	1	1



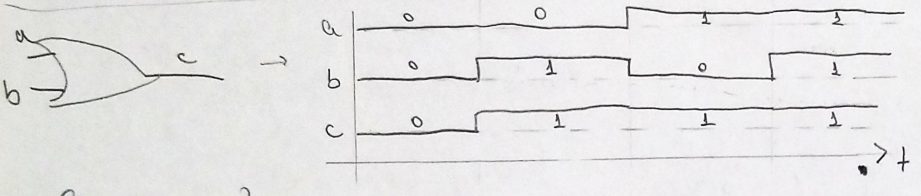


R	S	Q_A	$\bar{Q}_A$	Q_D	$\bar{Q}_D$	
0	0	0	1	0	1	} Se R=S=0, $Q_A=Q_D$ e $\bar{Q}_A=\bar{Q}_D$
0	0	1	0	1	0	
1	0	0	1	0	1	} Reset
1	0	1	0	0	0	
0	1	0	1	1	0	} set
0	1	1	0	1	0	
1	1	X	X	?	?	} não determinístico (depende de que responder 1º)

Q_A = antes (entrada)
Q_D = depois (saída)

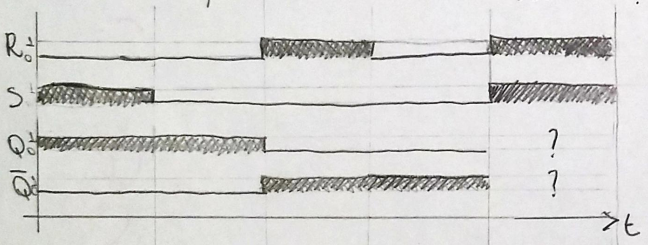


Desse modo, é impossível ativar o Data quando reset está ativado. Quando Reset é desligado, Data é copiado em Q (e $\bar{Q}$ fica invertido).

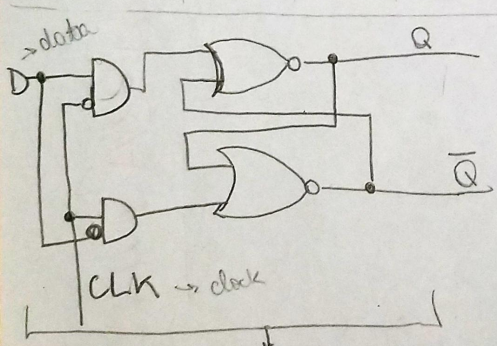


Vantagem dessa representação: acompanha a variação ao longo do tempo.

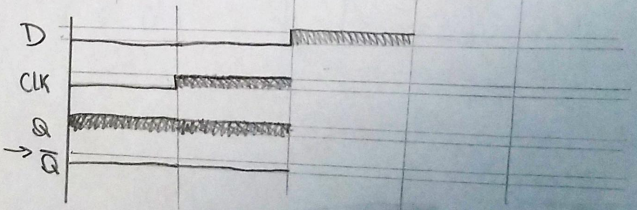
→ Representação do circuito latch:



Quando dá set, sobe Q e desce $\bar{Q}$.
Quando dá reset, desce Q e sobe $\bar{Q}$.
Nome: diagrama de tempos



LATCH tipo D



Não há mais configurações "proibidas". 1/1 e 0/0 geram o mesmo resultado.