Core Area Calculations				
Name of Block	**Category**	**Gate/FF Count**	**Area (um2)**	**Comments**
Input FIFO	Reg. w/ Reset	97	232,800	Based on rx_fifo.sv module from Lab 6
Comparator Block	Combinational	3860	2,895,000	((23 LUs * 4 subcomp.) + 4(2 * 8 bit inputs *17 XNOR) - (3 * 8 bit inputs * 17 XNOR)) * 5 instances
Output FIFO	Reg. w/ Reset	97	232,800	Based on rx_fifo.sv module from Lab 6
Controller State Register	Reg. w/ Reset	4	9,600	
Controller Next State Register	Reg. w/ Reset	4	9,600	
Controller Next State Logic	Combinational	8	6,000	Two 2-way MUX (4 each)
Controller Output Logic	Combinational	300	225,000	8 bit length * 17 characters + 32 bit address * 5 addresses + 4 output signal logic
Comparator Address Registers	Reg. w/ Reset	296	710,400	Stores 17 8-bit wide characters
Result Address FSM State Register	Reg. w/ Reset	3	7,200	
Result Address FSM Next State Register	Reg. w/ Reset	3	7,200	
Result Address FSM Next State Logic	Combinational	10	7,500	2-way MUX (4) + adder w/ rollover (6)
Result Address FSM Output Registers	Reg. w/ Reset	160	384,000	
Triple Speed Ethernet MAC	Combinational	266	199,500	Based on instantiation of Altera IP TSE MAC with one PLL (may be more in final design)
Total Core Area		5108	4,926,600	

Chip Area Calculations (units in um or um2)			
Number of I/O Pads:	12		
I/O Pad Dimensions:	90	by	300
I/O Based Padframe Dimensions:	870	by	870
Core Dimensions	2,220	by	2,220
Core Based Padframe Dimensions:	3,120	by	3,120
Final Padframe Dimensions:	3,120	by	3,120
Final Chip Area:	9,731,870		

Starting Component	Propagation Delay (ns)	Combinational Logic	Propagation Delay (ns)	Ending Component	Setup Time or Propagation Delay (ns)	Total Path Delay (ns)	Target Clock Period (ns)
Comparator Register	0.1	Comparator Logic	1.2	Match Flag Register (in Controller)	0.2	1.5	10
Result Address Register	0.1	Address selector (mux)	1	Result Address Register	0.2	1.3	10
Controller FSM State	0.1	Next State Logic: data_rdy mux, reset mux, match mux, state change	2.92	Controller FSM State	0.2	3.22	10
FIFO Full Flag Register	0.1	Full Flag Next Value Logic	3.96	FIFO Full Flag Register	0.2	4.26	10
Result Addresses FSM State	0.1	Next State Logic	1.96	Result Addresses FSM State	0.2	2.26	10

Comparator Logic consists of two 8 bit values compared bit by bit with an xor and then and'd together (6 levels * .2 ns/gate)

Combinational Adder logic consists of a 25 way selector, implying 5 levels of logic for each piece of data (5 levels * .2ns/gate)

Controller FSM next state logic consists of 3 multiplexers (3 * .2ns/gate) and the worst case scenario state change (log(5) = 2.32)

Fifo values obtained by running the course FIFO module.

Result Address FSM Next State Logic consists of 2 multiplexers (2 * .2ns) and worst case scnario state change (log(3) = 1.56)

*Assume negliglbe effect from inverters

Clock rate: 100 MHz, 10 ns/cycle