

Hardware User Guide

OMAP35x Evaluation Module



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About This Manual

Developed with Mistral Solutions, the OMAP35x Evaluation Module (EVM) enables developers to start immediate evaluation of OMAP™ processors and begin building low power applications such as Digital TV, Navigation, Games, Data Terminals, point of sale / service, software defined radio, Medical, media controllers and numerous other low power, high performance products that have yet to be invented.

This document describes the board level operations of the OMAP35x Evaluation Module (EVM). The EVM is based on the Texas Instruments OMAP3530 Applications Processor.

Notational Conventions

This document uses the following conventions.

The OMAP35x Evaluation Module will sometimes be referred to as the OMAP35x EVM or EVM.

Information about Cautions

This Document may contain cautions.



This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the OMAP 3530 Processor can be found at the following Texas Instruments website: <http://www.ti.com>

Table 1: Document History

Rev. No	History
Rev 1.0	Production Release
Rev 1.1	Changed the PoP memory to Micron
Rev 1.2	Merged Micron & Samsung PoP details
Rev 1.3	Processor module change from 3503 to 3530. Added details to Micron higher DDR memory.
Rev 1.4	Micron Memory changed from 1G/2G to 2G/2G On board MDC features added On board Camera Module support added
Rev 1.5	Reviewed , added new pics for the Main board, Processor & Power module

Table 2: Board History

PCB Revision	History
REV G	EVM Main Board
REV D	Power Module
REV C	Processor Module



The Boards contains Electro-static Discharge (ESD) sensitive devices. Take proper precautions to ground yourself before handling the board.

Chapter 1

Introduction to the OMAP35x EVM

1. Introduction

Chapter one provides a brief description of the OMAP35x EVM along with the key features and a high-level block diagram of the system.

1.1 System block diagram

Featuring the OMAP3530 high-performance application processor comprising of Super scalar ARM® Cortex™-A8 with NEON co-processing, IVA2.2 subsystem with a C64x+ digital signal processor (DSP) core and SGX subsystem for 2D and 3D graphics acceleration to support display and gaming effects, this EVM kit will allow developers to evaluate and jumpstart development. Equipped with daughter card expansion connectors, the OMAP35x EVM can be upgraded to prototype complete systems.

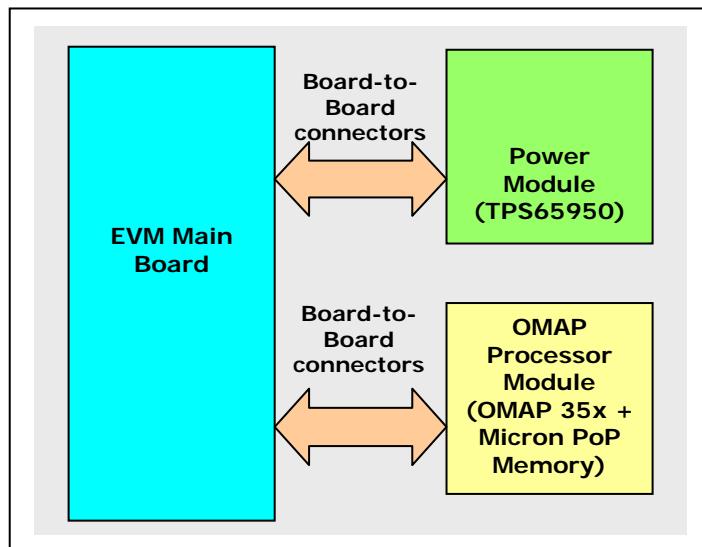


Figure 1: OMAP 35x EVM System Block Diagram

1.2 Functional block diagram

The EVM comes with complete set of on-board devices that suits a wide variety of application environments. The functional block diagram of the OMAP 35x EVM is given below:

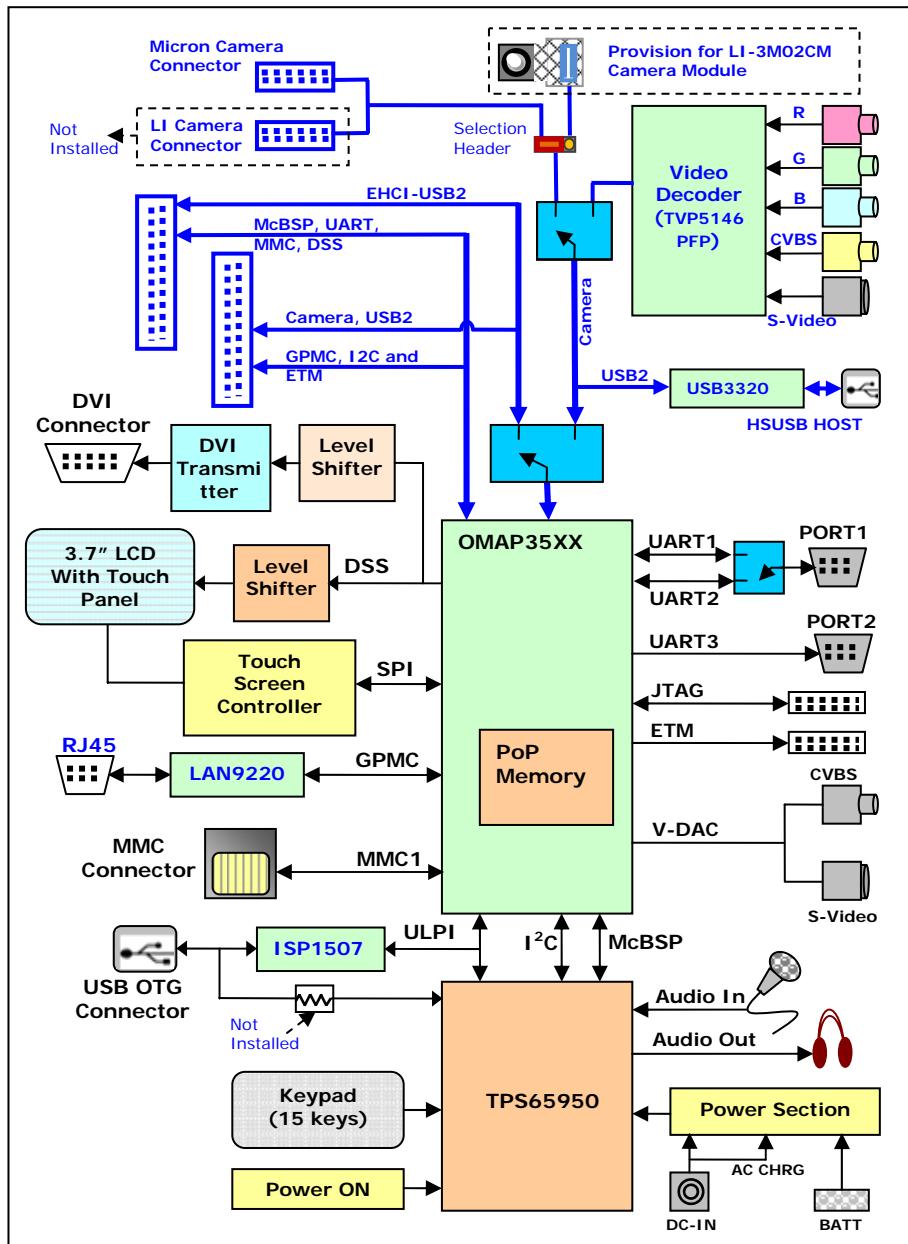


Figure 2: OMAP 35x EVM Functional Block Diagram

1.3 Key Features

The key features are:

- Texas Instruments' OMAP 3530 high performance applications processor based on the enhanced OMAPTM 3 architecture.
- Memory
 - Micron PoP memory supporting 2Gbit NAND flash and 2Gbit Mobile DDR SDRAM (64M x 32 bus width and 166 MHz maximum operating frequency)
- Power Module based on TPS65950 power management and audio companion device
- 3.7" dual mode (QVGA/VGA) LCD display with Touch Screen support
- CVBS and S-Video TV OUT interfaces
- High Speed USB OTG 2.0 interface using external transceiver ISP1507 from NXP
- High speed USB Host interface (USB2 port) using external transceiver USB3320 from SMSC
- 10/100 Mbps Ethernet interface
- Stereo Audio Interface – Auxiliary Line IN and Headset OUT
- 1/4/8 bit SD/MMC interface
- 4x4 Keypad Interface
- Three RS-232 UART interfaces (multiplexed on two ports)
- Dip switch to select Boot mode configurations
- Video Input options on camera interface port of OMAP (Either 1/2/3 shall be active at anytime)
 1. Video Encoder TVP5146
 - a. S-Video Input
 - b. Composite Video Input
 - c. Component Video Input
 2. Camera Interface from 26-Pin Micron Connector
 3. Provision for plugging the LI-3M02CM camera module from Leopard Imaging.

- Standard 14-pin JTAG debug interface
- Embedded Trace Macrocell (ETM) debug interface
- Dual general purpose expansion connectors supporting
 - TPS65950 ADC Input channels
 - 12 bit Camera Parallel Interface
 - UART(3), McBSP(2), SPI(2), SD/MMC(2), I2C(2) Interfaces
 - DSS(24 bit), GPMC(16-bit) bus
 - ETM debug interface
- The OMAP35x EVM is RoHS compliant

1.4 Functional Overview

The OMAP35x EVM is based on TI's OMAP 3530 applications processor. The Micron memory is interfaced to the OMAP 3530 processor via the Package-On-Package technology. The Micron PoP memory supports 2Gbit NAND flash and 2 Gbit Mobile DDR SDRAM. The DDR memory and NAND Flash are connected to SDRAM controller (SDRC) and General Purpose memory Controller (GPMC) interfaces of processor respectively.

It is also equipped with a 3.7" TFT LCD module from Sharp. This LCD Module is interfaced to the Display subsystem (DSS) interface of the processor.

Analog Video outputs of EVM support both Composite TV (CVBS) output and S-Video output on the main board. The CVBS or S-Video Outputs are available on respective connector by default.

OMAP35x EVM supports multiple video input options through OMAP3530's camera port. Any one of the below interface shall be active at a given point of time.

1. S-Video Input, digitized through Video decoder (TVP5146PFP)
2. Composite Video Input through Video decoder (TVP5146PFP)
3. Component Video Input through Video decoder (TVP5146PFP)
4. Camera Interface – 26-Pin camera connector to support Micron Camera Module
5. Camera Interface – Provision for LI-3M02CM camera module

The EVM has a SD/MMC slot using SD/MMC1 interface on the main board. And the SD/MMC2 interface is routed to the expansion connector.

The EVM has a 10/100 Mbps Ethernet interface using an external MAC/PHY controller LAN 9220 which is interfaced to the OMAP3530 via the GPMC interface.

The EVM supports three UART (UART 1, 2 and 3) interfaces via two serial ports on the main board.

High Speed USB OTG interface is supported on the EVM Main Board via an onboard external USB transceiver ISP 1507 from NXP.

High Speed USB HOST (USB2) interface is supported on the EVM Main Board via an onboard external USB transceiver USB3320 from SMSC.

One Stereo Line IN and Stereo Headset OUT audio interface is supported through the audio codec on the TPS65950 device. The audio codec on the power module is controlled by internal registers that can be accessed through high-speed I2C interface.

The EVM includes 11 status LEDs, 2 user DIP switches and 16 push button switches.

It supports the standard 14-pin JTAG and ETM debug interfaces. The EVM is designed to work with TI's Code Composer Studio development, or standard GDB tool environments. For more details refer Getting Start Guide.

The EVM is powered by a +5V external power supply. The TPS65950 power management device provides the required CPU core voltages and IO voltages.

The EVM can also be powered using an external Lithium Ion/Polymer battery. (Battery not supplied with EVM). RTC is supported through a coin cell.

1.5 Memory & I/O Mapping

The Memory and I/O space mapping for the OMAP 35x EVM is given below.

Device	Chip Select	Start Address	End Address	Size	Remarks
SDRC (DDR)	sdrc_ncs0	0x80000000	0x87FFFFFF	128 MB	PoP, Mobile DDR
		0x80000000	0x8FFFFFFF	256 MB	
	sdrc_ncs1				Not used
NAND Flash	gpmc_cs0	0x20000000	0x2FFFFFFF	256MB	PoP, NAND Flash
	gpmc_cs1	0x08000000	0x0FFFFFFF	128MB	Routed to Exp. Connector
	gpmc_cs3	0x18000000	0x1FFFFFFF	128MB	Routed to Exp. Connector
	gpmc_cs4	0x28000000	0x28FFFFFF	128MB	Routed to Exp. Connector

Ethernet controller LAN9220	gpmc_cs5	0x2C000000	0x2C0003FF	1024B	Ethernet MAC/PHY SW programmable start address
	gpmc_cs6	0x30000000	0x37FFFFFF	128MB	Routed to Exp. Connector
	gpmc_cs7	0x38000000	0x3FFFFFFF	128MB	Routed to Exp. Connector

Table 1: Memory & I/O Map

1.6 GPIO Mapping

OMAP Ball No.	Built-in Function	GPIO Function
V8 (NAND Flash)	GPMC_nCS2/GPIO_53	LOCK ¹ (or) DDR_TEMP_SENSE ²
L8	GPMC_WAIT1/GPIO_63	MMC1_WP
AE21	SYS_BOOT5/GPIO_7	ETH_nRESET
AC3	McSPI1_CS1/GPIO_175	TS_nPEN_IRQ
AB1	McSPI1_CS2/GPIO_176	LAN_INTRO
AE1	MCBSP4_CLKX/GPIO_152	LCD_INI
AD1	MCBSP4_DR/GPIO_153	LCD_EnVDD
AD2	MCBSP4_RX /GPIO_154	LCD_QVGA/nVGA
AC1	MCBSP4_FSX/GPIO_155	LCD_RESB
AH26	SYS_BOOT0/GPIO_2	LCD_LR
AG26	SYS_BOOT1/GPIO_3	LCD_UD
AF21	SYS_BOOT6/GPIO_8	LED D19 on Main board
N8	GPMC_nCS7/GPIO_58	HSUSB_OTG_FAULT
AF9	ETK_D8/GPIO_22	HSUSB2_VBUS_EN
AG9	ETK_D9/GPIO_23	USB2_HOST_FAULT
AH14	ETK_D7/GPIO_21	HSUSB2_RESET
D25	CAM_STROBE/GPIO_126	DEC_INT_3V3
C26	CAM_D11/GPIO_110	DEC_PWDN_3V3
B23	CAM_WEN/GPIO_167	DEC_FID_3V3
C23	CAM_FLD/GPIO_98	VDEC_RESET
AA21	McBSP1_FSR/GPIO_157	nCAM_VD_SEL_1V8
U3	GPMC_nBE1/GPIO_61	nUSB2_EN_1V8
T8	GPMC_nCS4/GPIO_55	nFULL_MODEM_EN_1V8

Table 2: GPIO Mapping (OMAP)

Note:

LOCK¹ - R56 is not mounted on the OMAP processor module by default and hence NAND lock functionality is disabled.

POP_INTERRUPT03 - Resistor R56 is NOT mounted on the OMAP processor module by default and hence this signal (INT) is not connected to GPMC_nCS2/GPIO_53.

DDR_TEMP_SENSE²- Resistor R2 is not mounted on the OMAP processor module by default and hence DDR temp sense is disabled.

If the user wants to enable the feature, corresponding resistors need to be mounted.

TPS65950 Ball No.	Built-in Function	GPIO Function
P13	GPIO_15	OSK_EN
F15	LEDA	LCD_ENBK
N14	GPIO_7	DVI_nDISABLE
L4	GPIO_2	T2_GPIO2
N12	GPIO_1	HS_DET
P12	GPIO_0	MMC1_CD
M4	GPIO6	AUDIO_MUTE
D8	UART1.RXD/GPIO8	nCAM_VD_EN_1V8

Table 3: GPIO Mapping (TPS65950)

1.7 I2C Address Mapping

The communication between the Processor and the TPS65950 device is established through the I2C1 interface. The TPS65950 has four I2C address groups. Each I2C address group allows access to a 256-byte register address map.

I2C2 of OMAP3530 is being shared across camera modules. Also it is routed to expansion connector

I2C3 of OMAP35x is connected to Video decoder as a control interface. Also it is routed to expansion connector

The register addressing for I2C interface is given below:

I2C Used	I2C Address Group	Address
I2C #1	ID1	0x48
I2C #1	ID2	0x49
I2C #1	ID3	0x4a
I2C #1	ID4	0x4b
I2C #3	Video Decoder	0xBA

Table 4: I2C Address Mapping

Chapter 2

Board Components

2. OMAP 35x EVM System

This chapter describes the operation of the major components on the OMAP35x EVM.

OMAP35x EVM system consists of

- EVM Main board
- Processor Module
- Power Module

2.1 EVM Main Board

The EVM Main Board provides the peripheral interfaces and connectors for the system along with Processor board and Power Module. In the OMAP35x EVM architecture, the Processor Module connector pin outs and functions are defined by the Main Board. The following sections describe about the various interfaces on the EVM main board.

2.1.1 LCD and Touch Screen

The EVM has a dual mode LCD module LS037V7DW01 from Sharp and is interfaced to the Display subsystem (DSS) of OMAP3530. The LCD panel supports 18-bit RGB format.

The QVGA/VGA selection (LCD_QVGA/nVGA) and LCD power (LCD_EnVDD) can be controlled through software using the GPIO signals. Refer GPIO Tables above.

The EVM supports Touch-screen using 4 wire resistive touch screen controller TSC2046. The primary interface between the touch-screen controller and the processor is McSPI1 interface. The TSC2046 also has the ability to interrupt the processor via the TS_nPEN_IRQ signal.

The TSC2046 is powered from the LCD_3v3 voltage rail, the same as the one that powers the LCD panel.

2.1.2 Audio Interface

The Audio section consists of one stereo Line IN and stereo Headset OUT through the audio codec on the TPS65950 device. The audio codec on the TPS65950 is controlled by internal registers that can be accessed through I2C interface (I2C1).

The McBSP2 interface of the OMAP3530 is connected to the TDM interface of the TPS65950 device to send and receive audio data (8-kHz up to a 48-kHz sampling rate) with 4 channels per frame and 16 or 32 bits per sample. The supported frequencies are 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, and 48 kHz.

The McBSP2 and McBSP3 are multiplexed between the Power module and the expansion connector. The McBSP2 (McBSP2_SEL) and McBSP3 (McBSP3_SEL) interface Multiplexers are controlled through SW1 switch on the Processor Module.

2.1.3 Video outputs

The EVM supports both Composite TV (CVBS) output and S-Video output on the main board. Either CVBS or S-Video is available from OMAP at a given point of time as both CVBS & S-Video are multiplexed on the same balls.

The digital output of the display controller is always a 24-bit RGB value based on a pixel request from the video encoder. The video encoder converts RGB video signals to conform to the NTSC/PAL standard analog video. The video encoder includes an integrated synchronization signal generator and a 2-channel video DAC with video amplifiers, data manager, luma stage, chroma stage, Macrovision™ insertion, modulator, and a control interface. The video encoder also provides the synchronization signals to the display controller: VSYNC, Active Video (AVID), and Field ID (FID).

2.1.4 Video Inputs

The OMP35x EVM has multiple video inputs options available on-board as well as from Expansion connector. The camera interface signals are routed by default to expansion connector. And the On board Video input options are gated through few GPIOs (from OMAP & TPS65950).

Though the EVM has multiple video input options, at a given point of time any one of the Video Input channels can be used. The OMP35x EVM has the below listed video input options:

- Video decoder (TVP5146PFP):
 - The TVP5146PFP video decoder supports A/D conversion of component RGB, composite video and S-Video into YCbCr. OMAP 35X EVM ISP processes this data and displays on the LCD

- An add-on Camera sensor shall be used in the front end to capture the image and process the data using OMAP 3530 ISP and displays on the LCD. The EVM supports the following parallel camera interfaces.
 - 26-Pin (13x2) Camera Box header, named Micron Connector.
 - Provision for on-board 3Mpixel camera module (LI-3MC02). Camera sensor is not part of EVM delivery.
 - 26-Pin (13x2) Receptacle, named LI/Image Connector. This is an optional connector and it will NOT be installed.
- Camera interface through expansion connector (Default).

There are three GPIOs and a 3-Pin header is used to select the video input options.

- **T2_GPIO2** – There are few T2/OMAP GPIOs used to enable/disable the on board interfaces (like on board Video Input, EHCI, etc) which are also routed to Expansion connector. Those GPIOs availability on Expansion / on-board is controlled through T2_GPIO2 (which is not available on Expansion connector).
- **T2_GPIO8 (nCAM_VD_EN_1V8)** – Selects the camera interface signals between Expansion connector and on-board video interface.
- **GPIO_157 (nCAM_VD_SEL_1V8)** - Selects the camera interface signals between Video Decoder and on board camera connectors
- **JP1**- Selects between Micron camera connector and on-board LI-3M02CM Module

Refer the below table to select the required video options.

T2_GPIO2	T2_GPIO8 (nCAM_VD_EN_1V8)	GPIO_157 (nCAM_VD_SEL_1V8)	JP1-Shunt Pos.	Selected Video Input
LOW	LOW	LOW	2-3	Micron Camera Connector (J32)
LOW	LOW	LOW	1-2	On board LI Module (LI-3M02CM)
LOW	LOW	HIGH	X	Video decoder (TVP5146)
LOW	HIGH	X	X	Expansion Connector
HIGH	X	X	X	Expansion connector. T2_GPIO8 & GPIO_157 also available on Expansion connector. (Default case)

Table 5: Video Input selection

2.1.5 Ethernet Interface

The OMAP35x EVM supports single 10/100 Mbps Ethernet interface using an external MAC+PHY controller, LAN9220 from SMSC. The LAN9220 controller interfaced to the OMAP processor via the General Purpose Memory Controller (GPMC).

The GPMC CS5 space of the OMAP processor is used to address the MAC controller. A serial EEPROM is provided for the plug-n-play configuration of LAN9220. The serial EEPROM is optional and can be used for configuring the MAC address on power up.

2.1.5.1 Programming the EEPROM

The MAC ID and board revision number with board serial number is stored in EEPROM. The MAC ID is stored at the address 0xb60800b4 and board information is stored at the address 0xb60800bb. These MAC ID and board information is factory programmed. In case of accidental erase of the EEPROM, the user can re-program the EEPROM using the following procedure:

NOTE: The below commands are available as a part of ITBOK.

MAC Write:

The MAC address can be written to EEPROM using the following u-boot command at u-boot prompt

```
mac write <MAC-ADDRESS>
```

Example:

```
mac write 00:50:c2:7e:8d:09
```

MAC Read:

The MAC address can be read from EEPROM using the following u-boot command at u-boot prompt

```
mac read
```

Example:

```
mac read
```

Board Information Write:

The board information can be written to EEPROM using the following u-boot command at u-boot prompt

```
board_info write <REVISION ID:SERIAL NUMBER>
```

Example:

```
board_info write REV-E:05:0027
```

Board Information Read:

The board information can be read from EEPROM using the following u-boot command at u-boot prompt

```
board_info read
```

Example:

```
board_info read
```

2.1.6 SD/MMC Memory Card Interface

The EVM supports two SD/MMC interfaces

- SD/MMC1 with 1.8V/3.0 V support
- SD/MMC2 with 1.8V support only

SD/MMC1 interface is routed to a SD/MMC slot on the main board. SD/MMC2 interface is routed to the expansion connector for future expansion.

The Card detect signal of SD/MMC card is routed to the card detect GPIO_0 of TPS65950. The power supply (VMMC1) for the SD/MMC interface is supplied by TPS65950 device. The TPS65950 device senses the card insertion using the card detect signal and enables the power to the SD/MMC card in the slot. The MMC1_WP is controlled by GMPC_WAIT1/GPIO_63 signal from the Processor.

2.1.7 High Speed USB OTG Interface

High Speed USB OTG interface is supported using an onboard USB transceiver ISP1507 from NXP. The transceiver is interfaced to the ULPI interface of the processor.

The ISP1507 is an 8-bit bidirectional UTMI+ Low Pin Interface (ULPI) transceiver, which provides a Hi-Speed Universal Serial Bus (USB) analog front-end solution to

Application-Specific Integrated Circuits to implement as a Hi-Speed USB host, peripheral or OTG device.

Resistor selectable option is provided on the Main board to use TPS65950 transceiver; however by default these resistors are NOT populated.

2.1.8 High Speed USB Host Interface

High Speed USB HOST interface is supported through an HSUSB transceiver, USB3320 from SMSC. The transceiver is interfaced to the USB2 (EHCI) port of the processor.

The USB3320 is an 8-bit bidirectional UTMI + Low Pin Interface (ULPI) transceiver, which provides a Hi-Speed Universal Serial Bus (USB) analog front-end solution to Application-Specific Integrated Circuits to implement as a Hi-Speed USB host.

High speed USB Host interface signals (USB2 EHCI) are shared between expansion connector and on board HSUSB Host transceiver. OMAP's USB Host (USB2) interface signals are routed by default to expansion connector. And the On-board HSUSB Host Transceiver has to be enabled through couple of GPIOs.

- **T2_GPIO2** – There are few T2/OMAP GPIOs used to enable on-board interfaces/features (Like on-board EHCI) that also go to Expansion connector. Such GPIOs are also routed to Expansion connectors; so it is gated through a T2_GPIO2 (does not go to Expansion connector).
- **GPIO_61 (nUSB2_EN_1V8)** – Selects on-board EHCI (USB2) interface.

Refer the below table to select between on-board EHCI and Expansion Conn.

T2_GPIO_2	GPIO_61 (nUSB2_EN_1V8)	EHCI signals
LOW	LOW	On board EHCI (USB2)
LOW	HIGH	EHCI (USB2) signals on Expansion Connector
HIGH	X	Expansion connector. GPIO_61 is also available on the Expansion connector. (Default case)

Table 6: On-board EHCI selection

2.1.9 UART Interface

The OMAP processor supports three UART interfaces. The UART interfaces 1 and 2 are multiplexed on a single RS232 port P20. Selection of the UART interface can

be done using appropriate settings on jumper J8. UART 3 is available on the connector P21.

- **UART 1:** This interface provides serial communication through Serial Port connector P20 on EVM Main Board. (Requires proper jumper selection on J8 – Install a Shunt between J8-1 & J8-2).
- **UART 2:** This interface provides serial communication through Serial Port connector P20 on EVM Main Board (Requires proper jumper selection on J8 – Install a Shunt between J8-2 & J8-3).
- **UART 3:** This interface is used for peripheral booting of the OMAP processor. (Connector P21 on EVM Main Board). UART3 can also be disabled and made available to the expansion connectors using the SW1-3 switch setting on OMAP Processor module.
 - SW1-3 – OFF → UART3 on RS-232 connector (P21)
 - SW1-3 – ON → UART3 on Expansion connector
 - UART3 communication port is supported with flow control. However by default it is not enabled. To enable the Flow controlled communication refer the below table

T2_GPIO_2	GPIO_55 (nFULL_MODEM_EN_1V8)	UART3 Port – Flow control
LOW	LOW	UART3 Port Supported with flow control on P21
LOW	HIGH	UART3 Port Supported without flow control. UART3_CTS & UART3_RTS signals are available on Expansion connector
HIGH	X	Expansion connector. GPIO_55 is also available on the Expansion connector. (Default case)

Table 7: Flow control Support on UART3

2.1.10 I2C Interface

The OMAP processor supports four I2C interfaces. The I2C interface connectivity on the EVM is given below

I2C #1 – Connected to TPS65950 device General Purpose register access

I2C #2 – Routed to the following interface

Expansion connectors for future use

Micron Camera connector

Option for on-board camera module (LI-3M02CM)

I2C #3 – Routed to the following interface

Expansion connectors for future use

On-board Video decoder (TVP5146)

I2C #4 – Connected to TPS65950 device for Smart Reflex interface

2.1.11 Key Pad

The EVM main board has 15 keys arranged in a matrix and one user key. The keypad row and column signals are connected to the TPS65950 device keypad interface.

The Keypad mapping on the EVM main board is given below:

Row Column	R0	R1	R2	R3
C0	S18	S15	S12	S9
C1	S6	S17	S14	S11
C2	S8	S5	S16	S13
C3	Not Used	S10	S7	S4

Table 8: Keypad mapping

2.1.12 Debug Interface

The EVM supports two debug interfaces namely: JTAG & Embedded Trace Macrocell interface. Debug connectors are used for test, debug, execute, trace and download the program from IDE to target unit. There are two connectors on the board

- 14pin JTAG connector
- 38 pin ETM connector

2.1.13 Expansion Connectors

The EVM Main board has dual 120 positions General Purpose expansion connectors through which Camera, Display, GPMC, UART and several other interfaces are brought out for future enhancement.

The end user can build their own application specific daughter-card to meet their application specific requirements.

The interfaces supported on the expansion connector are listed below

- GPMC bus with chip select spaces GPMC_CS0, GPMC_CS1, GPMC_CS3, GPMC_CS4, GPMC_CS6 and GPMC_CS7.
- 12 bit Camera Parallel interface with Camera control signals
- I2C 2 and 3 interfaces
- SD/MMC 1 and 2 interfaces
- McSPI 1 and 2 interfaces
- McBSP 1, McBSP 2 and McBSP3 interfaces
- UART 1, 2 and 3 interfaces
- ETM debug interface
- Power, reset, clock and system control signals
- 6 ADC Channels from TPS65950
- PCM Bluetooth Interface from TPS65950

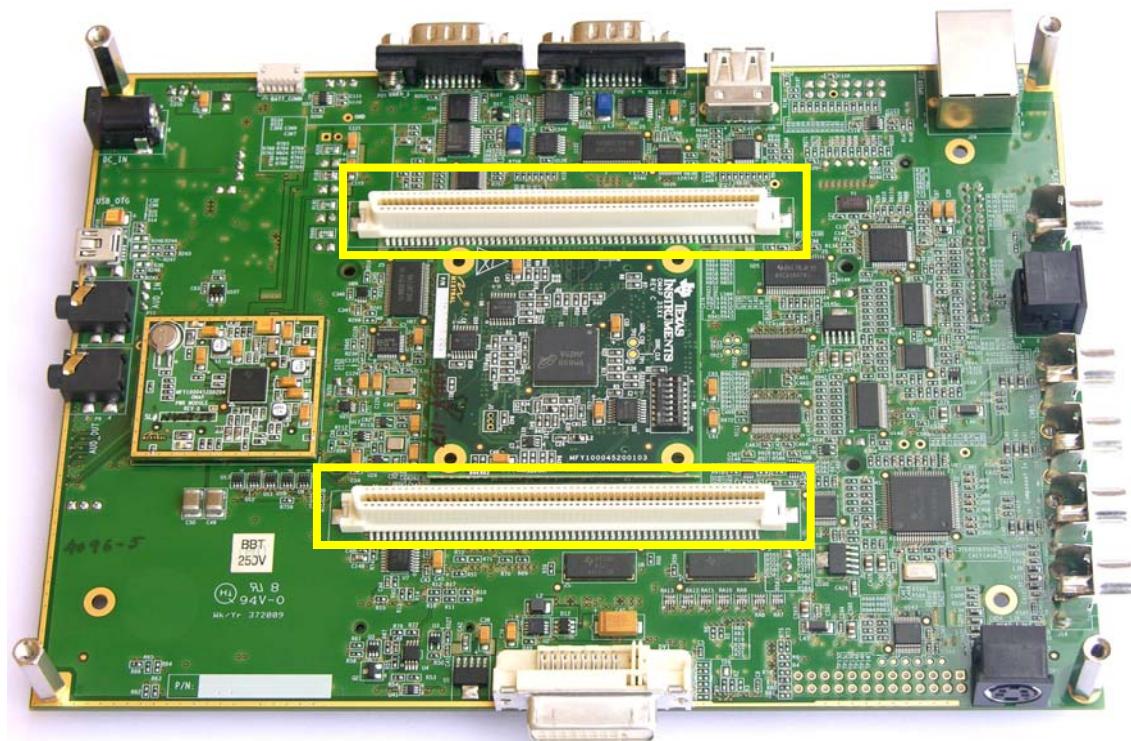


Figure 3: Expansion Connectors

2.1.14 Clock and LED

The EVM Main Board provides following clocks,

- 26MHz Clock for TPS65950 High Frequency HFCLKIN
- 25MHz Clock for Ethernet controller
- 26MHz Clock for ISP1507 USB transceiver
- 24MHz Clock for the on-board LI camera module

The following status LED's are present on the Main Board

- D1 – To Indicate MMC1 3V/MMC1 1.8V Enabled
- LD1 – To indicate Full Duplex mode for Ethernet

- LD8 – To indicate VBAT presence
- LD9 – To indicate DC Input's presence
- LD19 – To indicate Processor activity

Except LD19, all the LED's will turn "ON" when associated power rails or signals are active.

2.1.15 Power

The main power input for the EVM system is provided using an external 5V universal adaptor or from an external Lithium-Ion battery supply (Li-ion battery is not part of the EVM Kit). The LCD 3.3V and other voltages required for the main board are derived using on board regulators on the main board.

The Power module takes care of the generation and distribution of various power requirements of the OMAP Processor module listed below.

- **OMAP I/O supply** (1.8V, 600mA)
- OMAP core supply
 - VDD1 (1.2V, 1100mA) [used for OMAP mpu_iva]
 - VDD2 (1.2V, 600mA) [used for OMAP core]
- **USB VBUS** (4.8V, 100mA)
- **VAUX Supplies**
 - VAUX1 (2.5V, 2.8V, 3.0V, 200mA)
 - VAUX2 (1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 100mA)
 - VAUX3 (1.5V, 1.8V, 2.5V, 2.8V, 200mA)
 - VAUX4 (0.7V, 1.0V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 100mA)
- **OMAP Video DAC supply** (1.8V, 65mA)
- **PLL Supply**
 - VPPLL1 (1.3V, 40mA)
 - VPPLL2 (1.3V, 60mA)
- **MMC1 supply** (1.8V, 3.0V, 220mA) [used on MMC1 at 1.85V or 3.0V]
- **MMC2 supply** (1.85V, 100mA)

2.2 OMAP Processor Module

OMAP Processor Module consists of OMAP 3530 Processor with PoP memory (MT29C2G48MAKLCJ1-6 IT) micron Micron

The Processor Module can be plugged into the EVM main board on the board-to-board connectors shown below.

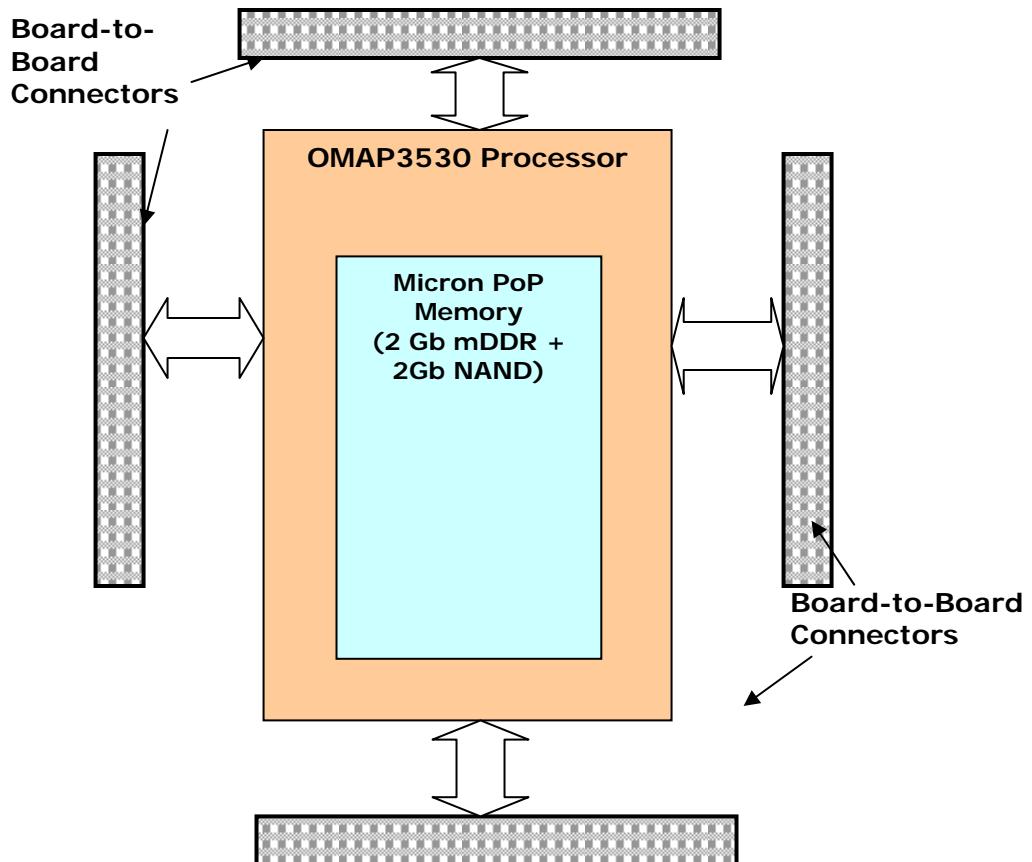


Figure 4: OMAP Processor module connector layout



Avoid frequent removal and insertion of the OMAP processor module on the OMAP 35x EVM. This may reduce the life span of the board-to-board connectors.

2.2.1 PoP Memory Interface

The OMAP 3530 processor supports memory stacking using a package-on-package implementation (PoP). The GPMC and SDRC interfaces of the OMAP processor are brought to the top of the die and the PoP memory can be directly mounted on top of the OMAP 3530 processor BGA device.

The Figures given below show the concept of the PoP solution.

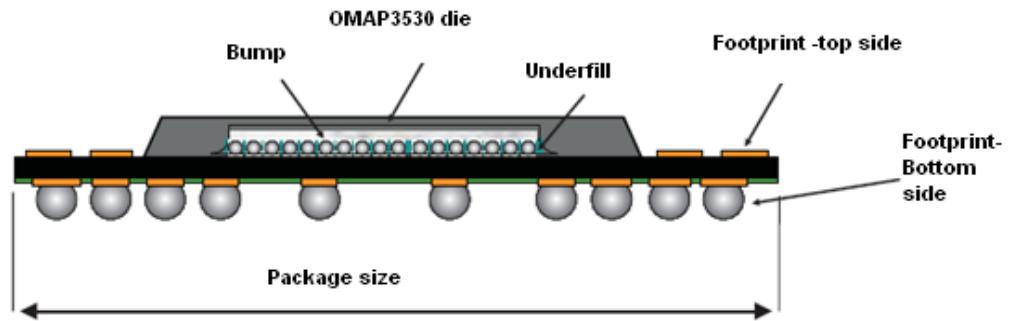


Figure 5: **OMAP PoP Concept**

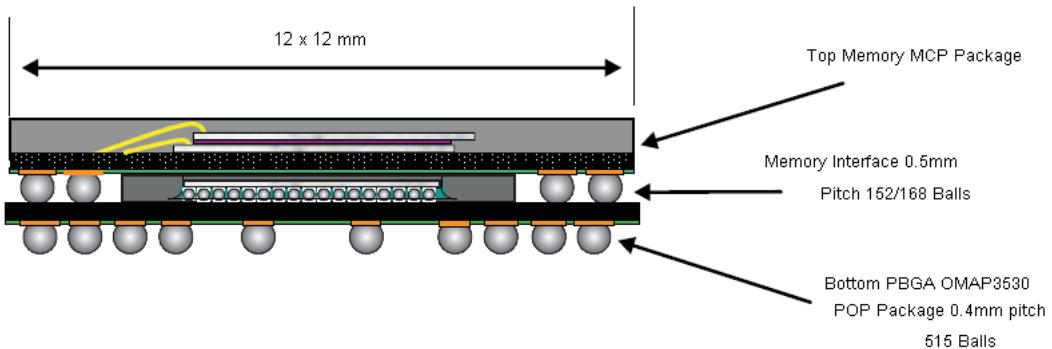


Figure 6: **PoP Memory Stacked on OMAP**

2.2.2 Flash Interface

EVM supports Micron PoP memory with 256 MBytes NAND flash memory mapped into the GPMC CS0 space.

The NAND flash memory is used primarily as a boot device and to create file system on the OMAP EVM. The GPMC CS0 is configured for 16-bit wide access on the OMAP35x EVM.

2.2.3 Mobile DDR SDRAM

64Mx32 bit Mobile DDR SDRAM memory is interfaced to the SDRC CS0 space of the OMAP Processor. The internal DDR controller uses a PLL to control the DDR memory timing. Memory refresh for DDR is handled automatically by the OMAP internal DDR controller.

2.2.4 Multiplexing on Interfaces:

To support additional interfaces with the limited pin-out available on expansion connector, the UART3, McBSP2/3, interfaces are multiplexed on the processor board using multiplexers.

The McBSP2 and McBSP3 are multiplexed between the Power module and the expansion connector on EVM main board.

The UART 3 interface is multiplexed between the EVM main board connector P21 and expansion connector.

These multiplexer selections are manually controlled through switch SW1 configuration on the OMAP processor module.

2.3 Power Module

The Power Module has TPS65950 Power and Audio companion device, which is responsible for OMAP power management, clock and reset generation. This can support multiple power supply designs in the EVM architecture. Communication to the OMAP Processor is via the High Speed I2C interface for voltage scaling, configuration, and ON/OFF control.

In addition to the power management functions, the TPS65950 handles:

- HS USB Transceiver (optional)
- Battery charger
- Keypad interface

- Audio Codec
- Real Time Clock
- ADC Inputs

There are three board-to-board connectors that are used to mount the Power Module onto the EVM main board.



Avoid frequent removal and insertion of the Power module on the OMAP 35x EVM. This may reduce the life span of the board-to-board connectors.

2.3.1 Clock and LED

The Power module clock signals are listed below:

- TPS65950 26 MHz HFCLKOUT provides the system clock input for OMAP processor
- TPS65950 32KHz_CLKOUT provides the low frequency clock input for OMAP processor
- The Power Module has a 32 KHz Crystal input onboard and a 26 MHz clock input supplied from the EVM main board.

The following status LEDs are present on the Power module:

- D1 – LED_B - VBAT Presence LED

This status LED will turn “ON” when VBAT is active.

Chapter 3

Physical Description

3. Physical Description

This chapter describes the physical layout of the OMAP 35x EVM.

3.1 OMAP 35x EVM layout

The OMAP35x EVM comprises of three different PCBs namely:

- Main board
 - 203.2 x 143.51 mm
 - 8 layer PCB
- Processor Module
 - 52.07 mm x 53.34 mm
 - 8 layer PCB
- Power Module
 - 37.47mm x 32.39mm
 - 6 layer PCB

3.1.1 OMAP 35x EVM Top View

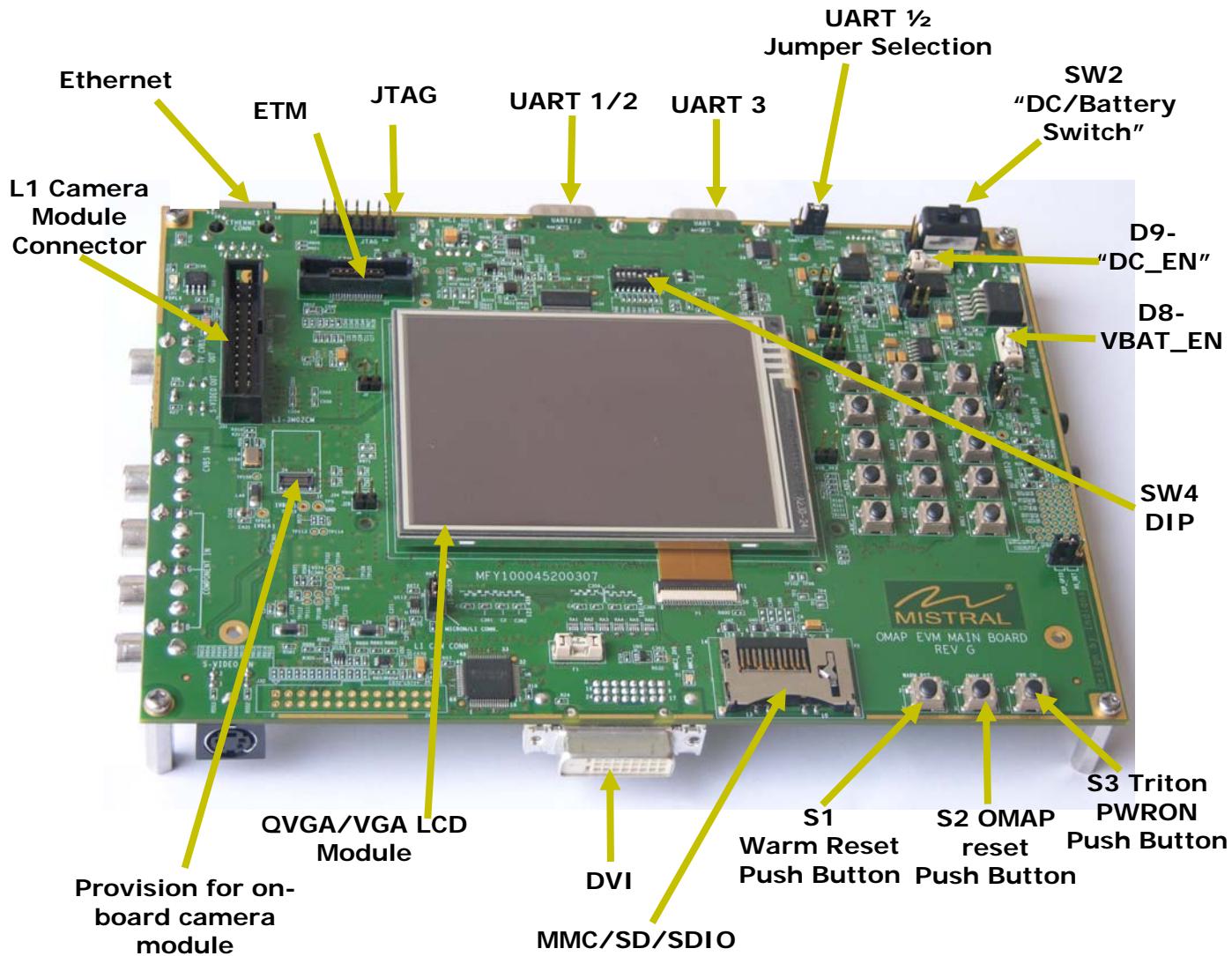


Figure 7: OMAP 35x EVM Top View

3.1.2 OMAP 35x EVM Bottom View

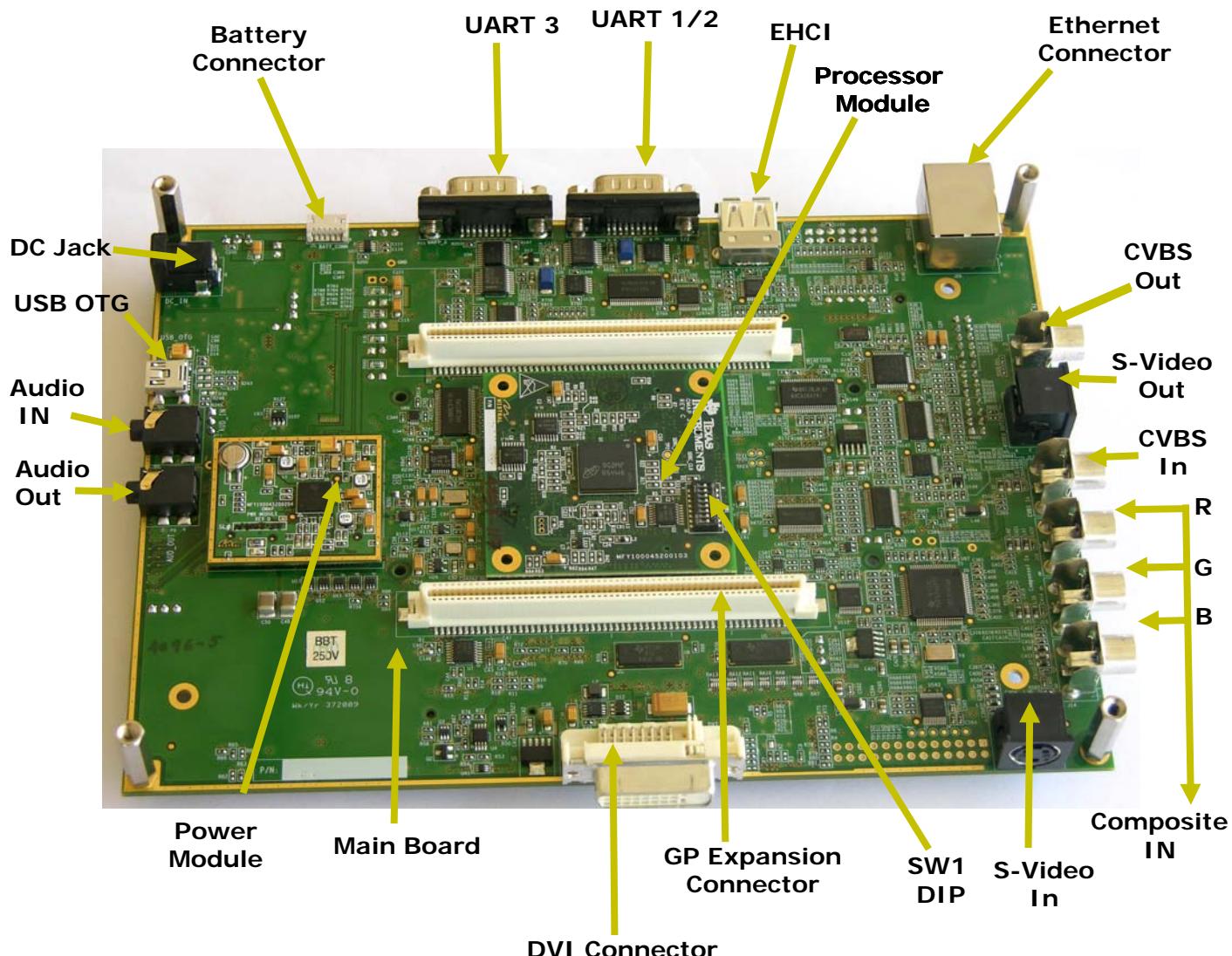


Figure 8: OMAP 35x EVM Bottom View

3.1.3 OMAP Processor Module Top View

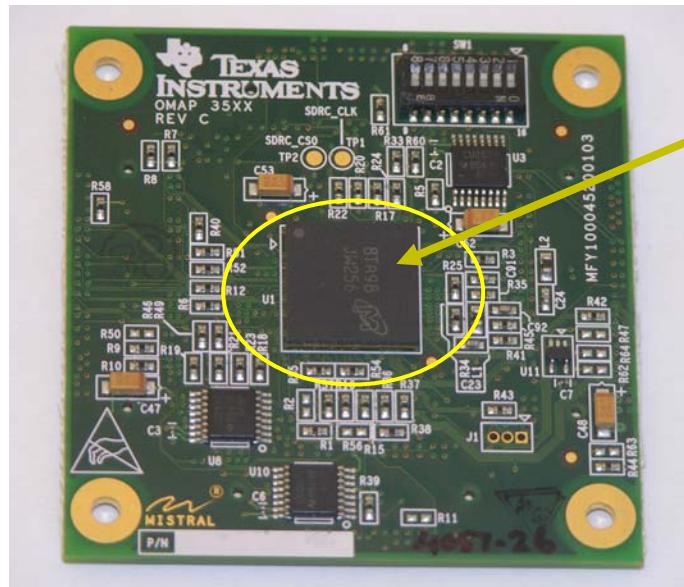


Figure 9: OMAP Processor Module Top View

OMAP 3530 Processor with Micron PoP memory on Top

3.1.4 OMAP Processor Module Bottom View

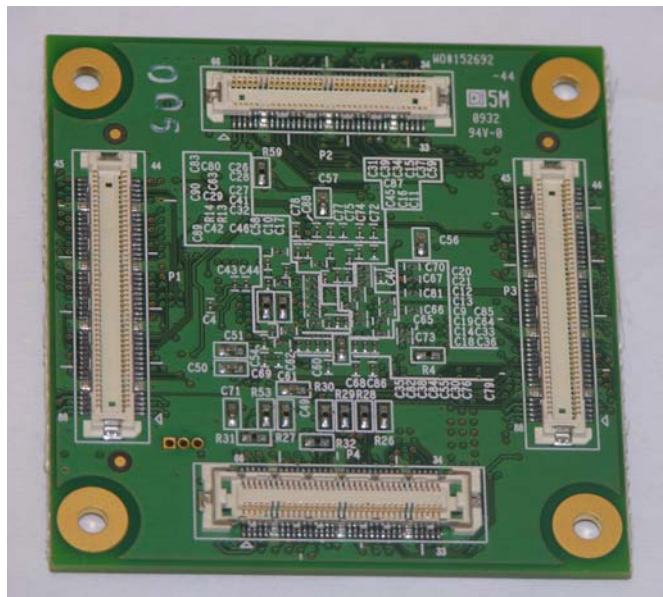


Figure 10: OMAP Processor Module Bottom View

3.1.5 Power Module Top View

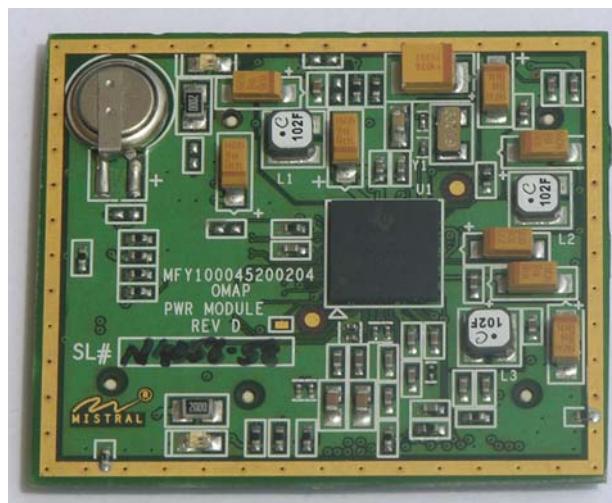


Figure 11: Power Module Top View

3.1.6 Power Module Bottom View

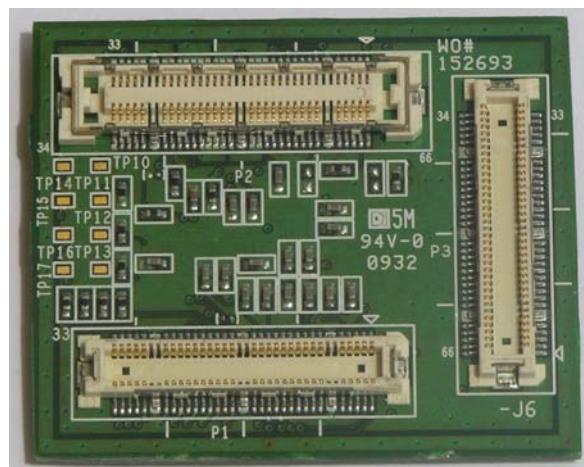


Figure 12: Power Module Bottom View

3.2 Connectors

The OMAP35x EVM has several connectors and option jumpers to control and provide connections to various peripherals. These connectors, switches, fuses and jumpers are listed below;

Connectors	Type	Location	Function
P1	51	EVM Main board	LCD
P2	28	EVM Main board	SD/MMC/SDIO
P3	19 X 2	EVM Main board	ETM Trace
P4	7 X 2	EVM Main board	JTAG
P6	4	EVM Main board	TV
P7, P18	60 X 2	EVM Main board	Expansion connector
P8, P12, P13, P17	33 X 2	OMAP Processor Module	Board to Board connectors
P9	5	EVM Main board	Audio Out
P10, P15 & J21	33 X 2	Power Module	Board to Board connectors
P11	5	EVM Main board	Audio IN
P14	5	EVM Main board	S- Video
P16	9	EVM Main board	USB
P19	3	EVM Main board	DC JACK +5V Input
P20	11	EVM Main board	UART 1/2
P21	11	EVM Main board	UART 3
P22	3	EVM Main board	Battery Charging Circuit
J10	12	EVM Main board	Ethernet
J11	6	EVM Main board	Battery Connector
J13	3	EVM Main board	Composite Video I/P Connector
J14	3	EVM Main board	Component Video In Blue connector
J15	3	EVM Main board	Component Video In Green connector
J16	3	EVM Main board	Component Video In Red connector
J18	4	EVM Main board	USB Host connector
J13	13x2	EVM Main board	Micron Camera Connector
J32	13x2	EVM Main board	LI/Image Connector
J34	12x2	EVM Main board	LI-3M02CM Connector
J22	3x1	EVM Main board	T2_GPIO1 selection Header
J23	3x1	EVM Main board	USB OTG VBUS current Selection Header

JP1	3x1	EVM Main board	Camera Interface selection Header
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Table 9: EVM Connectors

3.2.1 LCD Connector

The P1 connector is a 51 pin FFC SMD connector for LCD interface. It is located on the top of the Board. This connector has cable lock option to hold the LCD FFC cable. The connector pin out details is given below.

**Figure 13:** LCD Connector

Pin Number	Signal	Pin Number	Signal
1	LED+	2	NC1
3	LED-	4	NC2
5	XR	6	YD
7	XL	8	YU
9	GND	10	LCD RESB
11	GND	12	LCD MO
13	LCD UD	14	LCD LR
15	INI	16	LCD DEN
17	GND	18	LCD VSYNC
19	GND	20	HSYNC
21	GND	22	LCD CLKIN
23	GND	24	VCC
25	VCC	26	VCC
27	GND	28	DATA5
29	DATA4	30	DATA3
31	DATA2	32	DATA1
33	DATA0	34	GND
35	DATA11	36	DATA10
37	DATA9	38	DATA8
39	DATA7	40	DATA6
41	GND	42	DATA17
43	DATA16	44	DATA15
45	DATA14	46	DATA13
47	DATA12	48, 51	GND
49	LCD SMPSYNC	50	LCD SMPDATA

Table 10: LCD Connector

3.2.2 SD / MMC / SDIO

The P2 MMC/SD connector is located on top side of the board and is used to provide an interface to a MMC/SD/SDIO card. The pin-out for the P2 connector is shown in the table below.

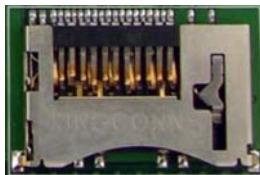


Figure 14: SD/MMC Connector

Pin Number	Signal
1, 16	DATA3
2, 17	CMD
5, 20	CLK
7, 22	DATA0
8, 23	DATA1
9 , 24	DATA2
10	DATA4
11	DATA5
12	DATA6
13	DATA7
14	WP
15	CD
3, 6, 18, 21, 27, 28	GND
4, 19	VCC
25, 26	NC

Table 11: SD/MMC Connector

3.2.3 JTAG & ETM Connector

The OMAP35x EVM main board supports a 38 pin (5 GND pins) connector for embedded trace macro cell debug interface and 14 pin JTAG connector.

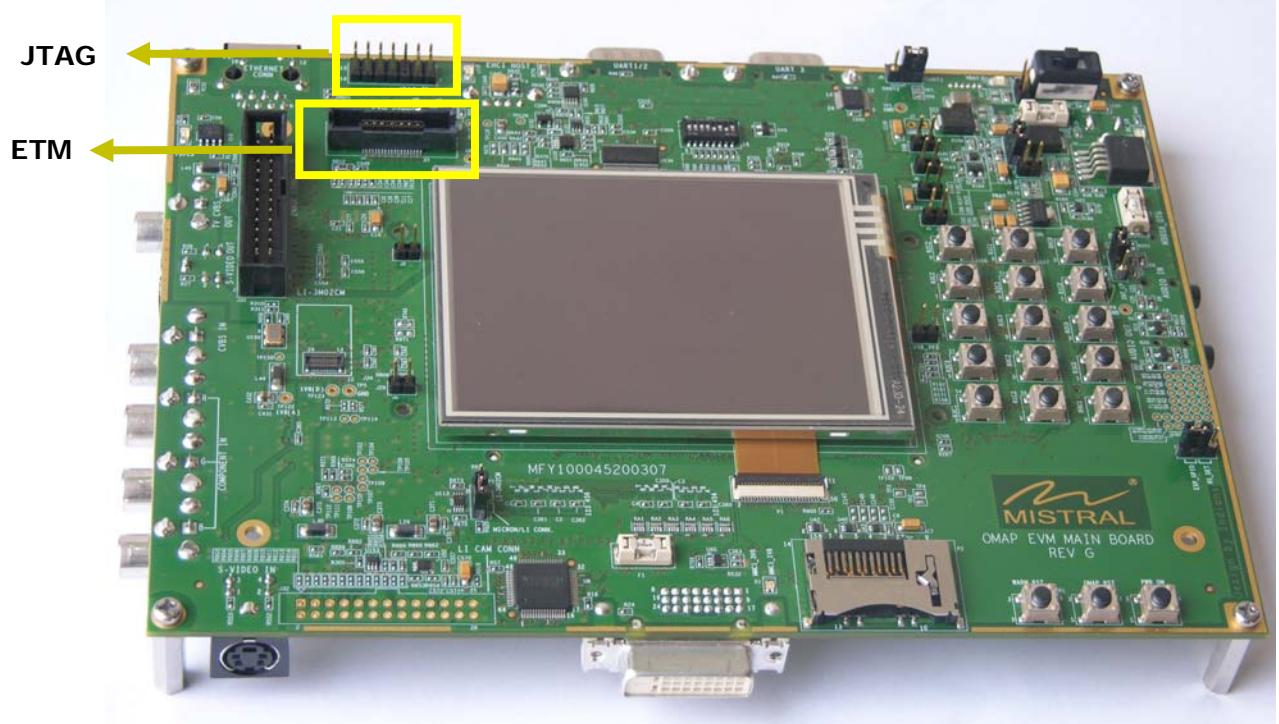


Figure 15: JTAG & ETM Connector

The pin out details of ETM connector is as below:

Pin Number	Signal	Pin Number	Signal
1	NC	2	HSI2C_SCL
3	GND	4	HSI2C_SDA
5	ETM_P05	6	ETK_C1
7	DBREQ	8	ETM_P08
9	ETM_P09	10	ETM_P10
11	JTAG_TDO	12	ETM_P12
13	JTAG_RTCK	14	ETM_P14
15	JTAG_TCK	16	ETK_D7
17	JTAG_TMS	18	ETK_D6
19	JTAG_TDI	20	ETK_D5
21	JTAG_TRST	22	ETK_D4
23	ETK_D15	24	ETK_D3
25	ETK_D14	26	ETK_D2
27	ETK_D13	28	ETK_D1
29	ETK_D12	30	GND
31	ETK_D11	32	GND

33	ETK_D10	34	ETM_P34
35	ETK_D9	36	ETK_C2
37	ETK_D8	38	ETK_D0
39, 40, 41, 42, 43	GND		

Table 12: ETM Connector

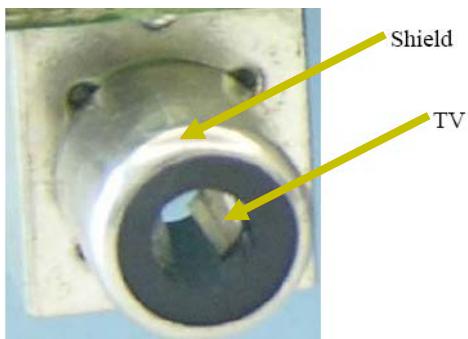
The pin out details of JTAG connector is as below:

Pin Number	Signal
1	R_JTAG_HDR_TMS
2	R_JTAG_HDR_TRST
3	R_JTAG_HDR_TDI
5	VDD_JTAG
6	Not Connected
7	R_JTAG_HDR_TDO
9	R_JTAG_HDR_RTCK
11	R_JTAG_HDR_TCK
4, 8, 10,12	GND
13	R_JTAG_HDR_nEMU0
14	R_JTAG_HDR_nEMU1

Table 13: JTAG Connector

3.2.4 CVBS TV out

The pin out details of the CVBS TV out RCA connector is as below

**Figure 16: CVBS TV out Connector**

3.2.5 S- Video

S-Video Connector P14 is a 4-pin mini din connector. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

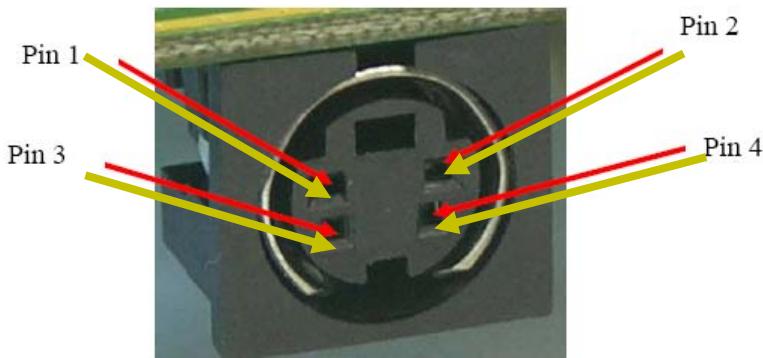


Figure 17: S-Video Connector

Pin No	Signal
1, 2	GND
3	Video Y (Luma)
4	Video C (Chroma)

Table 14: S-Video Connector

3.2.6 Expansion Connector

The pin-out details of the EVM expansion connector P7 are as below:

Pin No.	Signal	Pin No.	Signal
A1	VBAT	B1	VBAT
A2	VBAT	B2	VBAT
A3	VIO_1V8	B3	VIO_1V8
A4	VIO_1V8	B4	VIO_1V8
A5	T2_REGEN	B5	T2_LEDSYNC
A6	T2_nRESPWARM	B6	T2_GPIO.1_EXP
A7	T2_START.ADC	B7	EXP_T2_GPIO.8
A8	T2_PCM_BTDX	B8	T2_ADCINO
A9	T2_PCM_BTDR	B9	T2_ADCIN2
A10	EXP_SPI2_CLK	B10	T2_ADCIN3
A11	EXP_SPI2_SIMO	B11	T2_ADCIN4
A12	EXP_SPI2_SOMI	B12	T2_ADCIN5

A13	EXP_SPI2_nCS0	B13	T2_ADCIN6
A14	SYS_CLKREQ	B14	DSS_D0
A15	EXP_MCSPI2_CS1	B15	DSS_D1
A16	McBSP1_CLKR	B16	DSS_D2
A17	EXP_McBSP1_FSR	B17	DSS_D3
A18	McBSP1_RX	B18	DSS_D4
A19	McBSP1_DR	B19	DSS_D5
A20	McBSP1_FSX	B20	DSS_D6
A21	McBSP1_CLKX	B21	DSS_D7
A22	UART1_TX	B22	DSS_D8
A23	UART1_RX	B23	DSS_D9
A24	UART1_CTS	B24	DSS_D10
A25	UART1_RTS	B25	DSS_D11
A26	EXP_MCBSP3_CLKX	B26	DSS_D12
A27	EXP_MCBSP3_DR	B27	DSS_D13
A28	EXP_MCBSP3_RX	B28	DSS_D14
A29	EXP_MCBSP3_FSX	B29	DSS_D15
A30	I2C2_SDA	B30	DSS_D16
A31	I2C2_SCL	B31	DSS_D17
A32	EXP_UART3_RX	B32	DSS_D18
A33	T2_ADCIN7	B33	DSS_D19
A34	EXP_UART3_RTS	B34	DSS_D20
A35	EXP_UART3_CTS	B35	DSS_D21
A36	UART2_CTS	B36	DSS_D22
A37	UART2_RTS	B37	DSS_D23
A38	UART2_TX	B38	DSS_ACBIAS
A39	UART2_RX	B39	DSS_PCLK
A40	MMC2_CLKO	B40	DSS_VSYNC
A41	MMC2_CMD	B41	DSS_HSYNC
A42	MMC2_DAT7	B42	MMC1_CLKO
A43	MMC2_DAT6	B43	MMC1_CMD
A44	MMC2_DAT5	B44	MMC1_DAT7
A45	MMC2_DAT4	B45	MMC1_DAT6
A46	MMC2_DAT3	B46	MMC1_DAT5
A47	MMC2_DAT2	B47	MMC1_DAT4
A48	MMC2_DAT1	B48	MMC1_DAT3
A49	MMC2_DAT0	B49	MMC1_DAT2
A50	SYSEN	B50	MMC1_DAT1
A51	EXP_UART3_TX	B51	MMC1_DAT0
A52	REFCLK_EXP	B52	SYS_CLKOUT2
A53	32KHz_EXP	B53	SYS_CLKOUT1
A54	GND	B54	GND
A55	GND	B55	GND
A56	GND	B56	GND
A57	GND	B57	GND
A58	GND	B58	GND
A59	GND	B59	GND
A60	GND	B60	GND

Table 15: Expansion Connector P7

The pin-out details of the EVM expansion connector P18 are as below:

Pin No.	Signal Name	Pin No.	Signal Name
A1	VBAT	B1	VBAT
A2	VAUX1_OUT	B2	VAUX2_OUT
A3	VMMC2_OUT	B3	VAUX4_OUT
A4	VSIM	B4	GPMC_nCS6
A5	SYS_nRESPWRON	B5	NC
A6	GPMC_WAIT0	B6	GPMC_nWP
A7	EXP_GPMC_nBE1	B7	GPMC_nBEO
A8	GPMC_nADV	B8	GPMC_nOE
A9	GPMC_nWE	B9	GPMC_CLK
A10	EXP_GPMC_nCS7	B10	EXP_GPMC_nCS4
A11	GPMC_nCS1	B11	GPMC_NCS0
A12	GPMC_AD1	B12	GPMC_ADO
A13	GPMC_AD3	B13	GPMC_AD2
A14	GPMC_AD5	B14	GPMC_AD4
A15	GPMC_AD7	B15	GPMC_AD6
A16	GPMC_AD9	B16	GPMC_AD8
A17	GPMC_AD11	B17	GPMC_AD10
A18	GPMC_AD13	B18	GPMC_AD12
A19	GPMC_AD15	B19	GPMC_AD14
A20	GPMC_A2	B20	GPMC_A1
A21	GPMC_A4	B21	GPMC_A3
A22	GPMC_A6	B22	GPMC_A5
A23	GPMC_A8	B23	GPMC_A7
A24	GPMC_A10	B24	GPMC_A9
A25	EXP_CAM_FLD	B25	I2C3_SCL
A26	EXP_VDIN_CAM_STROBE	B26	I2C3_SDA
A27	EXP_CAM_WEN	B27	NC(SYSBOOT6???)

Pin No.	Signal Name	Pin No.	Signal Name
A28	GPMC_nCS3	B28	SYSBOOT5
A29	EXP_VDIN_CAM_XCLKB	B29	SYSBOOT4
A30	EXP_VDIN_CAM_XCLKA	B30	SYSBOOT3
A31	EXP_CAM_VS	B31	SYSBOOT2
A32	EXP_CAM_HS	B32	SYSBOOT1
A33	EXP_CAM_LCLK	B33	SYSBOOT0
A34	EXP_CAM_D0	B34	ETK_CLK
A35	EXP_CAM_D1	B35	ETK_CTL
A36	EXP_CAM_D2	B36	ETK_D0
A37	EXP_CAM_D3	B37	ETK_D1
A38	EXP_CAM_D4	B38	ETK_D2
A39	EXP_CAM_D5	B39	ETK_D3
A40	EXP_CAM_D6	B40	ETK_D4
A41	EXP_CAM_D7	B41	
A42	EXP_CAM_D8	B42	ETK_D6
A43	EXP_CAM_D9	B43	EXP_ETK_D7
A44	EXP_CAM_D10	B44	EXP_ETK_D8
A45	EXP_CAM_D11	B45	EXP_ETK_D9
A46	GPMC_WAIT3	B46	EXP_ETK_D10

Pin No.	Signal Name	Pin No.	Signal Name
A47	MCSPI1_CS3	B47	EXP_ETK_D11
A48	EXP_MCBSP2_FSX	B48	EXP_ETK_D12
A49	EXP_MCBSP2_CLKX	B49	EXP_ETK_D13
A50	EXP_MCBSP2_DR	B50	EXP_ETK_D14
A51	EXP_MCBSP2_DX	B51	EXP_ETK_D15
A52	T2_McBSP_CLKS	B52	T2_CLKEN2
A53	CLK_REQ_OD	B53	T2_CLKEN
A54	GND	B54	GND
A55	GND	B55	GND
A56	GND	B56	GND
A57	GND	B57	GND
A58	GND	B58	GND
A59	GND	B59	GND
A60	GND	B60	GND

Table 16: Expansion Connector P18

3.3 Micron Camera Module Connector

The Micron Camera connector J31 is a 13x2 Box Header. The table lists the signals

Pin No.	Signal Name	Pin No.	Signal Name
1	MN_CAM_D2	2	MN_CAM_D3
3	MN_CAM_D4	4	MN_CAM_D5
5	MN_CAM_D6	6	MN_CAM_D7
7	MN_CAM_D8	8	MN_CAM_D9
9	MN_CAM_D0	10	MN_CAM_D1
11	GND	12	GND
13	MN_CAM_HS	14	NC
15	NC	16	NC
17	MN_CAM_VS	18	CAM_I2C_SDA_3V3
19	CAM_I2C_SCL_3V3	20	NC
21	VCAM	22	VCAM
23	EXP_CAM_D5	24	GND
25	MN_CAM_PCLK	26	NC

3.4 LI/Image Connector

The LI/Image connector J32 (not installed on board) is a 13x2 Receptacle. The table lists the signals

Pin No.	Signal Name	Pin No.	Signal Name
1	MN_CAM_D2	2	MN_CAM_D3

3	MN_CAM_D4	4	MN_CAM_D5
5	MN_CAM_D6	6	MN_CAM_D7
7	MN_CAM_D8	8	MN_CAM_D9
9	MN_CAM_D0	10	MN_CAM_D1
11	GND	12	GND
13	MN_CAM_HS	14	NC
15	NC	16	CAM_nRESET_3V3
17	MN_CAM_VS	18	CAM_I2C_SDA_3V3
19	CAM_I2C_SCL_3V3	20	NC
21	VCAM	22	VCAM
23	EXP_CAM_D5	24	GND
25	MN_CAM_PCLK	26	NC

3.5 LI-3M02CM Module Connector

The LI-3M02CM Module connector J34 is a 12x2 fine pitch SMD connector. The table lists the signals

Pin No.	Signal Name	Pin No.	Signal Name
1	LI_CAM_D0	24	LI_FLASH
2	LI_CAM_D1	23	LI_CAM_GPIO0
3	LI_CAM_D2	22	SADDR
4	LI_CAM_D3	21	LI_CAM_STBY
5	LI_CAM_D4	20	CAM_nRESET_2V8
6	LI_CAM_D5	19	CAM_I2C_SCL_2V8
7	LI_CAM_D6	18	CAM_I2C_SDA_2V8
8	LI_CAM_D7	17	GND
9	LI_CAM_PCLK	16	LI_CAM_XCLKA
10	V_1V8_CAMERA	15	LI_CAM_HS
11	2.8VD_CAM	14	LI_CAM_VS
12	CAM_AGND	13	GND

3.5.1 Audio Connectors

The P9 and P11 connector is a 3.5 mm. stereo jack connector. This connector is located on the bottom side of the board. A view of the connector from the card edge is shown in the figure below.

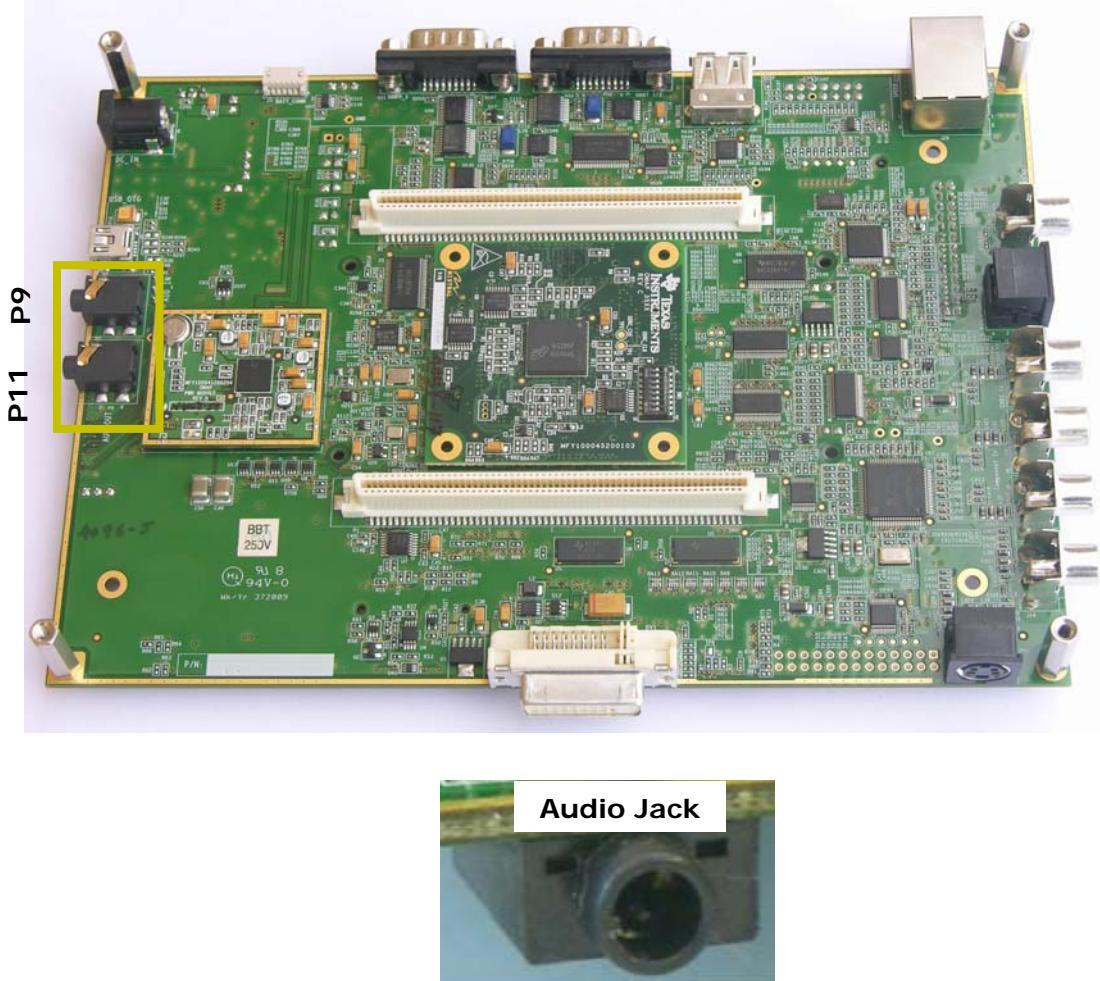


Figure 18: Audio Jack

The signals present on this connector are defined in the following table.

Pin No	Signal
1	GND
2	R-OUT
3	L-OUT
4	NC
5	NC

Table 17: Audio Output Jack

Pin No	Signal
1	GND
2	R-IN
3	L-IN
4	NC
5	NC

Table 18: Audio IN Jack

3.5.2 USB Connector

Connector P16 is a mini A/B USB connector.

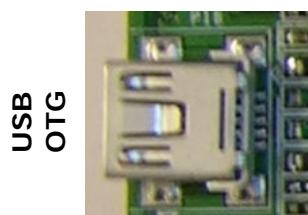
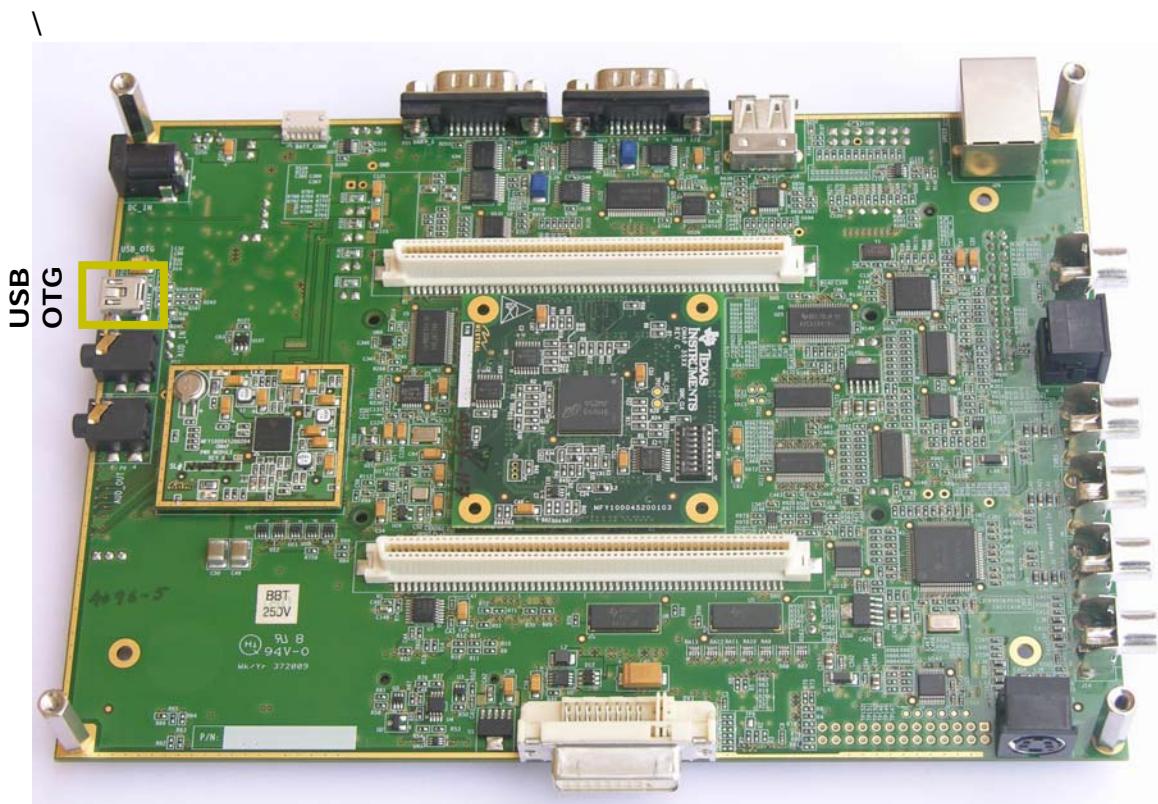


Figure 19: USB Connector

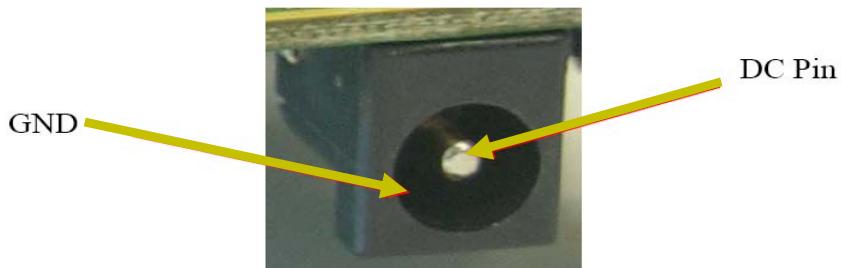
The pin out for the P16 connector is shown in the figure below.

Pins	Signal
1	USB_VBUS
2	USB_DM
3	USB_DP
4	USB_ID
5-9	USB_SHIELD

Table 19: USB Connector

3.5.3 DC Power Jack

Connector P19 is a 2.5mm DC input jack for power adaptor input. This connector brings in +5 volts to the EVM. It has its inner side tied to VCC +5V through a fuse and the outer side is tied to ground. The figure below shows this connector as viewed from the card edge.

**Figure 20: DC Power Jack**

3.5.4 UART Connector

The P20 and P21 connector is a DB9 -connector that provides a UART interface to the EVM. This connector interfaces to the MAX 3218 RS-232 line driver and is located on the bottom side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.



Figure 21: UART Connector

The pin numbers and their corresponding signals are shown in the table below.

Pin	Signal
1	NC
2	RX
3	TX
4	Short
5	GND
6	Short
7	NC
8	NC
9	NC

Table 20: UART DB9 Connector

3.5.5 Ethernet Connector

The J10 connector is located on the bottom side of the board and is used to provide an Ethernet interface. J10 integrates the magnetic and standard RJ-45 connector. The tables below show the signals present on the connector side.

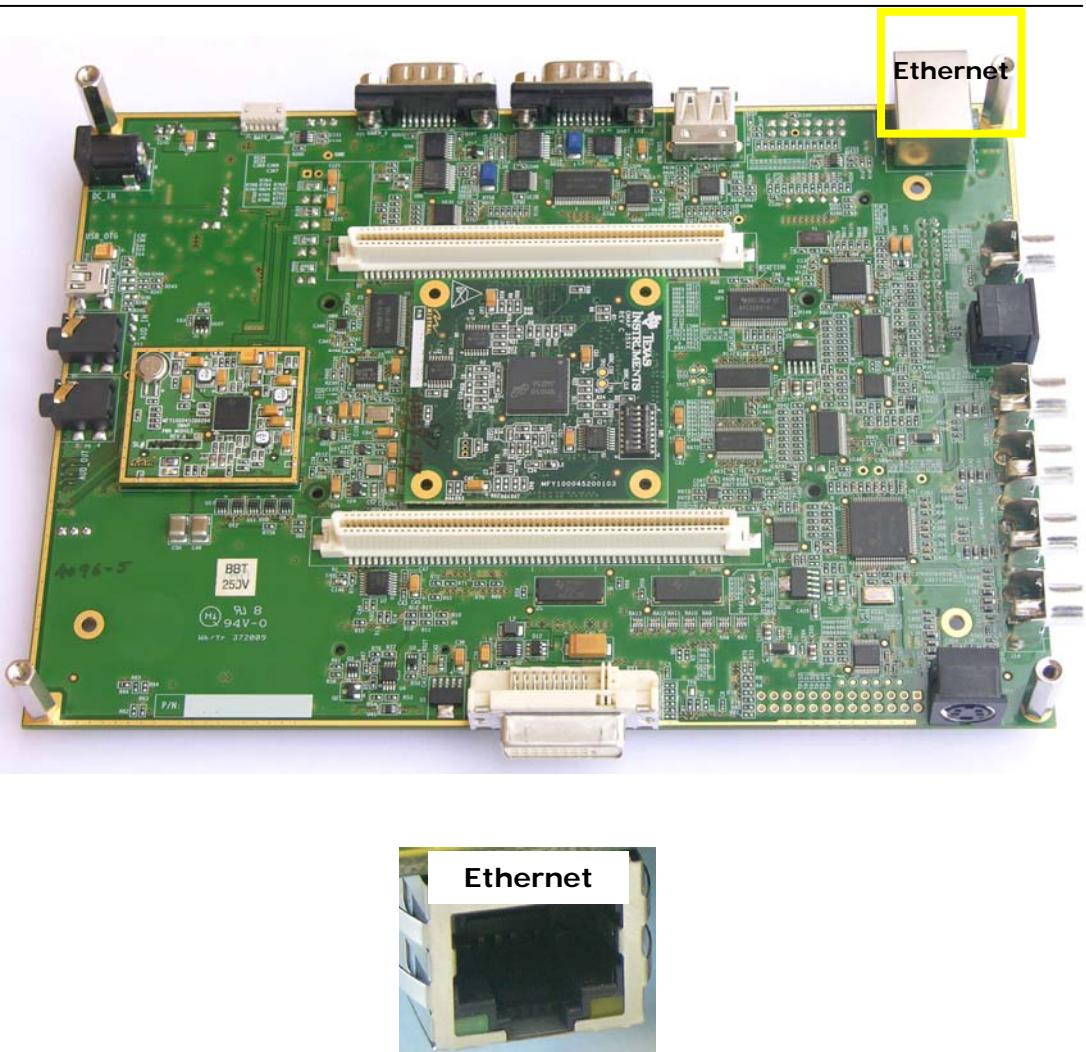


Figure 22: RJ45 Connector

Pin No	Signal	Pin No	Signal
1	TX+	2	Center Tap
3	TX-	4	RX+
5	Center Tap	6	RX-
7	NC	8	GND
9	LED-	10	LED+
11	LED-	12	LED+
13	GND	14	GND

Table 21: Ethernet RJ45 Connector

3.5.6 Battery Input Connector

J11 is a battery main input connector that will carry the battery power in the OMAP EVM board. It is placed on the bottom of the EVM main board. The J11 connector pin descriptions are given below.

Pin No	Signal
1	VBAT IN
2	NC
3	CHG TS
4	HDO 2V8
5	ADC IN0
6	GND

Table 22: Battery Terminal Connector

3.5.7 Processor Module Connector

P8, P12, P13 and P17 board-to-board connector is used to bring out most of the OMAP processor signals to the main board. OMAP processor module is a plug-in option module that will plug in to this connector. Refer schematic section for signal and pin out details for this connector.

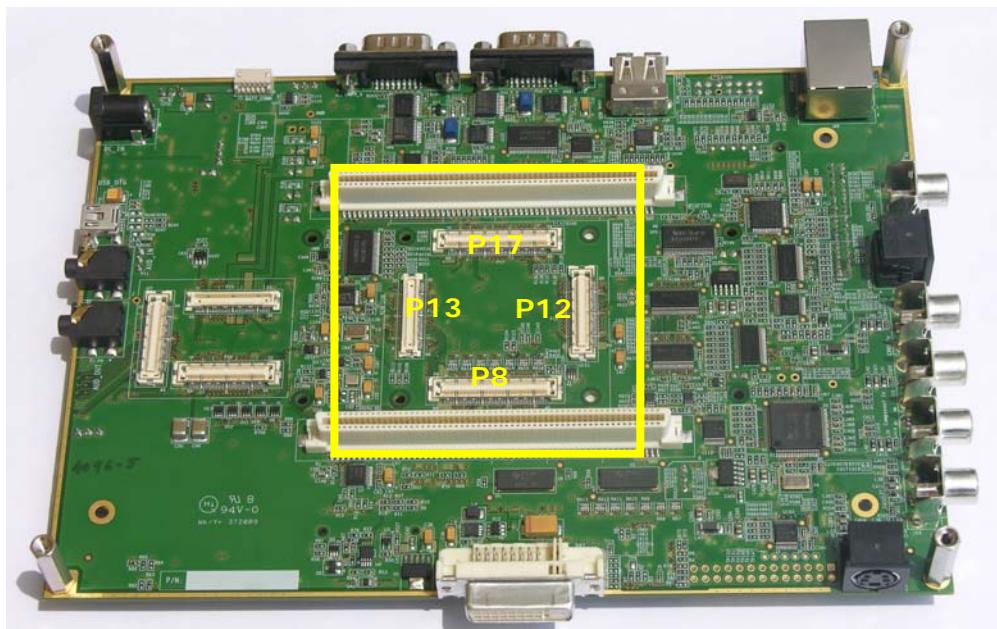


Figure 23: OMAP Processor Module board-to-board connector

3.5.8 Power Module Connector

P10 P15 & J21 board-to-board connector is used to bring out the entire Power Module signal to main board. Power module is a plug-in option module that will plug in to this connector. It is a 66 pin constructed as 33 pin in to 2 row connector of 3 numbers is used. Refer schematic section for signal and pin out details for this connector.

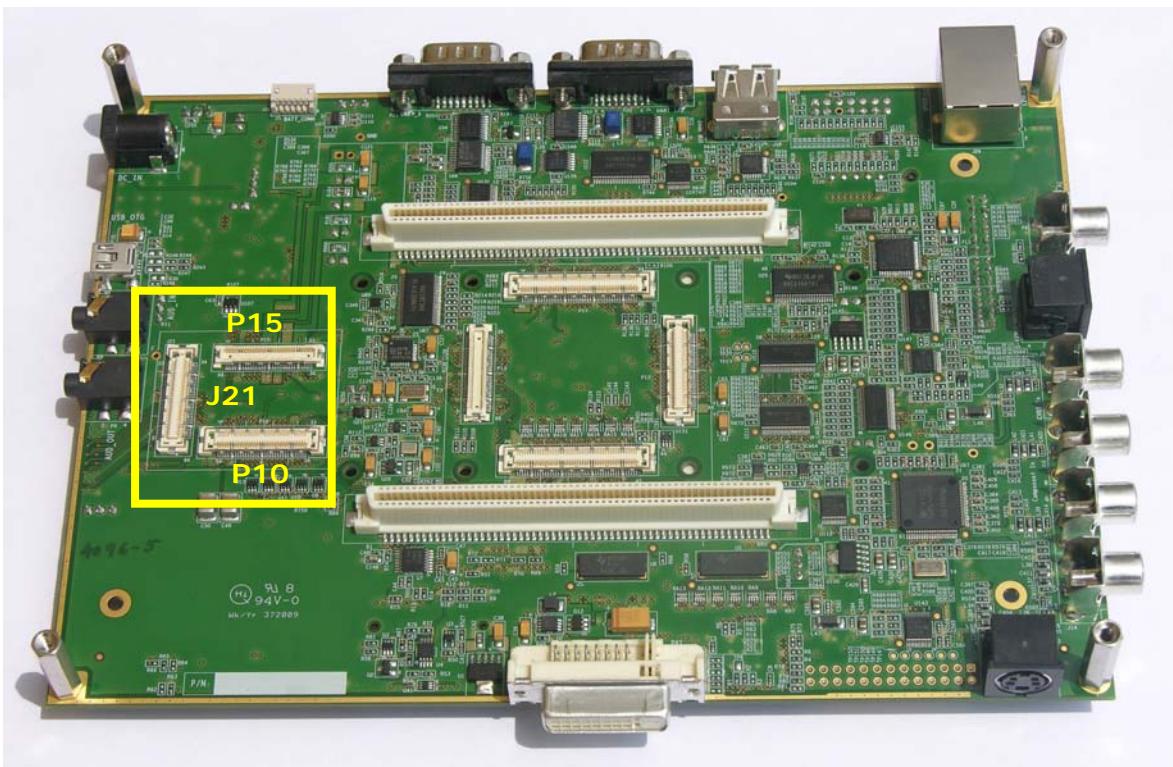


Figure 24: Power Module board-to-board connector

3.5.9 Switches:

The list of switches on OMAP 35x EVM is given below

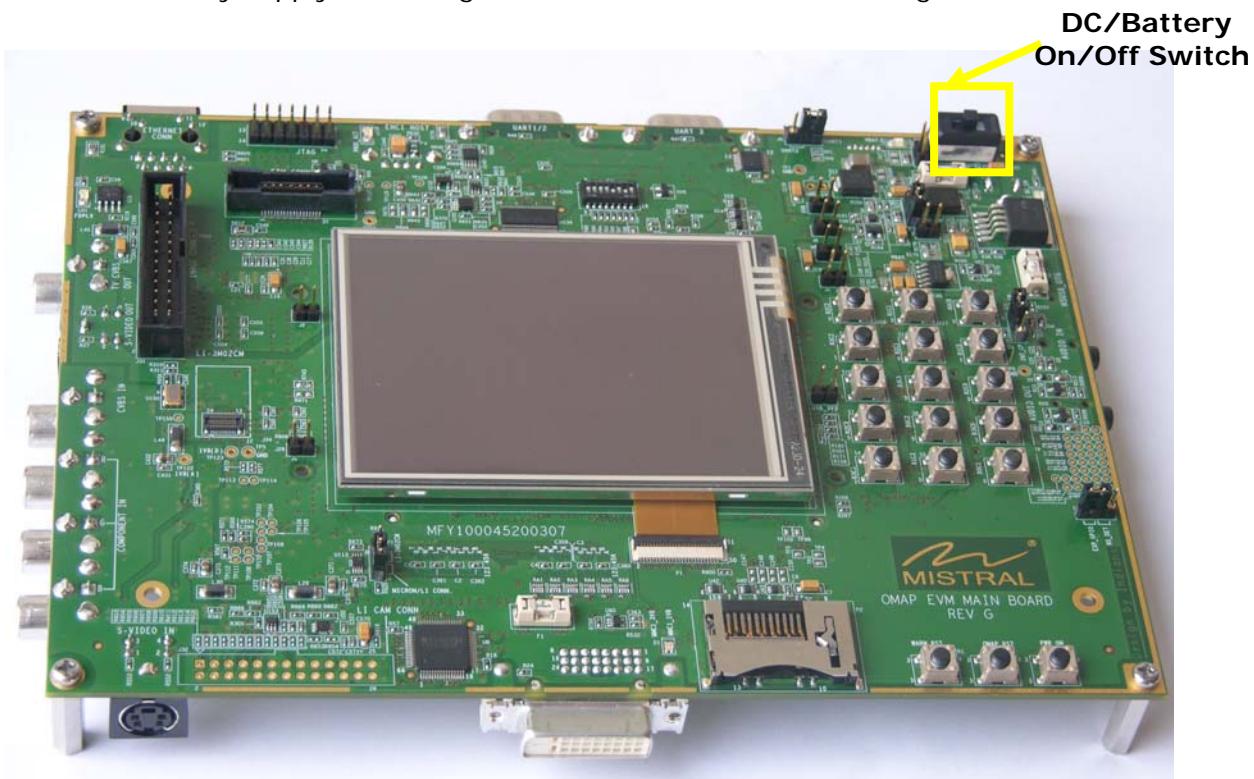
Switches	Type	Location	Function
SW2	POS	Main board	Battery or DC input selection
SW4	POS	Main board	SYSBOOT configuration
S1	MOM	Main board	Warm Reset
S2	MOM	Main board	OMAP EVM Reset

S3	MOM	Main board	Power ON / OFF
S4 to S18	MOM	Main board	15 - User Functional Keys
SW1	POS	Processor Module	Mux control

Table 23: EVM Switches

3.5.10 Main Board - SW2

The SW2 switch is a 2-position jumper located on the topside of the board and is used to select the source of the input Power as either external Power adaptor or Battery supply. The image of this switch is shown in the figure below.

**Figure 25:** SW2 Switch Location

Function	SW2 Switch Position	Description
Vdc_In (Default)	To connect an external 5V power supply, select the switch position to DC (refer the label on the EVM main board).	Main Supply (DC Wall Supply) will be enabled.
VBAT_In	To connect Battery, select the switch position to Batt (Pin 1).	Battery will be enabled.

Table 24: EVM Main Board – SW2**3.5.11 Main Board - SW4**

The 8-position, physical DIP switch (SW4) on the main board is used to control the various boot modes of the processor. DIP switch SW4 positions 1 through 6 and 8 controls the SYSBOOT options for OMAP3. The tables (shown below) provide a brief description of each setting.

SW-4 Switch Position	SW4-1	SW4-2	SW4-3	SW4-4	SW4-5	SW4-6	SW4-7	SW4-8
SYS_BOOT Signal	SYS_BOOT 0	SYS_BOOT 1	SYS_BOOT 2	SYS_BOOT 3	SYS_BOOT 4	SYS_BOOT 5	Not Used	Boot UART

Table 25: Main Board SW4 Switch Description

Table below shows the switch configuration required for booting from NAND Flash Memory.

Switch	1	2	3	4	5	6	7	8
SW4	OFF	ON	OFF	ON	OFF	ON	OFF	OFF

Table 26: SW4 configuration- NAND Boot

Table below shows the switch configuration required for peripheral booting from UART3.

Switch	1	2	3	4	5	6	7	8
SW4	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF

Table 27: SW4 configuration- Peripheral Boot

3.5.12 Main Board - S1 Warm Reset Button

This switch generates a warm reset to the Processor and the Power Module device.

Setting	Function
OPEN	Normal operating condition. Open = logical '1' state
PUSH BUTTON CLOSED	Active low reset signal commands system to reinitialize with all power supplies are still applied. Closed = logical '0' state

Table 28: Warm Reset Push Button

3.5.13 Main Board - S2 OMAP Reset

This switch can be used to reset and re-boot the OMAP35x EVM system.

Setting	Function
OPEN	Normal operating condition. Open = logical '1' state
PUSH BUTTON CLOSED	Active low Power On reset signal commands system (OMAP35x EVM) to Reset. Closed = logical '0' state

Table 29: EVM Reset Push Button

3.5.14 Main Board - S3 Power ON / OFF

The Power ON / OFF switch (S3) is connected to PWRON signal of TPS65950 device. This can be configured in software to switch ON or OFF the system.

Setting	Function
OPEN	Normal operating condition. Open = logical '1' state
PUSH BUTTON CLOSED	Active low signal will enable PWRON signal of TPS65950 device. Closed = logical '0' state

Table 30: Power Module ON/OFF Push Button

3.5.15 Main Board – Keypad Switches

4 x 4 Matrix keys are used for user functional buttons. All the keys are placed on the top of the board. The image of these keys is shown in the figure below.

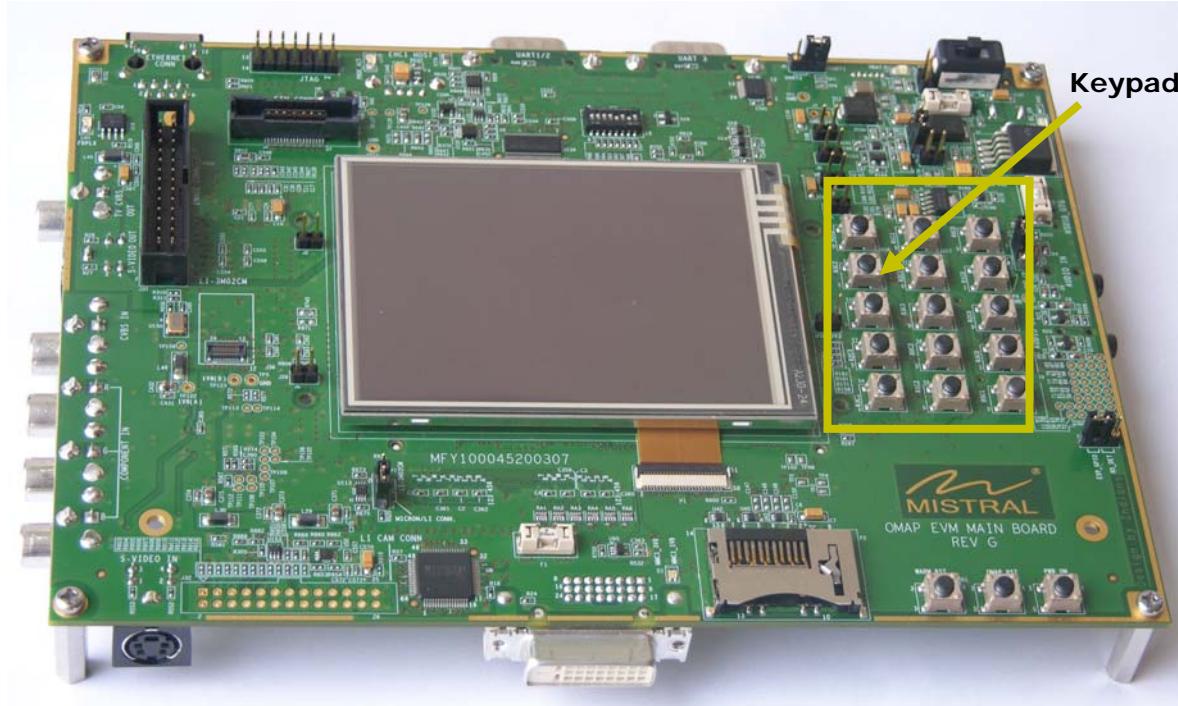


Figure 26: Key pad Switches

3.5.16 OMAP Processor Module - SW1

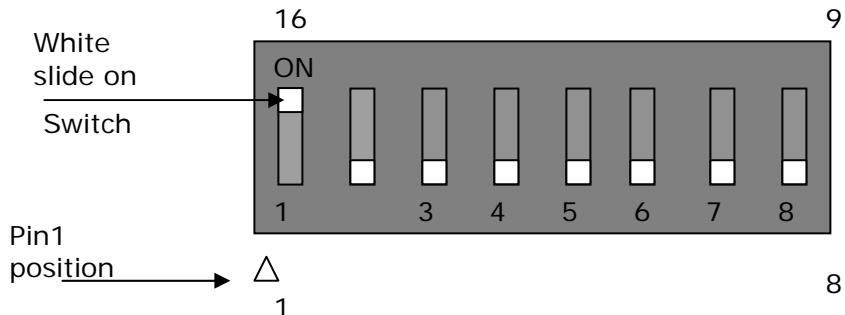
Switch Position	Signal Name	Switch state	Description
SW1-1	JTAG_EMU0	ON	JTAG enabled
		OFF	JTAG disabled
SW1-2	JTAG_EMU1	OFF	Default
SW1-3	UART3_SEL	ON	UART3 connected to Expansion connector (Daughter card)
		OFF	UART3 connected to OMAP EVM main board
SW1-4	McBSP2_SEL	ON	McBSP2 connected to Expansion connector (Daughter card)
		OFF	McBSP2 connected to OMAP EVM main board
SW1-5	McBSP3_SEL	ON	McBSP3 connected to Expansion connector (Daughter card)
		OFF	McBSP3 connected to OMAP EVM main board
SW1-6	SPARE	x	SPARE/Not used
SW1-7	SPARE	x	SPARE/Not used
SW1-8	SPARE	x	SPARE/Not used

Table 31: OMAP Processor Module – SW1**SW1 configuration for JTAG mode:**

SW1 Default Settings for JTAG Test							
SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6	SW1-7	SW1-8
ON	OFF						

Table 32: SW1 Switch configuration for JTAG

The figure below shows the switch layout.

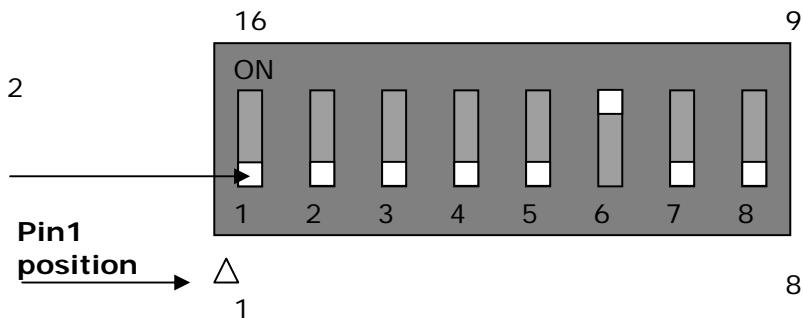


SW1 configuration for non-JTAG mode (Peripheral boot-UART3)

SW1 Default Settings for JTAG Test							
SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6	SW1-7	SW1-8
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF

Table 33: SW1 Switch configuration for Peripheral boot

The figure below shows the switch layout.



3.6 Jumpers

The list of jumpers on the OMAP 35x EVM is given below:

Jumpers	Type	Function
J2	1 x 2	GPIO 139 or GPIO 141 Select tap
J3	1 x 2	VDC IN or VBAT Select and short
J4	1 x 2	VBAT current measurement tap
J5	1 x 2	VDD2 current measurement tap
J6	1 X 2	VDD CORE 1V3 current measurement tap
J7 , J9	1 X 2	VIO 1V8 current measurement tap
J8	1 X 3	UART1 or UART2 Selection
J12	1 X 2	3V3 current measurement tap

Table 34: EVM Jumpers

3.6.1 *UART Selection Jumper*

Jumper J8 provides the option for selecting between UART1 and UART2. By Default UART1 is selected (pins 1 & 2 of J8 are shorted). For selecting UART2, pins 2 & 3 of J8 are to be shorted.

Peripheral	Pins To Be Shorted
UART 1 (Default)	1 & 2
UART 2	2 & 3

Table 35: UART Selection Jumper

3.7 Fuses

The list of fuses on the OMAP 35x EVM is given below:

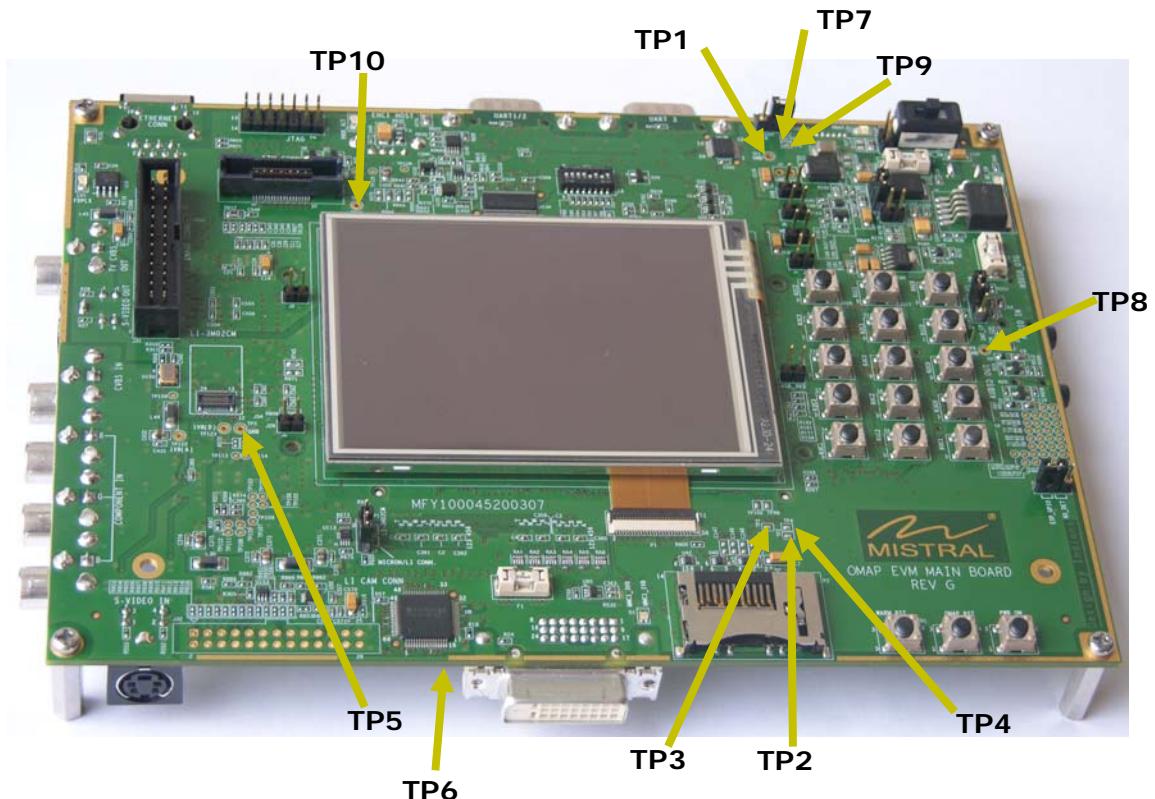
Fuse	Rating	Function
F1	250mA	DVI Interface fuse

F2	3A	DC power IN Fuse
F3	750mA	USB VBUS Fuse
F4	2A	Battery Charge input Fuse

Table 36: EVM Fuses

3.8 Test Points

The EVM has 10 test points. All test points are available on the top side of the board. The following figure identifies the position of each test point and the table lists the each test point signal.

**Figure 27:** EVM Test Points

Test Point	Signal
TP1	GND
TP2	TS Busy
TP3	TSC AUC
TP4	TSC VREFF
TP5	GND
TP6	DVI MSEN
TP7	Level Translator IO
TP8	GND
TP9	Level Translator IO
TP10	GND

Table 37: Test Points

Appendix A

Schematics

This appendix contains the schematics for the OMAP35x EVM.

OMAP Processor Module Schematics

REVISION HISTORY

REV	Description	DATE
REV C	<p>Baseline Version: OMAP35x PROC_SCH, Rev-B</p> <p>1) Connected SYS_BOOTs through Q_0ne (S40) to ENET_RST.</p> <p>2) Multiplexer for selecting S-video and Composite video are removed and these lines shall be connected always.</p> <p>3) DTM_NSECURE is connected to GPIO_64.</p> <p>4) Added 3.3nH inductor and 41pf capacitor in series with TVOUT1 and TVOUT2 lines.</p> <p>Review comments are updated</p>	28-MAY-08

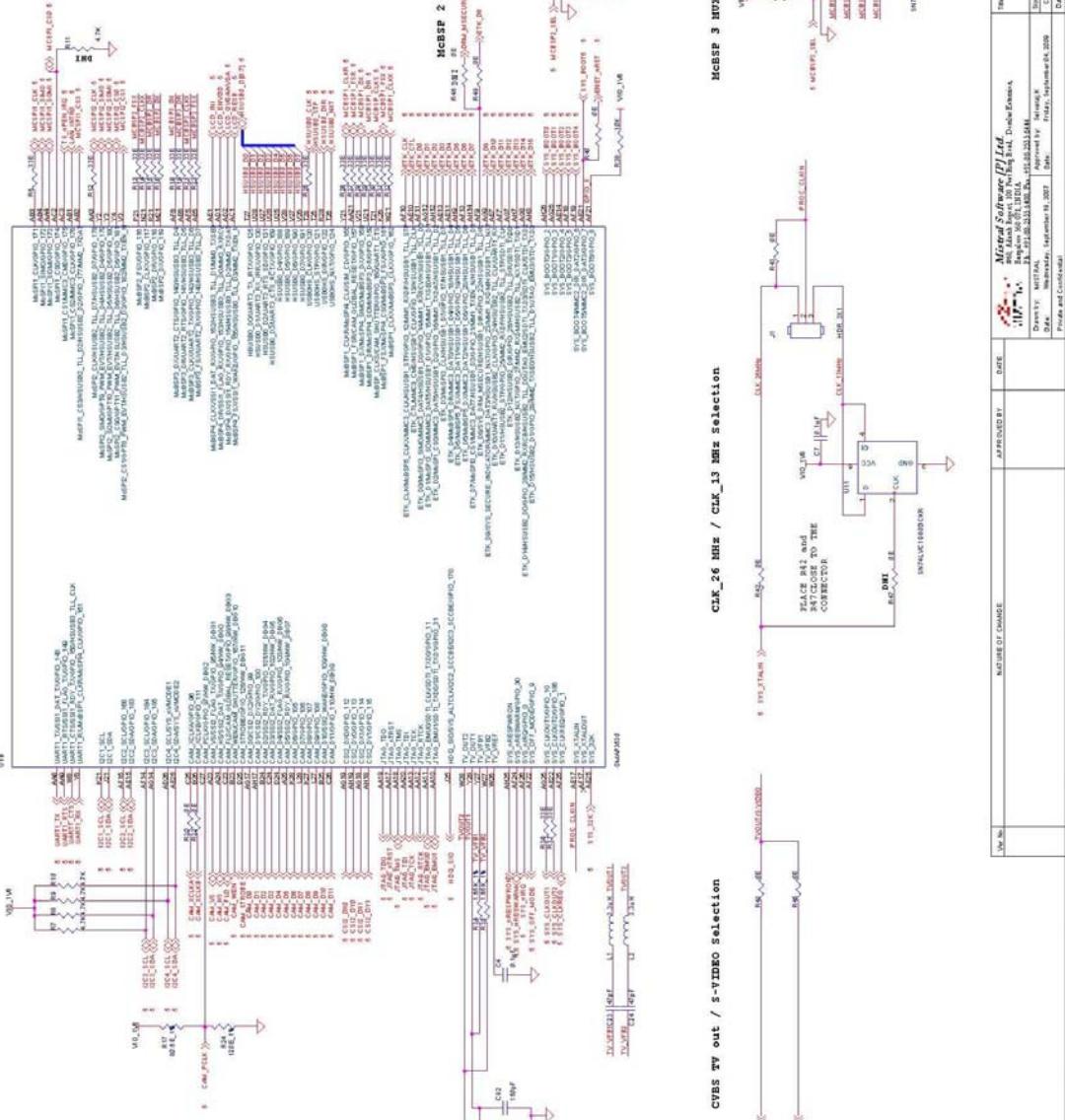
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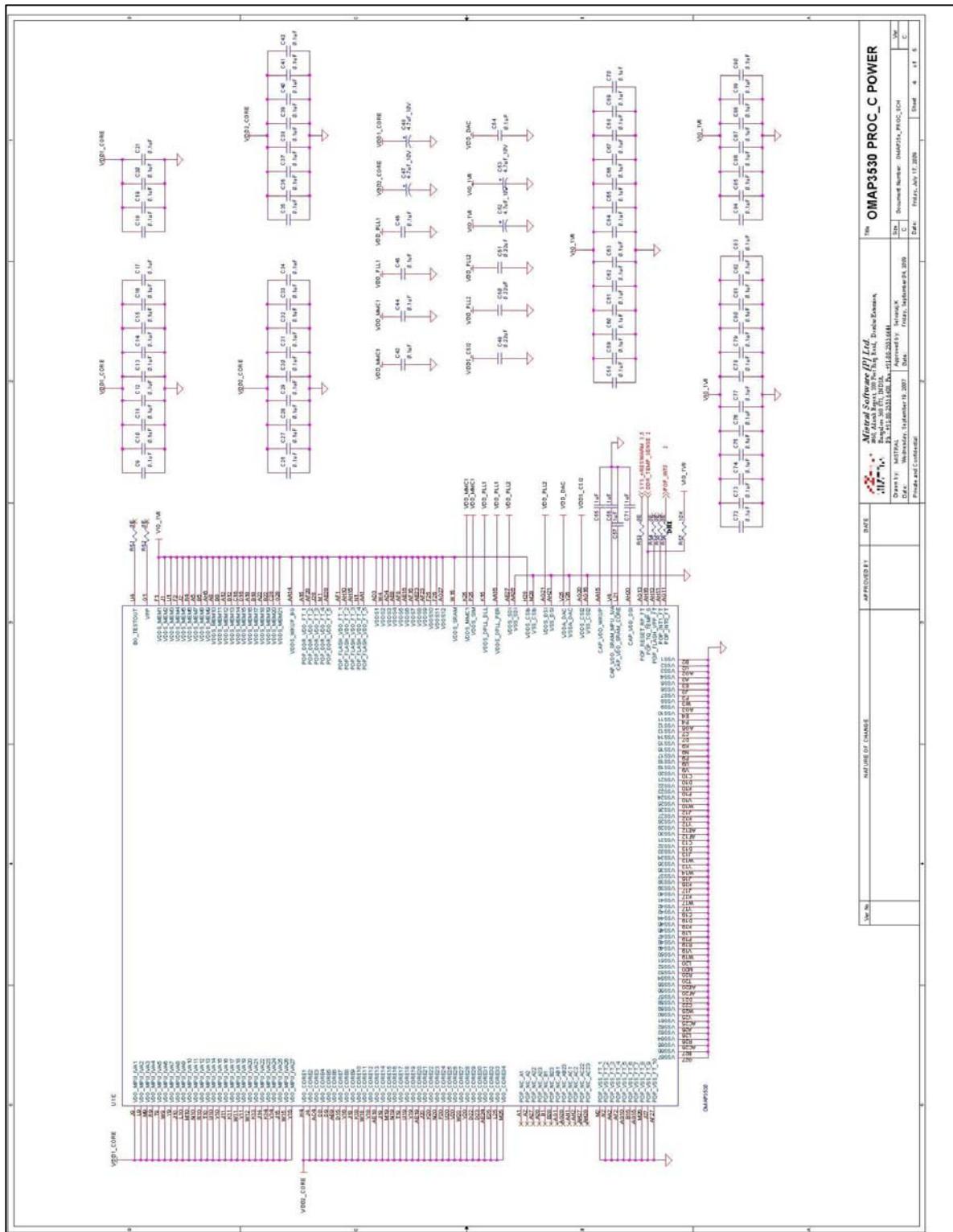
Page No	Schematic Page
01	Cover Page
02	OMAP3530 PROC_A
03	OMAP3530 PROC_B
04	OMAP3530 PROC_C Power
05	OMAP EVM Main board Connectors

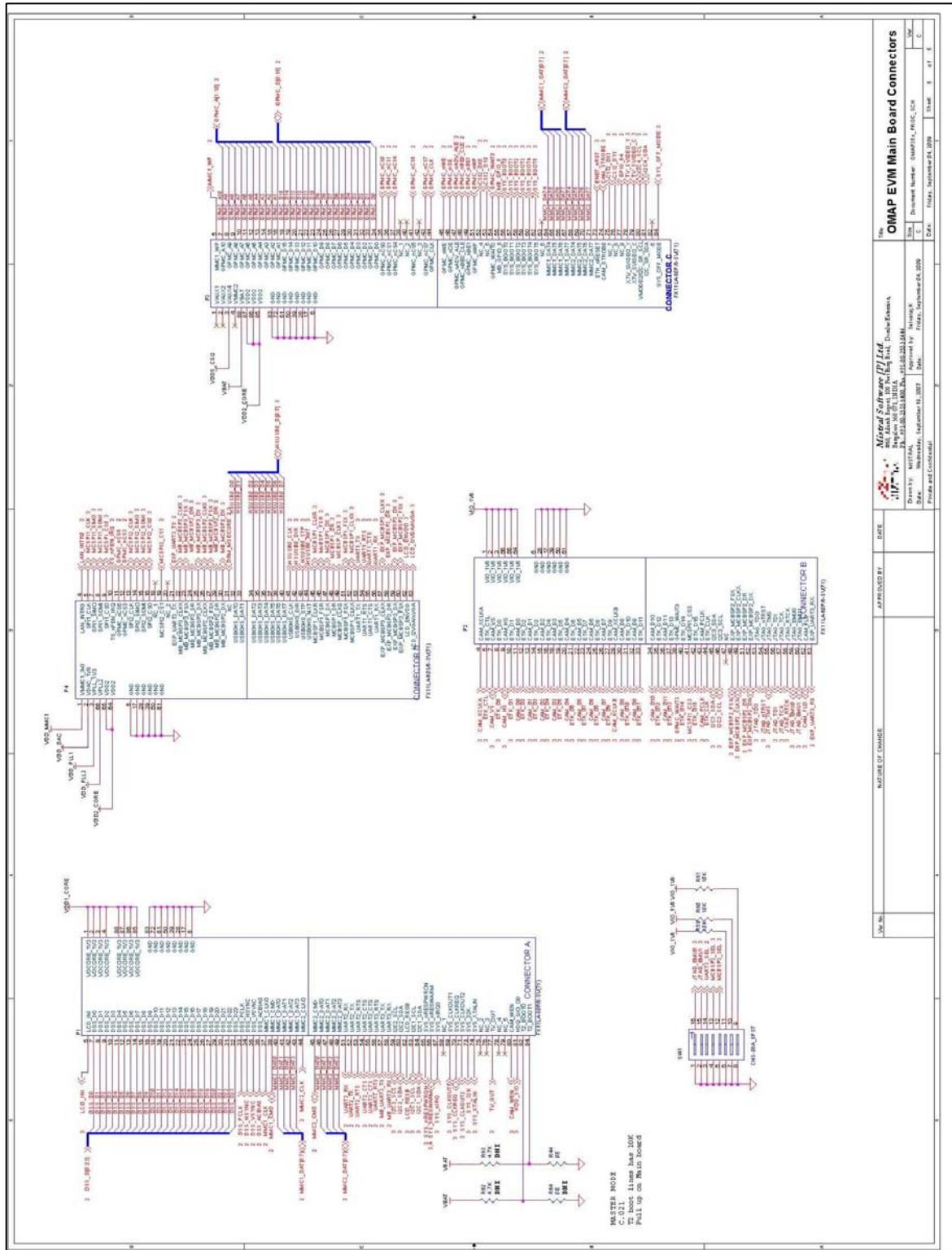
Ver No. _____ NATURE OF CHANGE _____ APPROVED BY _____ DATE _____

<i>P. S. HAN</i>	Misra Software Pvt Ltd. R#3, 3rd Floor, Sector 50, Noida, Uttar Pradesh - 201355, INDIA Ph: +91-98-2555-6000, Fax: +91-98-2555-6664	Approved by: Shrikant K. Date: Friday, September 04, 2009	Document Name: OMAP35x PROC_SCH	REVISION HISTORY
				Ver C Sheet 1 of 5









Power Module Schematics

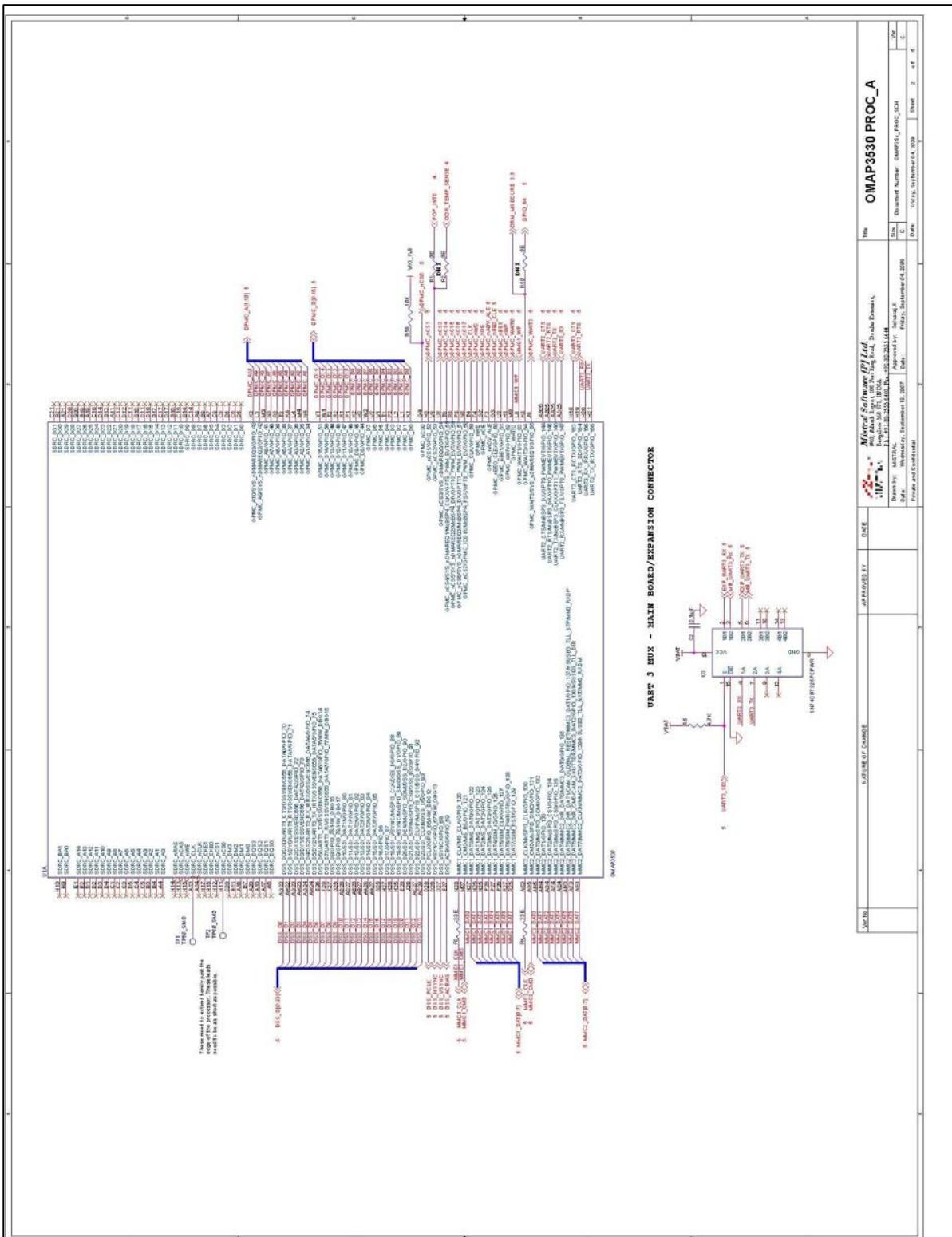
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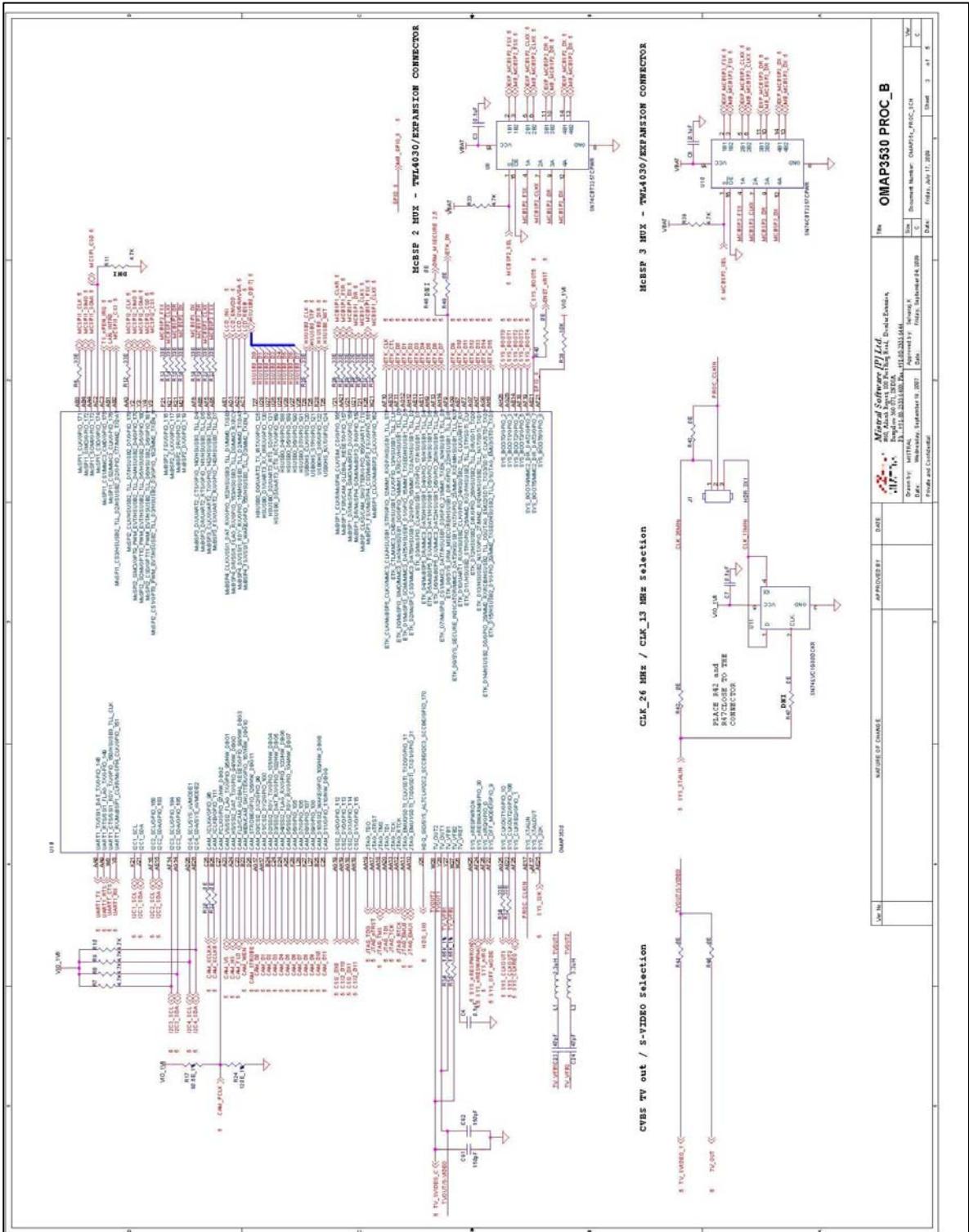
REV	Description	DATE
REV C	Baseline Version: OMAP35x PROC_SCH Rev-B <ul style="list-style-type: none"> 1) Connected SYS_BOOT5 through 0 pins (Pin0) to ENET_RST#. 2) Multiplexer for selecting S-video and composite video are removed and these lines shall be connected always. 3) DPA_MEASURE is connected to GPIO_64. 4) Added 3.3uH inductor and 47pf capacitor in series with TOUT1 and TOUT2 lines. <p>Review comments are updated</p>	28-MAY-09
		28-MAY-09

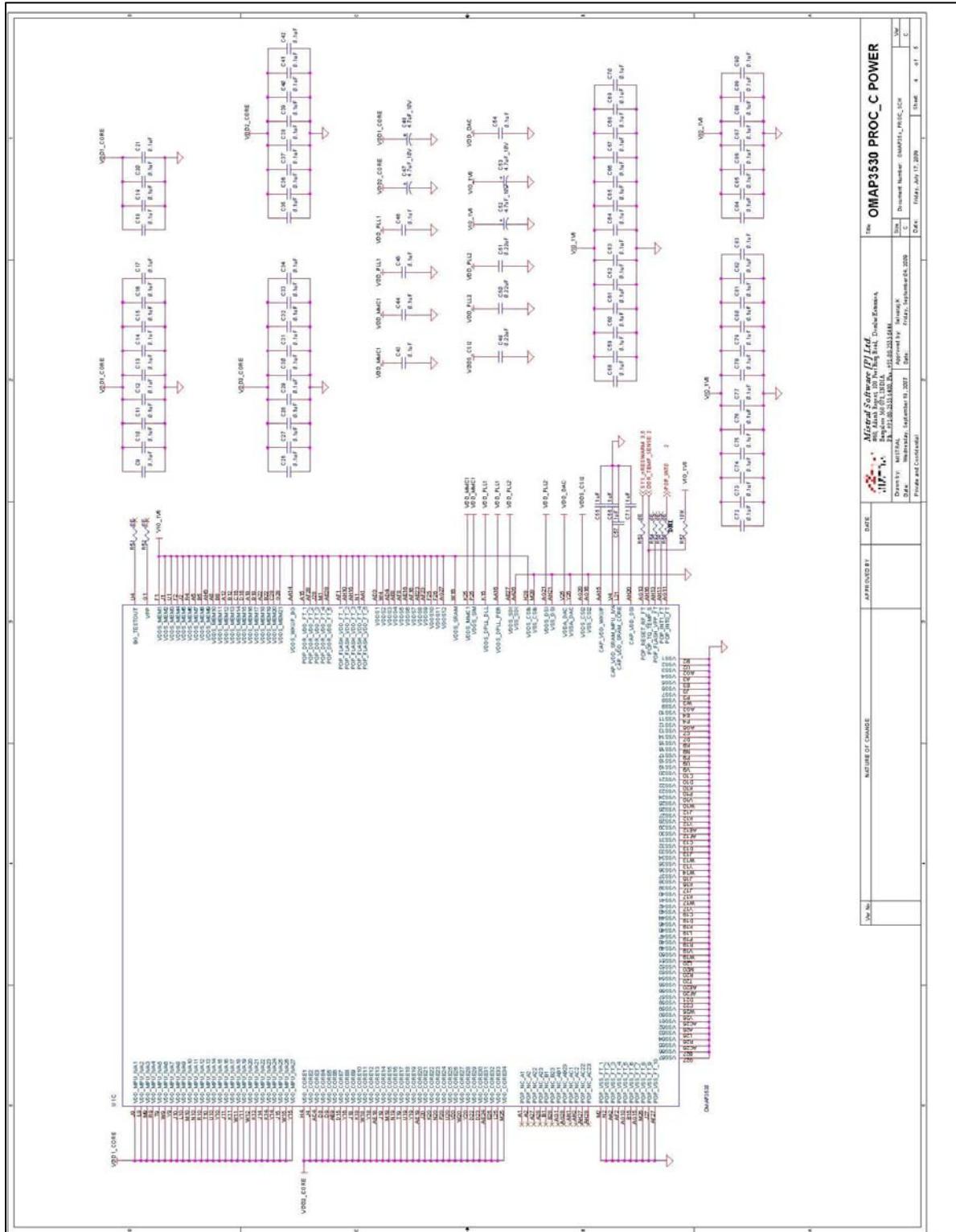
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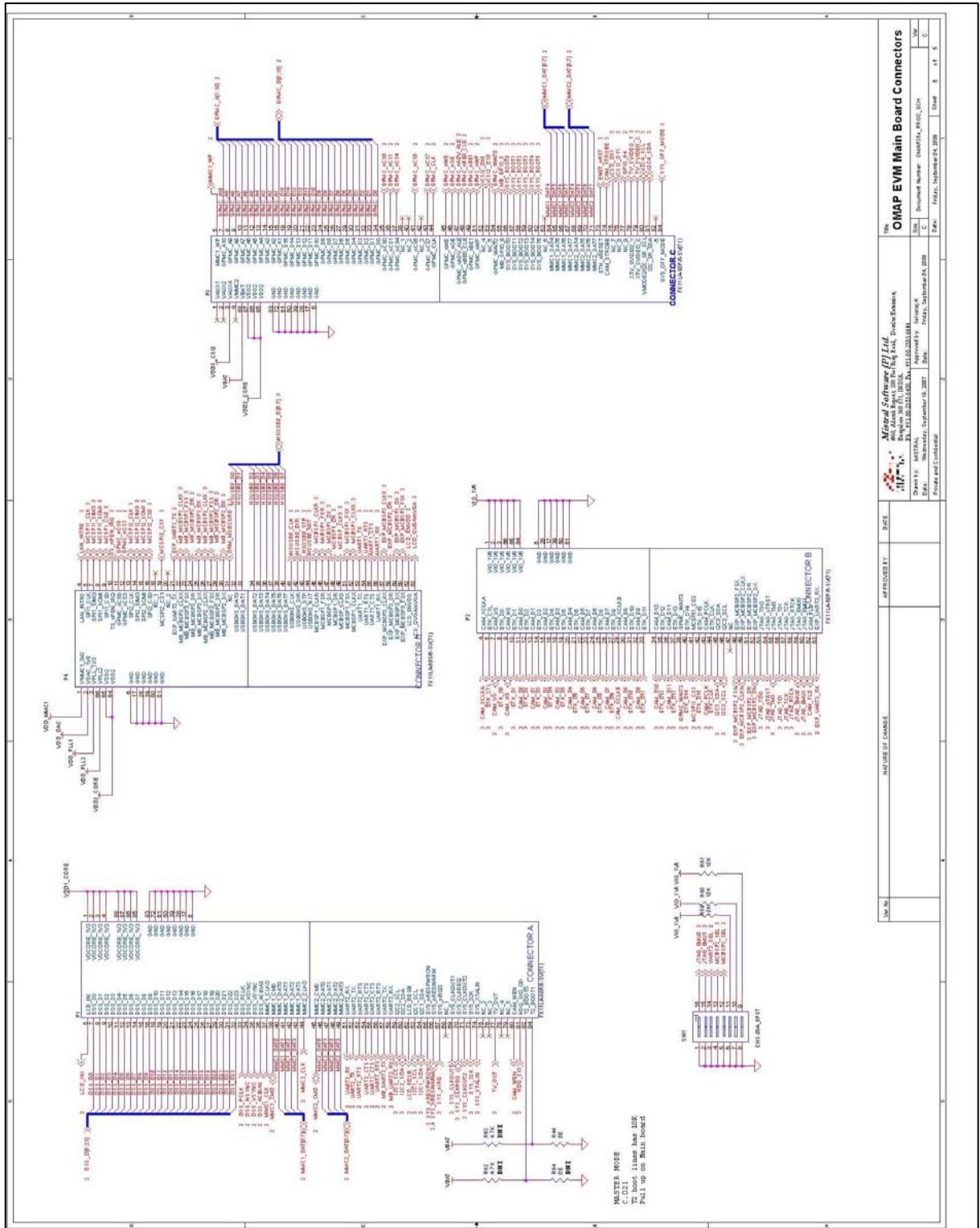
Page No	Schematic Page
01	Cover Page
02	OMAP3530 PROC_A
03	OMAP3530 PROC_B
04	OMAP3530 PROC_C Power
05	OMAP EVM Main board Connectors

Ver No	NATURE OF CHANGE	APPROVED BY	DATE	Mistral Software [P] Ltd.		Title
				Drawn by:	Approved by:	
5				MSTPL - Wednesday, September 16, 2009	Steve K. Friday, September 04, 2009	OMAP35x PROC_SCH
6						Sheet 1 of 5









EVM Main Board Schematics

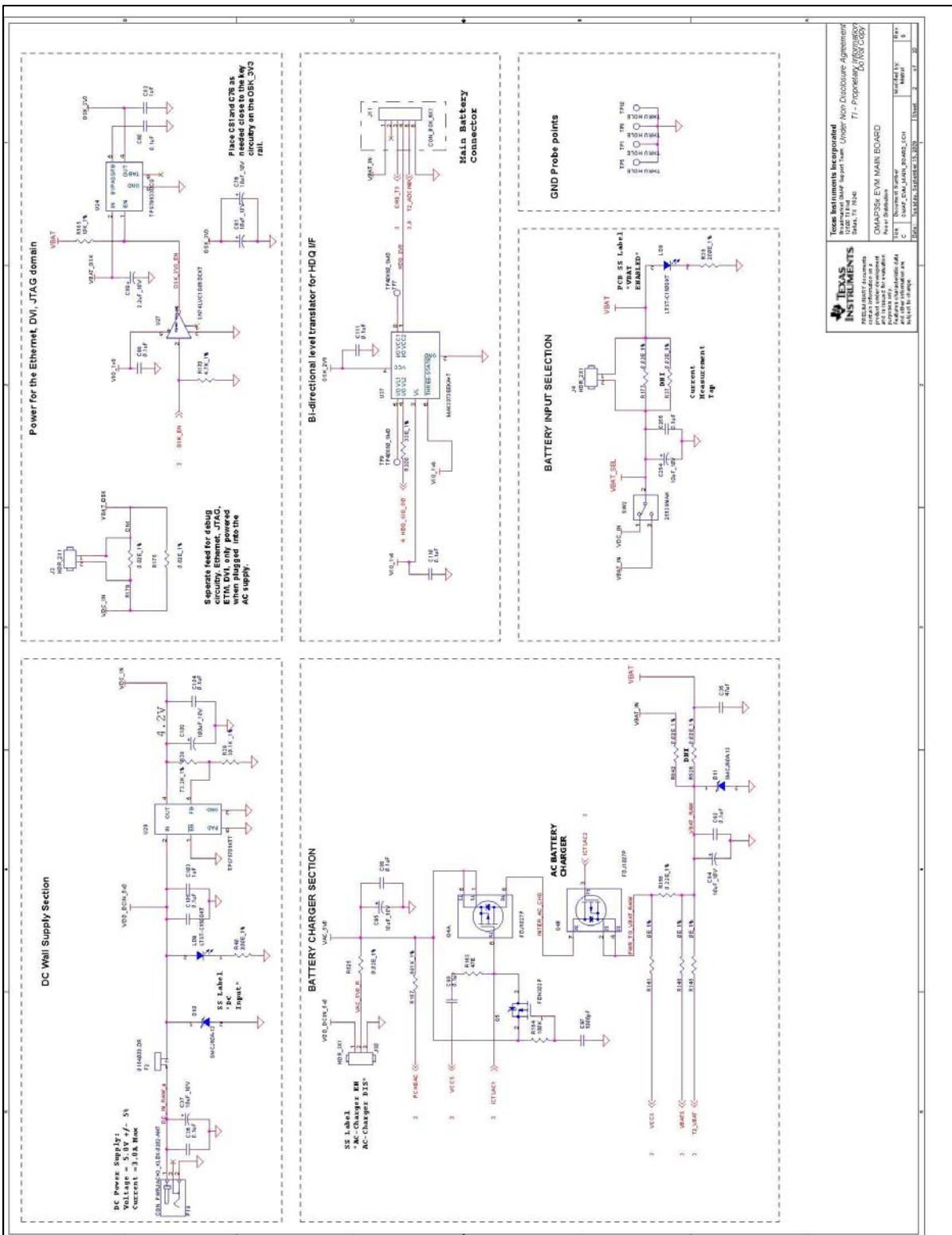
REVISION HISTORY

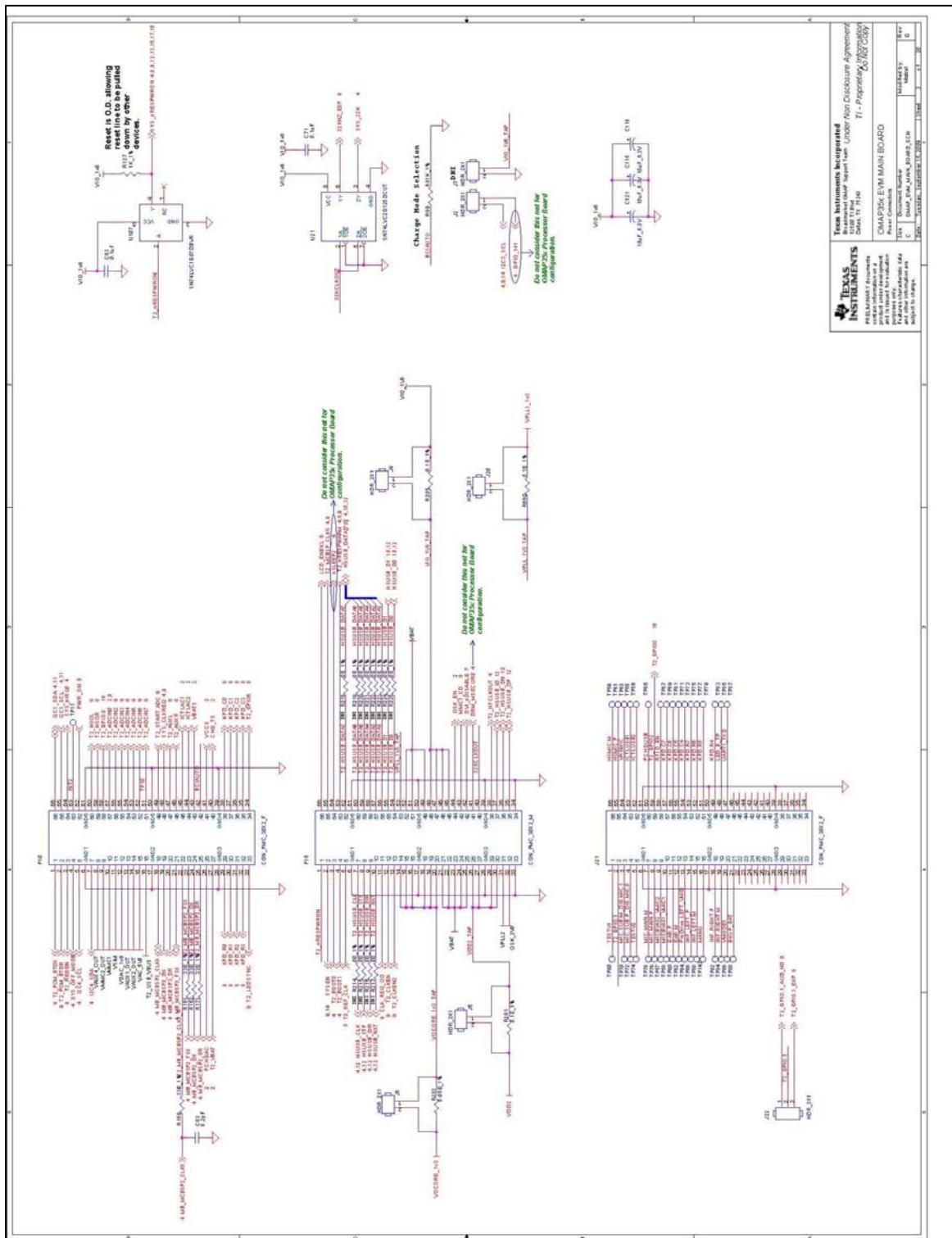
REV	Description	DATE
	BaseLine Revision : OMAP3EVMD8_EVM_M8_SCH_RevD	
REV E	1) Connected STB_BOOT to DTRZ_JTAGST. 2) Filtering capacitors added on the touch panel TFT lines 3) Battery charging sections cleaned up 4) USB OTG circuitry changed to provide up to 500mA 5) audio Headset detect Circuitry Added 6) DFB_PICURE connected to QSPI0 7) On Board I2C Support 8) On board Camera Support 9) WLAN271 Support Revout comments & updated	06-MAY-09
REV F	3-4 Pin Header added to Tab/Lev2 module AC Charger Ethernet Section: R822 - R811, R807/R808 changed to S314A4-1/0H Touch Screen Section: C187, C188, C189 & C180-1R81 1) WLAN Separate through 6pin connector removed. 2) Camera connection added for Micron connector, L1 connector & L1 -2P9 Pin Module 3) I2C-11 3.3V power fail asserted from VAD2 REV G 1) OTG VBUS Switch control flow T81E07 (500mA Support) 5) JF82: Lane RX1: nGM_TD, nGM_TS signal changed to nGM_OQ1_G2 to T2_QF10 Revout comments & updated	28-MAY-09 S04JUN-09
REV G	1. Settle Compensation added for GMIC_CLK 2. Move D14, D15, D10 & D11 as R81 Revout comments & updated	01-SEP-09

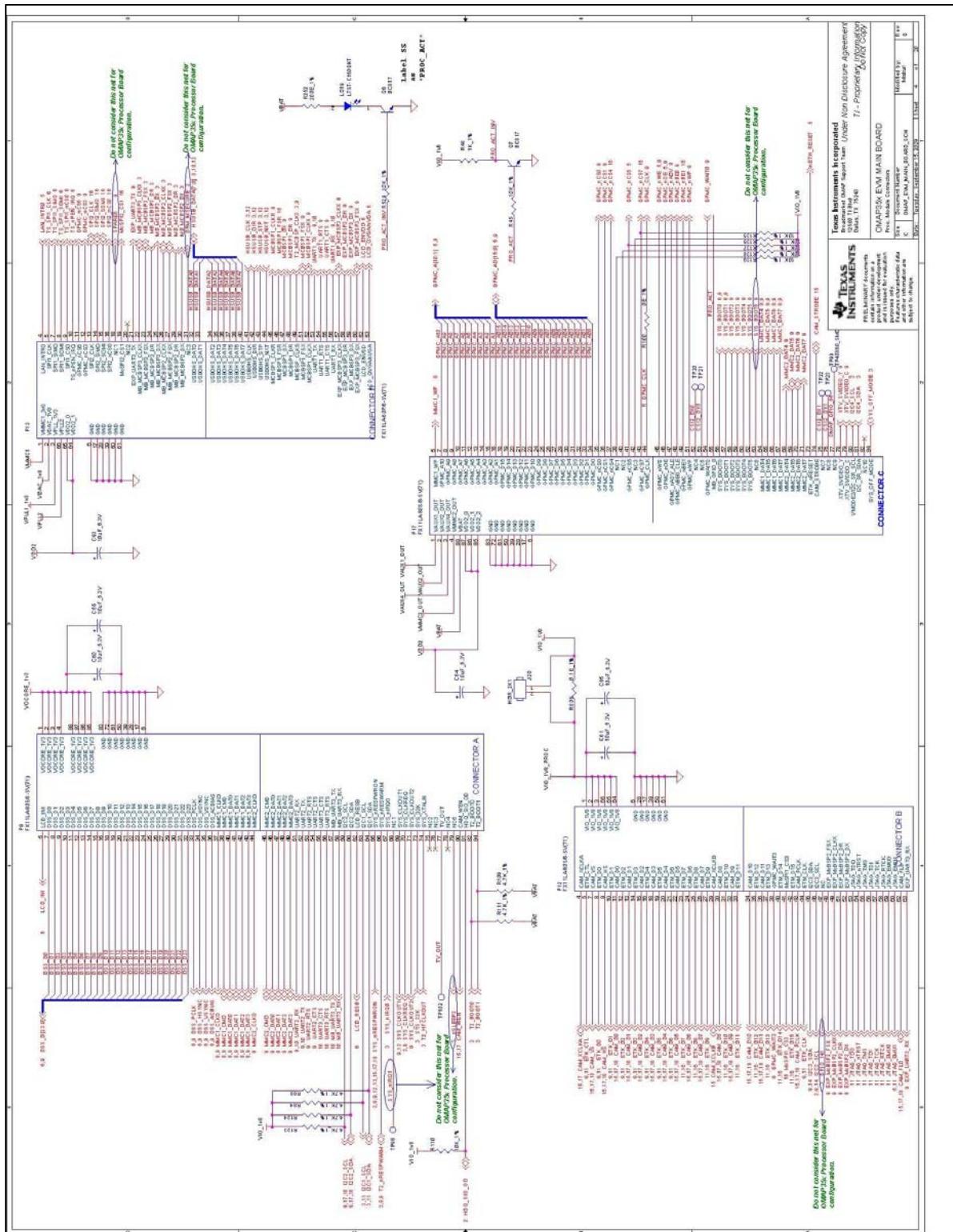
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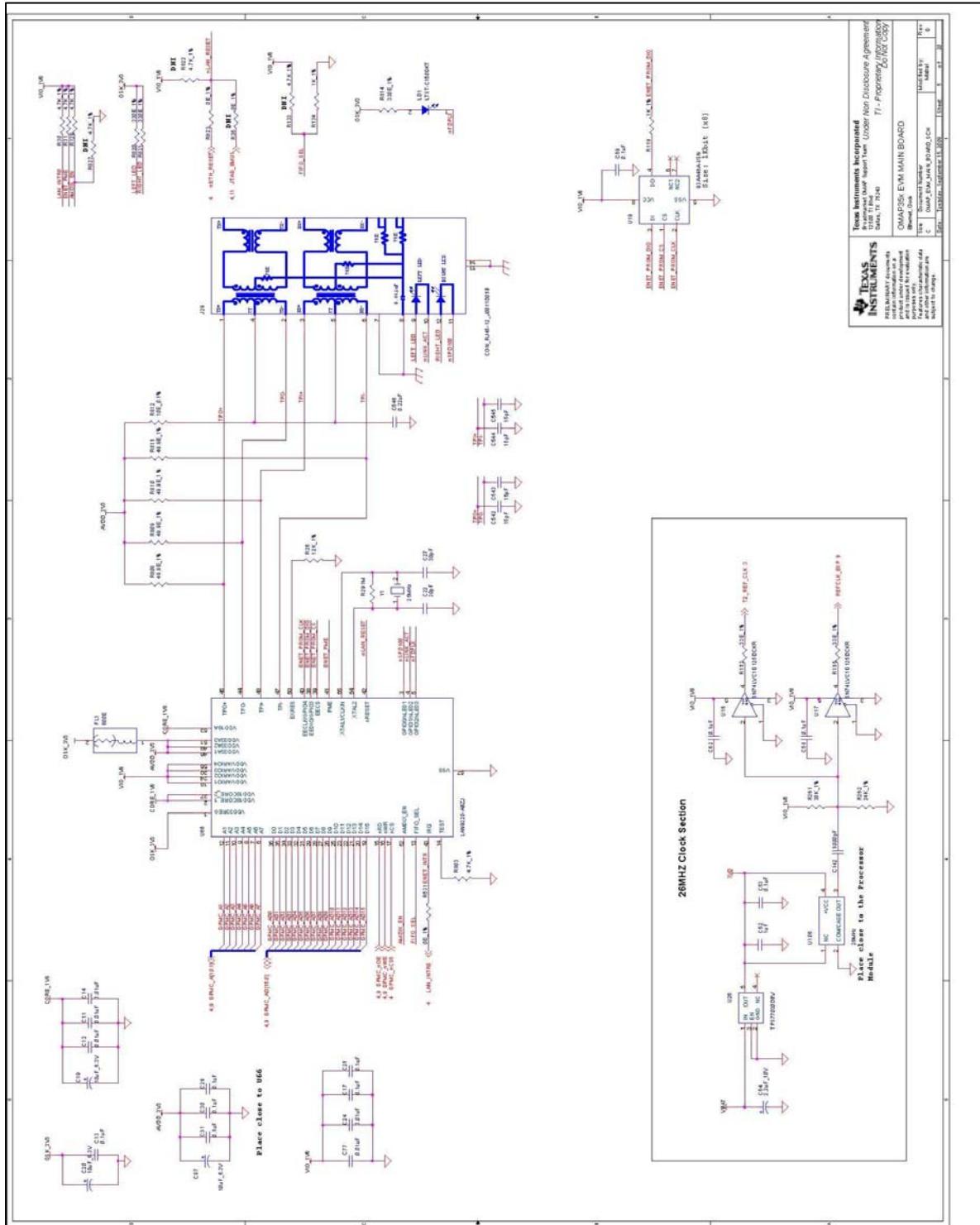
	Page No.	Schematic Page
01	Cover Page	
02	Power Distribution	
03	TWL4030 Power board connectors	
04	OMAP Processor board connectors	
05	Ethernet Interface and Clock Distribution	
06	LCD Panel, Touchscreen & Backlight	
07	DVI Interface	
08	SD/MMC, Audio and Keypad Interfaces	
09	Expansion Module Connectors	
10	UART Interface	
11	ETM & JTAG Interfaces	
12	HSUSB OTG Interface	
13	HSUSB Transceiver and USB	
14	Video Decoder Interface	
15	Video-IN Multiplexing	
16	Transceivers & Switches	
17	On Board Camera Interface	
18	Micron Connector Transceivers	
19	Micron & Li Camera Connectors	
20	Miscellaneous	

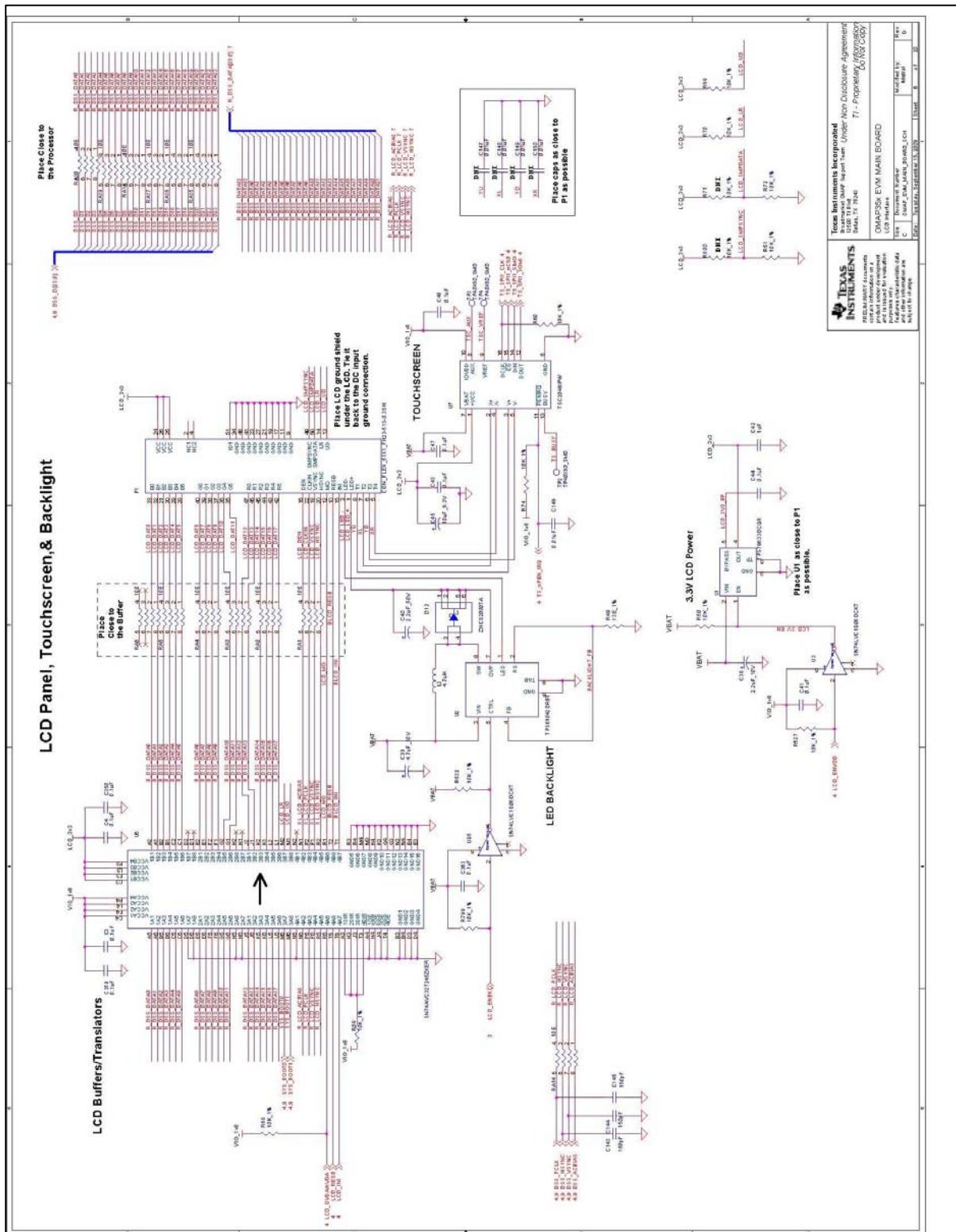


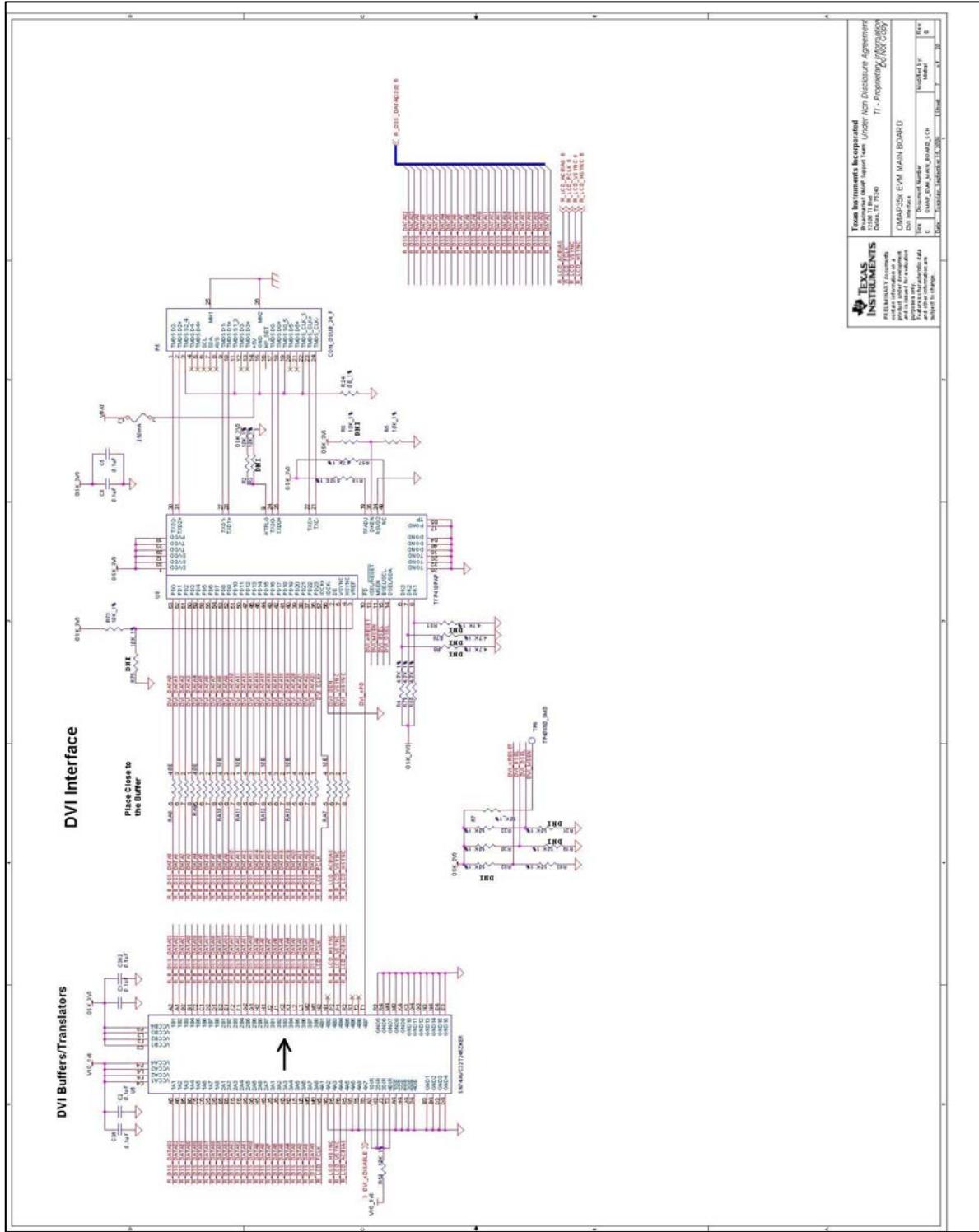


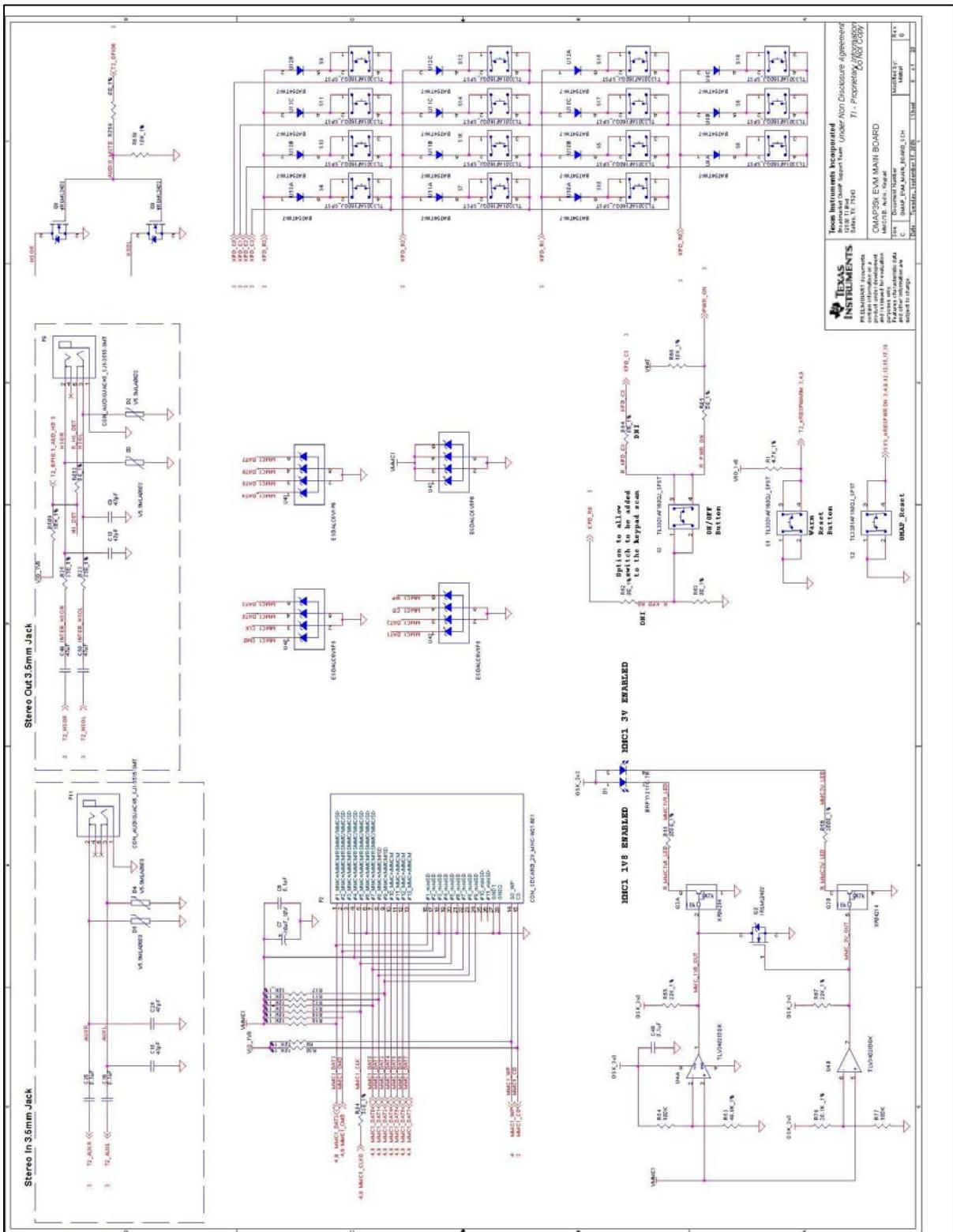


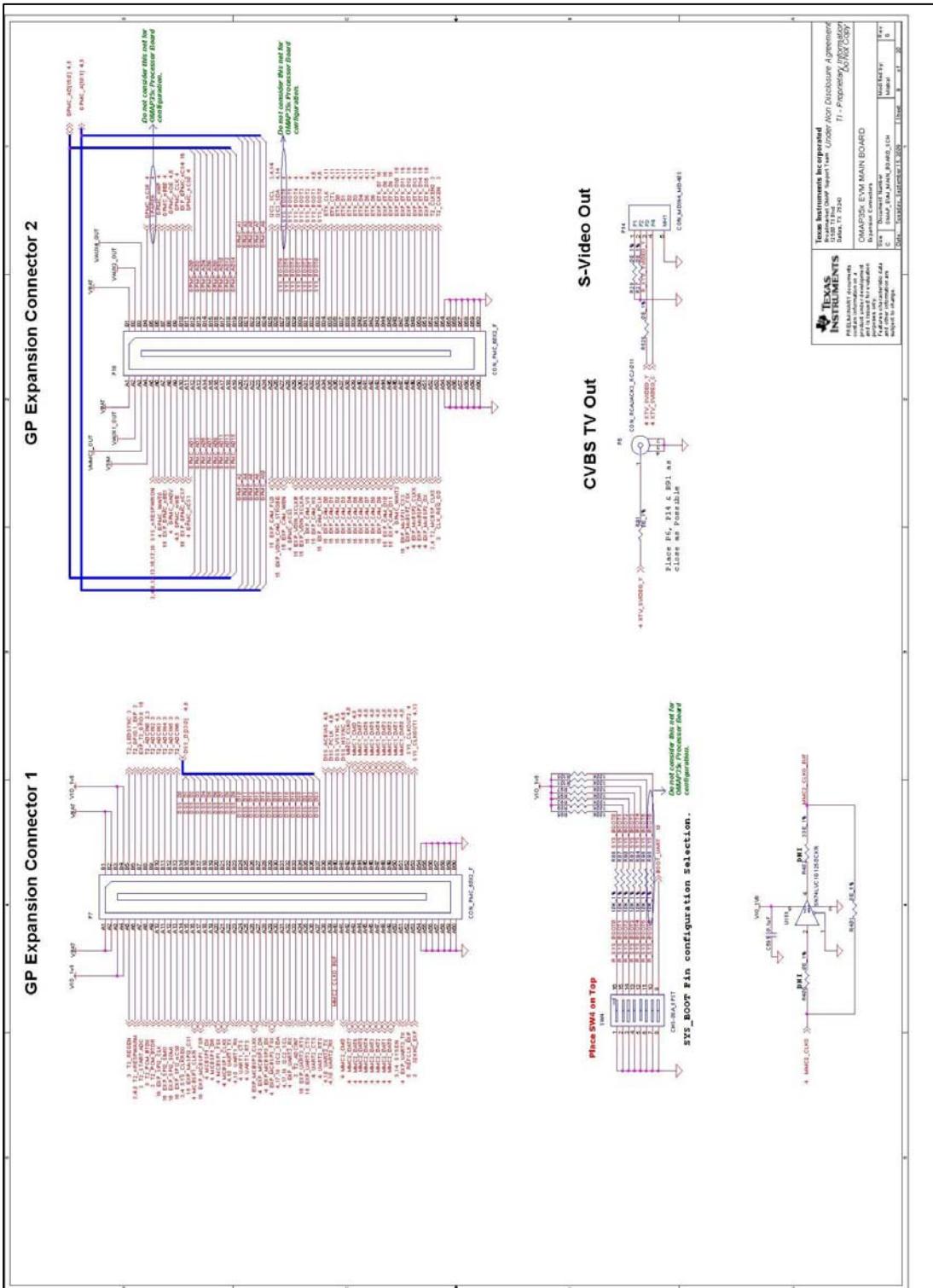


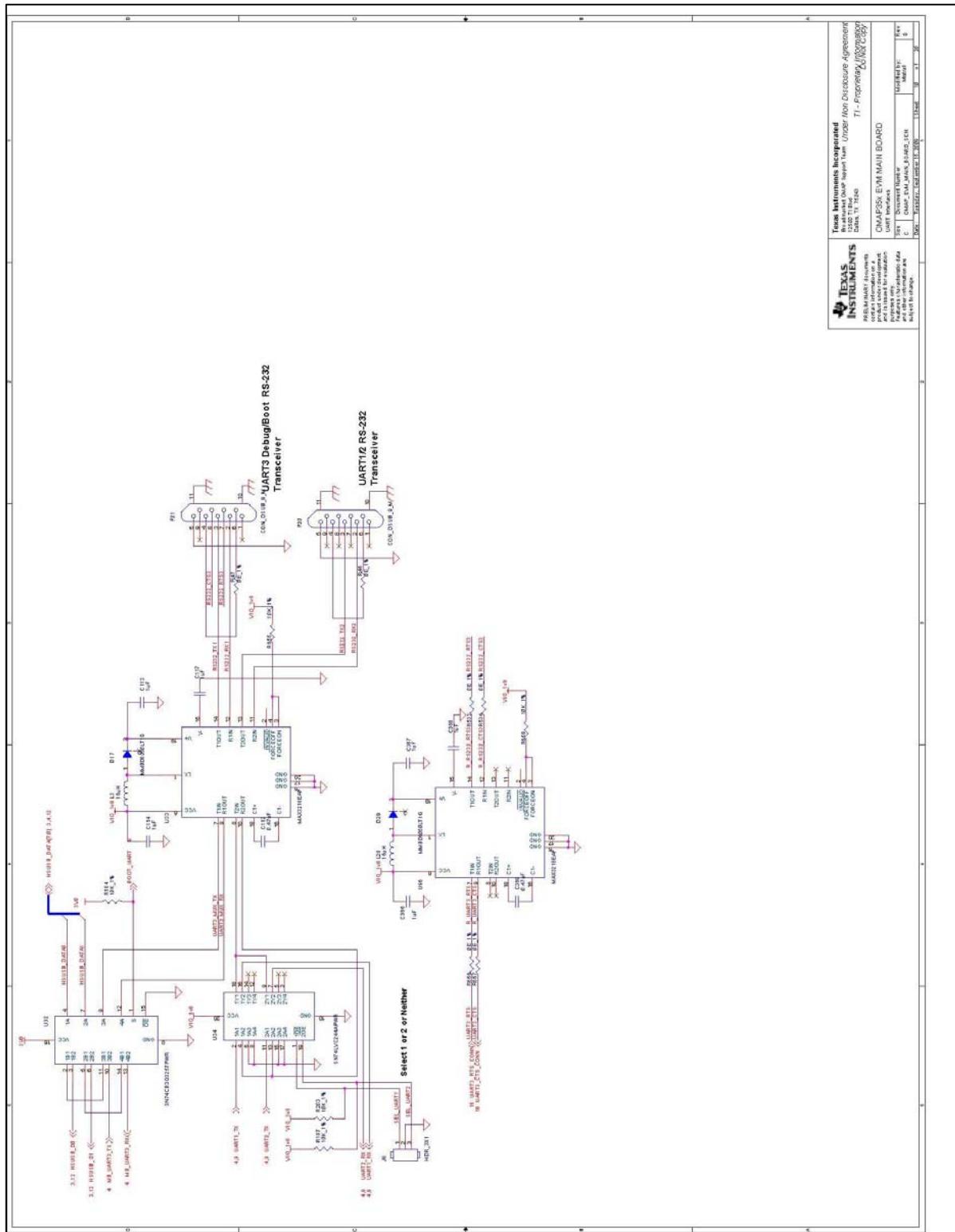


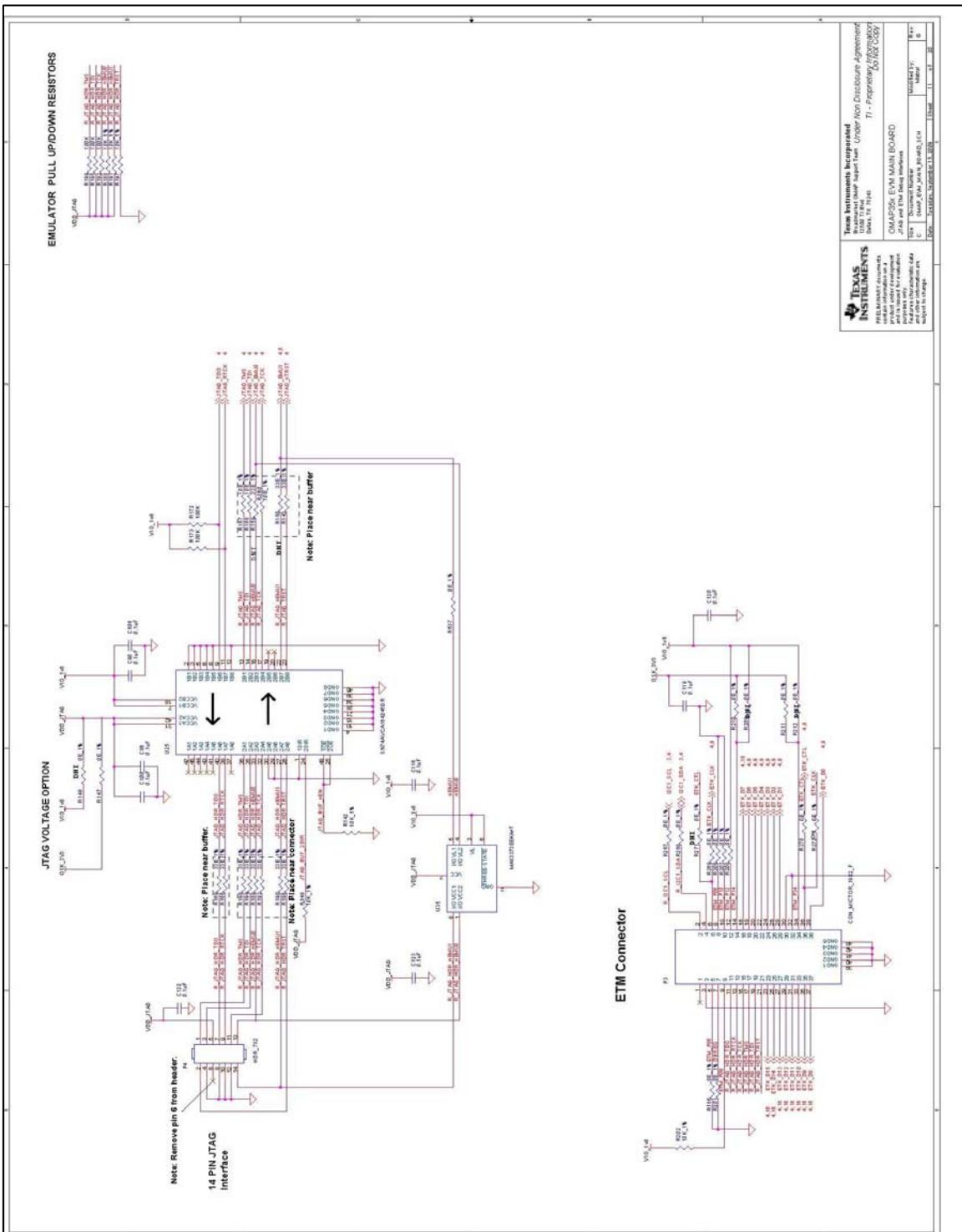


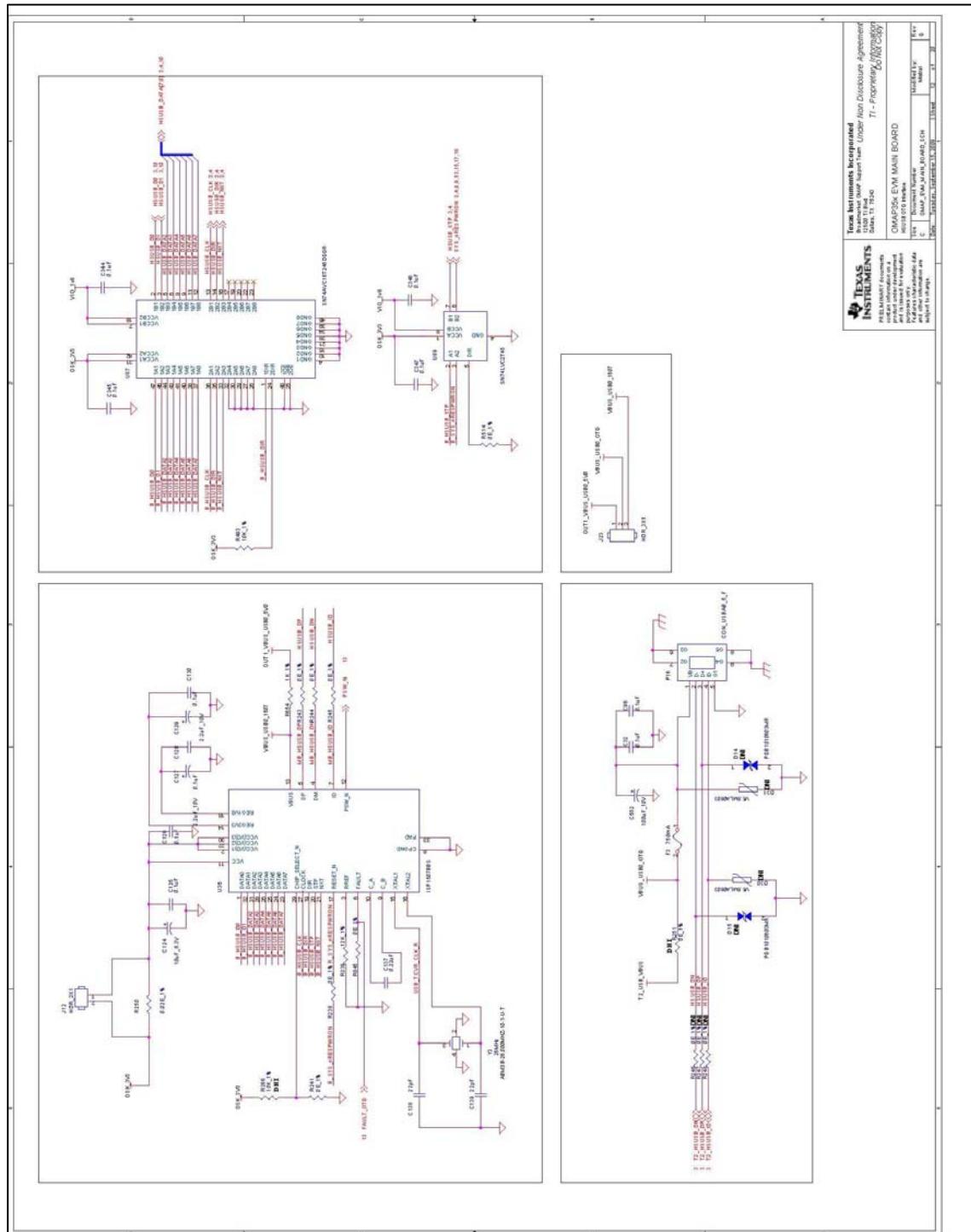


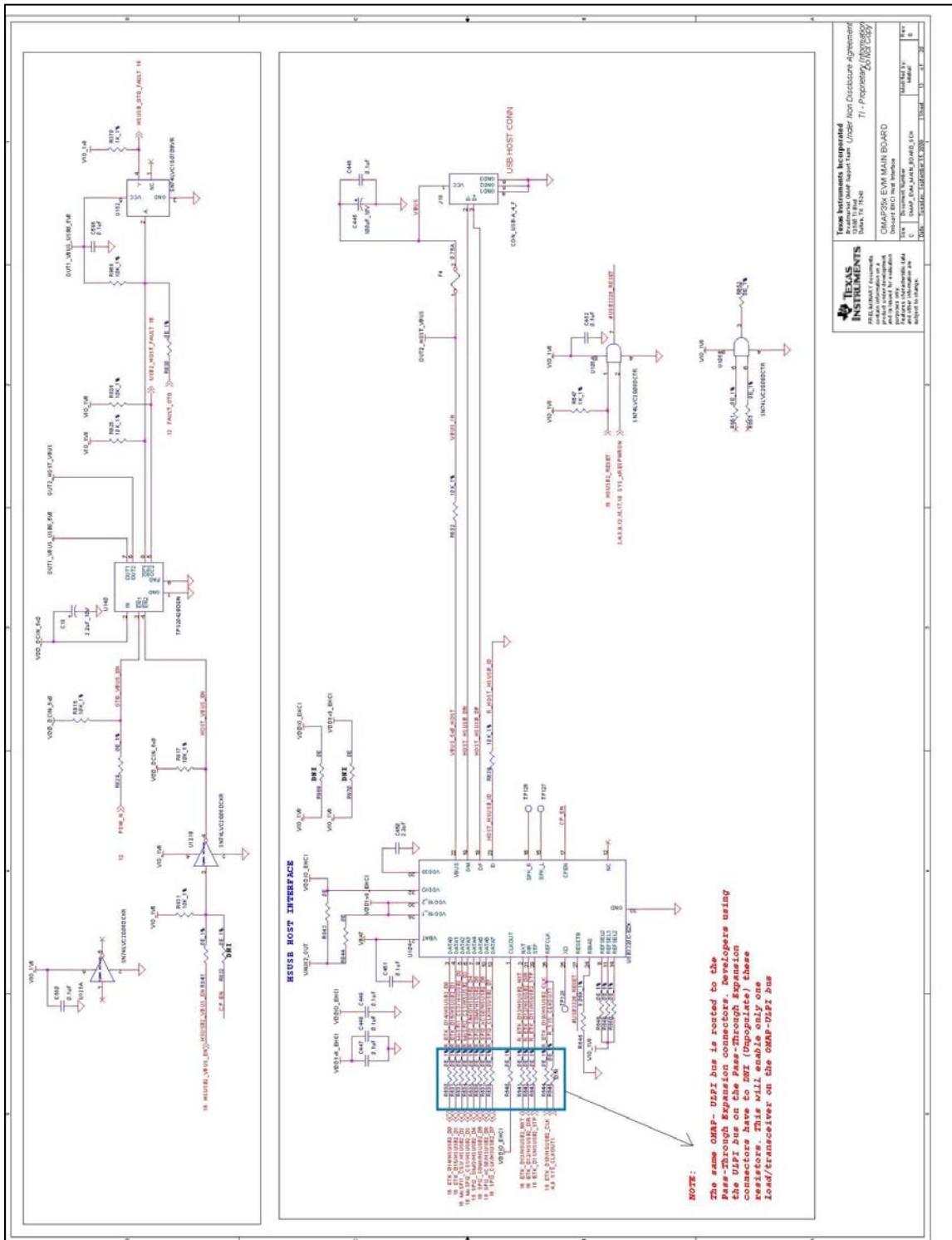




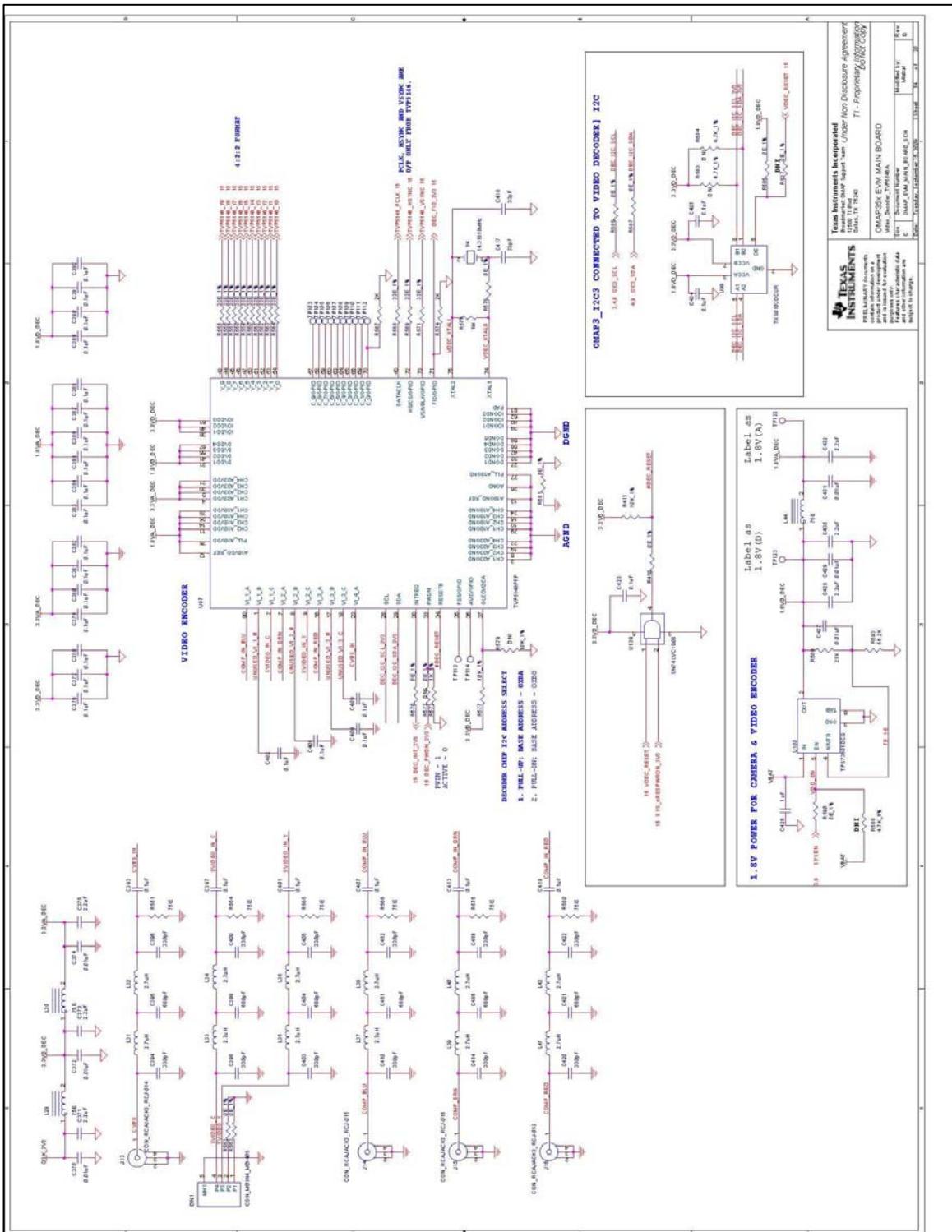


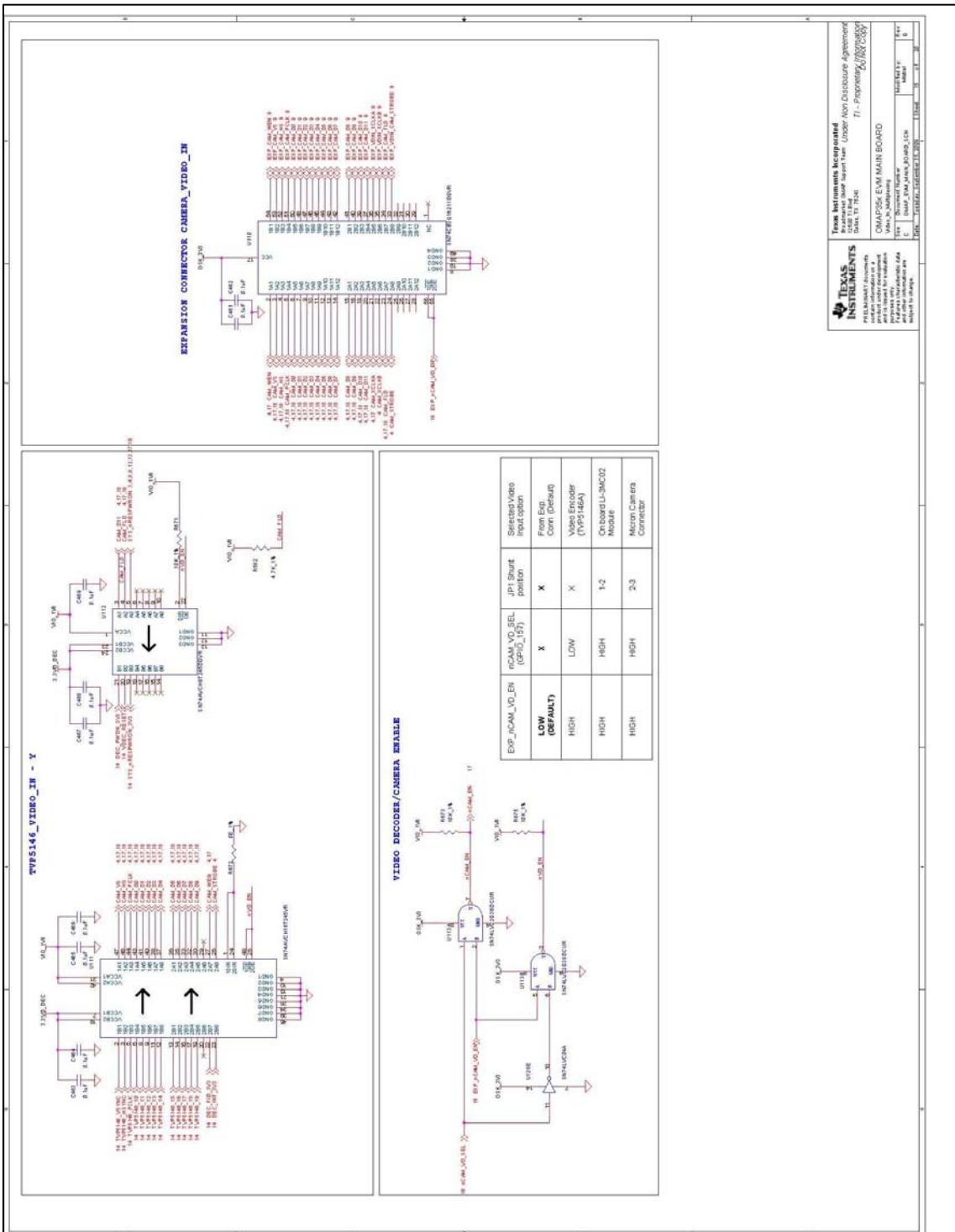


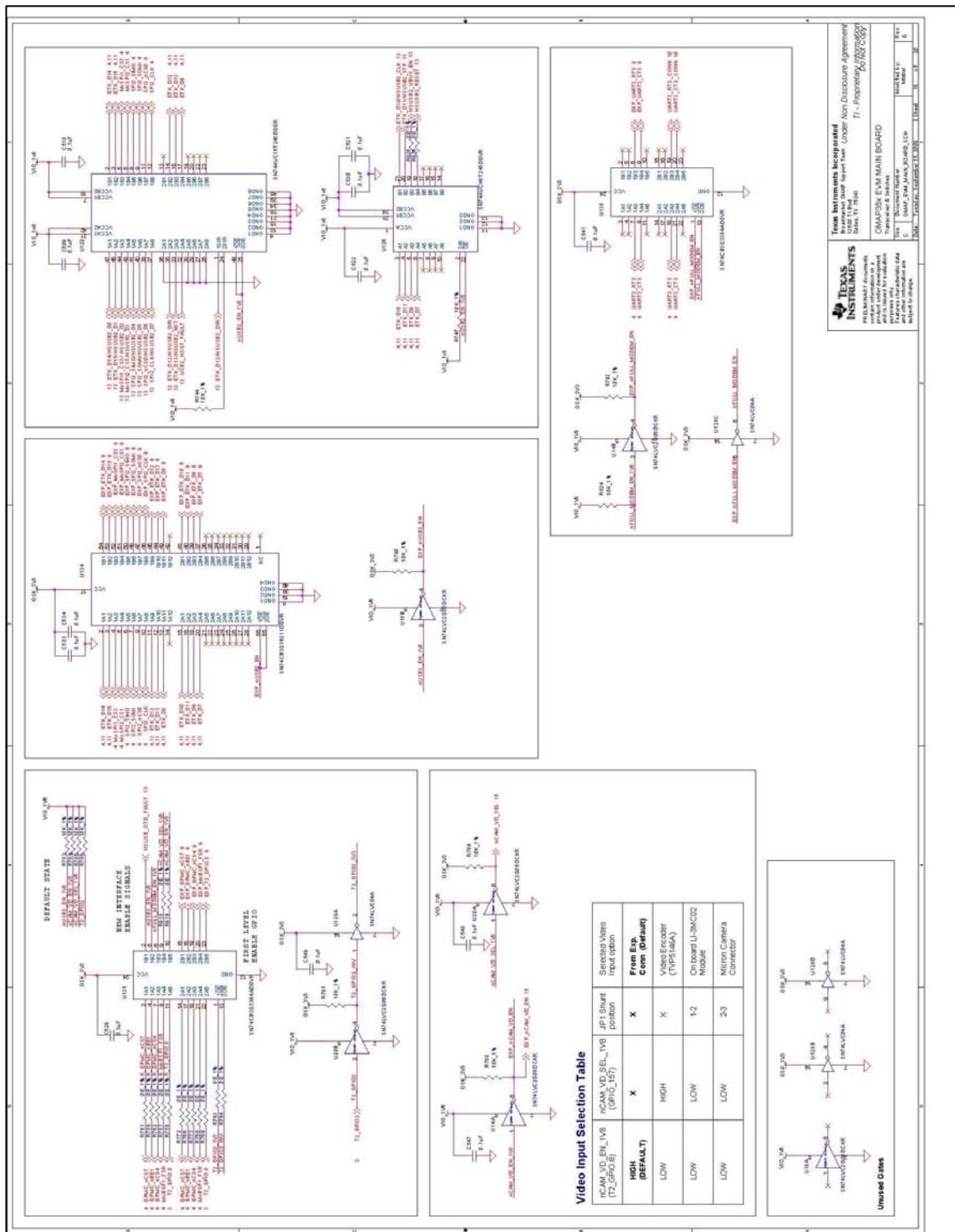


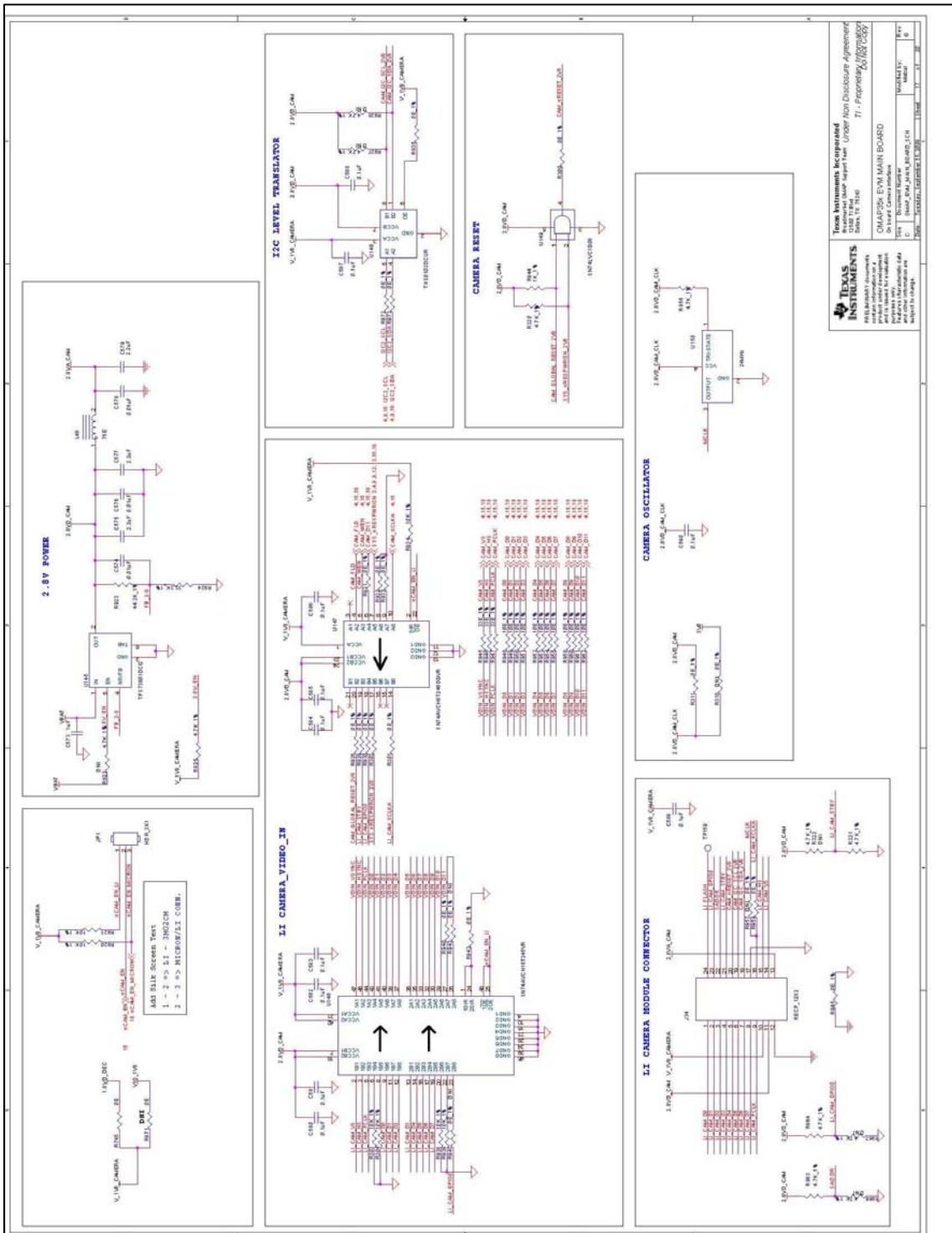


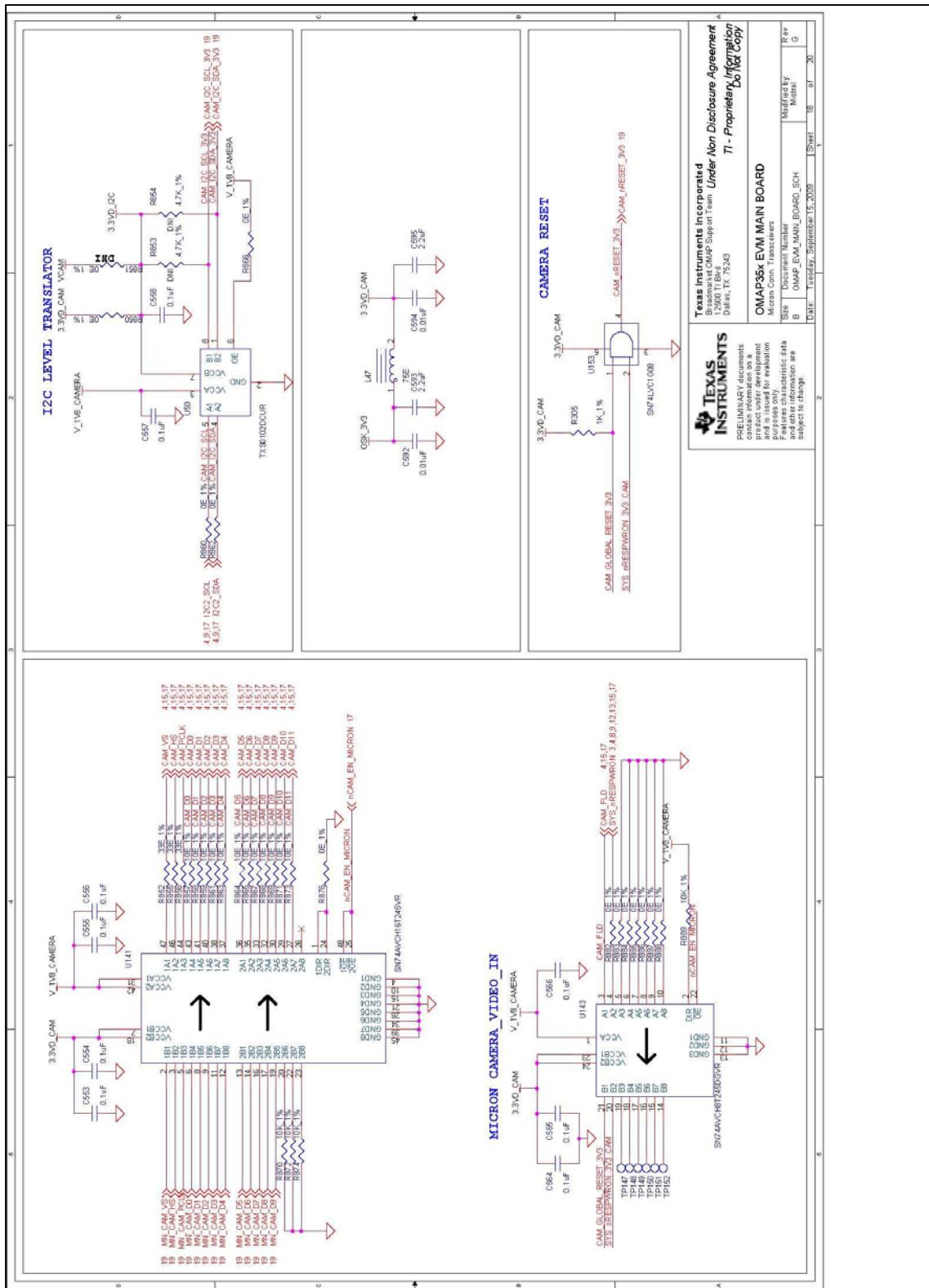
NOTE: The same GMANP-U2P bus is routed to the GMANP-Phase-Through Expansion connector. Developers using the U2P bus on the Pass-Through Expansion connectors have to DNI (Duplicate) these connectors. This will enable only one receiver. This will enable only one receiver. This will enable only one receiver.

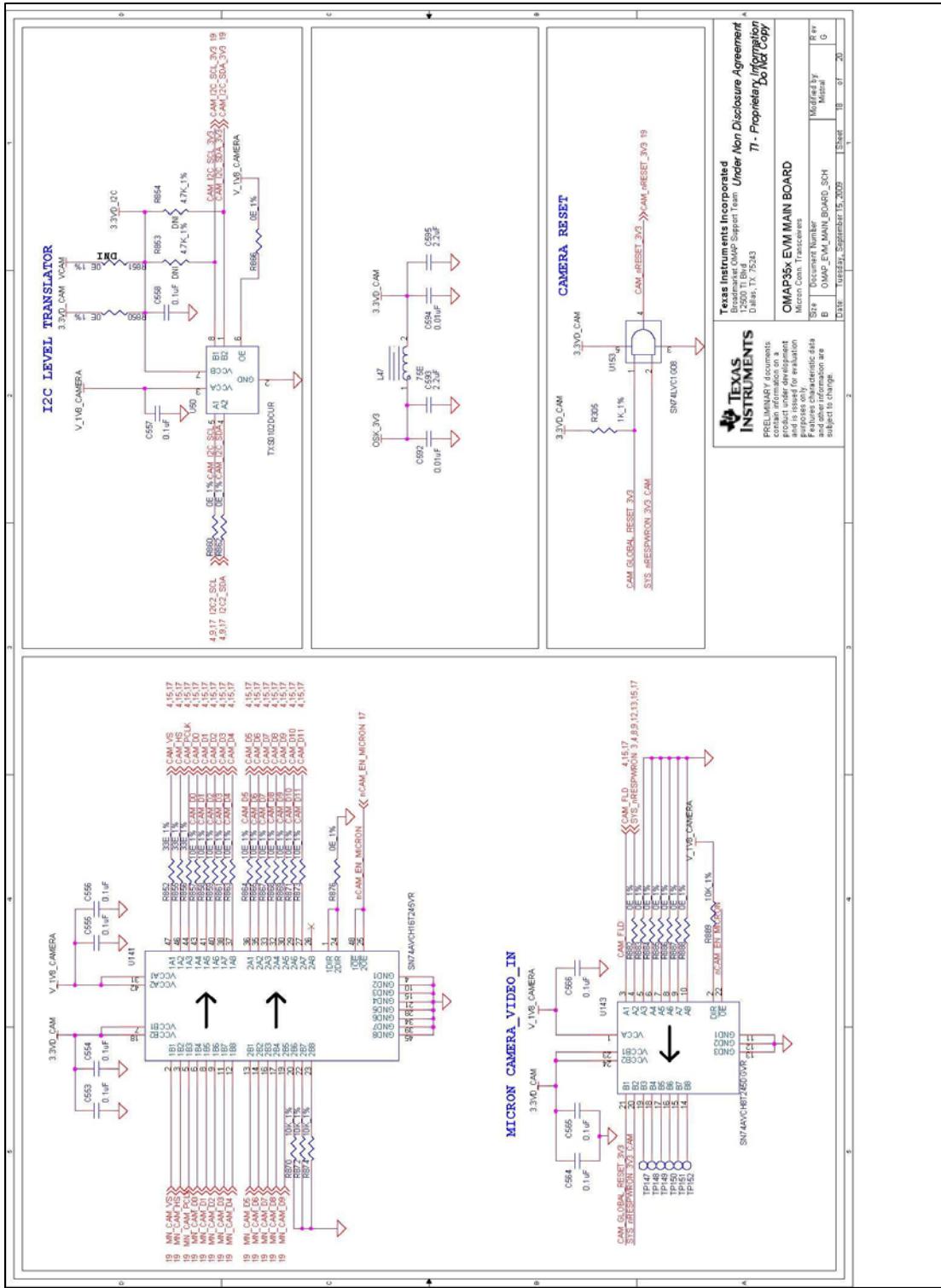


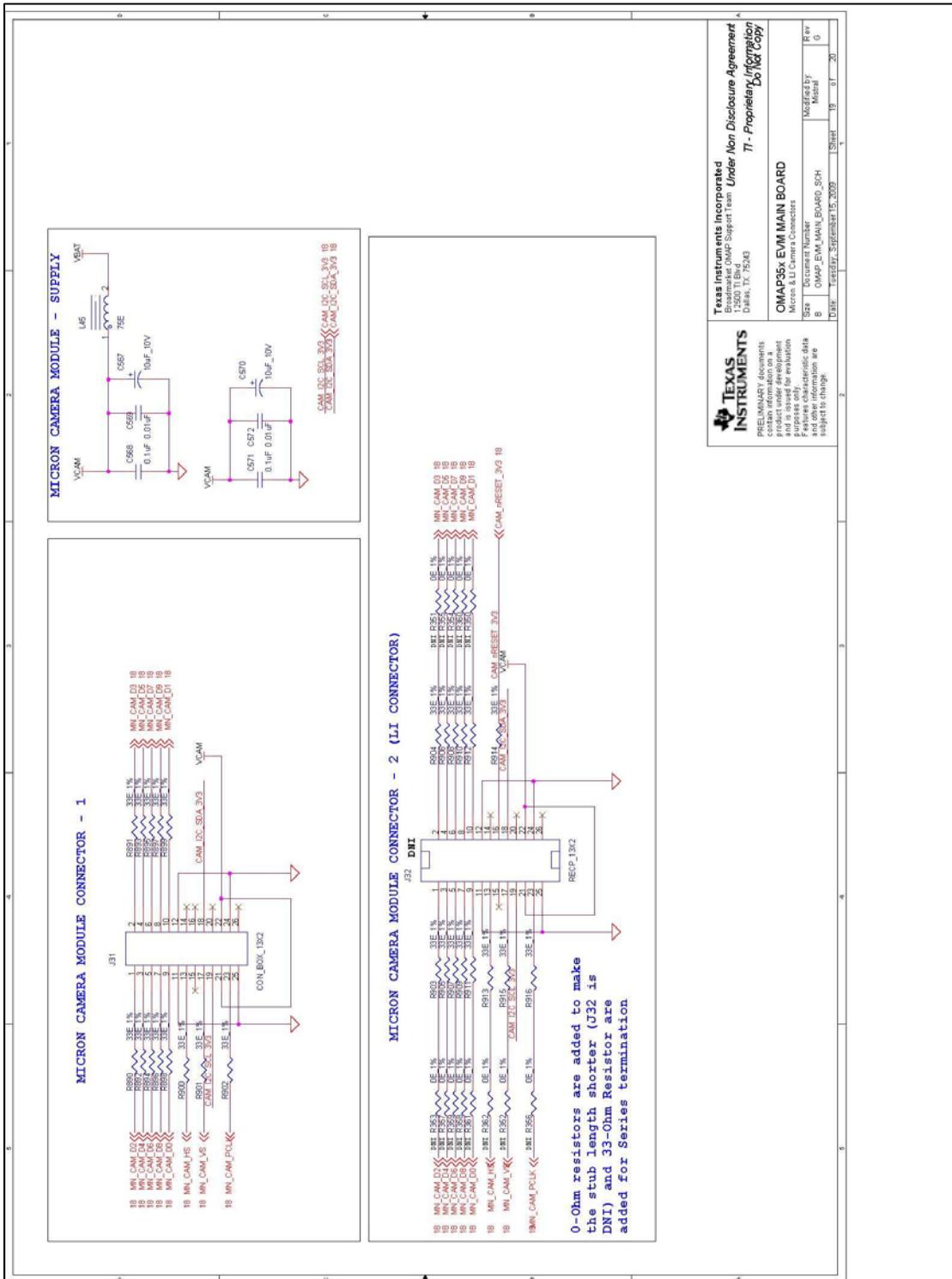


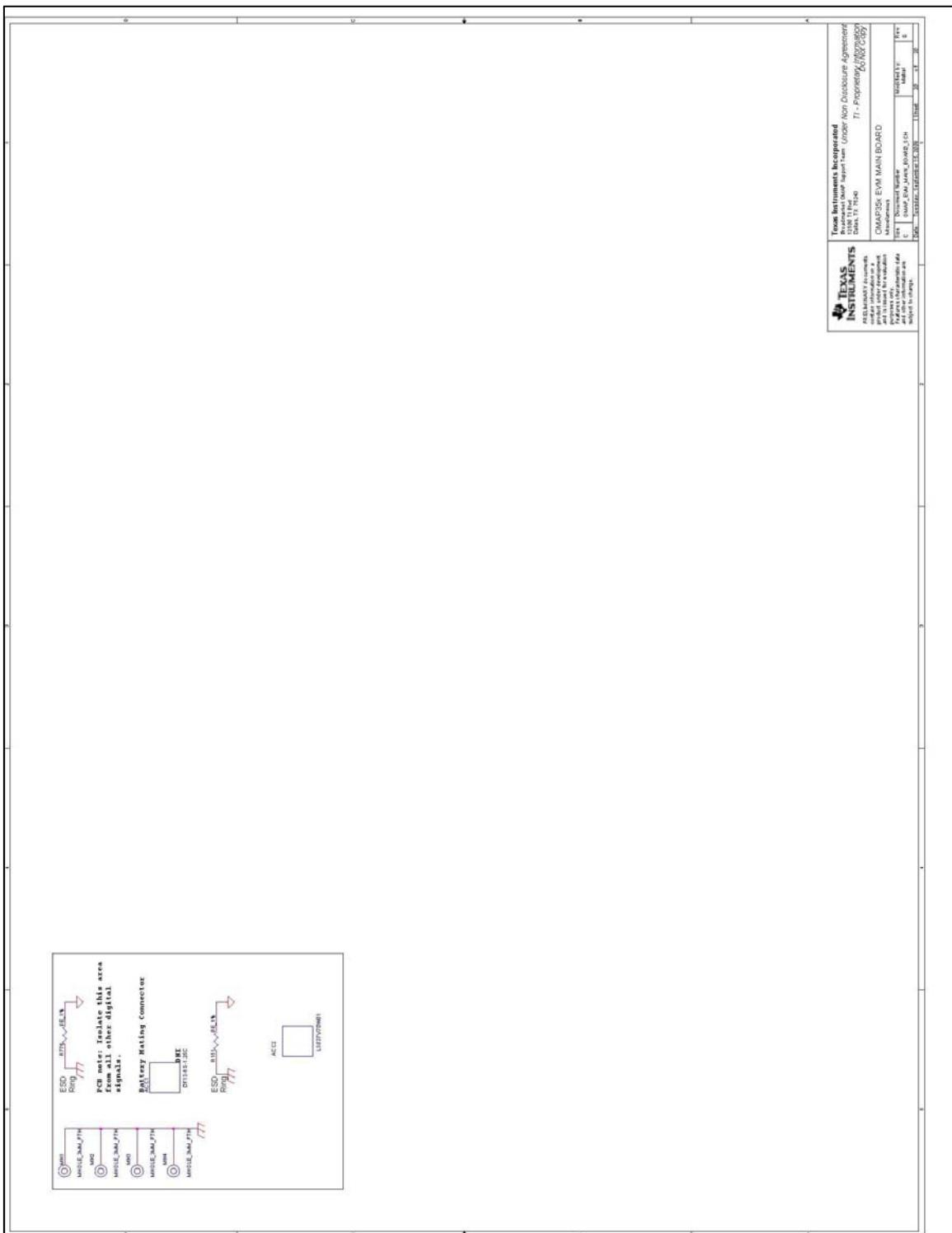










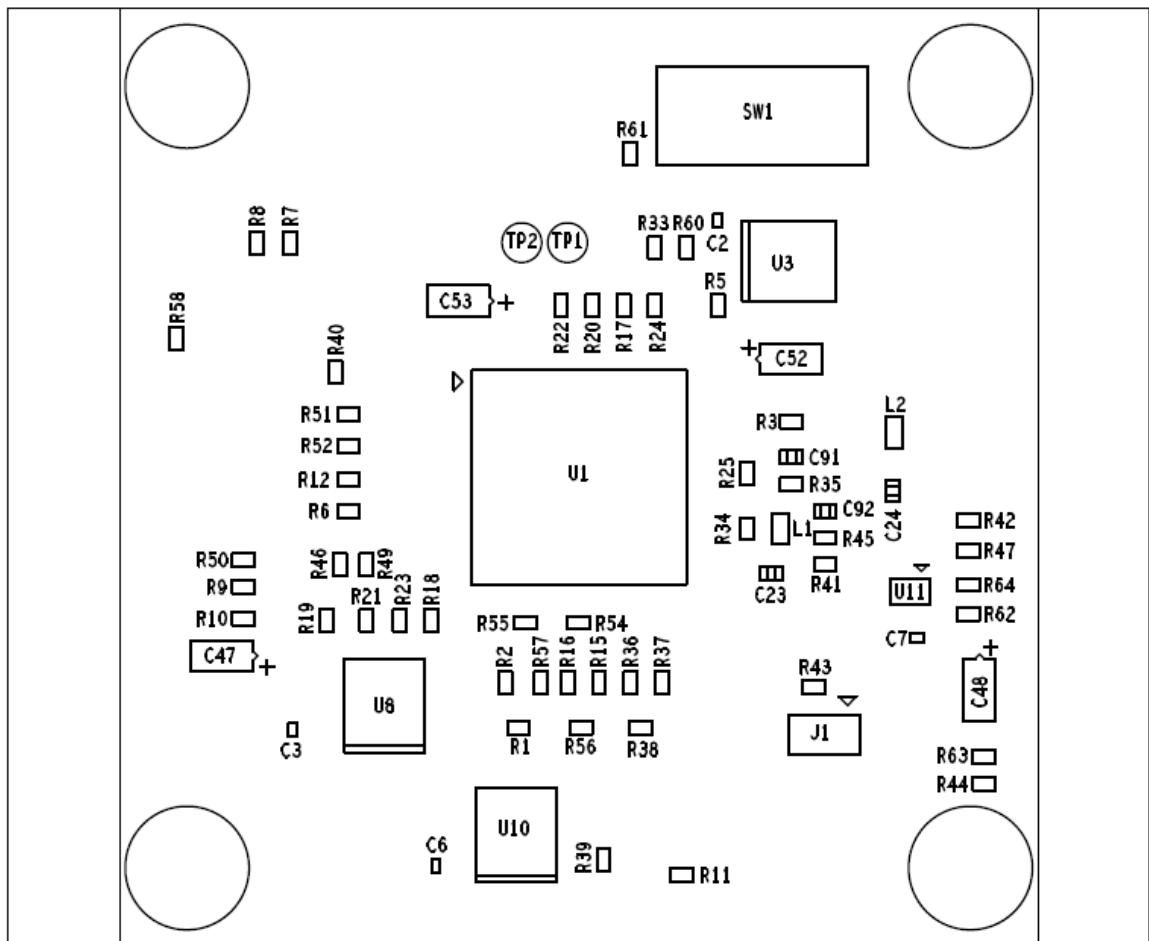


Appendix B

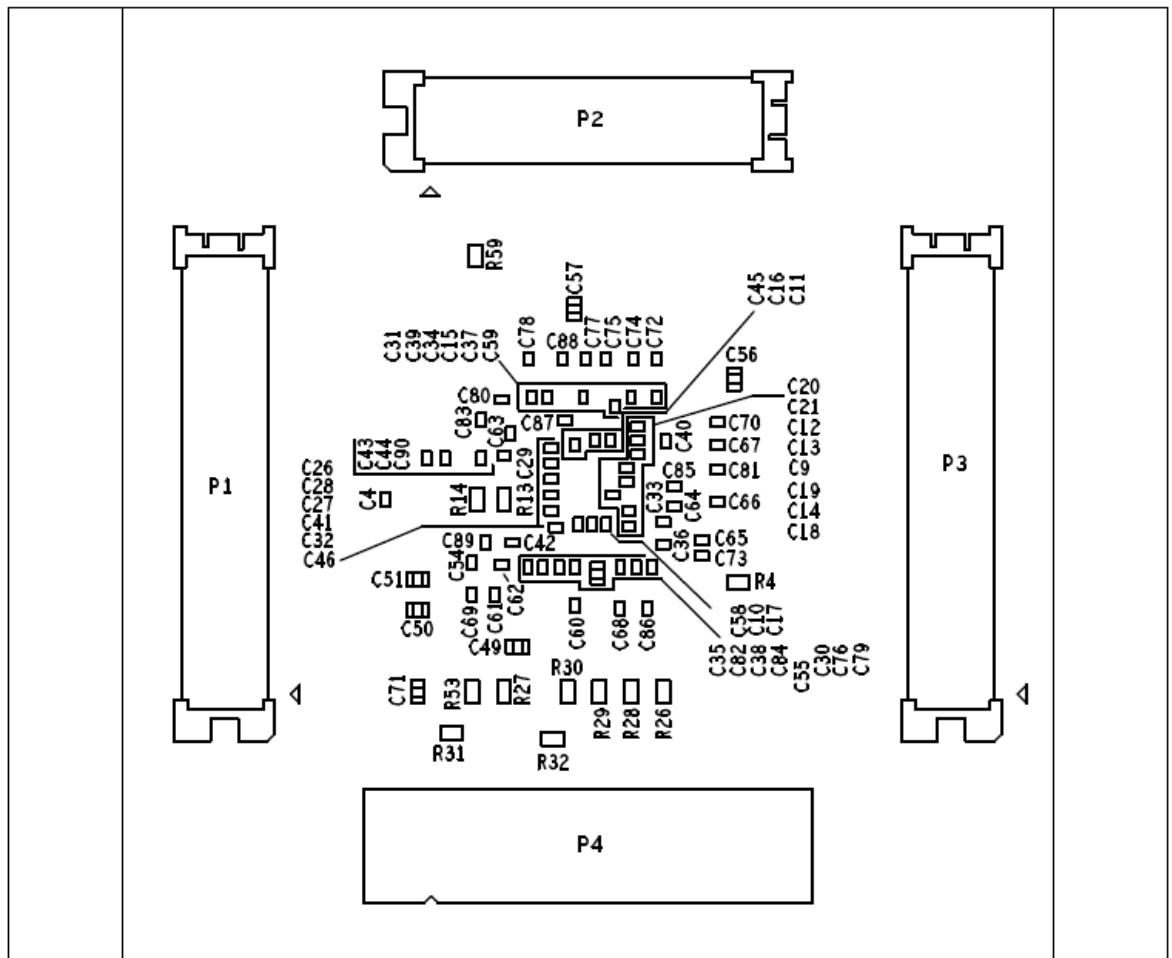
Mechanical Information

This appendix contains the mechanical information about the OMAP35x EVM.

OMAP Processor Module Layout

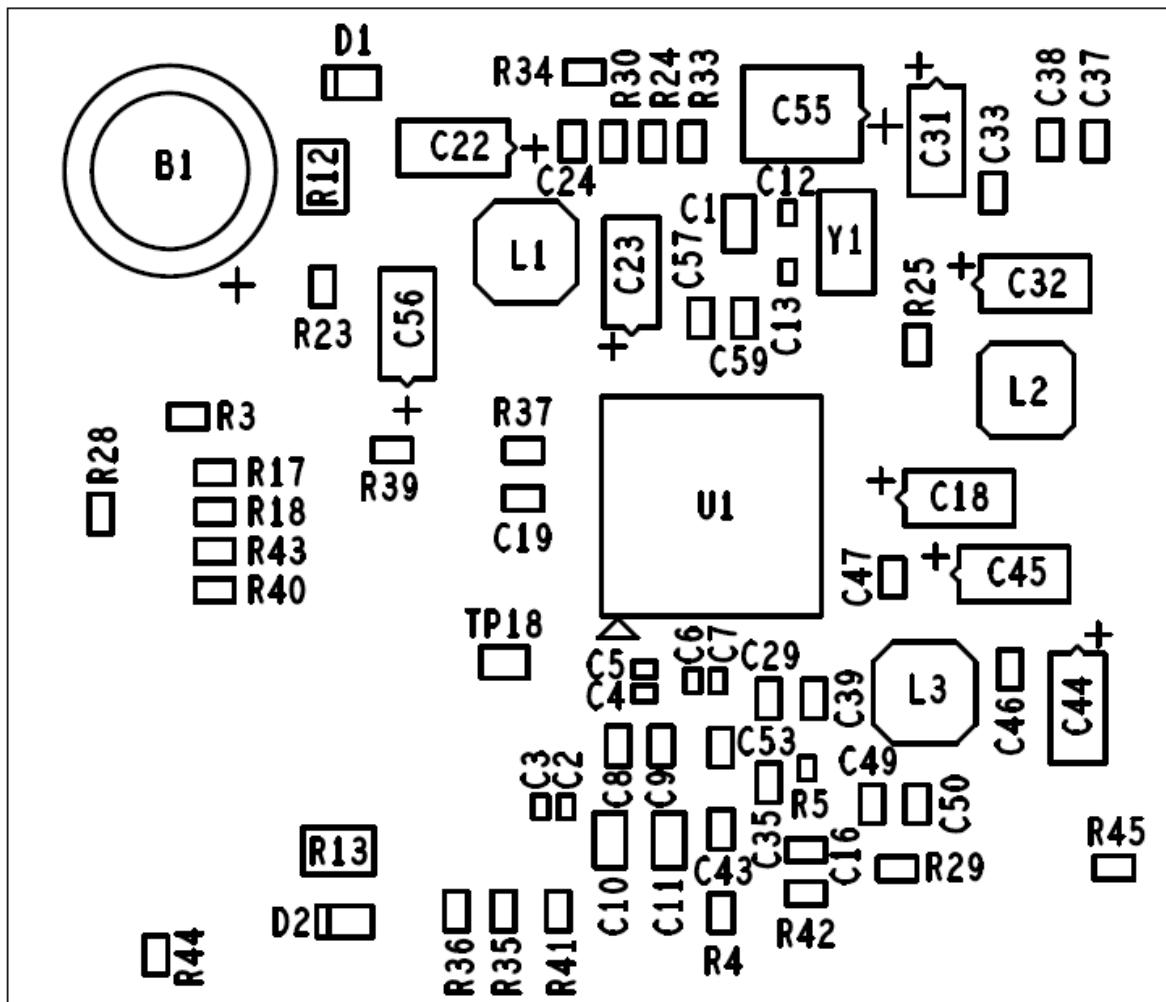


OMAP Processor Module Layout

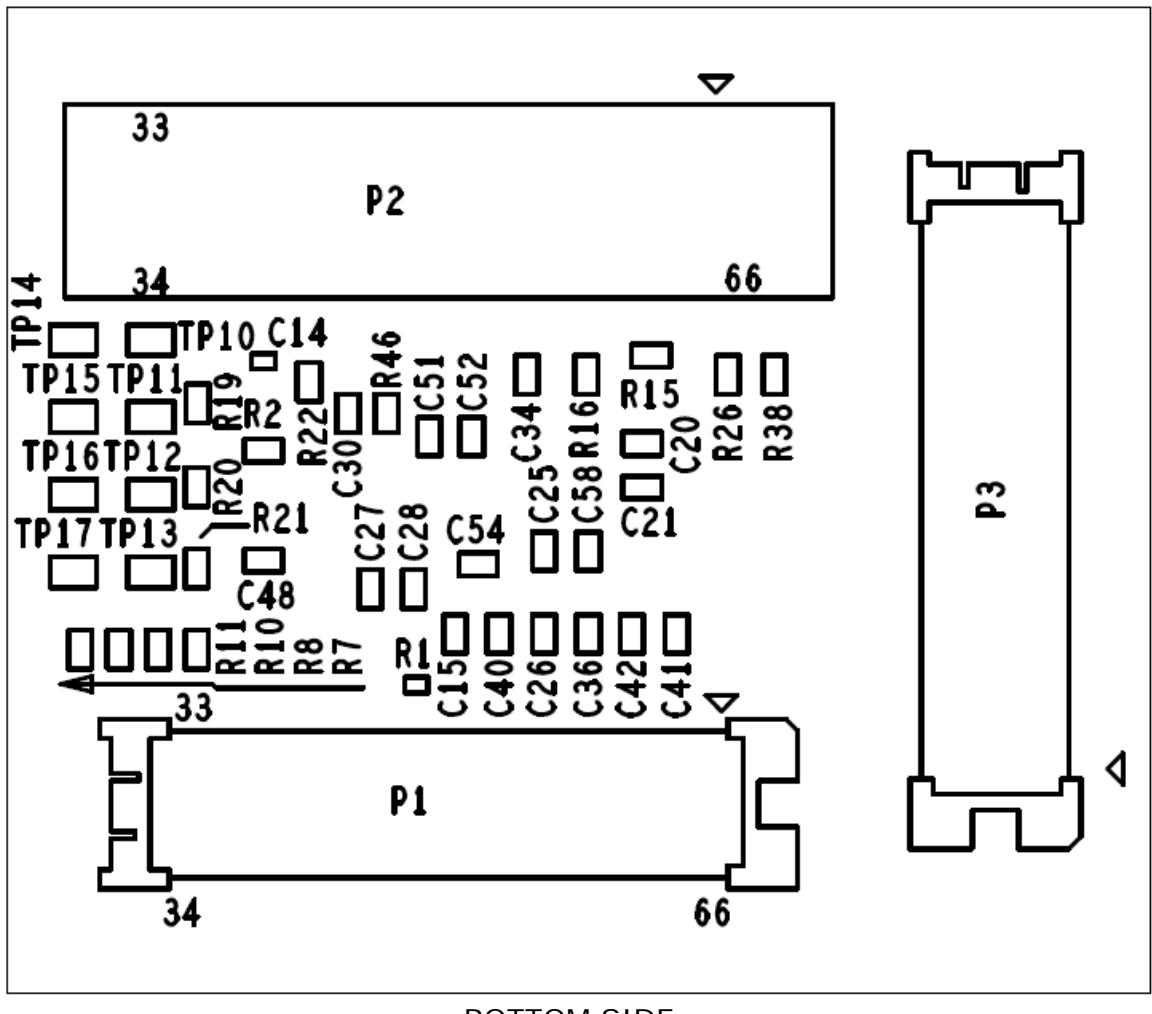


ASSEMBLY DRAWING BOTTOMSIDE

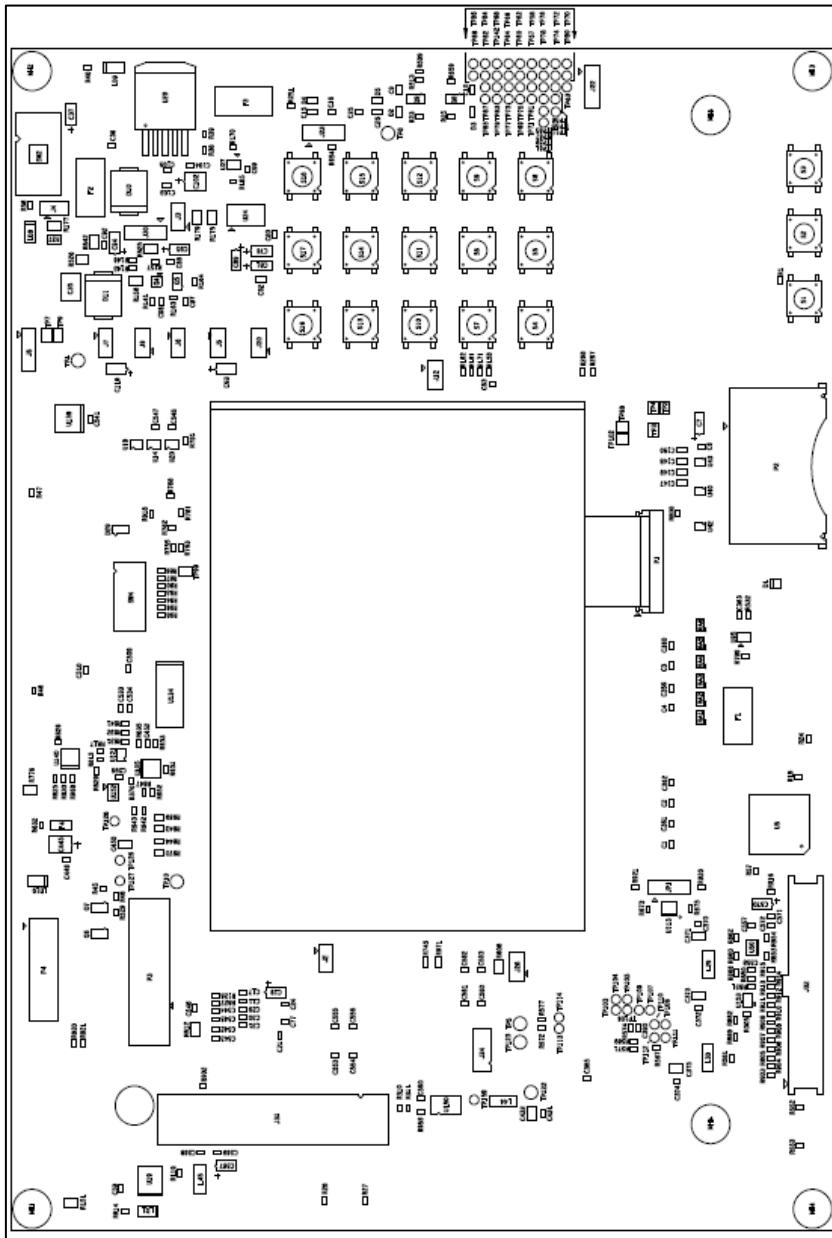
Power Module Layout



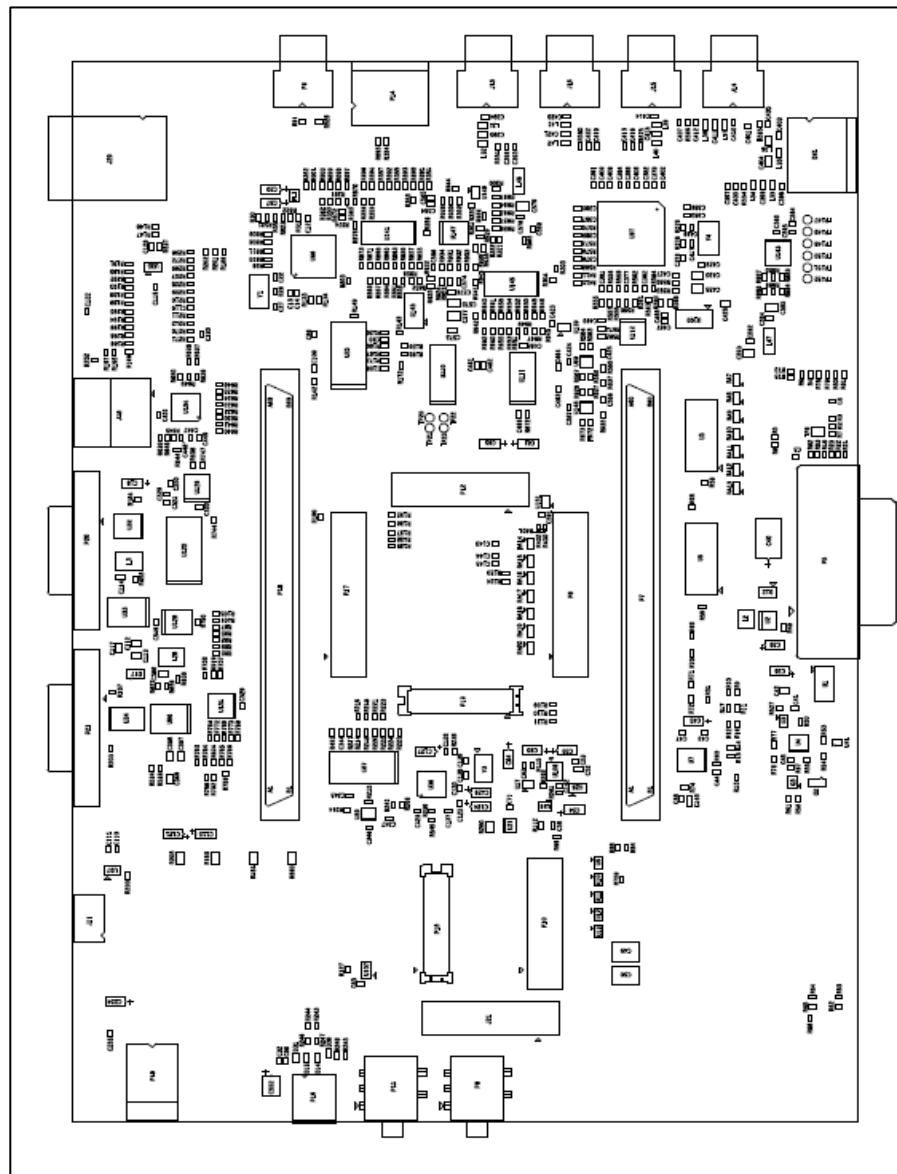
Power Module Layout



EVM Main Board Layout



EVM Main Board Layout



ASSEMBLY BOTTOM

Latest schematics & layout files can be downloaded from Mistral's website -
<http://www.mistralsolutions.com/assets/downloads/3530.php>

Acronyms

ADC – Analog to Digital Converter
AVID – Active Video ID
BGA – Ball grid Array
CCS – Code Composer Studio
DAC – Digital to Analog Converter
DDR – Double Data Rate
DIP – Dual-In Line Package
DSS - Display Subsystem
EEPROM – Electrically Erasable Programmable Read Only Memory
ESD - Electro Static Discharge
ETM – Embedded trace Macrocell
EVM – Evaluation Module
FID – Field ID
GPIO – General Purpose Input/Output
GPMC-General Purpose Memory Controller
I2C – Inter Integrated Circuit
JTAG – Joint Test Action Group
LCD – Liquid Crystal Display
LED - Light Emitting Diode
MAC – Media Access Controller
McBSP – Multi Channel Buffered Serial Port
NTSC – National Television Systems committee
OTG – On-The-Go
PAL – Phase Alternate Line
PCB – Printed Circuit Board
PCM – Pulse Coded Modulation
PHY – Physical Transceiver
POP – Package on Package
QVGA/VGA – Quarter Video Graphics Array
SD/MMC – Secure Digital/Multi Media Card
SDRC – SDRAM Controller
SDRAM – Synchronous Dynamic Random Access Memory
SPI – Serial Peripheral Interface
SPDT – Single Pole Double Throw
UART – Universal Asynchronous Receiver Transmitter
USB – Universal Serial Bus



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