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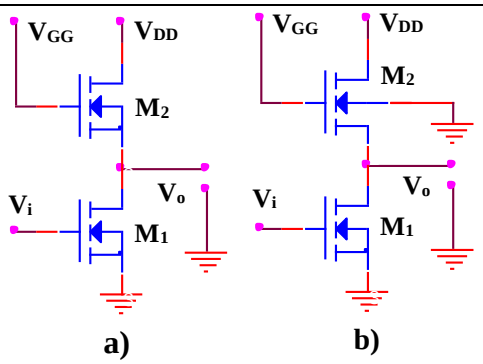
Report: NMOS Integrated Circuits

NMOS static inverter

Code:

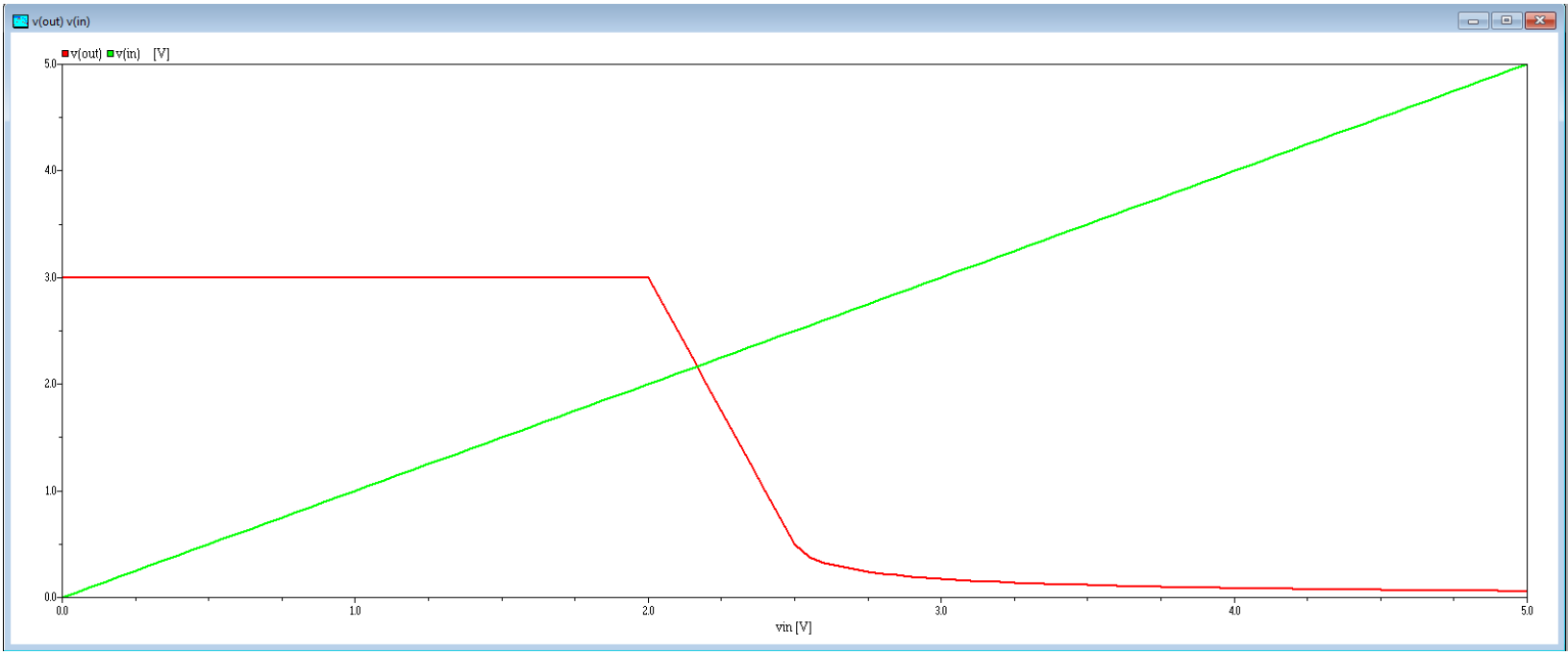
```
M1 OUT IN 0 0 NMOS1 W=1u L=1u
M2 VDD VGG OUT OUT NMOS1 W=1u L=25u
.MODEL NMOS1 NMOS VTO=2

C1 OUT 0 15e-12
VGG VGG 0 5
VDD VDD 0 3

*Circuit a)
```



Due to using NMOS transistors, the gate of M2 must be at a higher voltage than the drain, therefore, VGG was set to VDD+VTO=5v.

Circuit a)

DC Analysis (Vin = 0..5V):



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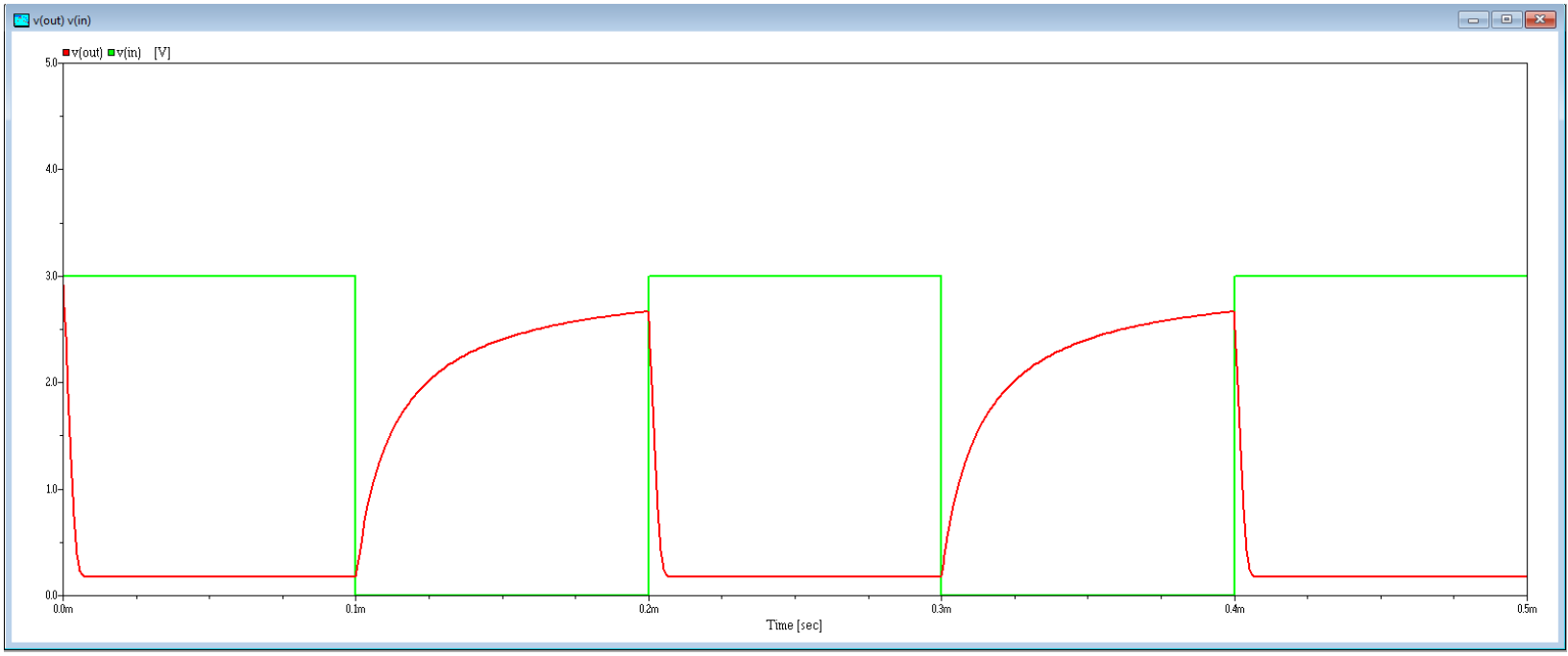
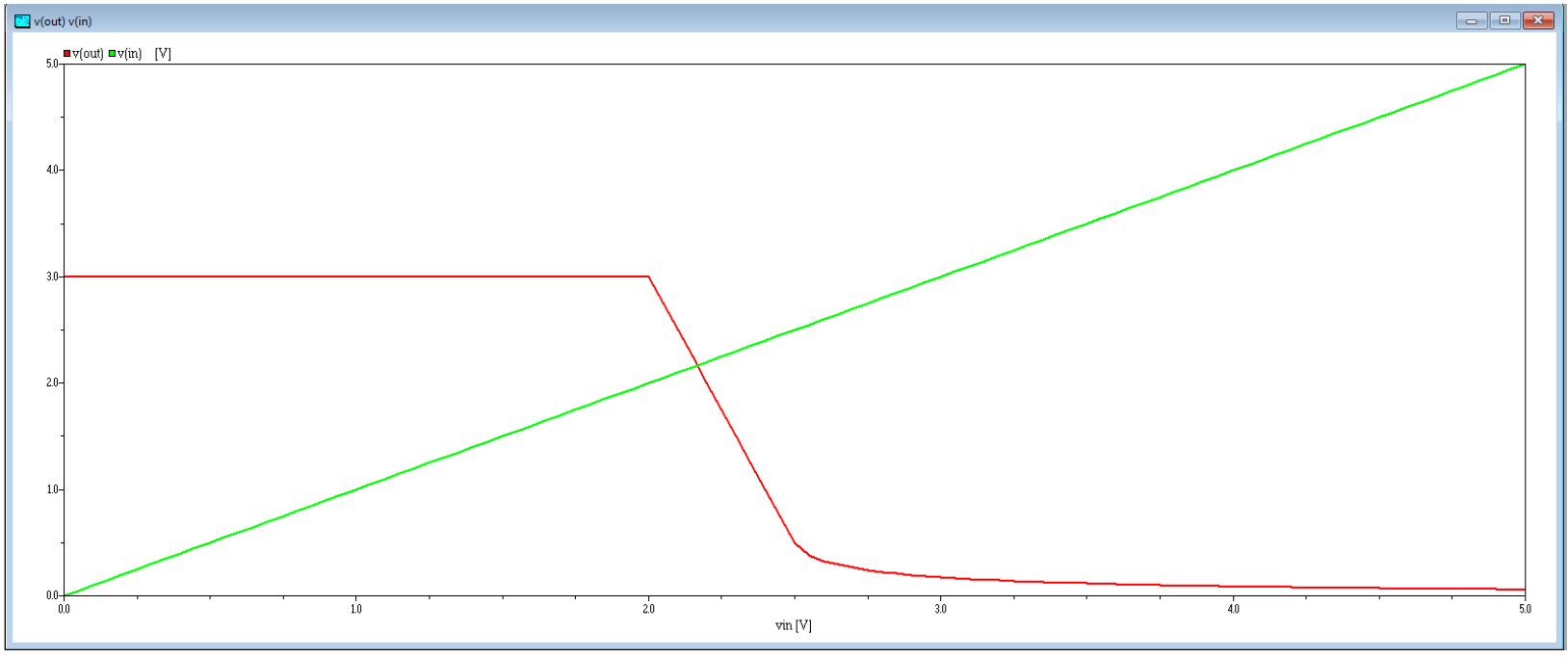
Transient Analysis (Vin = PULSE (0 3 0 1e-10 1e-10 1e-4 2e-4)):



Circuit b)

DC Analysis (Vin = 0..5V):



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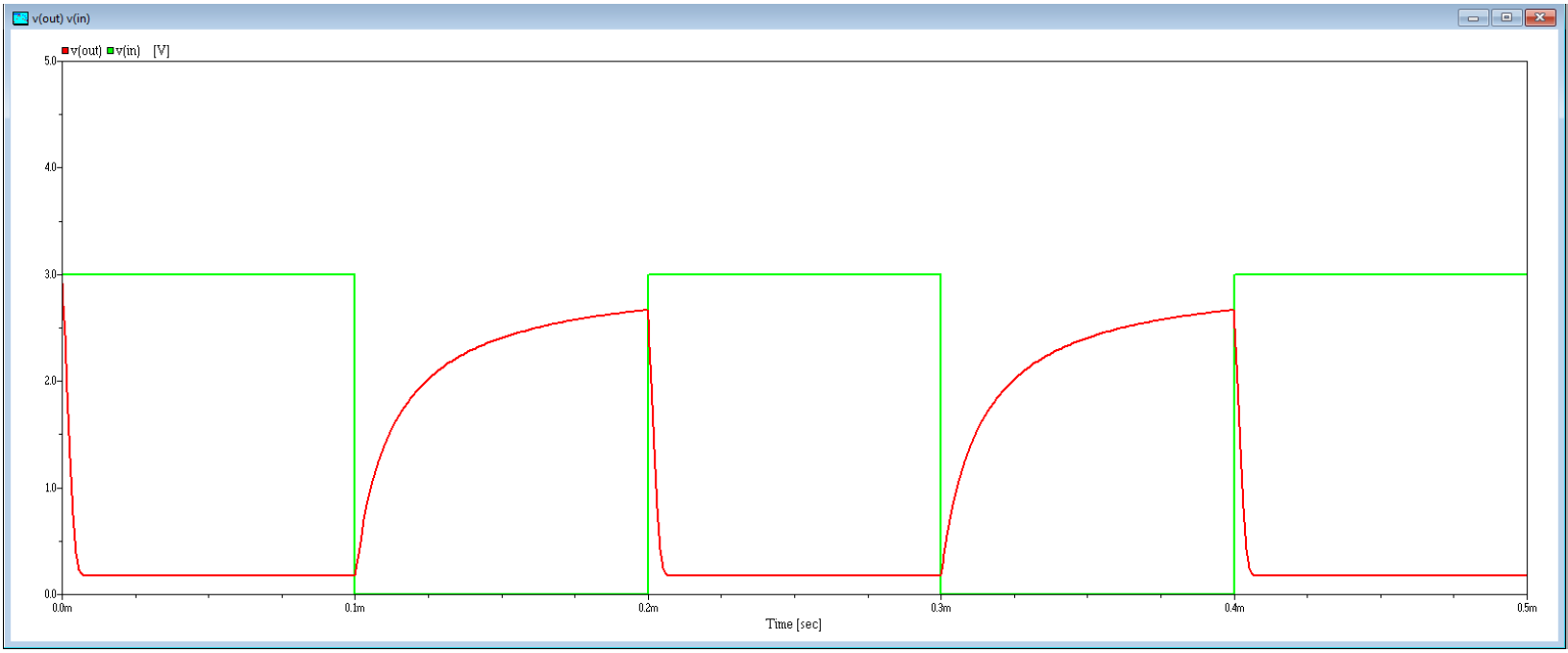
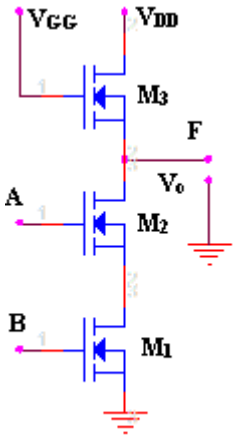
Transient Analysis (Vin = PULSE (0 3 0 1e-10 1e-10 1e-4 2e-4)):



NMOS static NAND gate

Code:

NAND NMOS M1 OUT A N1 N1 NMOS1 W=1u L=1u M2 VDD VGG OUT OUT NMOS1 W=1u L=50u M3 N1 B 0 0 NMOS1 W=1u L=1u .MODEL NMOS1 NMOS VTO=2 C1 OUT 0 15e-12 VGG VGG 0 5 VDD VDD 0 3	 Fig.4.3

Due to using NMOS transistors, the gate of M3 must be at a higher voltage than the drain, therefore, VGG was set to VDD+VTO=5v.

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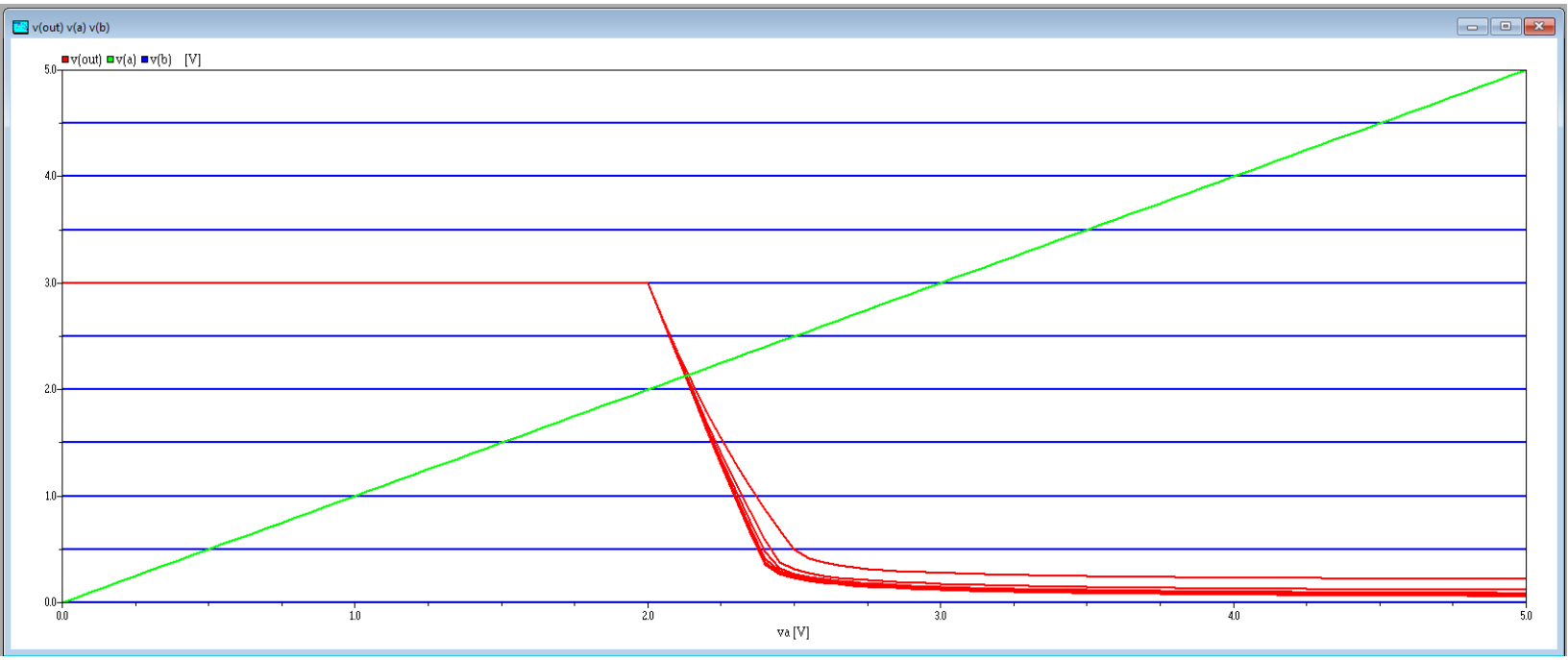
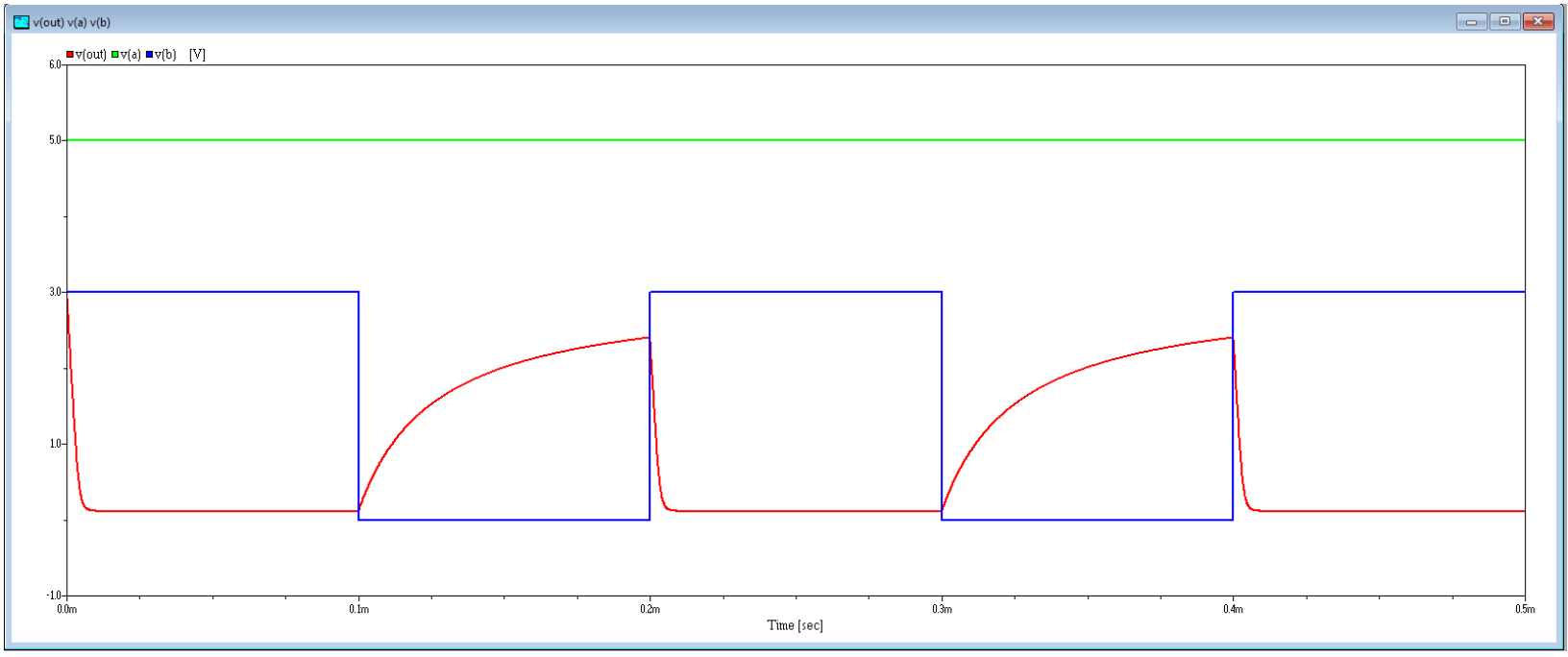
DC Analysis (Vin = 0..5V):



Transient Analysis (Va=5v Vb = PULSE(0 3 0 1e-10 1e-10 1e-4 2e-4)):



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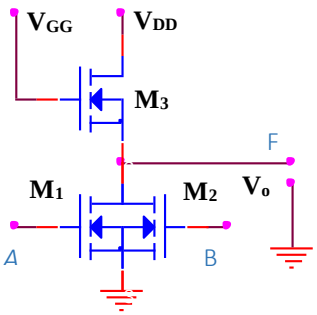
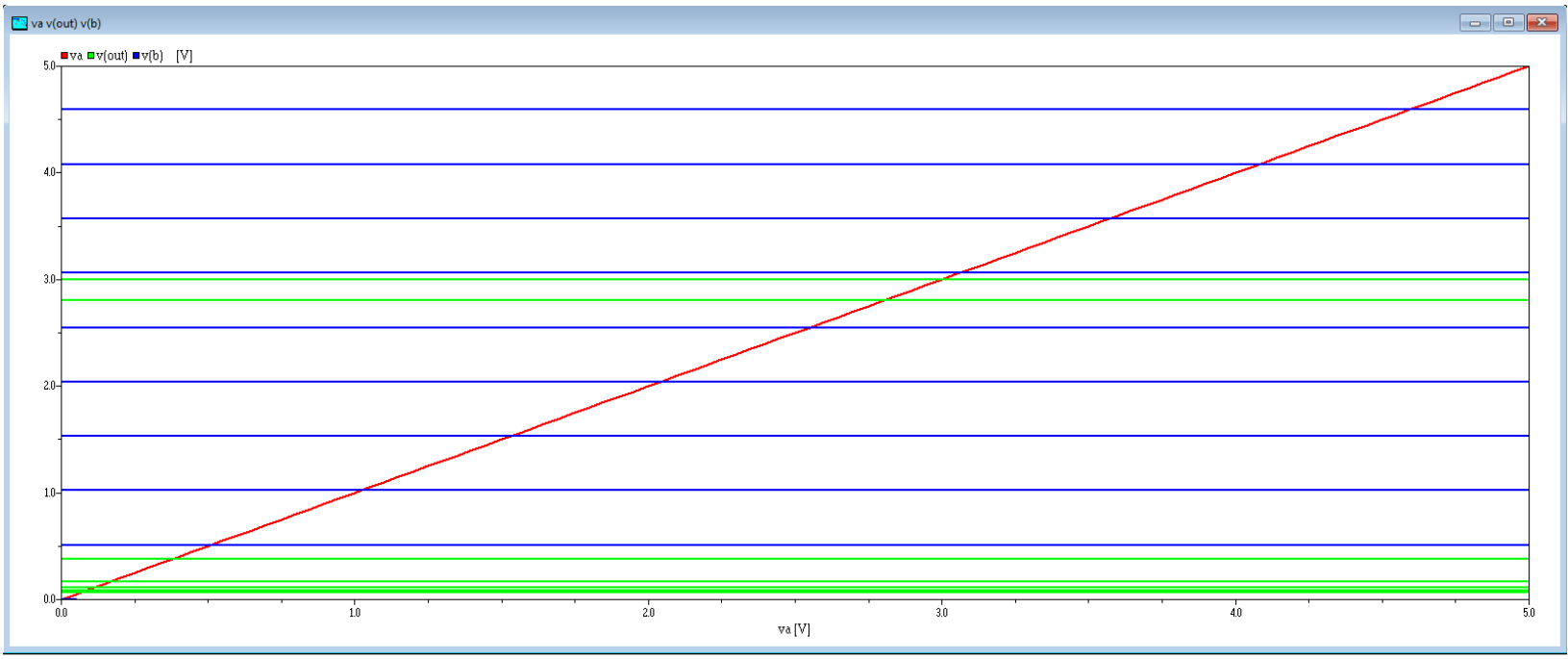
NMOS static NOR gate

Code:

NOR NMOS M1 OUT A 0 0 NMOS1 W=1u L=1u M2 VDD VGG OUT OUT NMOS1 W=1u L=25u M3 OUT B 0 0 NMOS1 W=1u L=1u .MODEL NMOS1 NMOS VTO=2 C1 OUT 0 15e-12 VGG VGG 0 5 VDD VDD 0 3	 **Fig.4.4**

Due to using NMOS transistors, the gate of M3 must be at a higher voltage than the drain, therefore, VGG was set to VDD+VTO=5v.

DC Analysis (Vin = 0..5V):



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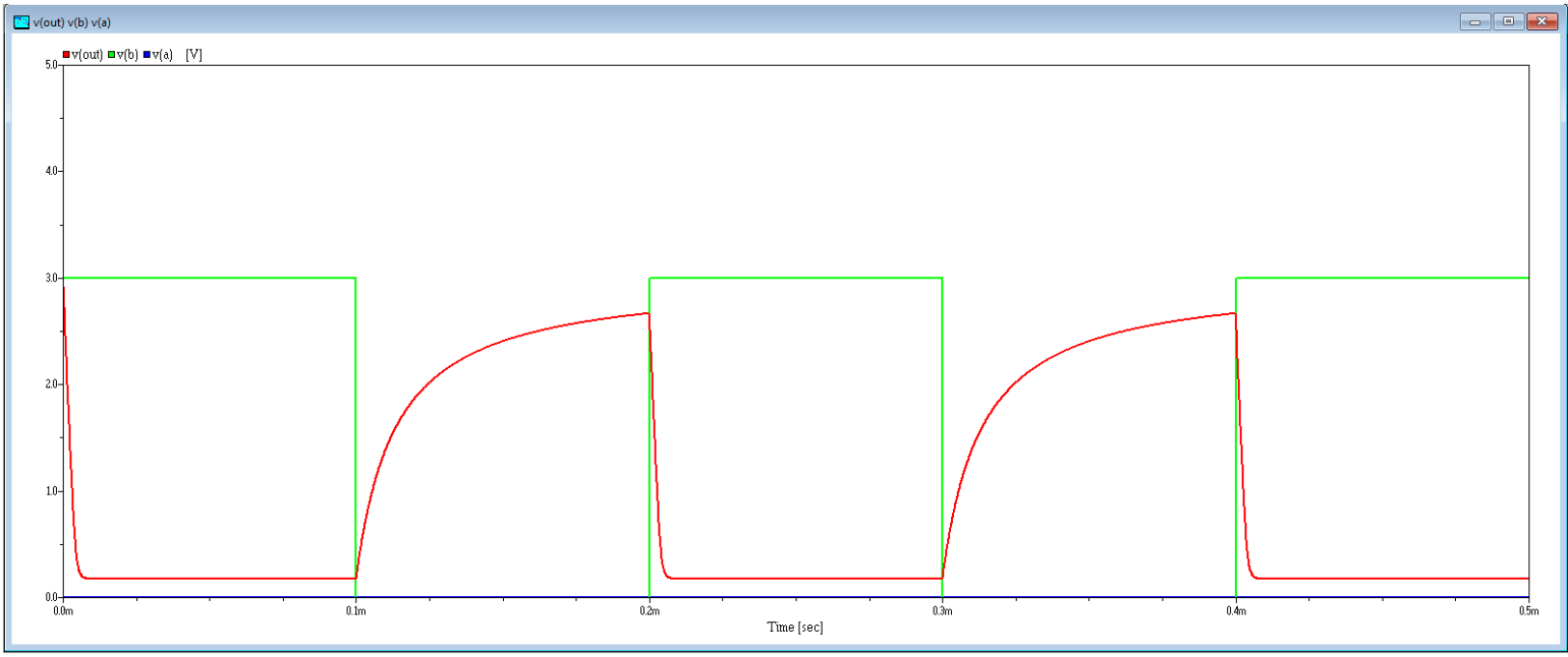
Transient Analysis (Va=0v Vb = PULSE(0 3 0 1e-10 1e-10 1e-4 2e-4)):



Personal remarks:

The NMOS implementation of the logic gates, although not complicated, looks to me as being an unnecessary hassle compared to the CMOS counterpart, especially considering today's advancement in technology. Despite CMOS being a tad slower due to the PMOS section, its implementation seems simpler, not needing a voltage boost section or a higher power supply voltage in order to achieve the same output voltage.

When simulated, supplying the same 3V to both the Vgg and Vdd connections, the current consumption increases slightly (from 0.3uA to almost 0.4uA) , as well as the output voltage swing being reduced by 2V, which is the threshold voltage. The output voltage difference is also observable on a breadboarded circuit, but I had no way of measuring current draw accurately, so I cannot comment on this aspect. I have used FQP30N06L N-FETs as I had a bunch laying around. They were matched as closely as possible, having a (measured) gate threshold voltage between 2.03 and 2.09V, hence the chosen value of VTO in all the previously ran simulations.