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IELET2121 - POWER ELECTRONICS

Design of a Boost Converter

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PROBLEM DEFINITON

In this report, the group are desigining an AC-DC rectifier with a boost-converter. The input voltage is $230V_{rms}$, and the output voltage is going to be 385 V DC. The output voltage ripple has to be maximum 5%, which means that it should be between 375 and 394 volts in all stable conditions. The output ripple should be maximum 1 A, which sets some demands for the inductor size. The group has to calculate what the active and passive components' characteristics needs to be, and choose components from the given alternatives according to this. The rectifier has to be able to deliver an output current of $10A_{DC}$. It shall also work according to the demand when the load is down to 20%(2 A). The design has to be simulated in Simulink to show that the demands are fulfilled. The power-losses of the inductor, capacitors, MOSFET and diodes has to be calculated at steps from 20-100% to find the efficiency. The duty cycle of the PWM-signals has to be regulated to keep the voltage at 385 V when the load changes.

Design criteria:

Parameter	Requirement
Input voltage	$230_{rms}@50Hz$
Output voltage	$385V_{DC}$
Max output current	$10A$
Output voltage ripple	5%
Max. inductor current ripple	$1A_{peak-peak}$
Input voltage ripple	4%
Ambient temperature	$25°$

Table I: Converter design parameters

The design of the converter must enable it to function within a 20-100% range of its maximum load capacity, while operating in the continuous conduction mode (CCM) throughout this entire range.

The switching frequency of the MOSFET is set to be $65kHz$

ABSTRACT

This project involves the design and simulation of a boost converter, a type of power electronics circuit used to increase the voltage of a DC power source. The design process includes selecting appropriate components such as the inductor, capacitor, and switch, as well as determining the optimal operating conditions. The simulation is performed using *LTspice* and *Simulink* to analyze the behavior of the circuit under different load conditions. For controlling the circuits voltage and current levels, the chosen components are a Si-FET transistor and five SiC-diodes. The chosen capacitors is one 10 mF 350 V electrolytic capacitor and a 12 μF 500V fast-switching solder pin capacitor. The inductor is designed to have an inductance of $874\mu F$. The circuit's duty cycle is controlled with a PI-regulator, with the values $K_p = 0.3, K_i = 40$. The calculated efficiency is 99%.

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I. Introduction

In today's society, electric energy is a vital component to peoples life, both when it comes to transport, communication and activities. Because of the ever lasting increase of energy consumption, and the introduction of technical devices like smartphones, computers and electrical vehicles, there is a need for well-designed "power electronics"-devices. These devices is also a component in the "green shift", since renewable energy sources like solar power needs to be inverted into AC.

One of the most used devices is the AC-DC-rectifier, and also voltage converters such as boost-converters, which can increase the voltage of a DC-source. In this project, the group has combined these two devices into a one devices, and has designed a $230V_{AC}$ to $385V_{DC}$ converter. To be able to do this, there is two main stages; Designing the AC-DC-rectifier, and then design the boost-converter. The rectifier consists of 4 diodes connected in a "H-bridge", which makes the sine-wave from AC to a high-ripple DC-voltage. A correctly chosen capacitor will then flatten out the large voltage variation according to what the demands are. The result is a DC-like voltage with a small ripple and voltage level close to V_{peak} of the AC-voltage.

The second part of the product is the "boost-converter". This part consists of an inductor for stabilizing the output current, and a capacitor in parallell with the load, designed to keep the voltage ripple below the desired level. The ripple, both in the inductor and the capacitor, comes from the constant switching of the MOSFET transistor

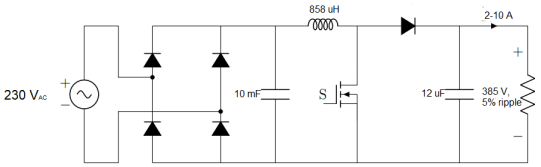

Figure 1: A full-bridge rectifier combined with a boost-converter

Figure 2 shows how the output voltage ideally should be compared to the input voltage. This is only an illustration figure.

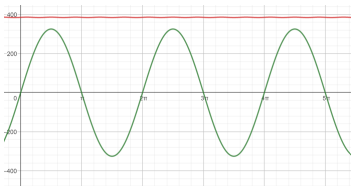

Figure 2: The theoretical input voltage, V_{in} is the green, while the desired output result V_{out} is red

II. Results

A. Simulation

1) SIMULINK: To simulate the boost converter, we utilized Simulink with the Simscape specialized power system package. The group selected a sample time of $1e-7$, which allows for accurate measurements of the converter's performance at a high switching frequency of 65kHz. Although we initially considered conducting the measurements in *Continuous* mode, we encountered a conflict with the *step* block used for variable loading. As a result, we proceeded with the chosen sample time to ensure reliable results.

The values of each component in the model is calculated in the following sub chapters. Figure 3 shows us how the converter is set up in Simulink.

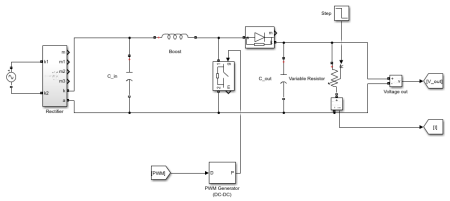

Figure 3: Boost converter Simulink

Converting from AC to DC is done with a full-wave bridge rectifier shown in figure 4. The diodes have a forward voltage at $V_f = 0.8V$. This gives us a converted voltage of $V_{DC} = 317.2V$

$$V_{DC} = V_{in-rms} \cdot \sqrt{2} - \frac{\Delta V}{2} - 2 \cdot V_{diode}$$
$$V_{DC} = 317.2V$$

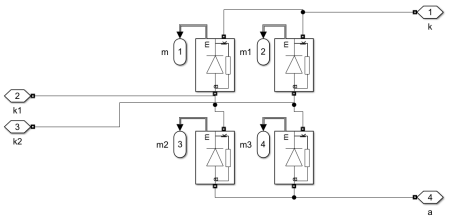

Figure 4: Full-wave bridge rectifier

Simulation results

Figure 5 shows a step response from 20% load to 70% load, over a time frame of $1s$. The step is set to happen at $0.5s$, and varies the load resistance from 192.5Ω to 55Ω, which gives us the following load currents $I_{load20\%} = \frac{385V}{192.5\Omega} = 2A$ and $I_{load70\%} = \frac{385V}{55\Omega} = 7A$.

As seen in figure 5, the control system regulates the voltage output back to its reference as soon as the step occurs.

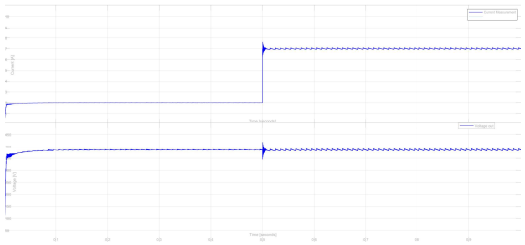

Figure 5: Simulation of a step response from 20% to 70% load

Steady state results

The steady state results is made with the same converter model as in figure 3, except that the capacitors and inductor has an added resistance according to the calculations and to the datasheets. One can see that the efficiency rises when the load increases, as to be expected when simulating this type of devices. The voltage output and inductor current ripple is found by studying the simulink data, and is somewhat inaccurate, as there were some variations at the different times in the simulations. The important point to note is that the voltage ripple, measured over the course of one time period of the rectified input voltage, increases with higher load. The inductor ripple is measured over the period of 1/65000 second, to control that it never reaches any discontinous mode, and the other variations in the inductor current is due to the voltage variations.

y	Efficiency	Voltage output ripple	Inductor current ripple
20	92%	8.8 V	0.86 A
30	95%	9.4 V	0.80 A
40	96%	8.4 V	0.81 A
50	97%	10.0 V	0.83 A
60	97%	11.4 V	0.84 A
70	98%	13.0 V	0.93 A
80	98%	17.1 V	0.84 A
90	98%	15.9 V	0.85 A
100	98%	16.2 V	0.87 A

Table II: Steady state results

2) Switching and conduction losses for diode and MOSFET: **Switching losses**

A double pulse test was conducted in LTSpice in order to simulate the boost converter to decide the most efficient combination through the components provided in terms of switching losses. The combination of Si-FET (Infeon IPP60R099C7) and SiC-diode (Cree CVFD20065A) proved itself to be the most efficient through several simulations. As expected, the FET provides significant losses to the circuit in comparison to the diode. This is a result of choosing a schottky diode, which has a low V_f and fast recovery time. Through choosing this component we mitigate the switching losses.

The energy of the switching losses were found through looking at the graph in LTSpice and integrating the correct lines. The energy was then multiplicated with the switching frequency in order to obtain the values in watts. Figure 6 indicates the switching losses generated from a double pulse test. It displays a Si-FET (red graph) and SiC-diode (blue graph) at 100% load. The switching losses are found by integrating these graphs at turn-on and turn-off.

Formula for calculating the switching losses:

$$P_{switchingloss} = E_{switching} \cdot f_{switching}$$

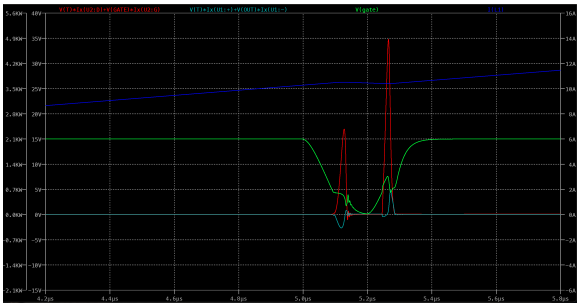

Figure 6: Plot 100% Si fet SiC diode

Conduction losses

Conduction losses is a crucial part of the losses for a boost converter. Conduction losses in case of the diode is a product of the current flowing through it and the voltage drop across it. This will be the majority of conduction loss between it and the MOSFET. The MOSFET's conduction loss is a cause of the voltage across it and current flowing through it in ON-state.

In order to calculate the conduction losses it is nessessary to find the resistance R_f through the components at ON-state. The resistance is found from the datasheet by calculating the slope of the performance graph of I_F / V_F, in our case at 125 °C. I_L is the load-current, witch is 10A at 100%.

The calculations was done by using the following formulas.

Current through the diode:

$$I_D = I_L(1 - D)$$

$$I_{Drms} = I_L\sqrt{1 - D}$$

Conduction loss for the diode:

$$P_d = V_F \cdot I_D + R_f \cdot I_{Drms}^2$$

Conduction loss for the MOSFET:

$$P_m = R_f \cdot I_{SWrms}^2 \cdot D$$

Results switching and conduction losses:

	Switching losses		Concuction losses	
Ispole	**Sum Diode (W)**	**Sum FET (W)**	**Cond. Losses Diode (W)**	**Cond. Losses FET (W)**
20% (2,34A)	1,02	2,08	2,09	0,13
30% (3,64A)	1,01	2,83	3,22	0,3
40% (4,86A)	1,00	3,66	4,4	0,54
50% (6,07A)	0,98	4,55	5,64	0,84
60% (7,28A)	0,97	5,55	6,94	1,2
70% (8,5A)	0,94	6,60	8,29	1,64
80% (9,71A)	0,88	7,67	9,7	2,14
90% (10,93A)	0,87	8,81	11,17	2,71
100% (12,14A)	0,85	9,94	12,69	3,35

Table III: Switching and conduction losses

3) Thermal design: In order to keep the components of the boost converter within the stated values of operating temperature values in the data sheets, some thermal design is needed. A temperature equivalent circuit is drawn in accordance to the thermal resistances found for the MOSFET and diode. Heat sinks are a common way to dissipate heat for electrical components and is also used for this boost converter.

Thermal resistance

The thermal resistance needs to be calculated in order to find the junction temperatures and to dimension the heatsink. Thermal resistance in diodes and MOSFETs refers to their ability to dissipate heat generated during their operation. It is a measure of how effectively they can transfer heat from their internal junctions to the outside environment.

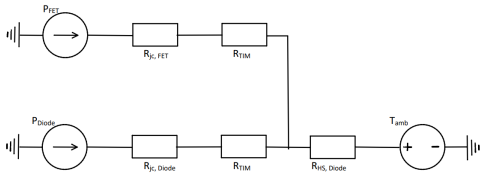

Figure 7: Thermal equivalent circuit

Thermal resistance for the thermal interface material:

$$R_{s-a} = \frac{Z_{TIM}}{A}$$

Thermal resistance:

$$R_{c-a,m} = \frac{T_{jmax} - T_a - R_{j-c,m} \cdot P_m - R_{s-a} \cdot P_m}{P_{tot}}$$

$$= \frac{125°C - 25°C - (1.135°C/W - 0.4°C/W) \cdot 13.29W}{26.83W}$$

$$R_{c-a,m} = 3.36°C/W$$

$$R_{c-a,d} = \frac{T_{jmax} - T_a - R_{j-c,d} \cdot P_d - R_{s-a} \cdot P_d}{P_{tot}}$$

$$= \frac{125°C - 25°C - (0.8°C/W - 1.06°C/W) \cdot 13.54W}{26.83W}$$

$$R_{c-a,d} = 3.86°C/W$$

Heatsink

The heatsink is chosen from the calculated $R_{c-a,m}$ and the provided datasheets from Fischer Elektronik and covers the needs for both the MOSFET and diode. A single heatsink is benefitial for practical reasons in regards to weight and space. The heatsink is 50mmX75mmX25mm(DxWxH) and consists of raw degreased aluminium. The weight will be approximately 140g and volume is around 47,62cm^3.

Junction temperature

Junction temperatures in regards to the MOSFET and diode is the internal operating temperature of the component. The junction temperature is calculated from the calculated thermal resistances and should not exceed stated operating temperatures in the datasheets. The junction temperatures is calculated for load scenarios from 20% to 100% to assure temperatures not going out of range for operating temperatures.

Formulas for calculating junction temperatures:

$$T_{j,m} = T_a + R_{c-a} \cdot P_{tot} + R_{j-c,m} \cdot P_m$$

$$T_{j,d} = T_a + R_{c-a} \cdot P_{tot} + R_{j-c,d} \cdot P_d$$

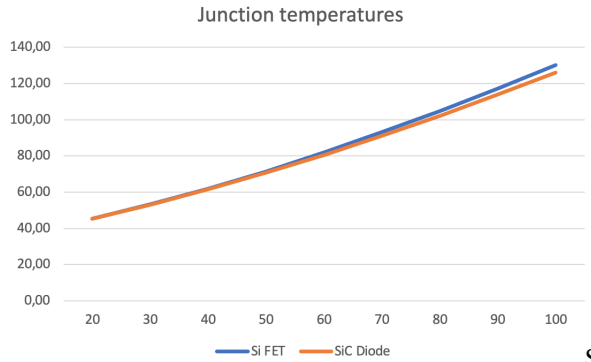

Figure 8: Junciton temperatures for Si-FET and SiC-diode at loads 20% - 100%

C_R 100 Hz 20 °C µF	Case dimensions d × l mm	ESR_{typ} 100 Hz 20 °C mΩ	Z_{max} 10 kHz 20 °C mΩ	$I_{AC,max}$ 100 Hz 40 °C A	$I_{AC,R}$ 100 Hz 85 °C A	Ordering code (composition see below)
V_R = 350 V DC						
1500	51.6 × 80.7	85	106	15	5.5	B434*4A4158M000
2200	51.6 × 105.7	57	71	20	7.3	B434*4A4228M000
2200	64.3 × 80.7	57	71	20	7.3	B434*4B4228M000
2700	64.3 × 80.7	45	56	23	8.5	B434*4A4278M000
3300	64.3 × 105.7	37	46	27	9.8	B434*4A4338M000
3900	64.3 × 105.7	32	40	30	10.9	B434*4A4398M000
4700	64.3 × 118.2	28	35	33	12.2	B434*4A4478M000
5600	76.9 × 105.7	25	31	37	13.4	B434*4A4568M000
6800	76.9 × 118.2	20	25	43	15.7	B434*4A4688M000
8200	76.9 × 143.2	16	20	50	18.4	B434*4A4828M000
10000	76.9 × 168.7	12	15	50	22.4	B434*4A4109M000
12000	76.9 × 190.7	10	13	50	26.1	B434*4A4129M000

Figure 9: Table of possible capacitators at 350 V

B. *Passive Components*

For calculating the capacitance we need to know the duty cycle D, the needed current I_d. We already know that $V_{DC} = 317.2V$

$$D = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{317.2V}{385V} = 0,176$$

$$I_d = \frac{V \cdot I}{V_{in,RMS}} = \frac{385V \cdot 10A}{317.2V} = 12,14A$$

1) Capacitors: We are going to have 2 capacitors in the circuit, C_{in} and C_{out}, which both has to be calculated.

$$C_{in,min} = \frac{I_{in} \cdot t}{\Delta V} = \frac{12,14A \cdot \frac{1}{100Hz}}{13V} = 9,34mF$$

$$C_{out,min} = \frac{I_0 \cdot D \cdot T_s}{\Delta \cdot V_0} = \frac{10A \cdot 0,176 \cdot \frac{1}{65000Hz}}{385 \cdot 0,01} = 7,03\mu F$$

When choosing the C_{in}-capacitor the datasheet for aluminium electrolytic capacitor is used, as these capacitors has the kind of voltage and capacitance as needed.

Since the needed capacitance is $9,34mF$ the capacitor "B434*4A4109M000", with a capacitance of 10 mF. The rated current is higher than the current that the boost converter will have, so it is okay to use. As read from the table, $ESR = 12m\Omega$ at 100 Hz, and the dissipation factor is ≤ 0.20. This will be used in the calculation of losses in the product.

The C_{out}-capacitor has to be larger than the calculated minimum, and there is some possibilities. The options is to choose a SP(solder pin) or a FA(flex assembly) capacitor. The parameters which needs to be taken into consideration is: losses, switching capability, current capability, large enough capacitor in stock. Since this is going to be a DC-signal, but with some AC-components with high frequency, the value that has to be considered in the datasheet is the "C_{eff}". When this is considered, the only capacitor which has a large enough capacitance is the $SP500$. The datasheet shows that the capacitance is 100% of C_{eff} at 400 V, which means the simulation can be done with a capacitance of $12\mu F$.

Finding the ESR for 65 kHz is done by linearizing between the values from the datasheet, and the value will be about $25m\Omega$ at this frequency.

The power loss for the capacitors can be calculated with this formula:

$$P_{loss} = I_{RMS}^2 \cdot ESR$$

The current through the capacitor is found through a simulink analysis, where the RMS-value is measured in the simulation.

2) Inductor: One of the objectives in the task is having a current ripple of 1 A or less, so when the inductance is calculated this is taken into consideration.

$$L_{min} = \frac{\frac{D}{f} \cdot V_{in}}{Ripple} = \frac{\frac{0,176}{65000Hz} \cdot 317.2V}{1A} = 858\mu H$$

When designing the inductor, heat dissipation is not taken in to consideration. The inductor material will be 3f3 and the core will be a double E shape. Because the heat dissipation of the inductor is not considered in this project, we are free to chose the value of J_{rms} ourselves. Typical values range between 2-6 A/mm^2. In this project J_{rms} is chosen to be $3.5\frac{A}{mm^2}$ at full load, as it results in a good balance between winding losses and the size of the inductor core. Giving us relatively low winding losses, and a relatively compact inductor. From data sheet, fig.3, the 3f3 material saturates at $340mT$, at $100°C$, giving us $\hat{B}$. The inductor will be designed with litz wire because the operating frequency in this system is $65kHz$ and the skin effect could be a problem. Practical value for fill factor k_{Cu} of a litz wire is 0.3.

$$J_{rms} = 3.5\frac{A}{mm^2}$$
$$\hat{B}_{100} = 340mT$$
$$k_{Cu} = 0.3$$

Inductor currents:

$$I_d\frac{V_{out}}{V_{in}} \cdot I_{out} = \frac{385V}{317.2V} \cdot 10A = 12.14A$$

$$\hat{I}_d \approx I_d(1 + \frac{I_{ripple}}{2 \cdot I_0}) = 12.14A(1 + \frac{1A}{2 \cdot 10A}) = 12.747A$$

The stored energy relation:

$$L\hat{I}Irms = k_{Cu}J_{rms}\hat{B}A_wA_{core}$$

Solved for area product A_wA_{core}:

$$A_wA_{core} = \frac{L\hat{I}Irms}{k_{Cu}J_{rms}\hat{B}_{100}} = \frac{858\mu H \cdot 12.747A \cdot 12.14A}{0.3 \cdot 3.5\frac{A}{mm^2} \cdot 340mT} = 3.7191 \cdot 10^{-7}m^4$$

When designing the geometric characteristics of the core the suggested value of a, based on the area product, from Power Electronics, P.751 [1] is used.

$$a = \sqrt[4]{\frac{A_wA_{core}}{2.1}} = 2.05cm$$

The maximum inductance achievable for a specified core is

$$L_{max} = \frac{NA_{core}\hat{B}_{core}}{\hat{I}}$$

$$N \geq \frac{L\hat{I}}{A_{core}\hat{B}_{100}}$$

$$\frac{L\hat{I}_d}{1.5a^2\hat{B}_{100}} = 51.03$$

$$N = 52$$

52 turns on this specific core and current will give an inductance L_{max} of $874\mu H$.

To find the airgap, equation 30-33 from Power Electronics, P.764 [1] is used.

$$\Sigma g \approx \frac{A_{core}}{\frac{A_{core}\hat{B}_{core}}{\mu_0 N\hat{I}} - \frac{(a+d)}{N_g}} = \frac{1.5 \cdot (2.05cm)^2}{\frac{1.5\cdot(2.05cm)^2\cdot 340mT}{4\pi\cdot 10^{-7}kg\cdot m\cdot s^{-2}\cdot A^{-2}\cdot 52\cdot 12.747A} - \frac{(2.05cm+1.5\cdot 2.05cm)}{4}}$$

$$\Sigma g \approx 2.578mm$$

$$g = \frac{\Sigma g}{N_g} = \frac{2.578mm}{4} = 0.645mm$$

The density of the 3f3 material $\rho_{3f3} = 4750kg/m^3$, and copper $\rho_{Cu} = 8.96g/cm^3$.

Inductor specifications	
a $[cm]$	2.05
N	52
A_{Cu} $[mm^2]$	3.47
$Airgap$ $[mm]$	0.645
V_{core} $[cm^3]$	116.3
V_{Cu} $[cm^3]$	105.97
m_{core} $[kg]$	0.552
m_{Cu} $[kg]$	0.949
m_{total} $[kg]$	1.5
L_{max} $[\mu H]$	874

Table IV: Specifications of inductor

Inductor hysteresis loss:
Equation 30-2a from Power Electronics [1].

$$P_{m,sp} = 1.5 \cdot 10^{-6} \cdot f^{1.3} \cdot (B_{ac})^{2.5}$$

$$P_m = P_{m,sp}V_{core}$$

The magnetic field density in the core is approximately proportional to the current in the inductance, as long as the the core is not saturated

$$B_{ac} = \hat{B}\frac{\hat{I} - I_{dc}}{\hat{I}}$$

Worst case in this system will be at
$\hat{B} = \hat{B}_{100} = 340mT$ and at maximum load
$\hat{I} = \hat{I}_d = 12.747A$ and $I_{dc} = I_d = 12.14A$

$$B_{ac,max} = 340mT\frac{12.747A - 12.14A}{12.747A} = 16.19mT$$

The maximum hysteresis loss in the core is then

$$\begin{aligned} P_{m,max} &= 1.5 \cdot 10^{-6} \cdot (65kHz)^{1.3} \\ &\cdot (16.19mT)^{2.5} \cdot 116.3cm^3 \\ &= 41.83mW \end{aligned}$$

Because the hysteresis loss is so low compared to other losses, even for the worst case, the hysteresis loss is negligible and wont be considered in the overall efficiency of the system.

Winding losses:

$$P_w = k_{Cu}\rho_{Cu}(J_{rms})^2 V_{Cu}$$

$$P_w = k_{Cu}\rho_{Cu}(\frac{I_{rms}}{A_{cu}})^2 V_{Cu}$$

Load[%]	**winding loss [mW]**
20	343
30	771
40	1370
50	2141
60	3084
70	4198
80	5483
90	6939
100	8567

Table V: Winding losses

These winding losses are quite small. There could be an argument to be made, that it would be better to allow a higher current density J_{rms} at maximum load. Resulting in a smaller core and a thinner wire. The trade-off being higher winding losses.

C. Others

1) Control System: The control system used in this project is a PI-controller, which utilizes the measured output voltage as feedback and sets the reference to the desired output voltage. The purpose of the control system is to regulate the duty cycle of the converter when there are variations in the load.

Figure 10 shows the block diagram of the control system in Simulink.

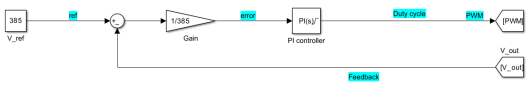

Figure 10: Controll system simulink

To test the effectiveness of the control system, the group conducted experiments with and without a nominal input. When a nominal input of the desired duty cycle was used, the regulation was initially more precise and faster. However, the control system struggled to regulate when the load was changed from, for instance, 20% to 70%.

As a result, the group decided to regulate the system without a nominal input. The PI-controller values were tuned using a *frequency plot* autotune method.

Variable	Value
k_p	0,3
k_{T_i}	40
Nominal input	0
Gain	$\frac{1}{385}$

Table VI: Control system values

The transfer function of the PI-controller is defined as

$$h = k_p + \frac{k_i}{s}$$

where K_p is the proportional gain and K_i is the integral gain of the controller. The proportional gain determines how much the controller responds to the current error, while the integral gain determines how much the controller responds to past errors. Together, these two gains allow the controller to adjust the output in order to minimize the error between the desired and actual values of the system being controlled.

Finding the Bode plot was a process of a lot of trial and error. The initial thought was to linearize the whole system and calculate a transfer function for the entire system. Calculating the transfer function by hand was too difficult, so there was done a lot of research on the *Model Linearizer* app in Simulink. The group weren't able to make this work and ended up plotting a bode-plot for the PI-controller in MATLAB. The following code lines shows how the bode-plot was plotted.

```
s = tf('s');
k_p = 0.3;
k_i = 40;
h = k_p + k_i/s
bode(h);
```

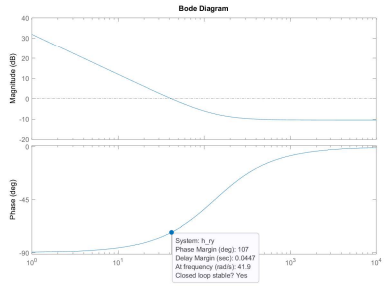

Figure 11: Bode plot of the PI-controller

D. Design Results

The results are somewhat suprising, given that the efficiency is about 99% through the whole load specter. The efficiency also decreases with increasing load, which was not expected, and does not match with the simulations. This can be because of simplifications or wrong numbers either in the simulation or in the calculations below, or both. Nonetheless, the results shows that the tempereature in the MOSFET increases as the load gets larger, and the losses increases too. Since the task is designing the circuit from the H-bridge, the losses in the diodes of the bridge rectifier are not taken into consideration.

Load (12,4A)	Total losses (inductor + capacitors + diode + MOSFET)	Efficiency	Diode junction temp	MOSFET junction temp
20%	6,7W	99,1%	45,4°C	45,4°C
30%	10,0W	99,1%	53,1°C	53,3°C
40%	13,9W	99,1%	61,6°C	62°C
50%	18,4W	99,1%	70,7°C	72°C
60%	23,4W	99,0%	80,6°C	82°C
70%	29,0W	98,9%	91,2°C	93,1°C
80%	35,0W	98,9%	102°C	104,7°C
90%	41,6W	98,8%	113,9°C	117,3°C
100%	48,6W	98,7%	126°C	130,3°C

Table VII: Design results

III. Conclusion

The group has sucsessfully been able to design a 230V AC to 385V DC rectifier which fullfills the requirements given in the project task. There was given some datasheets for different components the group could choose between, and the neccesary calculations and considerations were done to find the optimal components.

When choosing diodes and transistor, the simulation program ”LTSpice” was used to see the lost energy for switching and conduction in the components. This was done with a ”double pulse”-test, and with all the possible combinations of diodes and transistors. The best combination was a SI-FET and a SiC-diode. When designing and choosing the passive components, the worst load conditions were considered to make sure the components will be able to handle all load scenarios. Values to fulfill these requirements were calculated. When choosing the capacitors, the chosen capacitances were slightly larger than calculated. The inductor was designed with the intention of having a balance between winding losses and core size.

In Simulink, the PWM-signals for controlling the output voltage needed to be regulated, to keep the voltages stable with variable load. This was done with a bit of trial and error, but also with the help from the ”Q/A”-lectures. At the end, the circuit was well regulated with a fast reaction time on load changes.

The circuit regulates within the desired parameters, and there is some margin both at high and low loads. The calculated efficiency is a bit higher than expected in this kind of device, which can indicate that a big loss is neglected, or some mistakes in the calculation is done.

BIBLIOGRAPHY

[1] Mohan, Undeland and Robbins, *Power Electronics*. John Wiley and Sons, Inc, 2003.

APPENDIX A

	Losses															Junction temperature	
	Turn Off		Turn On		Sums												
Ispole	SI FET	SIC Diode	SI FET	SIC Diode	Sum Diode	Sum FET	Sum Diode in W	Sum FET in W	Cond. Losses Diode	Cond. Losses FET	Inductor Losses	Capacitor Losses	Total loss	Effiency	SI FET	SIC Diode
20% (2,34A)	4,53	7,21	27,47	8	15,2	32	1,02	2,08	2,09	0,13	0,343	0,99	6,7	99,14	45,40	45,38
30% (3,44A)	7,05	7,49	35,56	8	15,49	43,51	1,01	2,83	3,22	0,3	0,771	1,87	10,0	99,14	53,29	53,12
40% (4,66A)	12,57	7,5	43,69	7,9	15,4	56,26	1,00	3,66	4,4	0,54	1,37	2,96	13,9	99,10	62,04	61,60
50% (6,07A)	18,37	7,3	51,6	7,8	15,1	69,97	0,98	4,55	5,64	0,84	2,141	4,24	18,4	99,05	71,50	70,69
60% (7,28A)	24,99	7,1	60,4	7,8	14,8	85,39	0,97	5,55	6,94	1,2	3,084	5,7	23,4	99,00	81,96	80,62
70% (8,5A)	32,35	6,7	69,25	7,77	14,47	101,6	0,94	6,60	8,29	1,64	4,198	7,33	29,0	98,94	93,12	91,15
80% (9,71A)	39,85	6,1	78,1	7,5	13,6	117,95	0,88	7,67	9,7	2,14	5,483	9,12	35,0	98,88	104,70	102,04
90% (10,93A)	47,35	5,8	88,12	7,6	13,4	135,47	0,87	8,81	11,17	2,71	6,939	11,06	41,6	98,81	117,29	113,85
100% (12,14A)	55,6	5,6	97,2	7,47	13,07	152,9	0,85	9,94	12,69	3,35	8,567	13,17	48,6	98,75	130,31	126,05

Figure 12: Total losses and efficiency

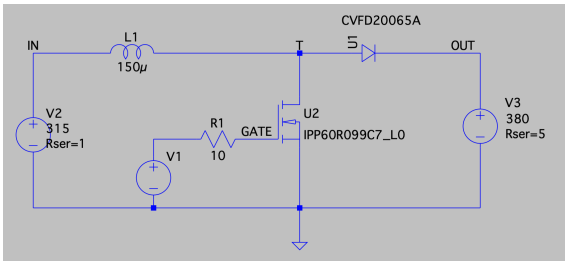

Figure 13: Schematic of the Si-FET SiC-diode boost converter in LT-spice

Chosen components		
Type	**Description**	**Size**
Inductor	Double E-shaped core, n=52	$874\mu F$
Capacitor	Electrolytic capacitor (B434*4A4109M000)	10mF, 350V
Capacitor	Fast switching soldier pin (SP500)	$12\mu F$, 500V
MOSFET	Si-FET (Infeon IPP60R099C7)	
Diode	SiC-diode (Cree CVFD20065A)	
Heatsink	SK 567 (from datasheet)	50x75x25(DxWxH)

Table VIII: Component list