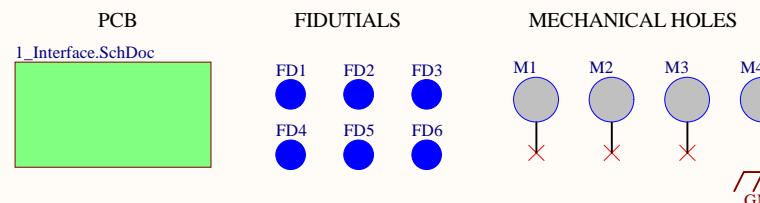


Rev	Description	Date	Author
1.0	Initial release.	30-Apr-2020	Andre M. P. Mattos

Revision History



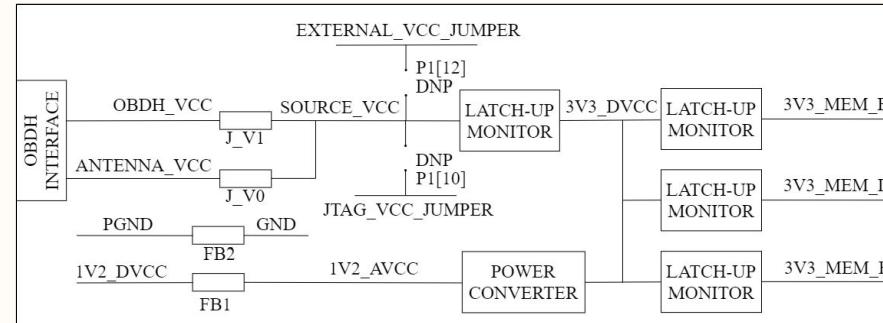
PCB Elements

HARSH Payload Daughter Board (HARSH_Payload) for OBDH 2.0 ALT Hardware

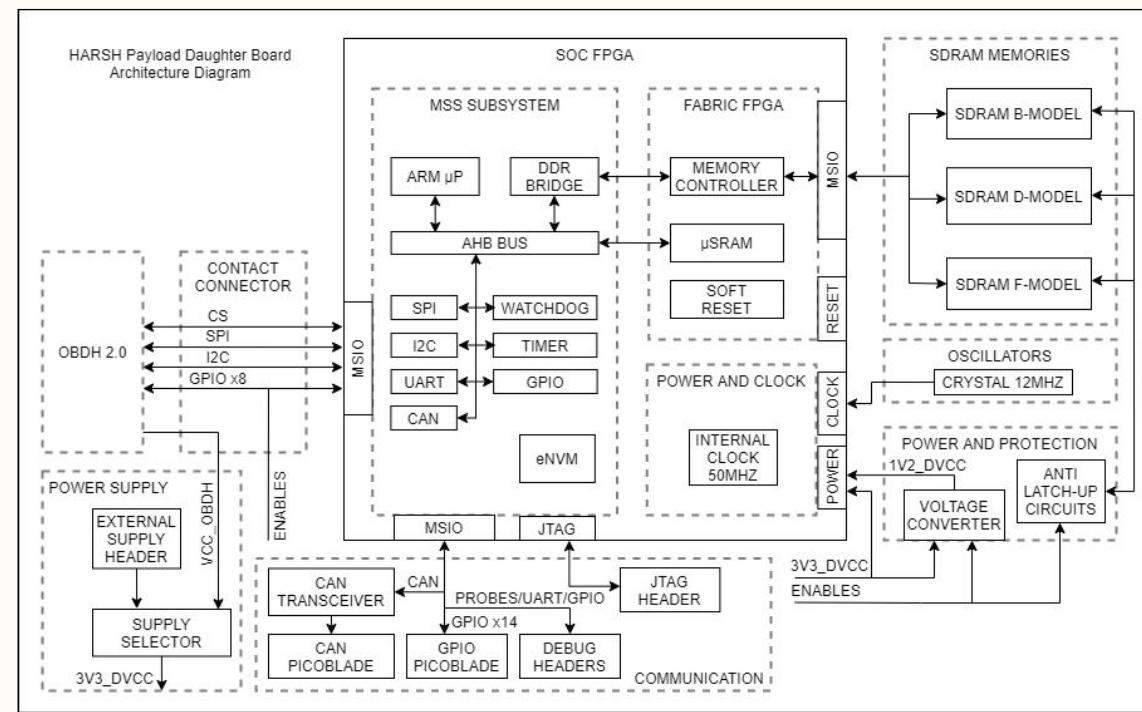
Copyright © 2020 by UFSC and LIRMM.

- Drawn by: André Martins Pio de Mattos.
- Reviewers: Yan Castro de Azeredo.
- Based on OBDH 2.0 designed by: André Martins Pio de Mattos.
- Based on DB_Memory designed by: Yan Castro de Azeredo.
- Support: Kleber Reis Gouveia Júnior.

Project Information



Power Diagram

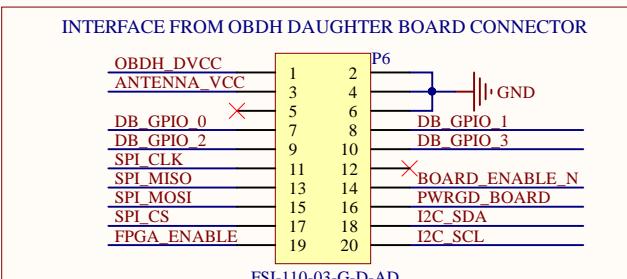
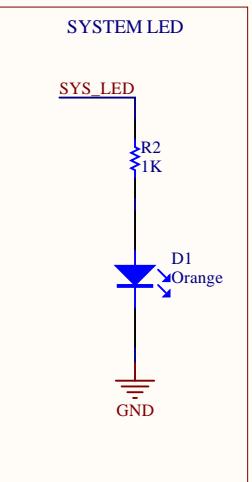
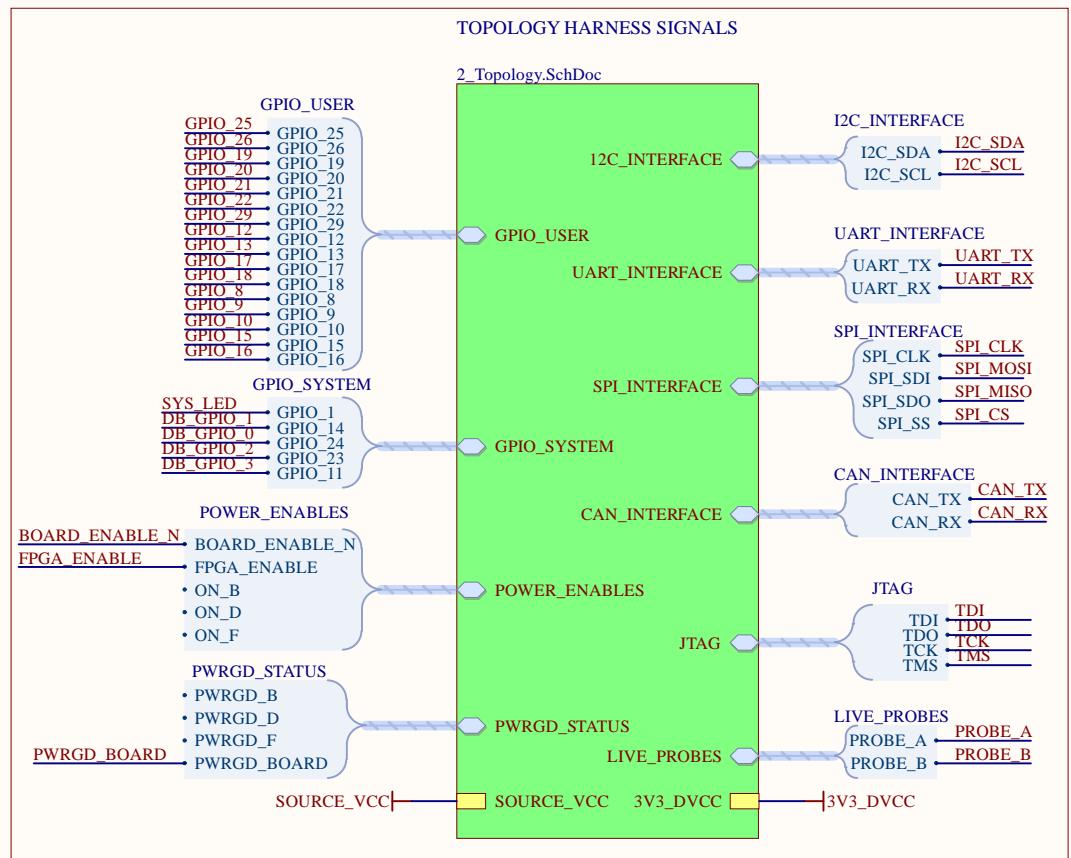
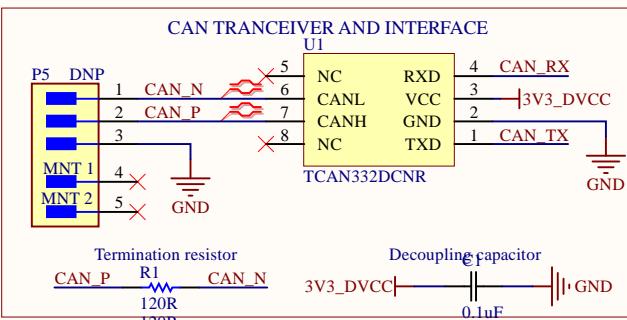
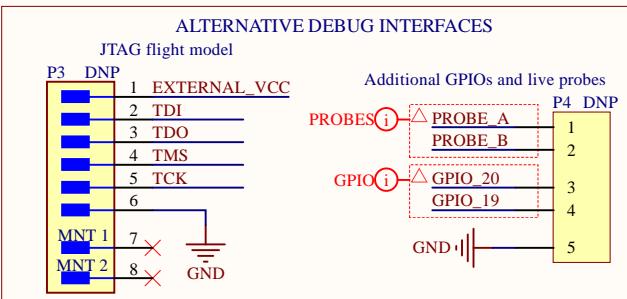
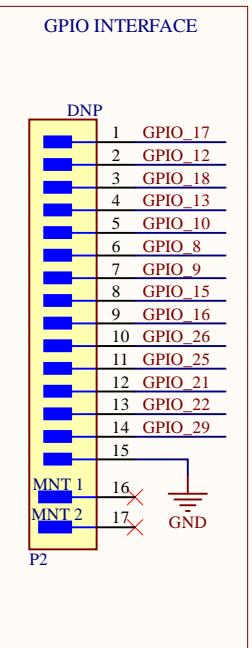
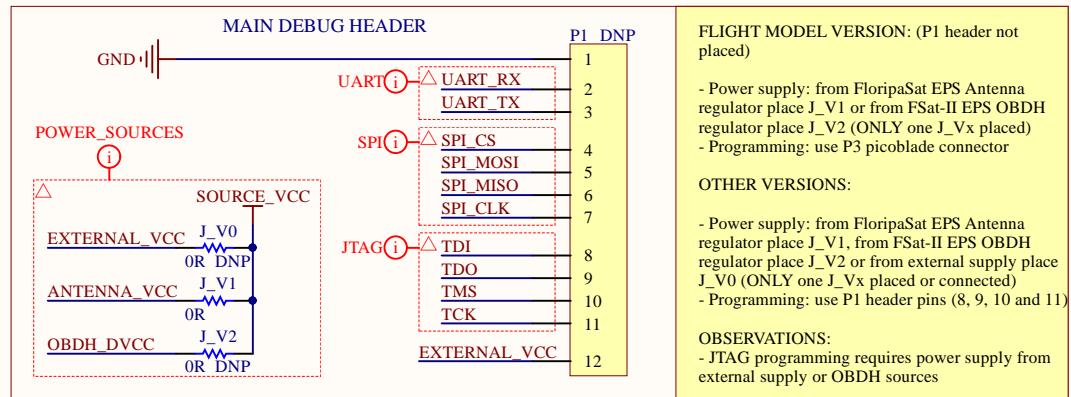


Block Diagram

Title: HARSH Payload Architecture		
Size: A4	Project: HARSH_Payload.PjPCB	Revision: 1.0
Date: 4/27/2020	Time: 7:11:21 PM	Sheet 1 of 8
Drawn By: Andre Martins Pio de Mattos	Model: HARSH_DB	

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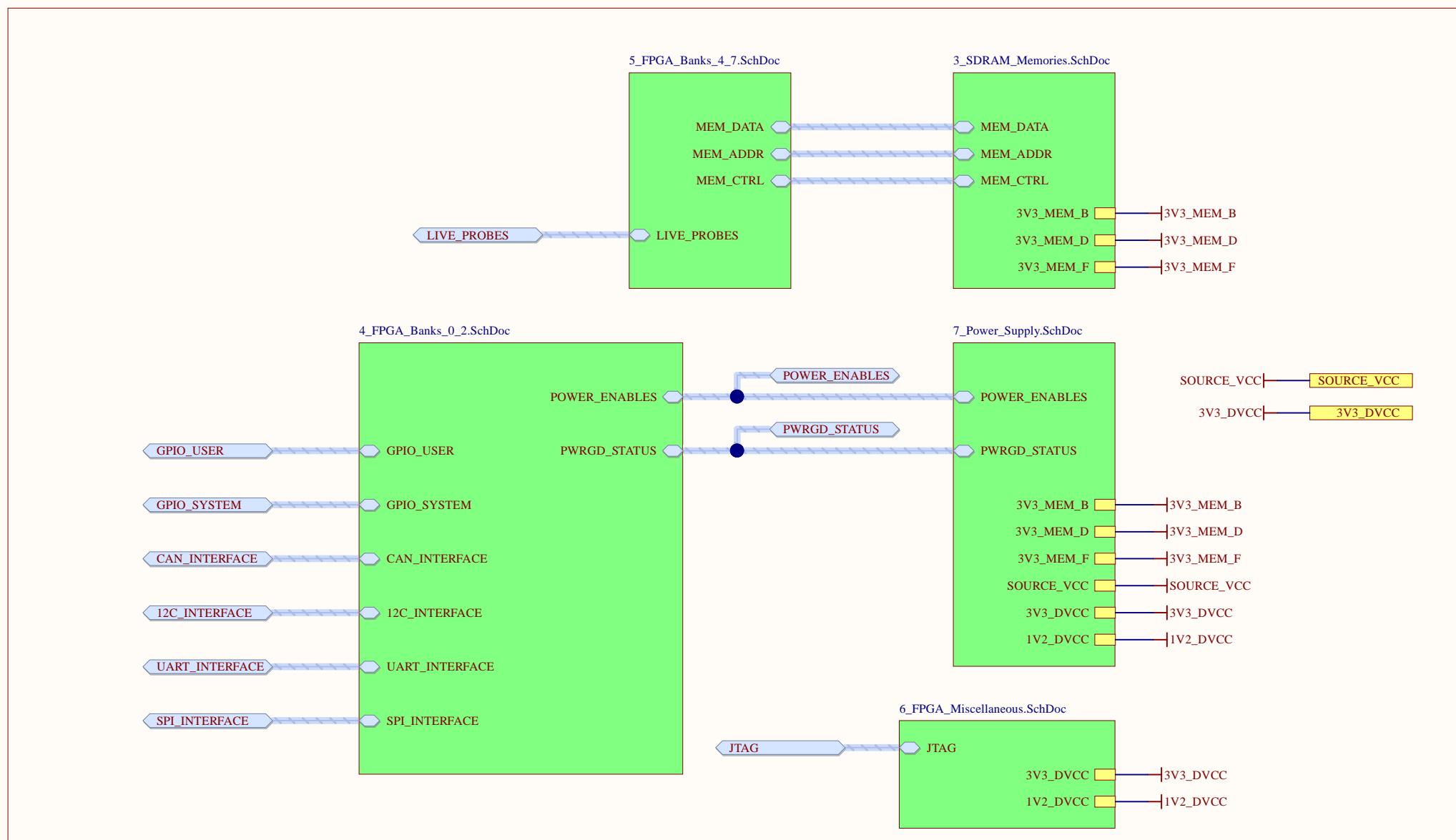


According to SAMTEC product specification, the maximum body height of the connector when pressed should be 3.28 mm.

Title: HARSH Payload Interface		
Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.0
Date: 4/27/2020	Time: 7:11:21 PM	Sheet 2 of 8
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB

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Title: **HARSH Payload Topology**

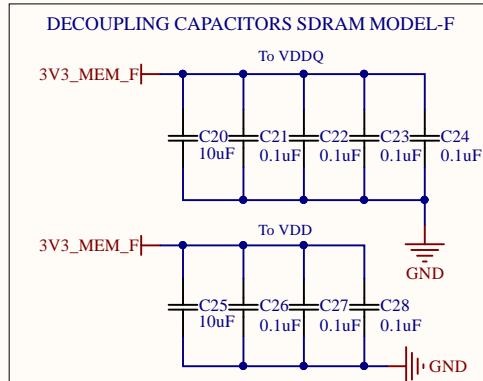
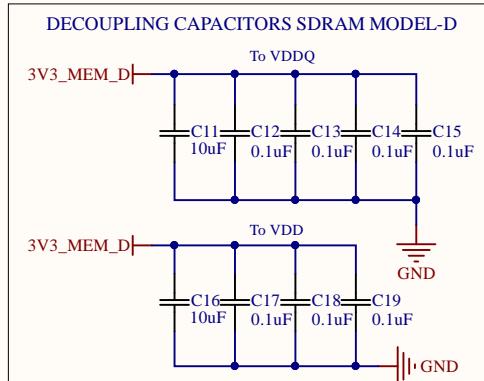
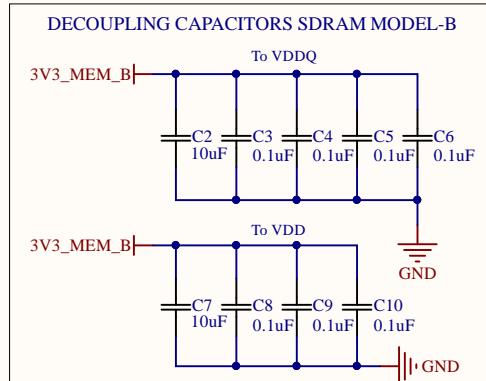
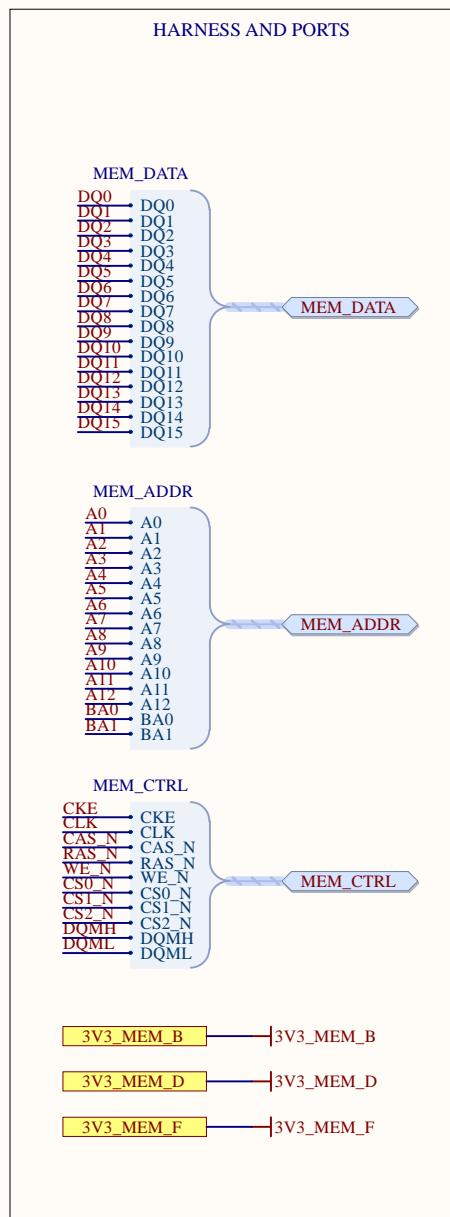
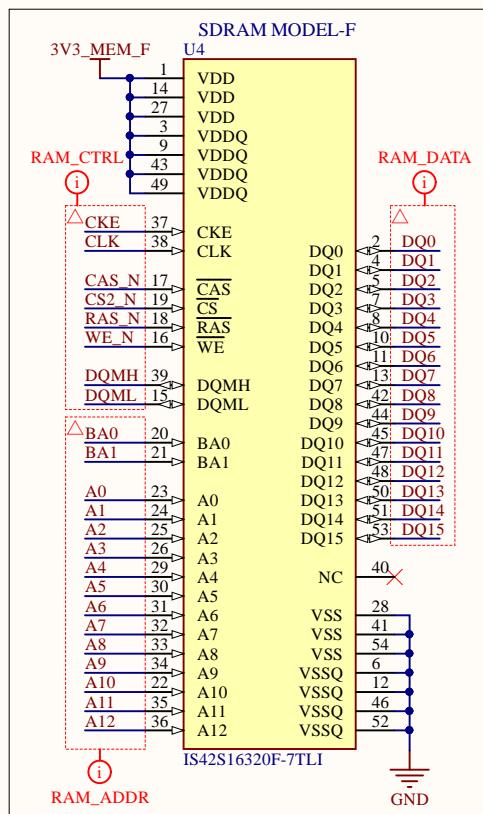
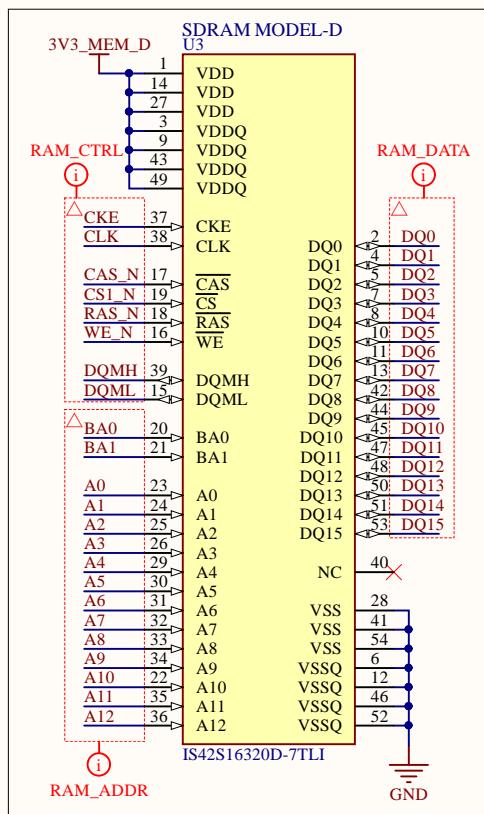
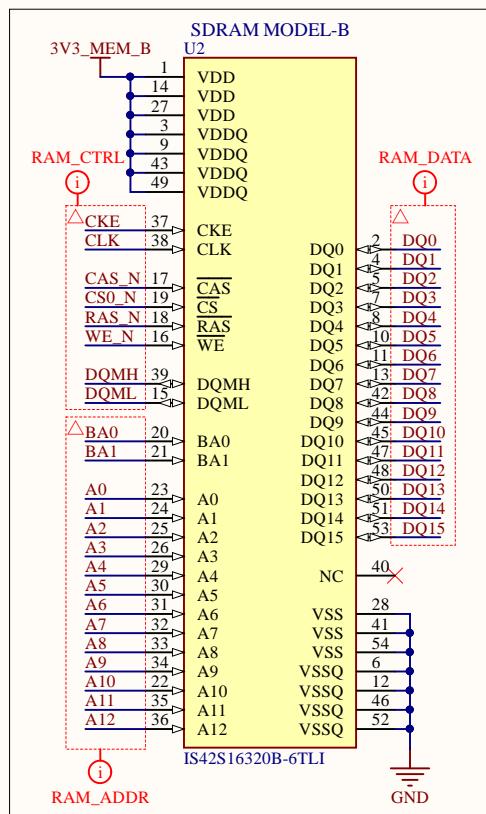
Size: **A4** Project: **HARSH_Payload.PjPCB** Revision: **1.0**

Date: **4/27/2020** Time: **7:11:22 PM** Sheet **3** of **8**

Drawn By: **Andre Martins Pio de Mattos** Model: **HARSH_DB**

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Title: **HARSH Payload SDRAM memories**

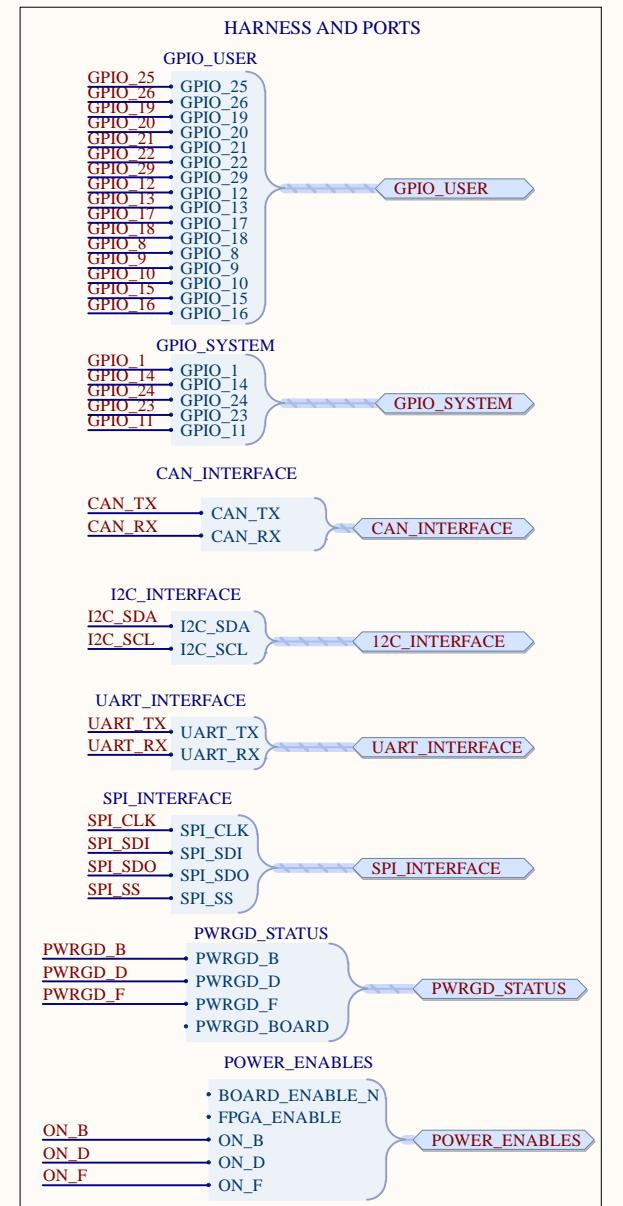
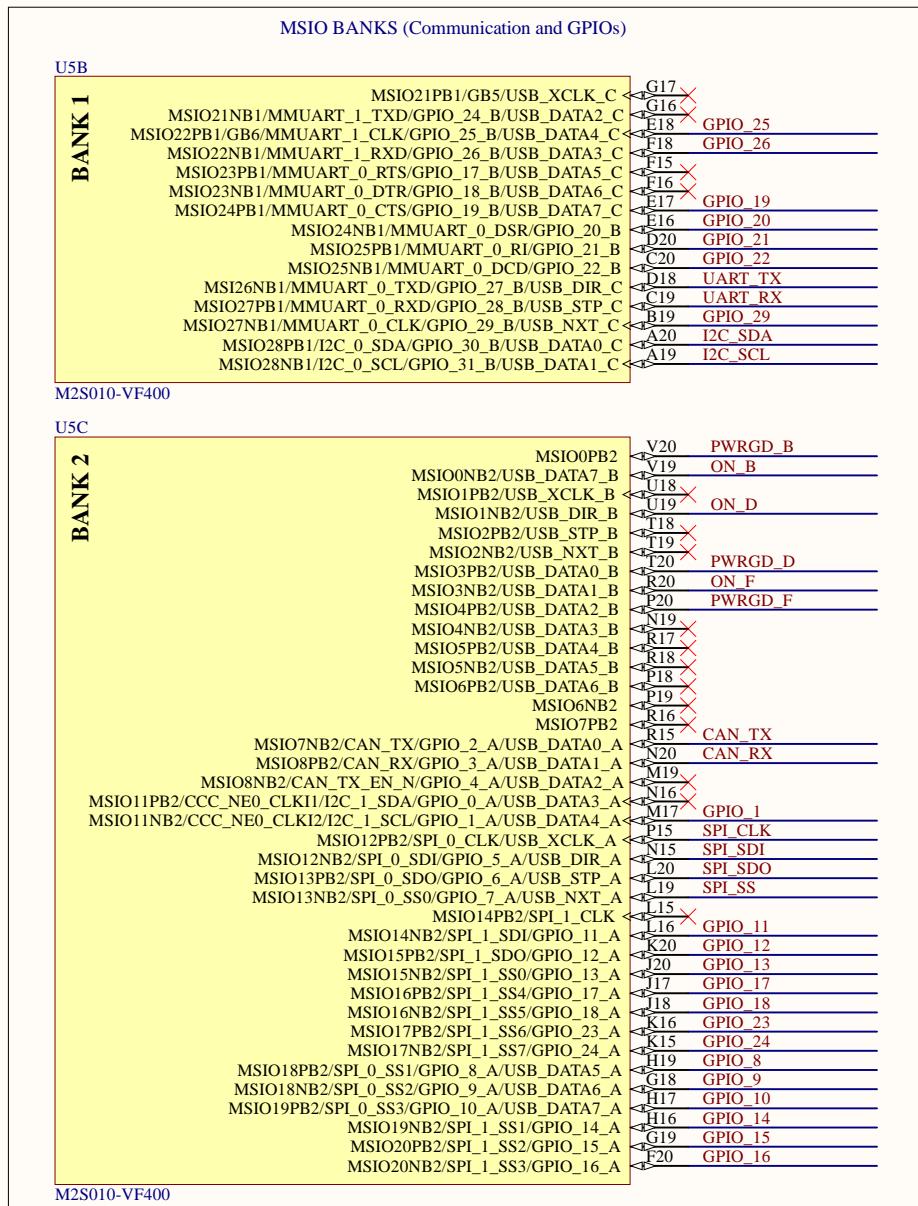
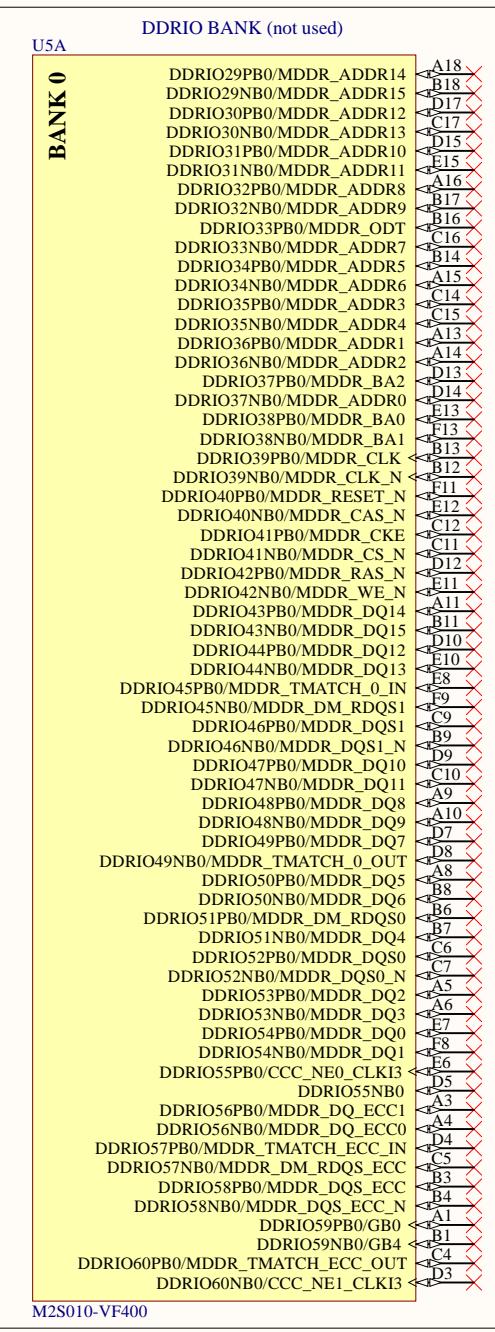
Size: **A4** Project: HARSH_Payload.PrjPCB Revision: **1.0**

Date: **4/27/2020** Time: **7:11:22 PM** Sheet **4** of **8**

Drawn By: **Andre Martins Pio de Mattos** Model: **HARSH_DB**

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Title: HARSH Payload FPGA Banks 0_2

Size: A4 Project: HARSH_Payload.PrjPCB Revision: 1.0

Date: 4/27/2020 Time: 7:11:22 PM Sheet 5 of 8

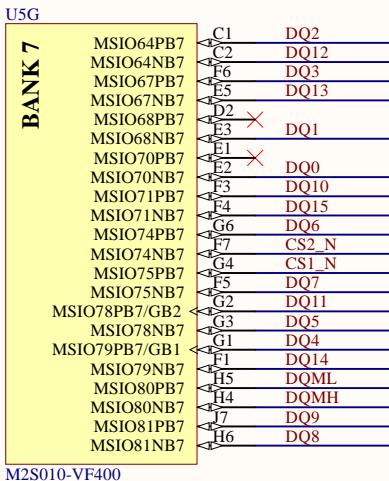
Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

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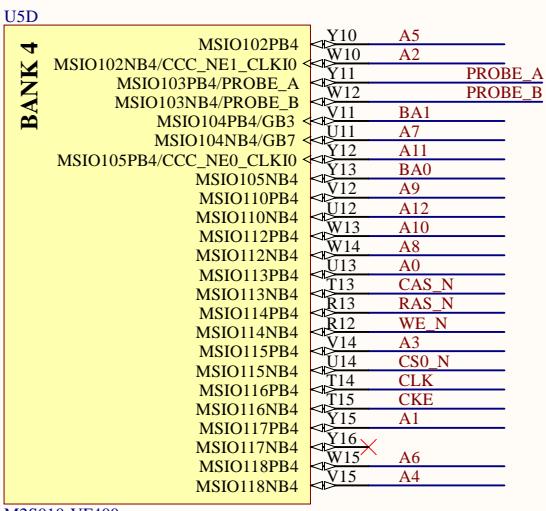
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MSIO BANKS (memories)

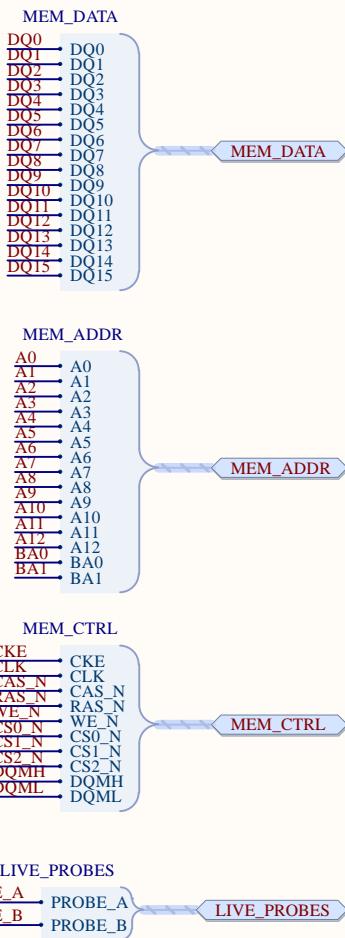
SDRAM data and control signals



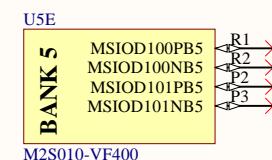
SDRAM address and control signals



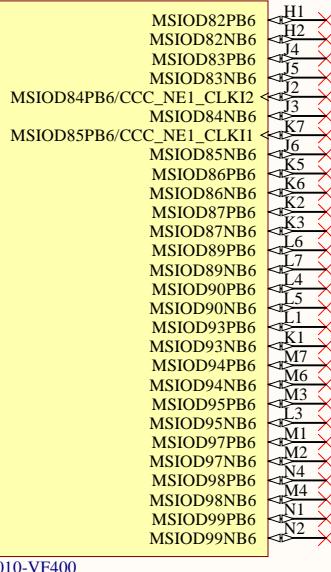
HARNESS AND PORTS



MSIOD BANKS (not used)



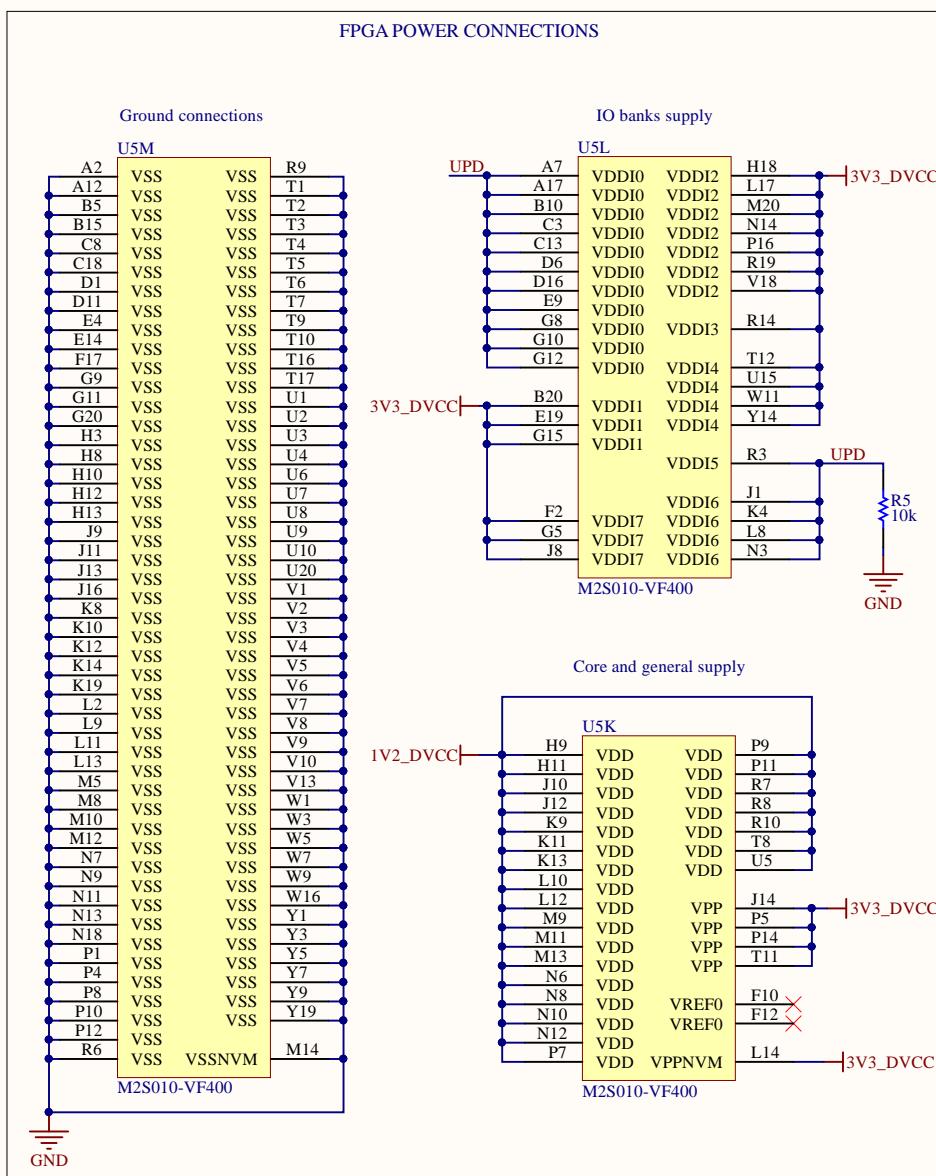
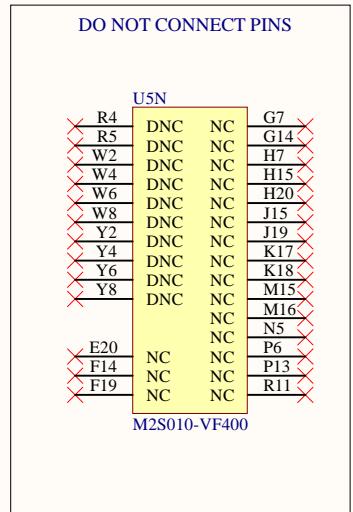
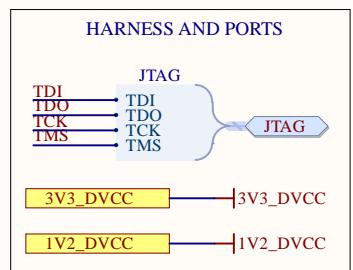
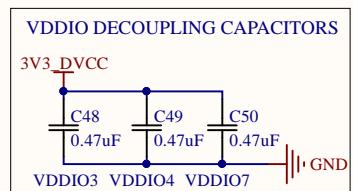
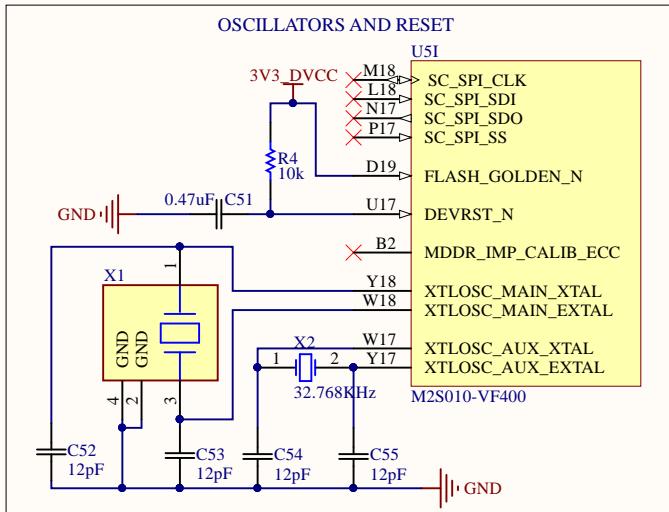
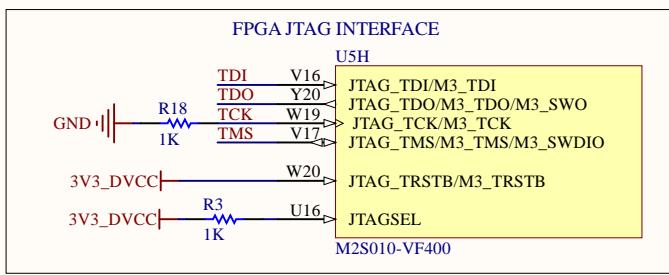
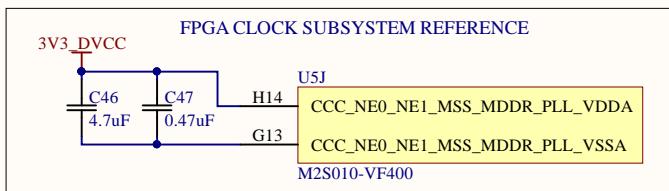
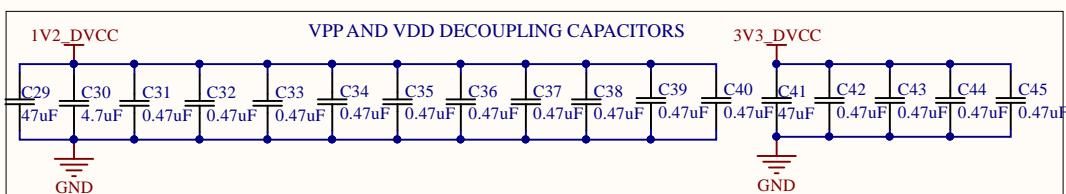
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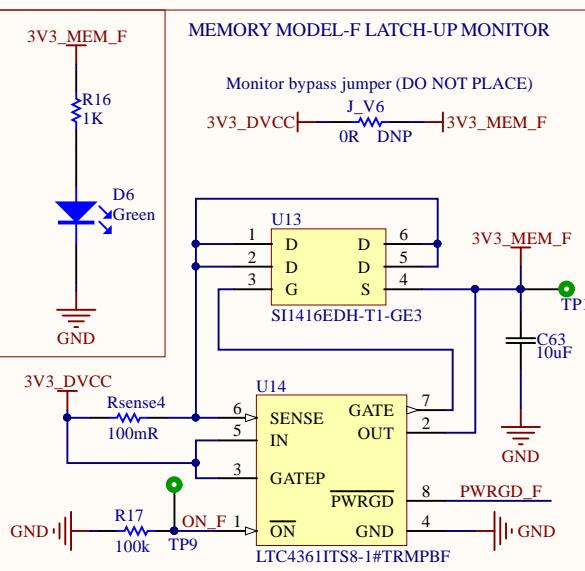
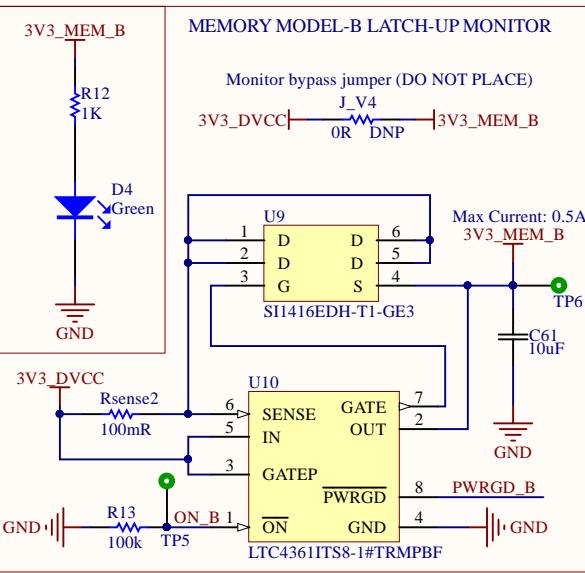
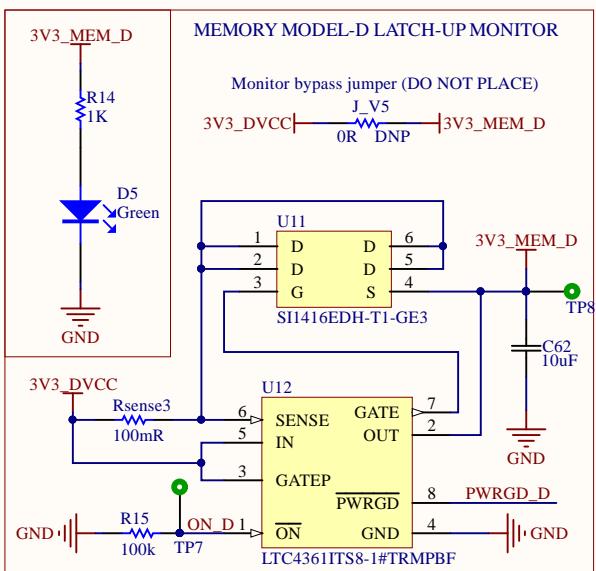
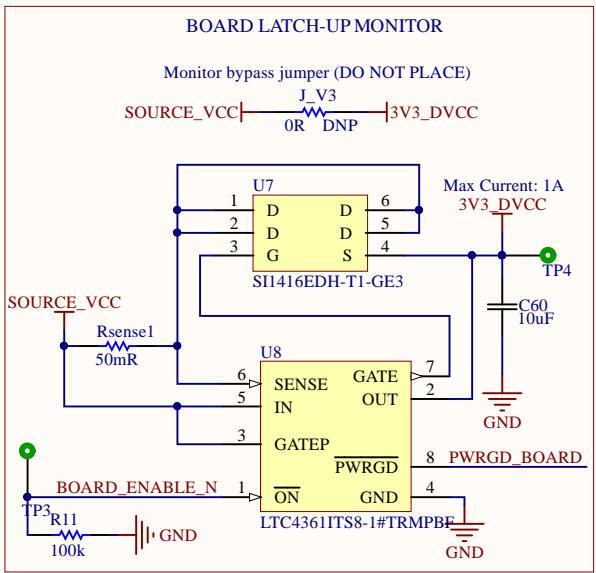
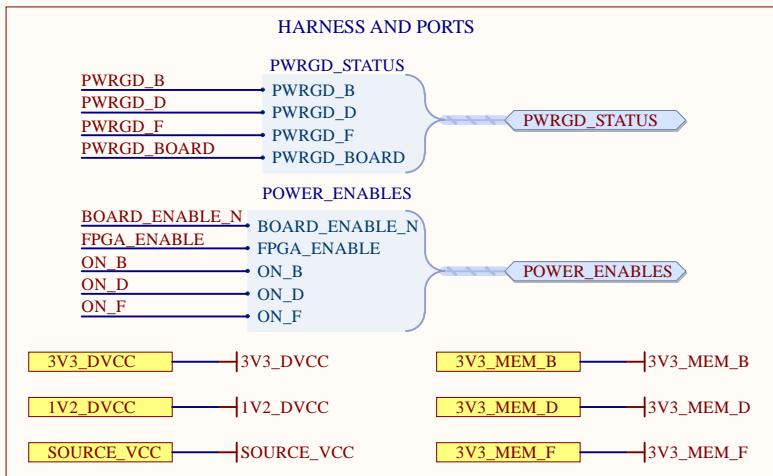
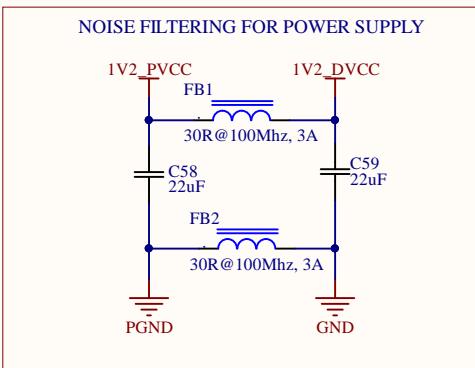
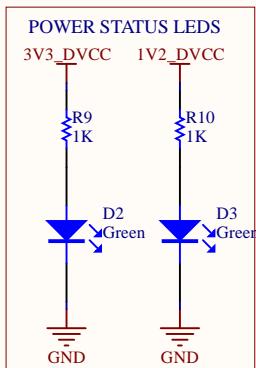
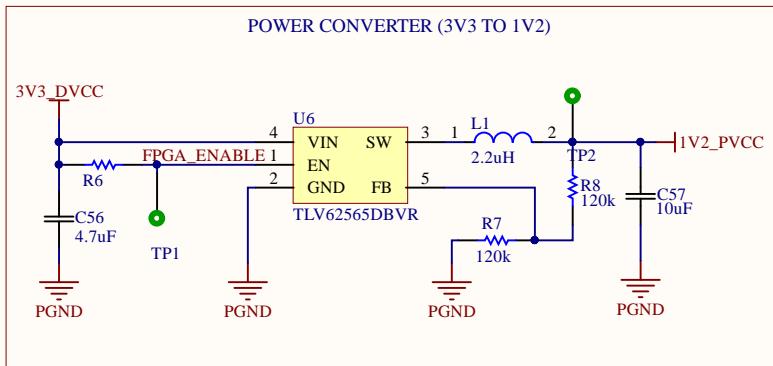


Title: HARSH Payload FPGA Banks 4_7	Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.0
Date: 4/27/2020	Time: 7:11:23 PM	Sheet 6 of 8	
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB	

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Title: HARSH Payload Power Supply

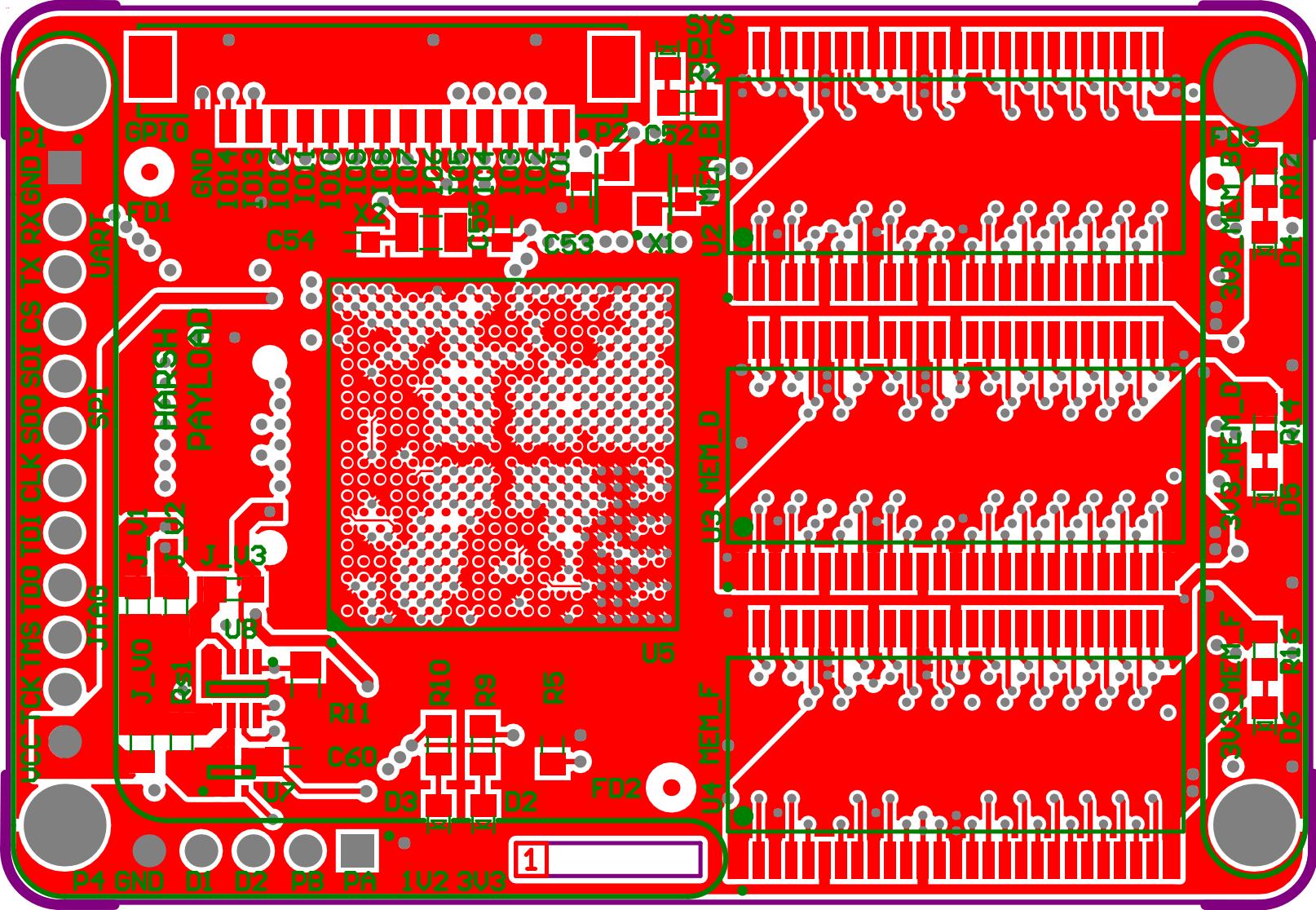
Size: A4 Project: HARSH_Payload.PrjPCB Revision: 1.0

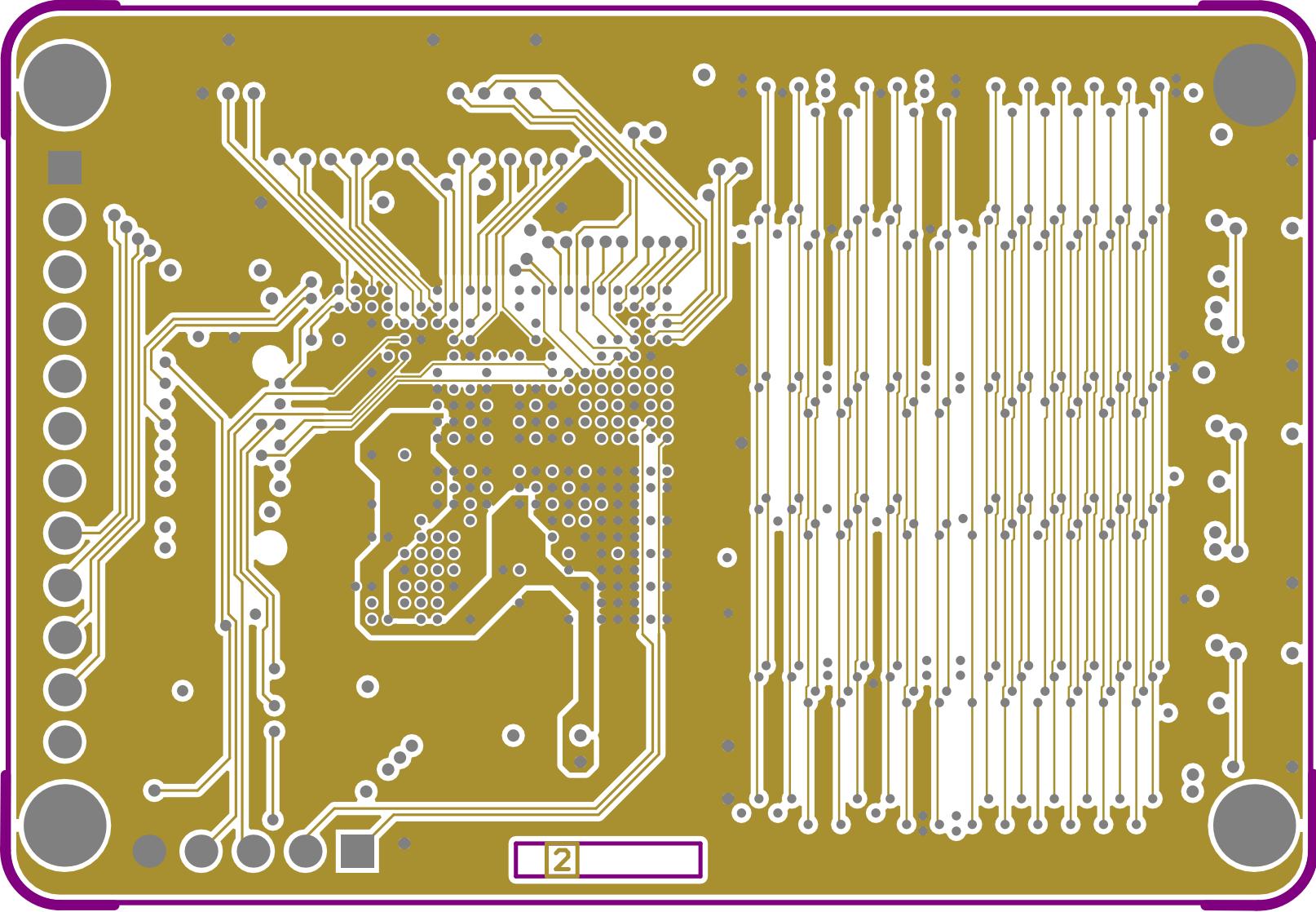
Date: 4/27/2020 Time: 7:11:23 PM Sheet 8 of 8

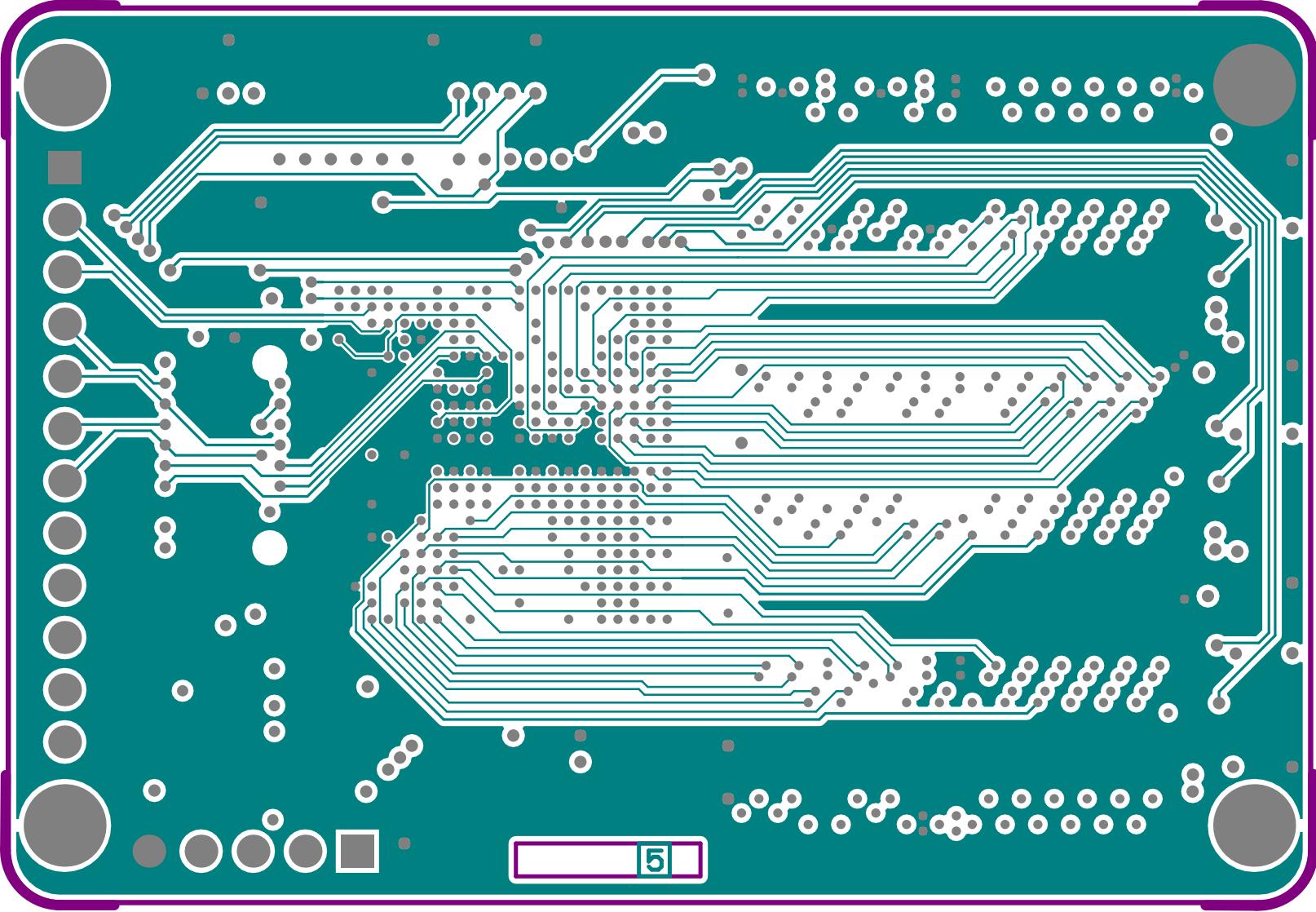
Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

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