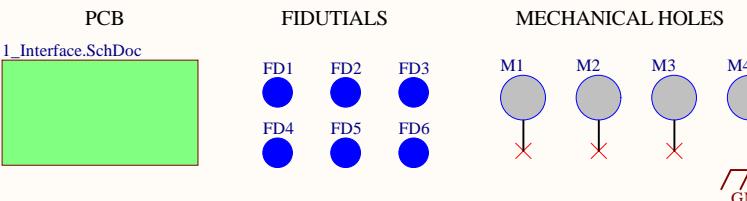


Rev	Description	Date	Author
1.0	Initial release.	30-Apr-2020	Andre M. P. Matto

Revision History



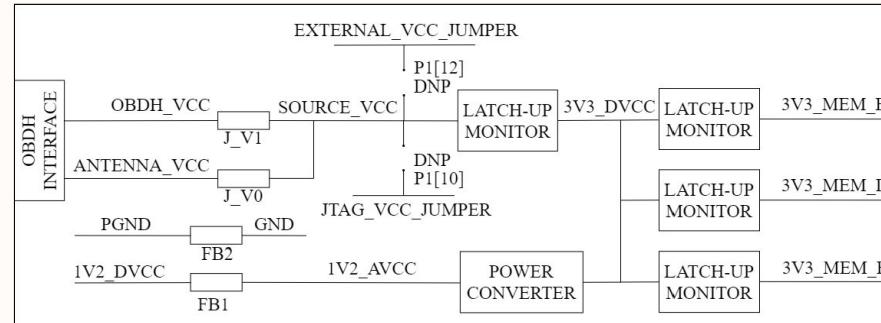
PCB Elements

HARSH Payload Daughter Board (HARSH_Payload) for OBDH 2.0 ALT Hardware

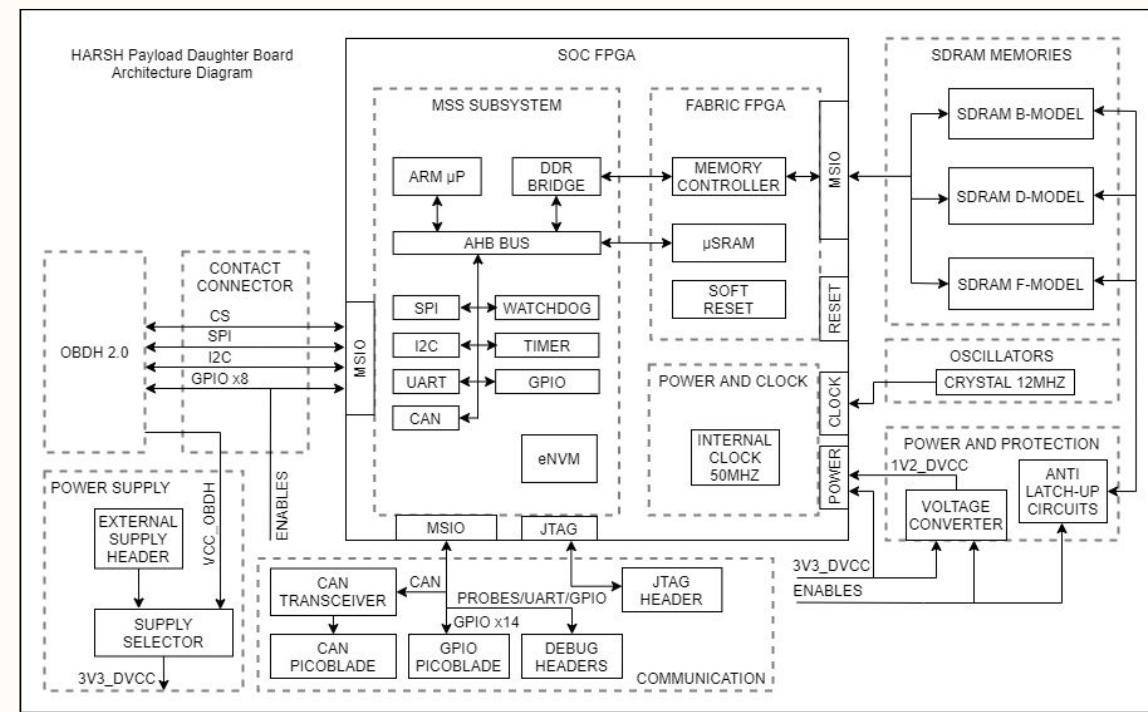
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- Drawn by: André Martins Pio de Mattos.
 - Reviewers: Yan Castro de Azeredo.
 - Based on OBDH 2.0 designed by: André Martins Pio de Mattos
 - Based on DB_Memory designed by: Yan Castro de Azeredo.
 - Support: Kleber Reis Gouveia Júnior

Project Information



Power Diagram

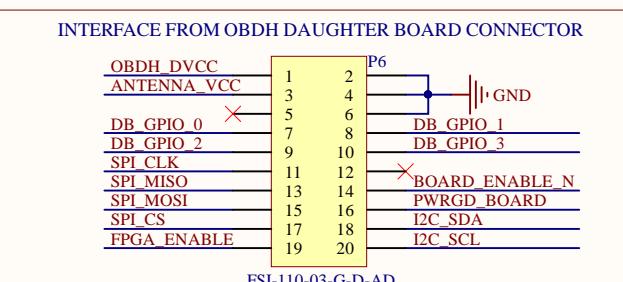
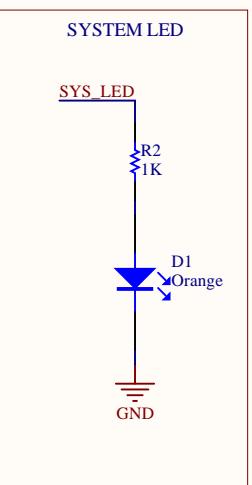
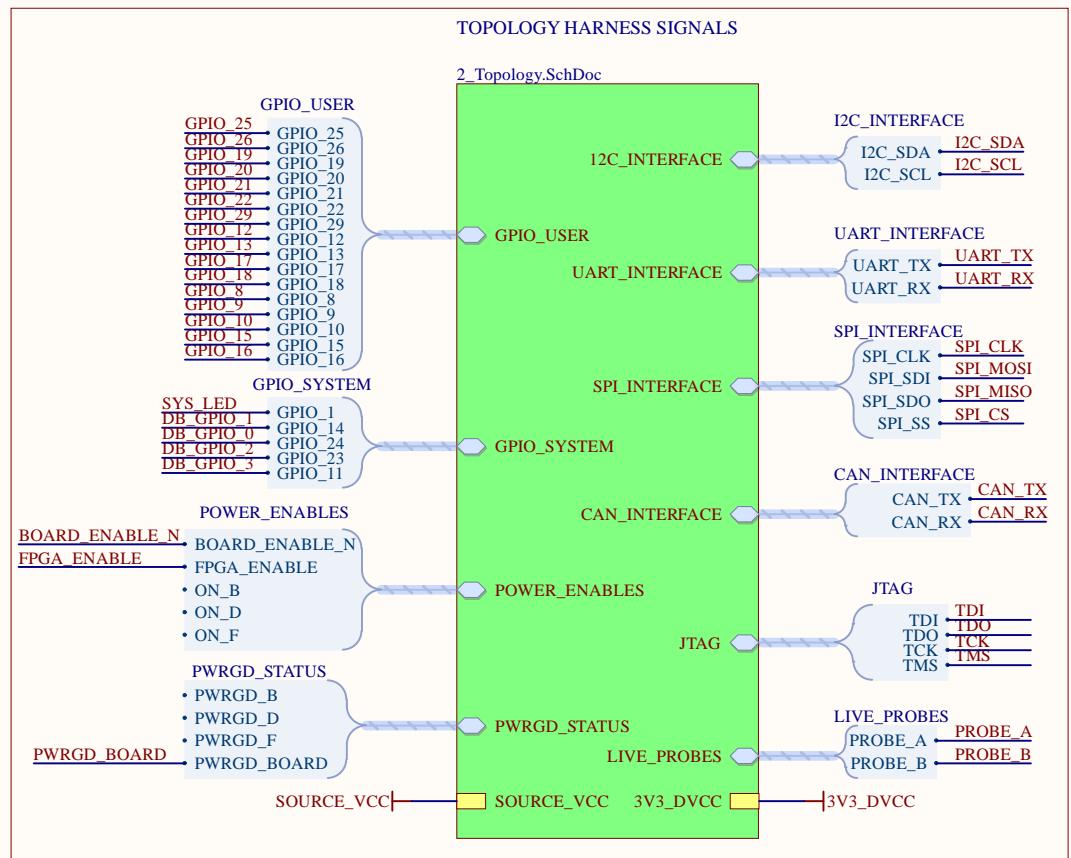
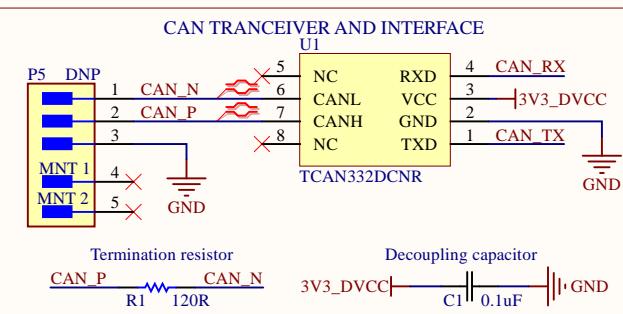
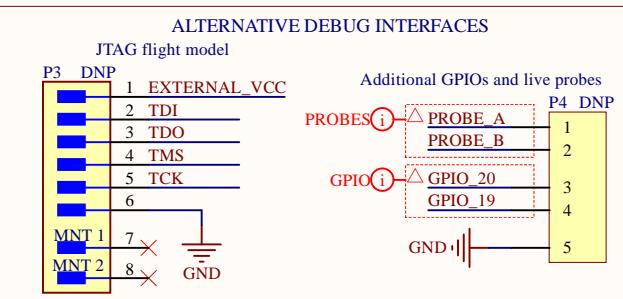
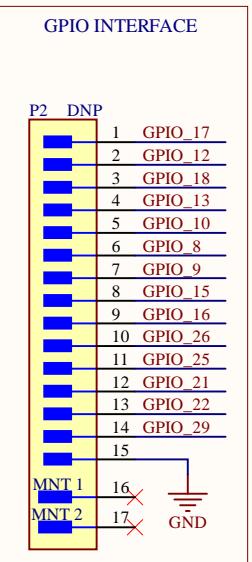
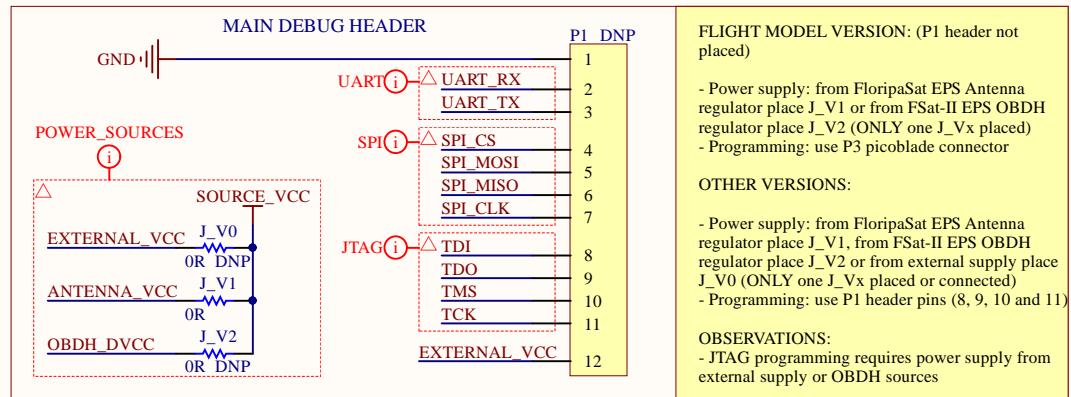


Block Diagram

Title: HARSH Payload Achitecture		
Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.0
Date: 4/27/2020	Time: 6:15:17 PM	Sheet 1 of 8
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB

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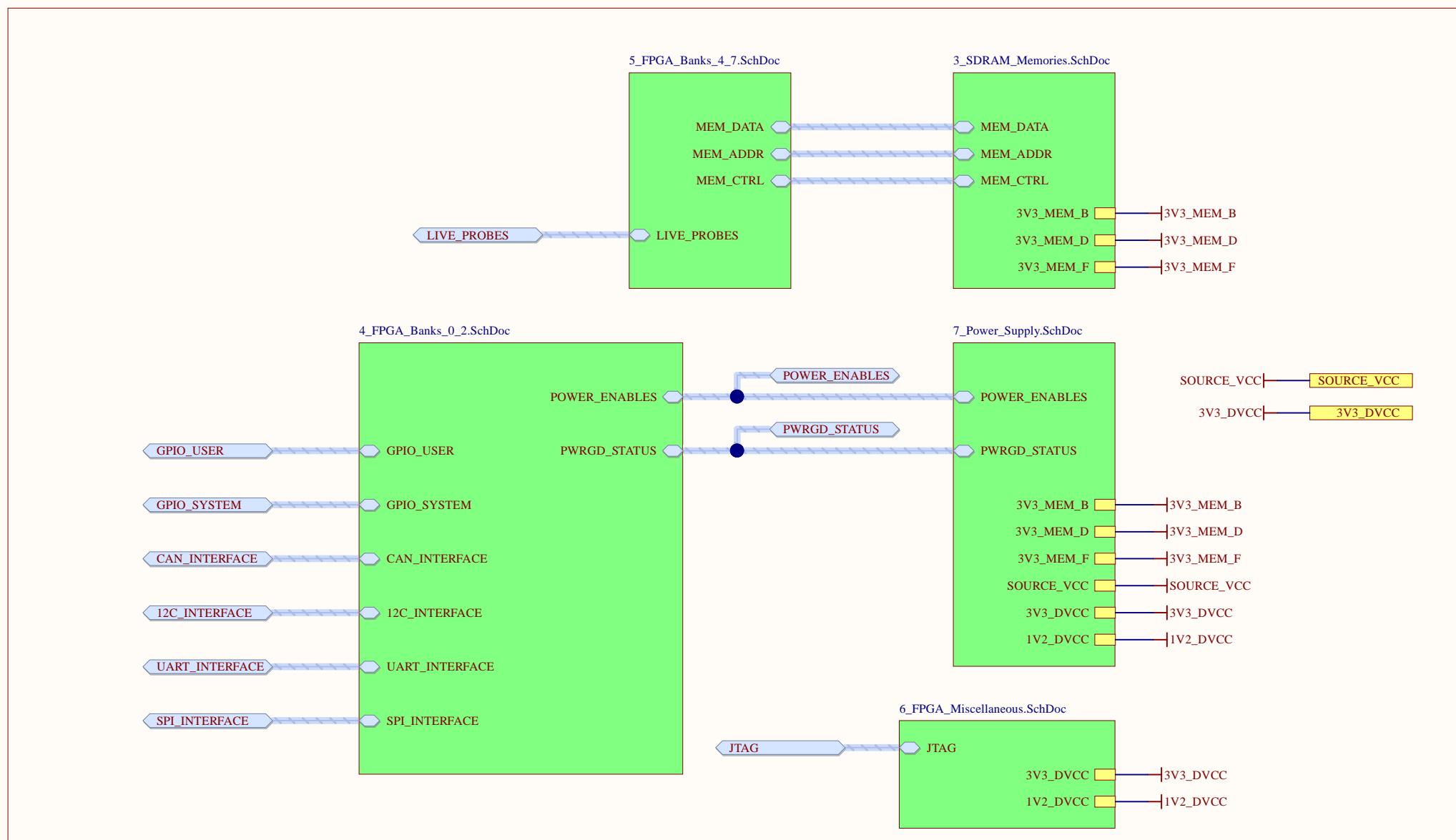
Features not used from the generic daughter board interface connector:
- BATTERY VCC
Features used differently, but compatible, in the generic daughter board interface connector:
- DB_CS2 as GPIO for FPGA enable (Active High)
- DB_ADC0 as GPIO for board "power good" status (feedback of payload power status)
- DB_ADC1 as GPIO for board enable (Active Low)

According to SAMTEC product specification, the maximum body height of the connector when pressed should be 3.28 mm.

Title: HARSH Payload Interface		
Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.0
Date: 4/27/2020	Time: 6:15:18 PM	Sheet 2 of 8
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB

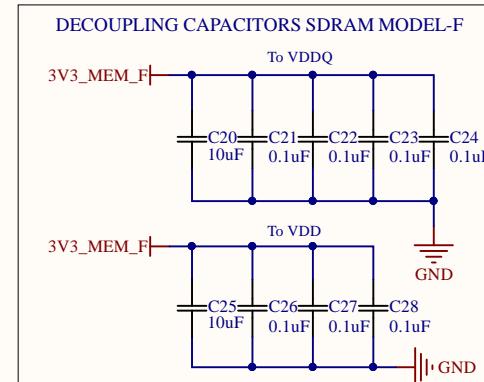
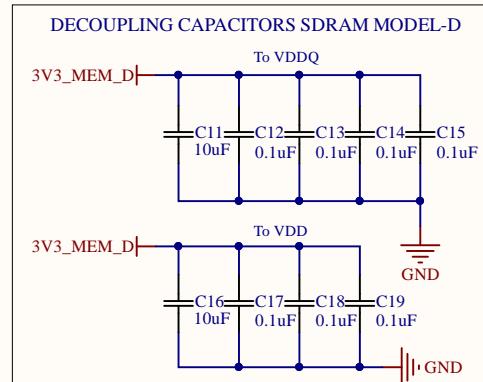
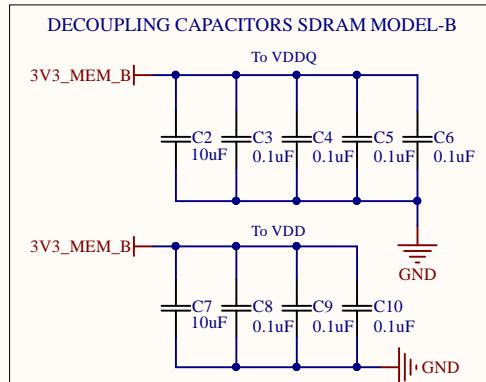
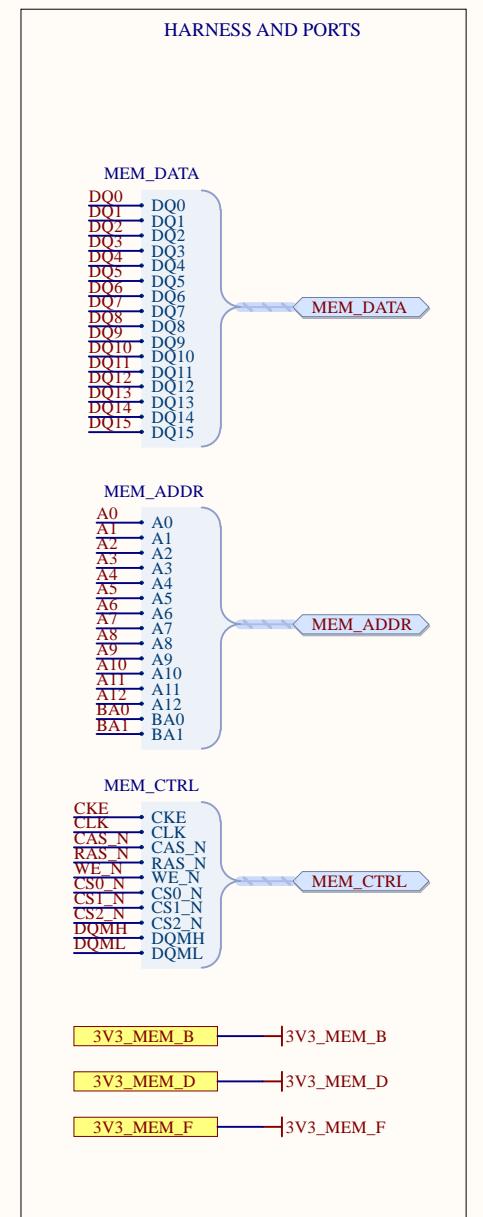
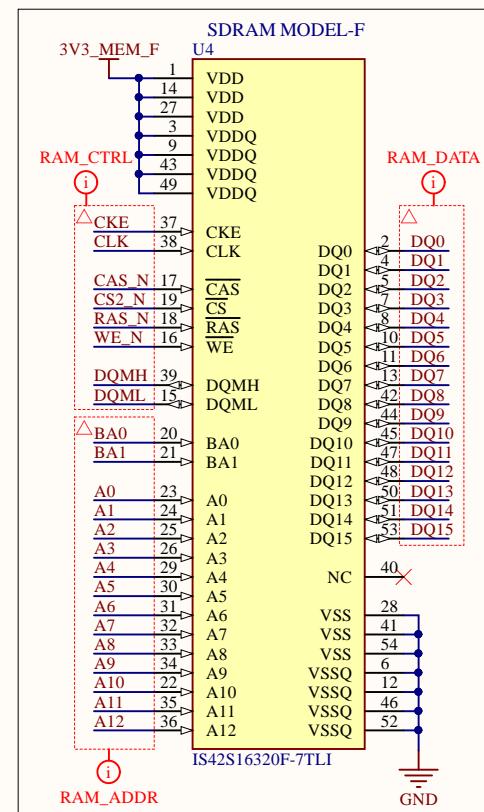
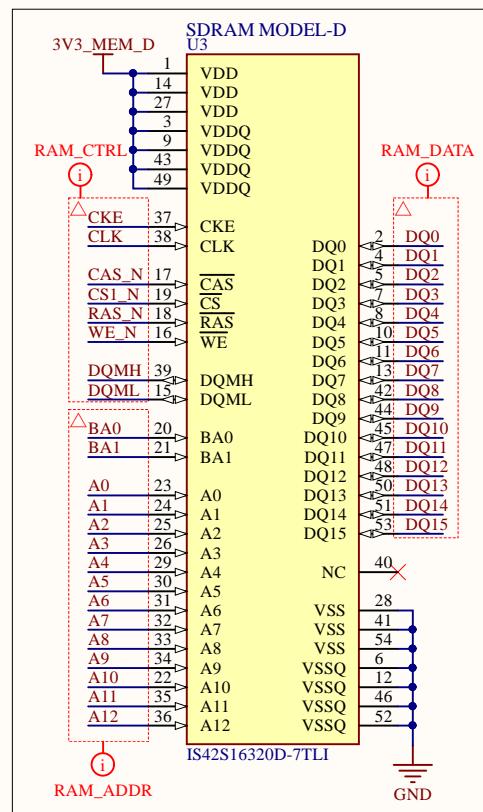
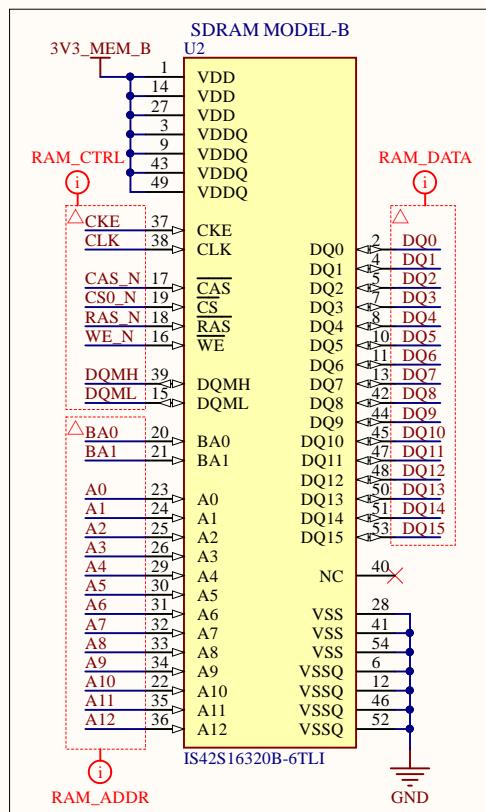
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Title: **HARSH Payload Topology**Size: **A4** Project: **HARSH_Payload.PjPCB** Revision: **1.0**Date: **4/27/2020** Time: **6:15:18 PM** Sheet **3** of **8**Drawn By: **Andre Martins Pio de Mattos** Model: **HARSH_DB**

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Title: **HARSH Payload SDRAM memories**

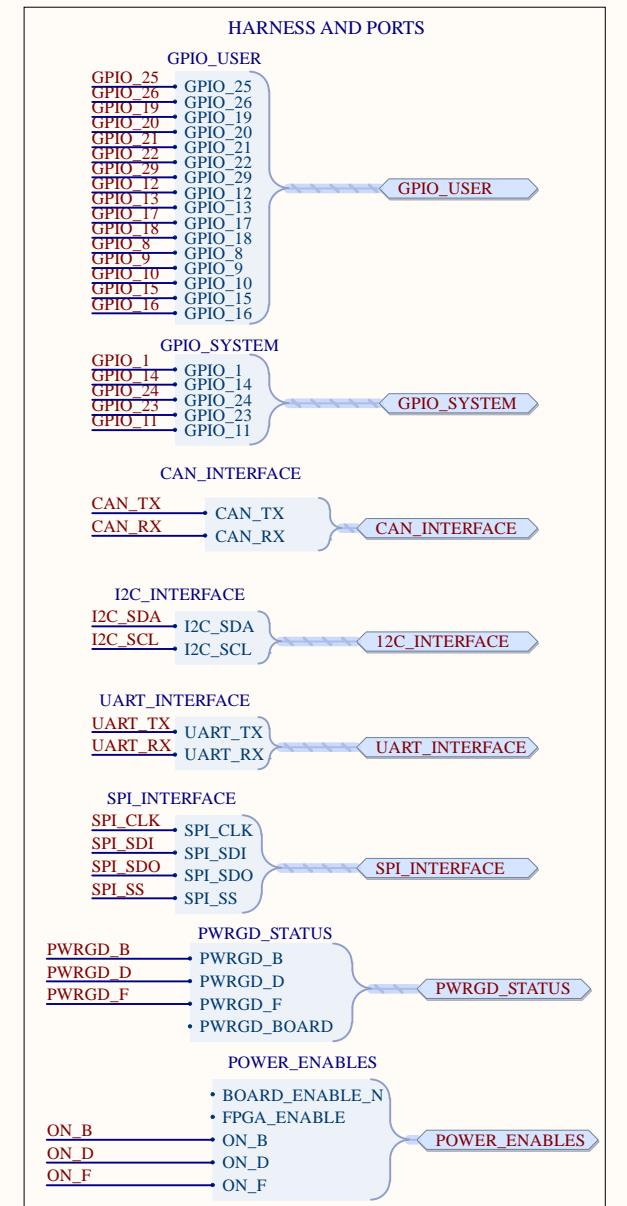
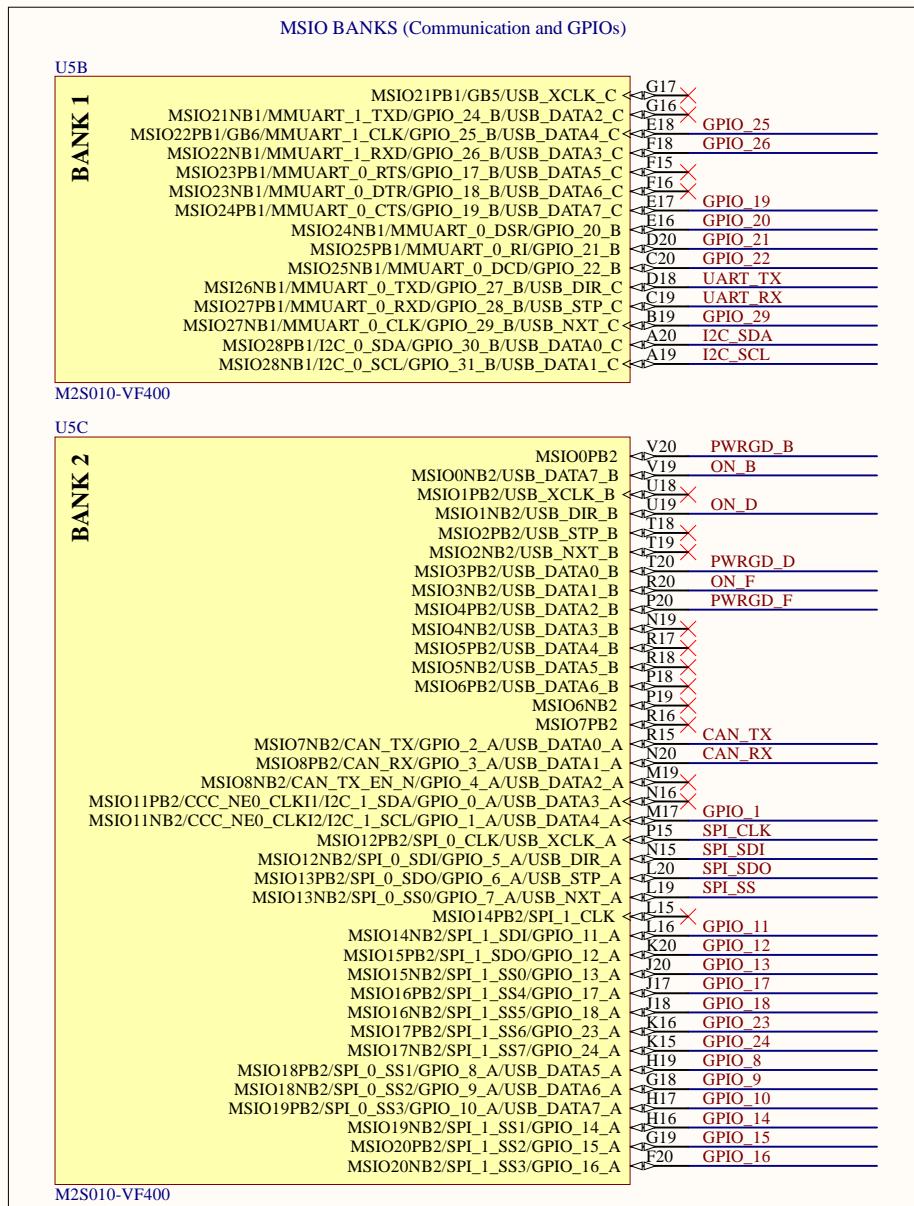
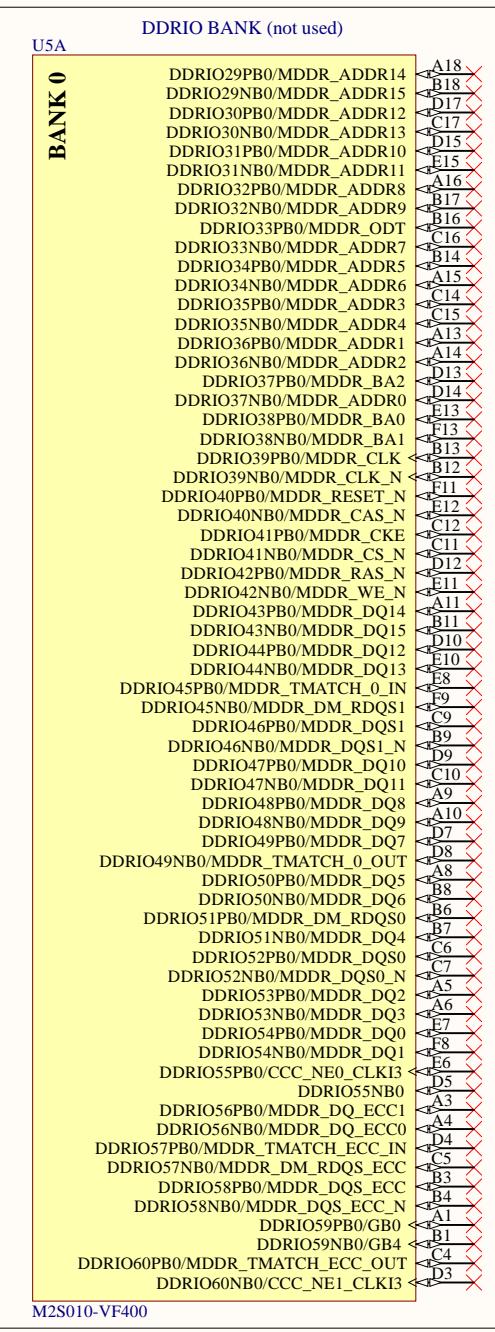
Size: **A4** Project: HARSH_Payload.PrjPCB Revision: 1.0

Date: 4/27/2020 Time: 6:15:18 PM Sheet 4 of 8

Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

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Title: HARSH Payload FPGA Banks 0_2

Size: A4 Project: HARSH_Payload.PrjPCB Revision: 1.0

Date: 4/27/2020 Time: 6:15:19 PM Sheet 5 of 8

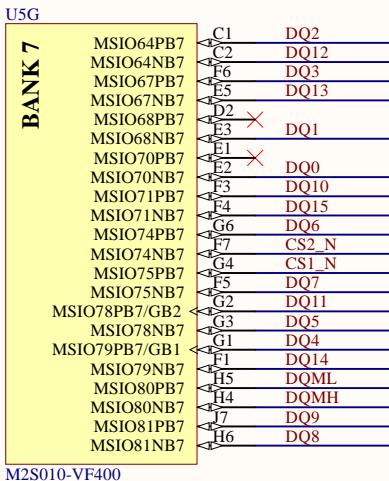
Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

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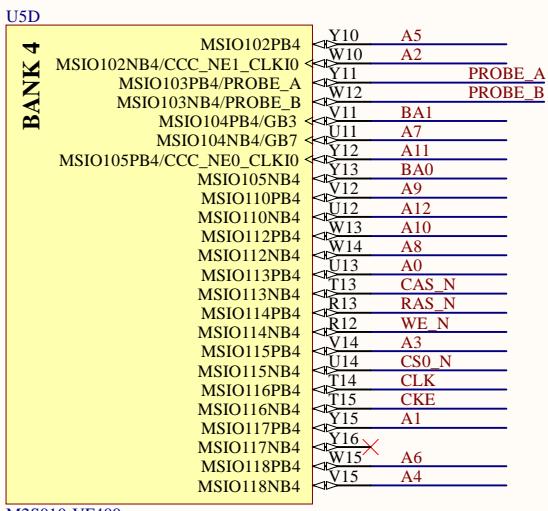
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MSIO BANKS (memories)

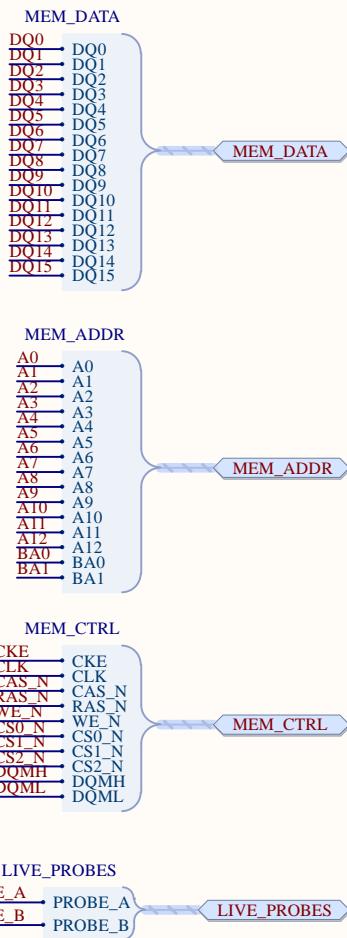
SDRAM data and control signals



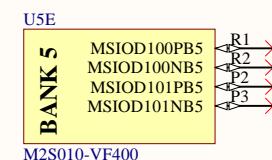
SDRAM address and control signals



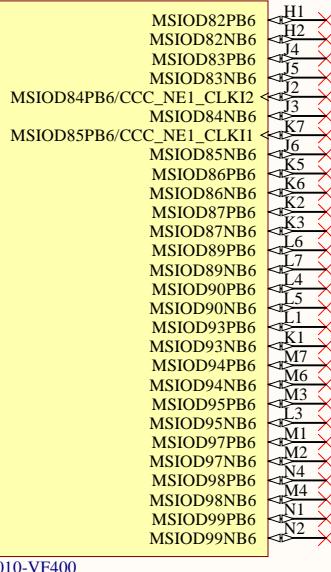
HARNESS AND PORTS



MSIOD BANKS (not used)



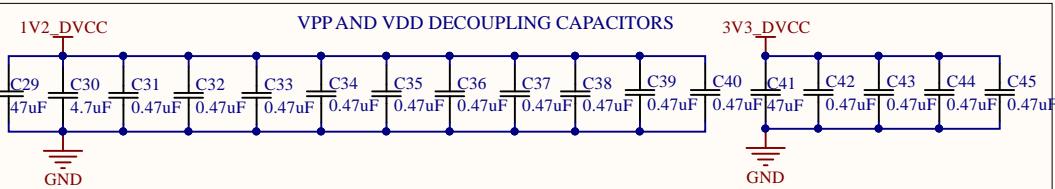
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Title: HARSH Payload FPGA Banks 4_7	Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.0
Date: 4/27/2020	Time: 6:15:19 PM	Sheet 6 of 8	
Drawn By: Andre Martins Pio de Mattos	Model: HARSH_DB		

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VPP AND VDD DECOUPLING CAPACITORS

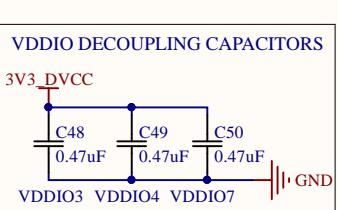
FPGA CLOCK SUBSYSTEM REFERENCE

U5J

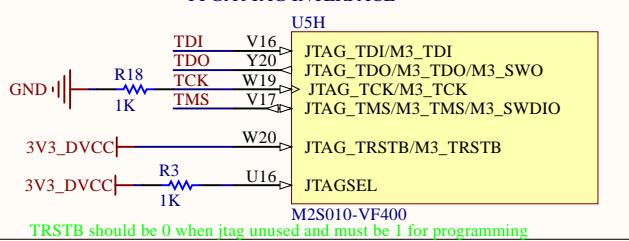
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CCC_NE0_NE1_MSS_MDDR_PLL_VSSA

M2S010-VF400

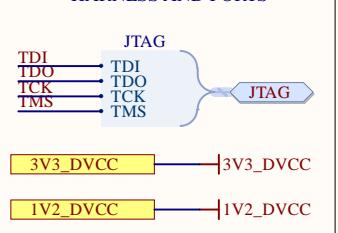
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FPGA JTAG INTERFACE

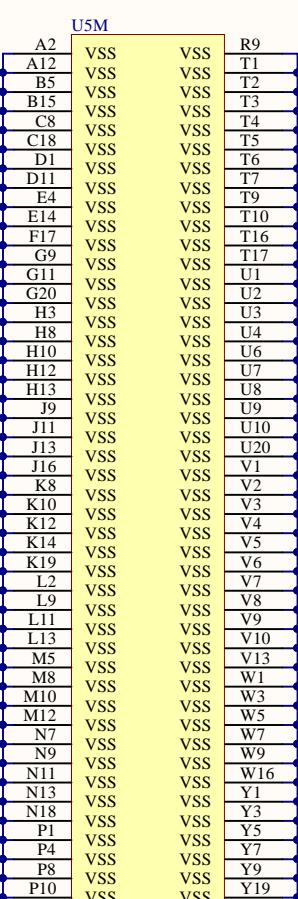


Harness and Ports

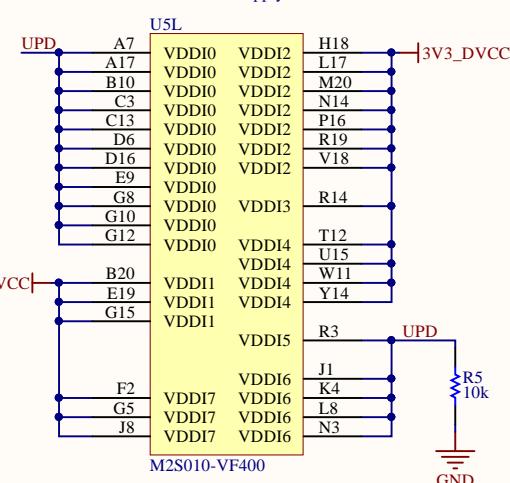


FPGA POWER CONNECTIONS

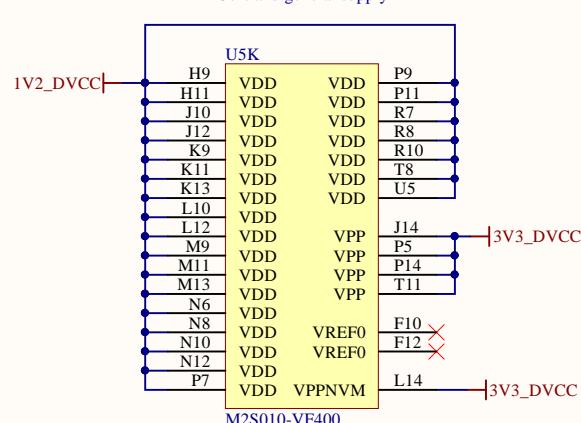
Ground connections



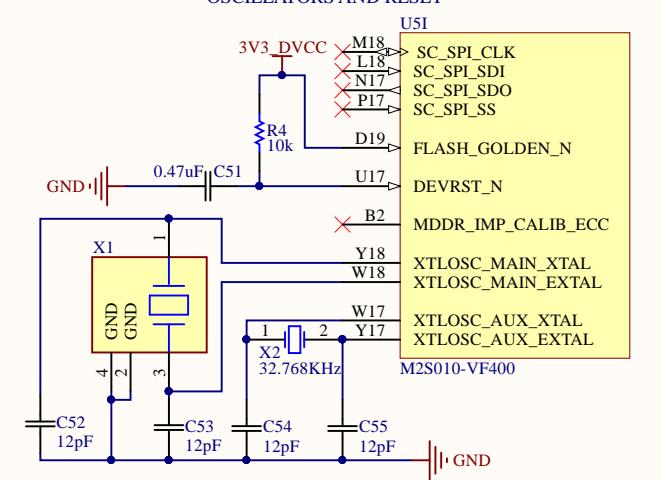
IO banks suppl



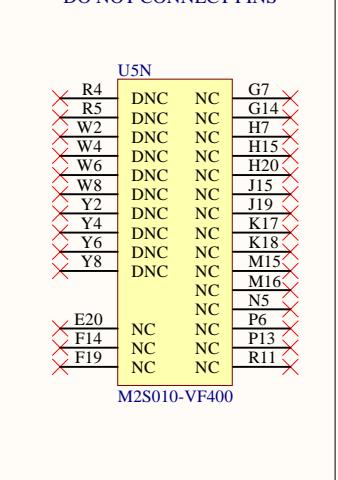
Core and general supply



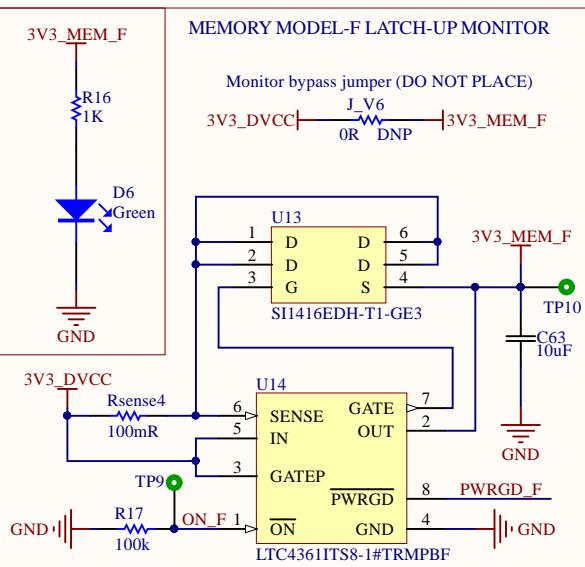
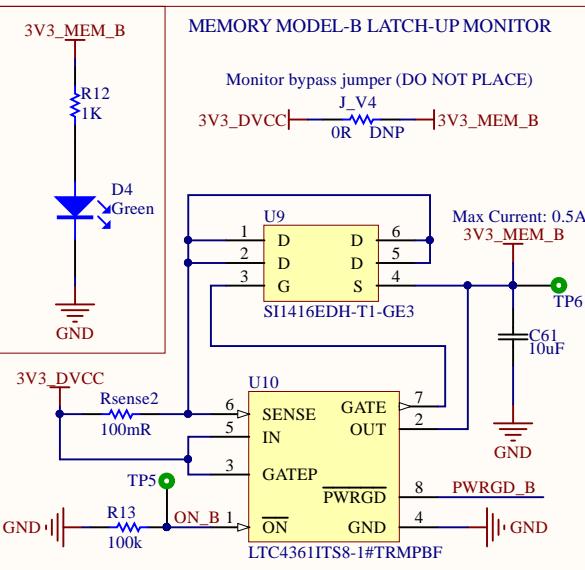
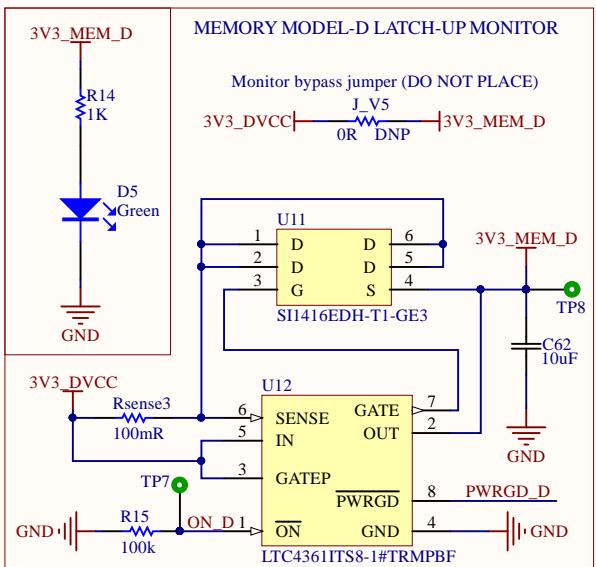
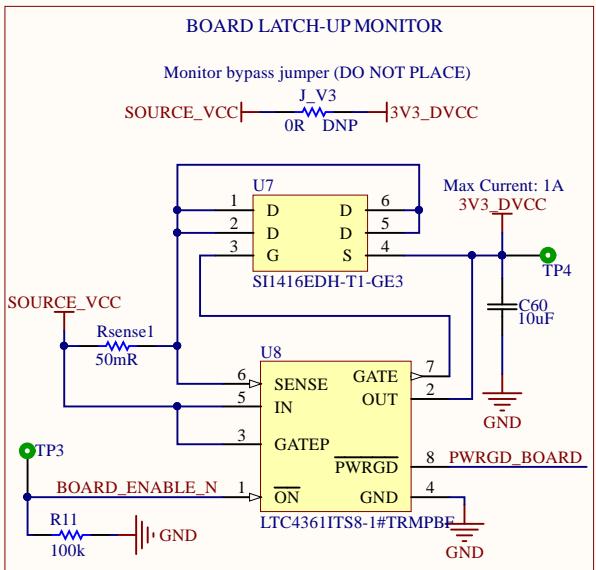
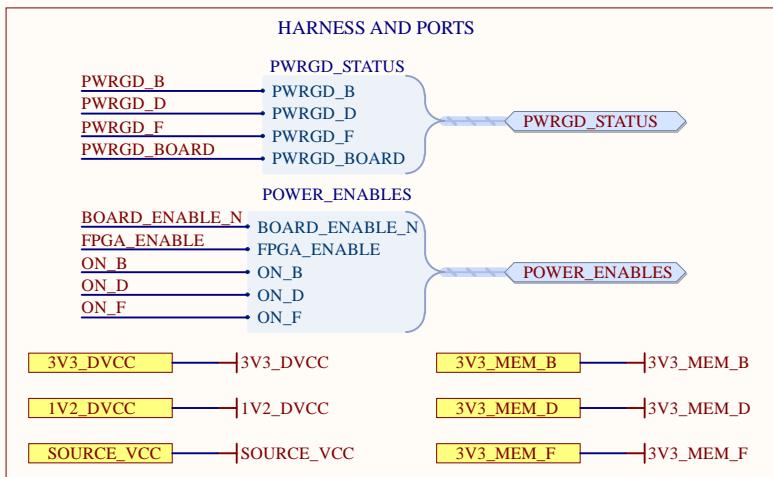
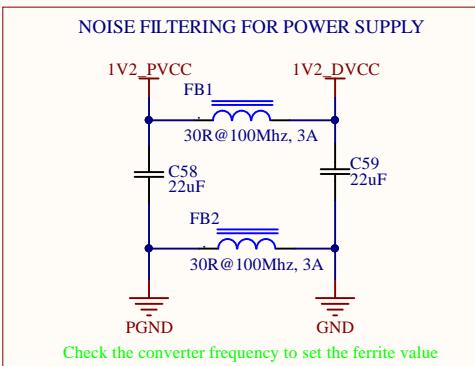
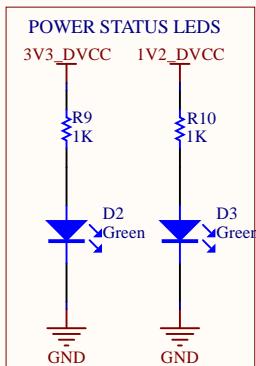
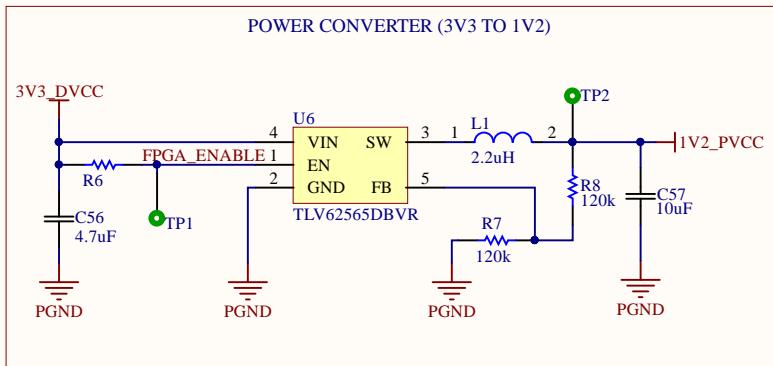
OSCILLATORS AND RESET



DO NOT CONNECT PINS



Title: HARSH Payload FPGA Miscellaneous			<i>UFSC - SpaceLab University Campus - Trindade Dep. of Electrical Engineering - CTC Florianópolis, Santa Catarina, Brazil CEP: 88040 - 900</i>	Cannot open file C:\Users\yanaz\OneDrive\Área de Trabalho\SpaceLab\Id entidadeVisual\docs
Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.0		
Date: 4/27/2020	Time: 6:15:19 PM	Sheet 7 of 8		
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB		



Title: **HARSH Payload Power Supply**

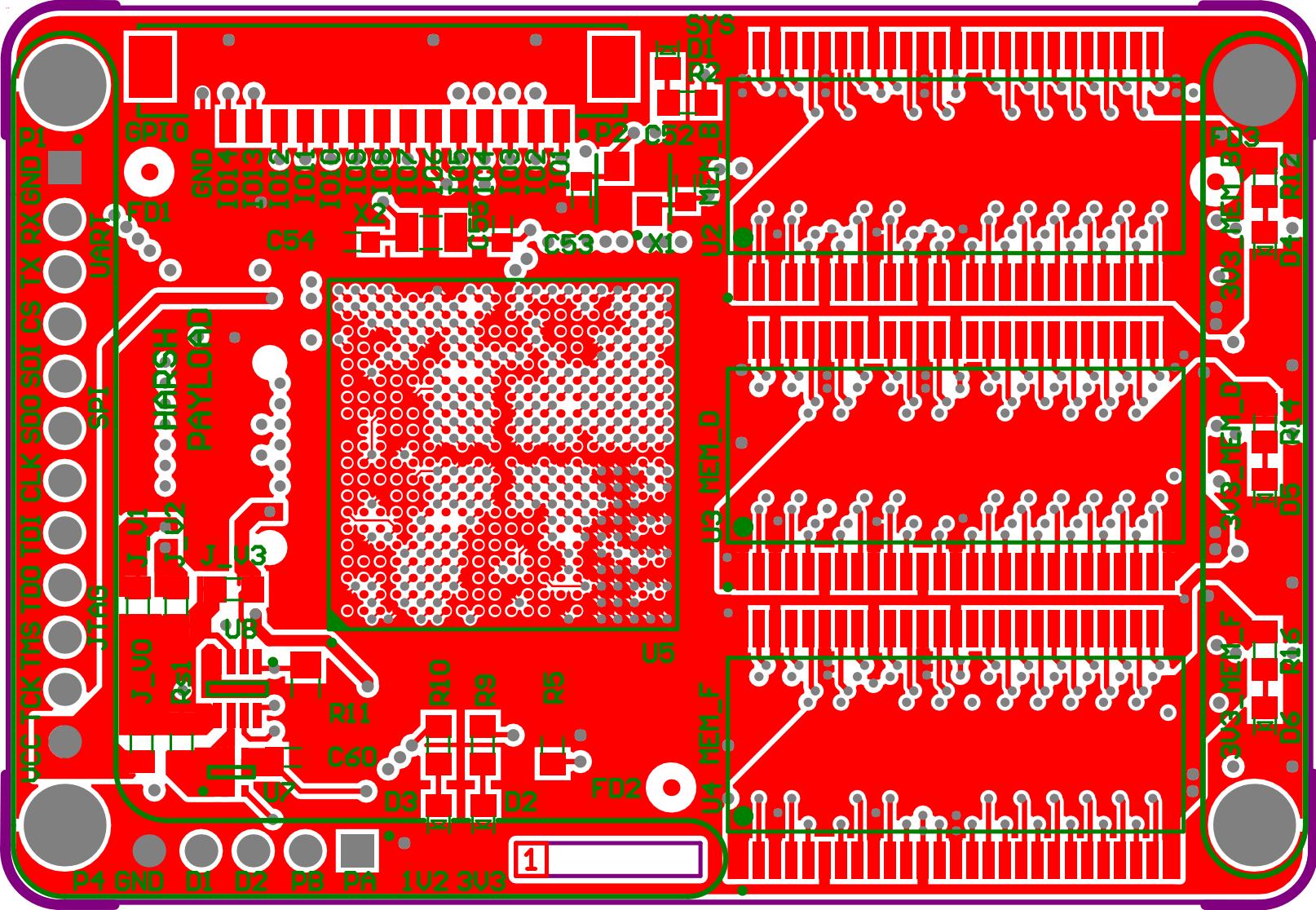
Size: A4 Project: HARSH_Payload.PrjPCB Revision: 1.0

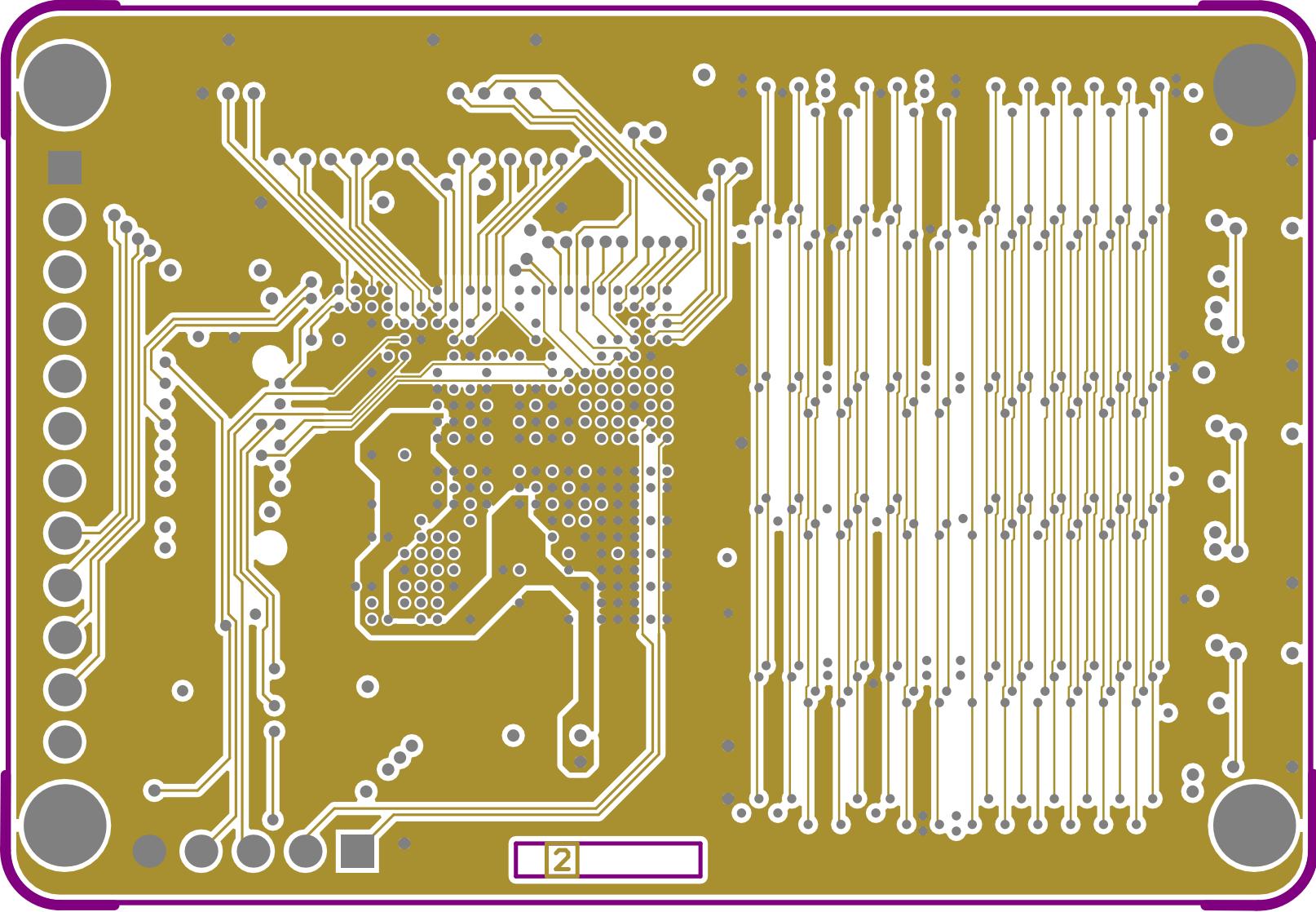
Date: 4/27/2020 Time: 6:15:20 PM Sheet 8 of 8

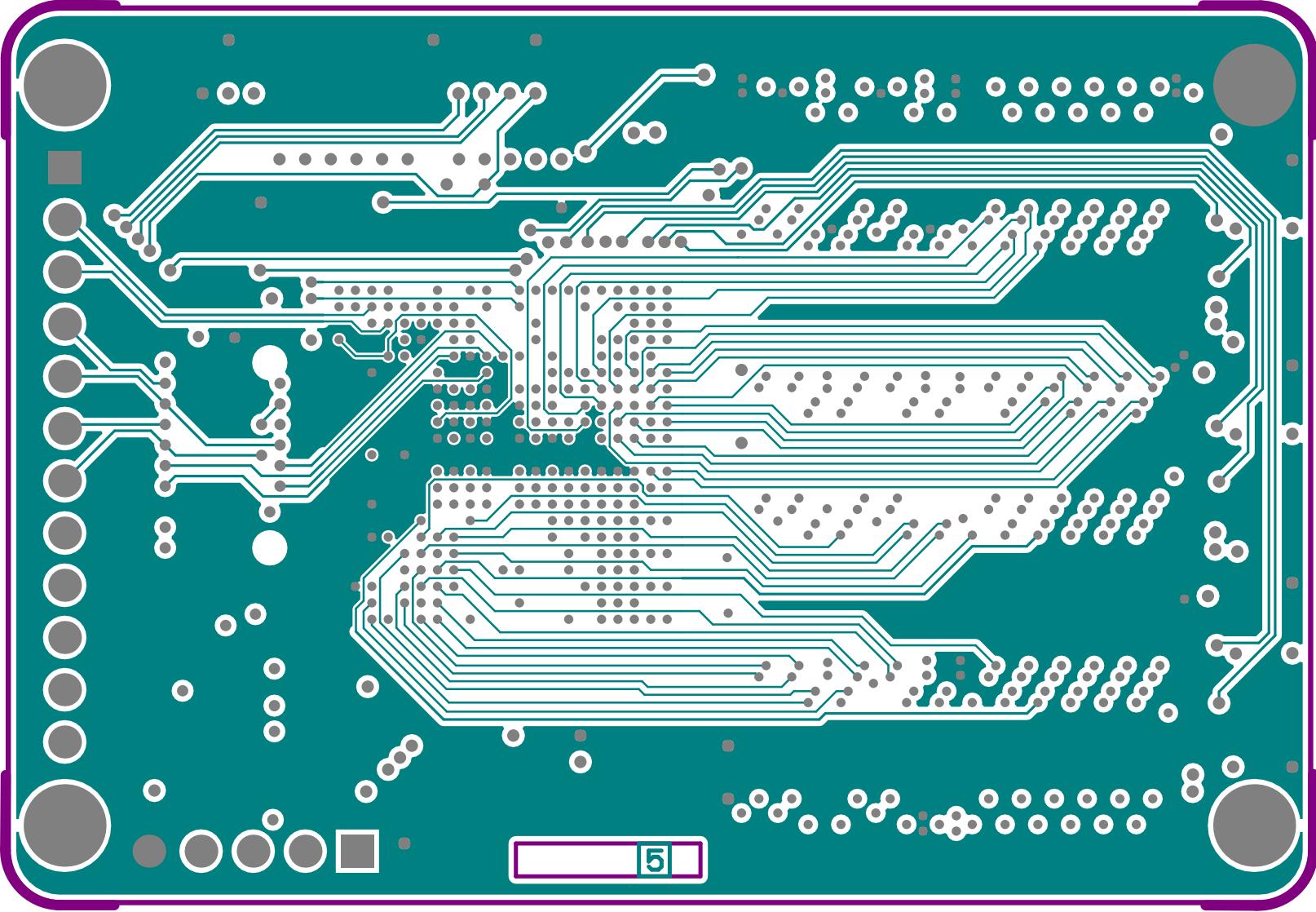
Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

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