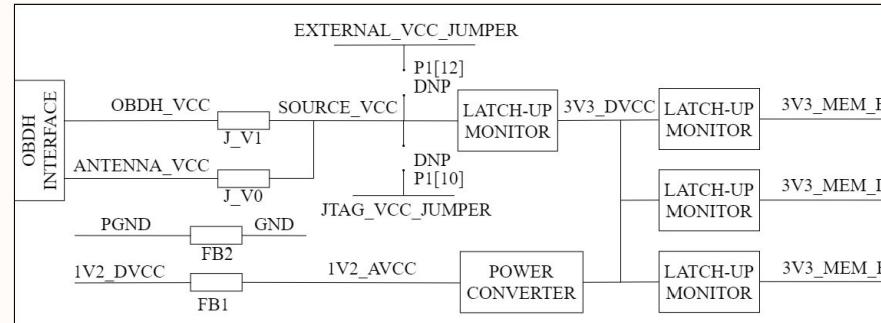
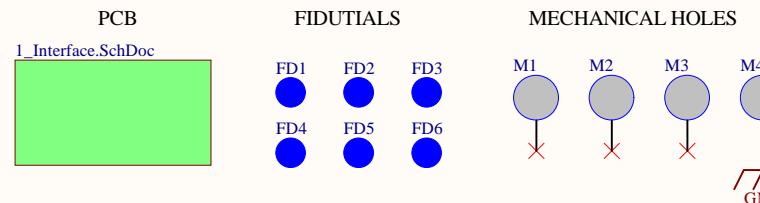


| Rev | Description      | Date        | Author             |
|-----|------------------|-------------|--------------------|
| 1.0 | Initial release. | 30-Apr-2020 | Andre M. P. Mattos |
|     |                  |             |                    |
|     |                  |             |                    |
|     |                  |             |                    |



Power Diagram

### Revision History



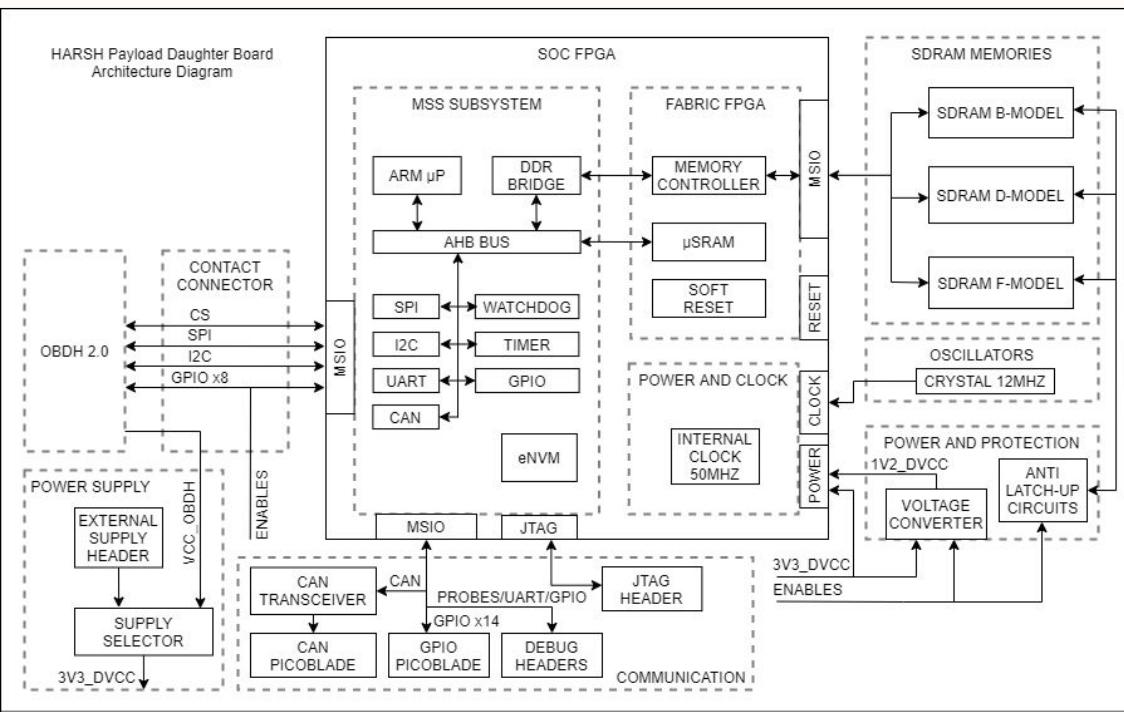
### PCB Elements

HARSH Payload Daughter Board (HARSH\_Payload) for OBDH 2.0 ALT Hardware

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by UFSC and LIRMM.

- Drawn by: André Martins Pio de Mattos.
- Reviewers: Yan Castro de Azeredo.
- Based on OBDH 2.0 designed by: André Martins Pio de Mattos.
- Based on DB\_Memory designed by: Yan Castro de Azeredo.
- Support: Kleber Reis Gouveia Júnior.

### Project Information

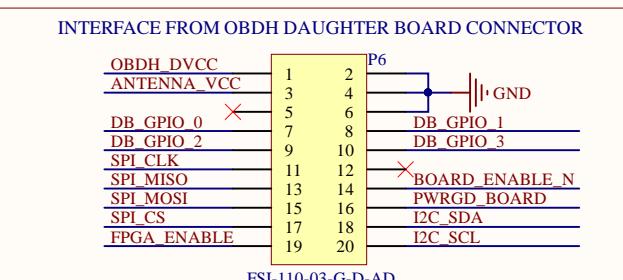
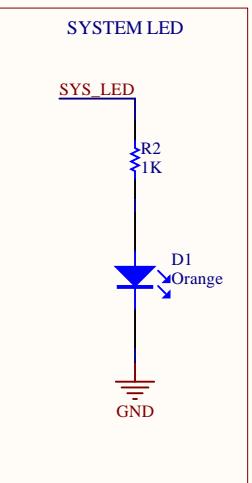
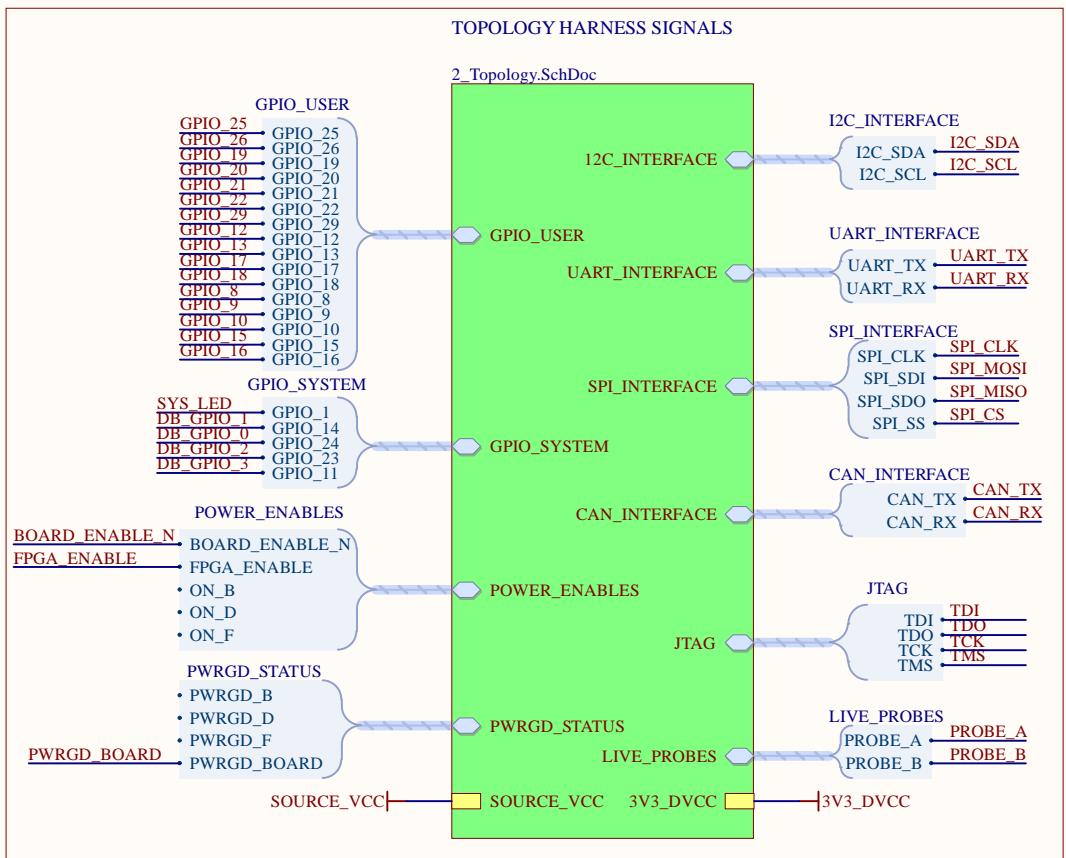
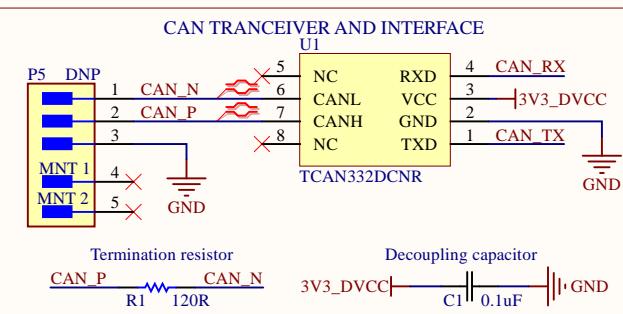
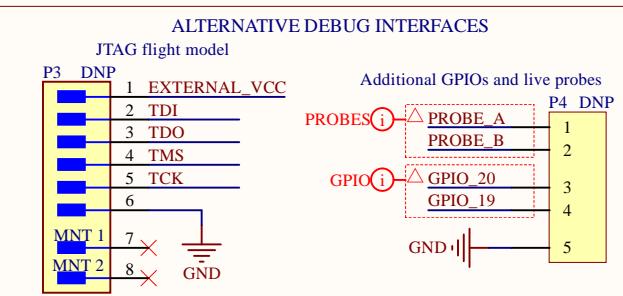
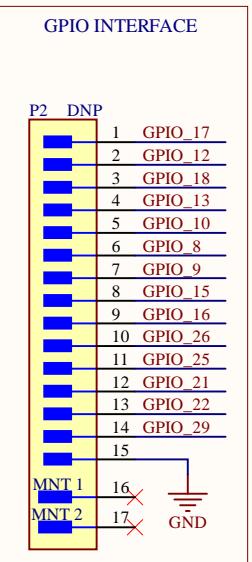
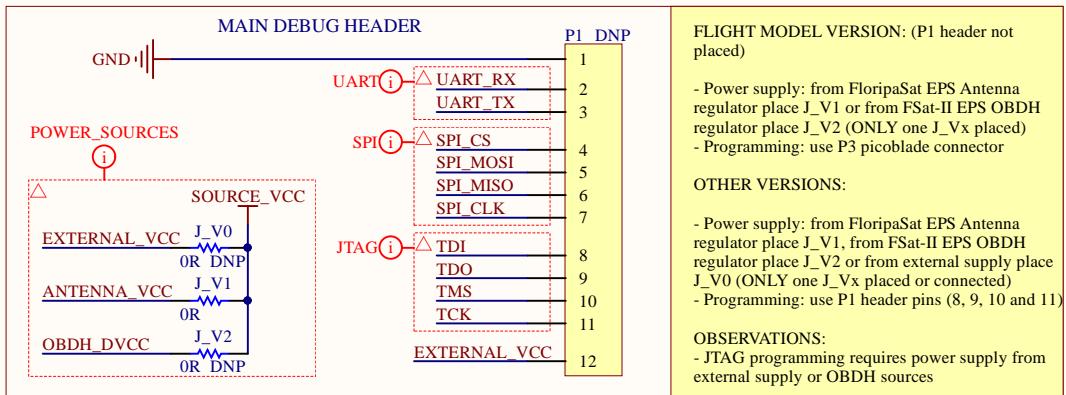


Block Diagram

| Title: HARSH Payload Architecture     |                              |               |
|---------------------------------------|------------------------------|---------------|
| Size: A4                              | Project: HARSH_Payload.PjPCB | Revision: 1.0 |
| Date: 4/25/2020                       | Time: 10:49:28 PM            | Sheet 1 of 8  |
| Drawn By: Andre Martins Pio de Mattos | Model: HARSH_DB              |               |

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Features not used from the generic daughter board interface connector:

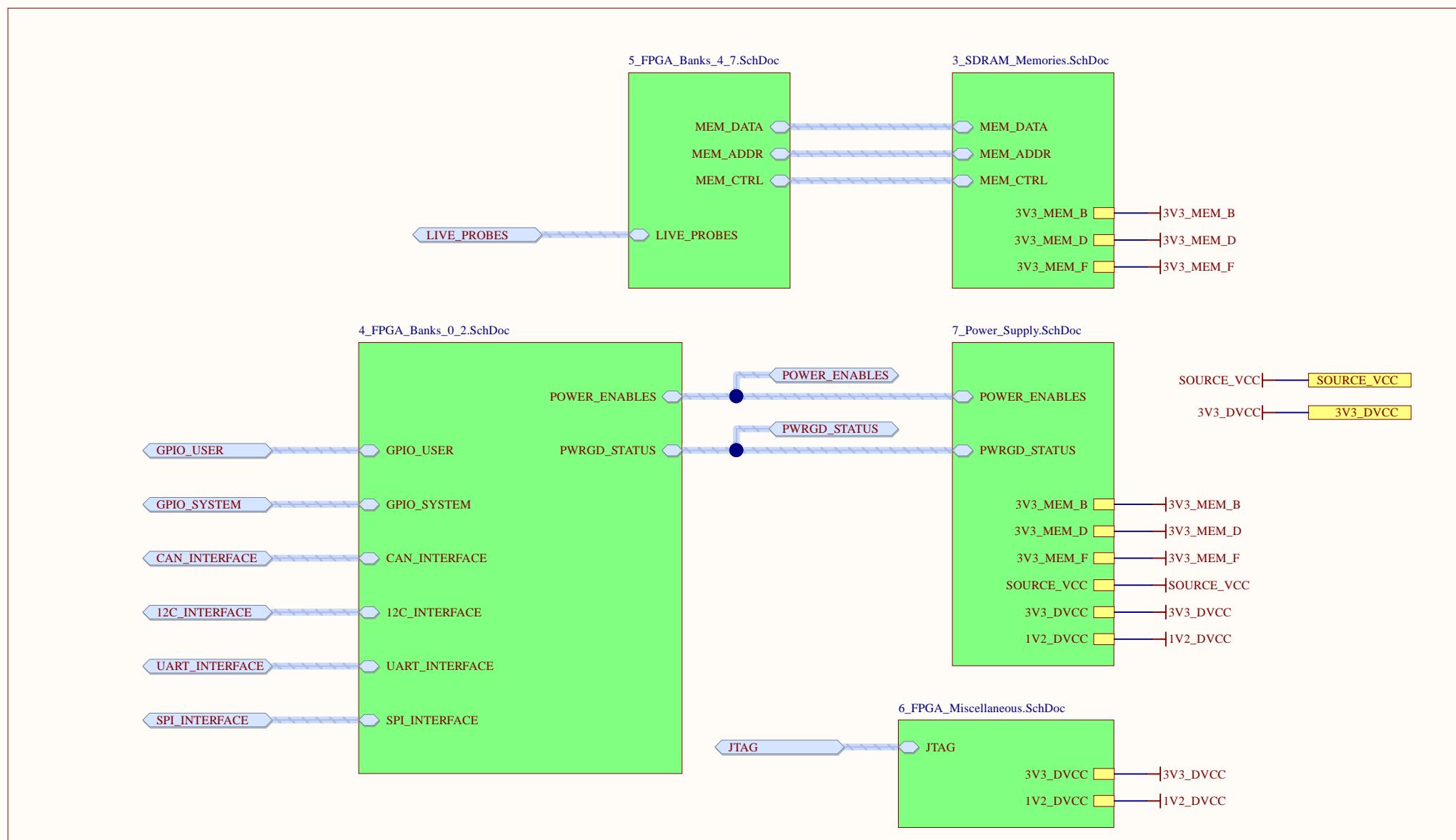
- BATTERY VCC
- Features used differently, but compatible, in the generic daughter board interface connector:
  - DB\_CS2 as GPIO for FPGA enable (Active High)
  - DB\_ADC0 as GPIO for board "power good" status (feedback of payload power status)
  - DB\_ADC1 as GPIO for board enable (Active Low)

According to SAMTEC product specification, the maximum body height of the connector when pressed should be 3.28 mm.

| Title: HARSH Payload Interface        |                               |                 |
|---------------------------------------|-------------------------------|-----------------|
| Size: A4                              | Project: HARSH_Payload.PrjPCB | Revision: 1.0   |
| Date: 4/25/2020                       | Time: 10:49:29 PM             | Sheet 2 of 8    |
| Drawn By: Andre Martins Pio de Mattos |                               | Model: HARSH_DB |

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Title: **HARSH Payload Topology**

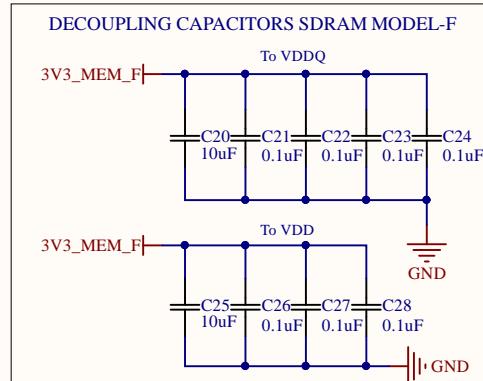
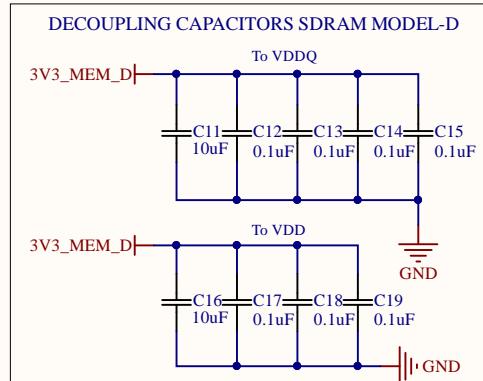
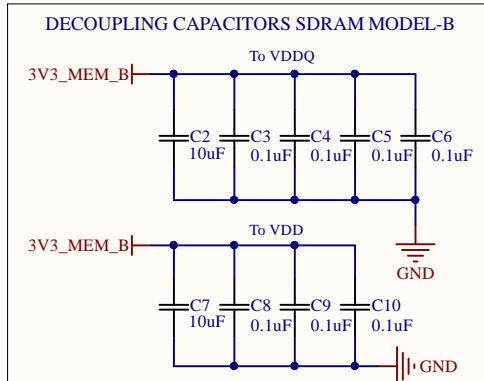
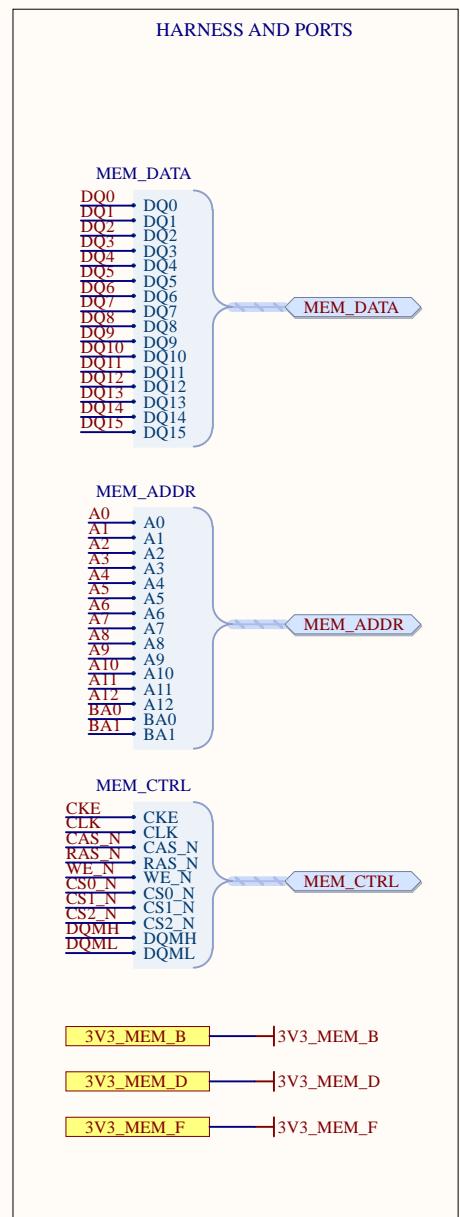
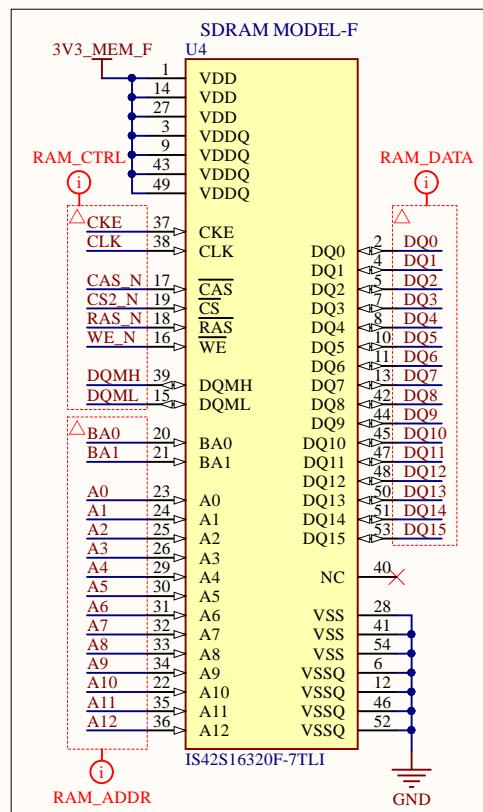
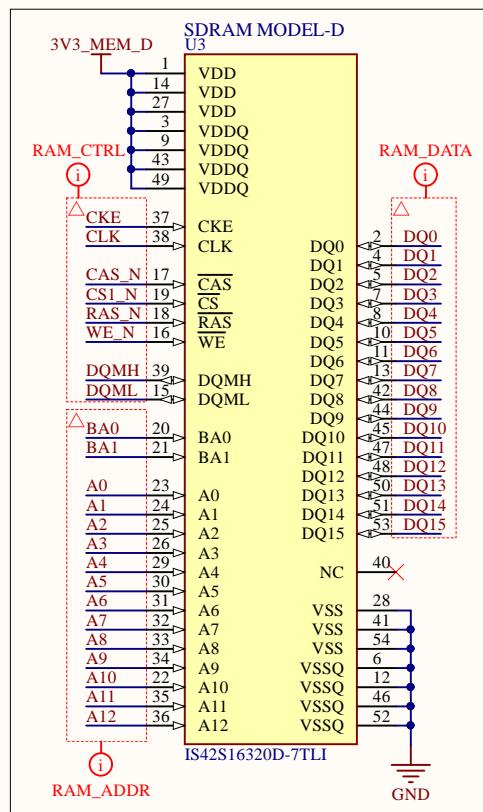
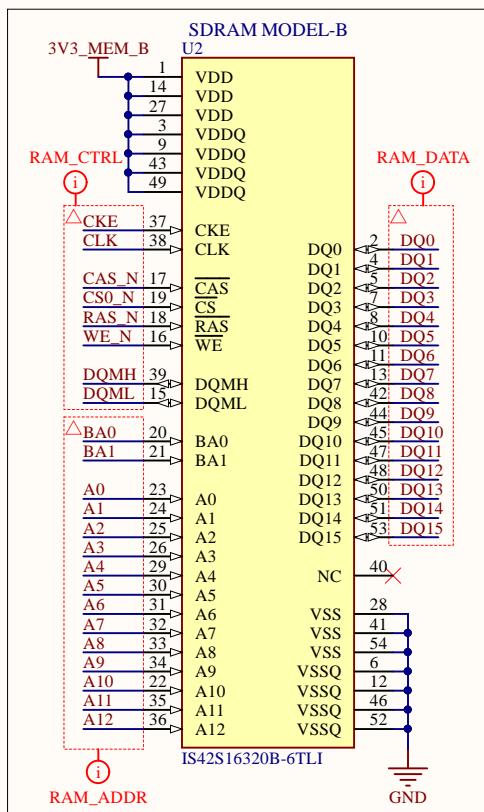
|                 |                                     |                      |
|-----------------|-------------------------------------|----------------------|
| Size: <b>A4</b> | Project: <b>HARSH_Payload.PjPCB</b> | Revision: <b>1.0</b> |
|-----------------|-------------------------------------|----------------------|

|                        |                          |                            |
|------------------------|--------------------------|----------------------------|
| Date: <b>4/25/2020</b> | Time: <b>10:49:29 PM</b> | Sheet <b>3</b> of <b>8</b> |
|------------------------|--------------------------|----------------------------|

|  |                        |
|--|------------------------|
| Drawn By: <b>Andre Martins Pio de Mattos</b> | Model: <b>HARSH_DB</b> |
|--|------------------------|

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Title: **HARSH Payload SDRAM memories**

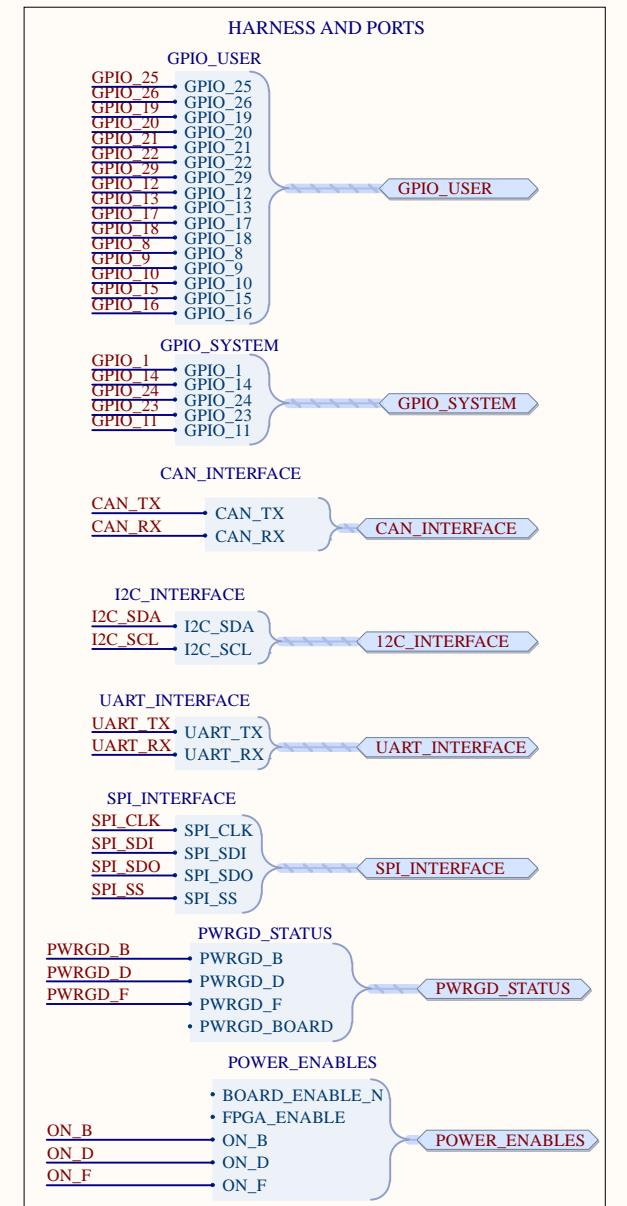
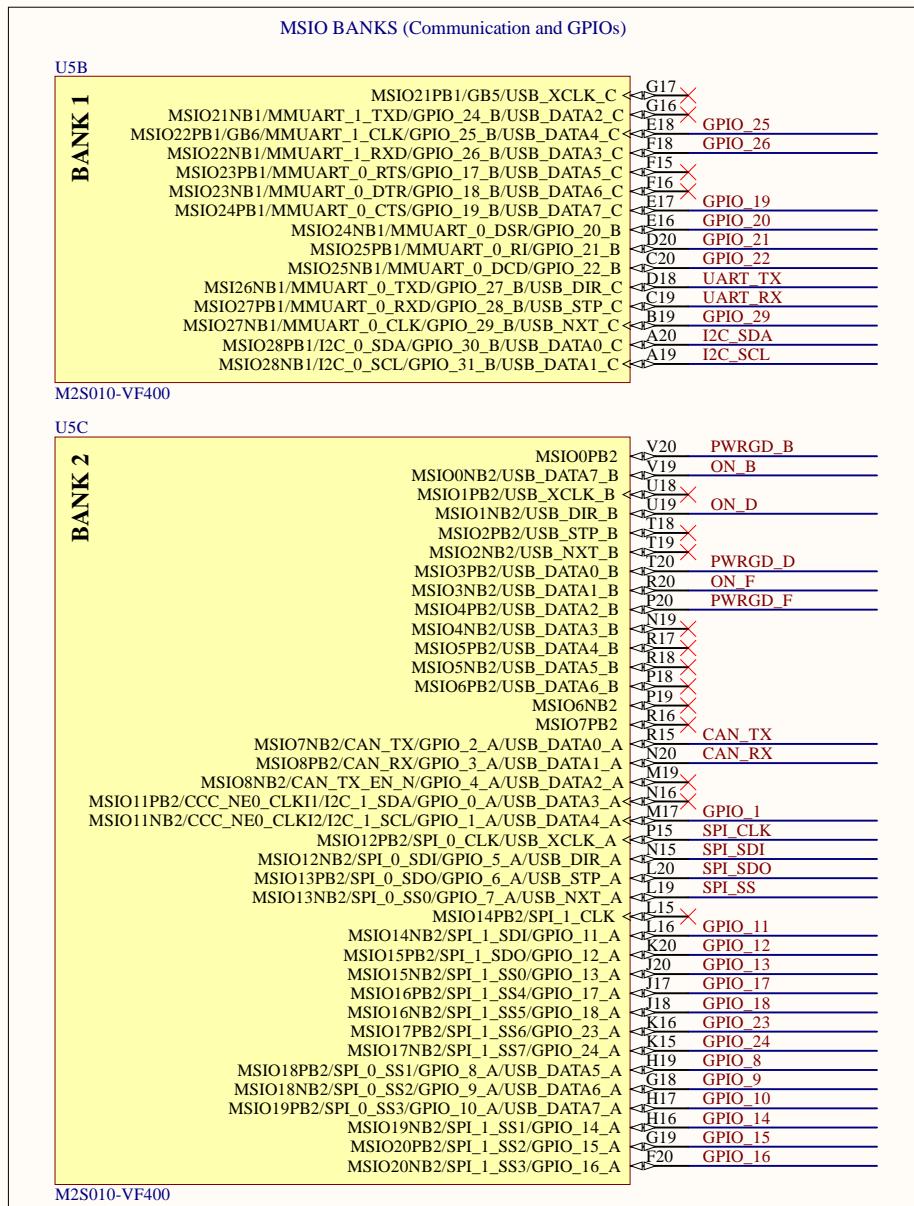
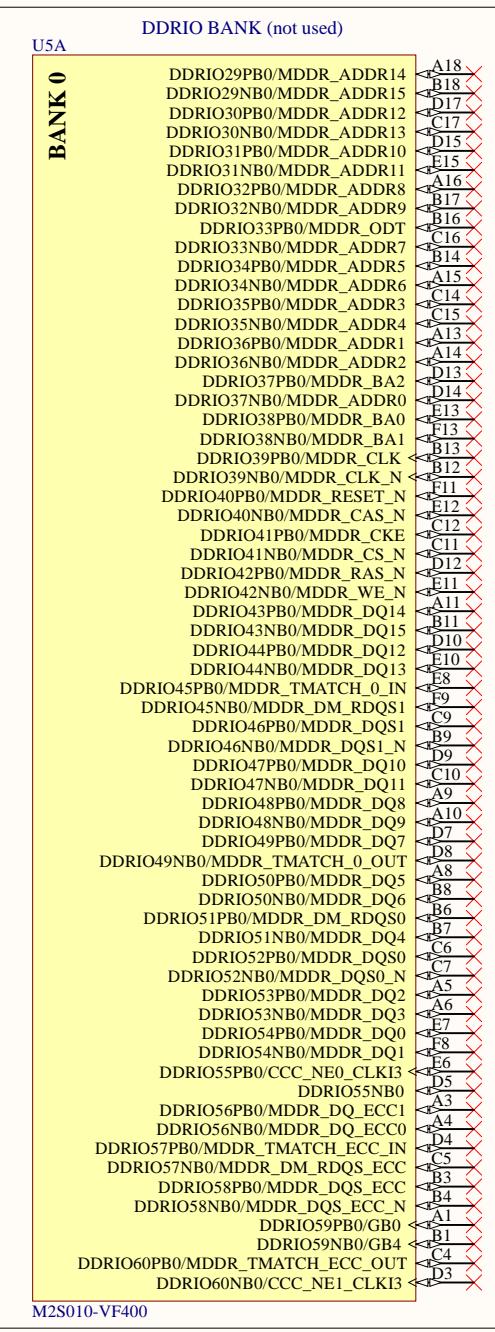
Size: **A4** Project: HARSH\_Payload.PrjPCB Revision: 1.0

Date: 4/25/2020 Time: 10:49:29 PM Sheet 4 of 8

Drawn By: Andre Martins Pio de Mattos Model: HARSH\_DB

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Title: HARSH Payload FPGA Banks 0\_2

Size: A4 Project: HARSH\_Payload.PrjPCB Revision: 1.0

Date: 4/25/2020 Time: 10:49:29 PM Sheet 5 of 8

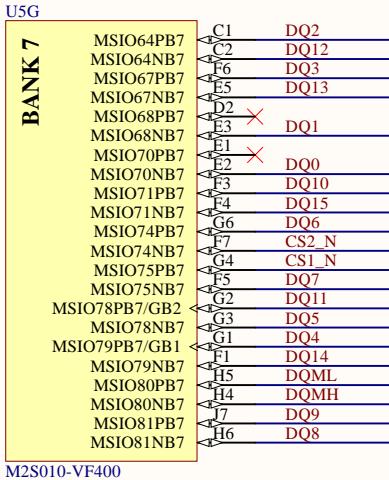
Drawn By: Andre Martins Pio de Mattos Model: HARSH\_DB

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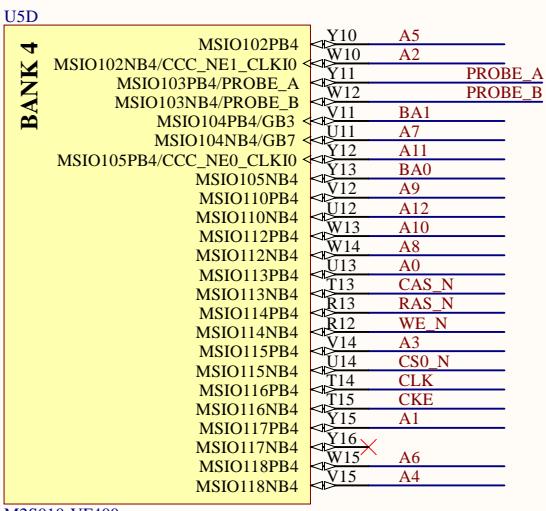
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## MSIO BANKS (memories)

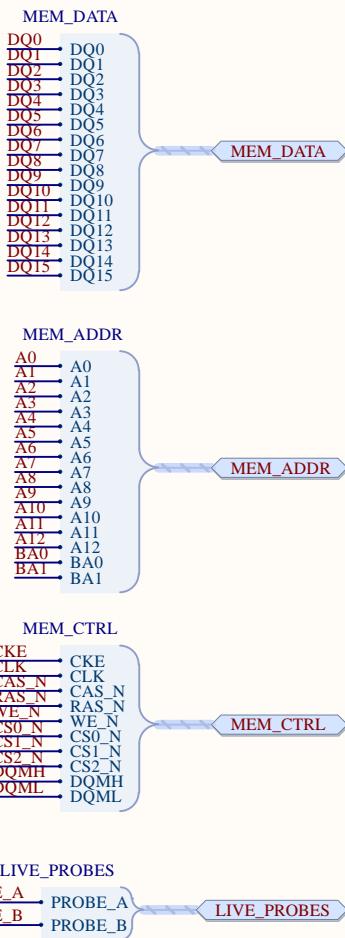
SDRAM data and control signals



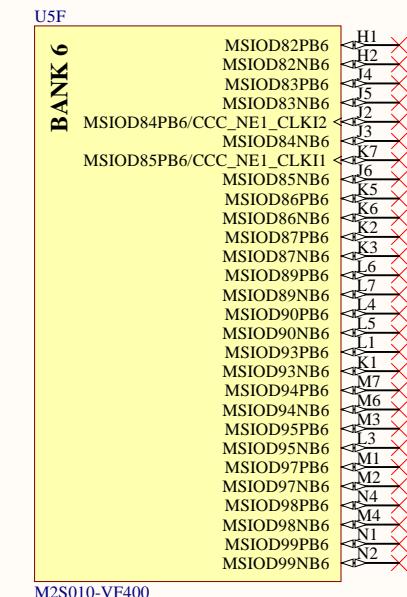
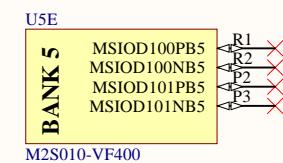
SDRAM address and control signals



## HARNESS AND PORTS



## MSIOD BANKS (not used)



Title: HARSH Payload FPGA Banks 4\_7

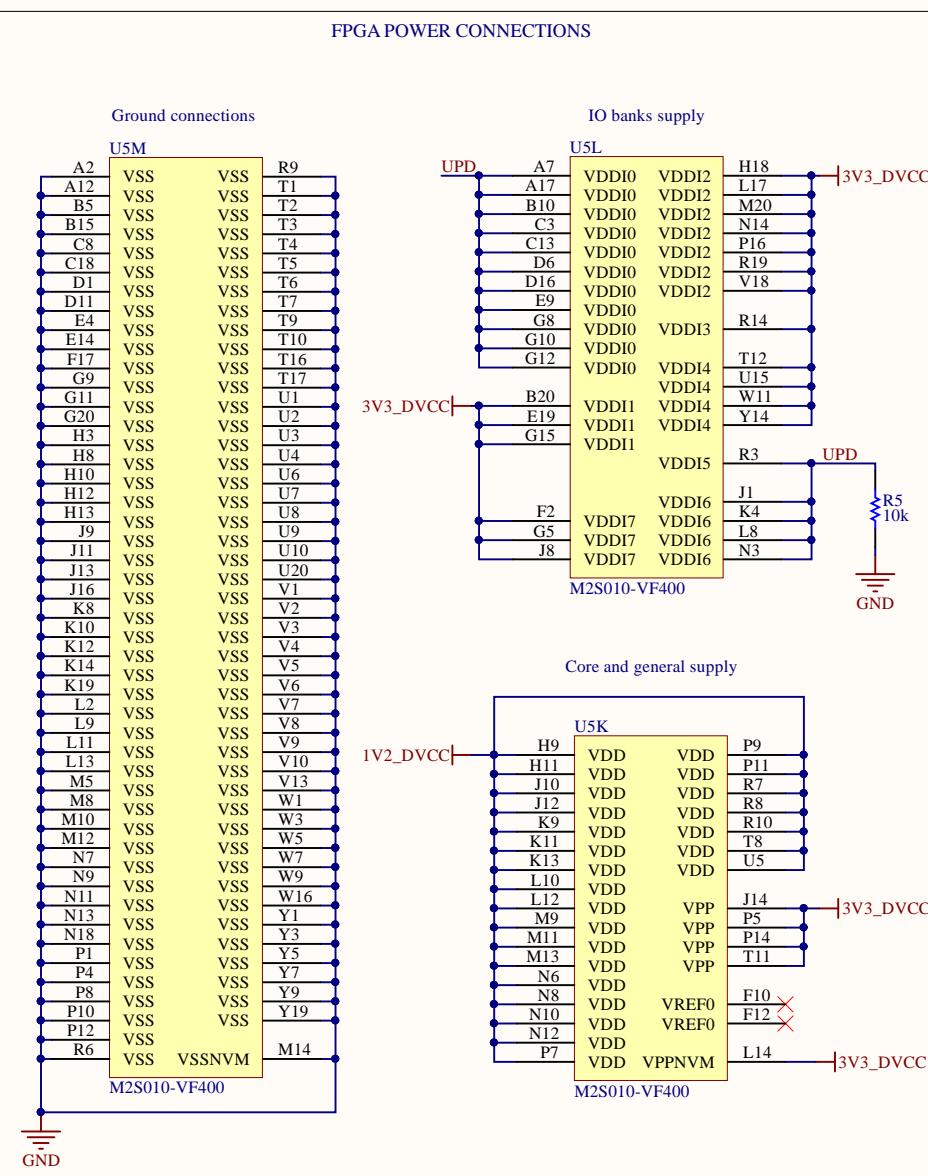
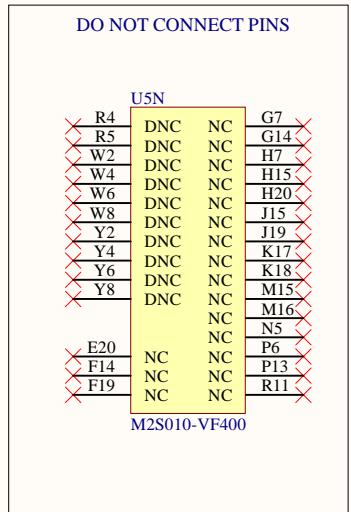
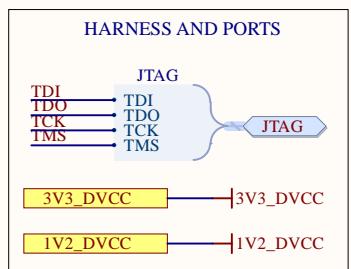
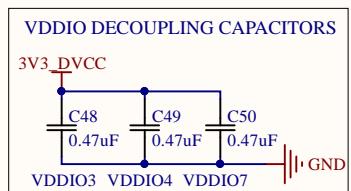
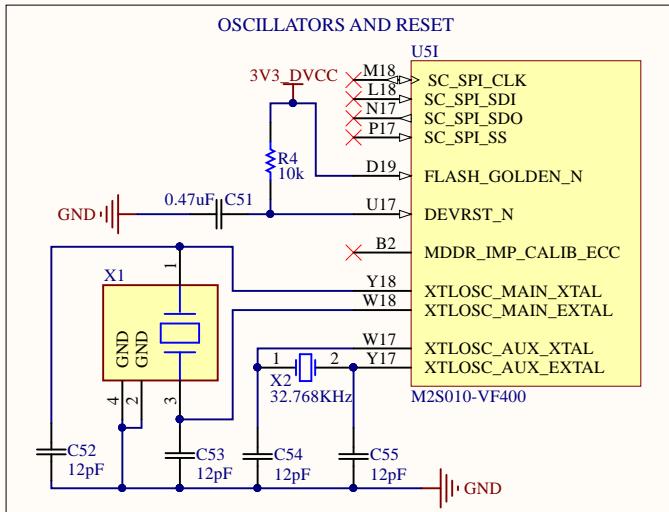
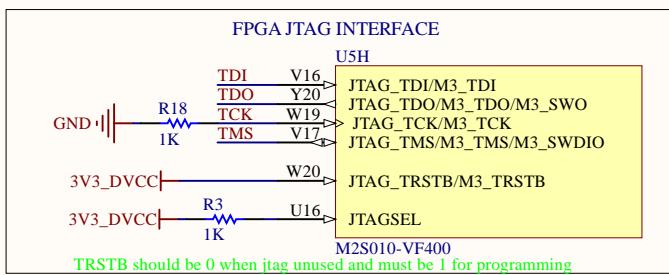
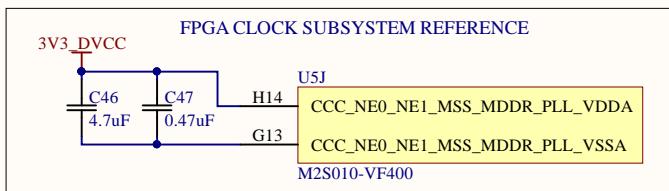
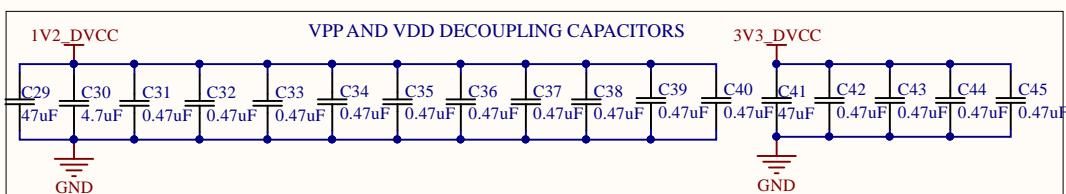
Size: A4 Project: HARSH\_Payload.PrjPCB Revision: 1.0

Date: 4/25/2020 Time: 10:49:30 PM Sheet 6 of 8

Drawn By: Andre Martins Pio de Mattos Model: HARSH\_DB

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**Title: HARSH Payload FPGA Miscellaneous**

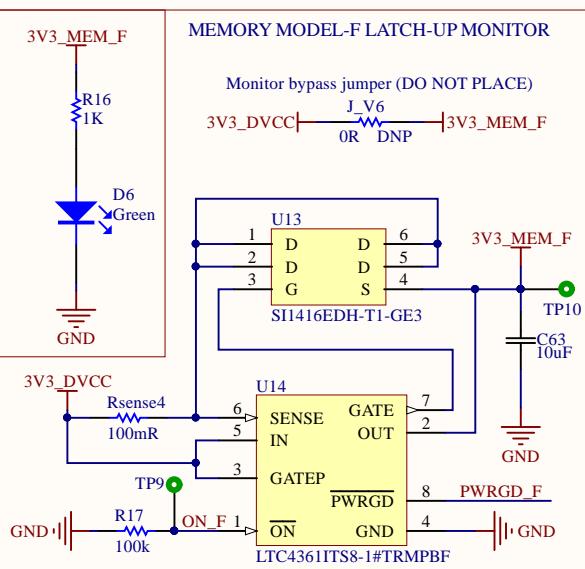
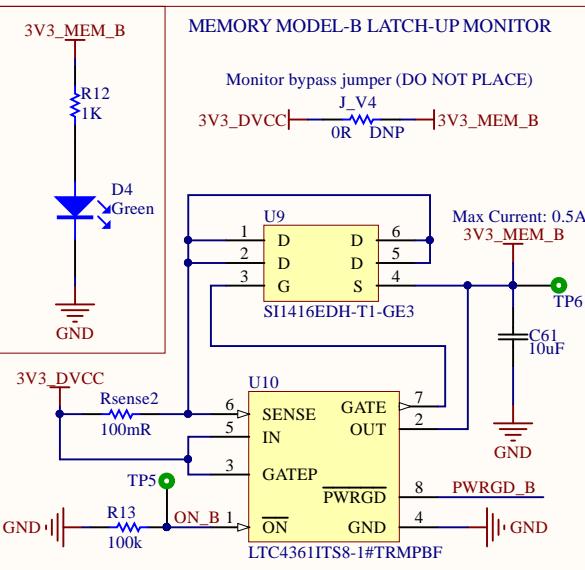
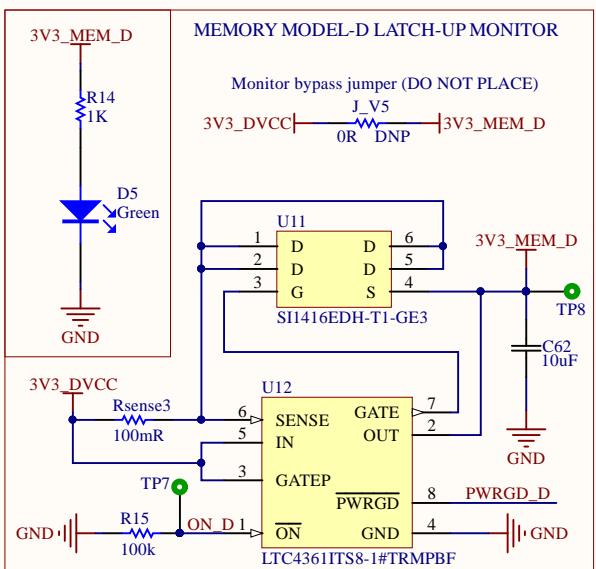
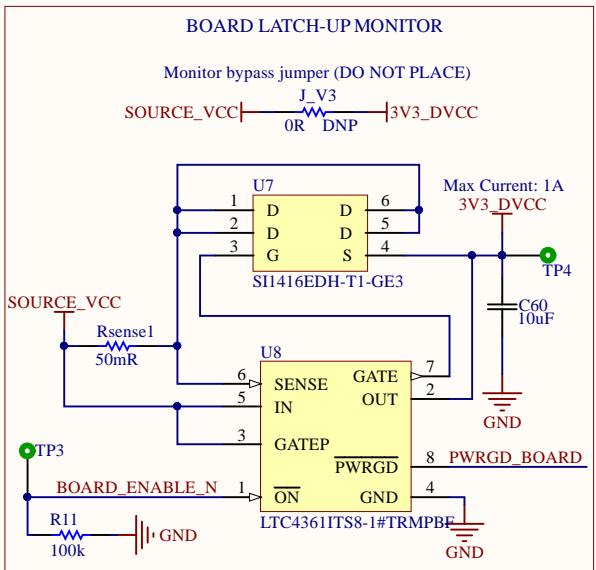
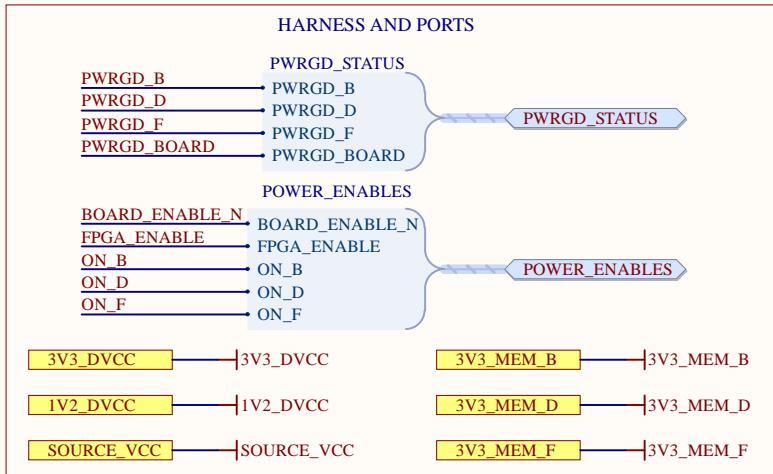
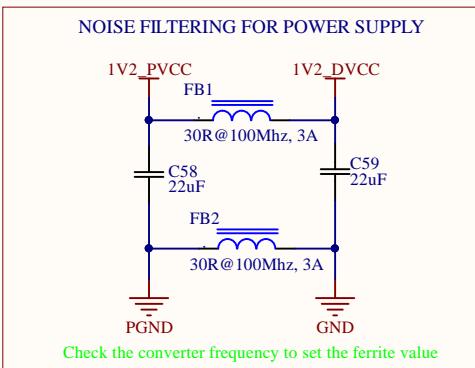
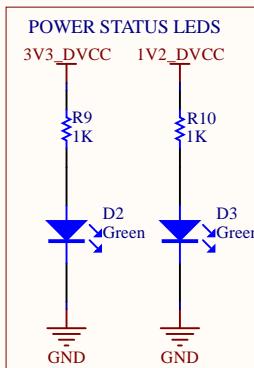
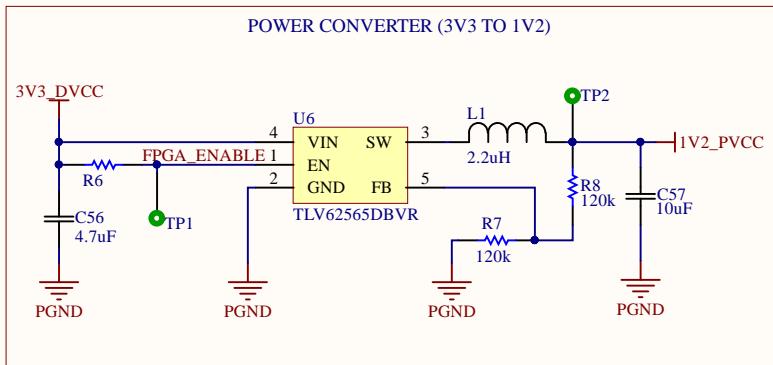
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Date: 4/25/2020 Time: 10:49:30 PM Sheet 7 of 8

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Title: **HARSH Payload Power Supply**

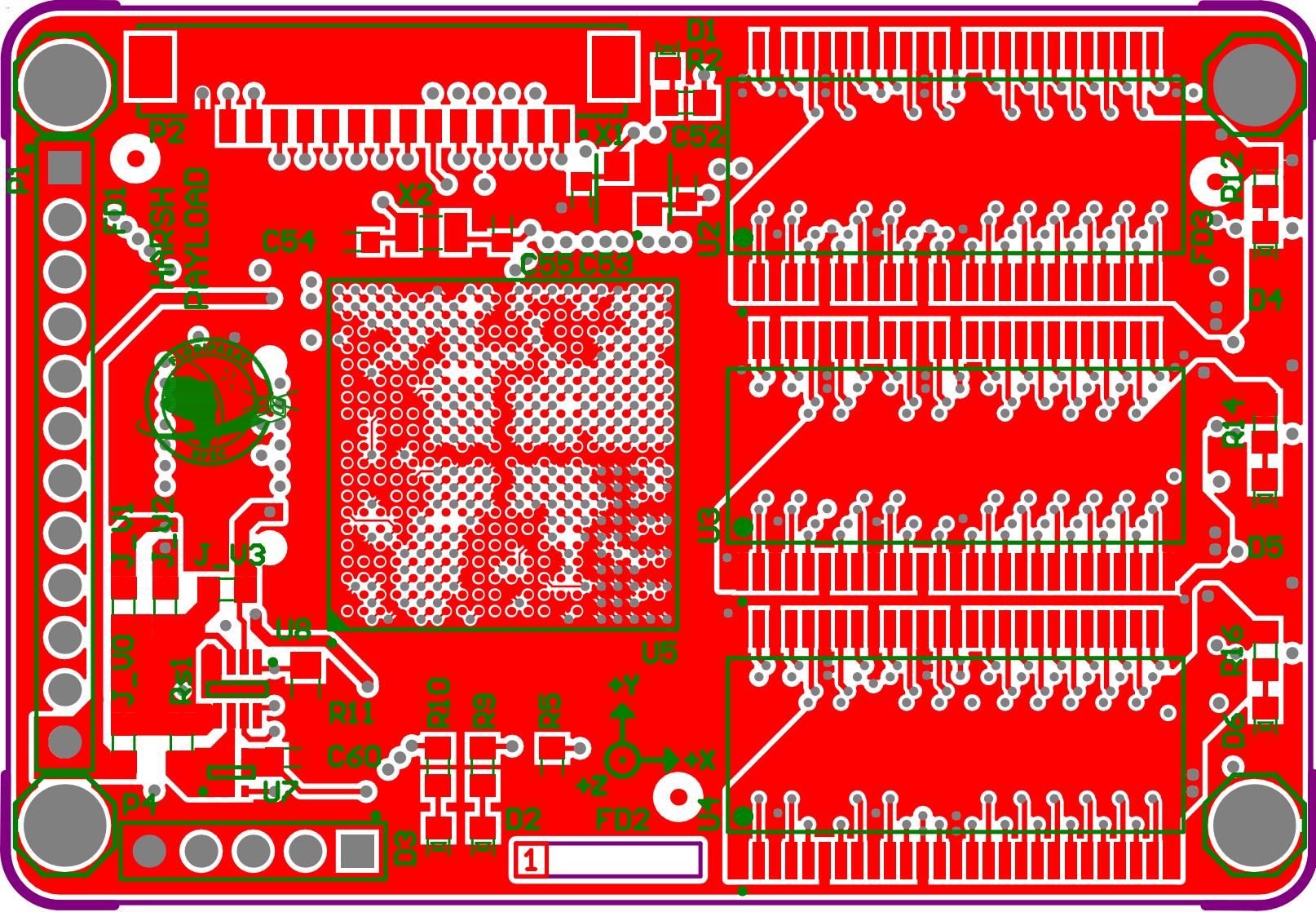
Size: A4 Project: HARSH\_Payload.PrjPCB Revision: 1.0

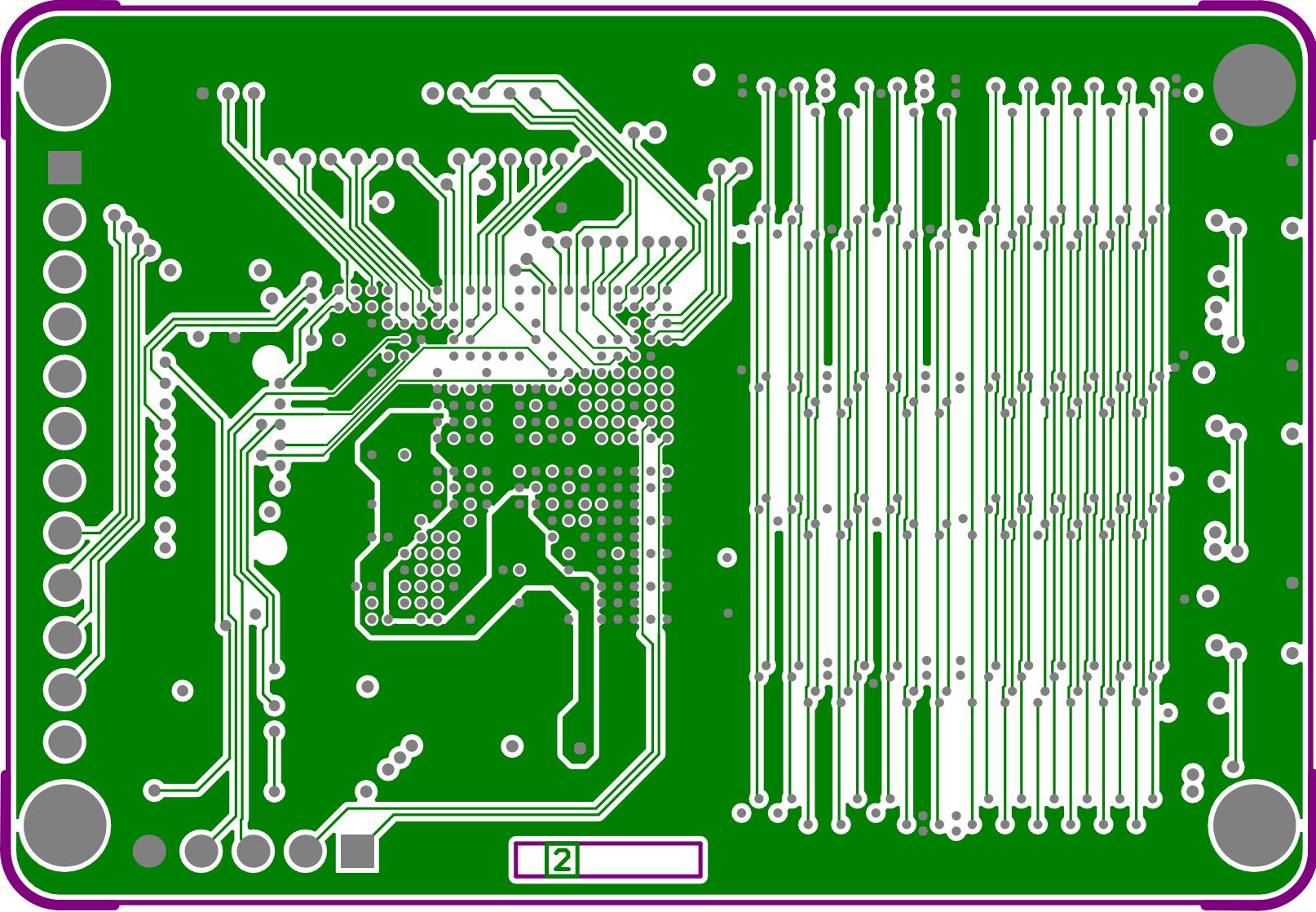
Date: 4/25/2020 Time: 10:49:31 PM Sheet 8 of 8

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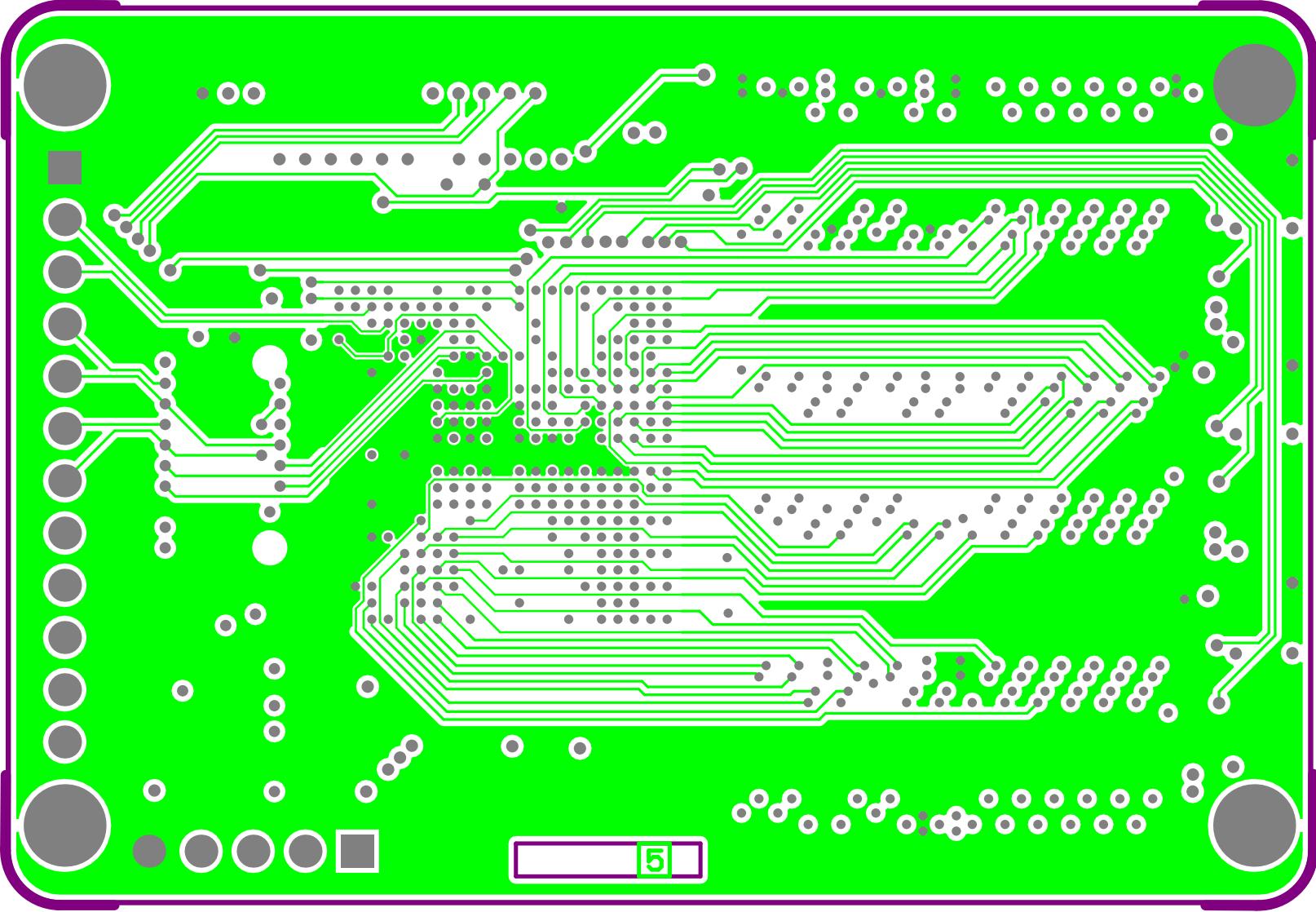
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