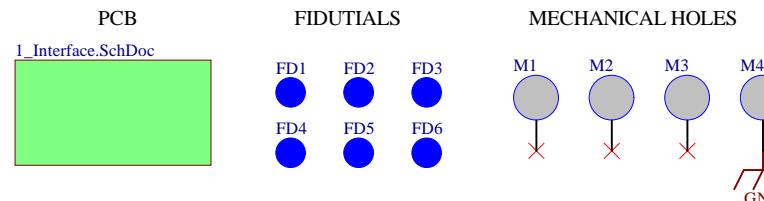


Rev	Description	Date	Author
1.0	Initial release.	30-Apr-2020	Andre M. P. Mattos
1.1	Review updates.	28-May-2020	Andre M. P. Mattos

Revision History



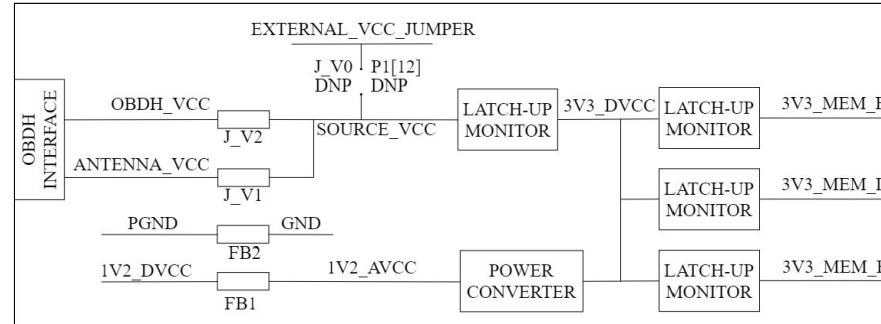
PCB Elements

HARSH Payload Daughter Board
(HARSH_Payload) for OBDH 2.0 Hardware

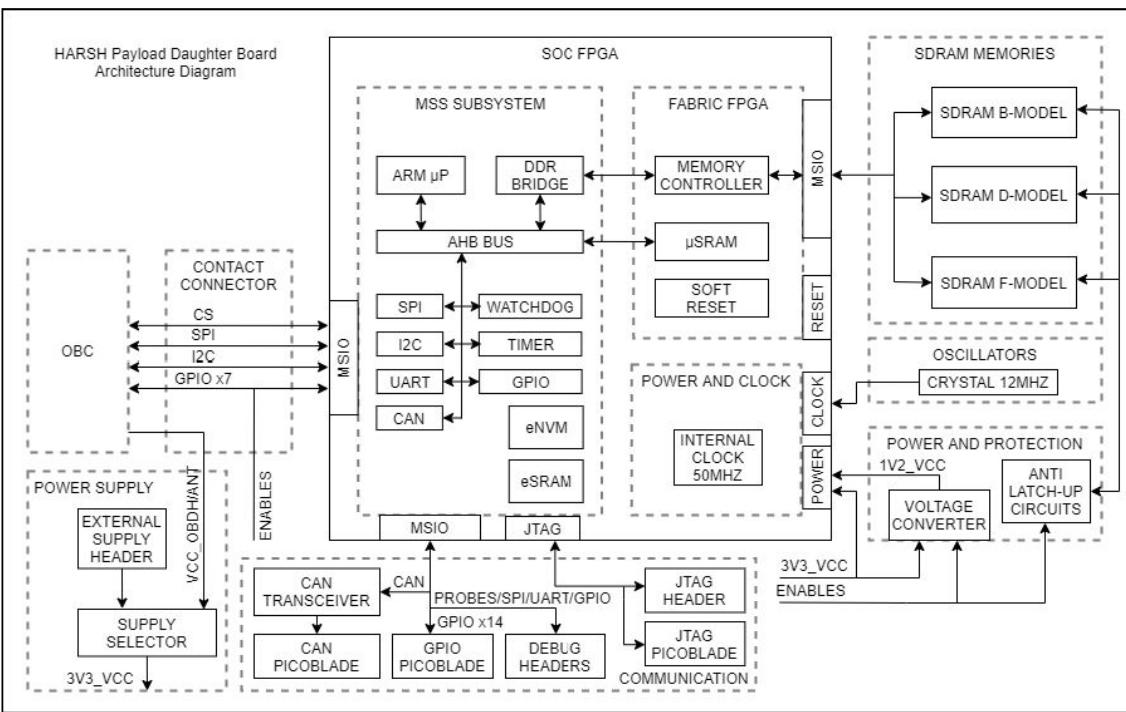
Copyright © 2020
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- Drawn by: André Martins Pio de Mattos.
- Based on OBDH 2.0 designed by: André Martins Pio de Mattos.
- Based on DB_Memory designed by: Yan Castro de Azeredo.
- Support: Kleber Reis Gouveia Júnior.

Project Information



Power Diagram



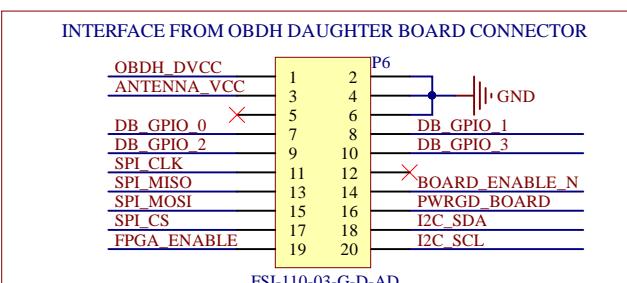
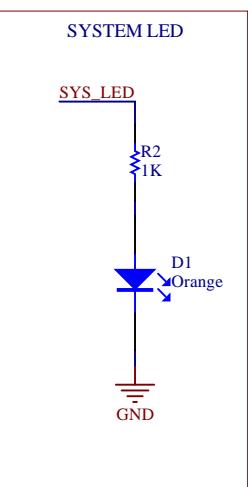
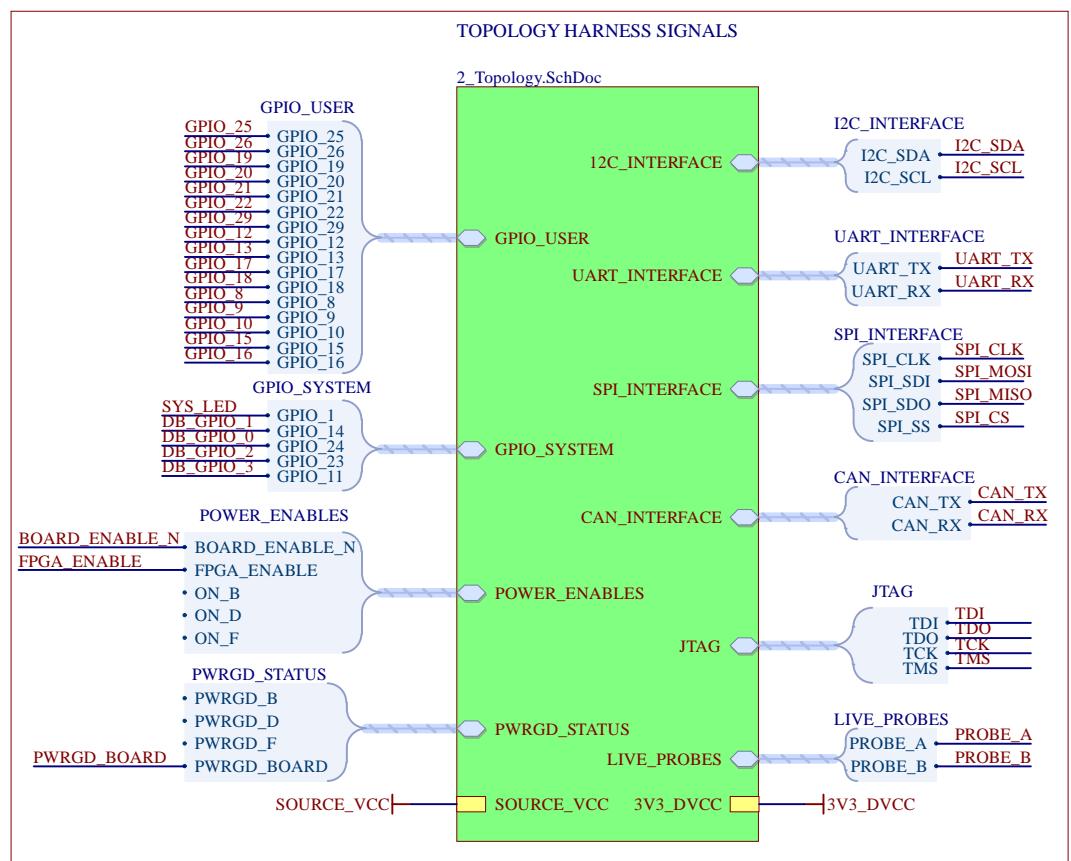
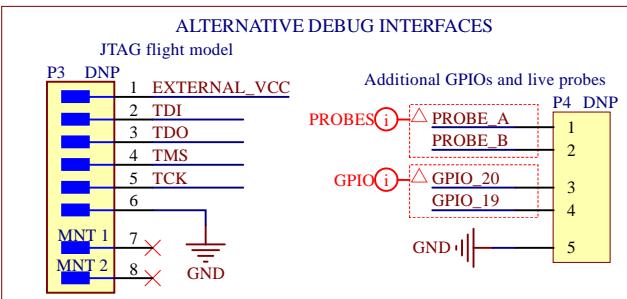
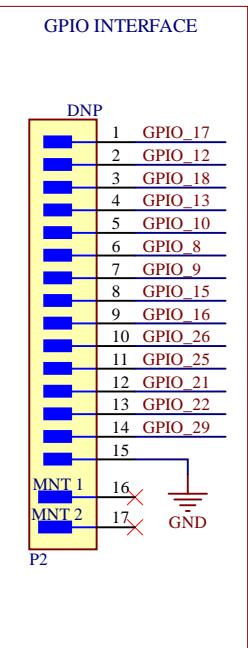
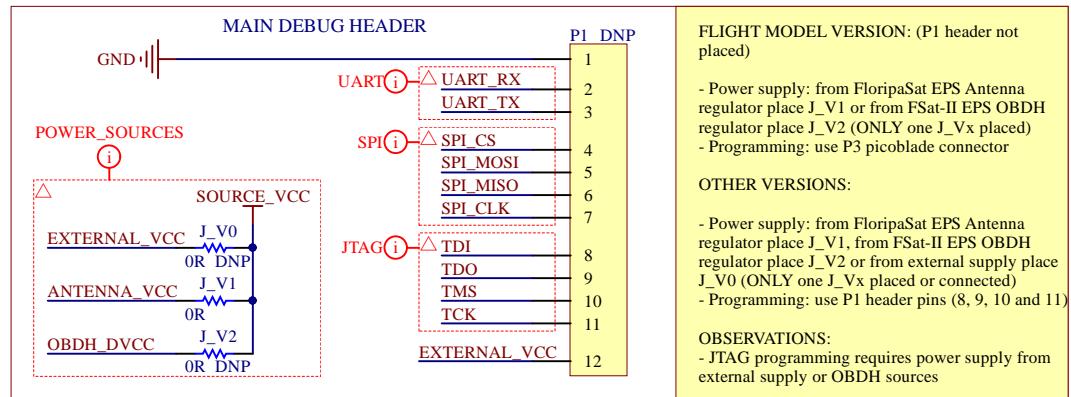
Block Diagram

Title: HARSH Payload Architecture		
Size: A4	Project: HARSH_Payload.PjPCB	Revision: 1.1
Date: 5/28/2020	Time: 2:10:38 PM	Sheet 1 of 8
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB

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Features not used from the generic daughter board interface connector:
- BATTERY VCC
Features used differently, but compatible, in the generic daughter board interface connector:
- DB_CS2 as GPIO for FPGA enable (Active High)
- DB_ADC0 as GPIO for board "power good" status (feedback of payload power status)
- DB_ADC1 as GPIO for board enable (Active Low)

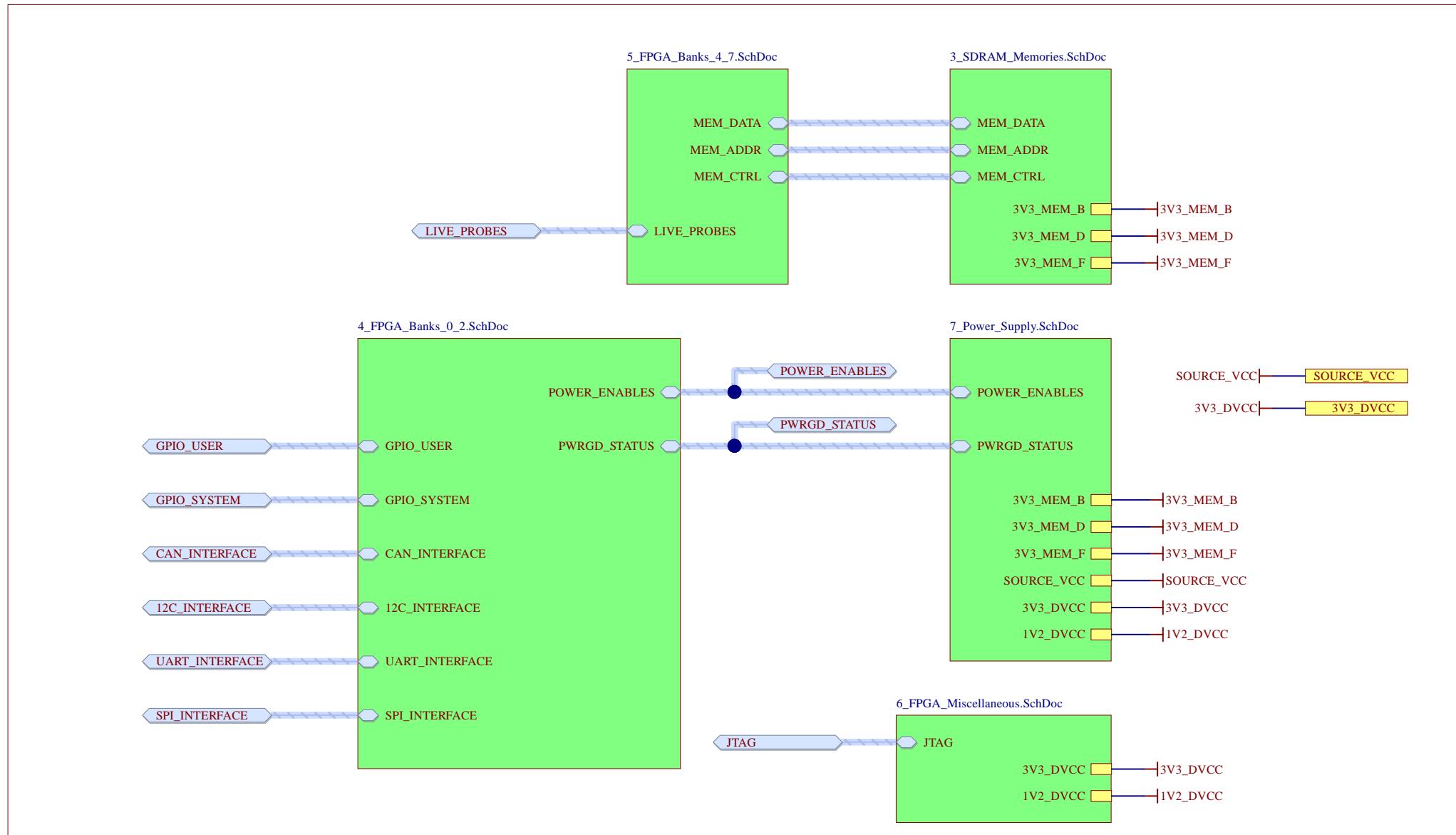
According to SAMTEC product specification, the maximum body height of the connector when pressed should be 3.28 mm.

Title: HARSH Payload Interface		
Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.1
Date: 5/28/2020	Time: 2:10:40 PM	Sheet 2 of 8
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB

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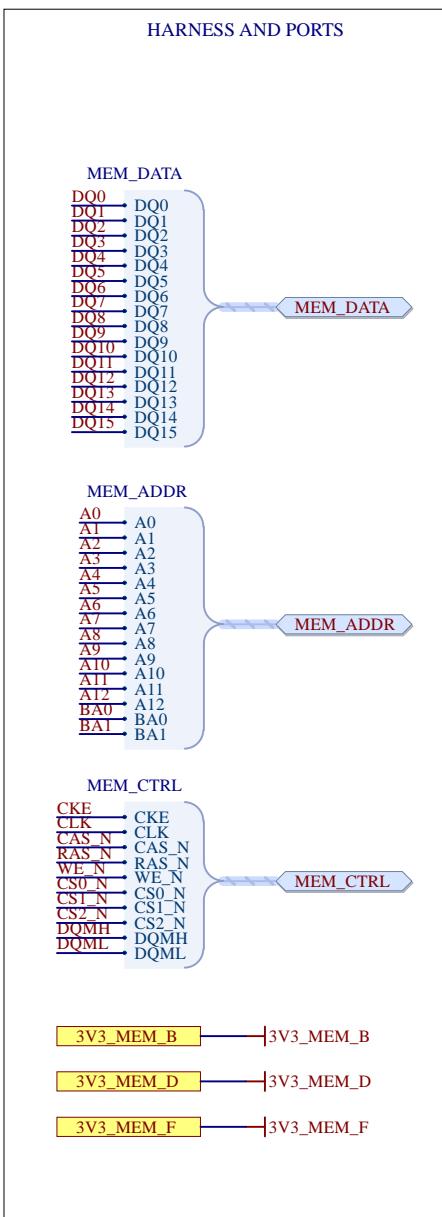
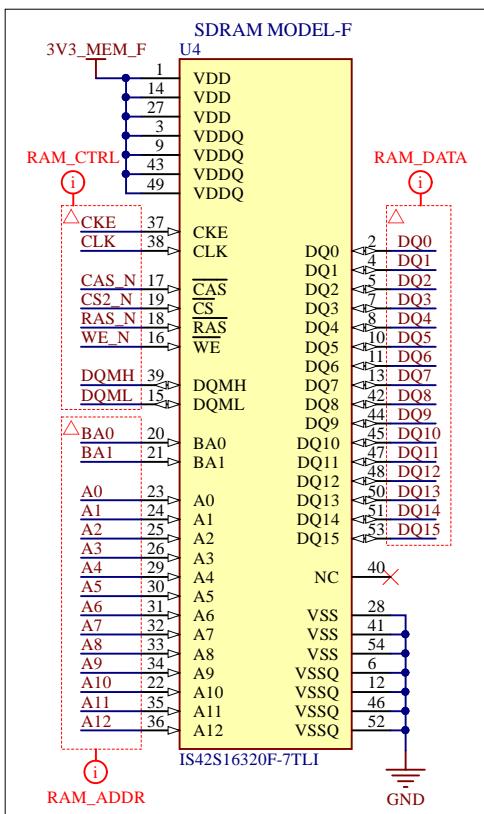
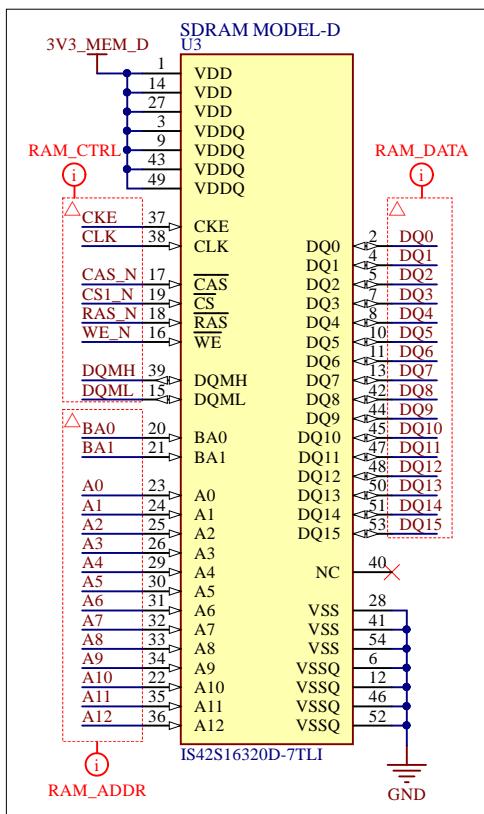
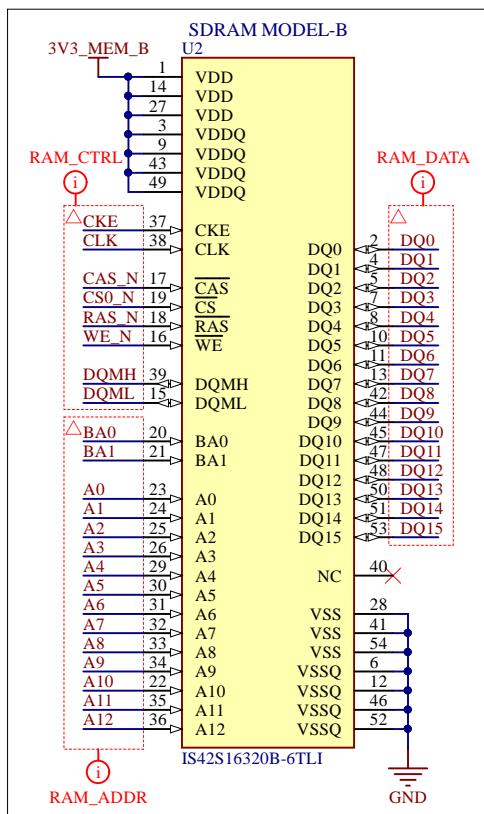


Title: HARSH Payload Topology		
Size: A4	Project: HARSH_Payload.PrjPCB	Revision: 1.1
Date: 5/28/2020	Time: 2:10:40 PM	Sheet 3 of 8
Drawn By: Andre Martins Pio de Mattos		Model: HARSH_DB

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Title: **HARSH Payload SDRAM memories**

Size: **A4** Project: HARSH_Payload.PrjPCB Revision: **1.1**

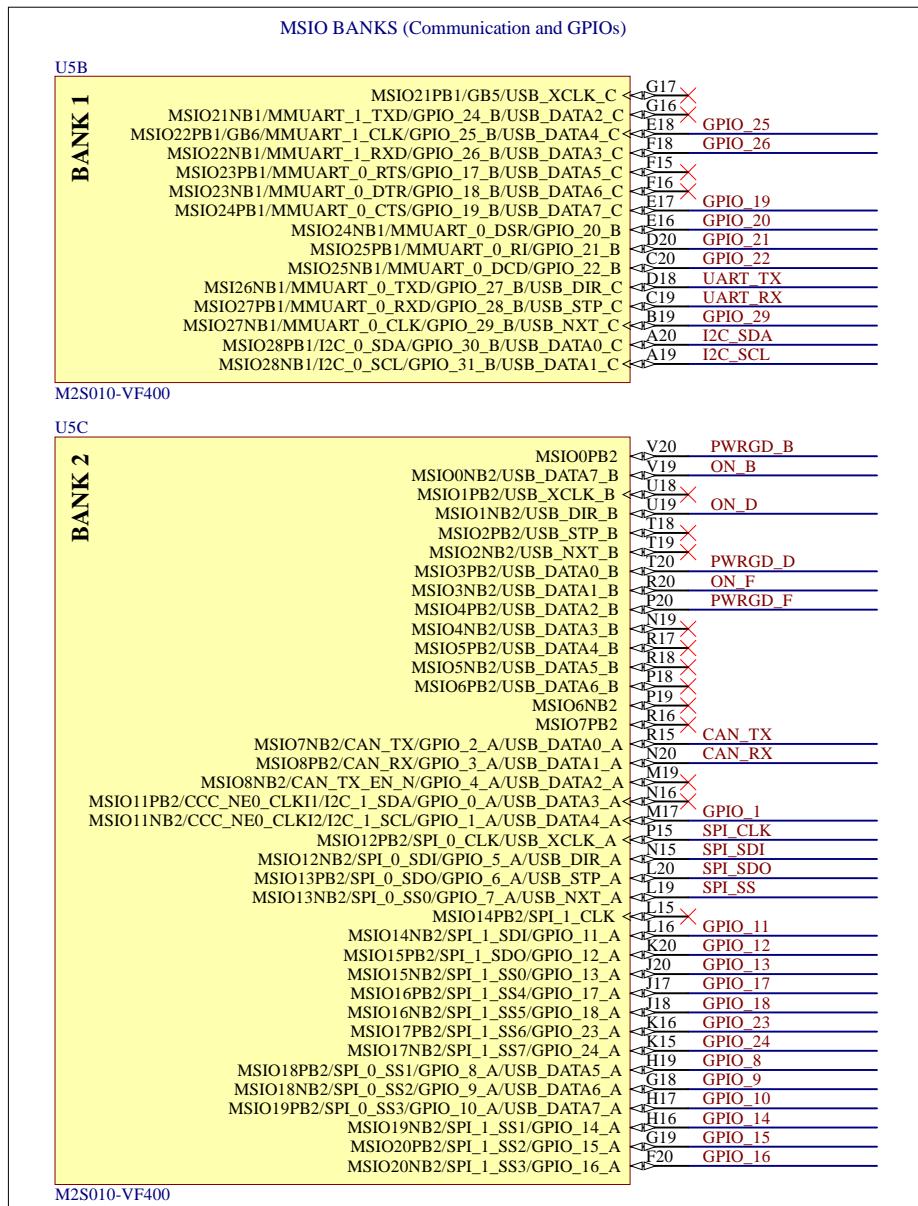
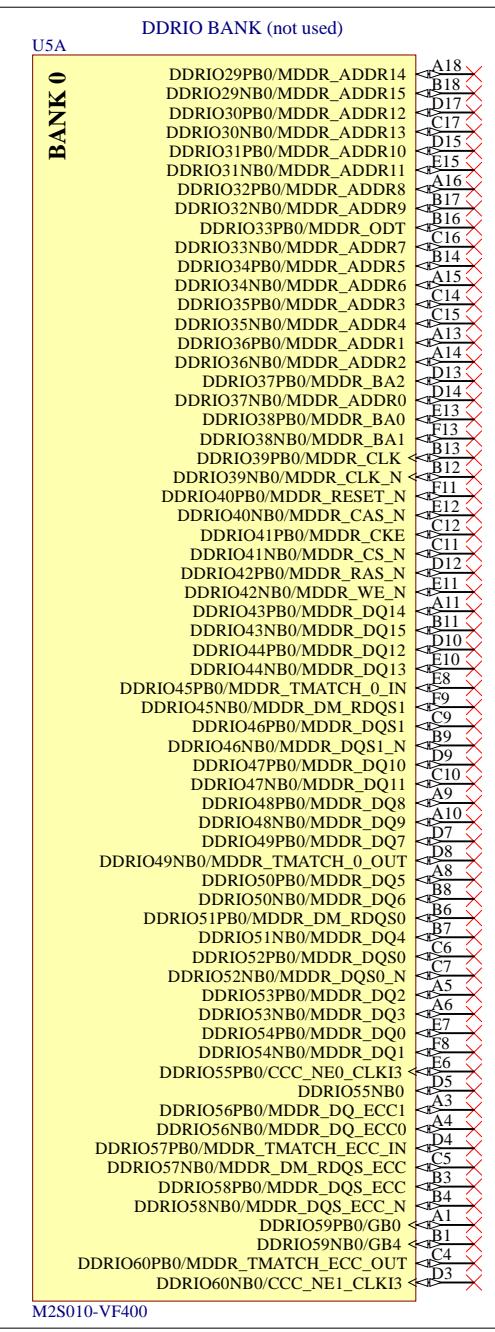
Date: **5/28/2020** Time: **2:10:40 PM** Sheet **4** of **8**

Drawn By: **Andre Martins Pio de Mattos** Model: **HARSH_DB**

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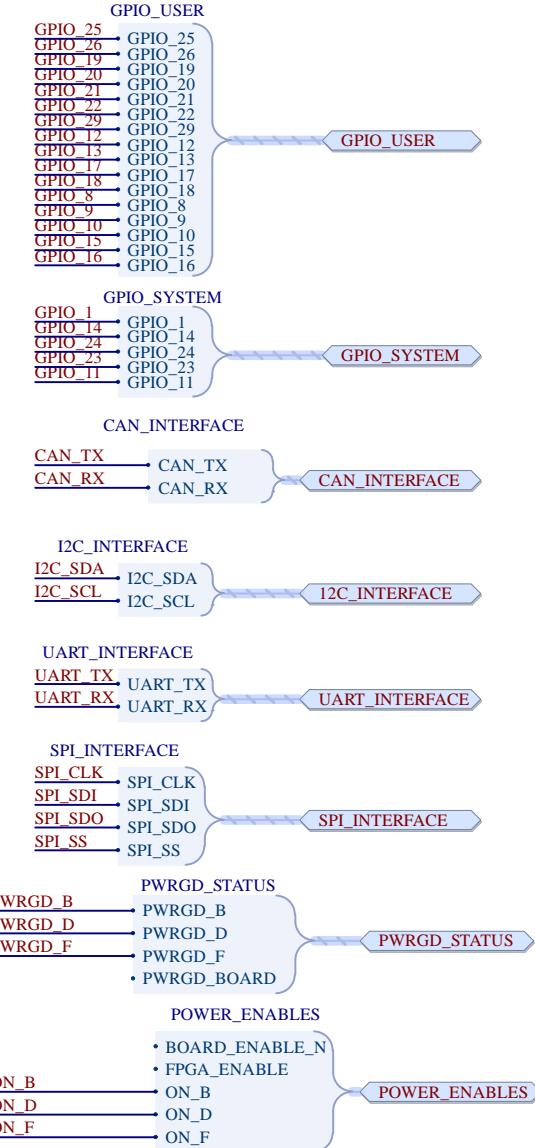
Title: HARSH Payload FPGA Banks 0_2

Size: A4 Project: HARSH_Payload.PrjPCB Revision: 1.1

Date: 5/28/2020 Time: 2:10:41 PM Sheet 5 of 8

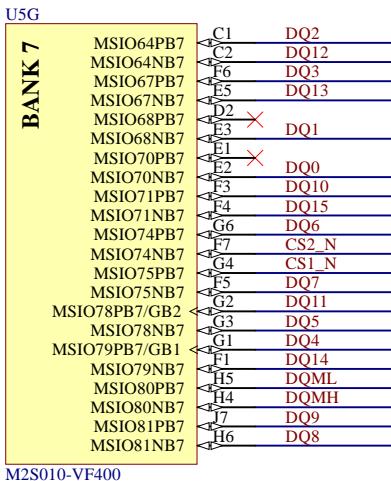
Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

HARNESS AND PORTS

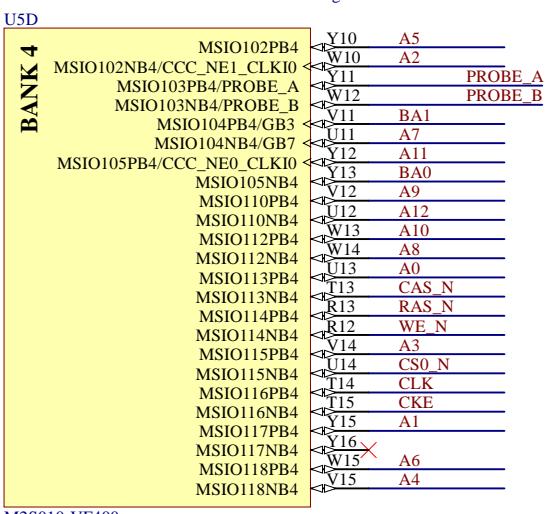
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MSIO BANKS (memories)

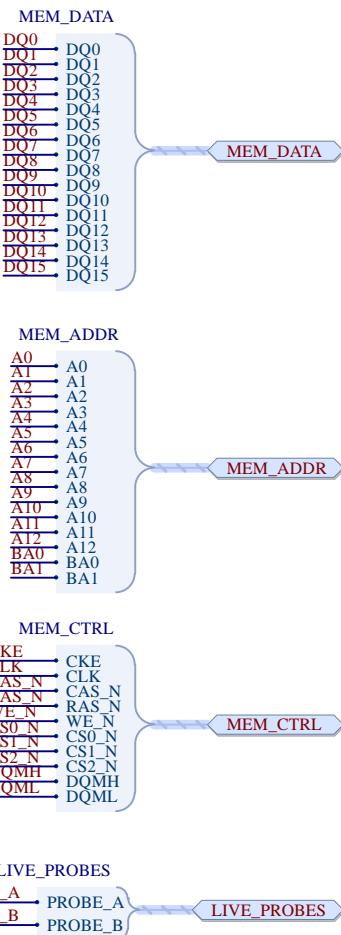
SDRAM data and control signals



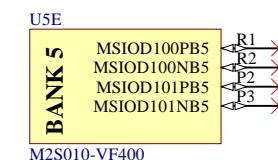
SDRAM address and control signals



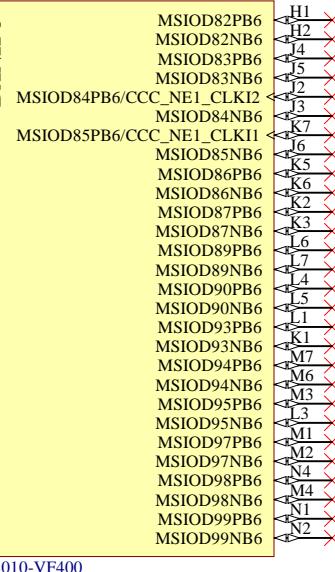
HARNESS AND PORTS

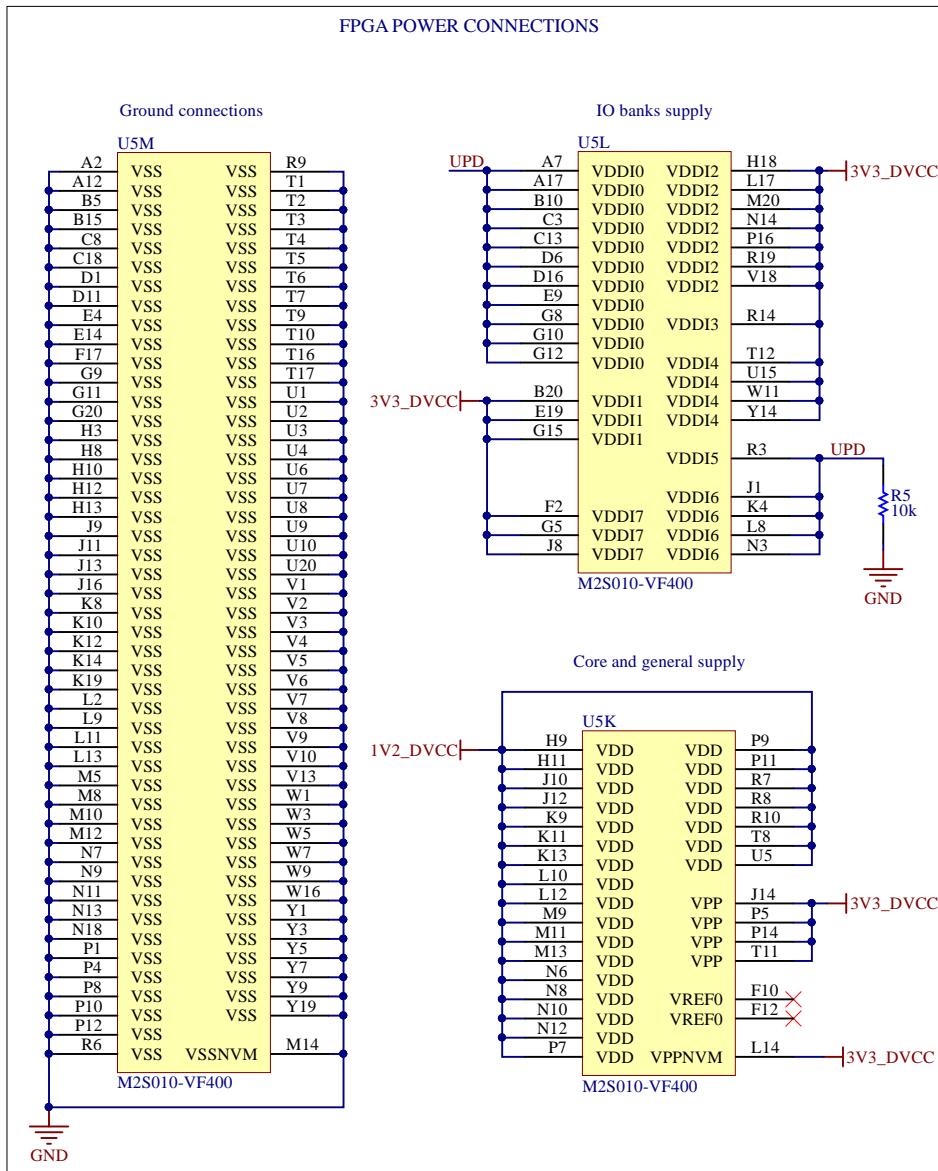
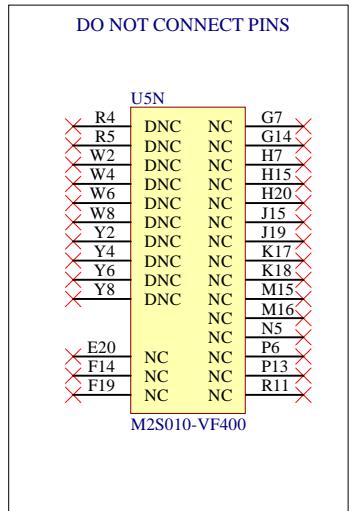
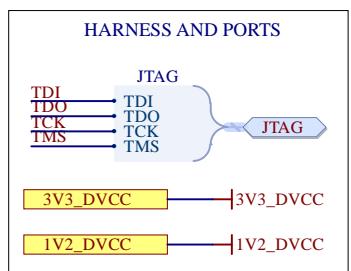
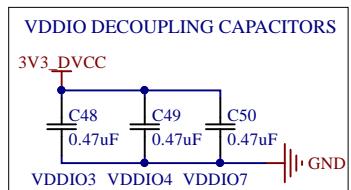
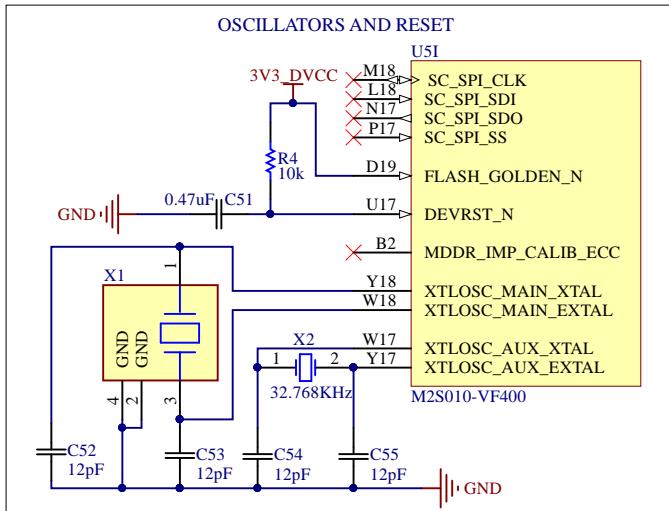
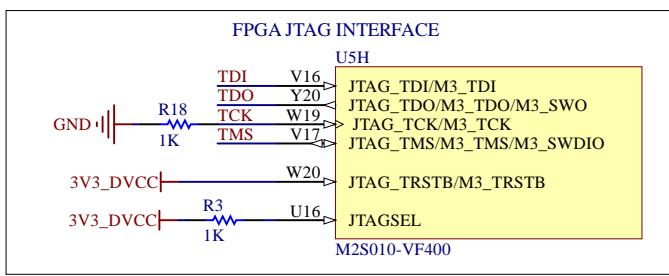
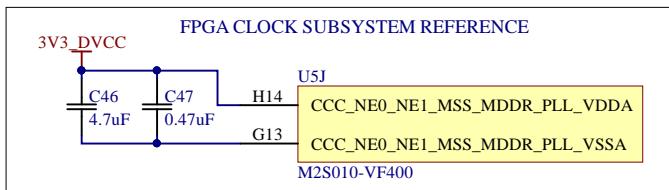
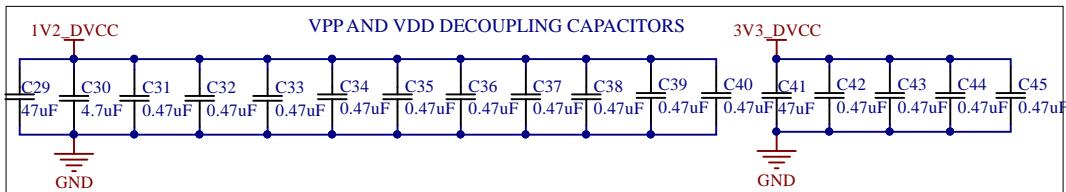


MSIOD BANKS (not used)



U5F

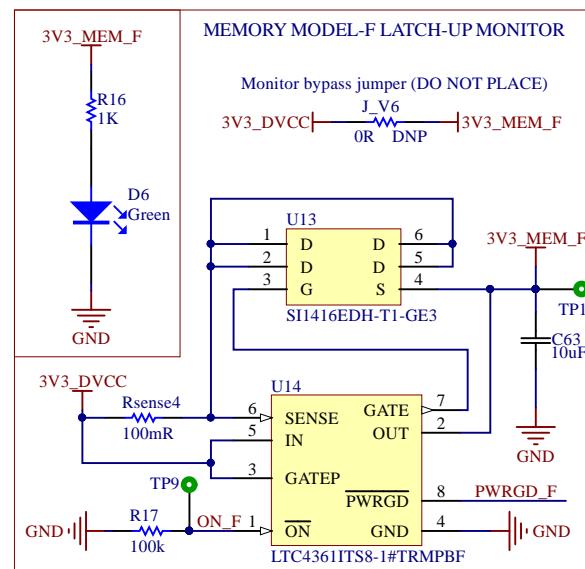
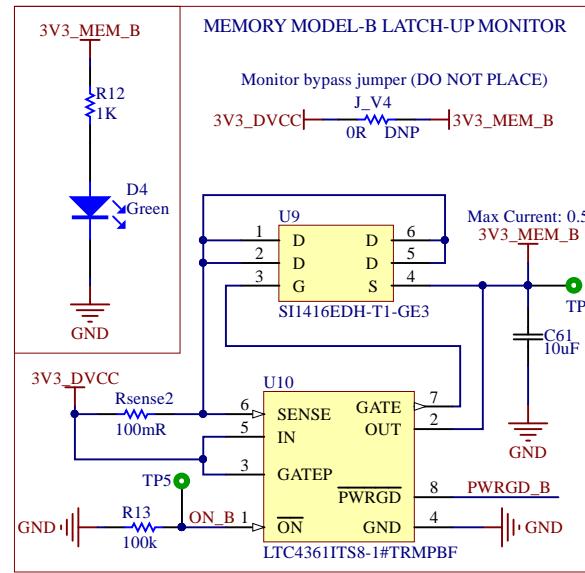
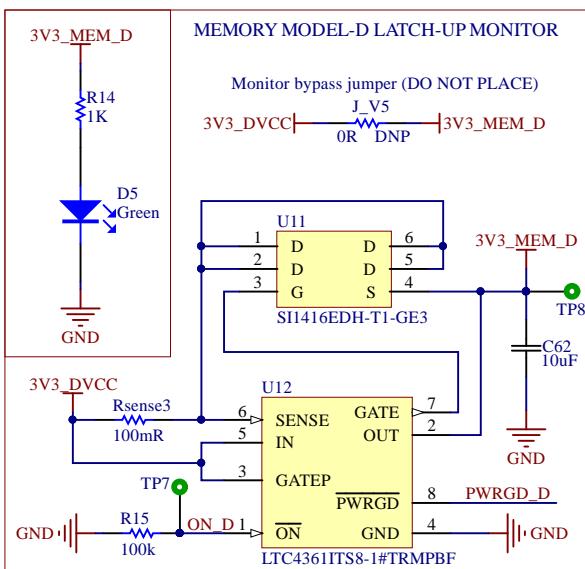
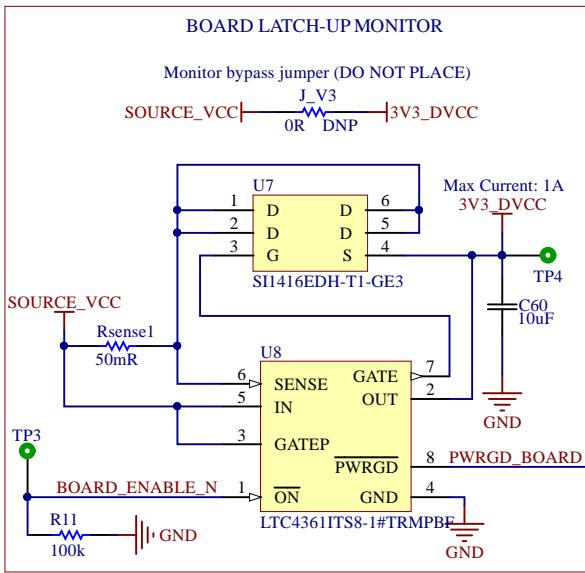
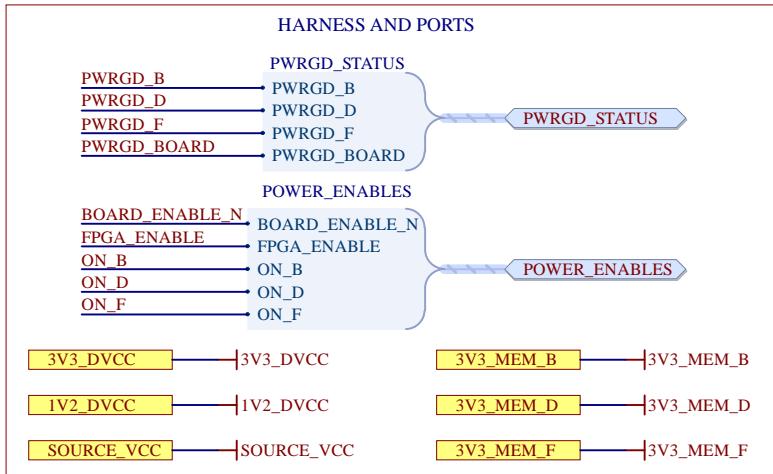
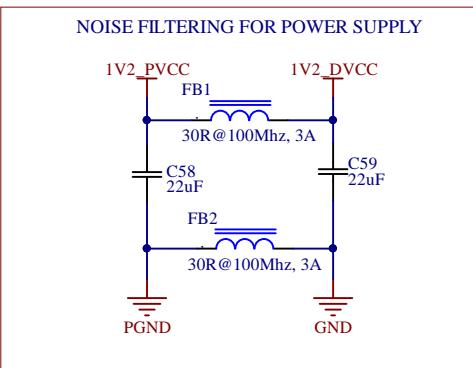
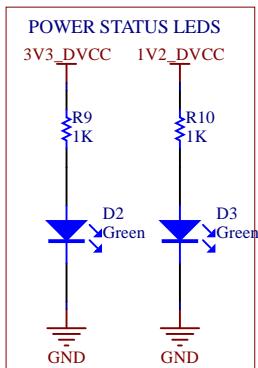
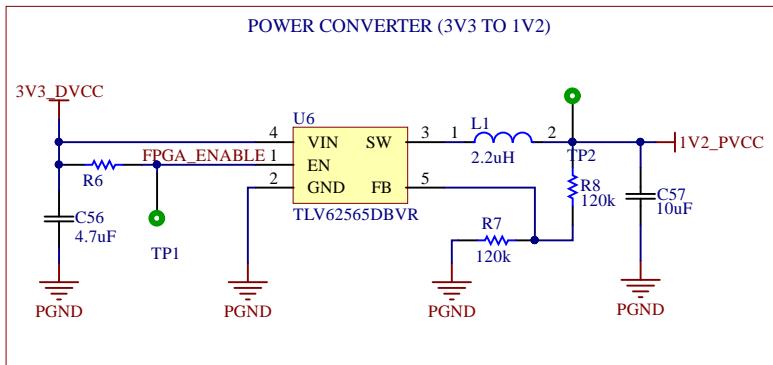


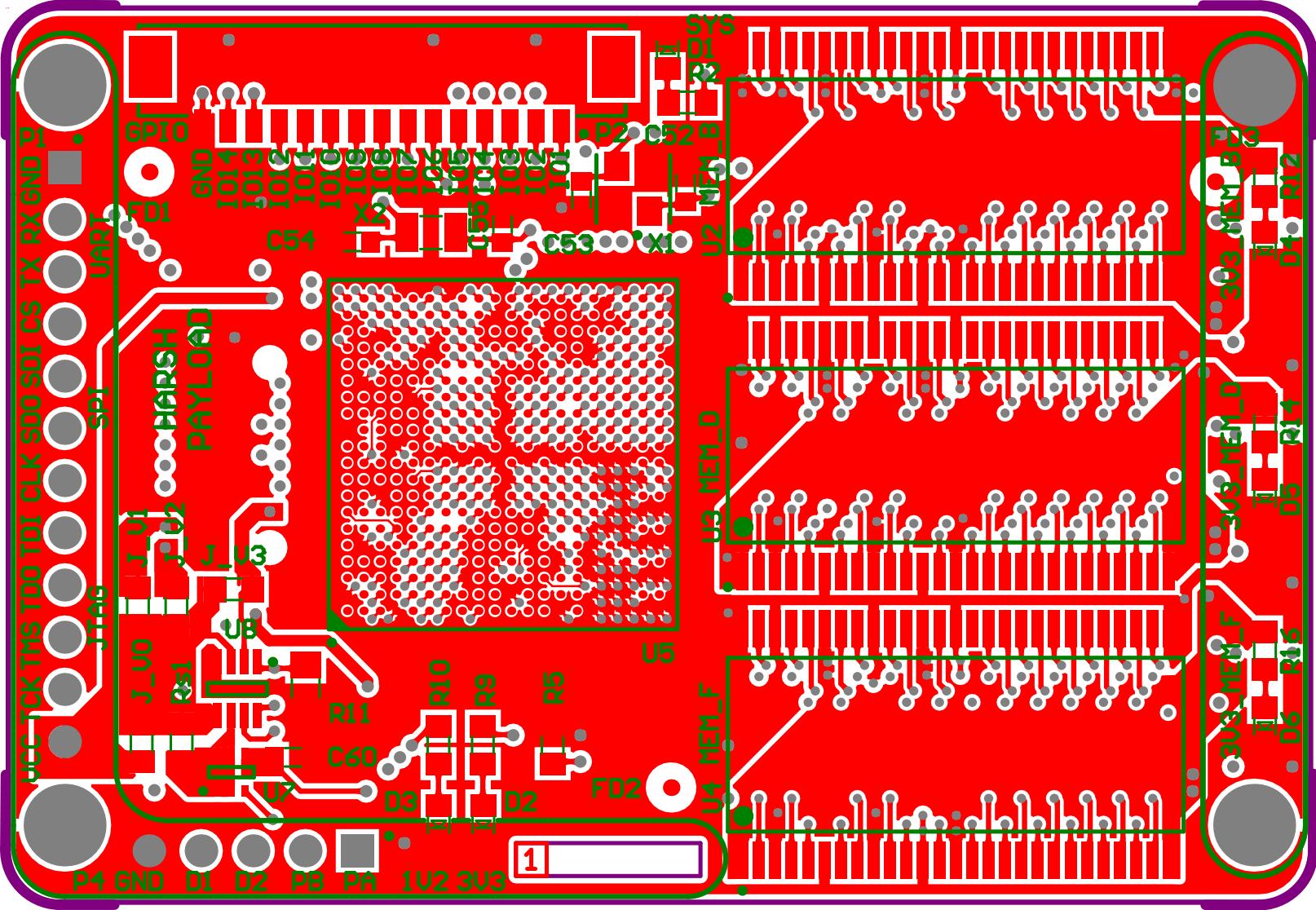


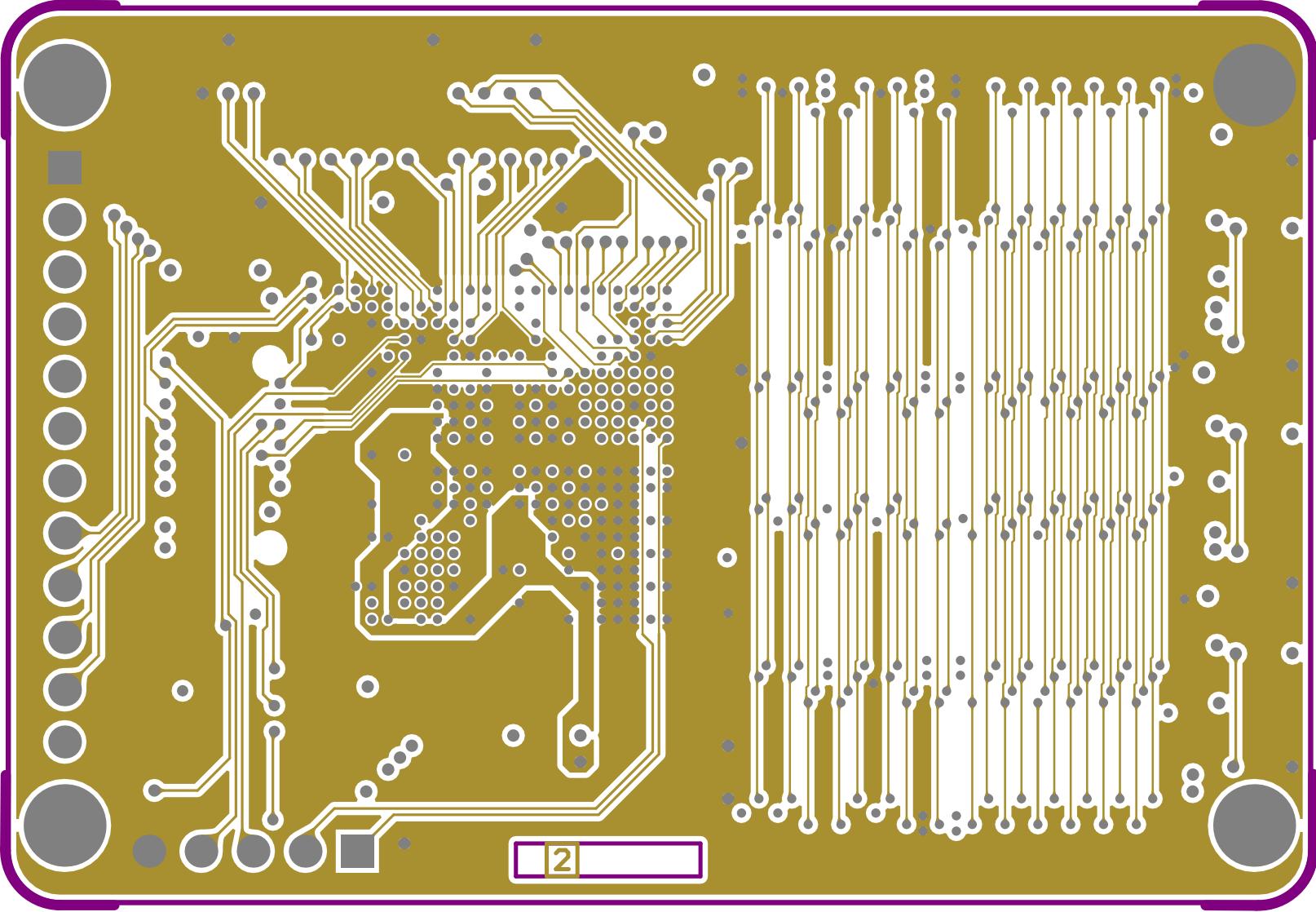
Title: HARSH Payload FPGA Miscellaneous
Size: A4 Project: HARSH_Payload.PrjPCB Revision: 1.1
Date: 5/28/2020 Time: 2:10:41 PM Sheet 7 of 8
Drawn By: Andre Martins Pio de Mattos Model: HARSH_DB

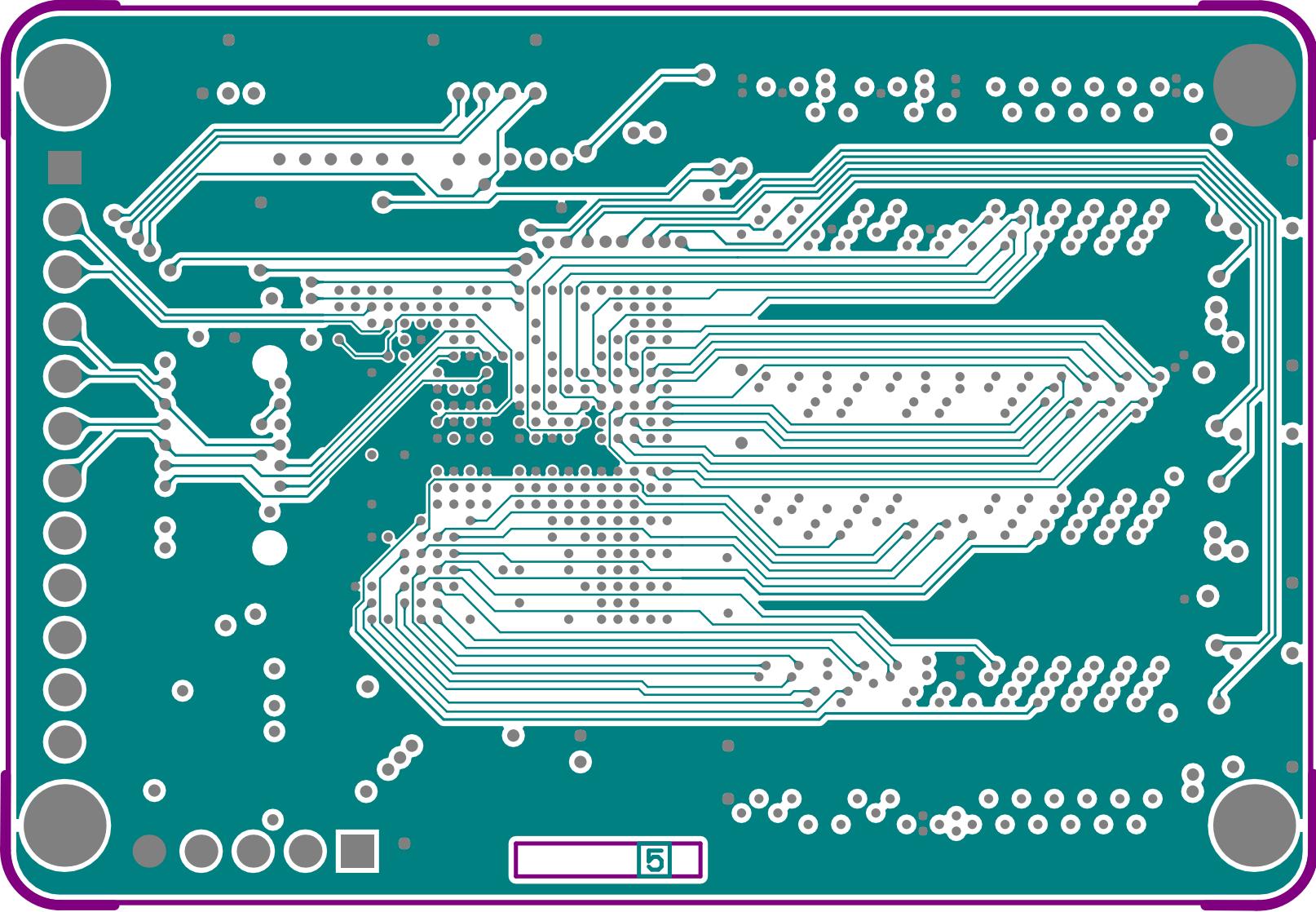
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DUAUHTEBOARD
REVISION V1.0

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