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High Frequency Technology

Design of a two-stage, balanced amplifier

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Contents

Chapter 1

Introduction

In this laboratory exercise, we focus on designing and understanding a two-stage microwave amplifier. Our goal is to create a device that can increase the power of microwave signals efficiently for a specific frequency range. We will be using a commercial integrated amplifier called GVA-83+ for the main part of our design. We will be using microstrip technology, which is common in microwave circuits, to build our amplifier.

Amplifiers have limits, like how much power they can give out and how much they can boost the signal. To overcome these limits, we're using a two-stage design. This means we connect two amplifiers together to get more power. We're also using special techniques like splitting the signal into two parts and amplifying each part separately. Then, we combine them again to get even more power and reduce the noise induced by the amplification. This is called a balanced amplifier. Our design also includes a band pass filter to make sure we only amplify the frequency range we want.

1.1 Initial parameters

For our case the initial parameters that we will be using will be the ones given in the Figure 1.1.

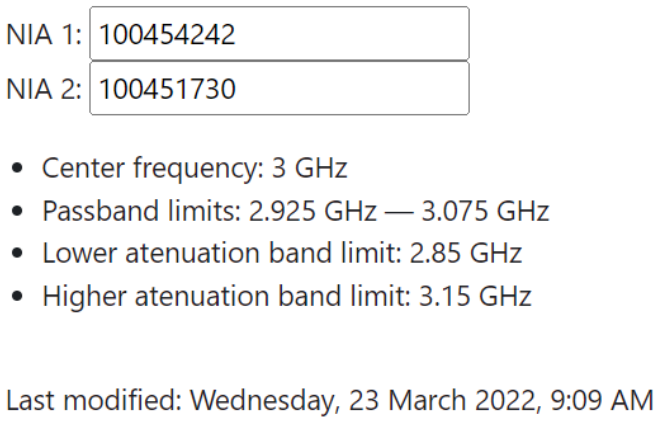


Figure 1.1: Initial parameters for our case study.

Chapter 2

Previous Work

2.1 Substrate Selection

For the circuit design we will be using a substrate with a microstrip structure with two possible dielectric thickness of $h = 0.508mm$ or $h = 1.27mm$ and a thick copper metallization of $t = 17\mu m$. For the substrate type the different configuration are seen in the Table 2.1.

Material	Relative permittivity (ε_r)	Loss tangent ($\tan\delta$)	Cost per area
Fiberglass (FR4)	4.7	0.01	$\times 1$
RT/Duroid 5880	2.2	0.009	$\times 10$
RT/Duroid 6006	6.15	0.0027	$\times 10$
RT/Duroid 6010.2LM	10.2	0.0023	$\times 10$

Table 2.1: Substrate types

2.1.1. Substrate type

As we can see in table 2.1, the *Fiberglass (FR4)* has a really high loss tangent $\tan\delta$. Even though it is the cheapest, we have decided to use another substrate that has a better $\tan\delta$ in order to improve our amplifier. For the choices, we can only choose the *RT/Duroid 6006* or the *RT/Duroid 6010.2LM* as the *RT/Duroid 5880* as almost the same $\tan\delta$ as *Fiberglass (FR4)*.

Comparing the *RT/Duroid 6006* and the *RT/Duroid 6010.2LM*, we can observe that they have the same price so we will go with the one with the lowest $\tan\delta$. That is as we want to reduce the losses at maximum. So let's study the *RT/Duroid 6010.2LM*.

If we use the values given the in the Table 2.1 for the *RT/Duroid 6010.2LM* and the AWR TXLine tool, we get a microstrip width of $w = 0.458$ when the dielectric thickness of $h = 0.508mm$ for a $Z = 50\Omega$ (See Figure 2.2). On the other hand, if we use a $h = 1.27mm$ for a $Z = 50\Omega$, we get a microstrip width of $w = 1.17mm$ which is larger (See Figure 2.2.

Considering that the width of each line must be no less than $200\mu m$, both lines would work perfectly fine at $Z = 50\Omega$. However, as we are designing a circuit where we might need different values of Z, we will see if they still work for for example $Z = 100\Omega$.

Using the *RT/Duroid 6010.2LM* with a dielectric thickness of $h = 1.27mm$ for $Z = 100\Omega$ we get a microstrip width of $w = 0.144mm$ (See Figure 2.3). As the width needed, is smaller than the one required, this substrate it is not the most recommended.

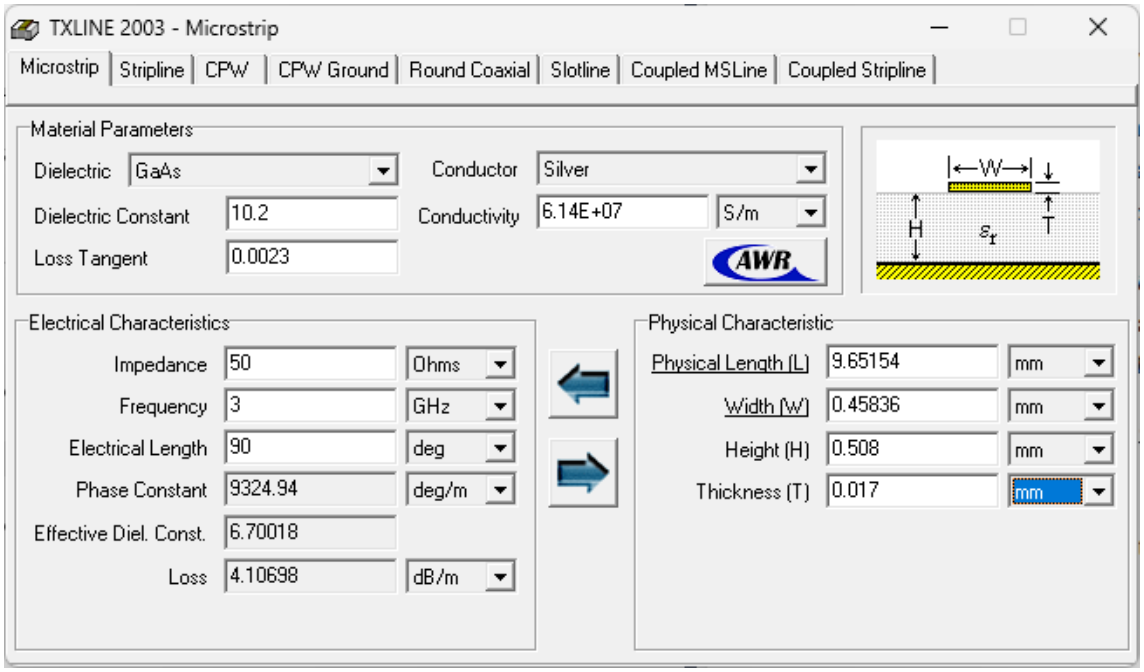


Figure 2.1: Width $w = 0.458mm$ for RT/Duroid 6010.2LM with $h = 0.508mm$ and a $Z = 50\Omega$

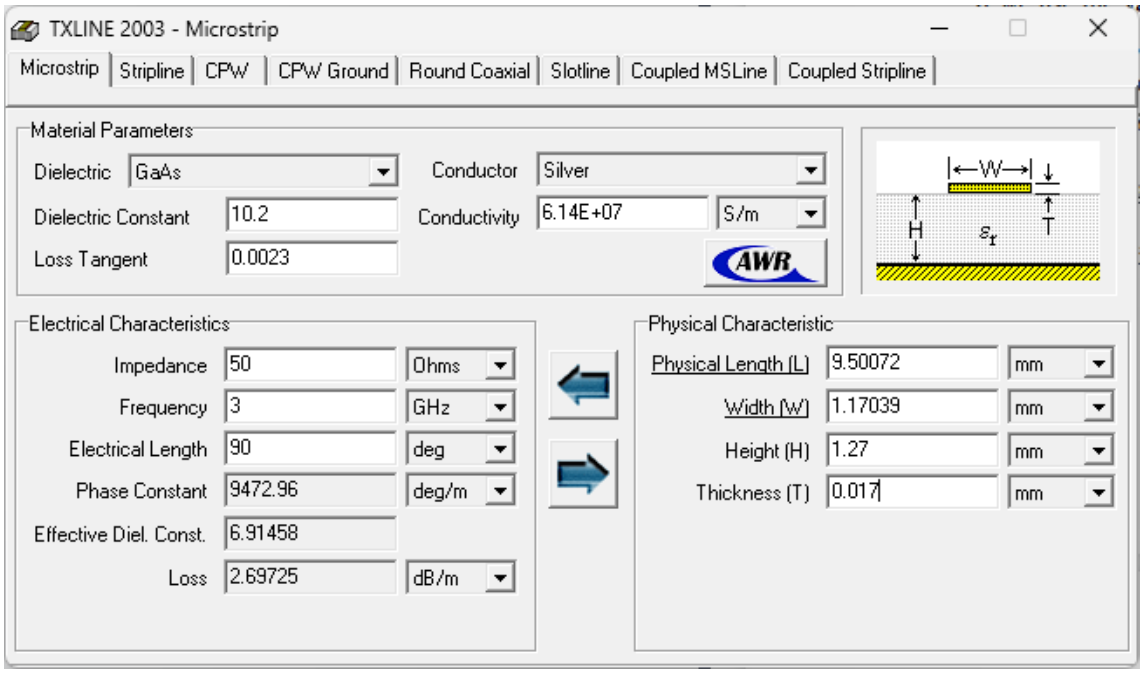


Figure 2.2: Width $w = 1.17mm$ for RT/Duroid 6010.2LM with $h = 1.27mm$ and a $Z = 50\Omega$

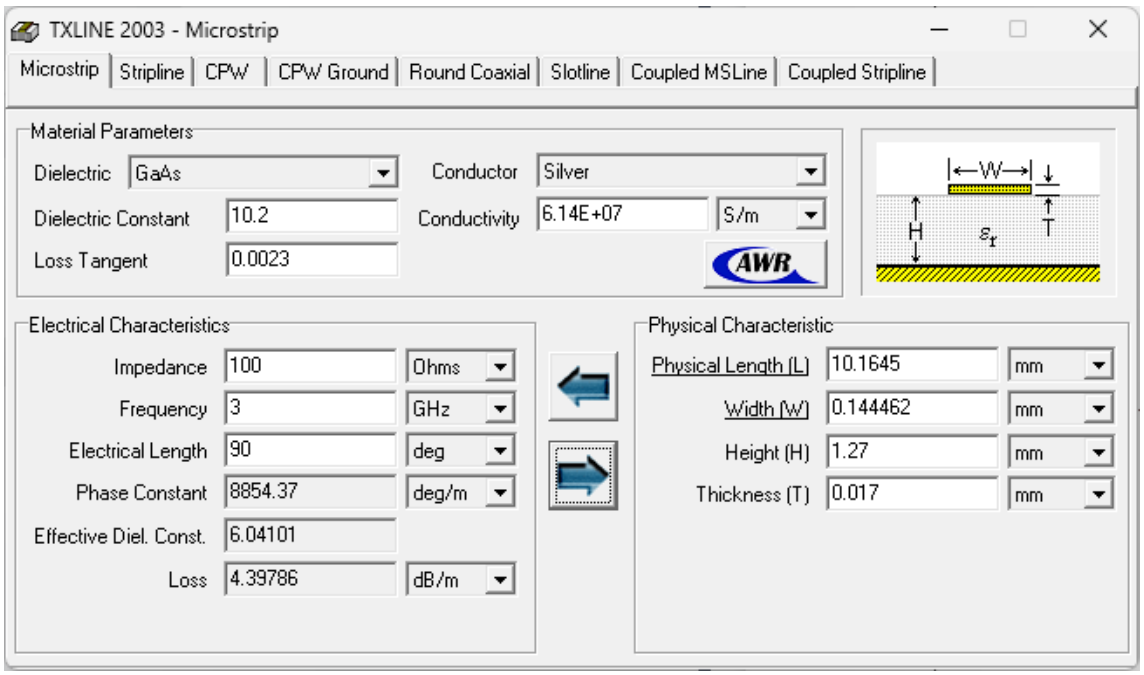


Figure 2.3: Width $w = 0.144mm$ for RT/Duroid 6010.2LM with $h = 1.27mm$ and a $Z = 100\Omega$

Due to that inconvenience, let's study the substrate *RT/Duroid 6006*. For this substrate with a $h = 1.27mm$ and a $Z = 100\Omega$, we get a width of $w = 0.343mm$ (See Figure 2.4). This width is much better than the *RT/Duroid 6010.2LM* with the $200\mu m$ minimum width constraint as we have more room to design our circuit. Therefore, we will be using the *RT/Duroid 6006*.

2.1.2. Substrate dielectric thickness

For the dielectric thickness, we can see in Figure 2.5 that for the *RT/Duroid 6006* with a $h = 0.508mm$ and a $Z = 100\Omega$, we get a width of $w = 0.128$. As stated before, that does not check the constraint of a minimum width of $w = 0.2mm$. Because of that we will select a dielectric thickness of $h = 1.27mm$.

2.1.3. Final substrate selection

For the substrate, we will select the *RT/Duroid 6006* as it is the best one for the same price that fits the constraints required. For the dielectric thickness, we will use a $h = 1.27mm$ for the very same reason. Choosing this dielectric will make our circuit as small as possible while keeping the losses at minimum. The price is not a concern as the *Fiberglass (FR4)*, even though it is the cheapest, we decided to discarded due to its really high $\tan\delta$. And among the rest of the substrates, the price is the same.

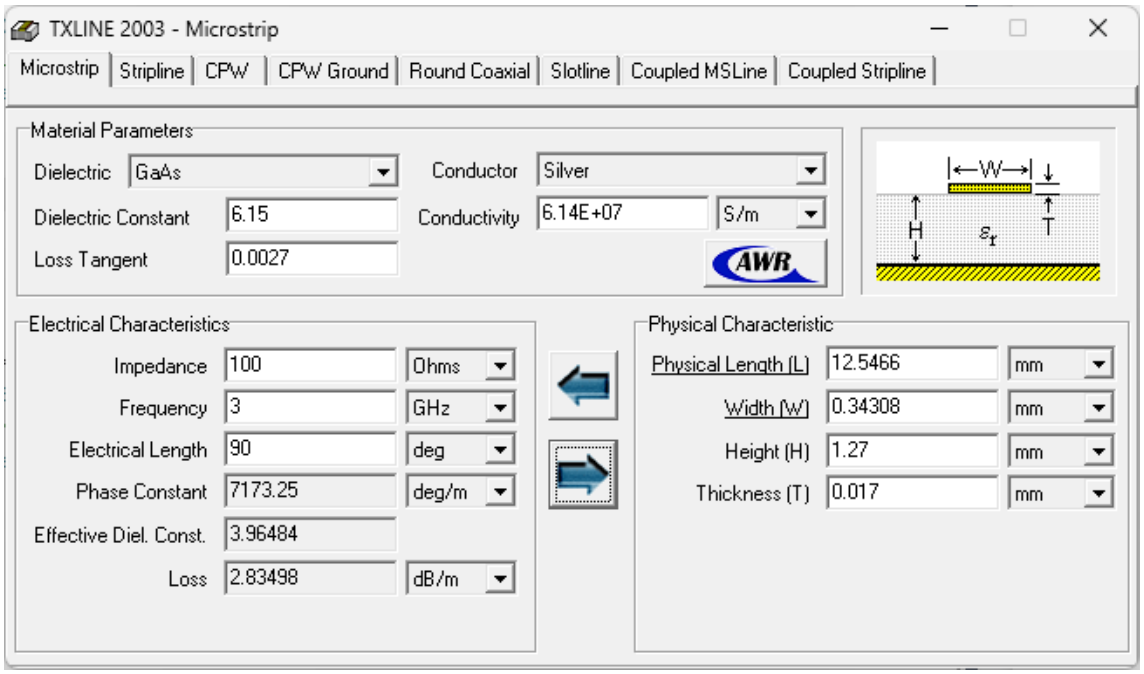


Figure 2.4: Width $w = 0.343mm$ for RT/Duroid 6006 with $h = 1.27mm$ and a $Z = 100\Omega$

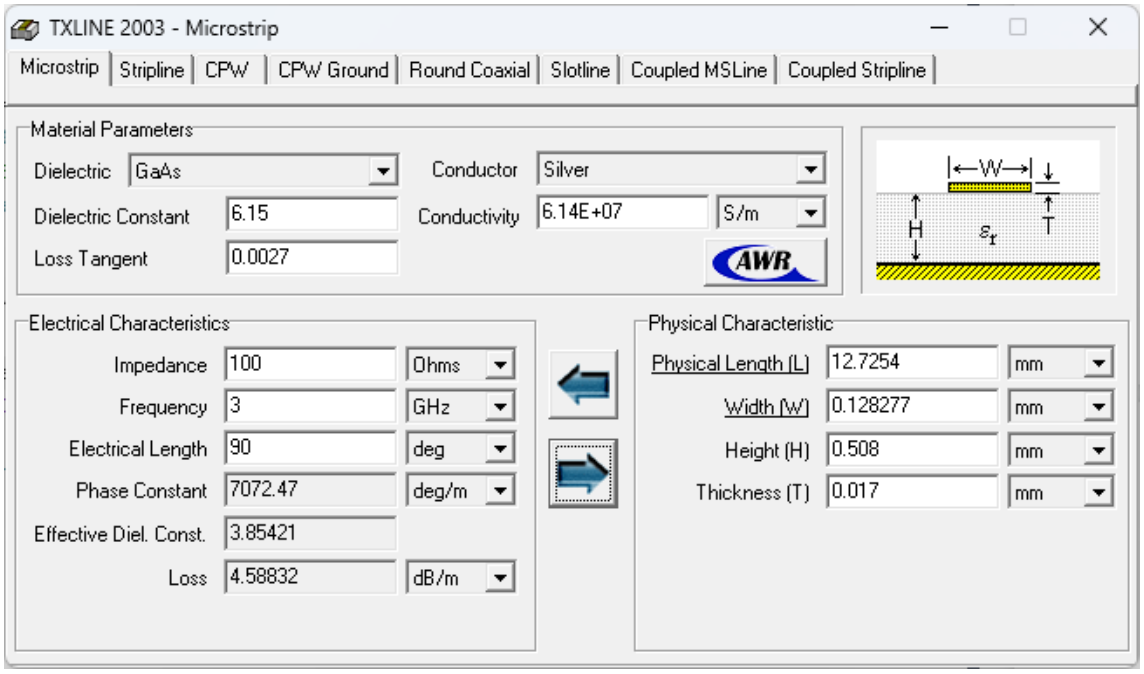


Figure 2.5: Width $w = 0.128mm$ for RT/Duroid 6006 with $h = 0.508mm$ and a $Z = 100\Omega$

Finally, in the Figure 2.7, we can see the calculations of the final width of $w = 1.85mm$ for a characteristic impedance of $Z_0 = 50\Omega$ and a dielectric thickness of $h = 1.27mm$. As we can see, the width is bigger than $w = 200\mu m$, therefore it checks the constraints and it will be the one we will be using further on.

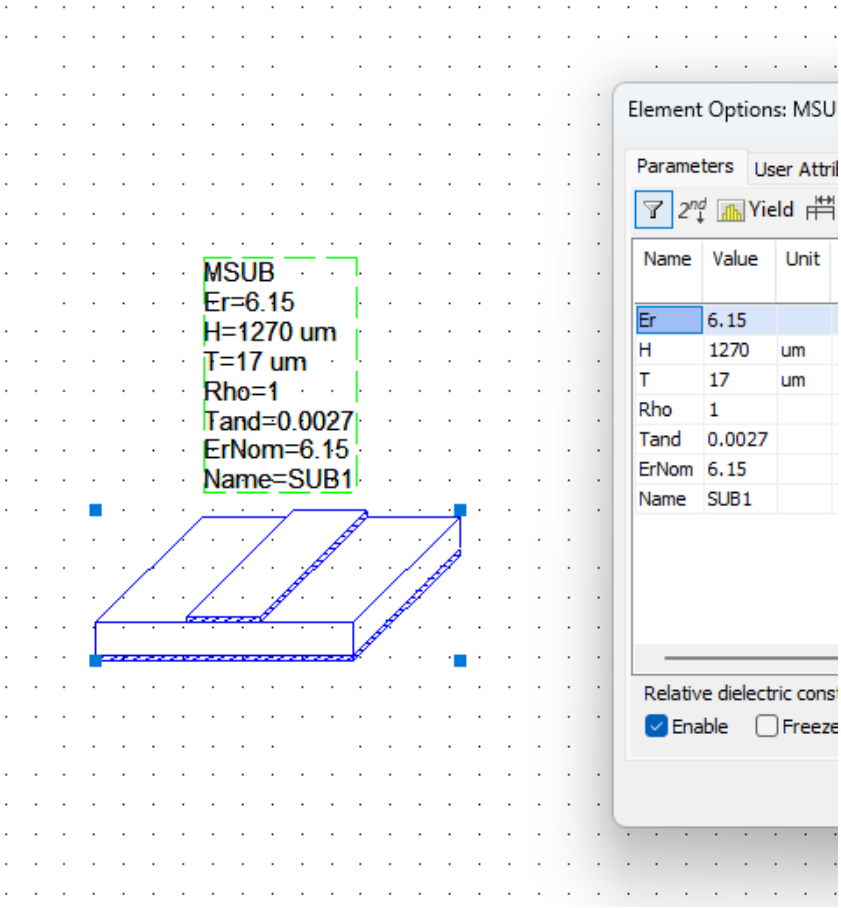


Figure 2.6: Final substrate selection

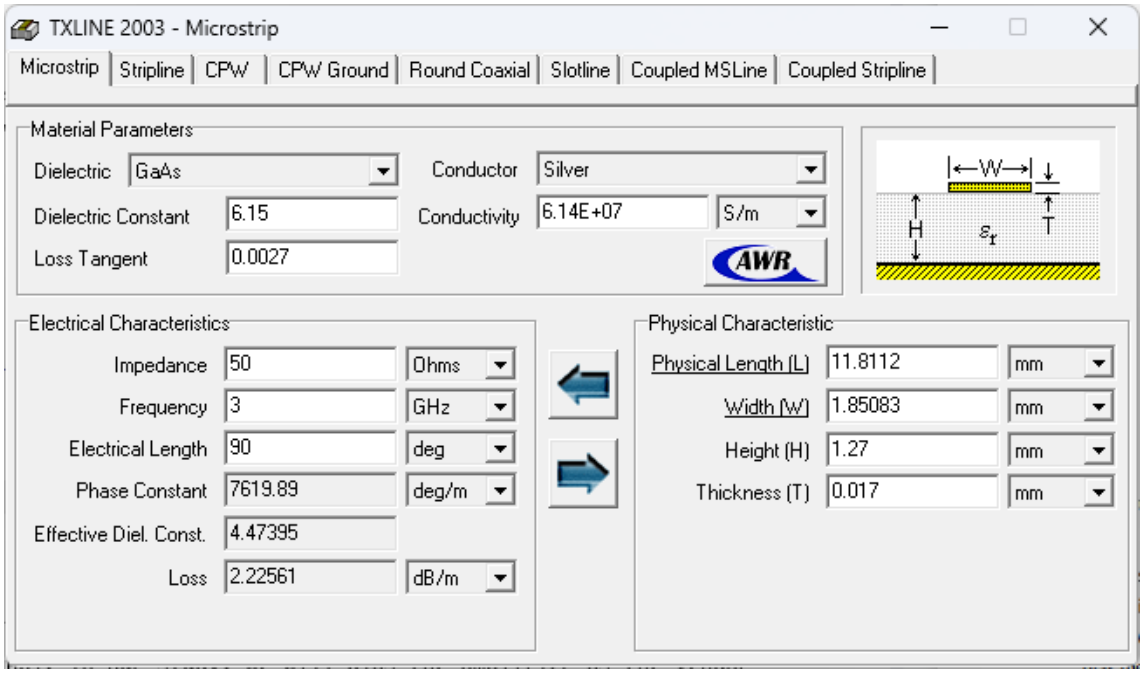


Figure 2.7: Width $w = 1.85mm$ for RT/Duroid 6006 with $h = 1.27mm$ and a $Z = 50\Omega$

Chapter 3

Design of the Circuit Elements

3.1 First Stage: Simple Amplifier

For the amplifier, we will be using the GVA83+, which is a wide band amplifier for a dynamic range of applications. In order for an amplifier to work, it needs to be supplied a DC power in order for it to perform the amplification of our signal. In our study, we will bias the amplifier as the vendor recommends, see Figure 3.1.

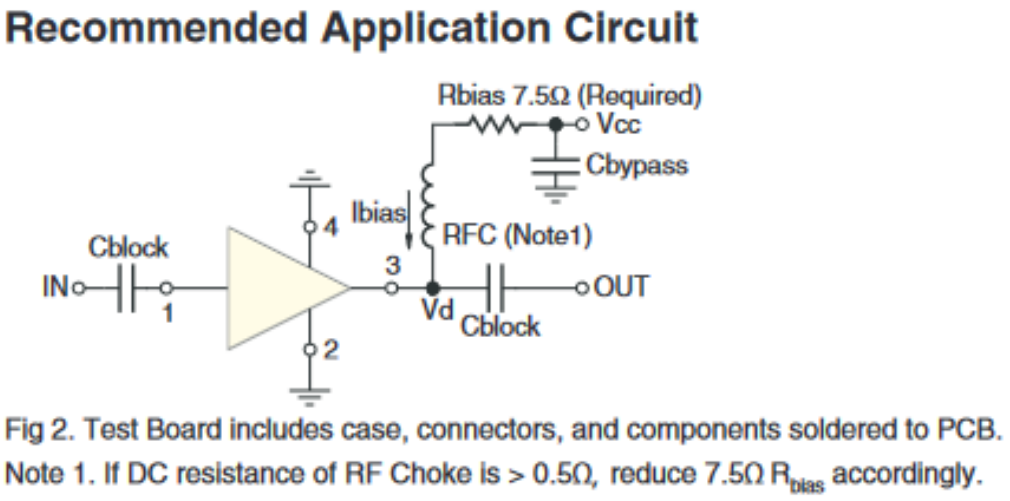


Figure 3.1: Bias network of the GVa83+ Amplifier recommended by the vendor

3.1.1. Analysis of the Bias Network (Figure 3.1) at f = 0 GHz and f = 3 GHz

When $f = 0GHz$, we can observe that the impedance of the capacitors $Z_C = \frac{1}{j \cdot 2 \cdot \pi \cdot f \cdot C} \rightarrow \infty$ when $f \rightarrow 0$ acting as an open circuit. On the other hand, the impedance of the inductor $Z_L = j \cdot 2 \cdot \pi \cdot f \cdot L \rightarrow 0$ when $f \rightarrow 0$ acting as a short circuit. Taking those points into account, we get that the circuit can be summarized as seen in Figure 3.2 when $f = 0GHz$. Since the output is not connected to the input, then the circuit will not work at very low frequencies. However, we can calculate the current flowing through the inductor as it is a short circuit now, and that current will be the one in charge of powering the amplifier. In this case $I_{bias} = \frac{V_{CC}}{R_{bias}}$.

On the other hand, if we study the circuit at the designed frequency $f = 3GHz$; the capacitors act as a short circuit and the inductor act as an open circuit. That way, the branch required to bias the amplifier is "disconnected" per say (See Figure 3.3) and the gain of the amplifier is $G = Av = s_{21}$.

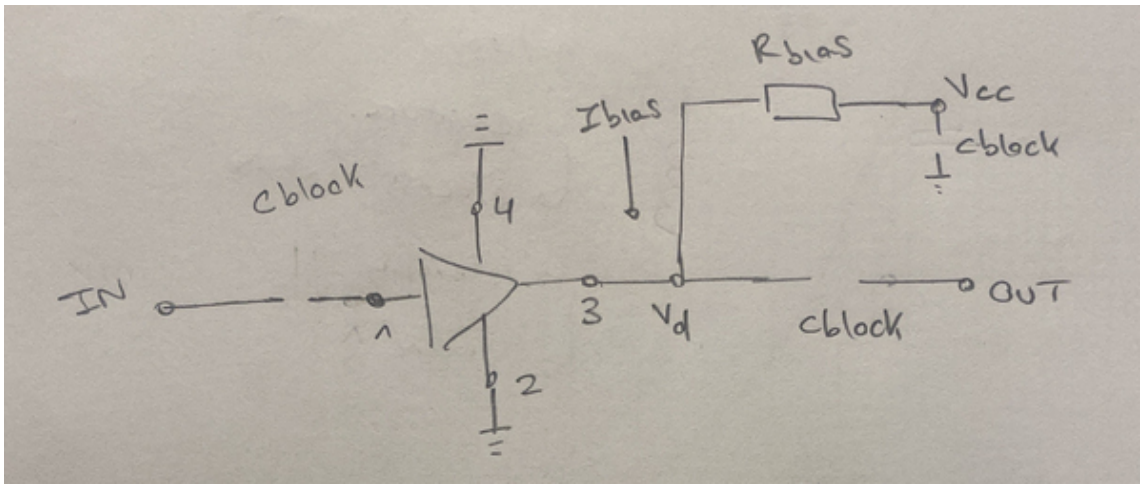


Figure 3.2: Bias network of the GVa83+ Amplifier at $f = 0GHz$

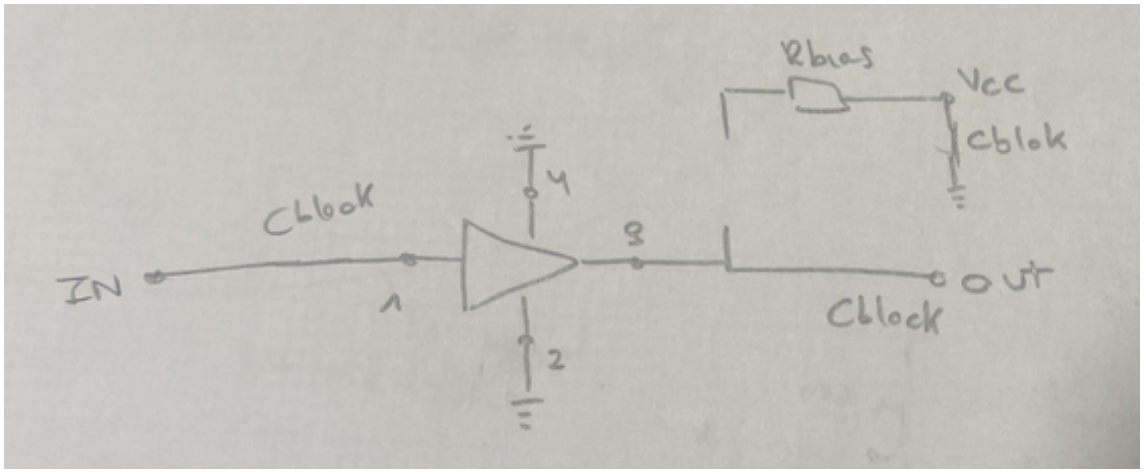


Figure 3.3: Bias network of the GVA83+ Amplifier at $f = 3GHz$

3.1.2. Analysis of the Bias Network (Figure 3.1) with the Transmission Line at f = 0 GHz and f = 3 GHz

The analysis of the proposed Bias Network with the Transmission Line (TL) (see Figure 3.4) is really similar to the one proposed by the vendor (see Figure 3.1). The only differences are that we are using a TL instead of an inductor and the bypass capacitor now it is in parallel with the TL.

At $f = 0GHz$, the capacitors act as open circuits and the TL acts as a short circuit. Again, since the output is not connected to the amplifier, the circuit does not work as previously stated. On the other hand, at $f = 3GHz$, the capacitors act as a short circuit and the TL acts as an open circuit as before. The gain of the circuit is still the same as before $G = Av = s21$.

Now if we study the inductor, we want that the inductor acts as a short circuit at $f = 0GHz$ and as an open circuit at $f = 3GHz$. For this, when $f = 0GHz$, the TL acts like a normal cable so it can be neglected. Thus, the amplifier is connected to V_{cc}, powering up the amplifier. On the other hand, we want that at $f = 3GHz$ the TL to act like a short circuit. We can see that as the capacitor acts like a short circuit in $f = 3GHz$, we will have an impedance of 0 at the end of the TL between the capacitor and the resistor. So if we make the length of the TL of $l = \frac{\lambda}{4}$, we will have at the output port an impedance of ∞.

In order to calculate the length of the TL in order to function as the inductor, we need to get the highest possible value of the characteristic impedance (Z_0). For this we have used the AWR TXLine tool and we got a length of $l = 12.692mm$ with a characteristic impedance of $Z_0 = 130.62\Omega$ (see Figure **??**). Keep in mind that we have used the minimum width available $w = 200\mu m$ in order to make it as small as possible. The reasoning for getting the maximum Z_0 is because that way, the TL will behave like an open circuit for high frequencies and like a short circuit for low frequencies.

3.1.3. Wide band Simulation of the Vendor's Bias Network

For the Vendor's Bias Network, we will be using the circuit pictured in Figure 3.5. As we can see in Figure 3.6, the amplifier works as expected. It is powered by the bias network as stated before, and works correctly at our desired frequency of $f = 3GHz$.

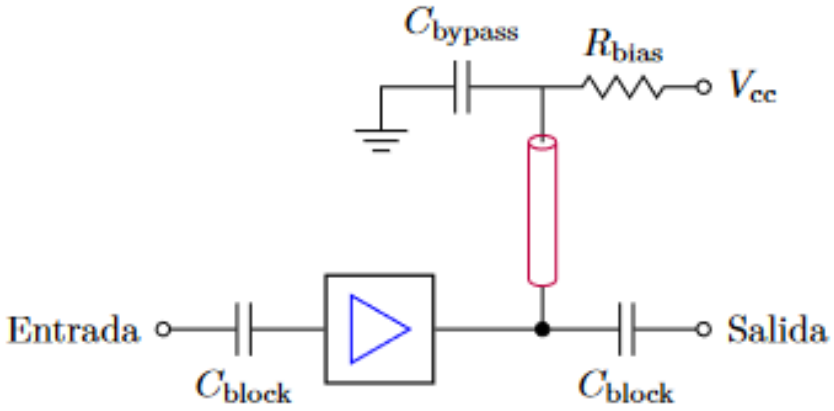


Figure 3.4: Proposed Bias Network of the GVA83+ Amplifier with a TL

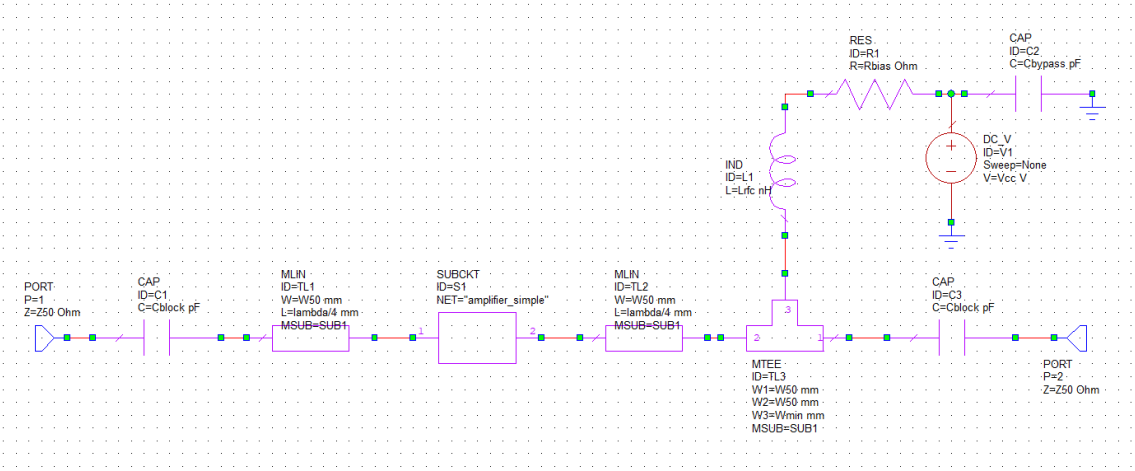


Figure 3.5: Circuit of the vendor's bias network

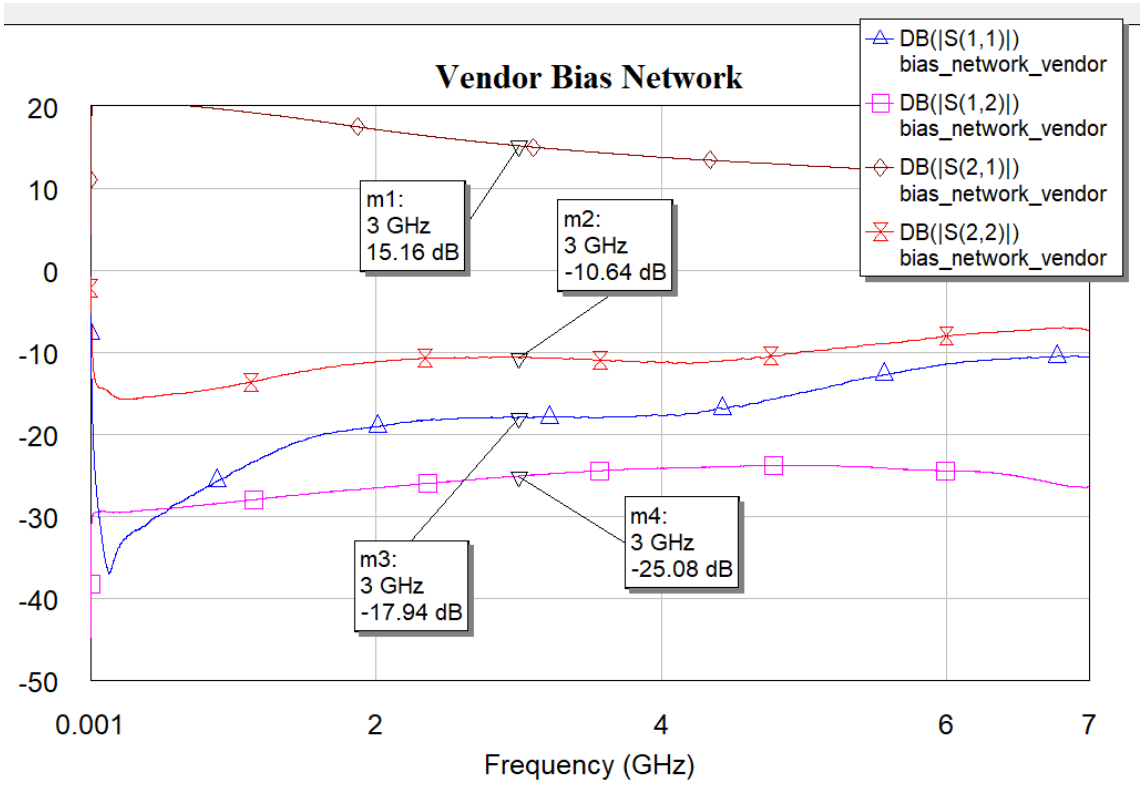


Figure 3.6: Simulation of the vendor's bias network of Figure 3.5

3.1.4. Wide band Simulation of the Proposed Bias Network

For the proposed bias network, we will be using the circuit shown in Figure 3.7. And for this circuit, we get the following simulation (see Figure 3.8). If we compare it to the bias network that the vendor recommended (see Figure 3.6), we can see that the values for the S-parameters are almost the same. However, that is only for our working frequency of $f_0 = 3GHz$. If we look at the s_{21} parameter, we can see that it is smoother in the proposed network. That is because as we have the capacitor in parallel with the resistor, then the node between them will have a stable ground when working at high frequencies.

If we modify the characteristic impedance of the transmission line (we will make it the same as Z_0), we can see in Figure 3.9, that the circuit behaves the same for the desired frequency of $f_0 = 3GHz$. However, outside that frequency the amplification diminishes and it is not as effective as the network with the highest Z_0, smallest width of $w = 0.2mm$ (see Figure 3.8). Therefore, having a really high Z_0 in the transmission lines assures us that the bias network will work at a wider range of frequencies than our f_0.

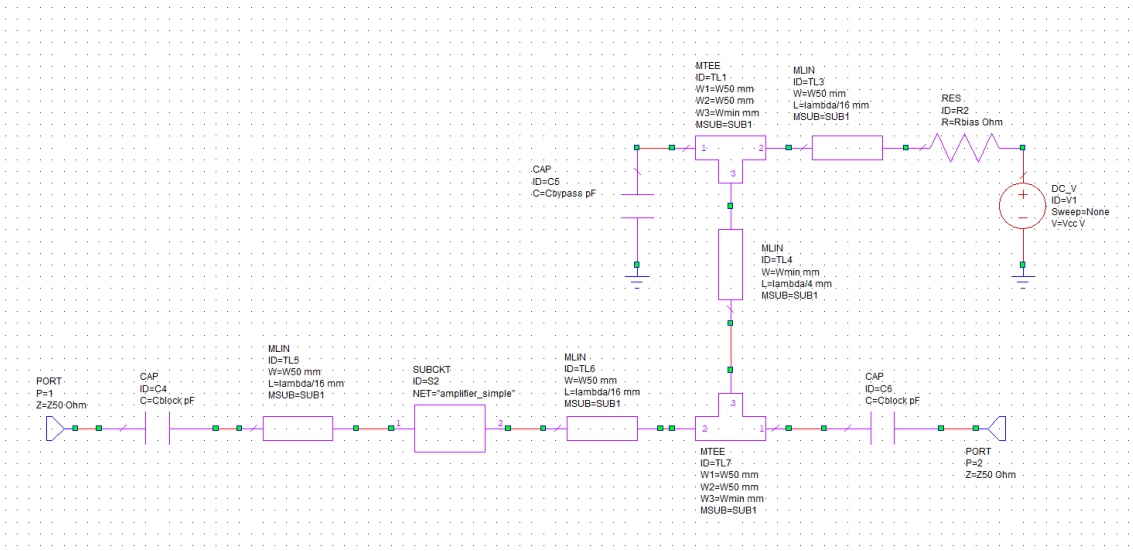


Figure 3.7: Circuit of the proposed bias network

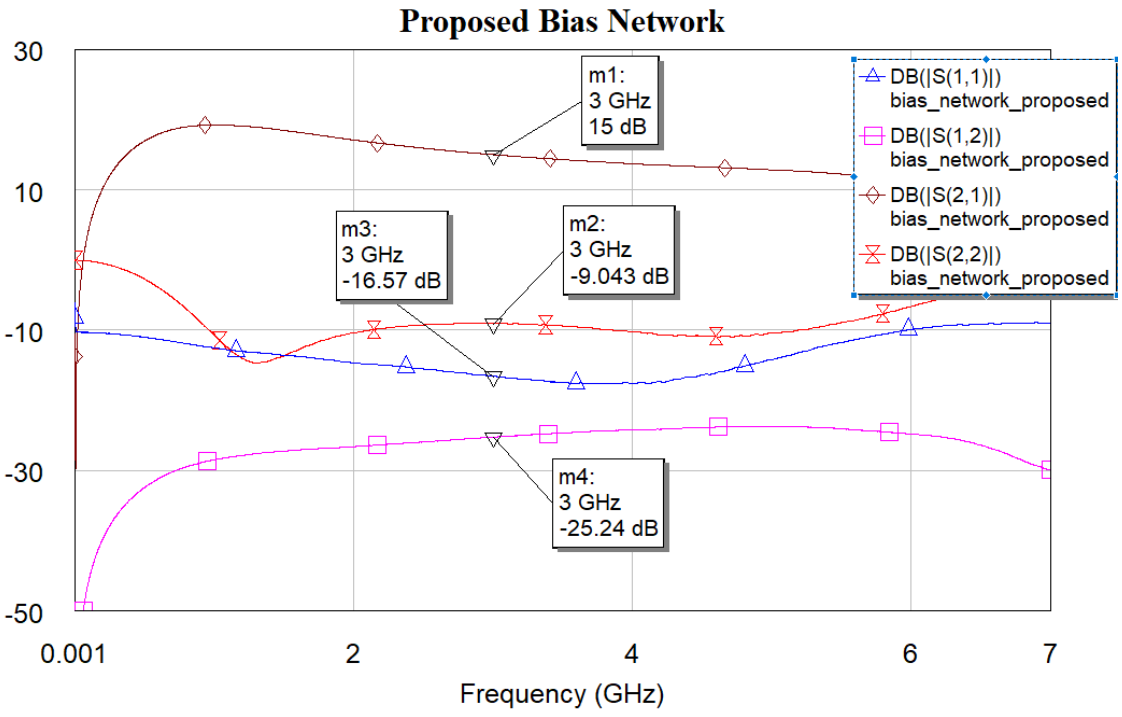


Figure 3.8: Simulation of the proposed bias network of Figure 3.7

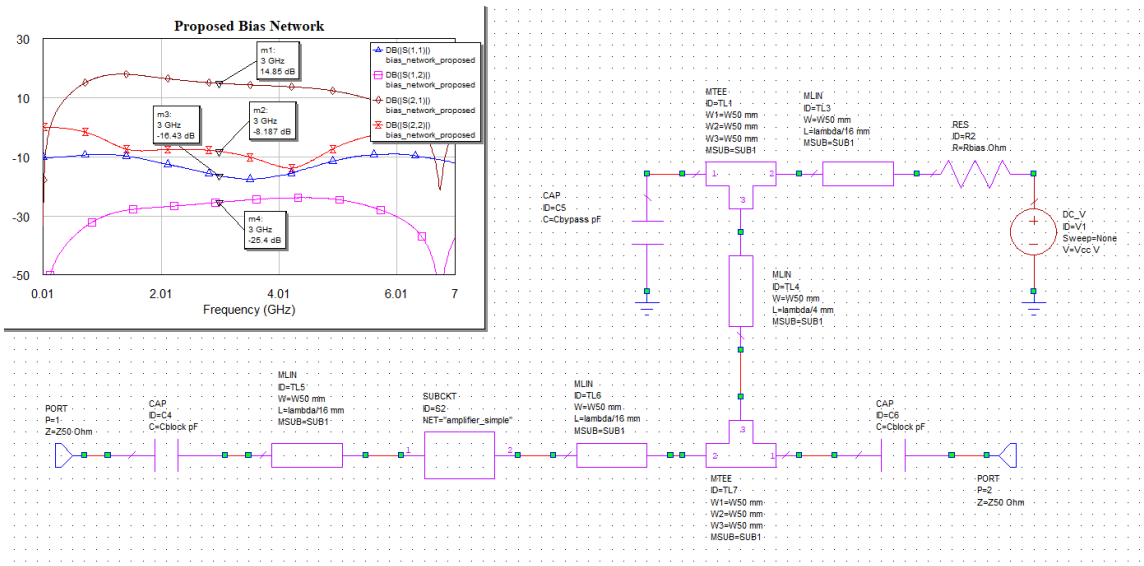


Figure 3.9: Proposed bias network with a TL width of $w = 1.85083mm$

3.2 GVA83+ response

3.2.1. Scattering parameters at f = 3 GHz

In our case, with a working frequency of f = 3 GHz (see Figure 1.1) and for the nominal temparture and bias conditions ($V_{CC} = 5V, R_{bias} = 7.5\Omega$), we get the following scattering parameters:

$$[S] = \begin{bmatrix} s_{11} = -16.87\ dB & s_{12} = -25.06\ dB \\ s_{21} = 15.34\ dB & s_{22} = -10.68\ dB \end{bmatrix}$$

Where:

s_{11} : Input Return Loss

s_{12} : Isolation

s_{21} : Gain

s_{22} : Output Return Loss

Note: this parameters are for the frequency $f = 2.9GHz$ (see Figure 3.10). However, that frequency is really close to our working frequency of $f = 3GHz$ so there will be almost the same.

MMIC Amplifier **GVA-83+**

Typical Performance Data

NOTE: Use PDF Bookmarks to view DATA at required conditions

Definitions:
Input Return Loss = -S11 (dB)
Gain(Power Gain) = S21 (dB)
Reverse Isolation = -S12 (dB)
Output Return Loss = -S22 (dB)

TEST CONDITIONS: Vd = 5.00V, Rb=7.5Ω @ Temperature = +25degC

FREQ	Gain	Isolation	Input Return Loss	Output Return Loss	Stability		IP-3 Output	1dB Comp. Output	Noise Figure
(MHz)	(dB)	(dB)	(dB)	(dB)	K	Measure	(dBm)	(dBm)	(dB)
2700.0	15.70	25.30	17.62	10.77	1.50	0.83	32.54	18.79	6.22
2900.0	15.34	25.06	16.87	10.68	1.53	0.84	32.43	18.72	6.22
3100.0	15.02	24.79	16.80	10.77	1.51	0.84	32.60	18.43	6.25

Figure 3.10: Scattering Parameters from the GVA-83+ datasheet

3.2.2. Gain of each amplifier stage and the full two-stage network

The gain of just one amplifier is the scattering parameter s_{21}, so in our case the gain is $G = S21 = 15.34\ dB$. As the first stage and the second stage have just one amplifier, the gain of both of the will be the same of $G = 15.34\ dB$. That is because the second stage behaves like a isolated amplifier with respect to the first stage.

For the full network, the gain of the whole circuit will be the product of both amplifiers as they are isolated to each other. That is the total gain will be $G_T = s_{21}^2$, so in dB it is $G_T = 2 \cdot s_{21}(in\ dB) = 2 * 15.34 = 30.60\ dB$.

3.2.3. Comparison of the wide band S parameters with the data sheet

In the Figure 3.11, we can see the scattering parameters at our working frequency $f = 3GHz$. If we take a look at each parameter, we can clearly see that they are almost the same values as the ones we obtained from the datasheet (see Figure 3.10).

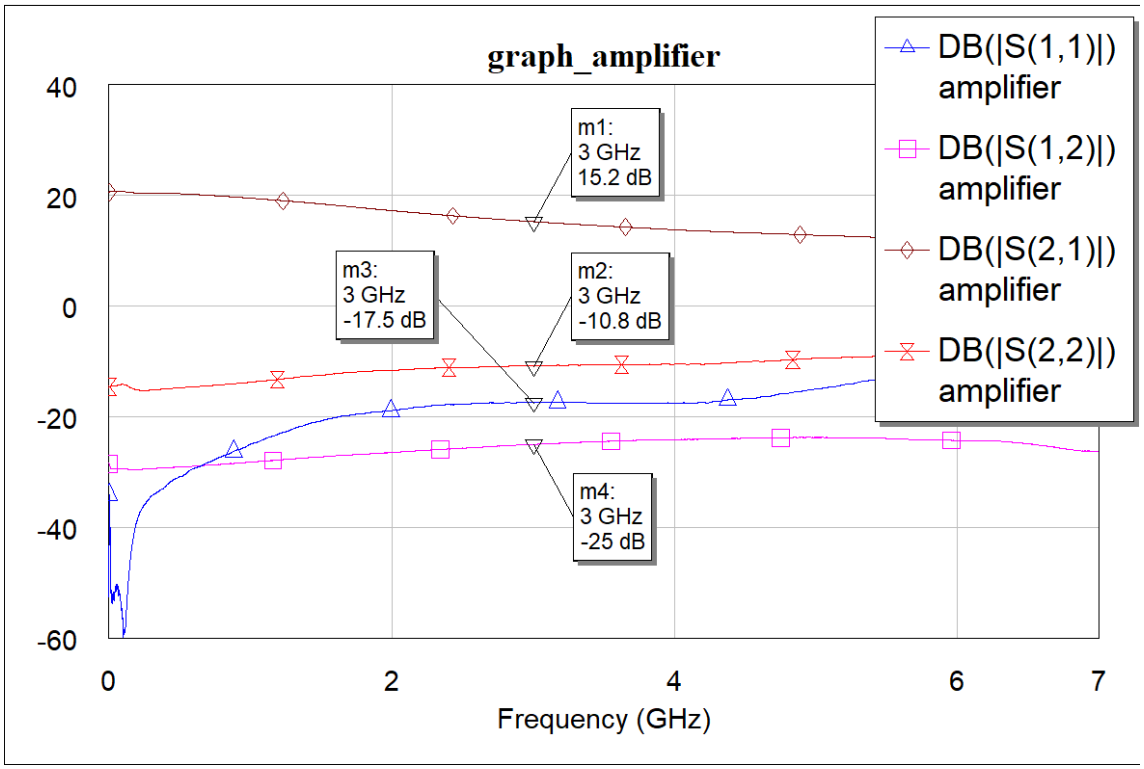


Figure 3.11: AWR Graph of the GVA83+ Amplifier

3.3 Second Stage: Balanced Amplifier

The second amplifier will be a balanced amplifier, that is a amplifier that first divides the signal into 2 signals and amplifies them separately. The idea with this amplifier, is to apply a phase shift to the signals of 180 degrees and them join them again at the end. With this configuration, as we are adding to signals that where shifted 180 degrees, any noise that we get in the amplifiers will be cancelled out resulting in a much cleaner signal.

For our case, we will have 3 different configurations depending on the order of the amplification and the phase shift. The configurations are described in Figure 3.12. So let's get started and start by studying the different configurations.

Note: that for all of the configurations we will consider ideal Wilkinson combiners / dividers and a reference impedance of $Z_0 = 50\Omega$. And we will be using the following scattering parameters:

For the Wilkinson we will be using:

$$[S_W] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}$$

For the amplifier:

$$[S_A] = \begin{bmatrix} s_{11A} & s_{12A} \\ s_{21A} & s_{22A} \end{bmatrix}$$

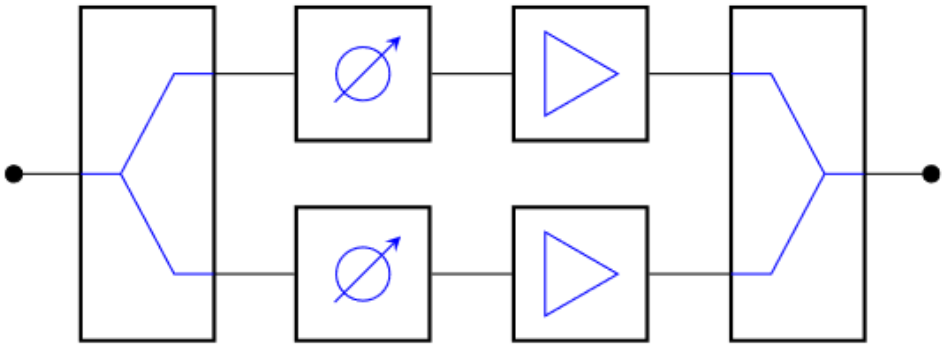
And finally for the phase shifter:

$$[S_\phi] = \begin{bmatrix} 0 & e^{-j\phi} \\ e^{-j\phi} & 0 \end{bmatrix}$$

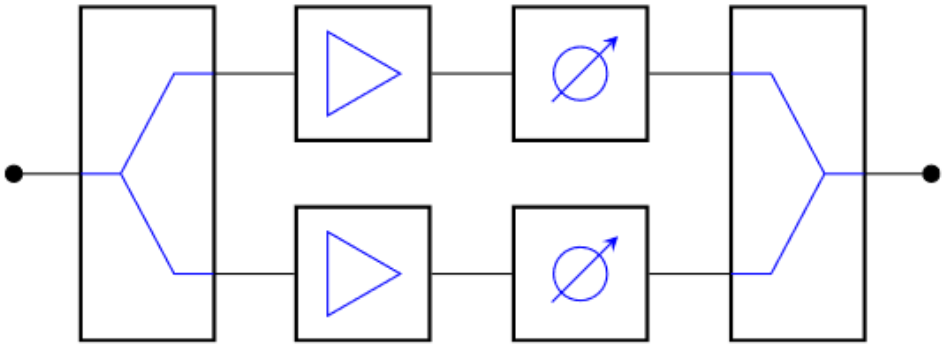
3.3.1. S matrix for configuration (a) of Figure 3.12

For the first configuration, we get the following scattering parameters:

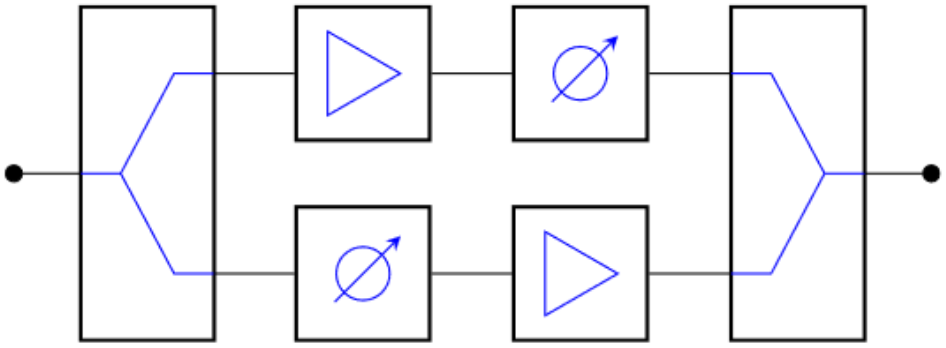
$$[S] = \begin{bmatrix} -s_{11A}e^{-2j\phi} & -s_{21A}e^{-j\phi} \\ -s_{21A}e^{-j\phi} & -s_{22A} \end{bmatrix}$$



(a) Phase shifters at the input.



(b) Phase shifters at the output.



(c) One phase shifter at each location.

Figure 3.12: 3 different configurations for the Balanced Stage

Note: that $s_{21} = s_{12}$ as the S matrix is reciprocal.

3.3.2. S matrix for configuration (b) of Figure 3.12

For the second configuration, we get the following scattering parameters:

$$[S] = \begin{bmatrix} -s_{11A} & -s_{21A}e^{-j\phi} \\ -s_{21A}e^{-j\phi} & -s_{22A}e^{-2j\phi} \end{bmatrix}$$

Note: that $s_{21} = s_{12}$ as the S matrix is reciprocal.

3.3.3. S matrix for configuration (c) of Figure 3.12

Finally, for the last configuration, we get the following scattering parameters:

$$[S] = \begin{bmatrix} -\frac{s_{11A}}{2}(1 + e^{-2j\phi}) & -s_{21A}e^{-j\phi} \\ -s_{21A}e^{-j\phi} & -\frac{s_{22A}}{2}(1 + e^{-2j\phi}) \end{bmatrix}$$

Note: that $s_{21} = s_{12}$ as the S matrix is reciprocal.

3.3.4. Comparison between the different configuration of Figure 3.12 and the simple amplifier

Now that we have the 3 different S matrices, we can observe that they have the same transmission coefficients $s_{21} = s_{12} = -s_{21A}e^{-j\phi}$. That means that they will transmit the same power to the load. This makes sense as the only thing that differs between the configurations is the order of the components, but they are still the same.

On the other hand, if we consider the reflection coefficients (s_{11} and s_{22}), we can see that they differ from one configuration to another. In order to see which configuration is best, we want the lowest reflection coefficients in order to have the least amount of power reflected as possible. In the first 2 configurations we can see that either s_{11} or s_{22} cannot be 0 (as they are not symmetrical), which means that in this two configuration we will have always some loss.

However, if we take a look at the last configuration we can see that if we apply a certain phase shift ϕ, where $e^{-j\phi} = -1$, both coefficients become 0. Thus making the amplifier perfectly matchable without having any reflection. And for this very reason, the third configuration is best as we can achieve no reflection.

3.3.5. Optimal phase shift

As stated before, in order to have the (c) configuration to behave without losses, we need to make that $-\frac{s_{11A}}{2}(1 + e^{-2j\phi}) = 0$. In order to do that, let's solve for ϕ:

$$
\begin{aligned}
-\frac{s_{11a}}{2}(1 + e^{-2j\phi}) &= 0 \\
\rightarrow (1 + e^{-2j\phi}) &= 0 \\
\rightarrow e^{-2j\phi} &= -1 \\
\rightarrow \phi &= \frac{\pi}{2}
\end{aligned}
$$

So the optimal phase shift for the configuration (c) is $\phi = \frac{\pi}{2}$.

3.3.6. Relationship between the output power at each branch of the balanced stage, and the total power at the output of the full balanced stage

As shown previously in the Subsection 3.2.2, we can see that the gain of one amplifier is $G = 15.34dB$. As we are dividing the input power by half at the input and the amplifying in each branch, the power at the end of each branch will be the same and will have a gain of $12.34dB$ with respect to the input power at the balanced stage. Finally, as we are combining both signals with the same phase, we will have a total gain of $G_T = 15.34dB$ in balanced stage.

If we simulate the results (see the circuit in Figure 3.13), we can see that the gain of the amplifier is exactly 15 dB, almost the same as the one calculated (see Figure 3.14).

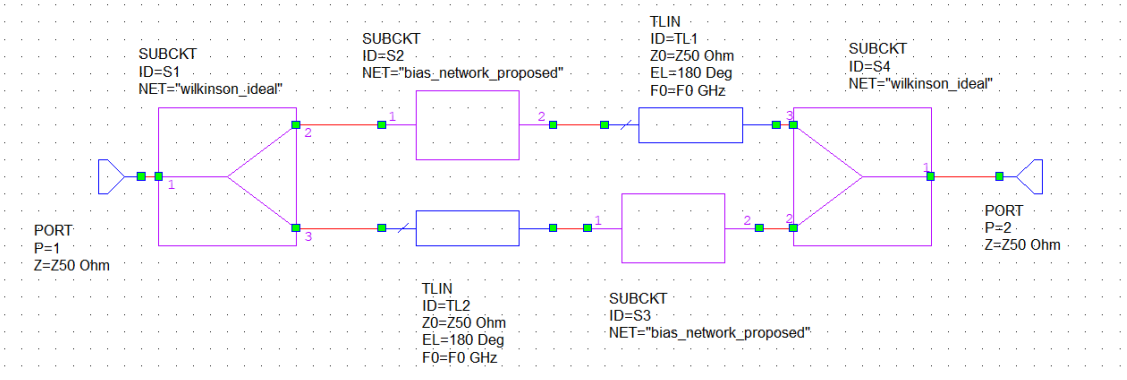


Figure 3.13: Ideal balanced amplifier circuit

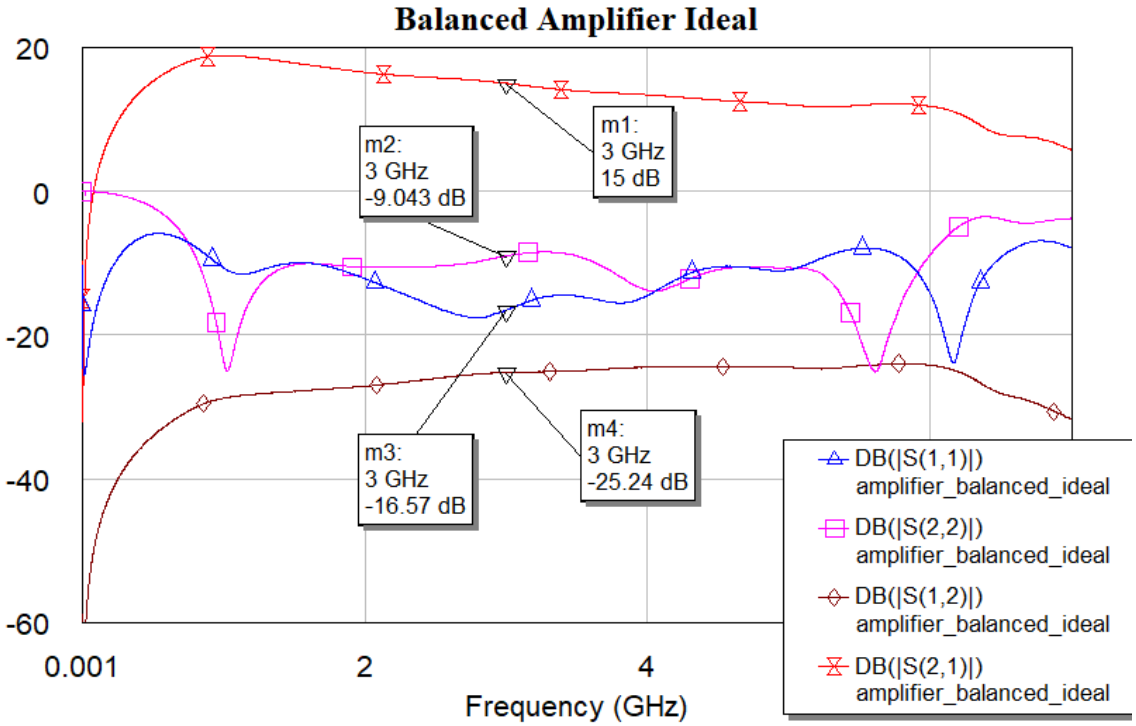


Figure 3.14: Simulation of the ideal balanced amplifier (see Figure 3.13)

3.4 Band Pass Filter

3.4.1. Filter order from the bandwidth, in-band return loss and the minimum attenuation at the stop bands

Given the following values in the Figure 1.1:

$$\begin{aligned}
\text{Center frequency} &: f_0 = 3GHz \\
\text{Pass band lower limit} &: f_{p1} = 2.925GHz \\
\text{Pass band upper limit} &: f_{p2} = 3.075GHz \\
\text{Lower attenuation band limit} &: f_{a1} = 2.85GHz \\
\text{Upper attenuation band limit} &: f_{a2} = 3.15GHz
\end{aligned}$$

Where:

$$\begin{aligned}
w'_{p1} &= 2\pi f'_{p1} = 2\pi 2.925 \cdot 10^9 = 1.838 \cdot 10^{10} rad/s \\
w'_{p2} &= 2\pi f'_{p2} = 2\pi 3.075 \cdot 10^9 = 1.932 \cdot 10^{10} rad/s \\
w'_{a1} &= 2\pi f'_{a1} = 2\pi 2.85 \cdot 10^9 = 1.791 \cdot 10^{10} rad/s \\
w'_{a2} &= 2\pi f'_{a2} = 2\pi 3.15 \cdot 10^9 = 1.979 \cdot 10^{10} rad/s
\end{aligned}$$

And also, we have a requirement of a minimum attenuation of 25 dB. Therefore, we will be choosing an attenuation of $\alpha_a = 30dB$ to be sure that the filter works correctly. As we want the input losses to be bigger than $20dB$ then:

$$\begin{aligned}
s_{11} >= 30dB \Rightarrow s_{11} &= 30dB \\
s_{11} &= 10^{\frac{-30}{20}} = 0.032
\end{aligned}$$

Now that we have the return loss, we can calculate the maximum transmission loss (or better said the maximum pass band attenuation). As we want our filter to be lossless, then $s_{11}^2 + s_{12}^2 = 1$. With this formula and the previous value we calculated, we can get the following:

$$\begin{aligned}\alpha_p &= -20\log_{10}(s_{12}) \\ &= 20\log_{10}(\sqrt{1-s_{11}^2}) \\ &= 20\log_{10}(\sqrt{1-0.032^2}) \\ &= 4.45\cdot 10^{-3} dB\end{aligned}$$

Now with the attenuation at each stage, the bandwidth of our filter is:

$$\begin{aligned}B &= \frac{(w'_{p2}-w'_{p1})}{w_p} = \frac{1.932\cdot 10^{10}-1.838\cdot 10^{10}}{1} \\ &= 9.4\cdot 10^{8} rad/s\end{aligned}$$

Where:

$w_p = 1 rad/s$ as it is the normalized angular frequency

And finally, we can calculate the filter order of our design by:

$$\begin{aligned}N &\geq \frac{\cosh^{-1} 1/k_d}{\cosh^{-1} 1/k_s} \\ &\geq \frac{\cosh^{-1} 1/1.013\cdot 10^{-3}}{\cosh^{-1} 1/0.509} \\ &\geq 5.853 \Rightarrow N = 6\end{aligned}$$

Where:

$$
\begin{aligned}
w_0^2 &= w'_{p2} w'_{p1} = 1.932 \cdot 10^{10} \cdot 1.838 \cdot 10^{10} \\
&= 3.551 \cdot 10^{20}\ (rad/s)^2 \\
w_{a1} &= \frac{((w'_{a1})^2 - w_0^2)}{B w'_{a1}} = \frac{(1.791 \cdot 10^{10})^2 - 3.551 \cdot 10^{20}}{9.4 \cdot 10^8 \cdot 1.791 \cdot 10^{10}} \\
&= -2.029 \\
w_{a2} &= \frac{((w'_{a2})^2 - w_0^2)}{B w'_{a2}} = \frac{(1.979 \cdot 10^{10})^2 - 3.551 \cdot 10^{20}}{9.4 \cdot 10^8 \cdot 1.979 \cdot 10^{10}} \\
&= 1.964 \\
w_a &= \min(|w_{a1}|, |w_{a2}|) = \min(2.029, 1.964) \\
&= 1.964 \\
k_s &= \frac{w_p}{w_a} = \frac{1}{1.964} \\
&= 0.509 \\
k_d &= \sqrt{\frac{1 - 10^{\alpha_p/10}}{1 - 10^{\alpha_a/10}}} = \sqrt{\frac{1 - 10^{4.45 \cdot 10^{-3}/10}}{1 - 10^{30/10}}} \\
&= 1.013 \cdot 10^{-3}
\end{aligned}
$$

3.4.2. Parameters of the frequency and impedance transforms

For the parameters, there were calculate before in order to get the filter order. We get a center pulsation of $w_0 = 1.8844 \cdot 10^{10} rad/s = 3GHz$ as expected and a bandwidth of $B = 9.4 \cdot 10^9 rad/s = 0.15GHz$; which correspond to the requirements of the filter.

3.4.3. Calculations of the normalized elements of the Chebyshev filter

To calculate the coefficients of the Chebyshev filter with order 6, we will be using the calculator found in Aula Global. In our case, as the requirements for the return losses are that it must be at least 18 dB, we will be using an attenuation of 25 dB. See Figure 3.15 to see the coefficients we will be using for the normalized elements (g_i).

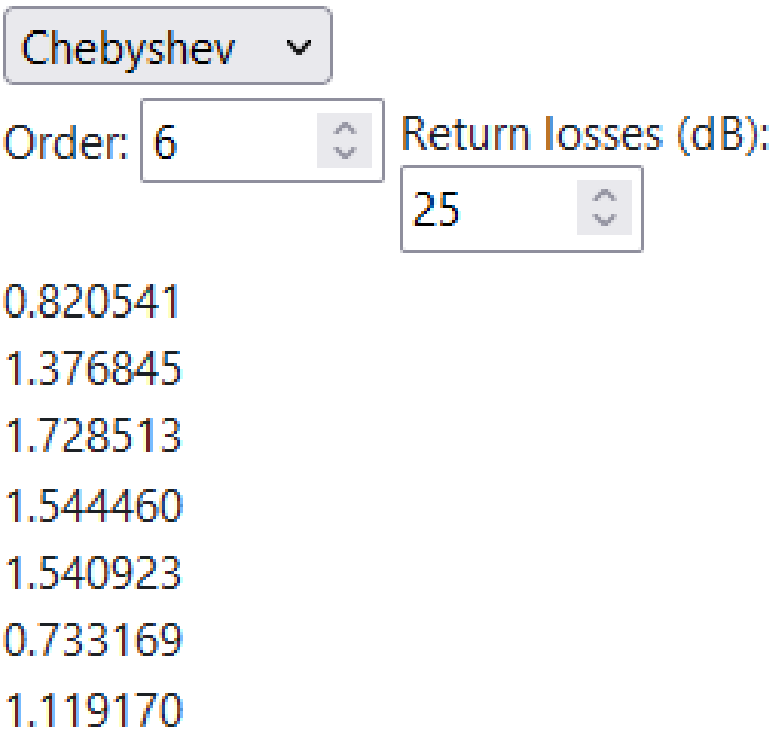


Figure 3.15: Calculations of the Chebyshev coefficients using the Aula Global calculator

Here are the values that we will be using:

$$g_1 = 0.820541$$
$$g_2 = 1.376845$$
$$g_3 = 1.728513$$
$$g_4 = 1.544460$$
$$g_5 = 1.540923$$
$$g_6 = 0.733169$$
$$g_7 = 1.119170$$

3.4.4. Calculations of the inverters and even and odd impedances of the couple lines

In order to calculate the inverters (J_i), we will use a bandwidth of $\Delta = 5\%$ as stated in the requirements. So let's calculate the inverters for the pass band filter to be able to implemented as a series of coupled lines. Note that as our filter order is 6, we will be using $6 + 1 = 7$ coupled lines.

$$J_1 \cdot Z_0 = \sqrt{\frac{\pi\Delta}{2g_1}} = \sqrt{\frac{\pi \cdot 0.05}{2 \cdot 0.820541}} = 0.30938$$
$$J_2 \cdot Z_0 = \frac{\pi\Delta}{2 \cdot \sqrt{g_1 \cdot g_2}} = \frac{\pi \cdot 0.05}{2 \cdot \sqrt{0.820541 \cdot 1.376845}} = 0.07389$$
$$J_3 \cdot Z_0 = \frac{\pi\Delta}{2 \cdot \sqrt{g_2 \cdot g_3}} = \frac{\pi \cdot 0.05}{2 \cdot \sqrt{1.376845 \cdot 1.728513}} = 0.05091$$
$$J_4 \cdot Z_0 = \frac{\pi\Delta}{2 \cdot \sqrt{g_3 \cdot g_4}} = \frac{\pi \cdot 0.05}{2 \cdot \sqrt{1.728513 \cdot 1.544460}} = 0.048069$$
$$J_5 \cdot Z_0 = \frac{\pi\Delta}{2 \cdot \sqrt{g_4 \cdot g_5}} = \frac{\pi \cdot 0.05}{2 \cdot \sqrt{1.544460 \cdot 1.540923}} = 0.050911$$
$$J_6 \cdot Z_0 = \frac{\pi\Delta}{2 \cdot \sqrt{g_5 \cdot g_6}} = \frac{\pi \cdot 0.05}{2 \cdot \sqrt{1.540923 \cdot 0.733169}} = 0.073892$$
$$J_7 \cdot Z_0 = \sqrt{\frac{\pi\Delta}{2 \cdot g_6 \cdot g_7}} = \sqrt{\frac{\pi \cdot 0.05}{2 \cdot 0.733169 \cdot 1.119170}} = 0.309382$$

And now we calculate the even and odd impedances of the coupled lines:

$$Z_{0e1} = Z_0 \cdot (1 + J_1 \cdot Z_0 + (J_1 \cdot Z_0)^2) = 50 \cdot (1 + 0.30938 + (0.30938)^2) = 70.255\Omega$$
$$Z_{0o1} = Z_0 \cdot (1 - J_1 \cdot Z_0 + (J_1 \cdot Z_0)^2) = 50 \cdot (1 - 0.30938 + (0.30938)^2) = 39.317\Omega$$
$$Z_{0e2} = Z_0 \cdot (1 + J_2 \cdot Z_0 + (J_2 \cdot Z_0)^2) = 50 \cdot (1 + 0.07389 + (0.07389)^2) = 53.967\Omega$$
$$Z_{0o2} = Z_0 \cdot (1 - J_2 \cdot Z_0 + (J_2 \cdot Z_0)^2) = 50 \cdot (1 - 0.07389 + (0.07389)^2) = 46.578\Omega$$
$$Z_{0e3} = Z_0 \cdot (1 + J_3 \cdot Z_0 + (J_3 \cdot Z_0)^2) = 50 \cdot (1 + 0.05091 + (0.05091)^2) = 52.675\Omega$$
$$Z_{0o3} = Z_0 \cdot (1 - J_3 \cdot Z_0 + (J_3 \cdot Z_0)^2) = 50 \cdot (1 - 0.05091 + (0.05091)^2) = 47.584\Omega$$
$$Z_{0e4} = Z_0 \cdot (1 + J_4 \cdot Z_0 + (J_4 \cdot Z_0)^2) = 50 \cdot (1 + 0.048069 + (0.048069)^2) = 52.519\Omega$$
$$Z_{0o4} = Z_0 \cdot (1 - J_4 \cdot Z_0 + (J_4 \cdot Z_0)^2) = 50 \cdot (1 - 0.048069 + (0.048069)^2) = 47.712\Omega$$
$$Z_{0e5} = Z_0 \cdot (1 + J_5 \cdot Z_0 + (J_5 \cdot Z_0)^2) = 50 \cdot (1 + 0.050911 + (0.050911)^2) = 52.675\Omega$$
$$Z_{0o5} = Z_0 \cdot (1 - J_5 \cdot Z_0 + (J_5 \cdot Z_0)^2) = 50 \cdot (1 - 0.050911 + (0.050911)^2) = 47.584\Omega$$
$$Z_{0e6} = Z_0 \cdot (1 + J_6 \cdot Z_0 + (J_6 \cdot Z_0)^2) = 50 \cdot (1 + 0.073892 + (0.073892)^2) = 53.968\Omega$$
$$Z_{0o6} = Z_0 \cdot (1 - J_6 \cdot Z_0 + (J_6 \cdot Z_0)^2) = 50 \cdot (1 - 0.073892 + (0.073892)^2) = 46.578\Omega$$
$$Z_{0e7} = Z_0 \cdot (1 + J_7 \cdot Z_0 + (J_7 \cdot Z_0)^2) = 50 \cdot (1 + 0.309382 + (0.309382)^2) = 70.255\Omega$$
$$Z_{0o7} = Z_0 \cdot (1 - J_7 \cdot Z_0 + (J_7 \cdot Z_0)^2) = 50 \cdot (1 - 0.309382 + (0.309382)^2) = 39.317\Omega$$

3.4.5. Simulation of the ideal band pass filter

In order to simulate the band pass filter, we will implement it with ideal inverters first and then with ideal coupled lines. And after that we will compare the two and see if we get similar results.

In the Figure 3.16, we can see the circuit we implemented with inverters and the values calculated previously. If we check the simulation (see Figure 3.17), we can see that the filter behaves correctly as the requirements stated. The attenuation at the pass band is less than 25 dB while the attenuation outside the attenuation band is more than 30 dB.

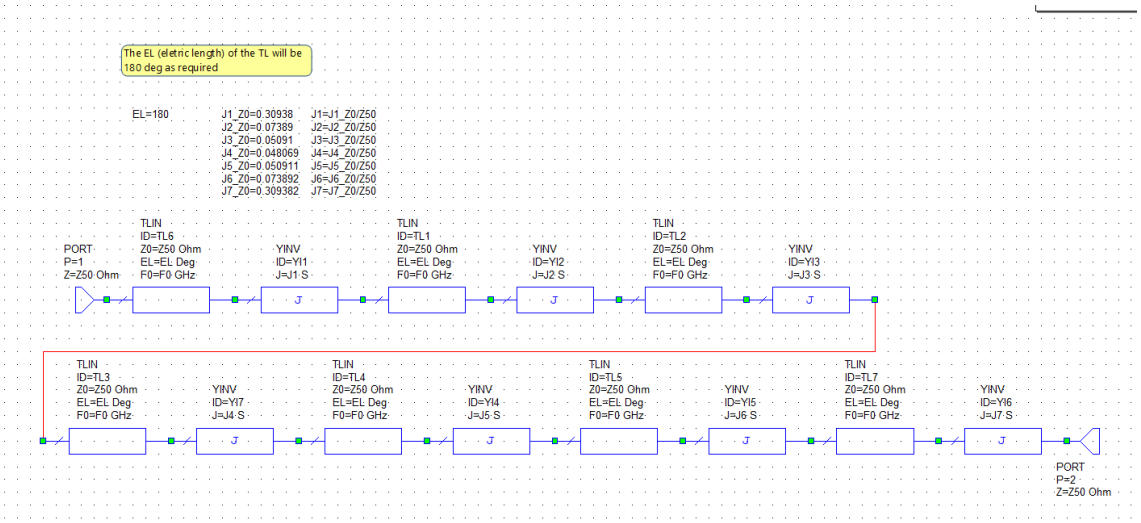


Figure 3.16: Circuit implementation of the band pass filter with inverters

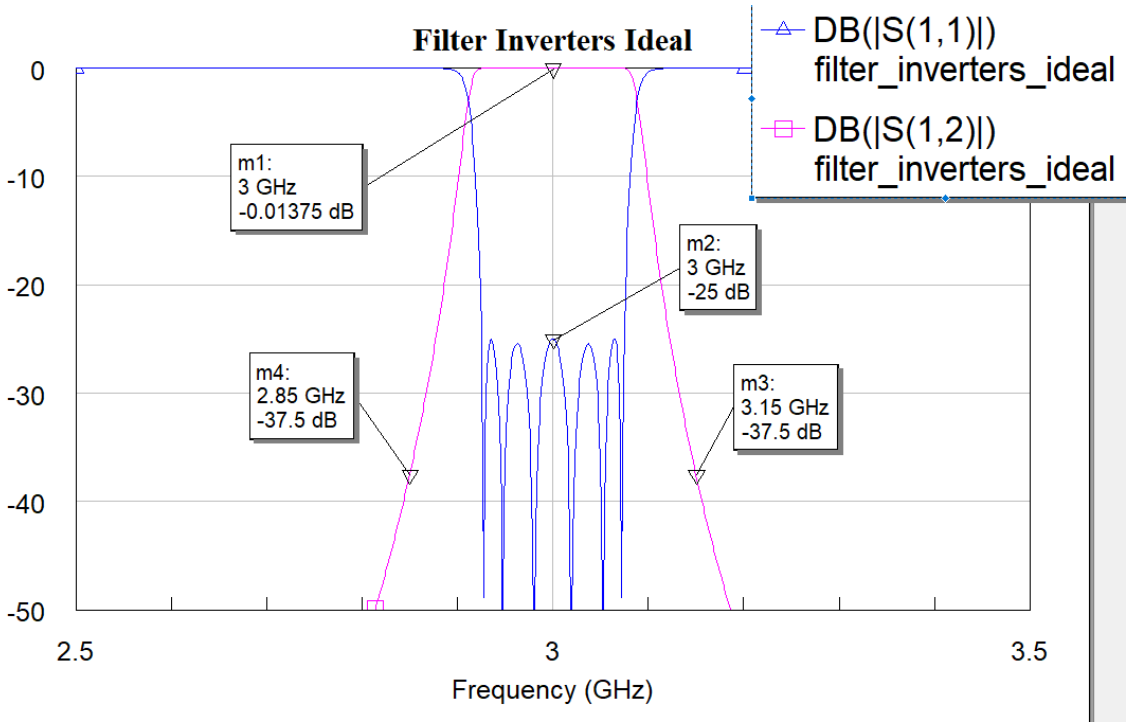


Figure 3.17: Simulation of the band pass filter with inverters of Figure 3.16

Now, that we know that our coefficients are correctly calculated, we will implement the pass band filter with ideal coupled lines. For that we will be using the different even and odd impedances calculated previously. For the circuit shown in the Figure 3.18, we get the simulation in Figure 3.19. In the simulation we can see that we get the same results as the filter implementation with inverters (see Figure 3.17).

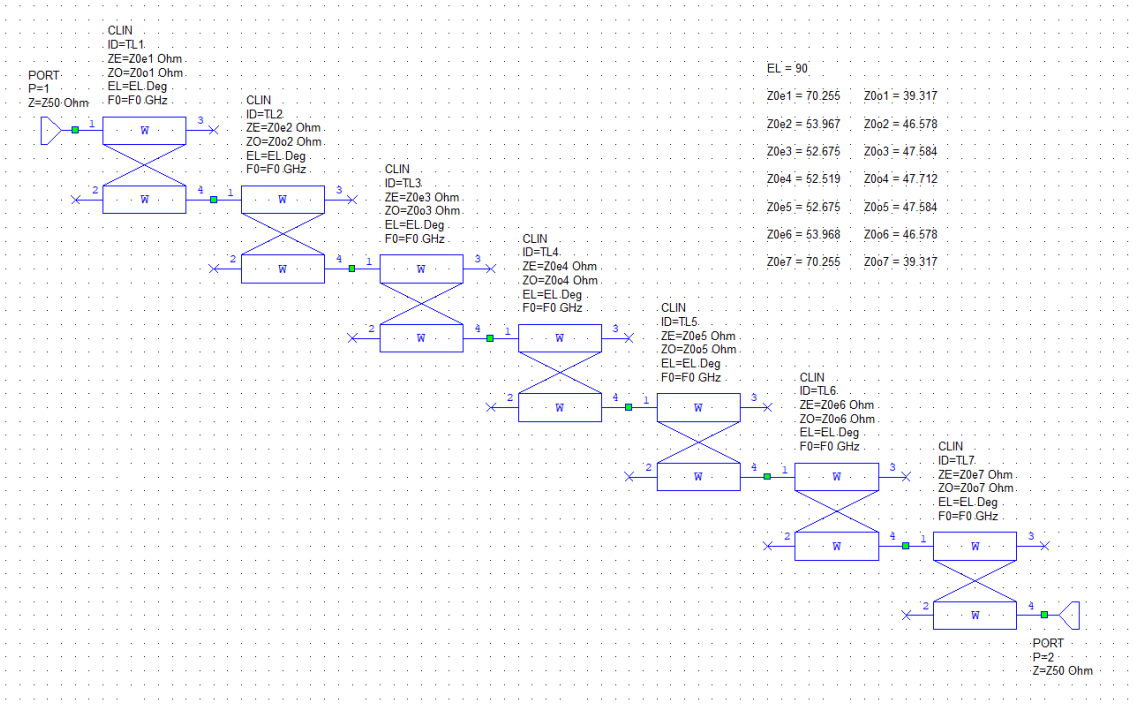


Figure 3.18: Filter implementation with ideal coupled lines

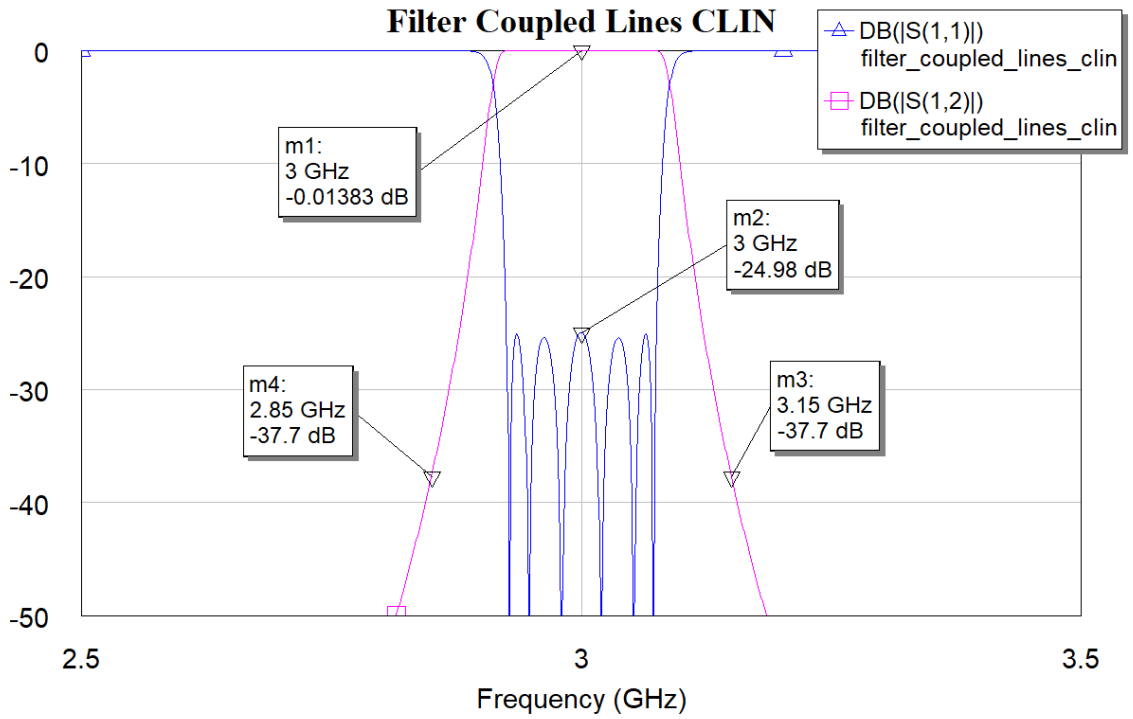


Figure 3.19: Simulation of the filter implementation with ideal coupled lines (see Figure 3.18)

3.5 Directional Coupler

In order to measure the signal and check the correct functionality, we will be using a directional coupler. Let's start with the study of the element.

3.5.1. Electrical length and even and odd characteristic impedances of the couple-line section

According to the requirements of the system, the power at the monitor port must be 20 dB below the main line. That means that the coupling of the directional amplifier must be $C_{dB} = 20dB$.

$$\begin{aligned} C &= 10^{\frac{-C_{dB}}{10}} \\ &= 10^{\frac{-20}{10}} \\ &= 0.1 \end{aligned}$$

Now, in order to calculate the characteristic impedances of the even and odd modes, first we will assume an electrical length of $\lambda/4$ or the same as 90 deg. That means that the coupler will be a symmetric coupler with a 90 deg phase shift between the transmitted and the coupled port,

Given a electrical length of $\lambda/4$, then we can use the following formulas to calculate the characteristic impedances of the even and odd modes, for the even mode we get:

$$\begin{aligned} Z_{0,even} &= Z_0 \sqrt{\frac{1+C}{1-C}} \\ &= 55.28\Omega \end{aligned}$$

And for the odd mode:

$$\begin{aligned} Z_{0,odd} &= Z_0 \sqrt{\frac{1-C}{1+C}} \\ &= 45.23\Omega \end{aligned}$$

3.5.2. Connection of the coupler

For this coupler, the main objective is to transmit the whole power entering from the input to the transmitted and coupled ports. For this case, we want the following scattering parameter matrix:

$$S = \begin{bmatrix} 0 & \alpha & j\beta & 0 \\ \alpha & 0 & 0 & j\beta \\ j\beta & 0 & 0 & \alpha \\ 0 & j\beta & \alpha & 0 \end{bmatrix}$$

Where:

We assume an isolation of $I = \infty\ dB$

Port 1 is the input port

Port 2 is the coupled port

Port 3 is the transmission port

Port 4 is the isolated port

Usually for a directed port, you want that the isolated port is degenerated with respect to the other 3. Therefore, we will be loading it with a matched load, that is equal to the characteristic impedance of $Z_0 = 50\Omega$. You can see the final circuit for the directed coupler in Figure 3.20.

If we simulate the circuit with AWR (see Figure 3.21), we can see that there is no reflection at the input port as the $s_{11} = -84\ dB$, the coupling is $C = -20\ dB$ as expected, and the rest of the power is directed to the transmission port.

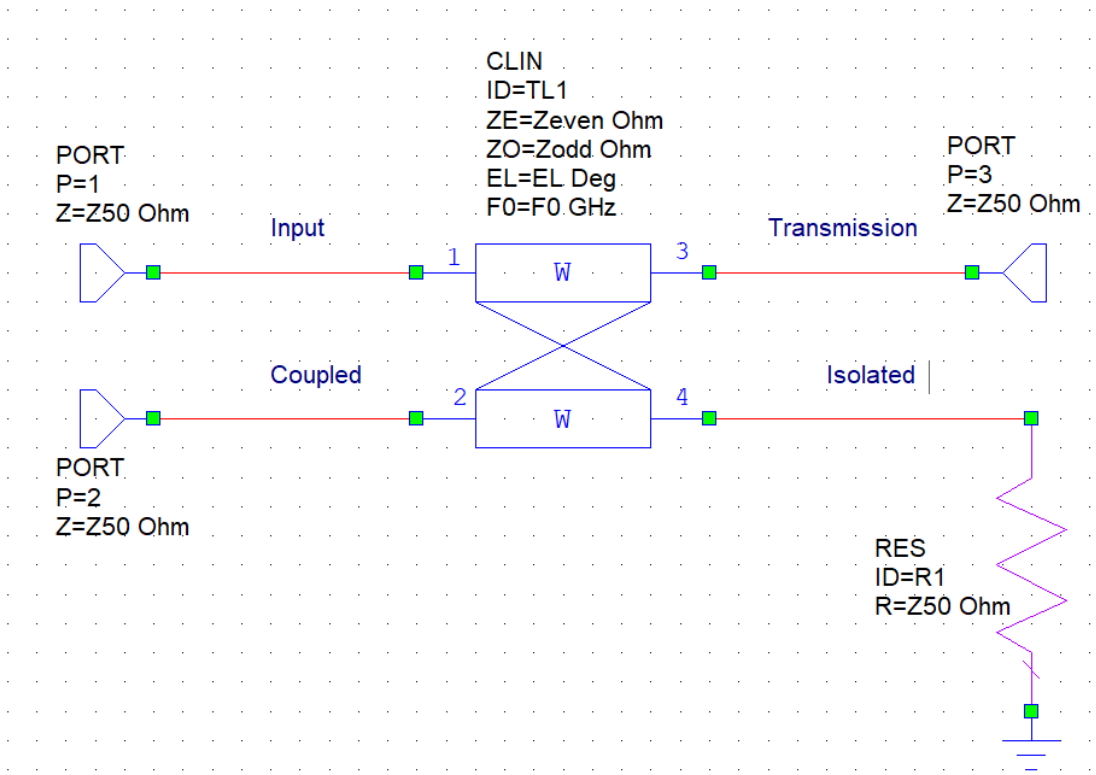


Figure 3.20: Ideal circuit for the directional coupler

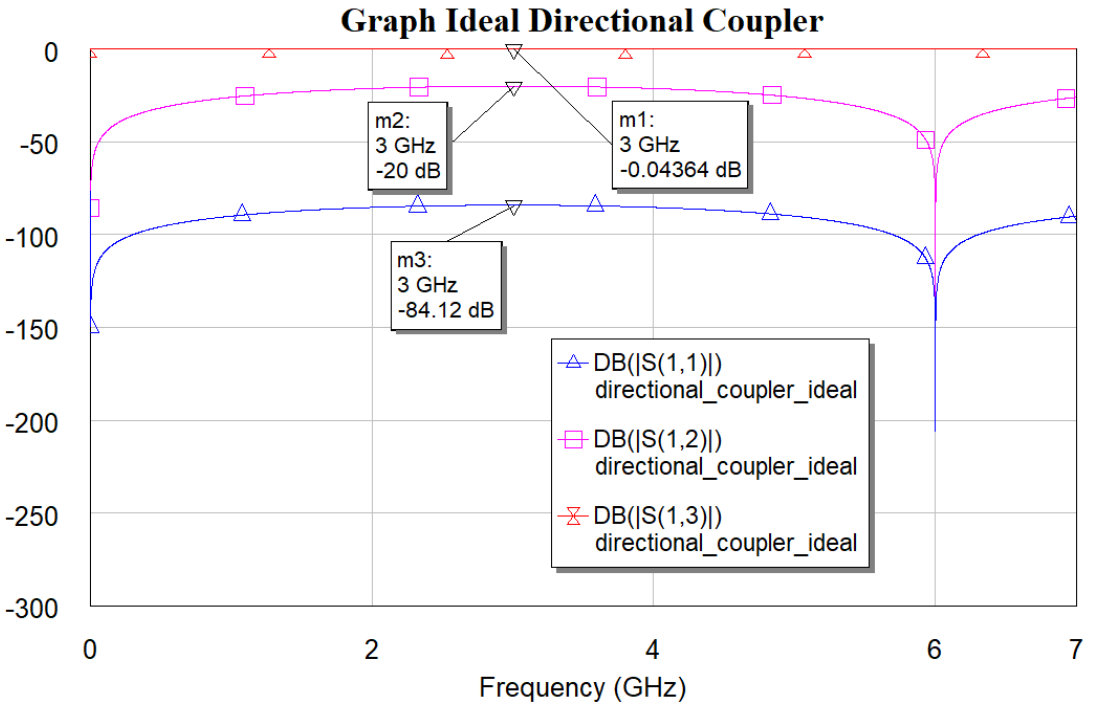


Figure 3.21: Simulation of the ideal directed coupler of Figure 3.20

Chapter 4

Design and Characterization of the Microstrip Elements

4.1 Wilkinson Power Divider / Combiner

In order to divide the input signal from the simple amplifier into to equal signals and then join the signals together after they have been amplified in the second stage, we will be using a Wilkinson divider / combiner.

4.1.1. Ideal Wilkinson Power Divider / Combiner

First we have designed an ideal Wilkinson divider / combiner (see Figure 4.1). We have used a resistance of $R = 2Z_0 = 100\Omega$ for the resistance between the two output ports. And also a characteristic impedance of the lines of $Z_{0,W} = \sqrt{2}Z_0\ \Omega = 70.71\ \Omega$.

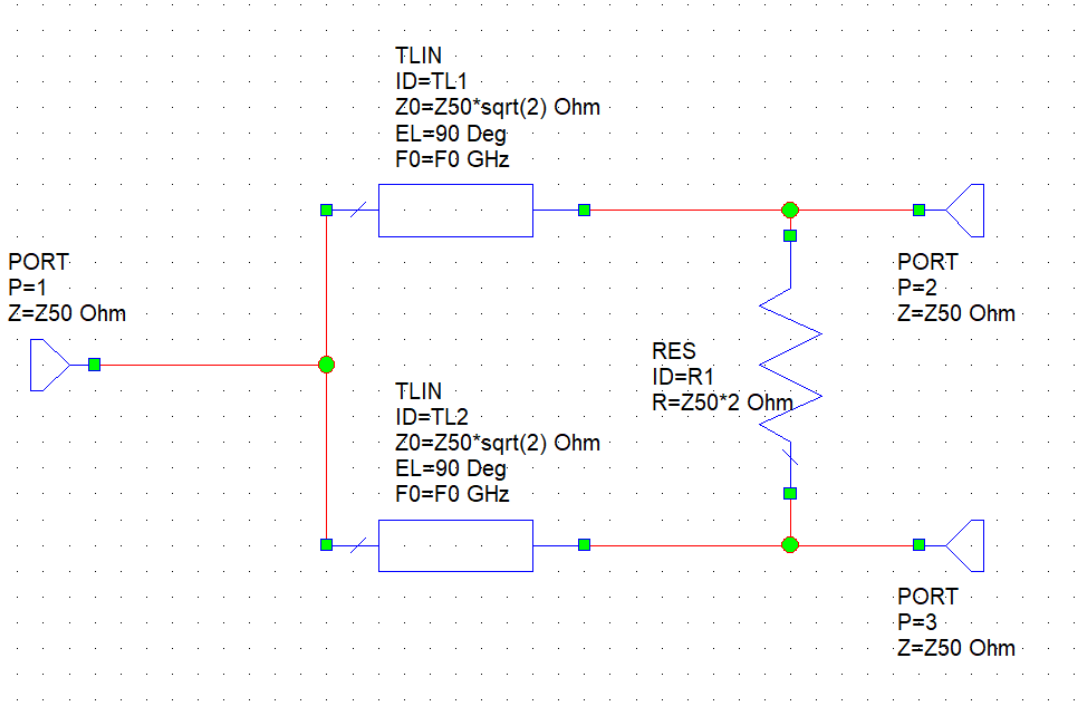


Figure 4.1: Ideal Wilkinson power divider / combiner circuit

If we simulate the circuit of Figure 4.1, we get the following graph (see Figure 4.2). Here we can see that the reflected power is 0 as $s_{11} = -249dB$. And the transmitted power for each port is $s_{21} = s_{31} = 3\ dB = 0.5$, that is half of the input power goes to each port.

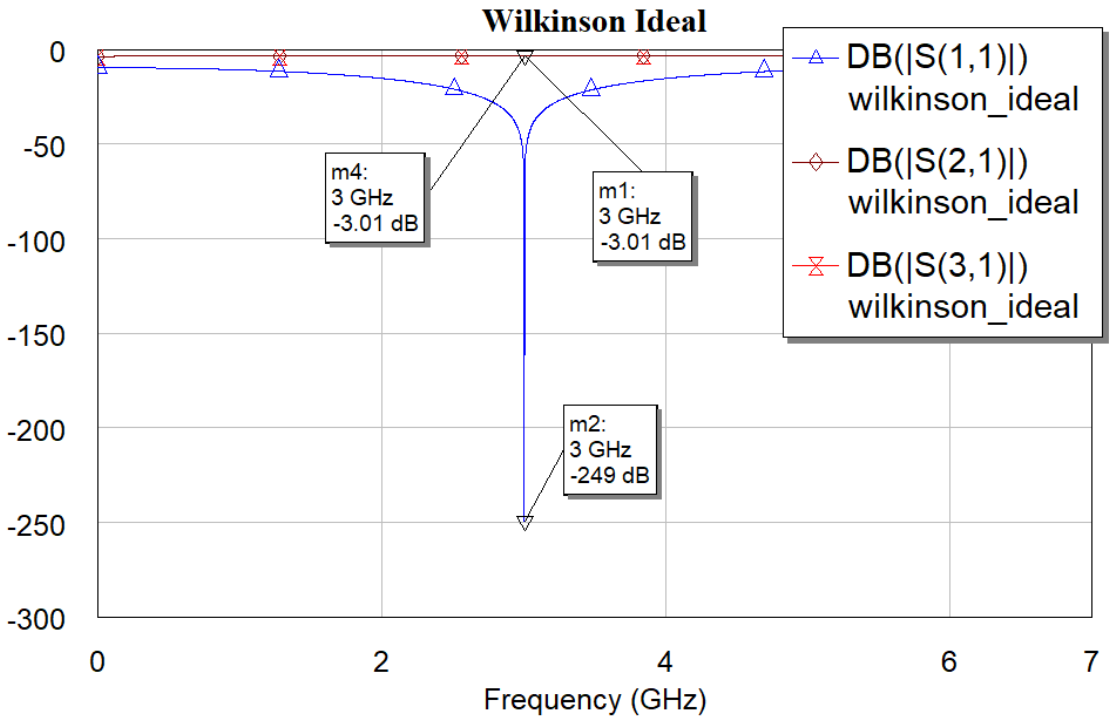


Figure 4.2: Simulation of an ideal Wilkinson power divider / combiner

4.1.2. Implementation with transmission lines

In order to implement this in our design, we will have to adapt the ideal Wilkinson power divider / combiner to our circuit. For this we will have to calculate the width and length of the TLs for a characteristic impedance of $Z_{0,W} = 70.71\ \Omega$. For this we have used the TXLine tool of AWR and we got a width of $w = 0.9065mm$ and a height of $h = 12.19mm$ (see Figure 4.3).

Now, if we simulate the following circuit with the TL with the correct dimensions (see Figure 4.4), we get the graph shown in Figure 4.5. Here we can observe that the implementation of the Wilkinson power divider / combiner works correctly as it divides the power in half and it has almost no reflection. However, this implementation is really difficult to implement in a microstrip line, so let's change the design to make it easier to implement.

4.1.3. Implementation with TEE junctions

In order to incorporate the Wilkinson power divider / combiner in a microstrip technology, we will be using TEE junctions. For this implementation we will have to calculate the different radius shown in Figure 4.6. Note that the Gap will be the one required to solder the 0603 SMD resistor, for our case, we will be using $Gap = 1mm$.

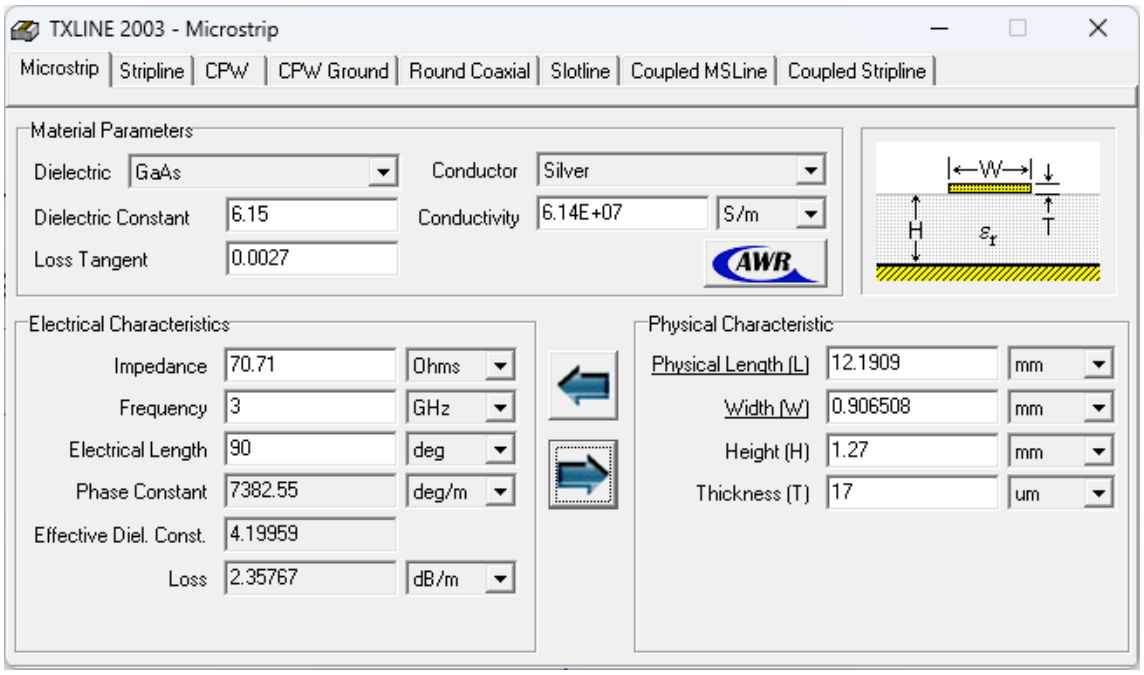


Figure 4.3: Calculations of the width and height of the Wilkinson power divider / combiner

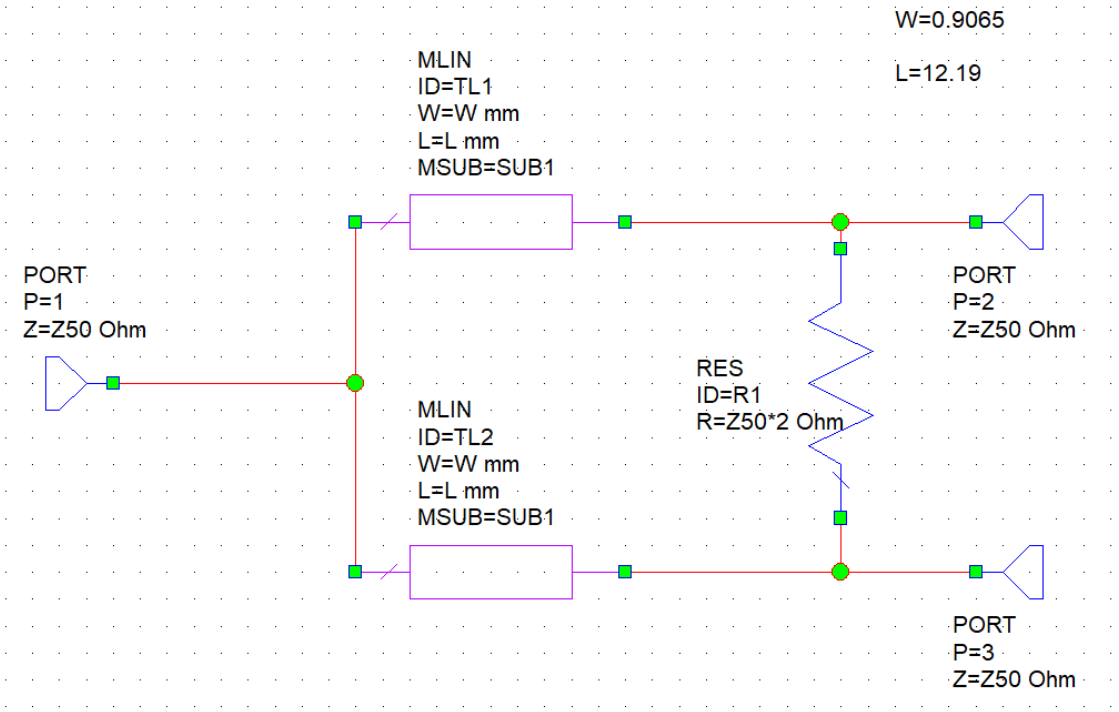


Figure 4.4: Microstrip circuit design of the Wilkinson power divider / combiner

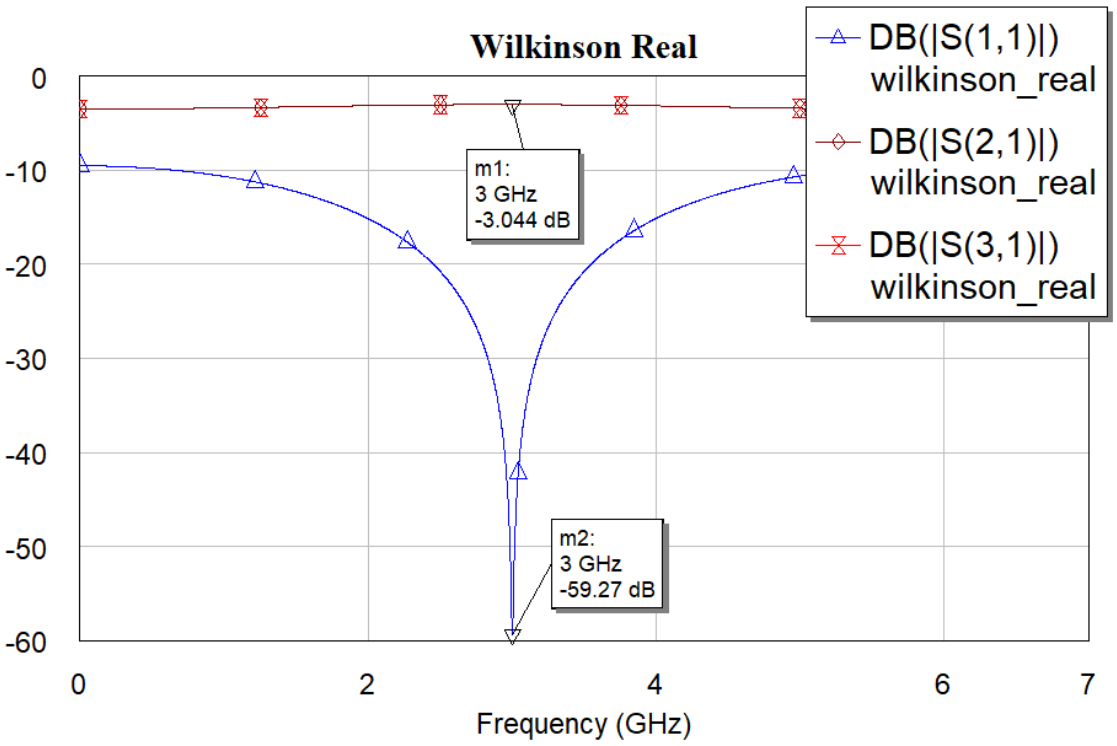


Figure 4.5: Simulation of the real Wilkinson power divider / combiner

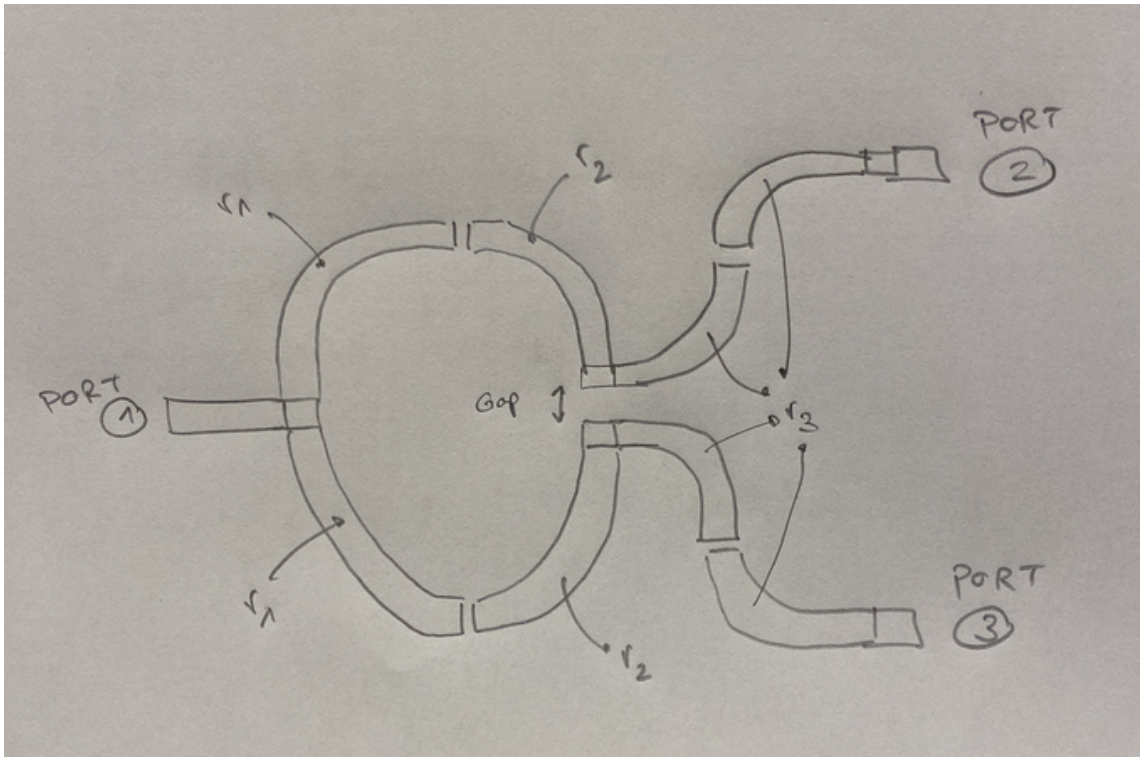


Figure 4.6: Design for the implementation of a Wilkinson with TEE junctions

$$
\begin{aligned}
r_1 &= \frac{1}{2}\left(\frac{\lambda}{2\pi} + \frac{W_{50} + Gap}{2}\right) = \frac{1}{2}\left(\frac{c}{2\pi f\sqrt{\epsilon_r}} + \frac{W_{50} + Gap}{2}\right) \\
&= \frac{1}{2}\left(\frac{3 \cdot 10^8}{2\pi 3 \cdot 10^9\sqrt{6.15}} + \frac{1.85 \cdot 10^{-3} + 1 \cdot 10^{-3}}{2}\right) \\
&= 4.031 \cdot 10^{-3} m = 4.031 mm
\end{aligned}
$$

$$
\begin{aligned}
r_2 &= r_1 - \frac{W_{50} + Gap}{2} \\
&= 4.031 \cdot 10^{-3} - \frac{1.85 \cdot 10^{-3} + 1 \cdot 10^{-3}}{2} \\
&= 2.606 \cdot 10^{-3} m = 2.606 mm
\end{aligned}
$$

Note: the width, $W_{50} = 1.85mm$, we use is the one calculated in Figure 2.7.

And for r_3, we will be using a radius big enough so the amplifier stage fits in the balanced amplifier. For our case we will be using a radium of $r_3 = \lambda/32 = 40.32/32 = 1.26mm$.

In the Figure 4.8, we can see the simulation of the Wilkinson power divider / combiner implemented in microstrip technology (see Figure 4.7 to see the circuit implemented). Here we can observe that the theoretical calculations do not fit the requirement for our working frequency of $f_0 = 3GHz$. Thus we will tune the circuit in order to adapt it for our working frequency using the AWR Tune Tool.

For the circuit tuned, we get slightly different values of $r_1 = 4.45mm$ and $r_2 = 3.35mm$. For this we get the simulation shown in Figure 4.9, we can see that the Wilkinson is working perfectly. This is because the power is divided in half to the two output ports s_{21} and s_{31} and the reflection s_{11} is negligible.

4.1.4. Layout

For the layout, we got the one show in Figure 4.10. One important note is that we added transmission lines at the junction between the input port and the two branches. The length was the one required for the layout to be able to snap together.

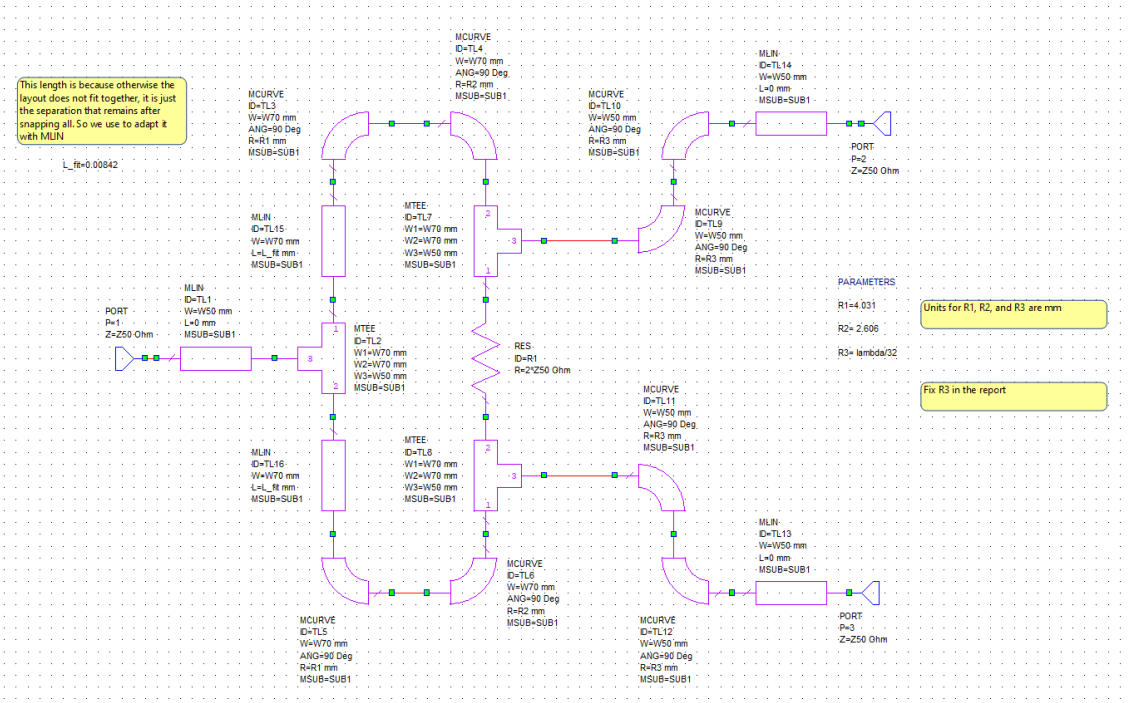


Figure 4.7: Wilkinson power divider / combiner circuit

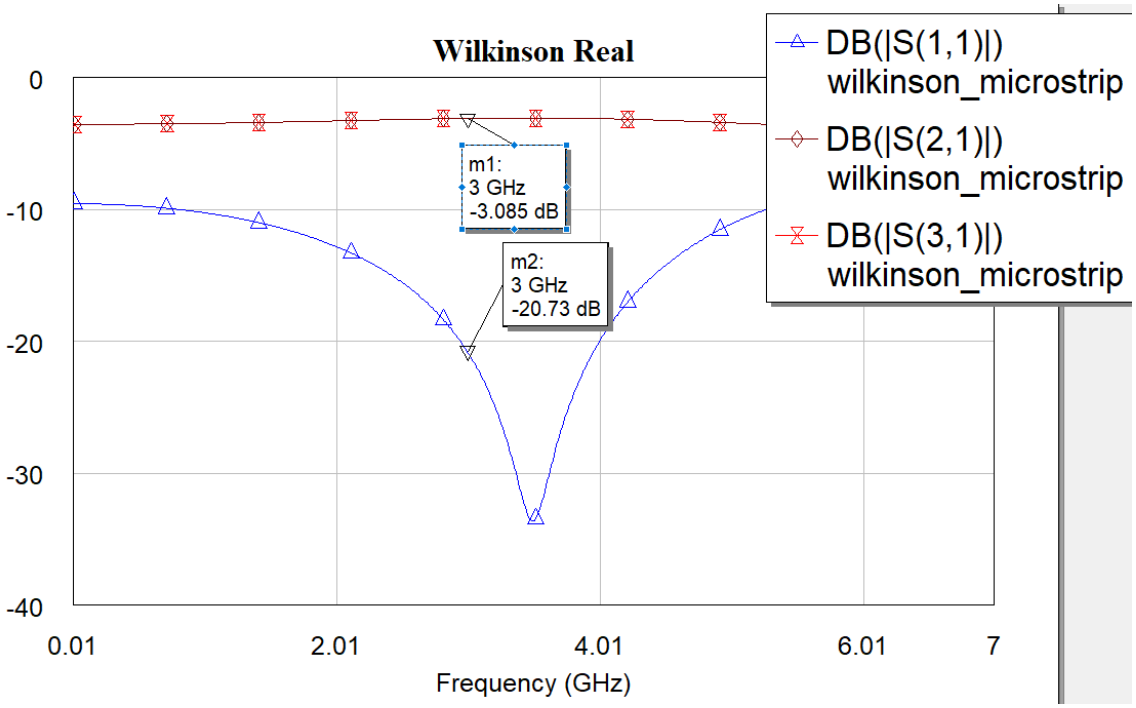


Figure 4.8: Wilkinson power divider / combiner simulation of circuit in Figure 4.7

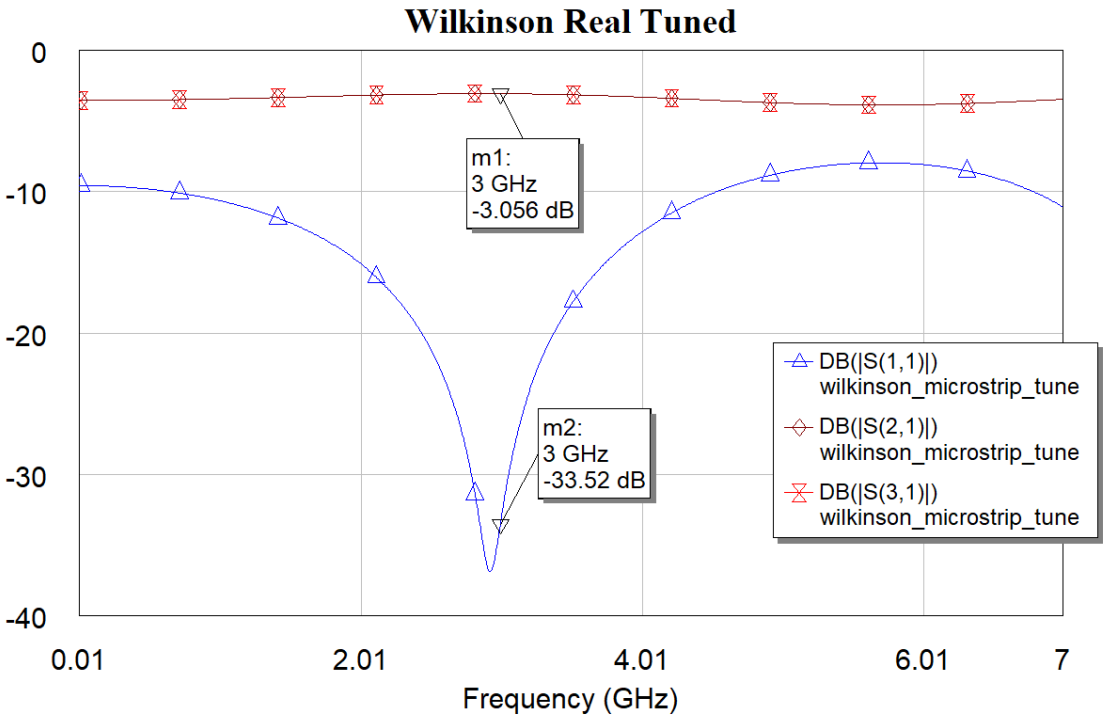


Figure 4.9: Simulation of the Wilkinson power divider / combiner tuned

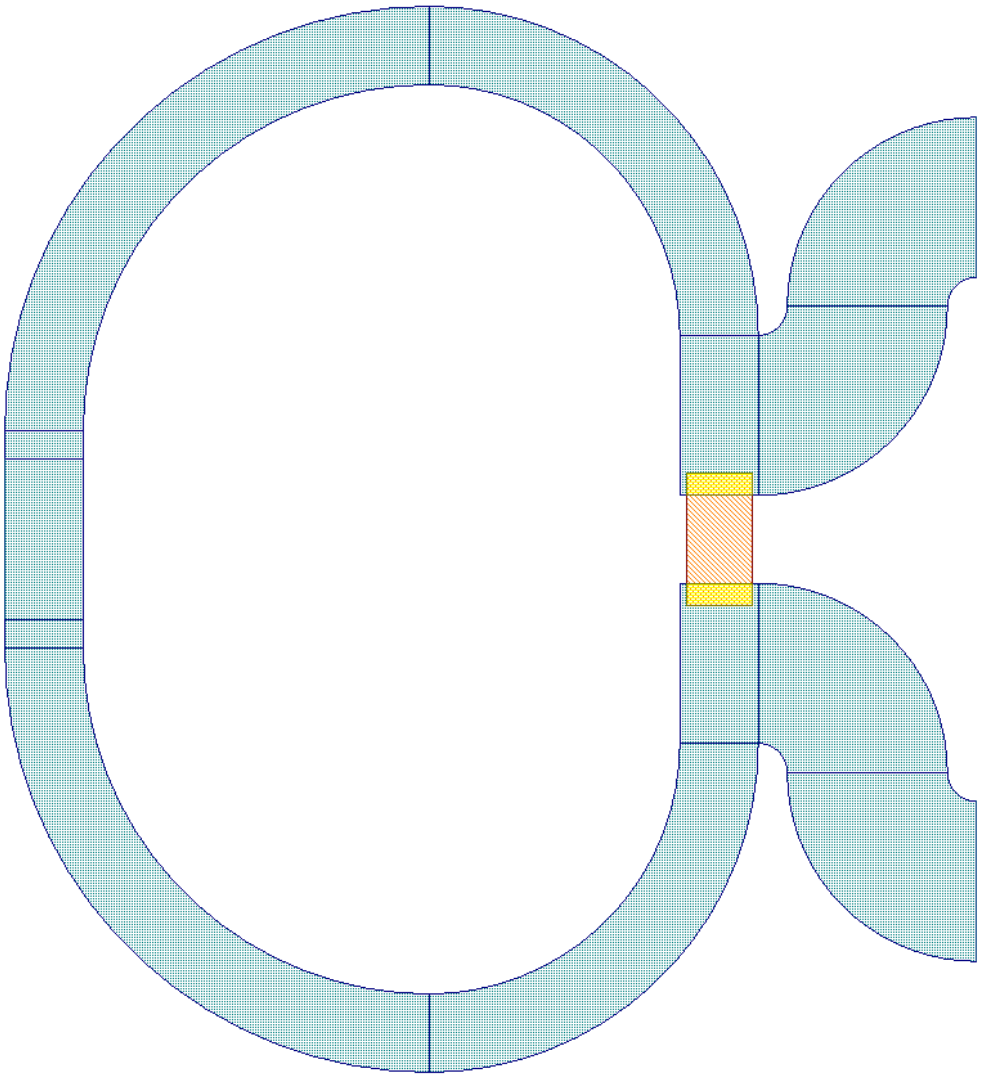


Figure 4.10: Layout of the Wilkinson power divider / combiner

4.2 First Stage: Simple Amplifier

For the simple amplifier, we have implemented the circuit show in Figure 4.11. One thing to take into consideration, is that we have added small segments of transmission lines between the lumped elements so there is space for the layout design to be implemented.

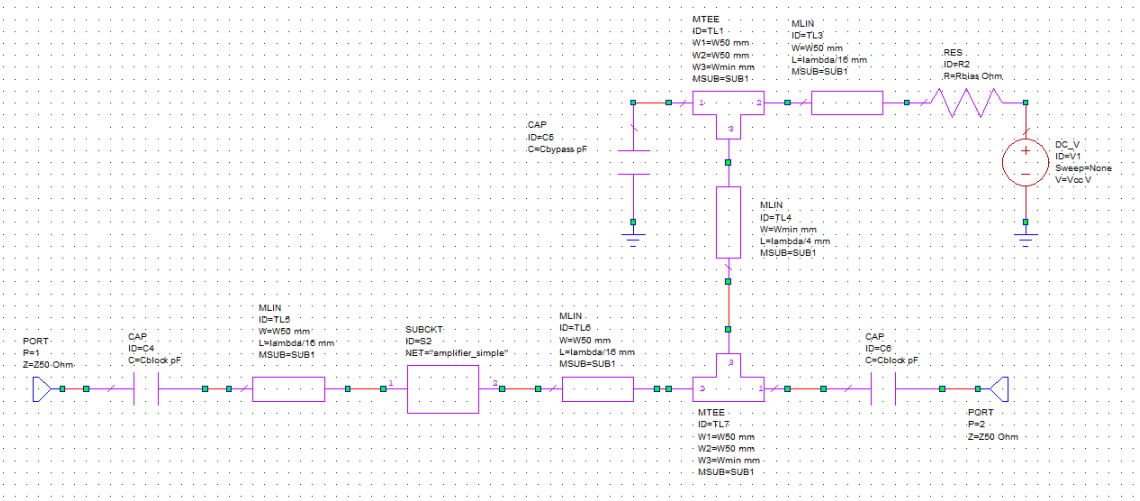


Figure 4.11: Circuit of first stage: simple amplifier

The simulation for this circuit can be shown in Figure 4.12. If we compare it with the data sheet of the amplifier (see Figure 3.10), we can see that they are almost the same.

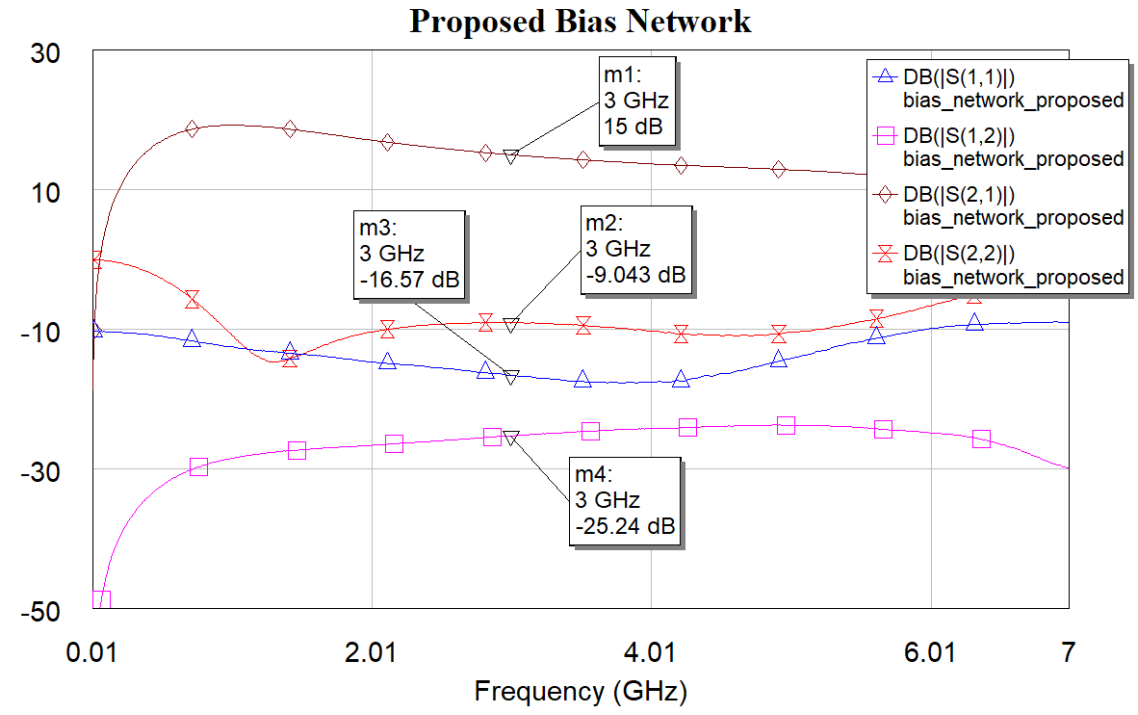


Figure 4.12: Simulation of the first stage: simple amplifier show in Figure 4.11

4.2.1. Layout

Finally, the microstrip layout can be seen in Figure 4.13.

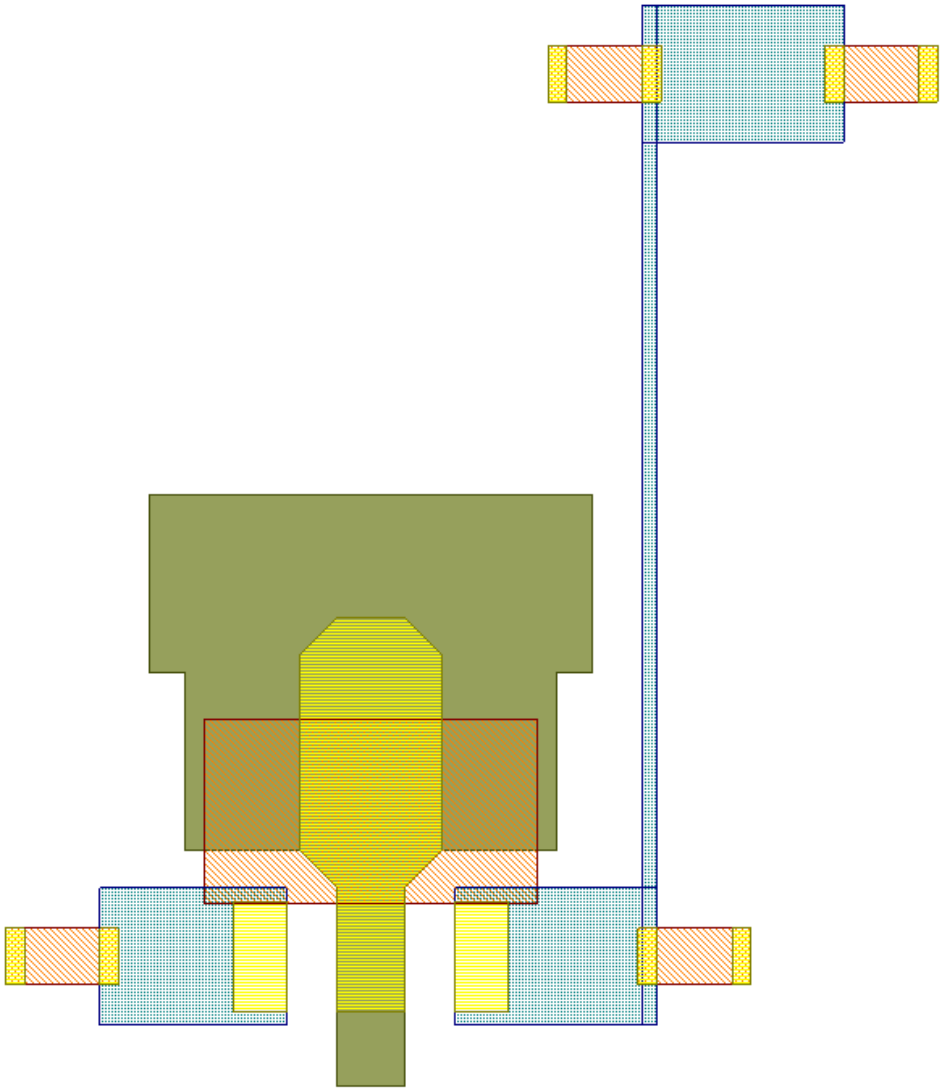


Figure 4.13: Layout of the simple amplifier

4.3 Second Stage: Balanced Amplifier

For the second stage, we have implemented the circuit show in Figure 4.14. Here we have used the previous circuits such as the Wilkinson power divider / combiner and the bias network for the amplifier.

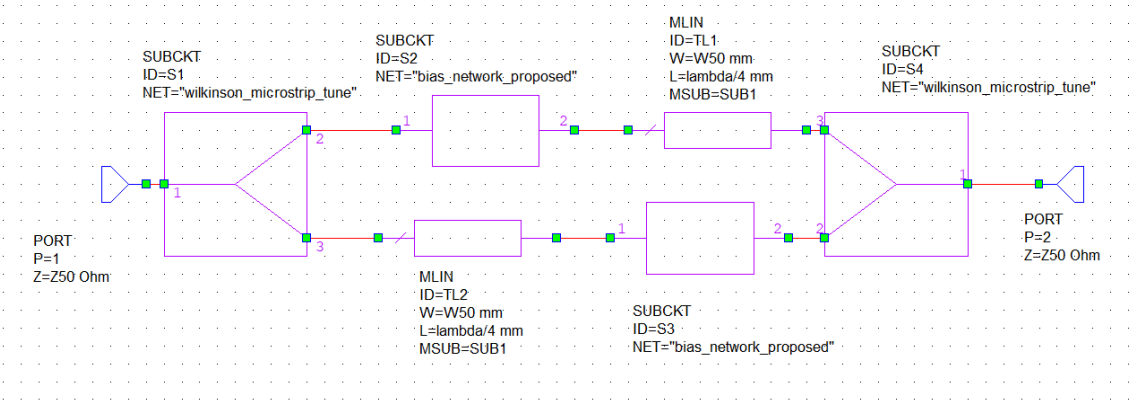


Figure 4.14: Circuit of the balanced amplifier

If we compare the simulation of the balanced amplifier (see Figure 4.15) with the simulation for the simple amplifier (see Figure 4.12); we can see that they have the same gain as calculated previously. However, the isolation of the balanced amplifier is much higher than the simple amplifier (as it has much lower s_{11}, s_{12}, and s_{22}.

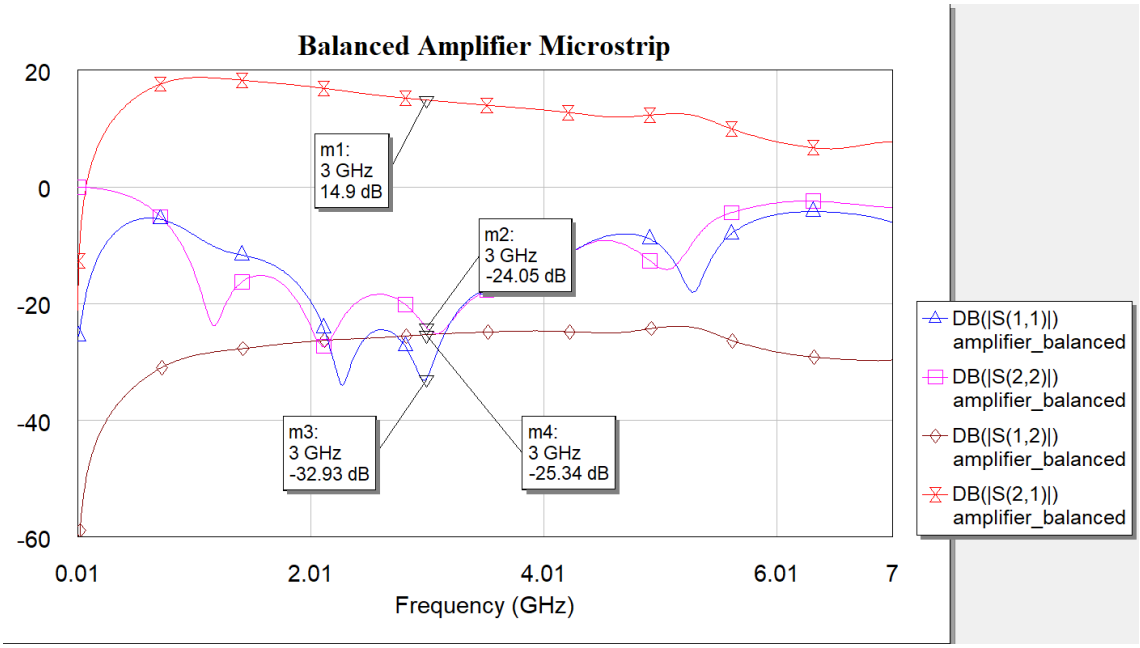


Figure 4.15: Simulation of the balanced amplifier in Figure 4.14

4.3.1. Layout

For the layout, it can be seen in Figure 4.16.

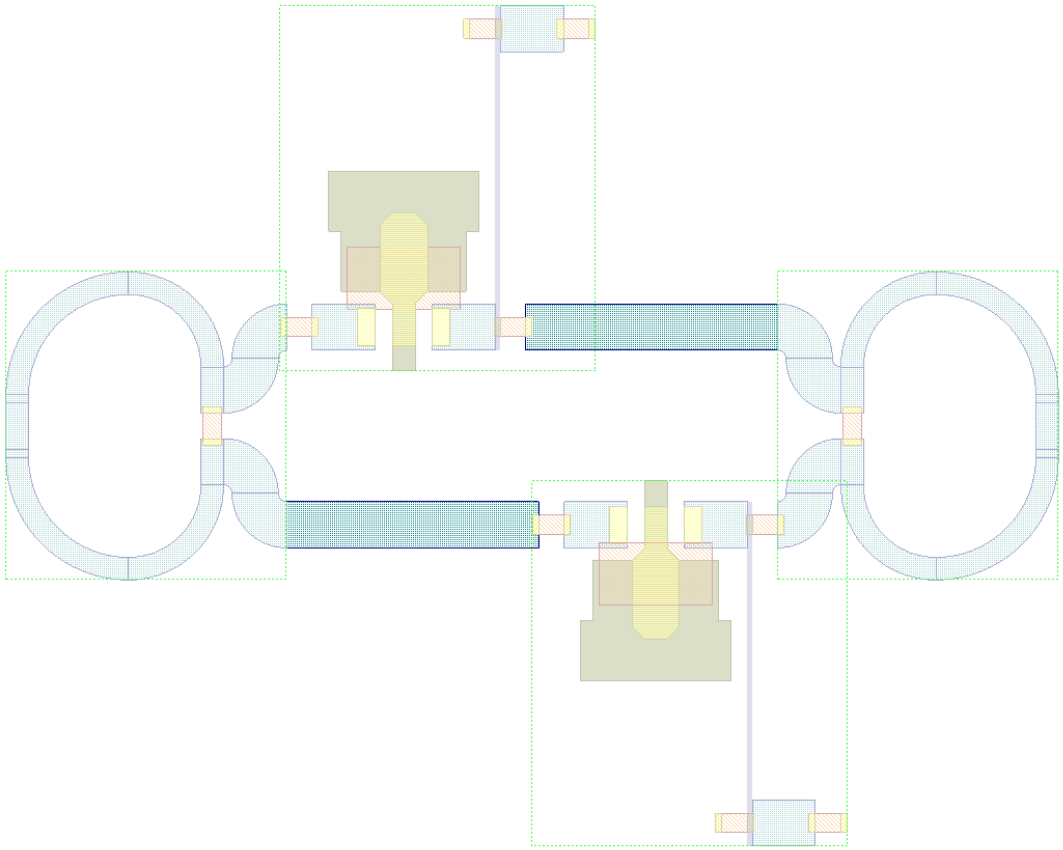


Figure 4.16: Layout of the balanced amplifier of Figure 4.14

4.4 Band Pass Filter

In the band pass filter, in order to design the circuit with microstrip technology, we will need to calculate the parameters of the coupled lines for the microstrip implementation.

4.4.1. Calculations of the length, width, and separation of the coupled lines

In order to calculate the dimensions, we will be using the Coupled Microstrip Analysis /Synthesis Calculator. See Figure 4.17 for the first calculation of the coupled lines.

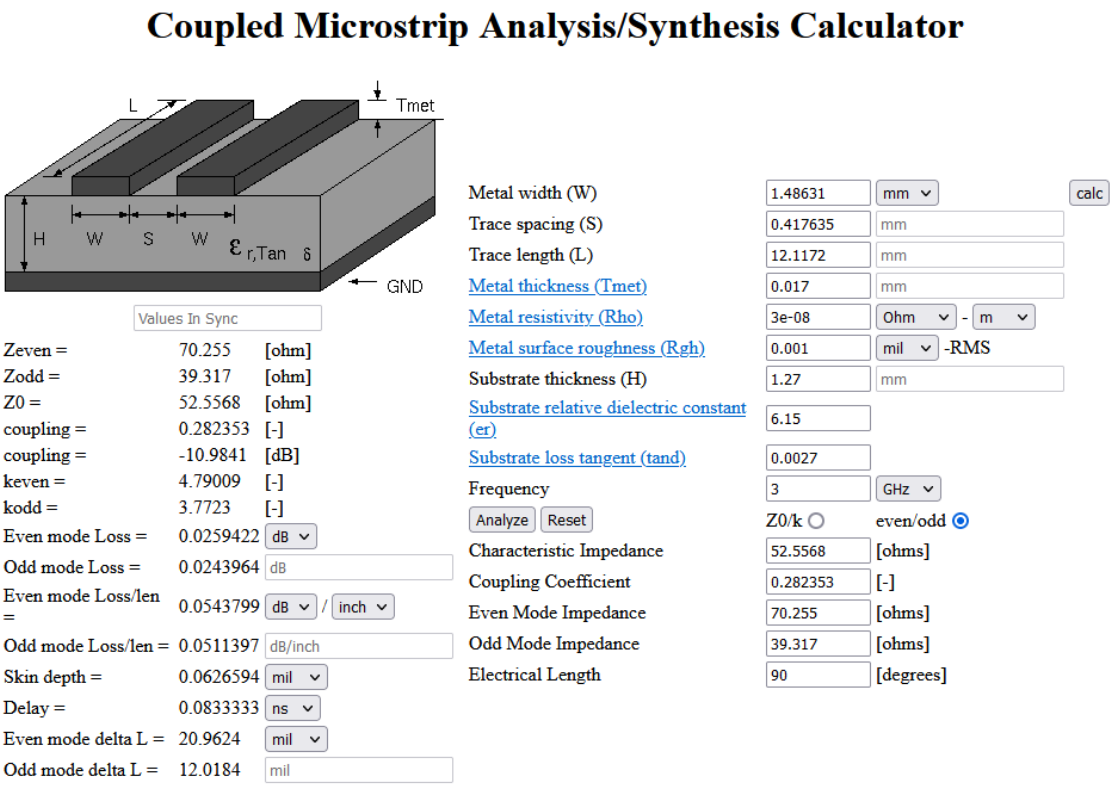


Figure 4.17: Calculator of the microstrip coupled lines for the band pass filter

If we repeat the process for every coupled line, we get the following results:

$$w_1 = 1.48631mm$$
$$s_1 = 0.417635mm$$
$$l_1 = 12.1172mm$$

$$w_2 = 1.84182mm$$
$$s_2 = 2.19832mm$$
$$l_2 = 11.8295mm$$

$$w_3 = 1.85223mm$$
$$s_3 = 2.91747mm$$
$$l_3 = 11.8078mm$$

$$w_4 = 1.85315mm$$
$$s_4 = 3.04061mm$$
$$l_4 = 11.8054mm$$

$$w_5 = 1.85223mm$$
$$s_5 = 2.91747mm$$
$$l_5 = 11.8078mm$$

$$w_6 = 1.84178mm$$
$$s_6 = 2.1981mm$$
$$l_6 = 11.8295mm$$

$$w_7 = 1.48631mm$$
$$s_7 = 0.417635mm$$
$$l_7 = 12.1172mm$$

Where:

w: is the width of the coupled line

h: is the height of the coupled line

s: is the separation of the coupled line

4.4.2. MCLIN implentation

With all the sections calculates, we can implement the circuit in AWR using MCLIN coupled lines (see Figure 4.18). For the simulation shown in Figure 4.19, we can see that the band pass filter is working correctly.

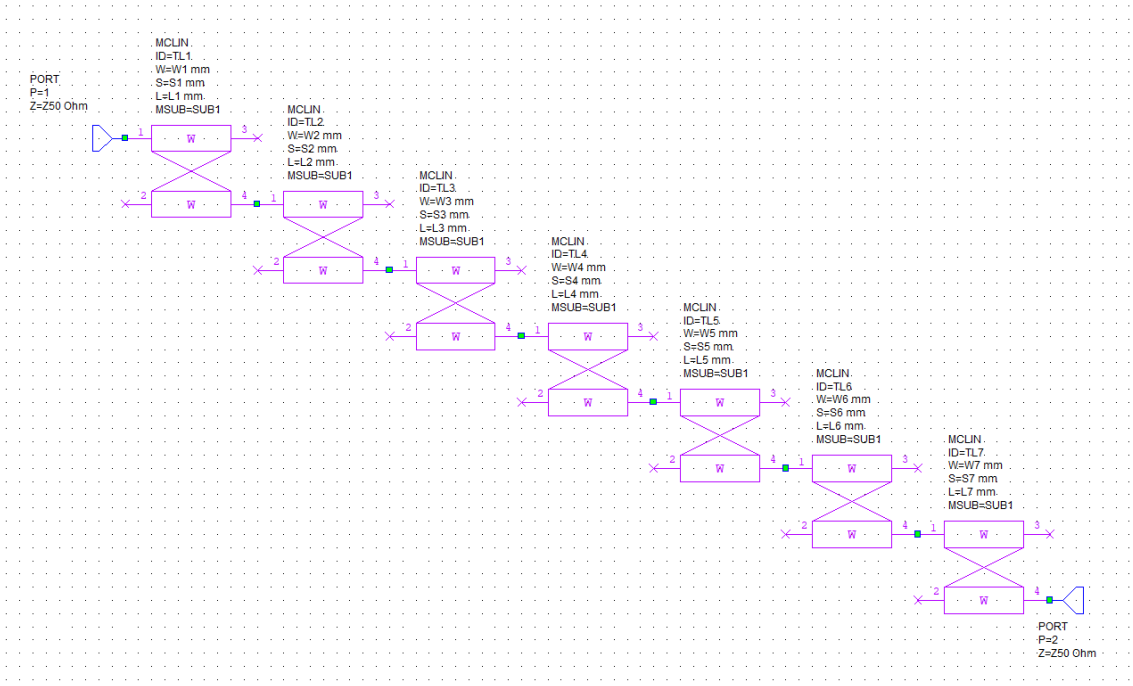


Figure 4.18: Circuit for the band pass filter implemented with MCLIN coupled lines

4.4.3. MCFIL implementation

Now we will implement it with MCFIL lines. In Figure 4.20, we can see the circuit implemented and in Figure 4.21, we can see the simulation. Here we can observe that the center frequency of the filter has been shifted to the left to around $f_0 = 2.9GHz$. This is because the difference in the widths of the coupled lines make the response of the filter shift. So let's fix it by tuning the widths and lengths of the coupled lines.

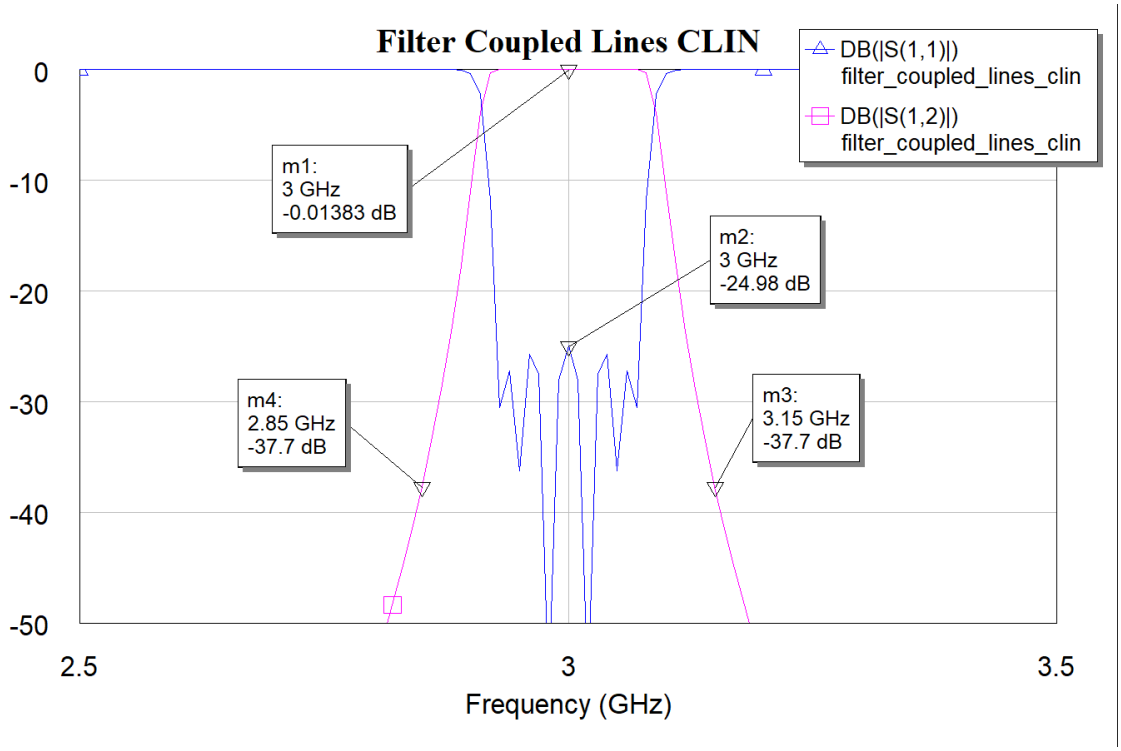


Figure 4.19: Simulation of the band pass filter with MCLIN coupled lines (see Figure 4.18)

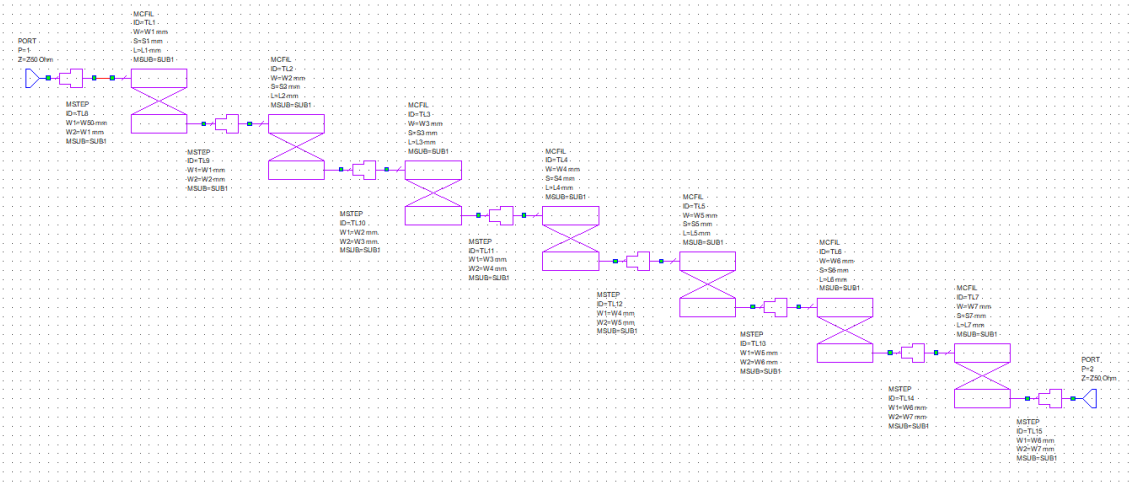


Figure 4.20: Circuit of the band pass filter with MCFIL coupled lines

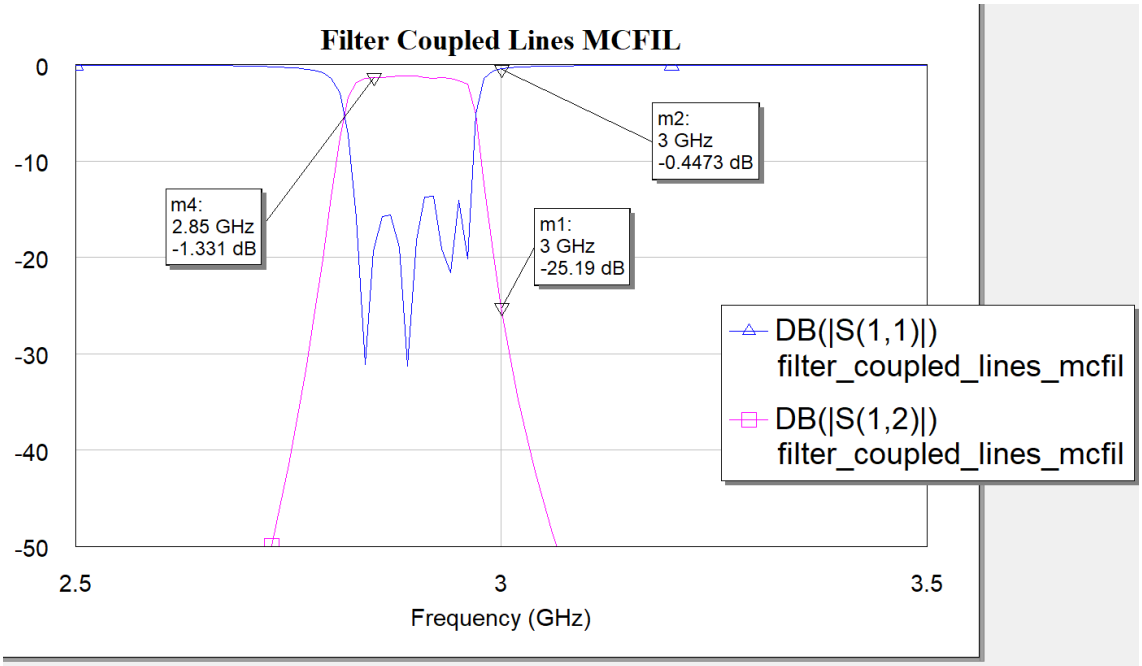


Figure 4.21: Simulation of the band pass filter with MCFIL coupled lines (see Figure 4.20)

4.4.4. MCFIL implementation tuned to our desired characteristics

After some tuning with the AWR Tune Tool, we got the following dimensions for the different coupled lines for the band pass filter:

$$w_1 = 1.3mm$$
$$s_1 = 0.417635mm$$
$$l_1 = 11.6mm$$

$$w_2 = 1.4mm$$
$$s_2 = 2.19832mm$$
$$l_2 = 11.5mm$$

$$w_3 = 1.3mm$$
$$s_3 = 2.91747mm$$
$$l_3 = 11.6mm$$

$$w_4 = 1.4mm$$
$$s_4 = 3.04061mm$$
$$l_4 = 11.5mm$$

$$w_5 = 1.3mm$$
$$s_5 = 2.91747mm$$
$$l_5 = 11.6mm$$

Where:

w: is the width of the coupled line

h: is the height of the coupled line

s: is the separation of the coupled line

For the final circuit, it can be seen in Figure 4.22. Noticed that we have used MSTEP elements in order to adapt the different widths of the coupled lines. And in the simulation (see Figure 4.23), we can see that now the filter is centered at our desired frequency of $f_0 = 3GHz$. However, the attenuation at the pass band is a little bit lower than desired, but we where not able to get an attenuation lower than 20 dB.

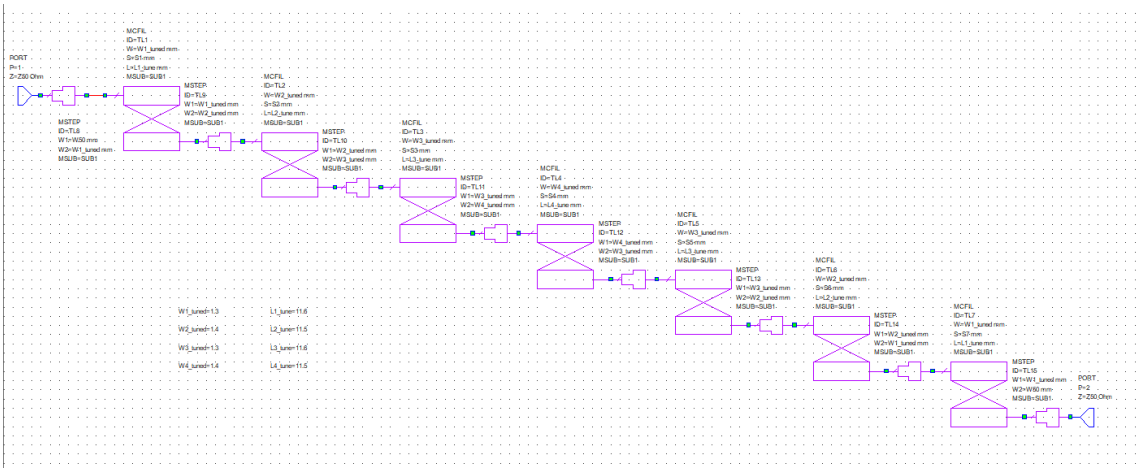


Figure 4.22: Circuit for the final band pass filter with MCFIL coupled lines

4.4.5. Layout

For the layout of the band pass filter, it can be seen in Figure .

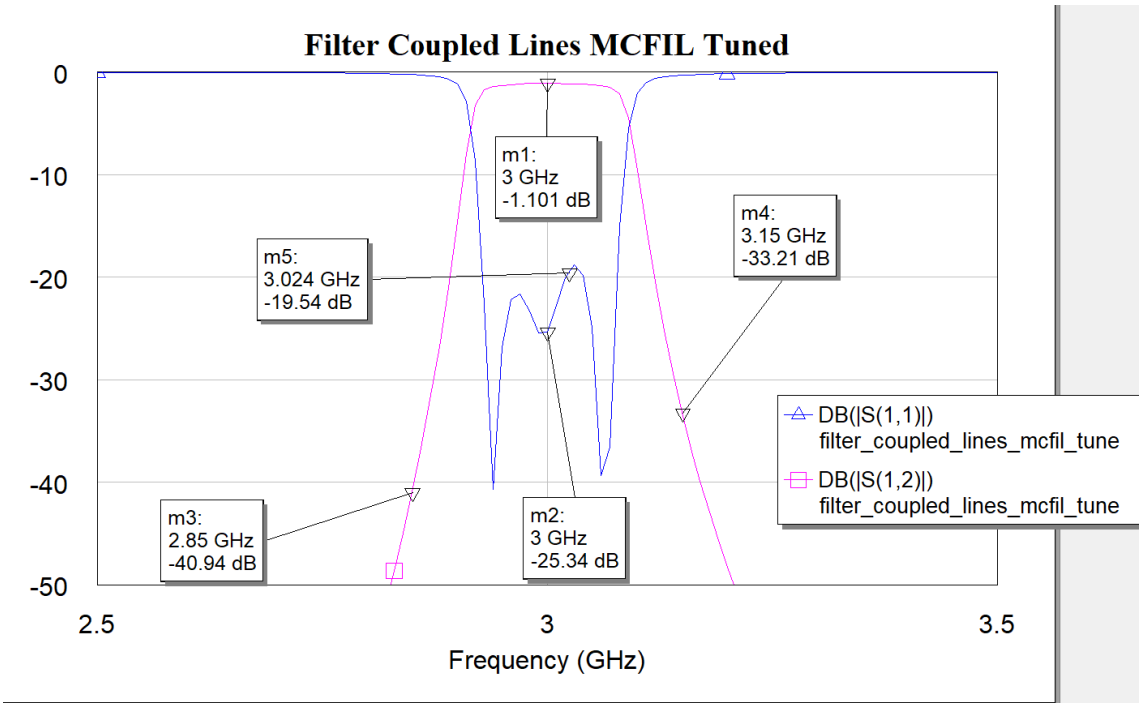


Figure 4.23: Simulation for the final band pass filter of Figure 4.22

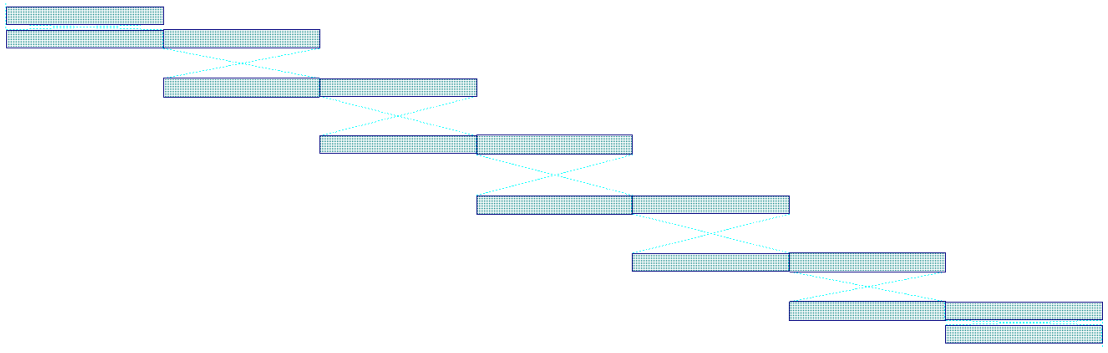


Figure 4.24: Layout of the final band pass filter of Figure 4.22

4.5 Directional Coupler

For the directional coupler, in order to adapt the ideal directional coupler of Figure 3.20, we need to calculate the parameters of the microstrip line.

4.5.1. Calculation of the length, width, and separation of the coupled microstrip lines

In order to calculate the, we used the Tunner Tool of AWR where we modified the length (L), width (W), and separation (S) until we got a coupling of $C = 20\ dB$ and a reflected power of as low as possible. For this simulation we have used the circuit pictured in Figure 4.25. Notice that the elements on the coupled port are just to be able to be implemented in the microstrip technology to have space in the PCB to place the elements.

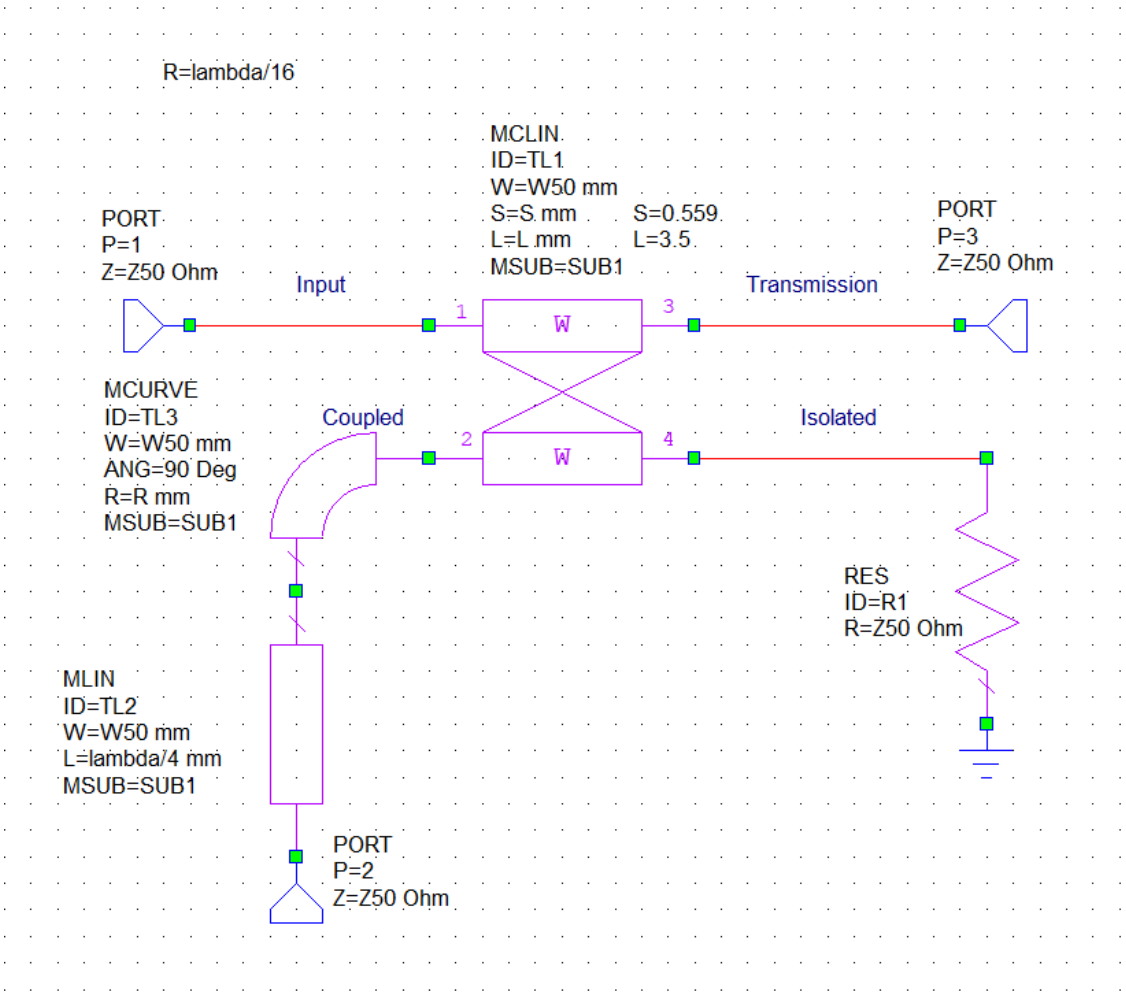


Figure 4.25: Circuit of the final directional coupler implementation

The simulation can be seen in the Figure 4.26. Here we can observer that the microstrip implementation is as good as the ideal implementation (see Figure 3.21).

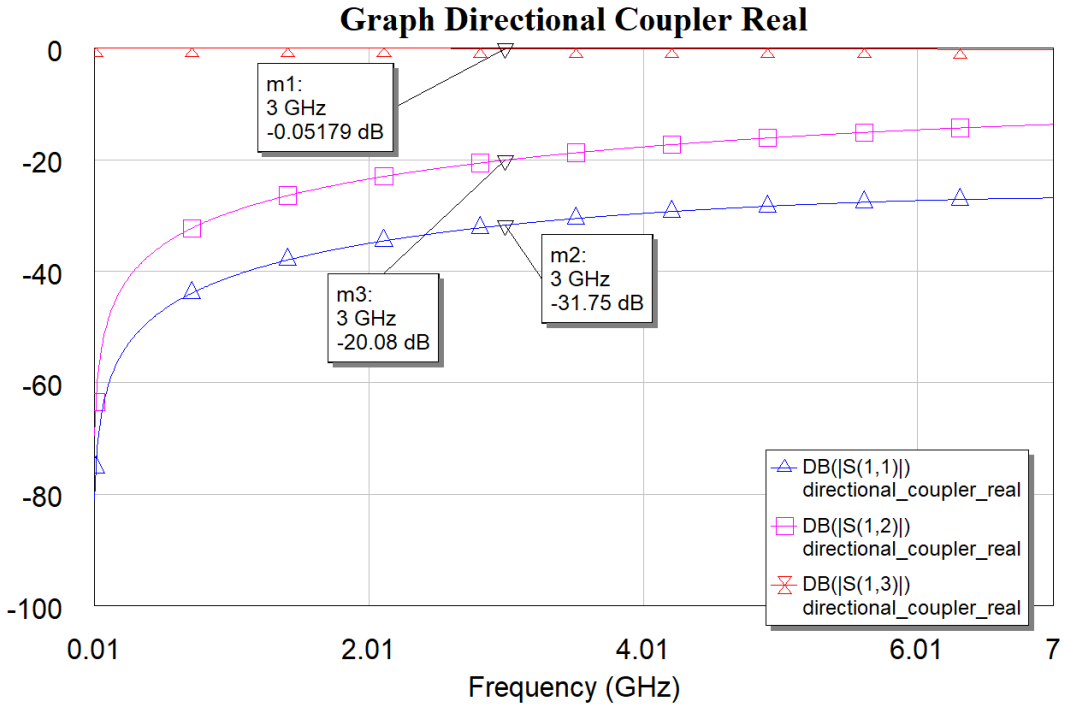


Figure 4.26: Simulation of the directional coupler shown in Figure 4.25

4.5.2. Layout

For the layout, it can be seen in Figure 4.27.

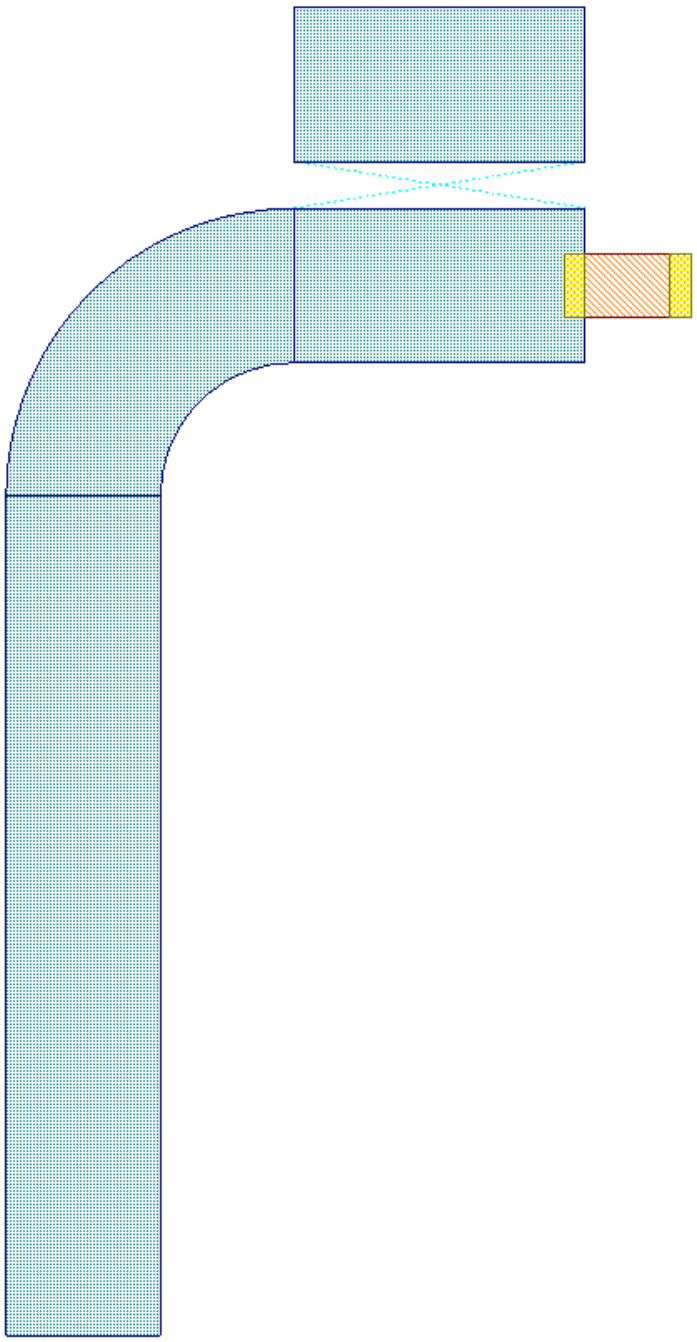


Figure 4.27: Layout of the directional coupler shown in Figure 4.25

Chapter 5

Integration

5.1 Common Microstrip Layout

The full circuit implementation can be seen in Figure 5.1 and the layout can be seen in Figure 5.2. One thing to take into consideration is that we have added TLs at the end of the ports in order to give some room in the PCB to solder the elements. And also, we did not need to add any matching elements as the circuits where matched to a characteristic impedance of $Z_0 = 50\Omega$, thus not needing any further matching.

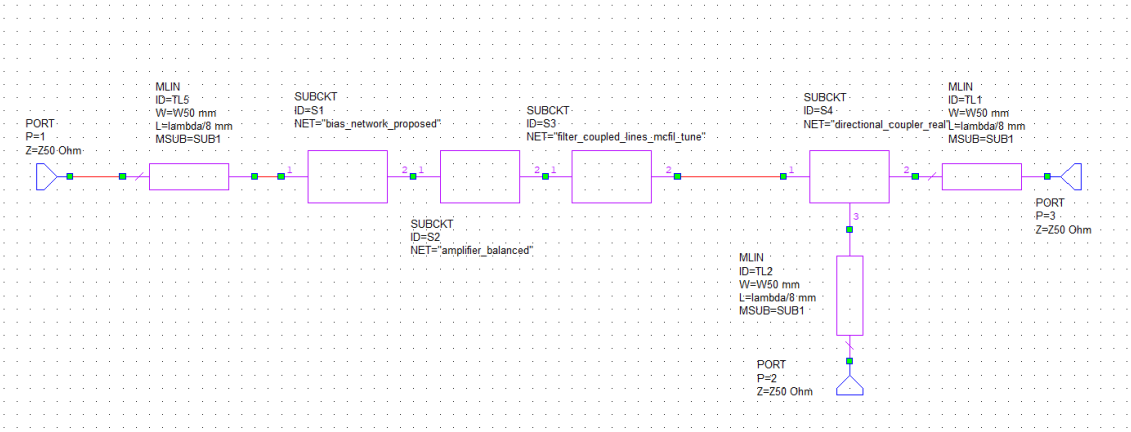


Figure 5.1: Full circuit schematics

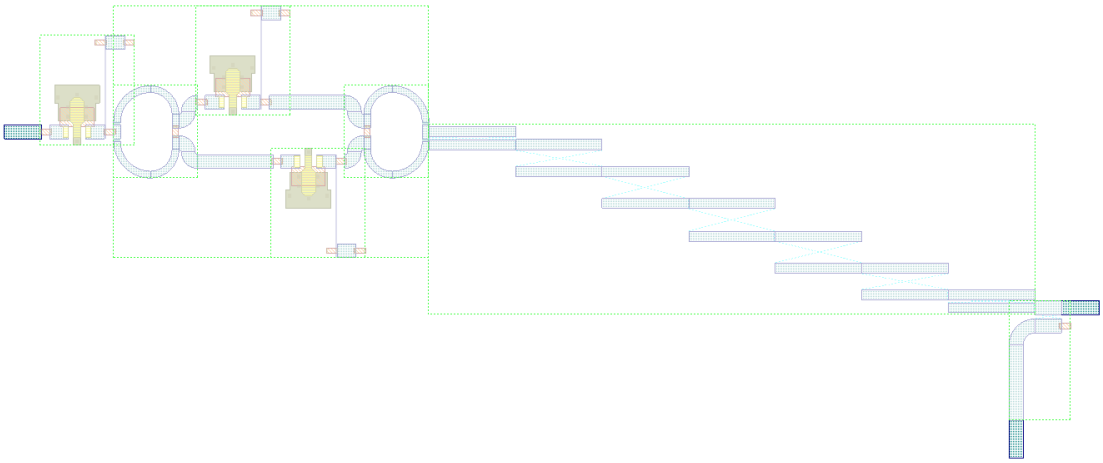


Figure 5.2: Layout of the complete circuit of Figure 5.1

5.2 Simulation of the Full Network at Working Frequencies

In the Figure 5.3, we can observe the response of our circuit at the working frequencies. Here we can observe that the 2 stage amplifier works at the desired pass band with a gain of $G = 28.71dB$ and an attenuation almost negligible. On the other hand, at the other frequencies, the filter does not allow any frequency through.

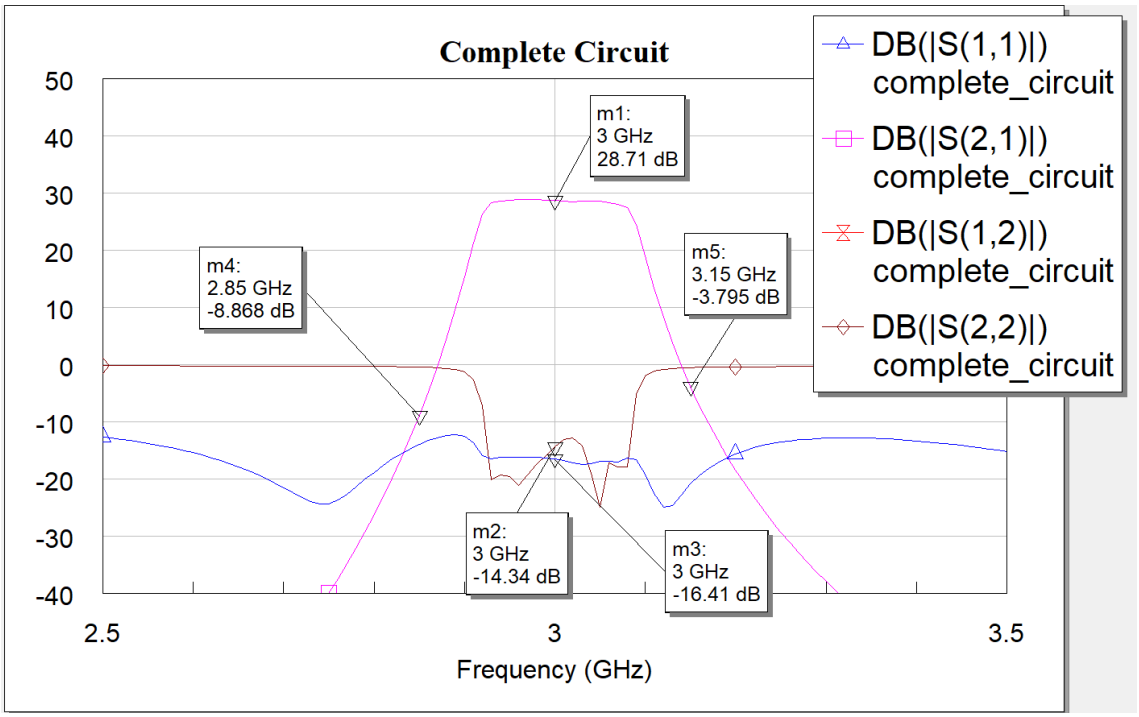


Figure 5.3: Simulation of the full circuit of Figure 5.1 at working frequencies.

5.3 Simulation of the Full Network Wide band Response (0GHz up to 7GHz)

For the full response of our circuit, it can be seen in Figure 5.4. Here we can see that the circuit works at expected as it only allows the desired frequency. However, at $f = 6GHz$, the filter allows the signal to be amplified. This is because the filter we have implemented has resonant frequencies and this is one of them.

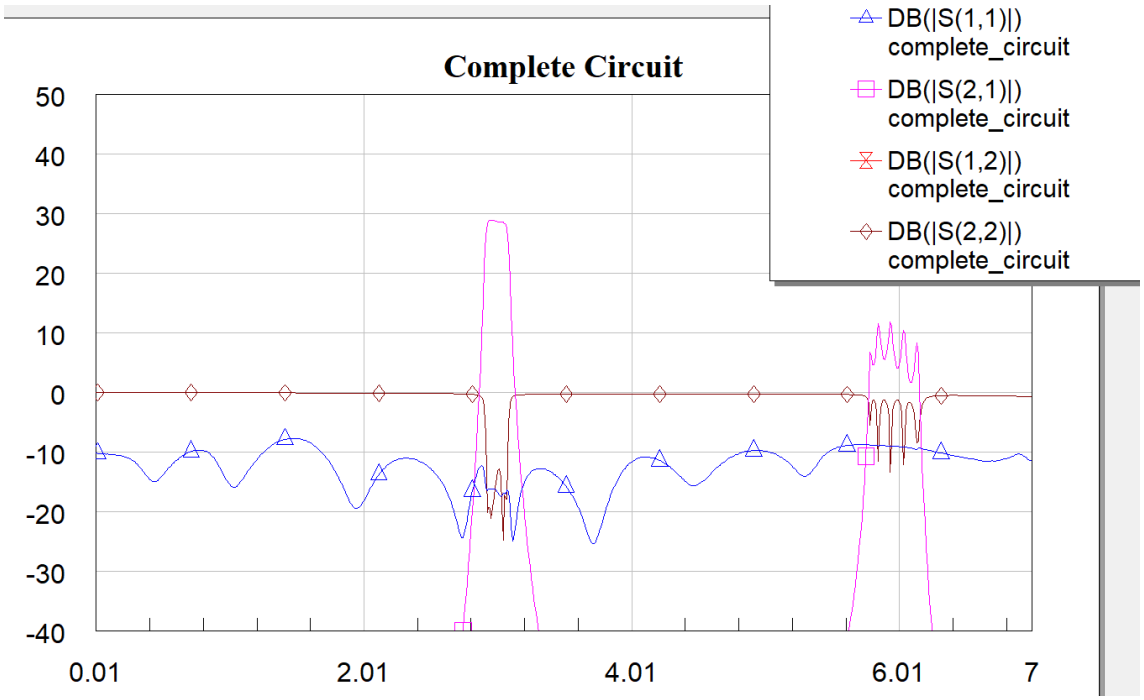


Figure 5.4: Simulation of the full circuit of Figure 5.1 at the full range of frequencies

Chapter 6

Results and Conclusions

6.1 Comparison of the System Specifications with the Simulated Results

For the final results we will comparing the simulated results to the requirements for the circuit. We will use the simulation in Figure 6.1 to make the comparisons.

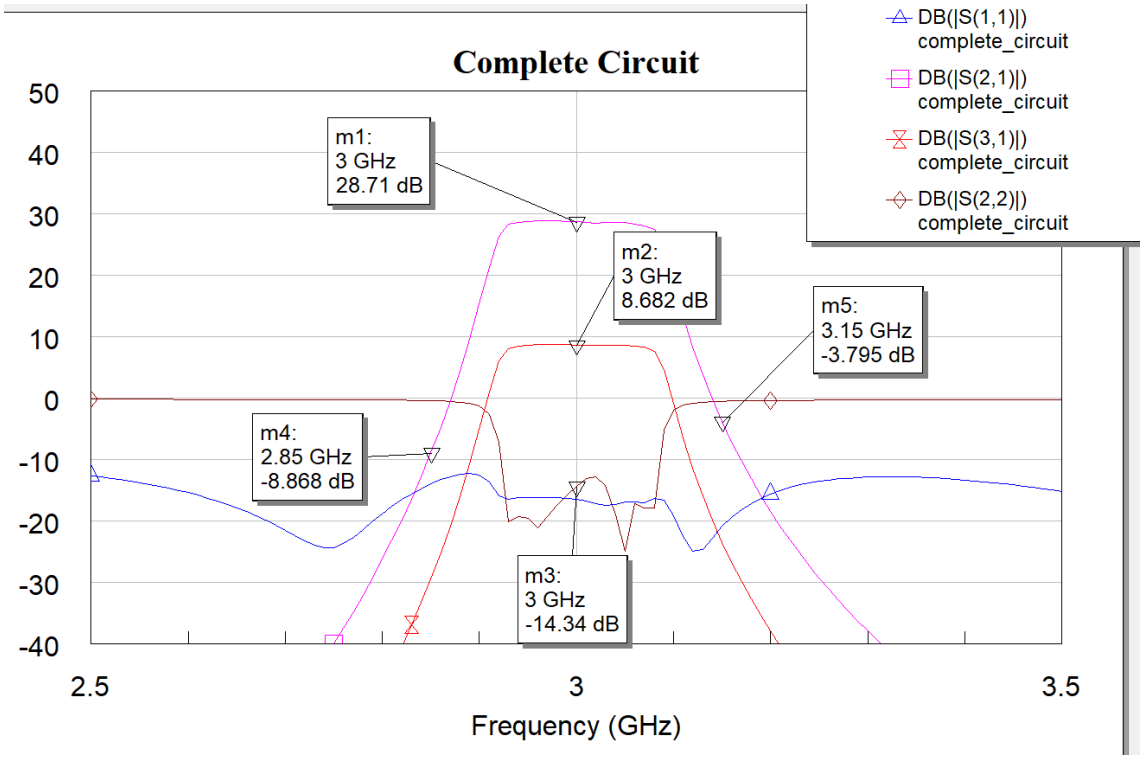


Figure 6.1: Simulation of the final circuit with interesting markers

- We can see that the centered frequency $f_0 = 3GHz$ is the same as the requirements.
- For the bandwidth, in the simulation we can see that it goes from $2.925GHz$ to $3.075GHz$; which is the same as the specifications stated.
- For the gain of the amplifier, we get the same results calculated previously of $28dB$.
- The return loss at the input port of our circuit is $15dB$ which does not pass the requirements of $30dB$. However, after trying to tune the filter and coupled lines we were not able to achieve any higher return loss at the input port.
- For the return loss at the output port, we get $16dB$ which is close to the requirement of $18dB$. We were able to increase the return loss by tuning the circuit but not to get the required return loss.
- For the attenuation outside the pass band, we get an attenuation much lower than 25 dB that were required.

- Finally, for the power at the monitor, we get exactly 20 dB lower to the main output port.

6.2 Conclusions

The design and characterization of a two-stage, balanced microwave amplifier represent a significant achievement in the field of high-frequency technologies. Through theoretical analysis and practical implementation, we have successfully met the objectives outlined in this laboratory exercise. Our design approach was guided by the need to overcome inherent limitations of amplifiers, focusing on maximizing gain while ensuring efficient power utilization.

The first stage of our amplifier utilized a commercial integrated amplifier, GVA-83+, configured as a simple amplifier. By leveraging data provided by the manufacturer and implementing bias and DC block networks, we ensured proper operation within specified parameters. Additionally, the balanced second stage, featuring phase shifters and Wilkinson power dividers/combiners, enabled enhanced performance and power distribution. Through careful design and simulation, we achieved the desired specifications, including a center frequency within the desired range, high gain, and effective suppression of out-of-band frequencies.

Furthermore, our design process involved the meticulous design and integration of other crucial components such as the band pass filter and directional coupler. These elements, designed with microstrip technology, contributed to the overall functionality and performance of the amplifier. Our comprehensive approach, from theoretical analysis to practical implementation and simulation, has resulted in a robust and efficient microwave amplifier design. However, further optimization and refinement may be warranted to address any discrepancies between simulated and desired specifications, ensuring the amplifier meets the highest standards of performance and reliability in real-world applications.