Final lab exercise

Design of a two-stage, balanced amplifier

March 29, 2024

The goal of this lab exercise is the design and characterization of a microwave amplifier, whose main component is a commercial, integrated wideband amplifier. This integrated circuit is encapsulated as a SMD (Surface Mount Device), also known as SMT (Surface Mount Technology), and therefore is easily compatible with the microstrip technology, that will be used for the design.

Two fundamental limitations of any amplifier, including the commercial device used in the exercise, are the maximum power that can be provided at the output, and the gain (that is, the ratio between the output and input powers). In order to overcome both limitations, the design will use certain techniques:

- The full circuit is composed of two stages, connected in cascade. Therefore, it is possible to reach a gain close to the product of the gains of each stage (using logarithmic units, their sum).
- Due to this two-stage configuration, the power level at the second stage is higher, and therefore the power limitation will be restricted to this stage. In order to increase the maximum achievable power, the stage splits the signal in two equal parts, that are independently amplified by two separated amplifiers. Both signals are then recombined, duplicating the maximum power at the output (at least ideally). This type of structure with two amplifying branches is called balanced amplifier. The basic structure, composed of two single amplifiers and two power dividers/combiners, is shown in Figure 1.

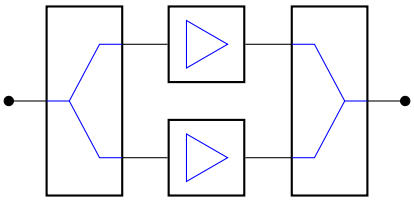


Figure 1: Basic diagram of a balanced amplifier.

The circuit to be designed must operate for frequency components inside certain band around a center frequency. Additionally, it is required to limit the power of frequency components that are outside this band, in order to avoid interferences. This frequency selective behaviour can be implemented by including a band pass filter, at the output of the second amplifying stage.

Finally, it is necessary to monitor at any time the output signal of the full circuit, in order to check its correct operation. For this, a coupler is included at the circuit output, that extracts a small sample of the output signal, and presents it at an auxiliar output port.

With all the elements described above, the full diagram of the amplifier is shown in Figure 2.

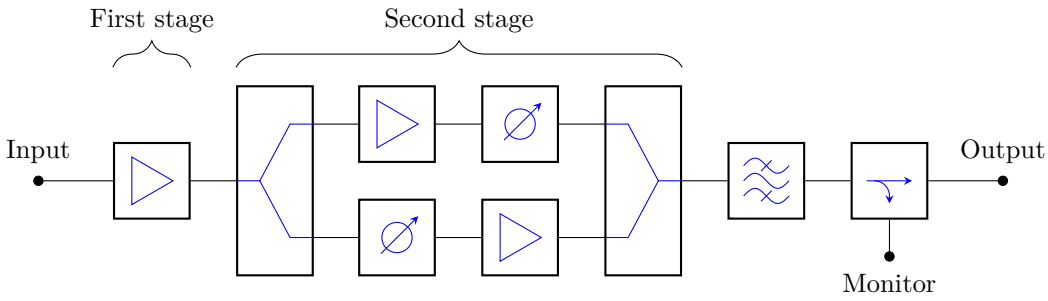


Figure 2: Diagram of the complete amplifier.

1 Design of the circuit elements

This section describes the particular aspects of the characterization and design of each of the elements that form the full circuit. The preparatory work, that should be solved before the practical exercise, is also included (it is marked as text in color).

1.1 First stage: simple amplifier

The first amplifying stage is composed of only one integrated circuit. The integrated amplifier model used in this exercise is GVA-83+, manufacture by Mini-Circuits[1]. Since this course does not study how amplifiers work, it will be used as a black box, recurring to the information and data provided by the vendor. In particular, the following files are available:

1. Device data sheet (`GVA83+.pdf`).
2. Measurements for different electrical and thermal conditions (`GVA83+_VIEW.pdf`).
3. S parameters in terms of the frequency, in a standard file format, compatible with AWR (`GVA83_UNIT1.s2p`).
4. Library with the graphical definition of the device layout (`GVA83.gds`).
5. An example of how the device is mounted in a circuit (`WTB-410-83+_P02.pdf`).

Use these documents, especially the data sheet, whenever you consider necessary.

Device format and circuit mounting

The physical casing of the device follows the SOT-89 standard (see Figure 3). The three metallic pins are the input, output and ground connections. The ground pin is bigger, and should (must) be soldered at both sides of the device, or even at its bottom face,

[1]Link: https://www.minicircuits.com/WebStore/dashboard.html?model=GVA-83%2B

that is exposed, in order to ensure good connection, both electrical and thermal (the power lost due to the amplifier inefficiencies is dissipated as heat, and may damage the device if not taken into account).

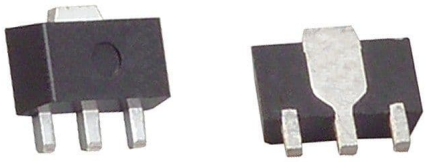
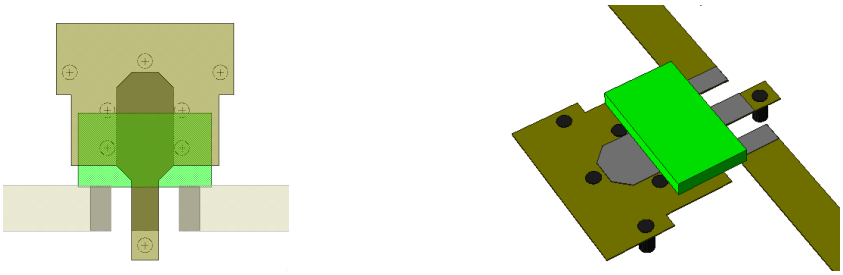


Figure 3: Integrated circuit with SOT-89 casing (top and bottom views).

As shown in Figure 4, when mounted in a microstrip structure, a good connection between the SOT-89 ground pad and the ground plane must be ensured by means of several metallized drilled holes (known as *via holes*, or simply, *vias*) across the dielectric substrate. The design recommended by the vendor[2] is included in the library `GVA83.gds`[3]. The input and output pins are directly soldered to the corresponding microstrip lines.



(a) Layout. (b) Vista en 3D.

Figure 4: Montaje del amplificador en *microstrip* (modelo de AWR).

Bias and block networks

As every amplifier, the GVA83+ must be biased in order to operate, that is, a DC power must be provided, ensuring certain DC voltage and current at some of its pins. The vendor recommends the use of the bias network in Figure 5, that imposes some bias conditions ((${V_d}$ and ${I_{\text{bias}}}$) at the output pin, by means of a voltage source ${V_{cc}} = 5\,\text{V}$ and a resistor ${R_{\text{bias}}} = 7.5\ \Omega$.

The bias network also includes the following elements:

- Two DC block capacitors (${C_{\text{block}}}$), with the purpose of avoiding the bias voltage to reach other external elements, and viceversa, preventing other bias voltages to reach this device. It must be similar to a short circuit at the operation microwave frequencies. The vendor recommends ${C_{\text{block}}} = 2.4\,\text{nF}$ to cover the GVA83+ full band of operation.

[2]Link: https://www.minicircuits.com/pcb/98-pl255.pdf

[3]Import it in AWR with `Project > Add Layout Library > Import GDSII Library...` Once imported, the library will be available in the `Layout` tab of the lateral panel, and you may assign it to an element from its properties dialog, in the `Layout` tab.

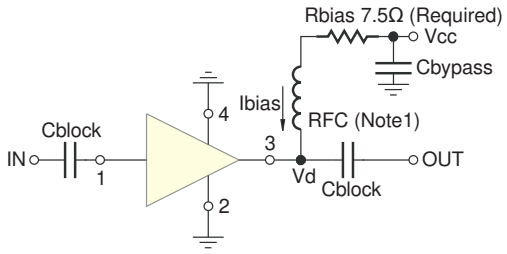


Figure 5: Bias network recommended by the vendor (wideband).

- The bypass capacitor (C_{bypass}), whose purpose is to isolate the DC bias source from the RF signal (or noise). In practice, it is very important since the DC source may be shared by many elements, and without the provided isolation spurious feedback may appear.
- The radio frequency choke (RFC, *RF choke*), that is an inductor.

The RF choke is a problematic element, due to its size[4], cost and high-frequency performance, but it is essential for the response to be wideband. However, when the response is band limited (as it is the case of our design), it can be substituted by a transmission line section, if the other elements are reorganized as shown in Figure 6.

1. Analyze the bias vendor's bias network at $f = 0\,\text{GHz}$ (DC) and at the design frequency. Take into account that the capacitances are high enough to guarantee that at the design frequency they behave almost like a short circuit. On the other hand, the RF choke inductance is also high enough to guarantee that at the same frequency it behaves like an open circuit.
2. Analyze the bias network with the transmission line, both at DC and the operation frequency. Determine the length of the transmission line so that the behaviour of this network is the same than the vendor's one.
3. Perform a wideband simulation (from DC up to 7 GHz) of the vendor's bias network, with the element values it provides ($C_{\text{block}} = 2.4\,\text{nF}$, $C_{\text{bypass}} = 100\,\text{nF}$, $L_{\text{RFC}} \geq 1\,\mu\text{H}$).
4. Perform a wideband simulation of the proposed bias network, comparing with the other one. Modify the characteristic impedance of the transmission line, and justify why it is interesting to use a characteristic impedance as high as possible.

Device response

The GVA-83+ device is a wideband amplifier that, as specified by the vendor, works at frequencies from 0 GHz (DC) up to 7 GHz. With the power level restrictions specified by the vendor, it can be considered a two-port linear device, and therefore its response can be described using a scattering matrix.

[4]Identify each element of the bias network in https://www.minicircuits.com/pcb/WTB-410-83+_P02.pdf.

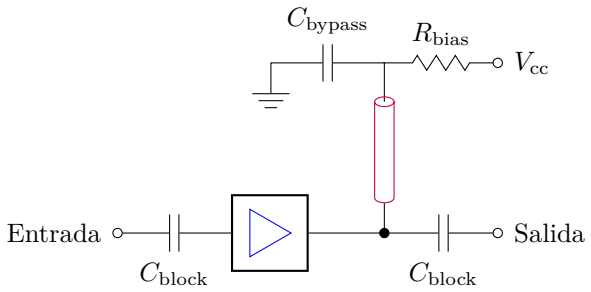


Figure 6: Bias network with transmission line (band pass).

1. Determine the scattering parameters of the device at your design center frequency from the provided data sheets, for the nominal temperature and bias conditions ($V_{cc} = 5\,\text{V}$, $R_{\text{bias}} = 7.5\ \Omega$).
2. Estimate the gain of each amplifier stage, and the gain of the full two-stage network.
3. Using AWR and the S parameters file (`GVA83_UNIT1.s2p`)[5], represent the wide-band S parameters (from 0 GHz up to 7 GHz), and verify if the result agrees with the one from the first question.

1.2 Second stage: balanced amplifier

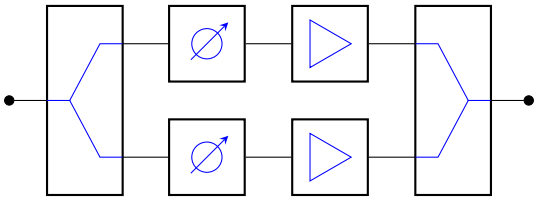
The performance of the basic balanced structure from Figure 1 can be improved if some phase shift is applied at the signals in each branch. Specifically, you must study the three possible alternatives shown in Figure 7.

1. Compute the S matrix of the structure with phase shifters at the input of each branch (figura 7a). To do so, consider a generic S matrix for each amplifier, and reciprocal, ideal phase shifters with an arbitrary phase ϕ.

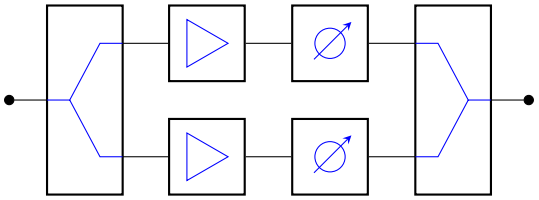
   Also consider ideal Wilkinson combiners/dividers. Of course, both the amplifiers and the phase shifters are identical, and the reference impedance is always Z_0.

2. Compute the S matrix of the structure with phase shifters at the output of each branch (figura 7b).
3. Compute the S matrix of the structure with one phase shifter at the input of a branch, and the other at the output of the other one (figura 7c).
4. Compare the transmission coefficients and, especially, the reflection coefficients of the three networks, and also of the simple amplifier. Prove with this that the performance of the network in Figure 7c is better, for certain phase shift ϕ.

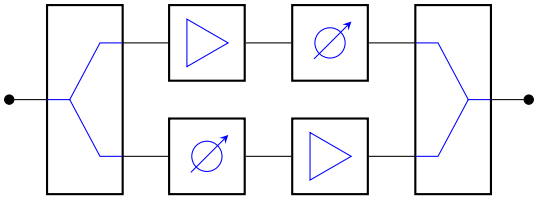
[5] Load it in AWR with `Project > Add Data File > Import Data File...` Once imported, you may examine it in the `Project` tab, and it will be available as a new circuit element in the `Elements` tab, category `Circuit Elements > Subcircuits`, that can be used as any other two port element.



(a) Phase shifters at the input.



(b) Phase shifters at the output.



(c) One phase shifter at each location.

Figure 7: Possible configurations of the balanced stage.

5. Compute the optimal ϕ phase shift.

6. Compute the relationship between the output power of each amplifier that are integrated in the branches of the balanced stage, and the total power at the output of the full balanced stage.

1.3 Band pass filter

The band pass filter design is a conventional structure, based on coupled lines, as the example shown in Figure 8). As the other elements, it will be implemented in microstrip technology, on the common dielectric substrate. Its response must follow a Chebyshev approximation, with the order, bandwidth and in-band return loss required to fulfill the specifications of the full design.

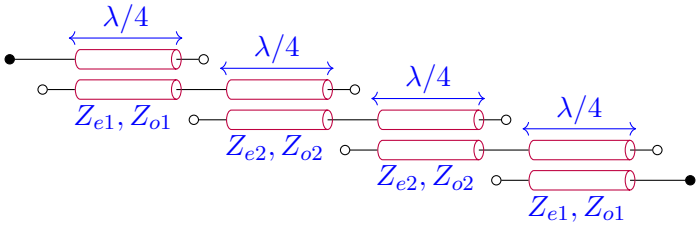


Figure 8: Coupled-line band pass filter (order 3, with four sections).

As a reminder, the design steps for the design of this type of filters are the following ones:

1. Determine the filter order from the bandwidth, in-band return loss and the minimum attenuation at the stop bands.
2. Determine the parameters of the frequency and impedance transforms. Remember that the frequency parameters for a band pass filter are ω_0 (center pulsation) and B (bandwidth). Take into account that the low pass prototype is normalized in frequency ($\omega_n = 1$).
3. Use a table of normalized elements (g_i) corresponding to Chebyshev filters with the suitable ripple. Better yet, use the calculator available in Aula Global.
4. Determine the inverters (J_i), and from them the sets of even and odd mode impedances of each coupled line section.
5. In this step you may check that the design is correct from simulations with `CLIN` elements.
6. Determine the length, width and separation of each microstrip coupled line section. Now, you may check that the design is correct from simulations with `MCLIN` elements.
7. Finally, include non-ideal effects (basically, the fringe or end effect of the open circuits at the end of each resonator), adding `MLEF` elements (with zero length) or, better, substituting the `MCLIN` elements by `MCFIL`.

1.4 Directional coupler

The monitor port at the circuit output (see Figure 2) will be implemented with a directional coupler. Since the power to be extracted is some orders of magnitude lower than the main output power, it is recommended to use a section of coupled lines (for simplicity, they will be symmetrical). The section is determined by its length and the characteristic impedances of the modes with even and odd excitation Z_{0e} and Z_{0o}, as indicated in Figure 9.

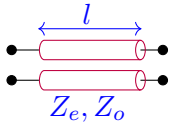


Figure 9: Directional coupler implemented with a coupled transmission line section.

1. Determine the electrical length of the coupled-line section, as well as the even and odd mode characteristic impedances, so that the specifications of coupled power are fulfilled, and the coupler is matched for Z_0.
2. Determine how the ports of the coupler should be connected. If necessary, include matched loads (Z_0) in the coupler. In this case, the loads must be included in the final circuit.

3. Determine the length, width and separation of the coupled microstrip lines. Now, you may verify that the design is correct from simulations with MCLIN circuit elements.

2 Formulation of the exercise

As a brief summary, the goal of this exercise is the design and characterization of the performance of a two-stage microwave amplifier, with one balanced stage, composed of the following elements:

1. A simple amplifying stage (first stage), with a single amplifier, including its bias and DC block network.
2. A balanced amplifying stage (second stage), composed of:
   (a) Two amplifiers (with their bias and DC block networks).
   (b) Two phase shifters, implemented with two transmission line sections.
   (c) Two Wilkinson power dividers/combiners.
3. A coupled-line band pass filter.
4. A coupled-line directional coupler.
5. Transmission line sections (with Z_0 characteristic impedance) to connect the other elements among them and with the ports, and some matching network, if required.

All the elements will be designed in microstrip technology, sharing a common dielectric substrate. The CAD tool to be used is Cadence AWR [1].

The design of each element must follow these general steps:

1. Theoretical analysis.
2. Design with circuit elements (TLIN, CLIN, ideal lumped elements).
3. Design with ideal microstrip elements (MLIN, MCLIN, MSUB).
4. Design with microstrip elements with discontinuities, and layout generation (the previous microstrip elements, and MCFIL, MTEE, MSTEP).

At each step, you must verify that the performance is the expected one, and justify and adjust the response if not. All the elements must be integrated to form a complete layout, and to characterize the full system response. To do so, you will need to add 50 Ω between each pair of elements, with bends (MBEND and similar, as MBENDA) or curves (MCURVE), so that the resulting layout is geometrically sound and possible. Avoid elements that are two close or overlapping, but also an excessive size or an awkward aspect ratio.

3 Specifications

The required system specifications are the following ones:

- Center frequency f_0 between 1 GHz and 6.5 GHz, computed from the NIA of the students using the equation[6]

$$f_0 = \frac{\sum_i \mathrm{NIA}_i \bmod 12}{2} + 1 \qquad \text{(in GHz)}$$

  or using the calculator available in Aula Global.

- Relative bandwidth of 5 %, that is, the band limits are 2.5 % above and below f_0. The following specifications must be fulfilled for all the frequencies inside this band:
  - Gain as high as possible (it depends on f_0, see the frequency response of the GVA-83+ amplifier).
  - Return loss at the input port higher than 30 dB.
  - Return loss at the output port higher than 18 dB.
- Attenuation equal or higher than 25 dB at frequencies separated from the center frequency more than 5 % (both above and below). This attenuation is measured with respect to the maximum gain in the pass band.
- Measured power at the monitor port 20 dB below the main output power.

All the specifications are defined with respect to $Z_0 = 50\ \Omega$ reference impedances at the ports. Each one of the components must be also designed for this reference impedance. Microstrip line widths and separations between lines should be larger than 200 µm.

3.1 Components and materials

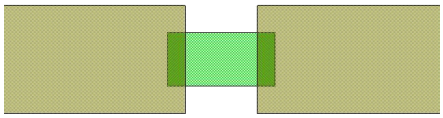
All the lumped elements must be SMD components, and should be included in the final layout. For the amplifiers, it has been already specified the SOT-89 format, and how to load the library, in section 1.1. In case of other lumped elements (resistors and capacitors), you must use components with 0603 metric (1.6x0.8mm). The library is included in the AWR installation[7].

The substrates available for the microstrip structure are included in the table below. The available dielectric thickness values are $h = 0.508$ mm and $h = 1.27$ mm, with $t = 17$ µm thick copper metallization.

[6] For example, if the NIA are 1234 and 6789, the remainder of the sum divided by 12 is $(1234 + 6789) \bmod 12 = 7$. Therefore, $f_0 = 7/2 + 1 = 4.5$ GHz.

[7] Search the file `Standard Chip Components.gds` in the `Examples` folder of the AWR installation path. Once loaded, assign the correct layout from the `Layout` tab of the properties dialog of the corresponding element.

(a) Physical appearance.



(b) Mounting in a microstrip line (AWR layout).

Figure 10: Component with 0603 metric.

Material	Relative permittivity (ε_r)	Loss tangent ($\tan\delta$)	Cost per area
Fiberglass (FR4)	4.7	0.01	$\times 1$
RT/Duroid 5880	2.2	0.009	$\times 10$
RT/Duroid 6006	6.15	0.0027	$\times 10$
RT/Duroid 6010.2LM	10.2	0.0023	$\times 10$

4 Report

The following are some recommendations you should follow when writing the report:

- Justify your design decisions.
- When you design each block, always check that its specifications are fulfilled by analyzing the essential parameters of the isolated circuit blocks. Later, when integrating them together, check that the full specifications are fulfilled.
- Use plots to show the performance and characteristics of the circuit elements, and also of the complete design. Especially, show that the specifications are fulfilled using markers or specification masks (they are available in AWR as optimization goals).
- AWR provides Cartesian plots and Smith charts, among others.
- Remember to clearly state the contents of each plot, and use suitable scales. Do not rely on the scales automatically adjusted by the software, specially for the vertical axis when logarithmic magnitudes are represented.
- Include the layout of the complete microstrip circuits. Do not forget to include the lumped elements, like resistors in the Wilkinson dividers, or the integrated amplifiers. Do not leave "loose" elements (you will identify them as red marks in the Layout view, as shown in Figure 12).
- For the input, output and monitor ports, simply leave a microstrip line with characteristic impedance Z_0 and length of some millimeters close to the circuit edge.
- *Optionally*, include ground via holes as required (see the geometric model of the integrated amplifier), and leave, for the power supply bias a metallic patch of 2x2 mm (see Figure 11).

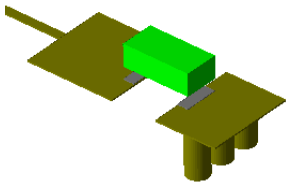
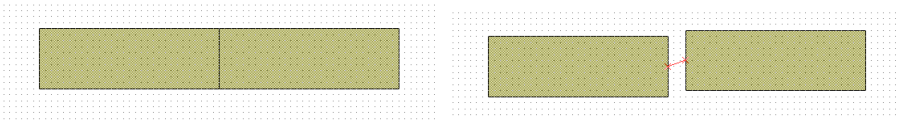


Figure 11: Example of SMD 0603 componente placed on a bias patch, with the other end connected to the ground plane through via holes.



(a) Right. (b) Wrong.

Figure 12: Connection of two layout elements.

Your report should contain the following sections.

4.1 Trabajo previo

The first part should be solved before the practical sessions.

1. Discussion of the most suitable microstrip substrate, taking especially into account the design center frequency. To do so, consider that the width of each line must be no less than 200 µm, but also much smaller than the length of the shorter section (take as a reference $\lambda/4$ at the operation frequency, since it is a length common to many elements in the design).

   A wrong decision when selecting the substrate may require going back to previous steps of the design, so be careful.

The following is a summary of the sections marked as color text from previous sections.

2. Study of the response of the GVA83+ amplifier, from the data provided by the vendor.
3. Study and design of the bias and DC block networks for the amplifiers.
4. Study of the balanced structure response.
5. Theoretical and geometric design of the Wilkinson power combiners/dividers.
6. Circuit design of the ideal low pass and band pass prototypes of the filter, so that the band specifications are fulfilled.
7. Theoretical and geometric design of the coupler.

4.2 Design and characterization of the microstrip elements

8. Design and characterization of the Wilkinson power divider/combiner.
9. Design and characterization of the first amplifying stage.
10. Combination of the two previous elements and phase shifters (transmission line sections) to obtain the balanced amplifying second stage. Characterization of the stage.
11. Design and characterization of the band pass filter.
12. Design and characterization of the output coupler.

4.3 Integration and complete

13. Integration of all the elements in a common microstrip layout.
14. Simulation of the full network response at frequencies in and around the pass band.
15. If the specifications are not fulfilled, slight modification of the required elements, or inclusion of additional, auxiliar elements, like matching networks.
16. Simulation of the full network wideband response (from 0 GHz up to 7 GHz).

4.4 Results and conclusions

17. Include the enumeration of all the system specifications, comparing the ones in this document with the simulated results.
18. Conclusions, where you justify your design decisions, and any possible specifications that are not fulfilled, and also the critical aspects of the design.

5 Deliverables

The results of your exercise will be delivered by means of an Aula Global form (assignment activity). They are the following ones:

- AWR Microwave Office *.emp file with schematics, layout of the elements and full circuit, and plots that show the suitable simulations.
- PDF file with the full report.

References

[1] *Awr microwave office*, https://www.awr.com/software/products/microwave-office, Visitado: 2021-04-07.

[2] D. M. Pozar, *Microwave Engineering*, 4th ed. John Wiley & Sons, 2011.

[3] R. E. Collin, *Foundations for Microwave Engineering*, 2nd ed. John Wiley & Sons, 2007.

[4] M. Steer, *Fundamentals of Microwave and RF Design*. University of North Carolina Press, 2019. [Online]. Available: https://uncpress.org/book/9781469656885/fundamentals-of-microwave-and-rf-design/.

[5] J.-S. Hong, *Microstrip filters for RF/microwave applications*, 2nd ed. John Wiley & Sons, 2011. [Online]. Available: https://learning.oreilly.com/library/view/microstrip-filters-for/9781118002124/.