Microelectronics and Integrated Circuit, Opamp design

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The sizes of the transistors have been obtained with these computations:

CIM, opamp design

$SR = \frac{I_7}{C_C}$

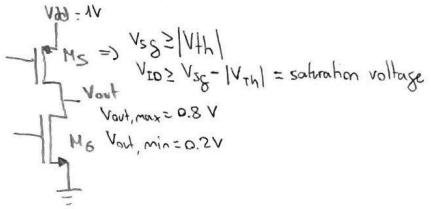
$SR \geq 10V/\mu s$

$C_C \geq 0{,}22 C_L\big|_{C_L = 4pF} = 0{,}88pF \Rightarrow \boxed{1pF = C_C} \Rightarrow I_7 = SR \cdot C_C = 100\mu A \Rightarrow I_7 = 150\mu A$

$P = V_{dd}(\underbrace{I_{bias} + I_7 + I_6}) \leq 0{,}5mW$

$I_{bias} = I_7 = I_6 = 150\mu A$

simplifies the circuit



$V_{SG} \geq |V_{th}|$

$V_{ID} \geq V_{SG} - |V_{th}|$ = saturation voltage

$I_{DS} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_5 (V_{SDS,sat})^2$

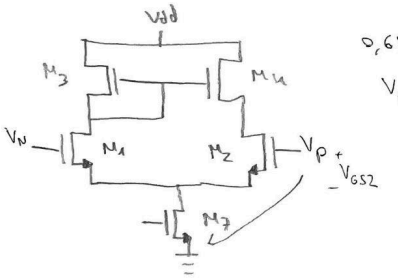
$I_{DS} = 150\mu A$; $V_{SDS,sat} = 0{,}2V$

$\left(\frac{W}{L}\right)_5 = \frac{2 \cdot I_{DS}}{\mu_p C_{ox} V_{SDS,sat}^2} = 166{,}67 \Rightarrow$

$\Rightarrow \boxed{\left(\frac{W}{L}\right)_5 = 170}$

$I_{D6} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 \cdot V_{DS,sat}^2 \Rightarrow \left(\frac{W}{L}\right)_6 = 83{,}3 \Rightarrow \boxed{\left(\frac{W}{L}\right)_6 = 90} \Rightarrow \boxed{\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_8 = \left(\frac{W}{L}\right)_6 = 90}$

$I_{D6} = 150\mu A$; $V_{DS,sat} = 0.2V$



$0{,}6V = V_{GS2} + V_{OS,sat2} \Rightarrow V_{GS2} = 0{,}6 - 0{,}2 = 0{,}4V$

$V_{GS2} \geq V_{thN} = 0.3V$

$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{th})^2$

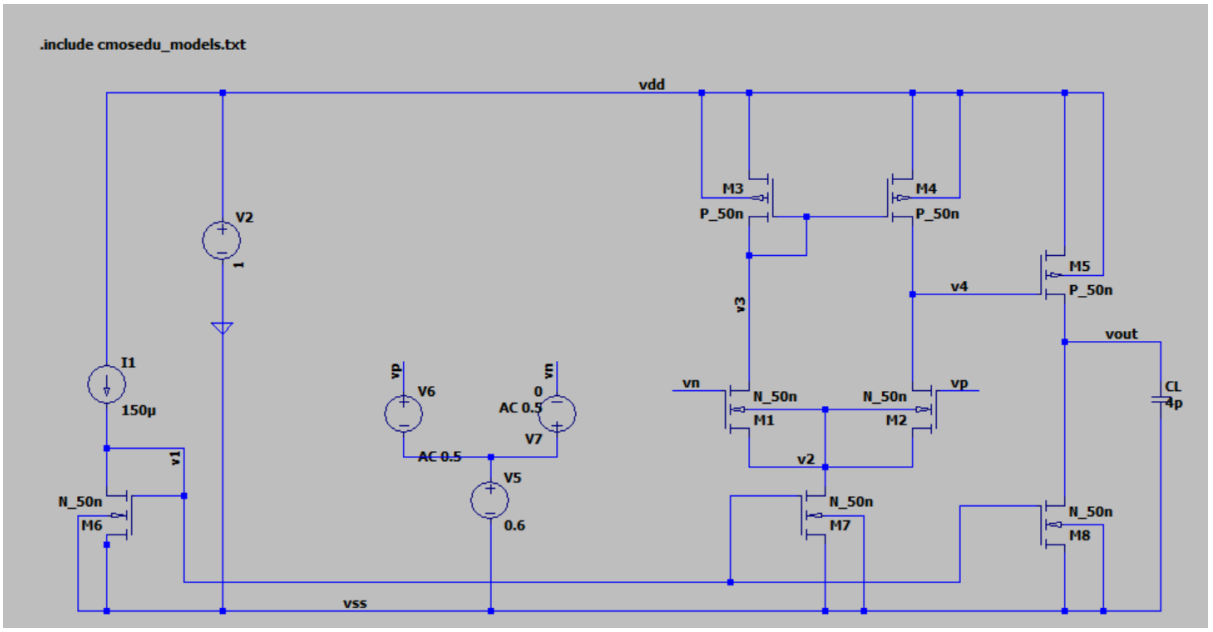
$\left(\frac{W}{L}\right)_2 = \frac{2 \cdot I_{D2}}{\mu_n C_{ox}(V_{GS2} - V_{th})^2} = \frac{2 \cdot 75}{90(0{,}4 - 0{,}3)^2} = 166{,}67$

$\Rightarrow \boxed{\left(\frac{W}{L}\right)_2 = 170 = \left(\frac{W}{L}\right)_1}$

$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 3\left(\frac{W}{L}\right)_1 = 510$

@50nm $\Rightarrow L = 200nm \Rightarrow \begin{cases} W_1 = W_2 = 34\mu m & W_5 = 34\mu m \\ W_3 = W_4 = 102\mu m & W_6 = W_7 = W_8 = 18\mu m \end{cases}$

This is the circuit we are going to use in the simulations:



After using these values in LTSpice we have seen that the output voltage is out of the range of the desired ones, which were between 0.2V and 0.8V.

```
--- Operating Point ---

V(vdd):          1                voltage
V(vout):         0.0137487        voltage
```

We can see that the transistor 8 is not saturated:

```
Id(M8):          -3.00576e-05     device_current
```

One possible way to solve this is to decrease the Vsd. To do that we have to increase Id and to achieve that we can increase the W of transistor 7. We will use 120um, the output voltage is now:

```
--- Operating Point ---

V(vdd):          1                voltage
V(vout):         0.490469         voltage
```

So we had to modify the W of transistor 7 from 18um to 120um.

After this modification we can measure the current flowing through M6, M7 y M8 and the sum of them will be multiplied by VDD to obtain the power consumption, which is 650 uW.

The computations of the gain are the following ones:

$$gain \geq 50dB$$

$$gain = gain1 \cdot gain2$$

$$gain1 = g_{m1} \cdot (r_{o2} \| r_{o4})$$

$$g_{m1} = \sqrt{2 \cdot \mu_n C_{ox} \left(\frac{W}{L}\right) \cdot I_D} = \sqrt{2 \cdot 90 \cdot 170 \cdot 75} = 1514\,\mu A/V$$

$$r_{o2} = \frac{1}{\lambda_n I_D} = \frac{1}{0{,}6 \cdot 75\mu} = 22k\Omega$$

$$r_{o4} = \frac{1}{0{,}3 \cdot 75\mu} = 44k\Omega$$

$$r_{o2} \| r_{o4} = 14{,}6k\Omega$$

$$gain1 = 22V/V$$

$$gain2 = g_{m5} \cdot (r_{o5} \| r_{o6})$$

$$g_{m5} = \sqrt{2 \cdot 45 \cdot 100 \cdot 150} = 3674\,\mu A/V$$

$$r_{o5} = \frac{1}{0{,}3 \cdot 150\mu A} = 22k\Omega$$

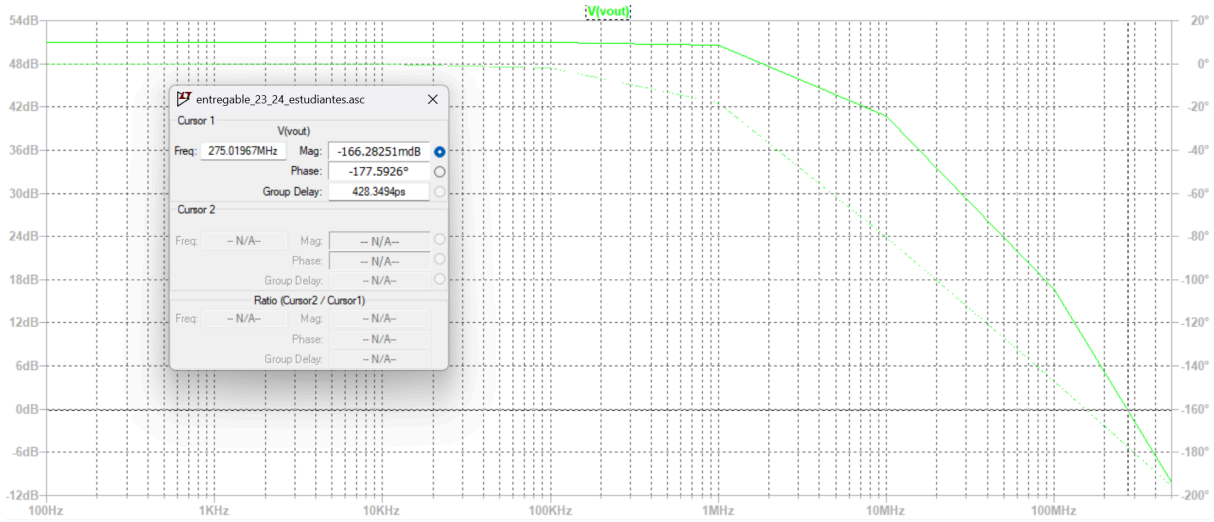
$$r_{o6} = \frac{1}{0{,}6 \cdot 150\mu} = 11k\Omega$$

$$r_{o5} \| r_{o6} = 7{,}3k\Omega$$

$$gain_2 = 26{,}8V/V$$

$$gain = 22 \cdot 26{,}8 = 589{,}6\,V/V \Rightarrow 20\log(589{,}6) = 55dB$$

After the AC simulation we obtain:



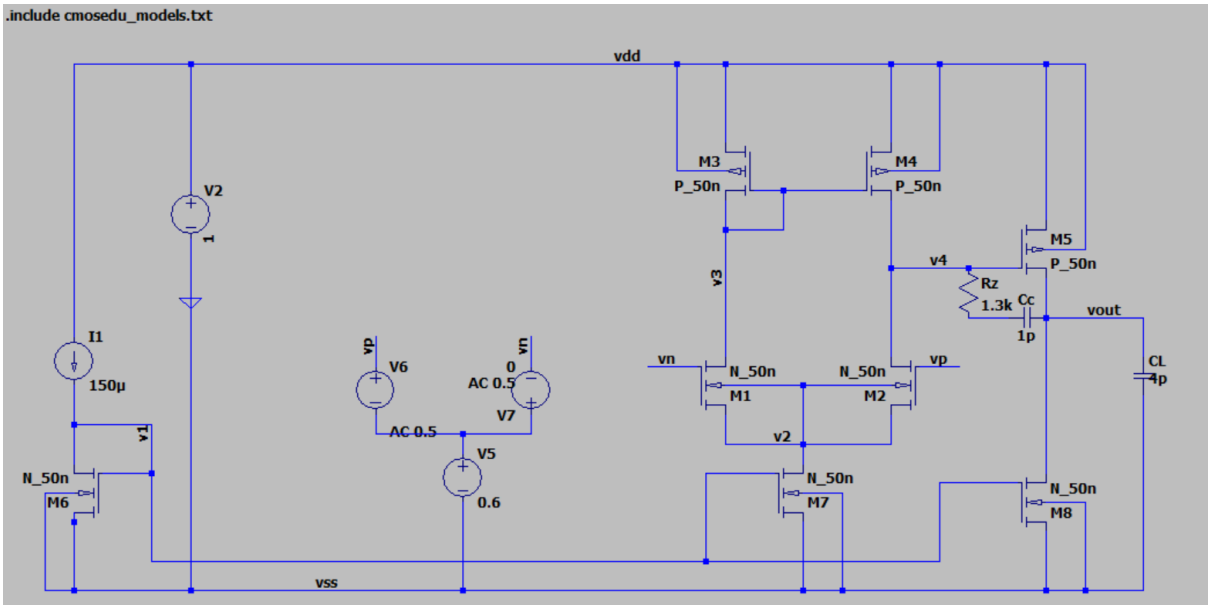
where we can see that the gain is 50dB which is similar to the one computed before. The GBW is 275 MHz.

For the stability we can see that the amplifier is stable because the phase at 0dB is 177.6 degrees, and the phase margin is 180 - 177 = 3 degrees, which is positive.

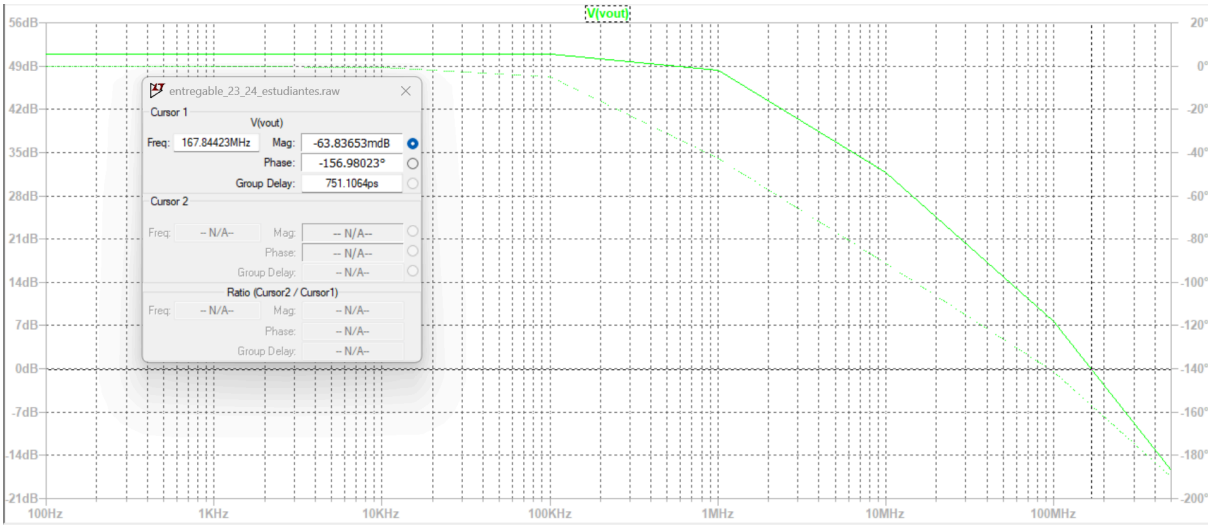
We can increase the phase margin by adding a resistor and a capacitor in series connecting v4 and vout. The capacitance of Cc was already computed, 1pF, and for the impedance of Rz we can use the formula of the statement:

$$R_Z = \frac{C_C + C_L}{C_C} \frac{1}{g_{m5}}$$

and we obtain that Rz = 1360Ω
The resulting circuit is:

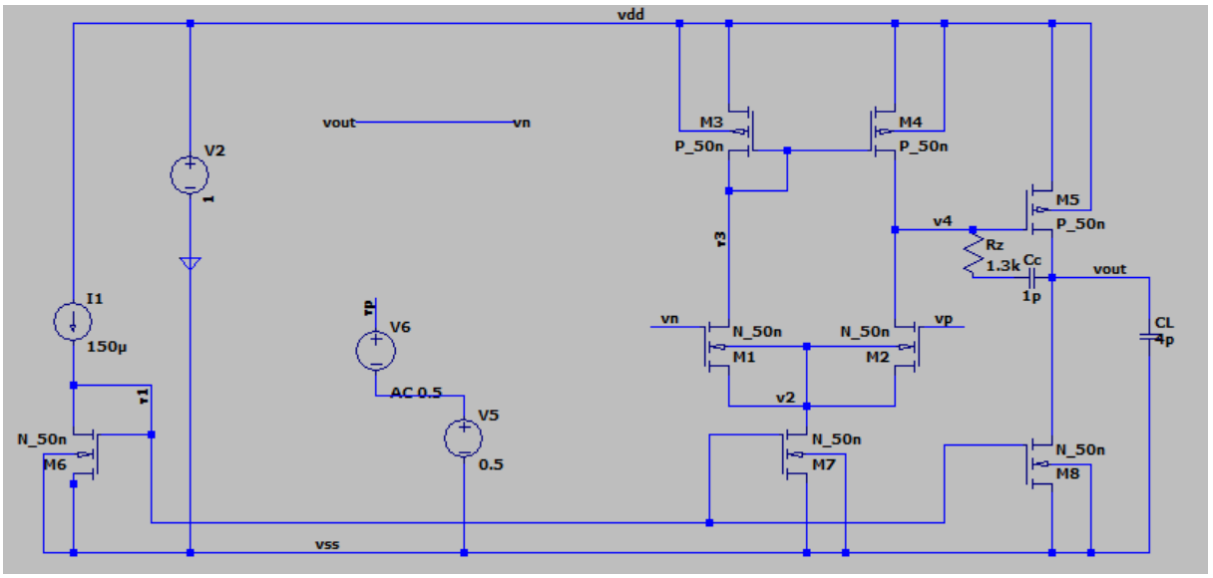


We can see that now the phase at 0 db is:

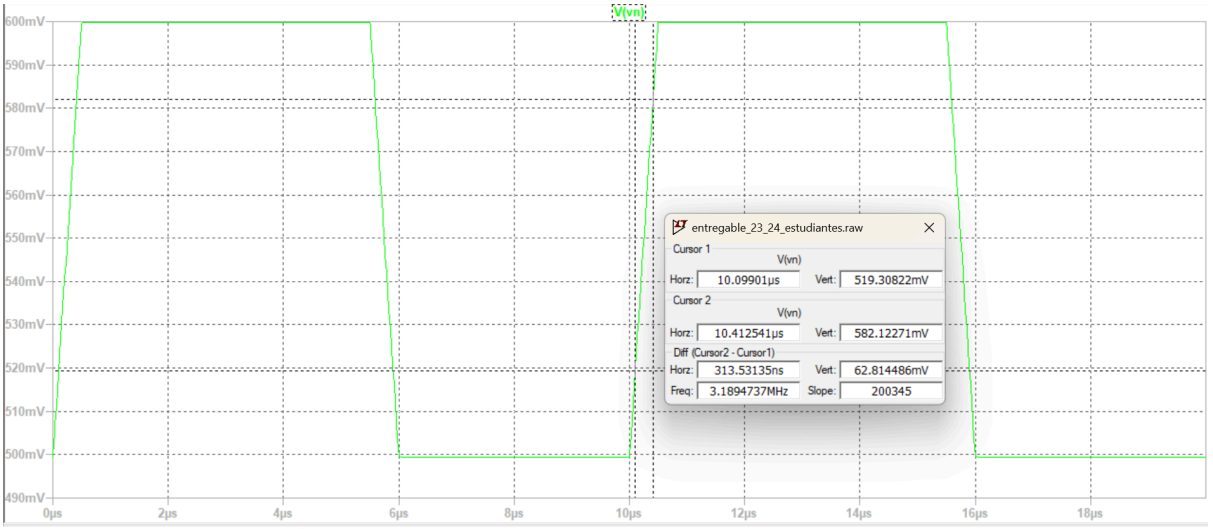


so the phase margin is 180 - 157 = 23 degrees. We can see that we have increased the phase margin but the GBW is smaller, 168 MHz.

For the third experiment we have to set up as a buffer the architecture. The resulting circuit is:

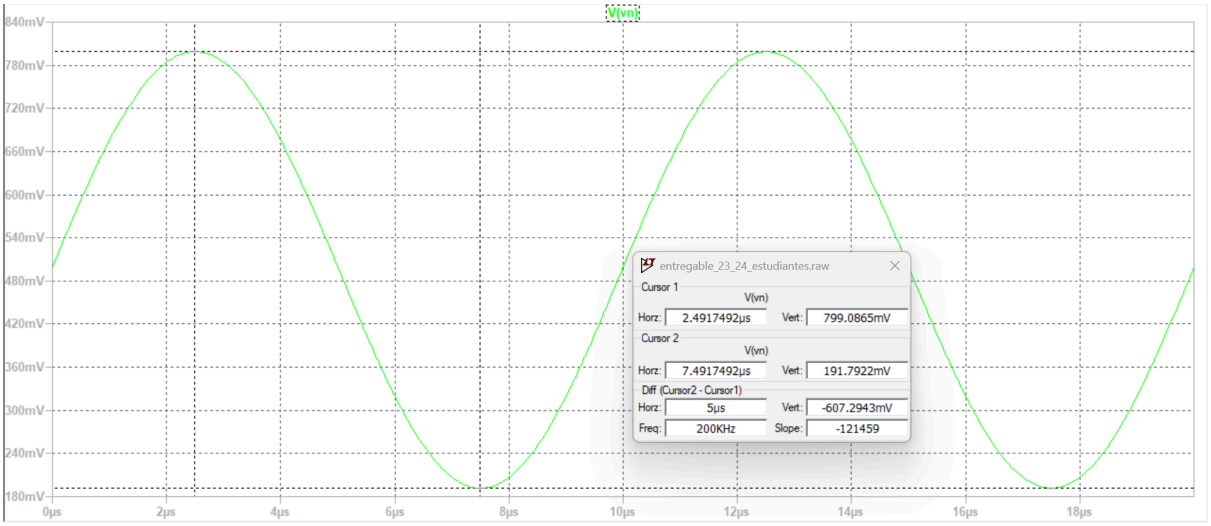


We obtain this plot with a pulse between 0.5V and 0.6V with a frequency of 10 KHz :



and we can compute the slew rate is 200345 mV/us = 200.345 V/us which is higher than the 10V/us of the requirement.

This is the plot when we use a sinusoidal signal of 100 kHz, amplitude of 0.3 V and common-mode voltage of 0.5 V:



where we can see that the Vout,min = 0.19V and Vout,max = 0.8V which fulfills the requirements.

After carrying out the experiments we can answer the following questions:

- What is the purpose of the DC simulation performed?
  The purpose is to obtain the currents in the transistors and the voltage in the output. We are also able to compute the power consumption.

- What is the purpose of the AC simulation performed?
  With the AC simulation we can see the gain and the GBW. We can also compute the phase margin to see if the amplifier is stable.

- If the “hand-made” gain is not enough, how could you improve it?
  We can obtain a higher gain by increasing gm, that can be increased by increasing the width of the transistor.

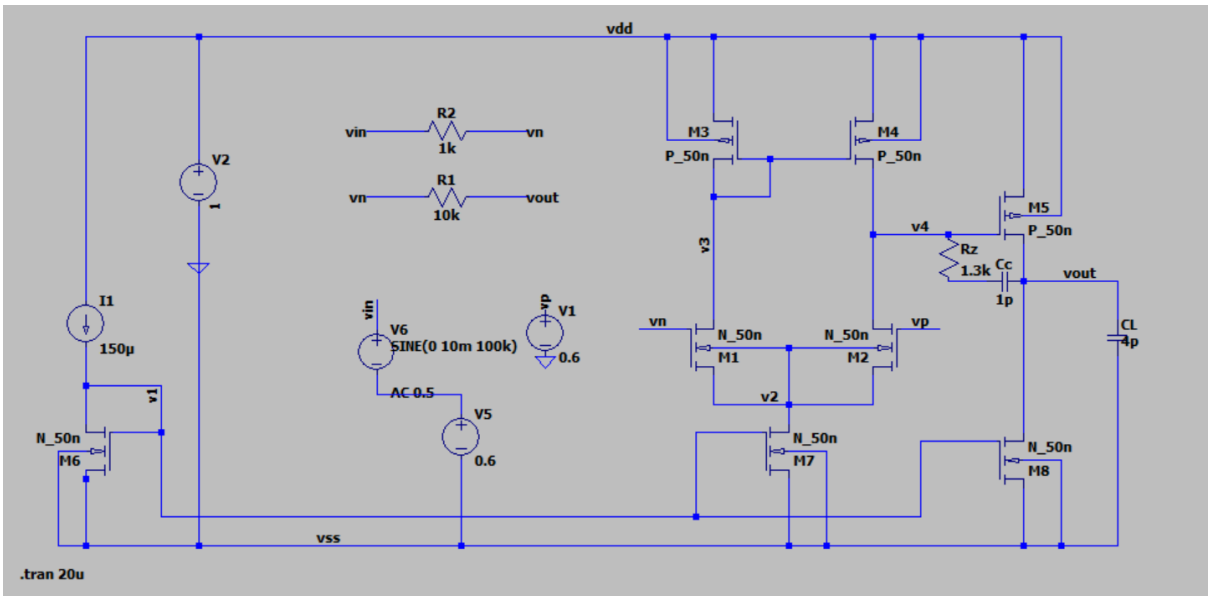
- If CL is reduced, how does GBW change?
  If CL is reduced the GBW increases.

- What is the purpose of CC and RZ?
  The purpose is to obtain a higher phase margin and make the operational amplifier more stable.

- How could you increase Vout,max?
  We can increase Vout,max by increasing the total gain which is the product of gm1 and gm5, as we can see in the computations, so by increasing the size of m1 or m5 we can increase the Vout,max.

- And decrease Vout,min?
  We can decrease Vout,min by applying the same solution as in the previous question

Setup the design as follows:
Vin is a sinusoidal signal of 10-mV amplitude, 0.6 V common-mode voltage and frequency of 100kHz. What is the theoretical gain Vout/Vin? Justify your answer. Run a transient simulation to verify whether the theoretical gain is accomplished or not. Copy the result of the simulation.



The theoretical gain is -R1/R2 = -10 and in the following plot we can see a gain of -10: