UNIVERSIDAD CARLOS III DE MADRID

Laboratory Report

Integrated Circuits and Microelectronics

Andrés Navarro Pedregal (100451730) & Daniel Toribio Bruna (100454242)

Dual Bachelor in Data Science and Engineering and Telecommunication Technologies Engineering

March 7, 2024

Contents

1 Introduction

In this lab report, our goal is to create a waveform generation and FIR (Finite Impulse Response) filter implementation. Our objective is to understand and construct circuits that can generate sinusoidal signals and filter them effectively. These circuits will be designed to operate on FPGA (Field-Programmable Gate Array) boards, specifically the Basys 3 model, utilizing components such as LEDs and digital-to-analog converters (DACs).

Session 1: Waveform Generator In our first session, we create a circuit capable of generating sinusoidal signals represented with 8 bits of precision. This circuit will be responsible for producing these signals at different frequencies, which will be selected through input switches. The generated waveform will be visualized through both LEDs on the FPGA board and an 8-bit DAC (Pmod R2R), ensuring versatility in signal output. Our design will consist of various components including timers, memory units, and counters to facilitate accurate signal generation and display.

Session 2 and 3: FIR Filter Implementation Moving forward, we implement a digital FIR filter alongside the previously developed waveform generator. The FIR filter serves the purpose of refining the generated signals by attenuating frequencies beyond a specified cutoff point. Utilizing filter coefficients obtained from MATLAB, we construct a filter with a predetermined number of stages to achieve the desired filtering effect. Integrating this filter into our existing circuitry, we aim to enhance the quality of the generated signals for various applications.

Throughout these sessions, we'll engage in simulation, synthesis, and practical implementation of our designs on FPGA boards. Additionally, we'll document our progress through test benches, oscilloscope measurements, and final reports, ensuring a comprehensive understanding of the design process and its outcomes.

By the end of these sessions, we anticipate gaining valuable insights into circuit design, signal processing, and FPGA-based system implementation, laying a solid foundation for further exploration in the field of integrated circuits and microelectronics.

2 Design Characteristics

2.1 Full Implemented Functionality

2.2 I/O Interface, Type And Functionality

3 Design Structure

3.1 Block Diagram

3.2 Component Description

3.3 Calculation

3.3.1 Frequencies

3.3.2 Filter Coefficients

3.4 Simulations

4 Architectures

4.1 Parallel Architecture

4.2 One Flip-Flop Pipeline Architecture

4.3 Two Flip-Flop Pipeline Architecture

5 Synthesis Results

6 Conclusion