uc3m | Universidad Carlos III de Madrid

Dual Bachelor in Data Science and Telecommunications Technologies Engineering 2020-2025

Microwind LAB 4

Integrated circuits and microelectronic 23/24-S2

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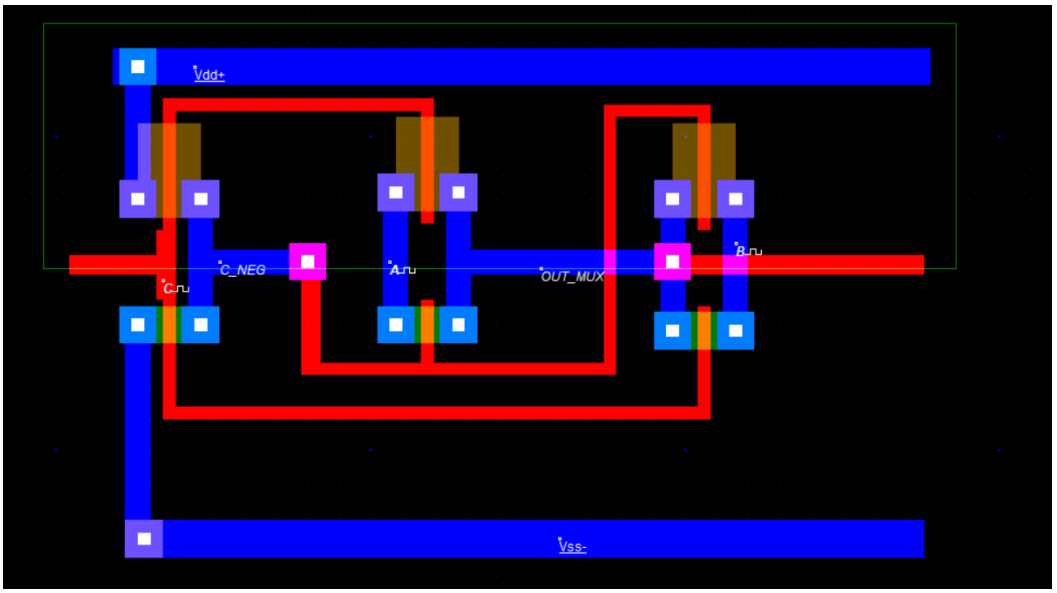
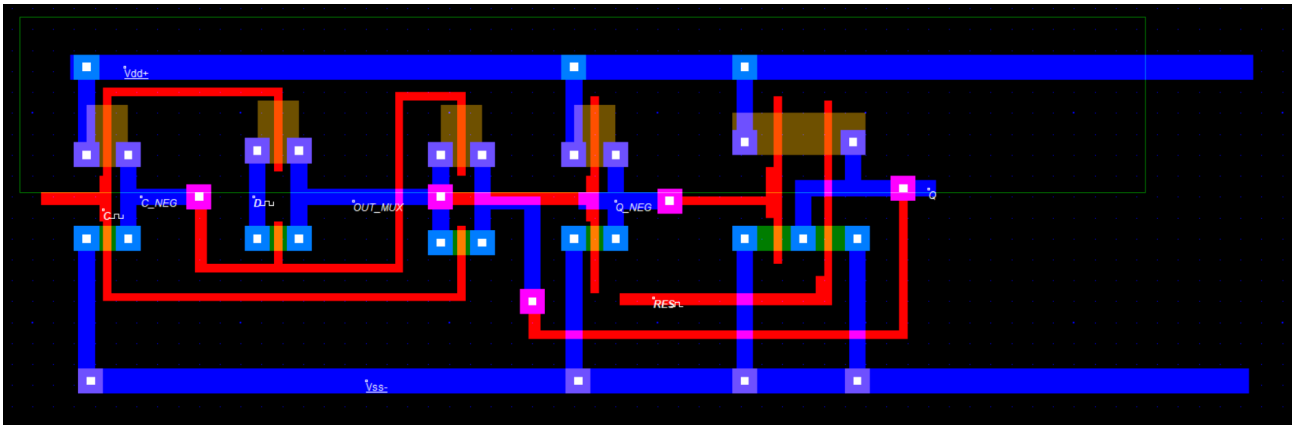
1. Draw the schematic for a multiplexer using transmission gates.



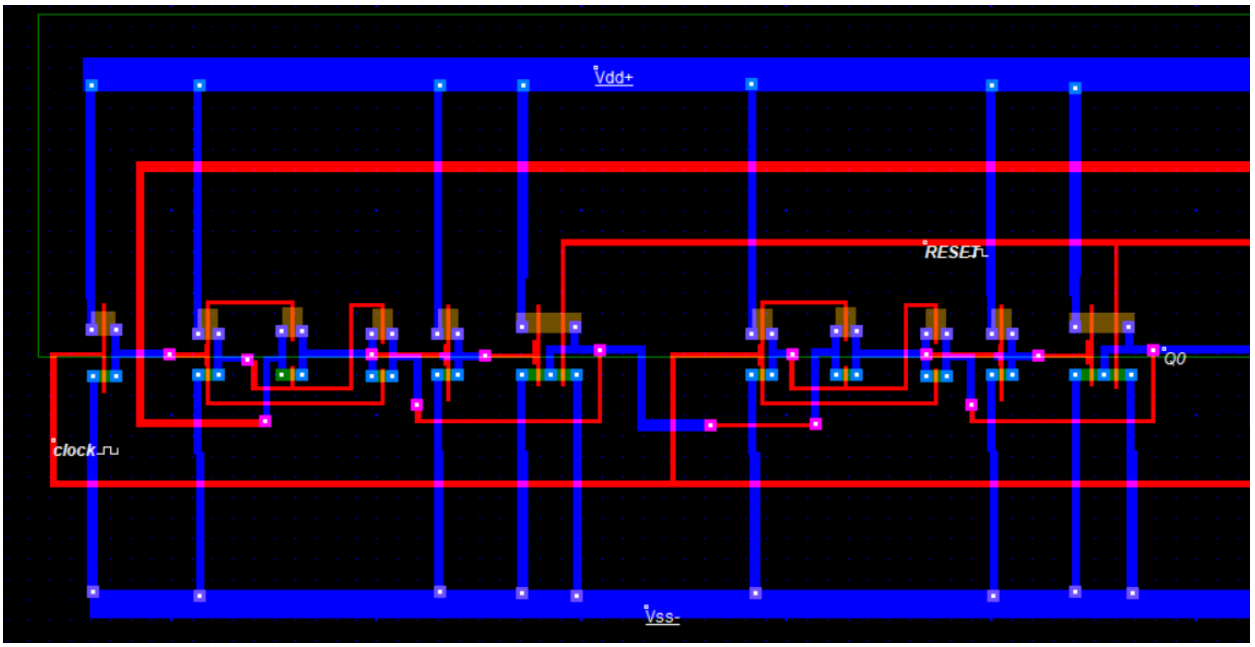
On the left side we have an inverter and on the right, two transmission gates, one after the other.

2. Draw the schematic for a D-latch.



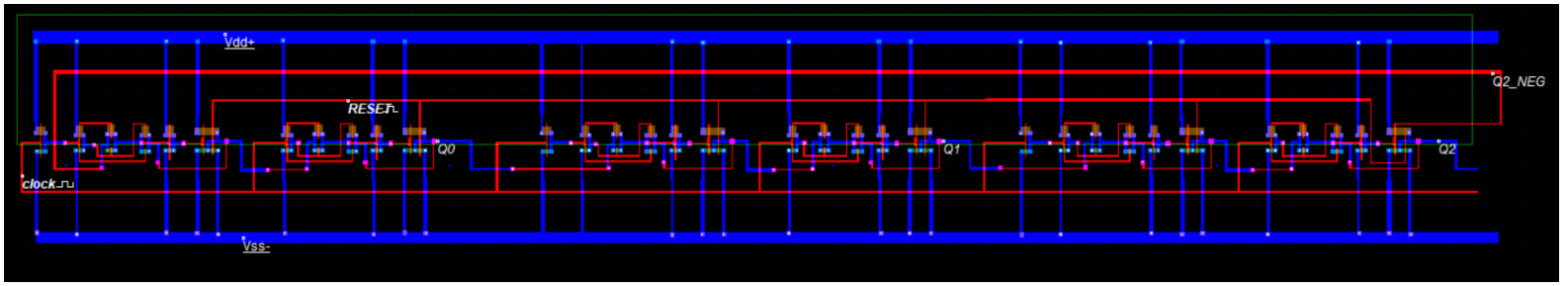
Here we have the D-latch composed by the previous MUX in the left side followed by an inverter and a NOR Gate.

3. Use two D-latches and an inverter to build an edge-triggered flip-flop.



Now we have joined both D-latches together to get the flip flop.

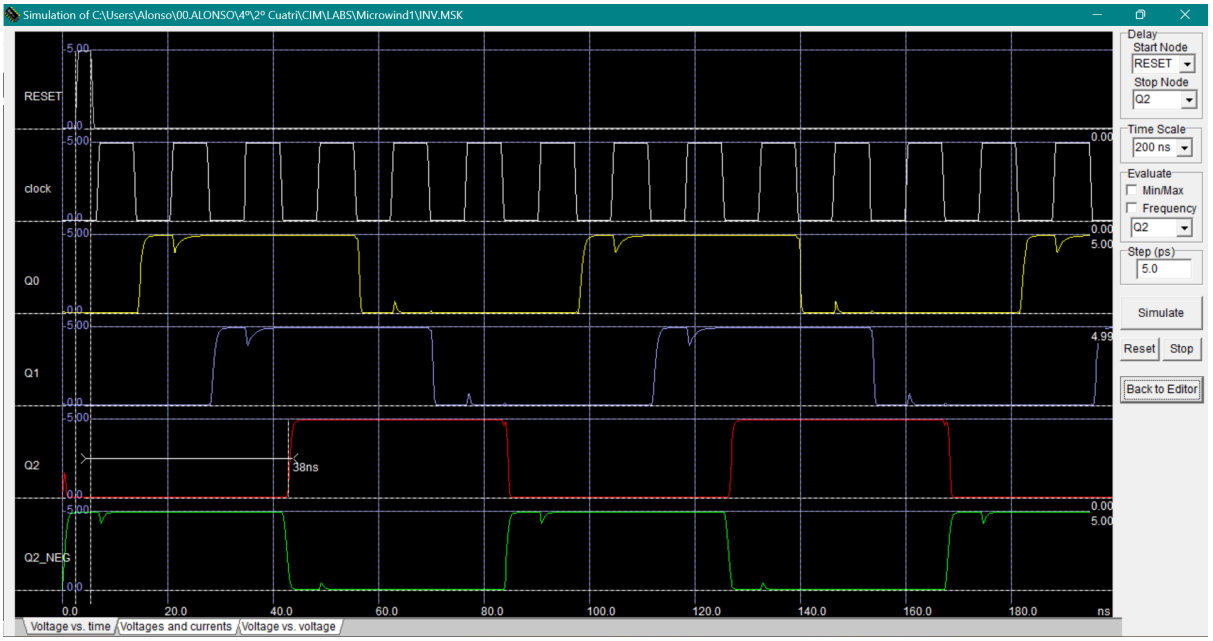
4. Use three flip-flops to build the counter.



5. Use the MicroWind tool to draw the layout of the counter.
6. Perform a simulation to verify them, showing all inputs (Clk, Reset) and outputs (Q2, Q1, Q0).
For a 3-bit Johnson counter implemented with three flip-flops (bistables) labeled as Q0, Q1, and Q2, we expect to see the following bit sequence:

Initially, all flip-flops are reset to 0. So, the initial state is 000.
As the clock pulses, the counter should progress through the following sequence:
000, 001, 011, 111, 110, 100, 000 (it loops back to the initial state and repeats).

We are asked about Q2, Q1 and Q0:
Q0 corresponds to the least significant bit (LSB).
Q1 corresponds to the middle bit.
Q2 corresponds to the most significant bit (MSB).

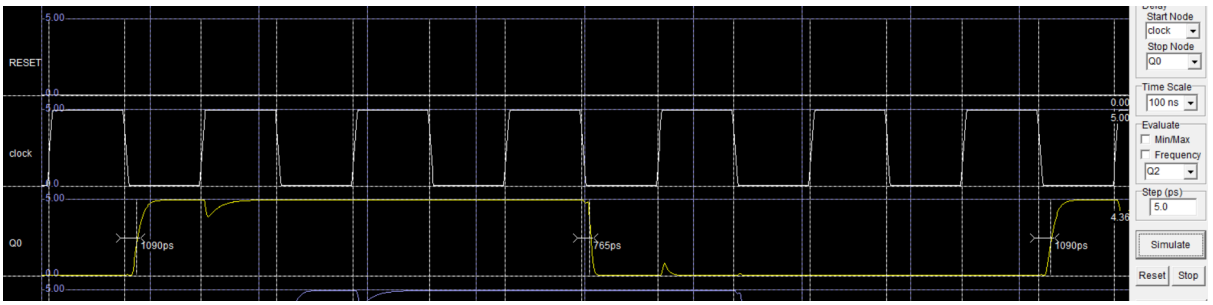


Initially: Q2 = 0, Q1 = 0, Q0 = 0
After the first clock pulse: Q2 = 0, Q1 = 0, Q0 = 1
After the second clock pulse: Q2 = 0, Q1 = 1, Q0 = 1
After the third clock pulse: Q2 = 1, Q1 = 1, Q0 = 1
After the fourth clock pulse: Q2 = 1, Q1 = 1, Q0 = 0
After the fifth clock pulse: Q2 = 1, Q1 = 0, Q0 = 0
After the sixth clock pulse: Q2 = 0, Q1 = 0, Q0 = 0 (back to the initial state)

And this is the exact behaviour that we expect from the counter, so this should be correct.

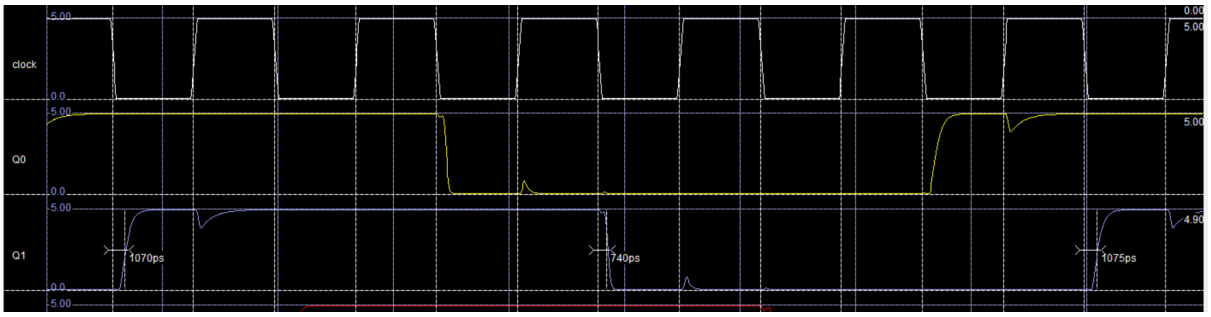
7. Analyse the maximum circuit delay.
To see the delay, in the simulation we have to place the clock in the start node and the variables in the stop nodes.

Delay between clk and Q0:



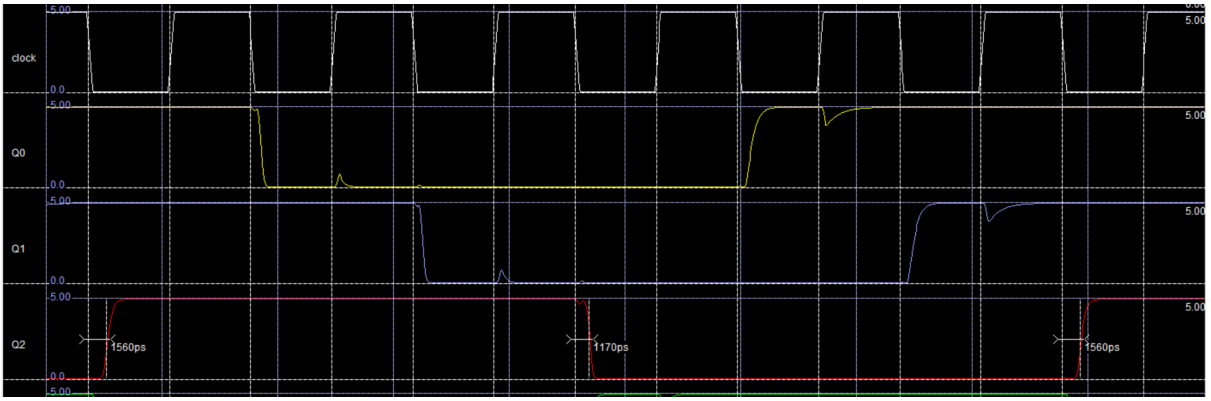
In the rising edge we all the time have higher delay. Trise = 1090ps, Tfall = 765ps.

Delay between clk and Q1:



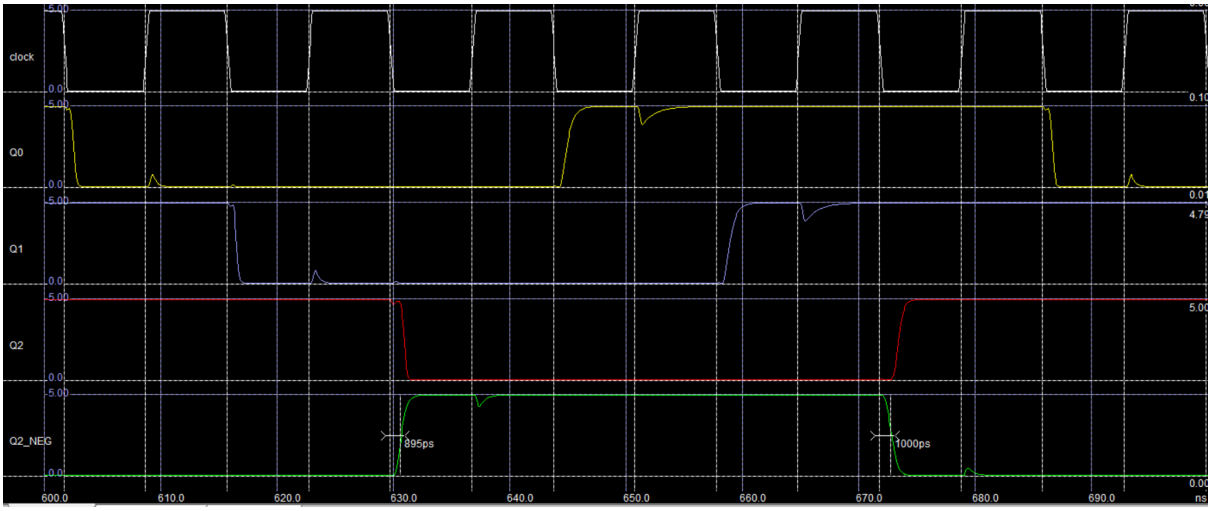
Trise = 1070ps, Tfall = 740ps.

Delay between clk and Q2:



Trise = 1560ps, Tfall = 1170ps.

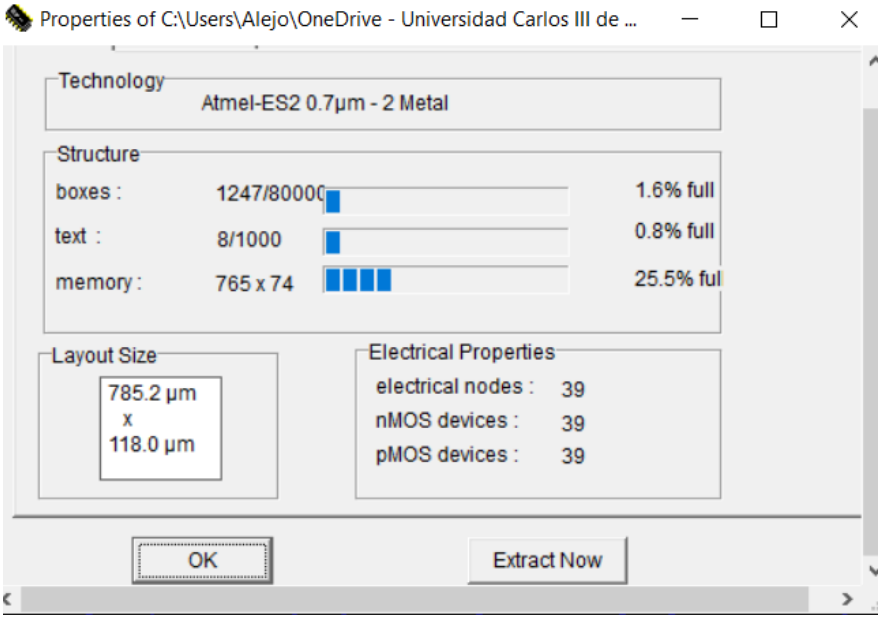
Delay between clk and Q2_NEG:



Trise = 895, Tfall = 1000ps. The difference between Q_NEG and the others is that here Tfall is longer than Trise.

The maximum circuit delay is the maximum value, 1560 ps.

8. Calculate the area of the obtained circuit.



At the end, the total area is 92,653.6 um^2 or what it is the same: 0.092653 mm^2.
Notice that this area could be significantly reduced as we are wasting a lot of space.