

*Dual Bachelor in Data Science and Telecommunications Technologies Engineering 2020-2025*

***Microwind Lab Work***



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Descripción generada automáticamente

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## Schematics

Multiplexer using transmission gates.

Diagrama

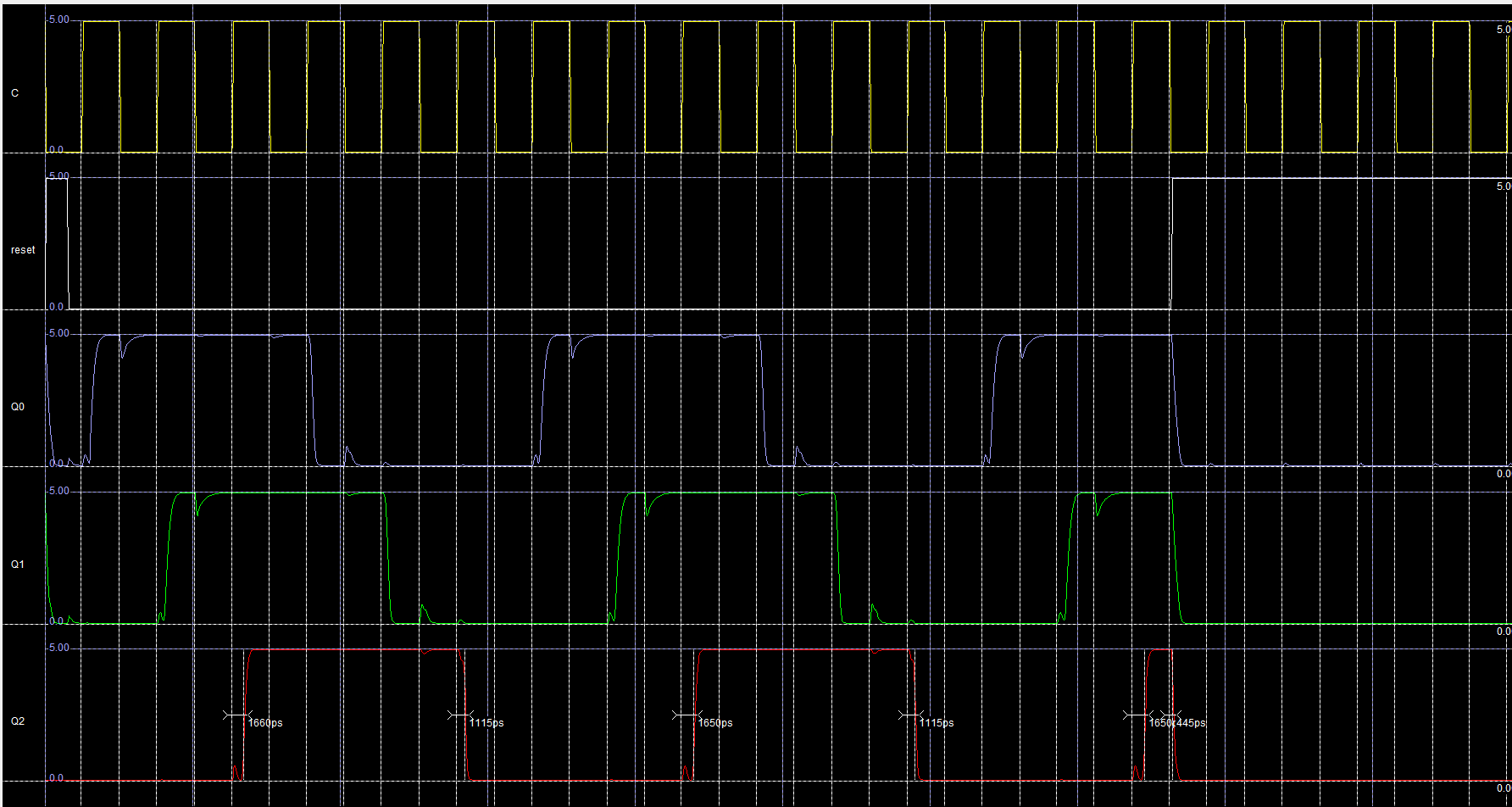
Descripción generada automáticamente

D-latch

Un dibujo de un pizarrón blanco

Descripción generada automáticamente con confianza baja

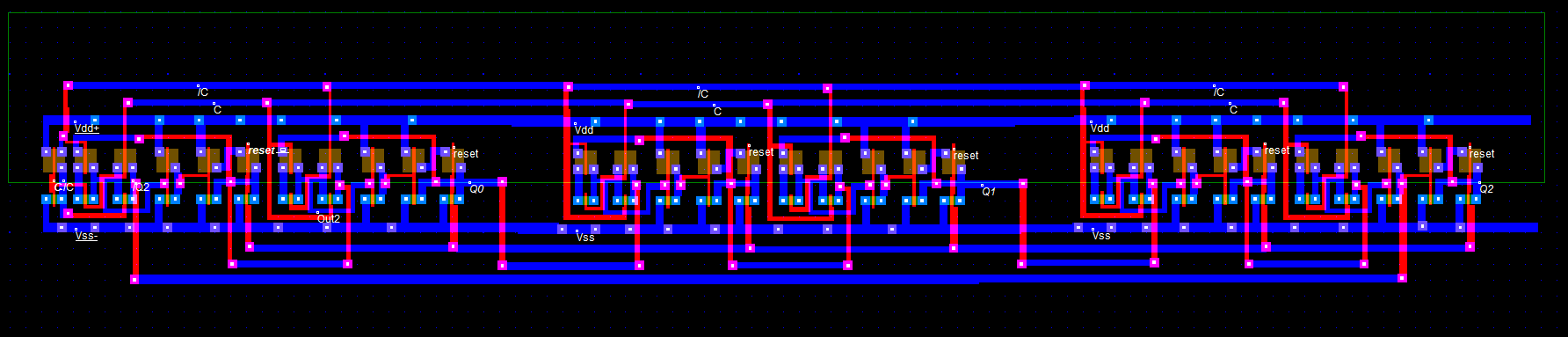
## Capture of step 5 simulation and explanations about the waveforms showed



Here we can see the simulation of the circuit. The first wave is the clock, the second is the reset, the third is Q0, the fourth is Q1 and the fifth is Q2.

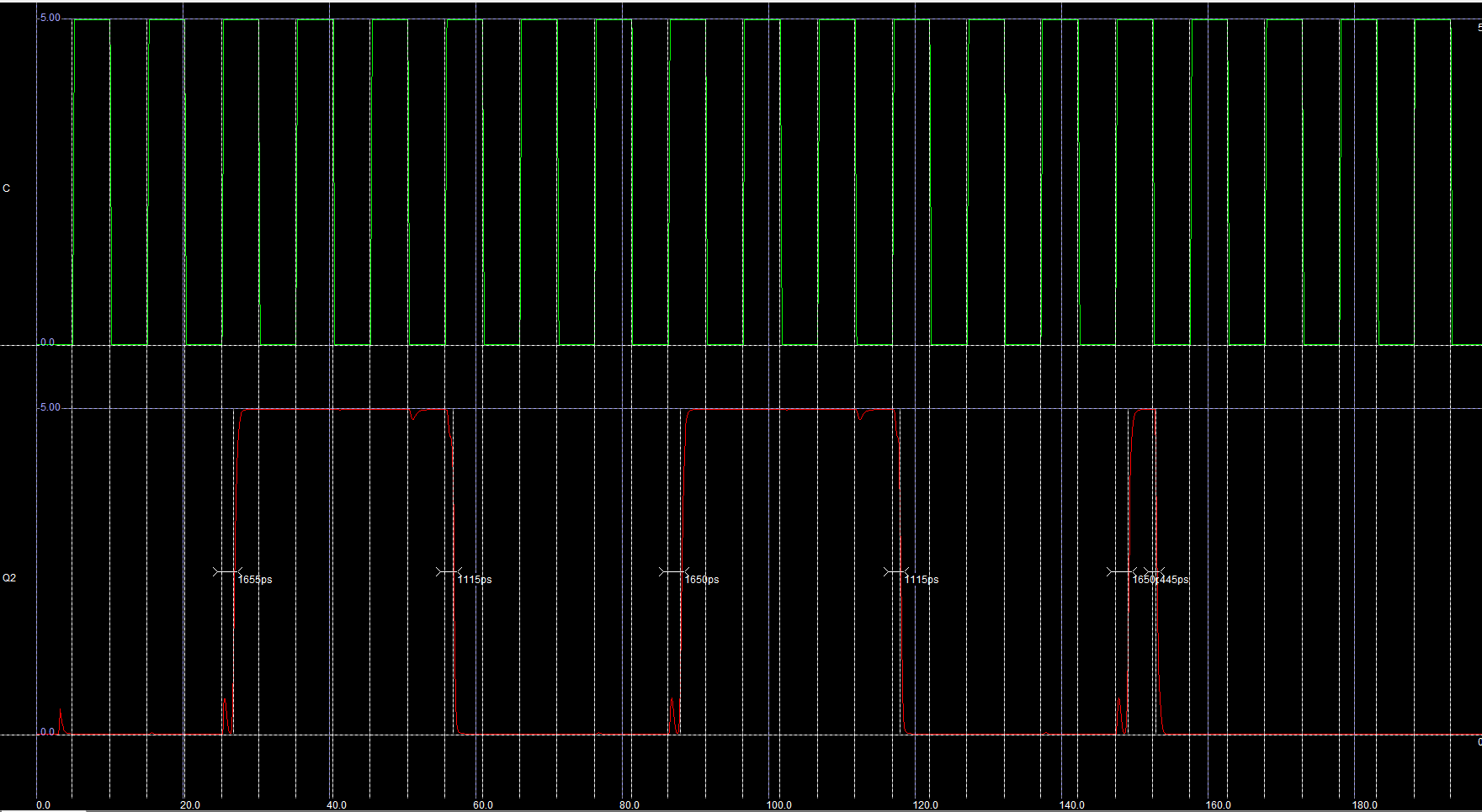
We can see that initially when the reset is high, all the Q are set to 0.

When there is a rising edge in the clock, the counter starts counting as expected. if Q2 is 0, Q1 is set to 1. If Q0 is 1, Q1 is set to 1, and if Q1 is 1, Q2 is set to 1. As seen. Also at the end of the simulation, when the reset is set to 1, then the circuit is reset and is stopped as it is expected.

Here you can see a picture of the final circuit implemented.  


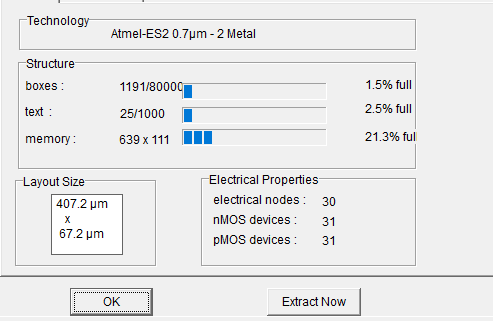
# Delay and Area

Also in the simulation as show below:



We can see that the maximum delay between the clock and Q2 (end of the circuit) is 1650 ps.

For the area:



We get a total area of 27363 um^2.