Size saving FFT core for OFDM comunications

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***Abstract*—A software tool for high-level synthesis of Finite Impulse Response (FIR) filters is presented. The tool is based on Canonic Signed Digit (CSD) coding for filter coefficients and Non-recursive Signed Common Subexpression Elimination algorithm (NR-SCSE) for logic operators (adders and subtractors) minimization. By means of this tool a fully-synthesizable HDL code can be generated which is suitable for Field Programmable Gates Arrays (FPGA) as well as for Application Specific Integrated Circuits (ASIC). In this paper all the algorithms implemented are described. Logic operators (LOs) are based on ripple carry structures (RCS) in order to save area and simplify routing. The source code was developed in C programming language and can be used under GNU General Public License (GNU-GPL).**

I. Introduction

FIR filters are widely used in a variety of applications such as channel equalization, matched filtering, pulse shaping, etc. The main advantages of stability and linear phase make FIR filters the prefered option in most of the cases. However, the complexity of a FIR filter implementation lies in the number of filter coefficients. In those applications where throughput is the principal constraint, the bit parallel transpose architecture [1] is commonly chosen. In this architecture the filter input is multiplied by all the coefficients at the same time. This problem is known as multiple constant multiplication (MCM).

The basic method to multiply a variable by a constant without using a multiplier is to represent the constant with some fixed point arithmetic encoding and to use a *shift-and-add* procedure. This problem is known as single constant multiplication (SCM). A common employed coding technique is Canonic Signed Digit (CSD) representation which minimizes the number of nonzero bits in comparison with two's complement representation. Dempster and McCleod [2] developed an optimal solution based on an exhaustive search algorithm for word length up to 12 bits which was later extended by Gustafsson et al. up to 19 bits [3].

When MCM must be accomplished, finding shared intermediate results between coefficient decompositions helps to reduce the hardware complexity. It has been proved that the optimal solution to this problem is NP-Complete [4] and is strongly dependant of arithmetic coding employed in the coefficients representation. This fact encourages the use of heuristic techniques. There are two different groups of heuristic algorithms: graph dependence (GD) based and common subexpression elimination (CSE) based.

One of the first works describing the problem of MCM optimization based on a GD was developed by Bull and Horrocks [5]. In their work, the FIR filter structure is represented by a GD creating a new coefficient depending on the previous ones by using an heuristic method. Dempster and McCleod proposed to use their optimal solution to the SCM problem to each filter coefficient and to use what they called n-dimensional reduced adder graph (RAG-n) to exploit redundancy between coefficients decomposition. The algorithm was named Bull-Horrocks-Modified (BHM) algorithm in subsequent works. The main disadvantage of BHM algorithm is the increasing of the logic depth (LD), i.e. number of cascaded adders/subtractors. Other methods that use dependence graphs are Pasko's [6], CRA [7], HCUB [8].

A different approach is based on finding common subexpressions between binary representation of filter coefficients. Generally, the common subexpressions extracted from filter coefficients are grouped in a premultiplier block (PB) and then combined in the multiplier block (MB) to build the filter coefficients as it can be seen in Fig. (**??**). The accumulator block (AB) completes the transpose architecture. Hartley [9] proposed a common subexpression elimination (CSE) algorithm based on CSD representation. The main advantage of CSE based algorithms is that a more regular layout can be obtained regards to those GD based. In order to increase the common subexpression found given a coefficient set, different alternatives have been developed. Park and Kang [10] proposed to use minimal signed digit representation (MSD) instead of CSD. Given a constant, MSD produces a number of representations with the same number of nonzero digits as CSD but increases the common subexpression searching set. Martínez-Peiró et. al [11] suggested the NR-SCSE algorithm allowing a structure that can be easily synthesized into hardware with the objective of improving routability and reduce LD. In NR-SCSE, vertical subexpressions neither super subexpressions are considered allowing to reduce LD and increase the operation frequency.

Our election for an adequate FIR filter minimization algorithm to be implemented in a software tool was having in mind routability, LD and low programming effort. Because of these concerns, FIRSynth implements the NR-SCSE algorithm.

II. Architecture

The selected architecture.

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