Size saving FFT core for OFDM comunications

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***Abstract*—Two FFT architectures are presented. The architectures are based in the Radix algorithm. In particular, a radix-2 and a radix-4 are implemented.**
The main objetive is to achieve a very small architecture, in terms of the resources/space demanded by the core, keeping the performance of a regular FFT core. That restriction is due to compliance the specifitacions of a ISDB-t oriented OFDM modulator, which will be the final use of the core.
Radix algorithm has been selected becasue it provides high modules re-utilization, implemented over an iterative structure, using only one butterfly module, one multiplier and one memory. In that scheme, the main complexity is in the control unit and the datapath.
The design was made in Verilog hardware description language and the test scripts were made in Matlab scripting language.

I. Introduction

The continuous growing demand for speed in telecomunications leads to the implementation of faster transmision systems.
One of the most used data transmision systems is Orthogonal Frecuency Division Multiplexing, *OFDM* [2], which uses multiple carriers to modulate the transmited data.
The main difference between the traditional frecuency multiplexing systems and OFDM is that in in the last one the carriers are overlapping, taking advantage of their orthogonality as seen in Fig. (1), in oposition to the traditional system where the carriers have a gap between them to prevent inter-carrier interference.

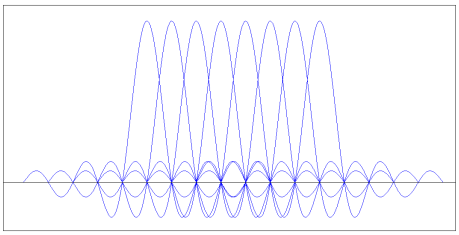

Fig. 1. OFDM sub-carriers scheme

The basis of the OFDM transmision is the sum of sub-carriers (wich can be expressed by a complex exponential, or a *frequency* in the complex plane) multiplied by the data complex symbols. Matematically, it is expressed as seen in equation (1)

$$s_k(t-kT) = w(t-kT)\sum_{i=-N/2}^{N/2-1} x_{i,k} e^{j2\pi\left(\frac{i}{T_{FFT}}\right)(t-kT)} \quad (1)$$

where k is the sub-carrier number. It's easy to recognize in this equation the form of an Inverse Discrete Fourier Transform (where the points in the frequency domain are translated to the time domain).
Using this, the OFDM modulator bank can be replaced by the computation of a IDFT and the demodulator bank by the computation of a DFT, making it possible to implement an OFDM modulator/demodulator using a mathemathic computing core. It's even possible to make the implementation more optimal by the use of efficient IDFT/DFT algorithms known as Fast Fourier Transform.

The objetive of this work is to obtain an FFT computing core, small enough to be included in a complete OFDM transeiver without consuming to much resources or space, but efficient and accurate enough to be usefull in an ISDB-t television system.

II. Architechture selection

There are several algorithms for FFT calculation. Each has some advantages and disadvantages. As we are trying to achieve the smallest implementation, the radix-r algorithm is selected beacause of it's particularity of using equal modules in every step of the transform [1].
Radix-r algorithms are a variation of Cooley-Tukey algorithms [3]. Radix-r factorices the FFT length, N, in the form of $N = r^\nu$, so the N-point FFT is decomposed in ν r-points sub-FFTs. The main advantage of the factorization in r is that the computation module can be replied or reused for each sub-FFT calculation.

A. Radix-r Algorithm

This algorithm is based in the factorization of the FFT the length N through the bidimentional mapping:

$$n = N_2 n_1 + n_2 \qquad \begin{cases} 0 \le n_1 \le N_1 - 1 \\ 0 \le n_2 \le N_2 - 1 \end{cases} \quad (2)$$

$$k = k_1 + N_1 k_2 \qquad \begin{cases} 0 \le k_1 \le N_1 - 1 \\ 0 \le k_2 \le N_2 - 1 \end{cases} \quad (3)$$

where n is the time domain index and k is the frequency domain index, and $N = N1 * N2$.
Expressing the DFT and IDFT in the forms of equations (4) and (5)

$$X[k] = \sum_{n=0}^{N-1} x[n] W_N^{kn} \tag{4}$$

$$x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] W_N^{-kn} \tag{5}$$

where $W_N^{kn} = e^{\frac{-j2\pi kn}{N}}$ are known as *twiddle factors*, n and k can be replaced by (2) and (3), wich in (4) results in:

$$X[k1, k2] = \sum_{n_2=0}^{N_2-1} W_{N_2}^{n_2 k_2} \left(W_N^{n_2 k_1} \sum_{n_1=0}^{N_1-1} x[n_1, n_2] W_{N_1}^{n_1 k_1} \right) \tag{6}$$

The inner summation in (6) is a N_1 points DFT multiplied by the factor $W_N^{n_2 k_1}$. Taking $\tilde{x}[n2, k1] = W_N^{n_2 k_1} \sum_{n_1=0}^{N_1-1} x[n_1, n_2] W_{N_1}^{n_1 k_1}$ and replacing in (6):

$$X[k1, k2] = \sum_{n_2=0}^{N_2-1} W_{N_2}^{n_2 k_2} \tilde{x}[n2, k1] \tag{7}$$

(7) shows the N_2 points $\tilde{x}$ DFT. It demostrates the power of the algorithm by replacing an N point DFT with two smaller sequential DFT.

Here we can subdivide the sub-DFTs applying the described method in turn to reduce the original DFT to several sub-DFTs of smaller length and simpler to operate.

An extra advantage of this algorithm is the posibility of in-place memory using, where the results of an operation is holded in the memory position of the operands, so for a N point DFT, N length memory is needed.

The value of r affects the type and quantity of operations needed, as can be seen in table I.

r	Multiplications	Non trivial multiplications	additions
2	2	0	2
3	3	2	6
4	4	0	8
5	6	5	17
7	9	8	36

TABLE I. OPERATIONS NEEDED BY DIFFERENT VALUES OF *r*

For $r = 2$ and $r = 4$ there aren't non trivial multiplications, so this are the values chosen for r.
A radix-r FFT has $log_r N$ stages. As table I shows, for $r = 4$ more operations per stage are needed but there are half the stages than for $r = 2$. Both are implemented in order to compare them and bring the posibility to choose depending on the requirements of the specific application.

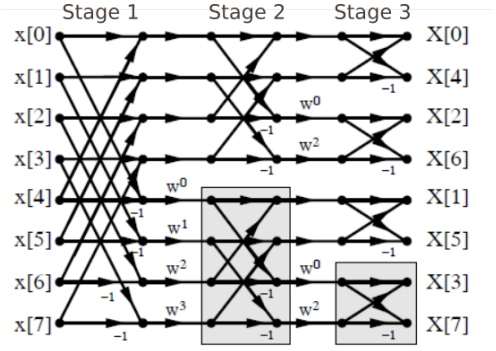

Fig. 2. 8 points Radix-2 FFT

B. Implementation of the Radix-r architechture

Figure 2 shows the simplified scheme for 8 points radix-2 FFT.

Each node represents an addition and the arrows represents the multiplication by the value over it. The figure shows the stage division of the algorithm, each of them performing a 2 points DFT.
In general, for a N points DFT $\frac{N}{2} * \log_2(N)$ butterflies and $\frac{N}{2} * (\log_2(N) - 1)$ complex multipliers are needed. There are different implementations for the radix algorithms wich provides optimizations in different aspects of the performance. Possible implementations are:

- **Parallel** All *butterfly* and multipliers are implemented in similar scheme as the one showed in Figure (2).
- **Unrolled** Single Delay Feedback (SDF) architechture [4]. Uses a *butterfly* and a complex multiplier per stage.
- **Iterative** Only one *butterfly* and one complex multiplier, used secuencially by all the stages. Figure (3) shows an 8 points iterative radix-2 FFT scheme.

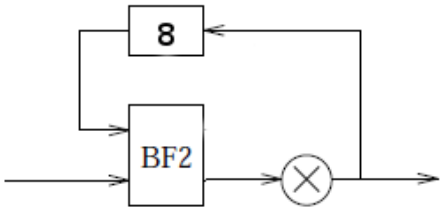

Fig. 3. Iterative Radix-2

Table (II) shows the comparision of characteristics of the three implementations descrived above.

Characteristic	Parallel	Unrolled	Iterative
# *butterfly*	$\frac{N}{\nu} * \log_\nu(N)$	$\log_\nu(N)$	1
# multipliers	$\frac{N}{\nu} * (\log_\nu(N) - 1)$	$log_\nu(N) - 1$	1
Memory length	0	$N - 1$	N
Bus type	Parallel	Serie	Serie
throughput	N points per cicle	1 point per cicle	1 per $\log_\nu(N)$ cicles
pipeline	Yes	Yes	No

TABLE II. COMPARATIVE BETWEEN PARALLEL, UNROLLED AND ITERATIVE RADIX-R

In order to ensure the low space and low resource requirement, iterative implementation has been chosen.

C. Twiddle factors multiplication

Radix algorithms require the multiplication by twiddle factors. Is well known that multiplications in digital implementation are expensive, spacial and temporaly. So to choose the better alternative needs a carefully analisys.

Three methods were analised:

- Cordic Algorithm
- BKM Algorithm
- Efficient complex multiplication

1) Cordic Algorithm: Twiddle factors have the form $W_N^{kn} = e^{\frac{-j2\pi kn}{N}}$. So they represent a rotation in the complex axis. A well known and well proved algorithm for rotations is the cordic algorithm [5]. It is based on successive aproximations by micro-rotations until the desired angle is reached.
The main advantage of this algorithm is that it only uses additions (and substractions) and shifts, both of them very cheap in terms of resources. Also it can be pipelined, improving the speed of processing.

2) BKM Algorithm: Like the cordic algorithm, it resolves elemental equations using only additions and shifts.
In comparition with Cordic Algorithm, BKM requires more storage and is more complex. In addition, it's greater efficience is obtained using redundant numeric system, wich is not the case of the present work. Because of this reasons, BKM is discarded for this project.
For more information about BKM algorithms refer to [6].

3) Efficient Complex multiplier: Cordic algorithm is widely used in FFT calculation because of its very low cost in terms of space and resources. But in an iterative implementation, where only one multiplier is required, the difference between the cordic core and a complex multiplier is very little.
For twiddle factors, the multiplication required is:

$$R+jI = (A+jB)*(C+jD) = (A*C-B*D)+j(A*D+B*C) \tag{8}$$

where $(C+jD)$ is the twiddle factor. A straight implementation would need four multipliers, but pre-calculating some of the factors and storing them in memory (as the $tg\theta$ in cordic) can reduce the implementation to three multiplications.
Pre-calculated factors are C, $(C+D)$ and $C-D$. Then, pre-calculated values are used to obtain $Z = Cx(A-B)$ and then:

$$R = (C-D) \times B + Z \tag{9}$$

$$I = (C+D) \times A - Z \tag{10}$$

Taking into account that several FPGAs have DSP integrated modules, the implementation of multipliers could be very efficient.

D. Summary of implementation

As it has been exposed in this section, the following architechtures are implemented:

- Radix-2 iterative architechture.
- Radix-4 iterative architechture.
- Cordic algorithm for twiddle factors multiplications, for radix-2 and radix-4.
- Efficient complex multiplier for twiddel factors multiplications, for radix-2 and radix-4, as an alternative to cordic algorithm.

III. Radix-2

In Figure (2) are shown the different stages of radix-2 FFT implementation.
On each clock cicle, one of two posible operations can be performed:

- A point is stored in memory while another point is sended from memory to twiddle factor multiplier or to the core output.
- A butterfly operation between a core-input point or last-stage point and a memory-stored point. Two points results from the butterfly operation: one is stored in memory while the other is sended to the twiddle factor multiplier or to the output.

Main components of the core are: N point memory, butterfly, multiplier an the control unit.

A. Memory

Due to the type of memory operations simultaneous store and read datais needed, so the memory unit is implemented as a dual-port RAM memory of length N.

B. Butterfly

The butterfly unit has to perform the two-operands complex operations:

$$\begin{aligned} c &= a + b \\ d &= a - b \end{aligned} \tag{11}$$

C. Control Unit

The control unit has to set the multiplexers according to the operation that is performed in that clock cicle, address the memory to the position where the actual operand has to be readed or stored and generate the twiddle factors for the multiplier.
Given that the core has $log_2(N)$ stages, the control unit has a stage-counter with length $log_2(log_2(N))$. Another counter, with a length of $log_2(N)$ counts the number of points that have entered into the core by that moment. A state machine is controlled with these counters, and controls the architecture in base of the stage and point number.

D. Integration

Figure (4) presents the integrated core. Control unit signal are showed as arrows to keep the graphic clear.
An additional register is placed before the multiplier because one result of a given stage is used in the following stage, so it must be keeped for one clock cicle. Another register is placed in the output in order to bring secuencial sinchronization with the circuit connected to the core.
An optional rounding/clipping unit is provided after the butterfly to give a method to deal with overflow. This can be turned on selectivelly for each stage in real time.

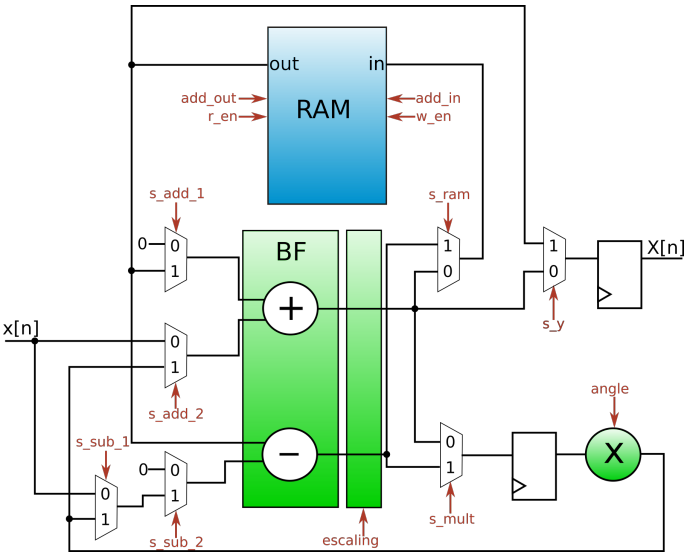

Fig. 4. Datapath with control signals

IV. Radix-4

Radix-4 algorithm divides a N-point DFT in ν 4-point DFT, so that $N = 4^{\nu}$.
The following expressions resumes the operations that the radix-4 has to process [3]:

$$y_n = (x_n + x_{n+\frac{l}{4}} + x_{n+\frac{l}{2}} + x_{n+\frac{3l}{4}}) \tag{12}$$

$$z_n = ((x_n - x_{n+\frac{l}{2}}) - j(x_{n+\frac{l}{4}} - x_{n+\frac{3l}{4}}))W_N^k \tag{13}$$

$$g_n = ((x_n + x_{n+\frac{l}{2}}) - (x_{n+\frac{l}{4}} + x_{n+\frac{3l}{4}}))W_N^{2k} \tag{14}$$

$$h_n = ((x_n - x_{n+\frac{l}{2}}) + j(x_{n+\frac{l}{4}} - x_{n+\frac{3l}{4}}))W_N^{3k} \tag{15}$$

for $k = 0, 1, \ldots, \frac{N}{4} - 1$, where l depends on the current processing stage. Figure (5) shows the operatinal scheme of a 16-points radix-4 algorithm.

On each clock cicle, one out of four posible operations is performed:

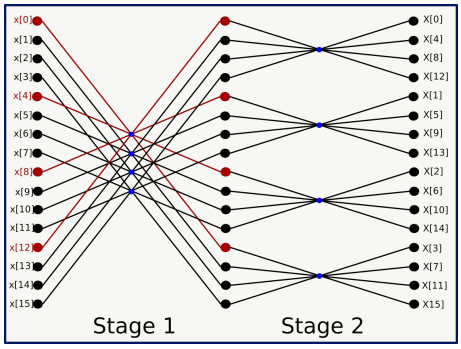

Fig. 5. 16 points Radix-4 FFT diagram

- A point is stored in a memory sub-block from the core input or the twiddle factor multiplier, while another point is sent from the same memory sub-block to the multiplier or the output. For every sub-block, a different operation is considered.
- An arithmetic operation is performed with a point from the core input or the previous stage and 3 points from memory, each from a different memory sub-block.

Main components are the memory, the aritmetic unit (called dragonfly), multiplier and the control unit, specially designed for radix-4.

A. Memory

Each arithmetic operation needs 4 operands, one coming from the core input or the previous stage and another 3 coming from the storage, so a 3-way in/3-way out memory is needed. In order to take advantage of memory blocks present in most FPGAs, a special memory is designed for this core. It is formed by 3 dual-port RAMs similar to radix-2 memories, so in each arithmetic operation, an operand of each memory sub-block can be readed and stored simultaneously.
As the directions may not be succesive, because in each clock cicle a different stage operation is performed, each sub block is divided in ν regions delimited by addresses. Sub-block lenght decreases successively in the form $N/4$, $log_4(N/4)$, $Log_4(Log_4(N/4)) \ldots 1$.

B. Dragonfly

The arithmetic unit performs the equations (12) to (15), wich are directly implemented in the logic.
In each stage two different types of operations can be performed: a four point arithmetic calculation or a memory data traslation. In the last case, a point from a memory sub-block is trasferred to the multiplier, while a point is stored in the next stage memory sub-block region. The dragonfly unit includes an inner datapath wich guides the data according to the operation in progress.

C. Control unit

As well as in radix-2, the control unit configures the datapath and generate the memory addresses and the twiddle factors for the multiplier. As in radix-2, two counters are used: a $log_2(N)$ length points counter and a $log_2(log_4(N))$ length

stage counter. Determining wich operation must be perform in a given clock cicle is done by evaluating the pair of the point counter's bits refered by the value of the stage counter.
Memory addressing is done by mapping directly the point counter to the memory address. The sub-block region is selected with the stage counter because each sub-block is subdivided in regions for each stage. The read and write control signalas are controlled according to the type of operation: in memory transfer operations only one sub-block is enabled while in arithmetical operations all three sub-blocks are allowed to be readed and writed.

D. Integration

Figure (6) presents the iterative radix-4 core. As in radix-2, extra registers are added after arithmetic unit and in the output. Also the rounding/clipping unit is added to the dragonfly to prevent overflow.

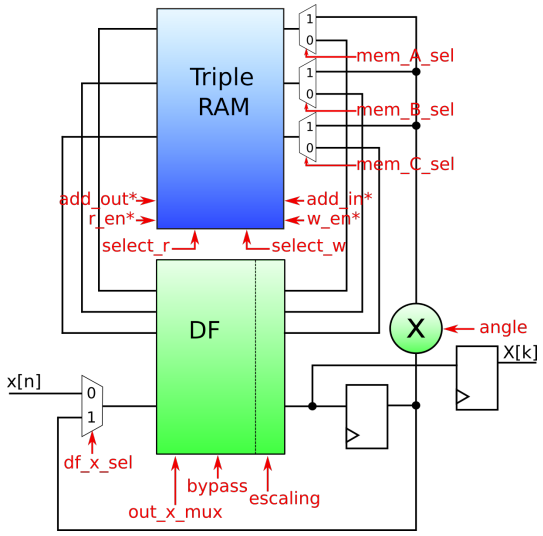

Fig. 6. Datapath with control signals

V. Architecture Characterization

Beside of the individual tests for every composing unit, a set of tests is made over the entire architectures in order to verify and validate the design.
For a complete description of tests and results, refer to [9].

A. Standard signals

First, a set of standard signals is applyed to the cores, and the result is compared to the expected result. The cores are configurated in IFFT mode. The signals are:

- Delta in frequency component '0'. Expected a continuous signal.
- Delta in frequency component 6. Expected six cicles of a sin.
- Sin of period N/6. Expected a delta in time component 6.

All the tests were passed correctly.

B. Error measurement

In order to measure the architecture error, Matlab fft is taken as a benchmark because it operates with 64 bits floating point numbers.

Two metrics are used for error measuring, E_∞ and E_2:

$$E_\infty = MAX(\frac{X_o[n] - X_{dut}[n]}{X_o[n]}) \tag{16}$$

$$E_2 = \|\frac{X_o[n] - X_{dut}[n]}{X_o[n]}\|_2 \tag{17}$$

It's important to note that the radix architectures are non lineal, so every test consists of 1024 simulations with random vector inputs. In each simulation, the result of the core computation is compared with Matlab result to obtain the error. After the 1024 simulations, error values are promediated to obtain the final error values.
This is done for 12 and 16 bit implementations of radix-2 and radix-4 cores. This is because 12 bits is a standard word length in OFDM comunication systems and 16 bits is a standard in signal processing. Also cordic and complex multiplier versions are tested, in order to comparate their performance.
As an extra test bench, a widely used, 16 bit integer C++ FFT core is tested [7].

	1024, 12 bits	1024, 16 bits	4096, 12 bits	4096, 16 bits
Radix-2, Cordic	0.092	0.006	0.099	0.008
Radix-2, Mult.	0.232	0.003	0.340	0.108
Radix-4, Cordic	0.077	0.003	0.074	0.007
Radix-4, Mult.	0.224	0.002	0.334	0.105
Kiss FFT		0.017		0.035

TABLE III. E_∞ FOR 1024 SIMULATIONS WITH RANDOM INPUTS

	1024, 12 bits	1024, 16 bits	4096, 12 bits	4096, 16 bits
Radix-2, Cordic	0.095	0.007	0.116	0.053
Radix-2, Mult.	0.257	0.004	0.356	0.131
Radix-4, Cordic	0.084	0.002	0.094	0.027
Radix-4, Mult.	0.258	0.003	0.358	0.126
Kiss FFT		0.017		0.035

TABLE IV. E_2 FOR 1024 SIMULATIONS WITH RANDOM INPUTS

In tables III and IV is clear that performance of the cores is perfectly suitable for OFDM systems. Moreover, the cores can be used in signal processing as the error is under 1%. For complex multiplier the error can be cutted down by increasing the word length of the factors stored in memory. For Cordic rotator, the error can be cutted down by adding rotation steps.

C. THD

In order to measure the THD of the architectures, 16 test are performed. One for each architecture, radix-2 or radix-4, for all flavours described before: 12 or 16 bits, 1024 or 4096 points and cordic or complex multiplier for twiddle factors. Additionally, THD test is made over KISFFT to get a testbench.
Each test run consecutive simulations that use as input a tone in every input point each time. That way, a graphic can be made with the armonic response to every frequency tone. Figures (7) to (8) shows some of the results.

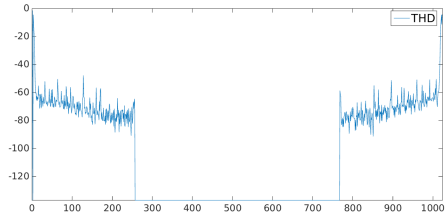

Fig. 7. Radix-2, Cordic, 12 bits

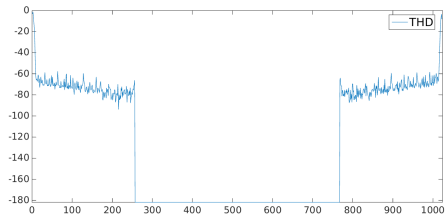

Fig. 8. Radix-4, Cordic, 12 bits

D. Test on Hardware

For hardware validation, a Xilinx XC5XVL110 Virtex-5 FPGA is used. 1024 points, 12 bits iterative radix-2 and radix-4 are sinthesized with Xilinx ISE v13.4 and routed into the FPGA along with a testbench circuit wich provides PC connection via a UART port.
Standard signal and error tests, described above, are repeated on the hardware implementation obtaining same results as simulation tests, providing the succesfull on-hardware validation of the cores.

E. Resource ocupation

The main requirement for the design is the low space/resource ocupation. In order to validate this requirement accomplishment, 1024 and 4096, 16 bits, iterative radix-2 and radix-4 architectures are sinthesized. To have a comparative reference, a 16 bits radix-2 sdf is implemented for 1024 and 4096 points. Also, as a rigorous testbench, Xilinx's LogiCORE FFT v7.1 [8] is sinthesized.

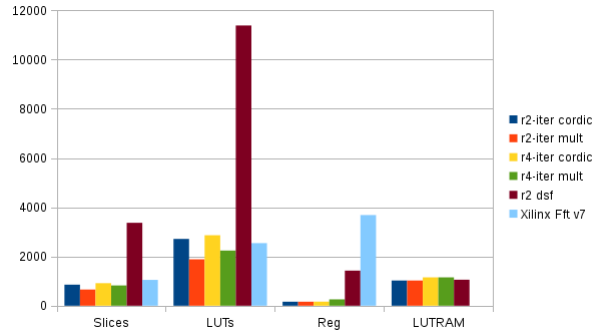

Fig. 9. Size/resource comparitionComparativa for 1024 points FFT

Figures (9) and (10) clearly shows that the designed cores are really small compared with another implementations, inclulding a propietary, device-optimized one like the LogiCORE FFT. Another important fact is that radix-4 and radix-2 needs

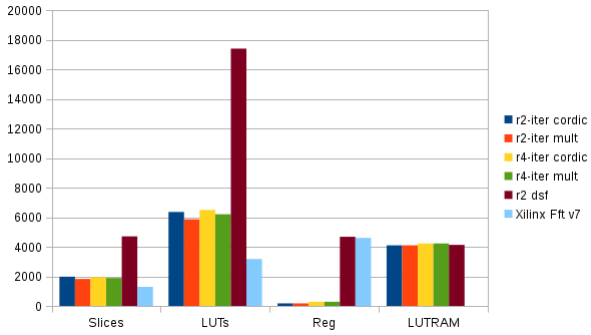

Fig. 10. Size/resource comparitionComparativa for 4096 points FFT

approximately the same resource quantity, but radix-4 has double the throughput than radix-2.

VI. Conclusion

This paper presented two iterative radix-r FFT computing cores, designed for OFDM comunication systems. Their main advantage is the extremly low space/resource comsuption, wich made them suitable for integration in large systems without impacting in the resource distribution, in case of FPGA implementation, or space in case of ASIC implementation. A complete description of the design and the verification and validation process has been presented.
A lot of effort was spent in the verification process in order to provide a useful ip core.
The architectures were implemented in Verilog HDL code. Also there were developed several testing tools comprising Matlab, C++ programs and Verilog testbenchs.
For future work, it can be considerated to add a dithering system, in order to reduce the noise generated by the architectures, and implement a pipelined cordic without modifing the global architecture timing, in order to improve the throughput.

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