Rangefinder Instrumentation

NASA's *Curiosity* rover: Self-portrait in Gale Crater on the surface of Mars (October 31, 2012).

Introduction

Almost all modern instrumentation uses electronics, because electronic building blocks are the most powerful, most versatile, most reliable, and lowest cost. Two broad categories can be distinguished: -

- Analog, for the generation of signals (ultimately, usually voltages) from physical transducers (sensors), often involving amplification; and sometimes for the control of some physical variable, e.g., holding a magnetic field at a constant value by supplying a wire-wound solenoidal coil with a constant current; or, more simply, switching (e.g.) a heater on or off.
- Digital, for a wide range of tasks. At its simplest, this might involve making straightforward (autonomous) decisions, as in the case of the Curiosity rover on Mars; but modern instrumentation often captures signals over time as a sequence of digital numbers, through the process of Analog-to-Digital conversion. It is then much simpler to carry out signal processing tasks, such as digital filtering, or linearizing non-linear transducers (e.g., thermistors, acting as thermometers), and then to display, or store, or to control, or otherwise to manipulate, the results of the measurements.

In both the Analog and Digital domains a number of powerful, but technologically generic, building blocks have evolved over time, and these are discussed below in the context of the Ultrasonic Rangefinder project, whose circuit diagram is shown in Figure 1. Notwithstanding this particular application, it should be appreciated that precisely these same generic building blocks and techniques were used in constructing, for example, the *Curiosity* Mars rover, and so where more generally applicable principles, or technological building-blocks, are encountered, the discussion has been broadened to cover these more fully.

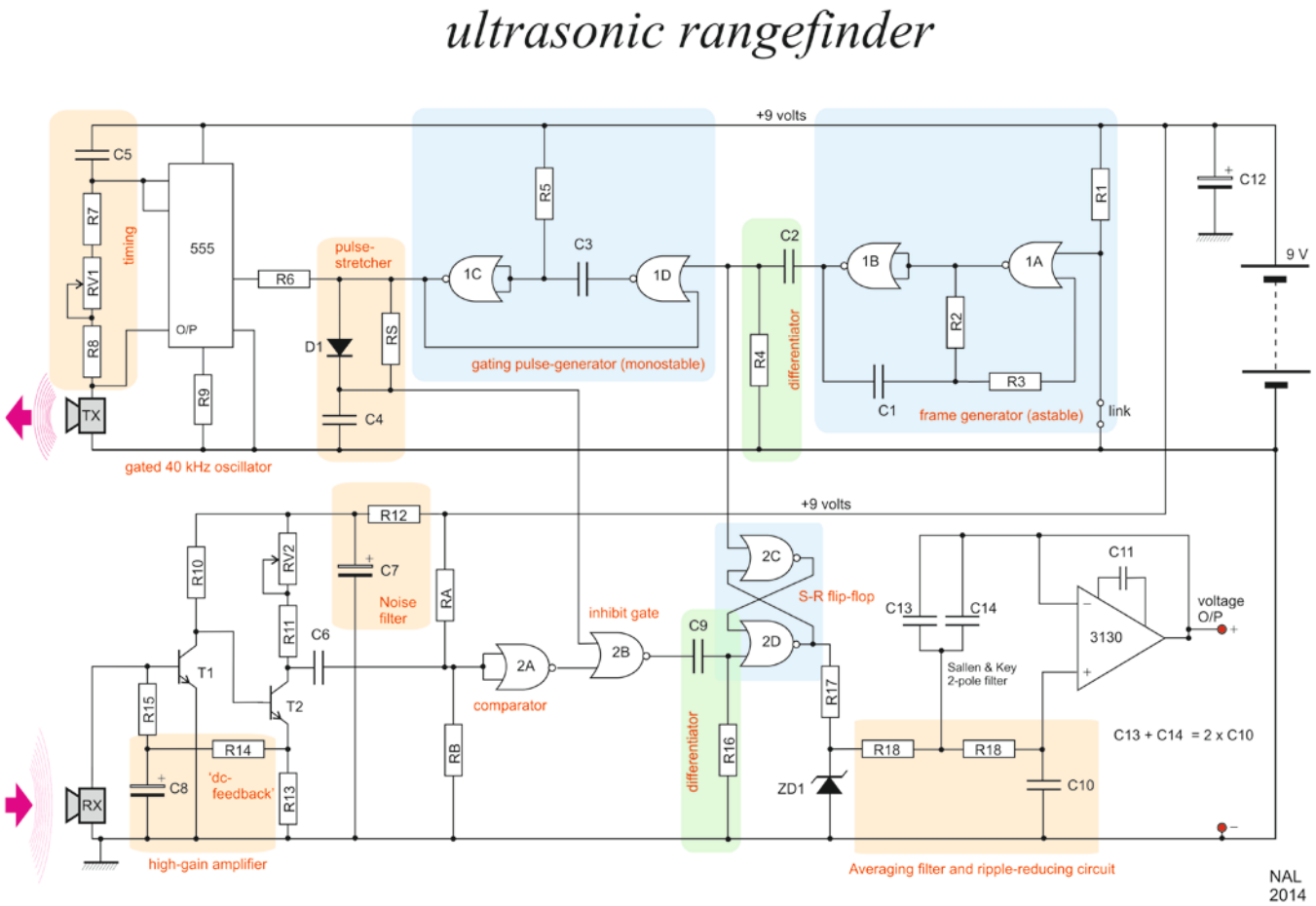


Figure 1. Circuit diagram of the Ultrasonic Rangefinder. TX: 40 kHz Transmitter; RX: Receiver. RC (low-pass) timing and filtering units are shown blocked in beige, pairs of NOR gates with feedback in pale blue, and differentiating units in pale green. The op-amp based filters have been treated with, and without, C13 and C14.

Analog electronics

This covers passive linear components, such as the resistor, capacitor, and inductor, and non-linear and active components, such as the diode, the transistor, and the operational amplifier.

Digital electronics

This covers logic gates (e.g., NAND, NOR, XOR), programmable microcontrollers, and, of course, personal computers, tablets, etc.

Modelling

Understanding the operation of both the Analog and Digital building blocks of instrumentation is made very much easier by replacing actual components and devices by simple equivalent physical models, and then by subjecting these models to a small number of over-arching, simplifying, principles: -

- The sum of voltage drops (say) around any closed path in a circuit equals zero, so that the sum of the voltage- (potential-) drops along any path connecting two locations ('nodes') in a circuit must be independent of the path taken connecting these points—this is Kirchhoff's Voltage Law. Often, one of these locations is called the circuit ground or circuit 'common', in which case an unambiguous voltage can be said to exist 'at' all other points in the circuit (understood, tacitly, to be measured relative to the circuit's ground, or zero, potential).
- Currents represent the flow of positive charge, and all currents must flow in loops.
- Following on from the preceding point: the sum of all currents flowing into a circuit 'node' must be zero—this is Kirchhoff's Current Law. Therefore, the total current flowing into a node must equal the total flowing out. Even when current flows into (say) the positive plate of a capacitor (so as to charge the capacitor), an equal current must flow out of the capacitor's negative plate. It is as if the same current flowed 'through' the notional, or actual, gap separating the two plates of the capacitor—which can be treated overall as if it were a single node in the circuit. Of course, the capacitor actually is accumulating equal and opposite charges on its two plates as a result of the current flow, so that, overall, it remains neutral.
- The behaviour of ideal 'voltage' and 'current' sources.
- ➢ The principle of superposition (used with linear circuits comprising resistors, capacitors, inductors, or a mixture of these, together with voltage and current sources. For example, the AC and DC behaviours of such circuits are most easily treated separately, and their separate results simply added together (superposed), in order to find the total voltage at a node, or the total current flowing in a conductor. AC analysis first requires the suppression of all DC sources, and vice versa.
- The 'equivalent' circuit (used with circuits comprising resistors, capacitors, inductors, or a mixture of these), which is a simplification of the actual circuit, but which behaves in exactly the same way as the real circuit from the point of view of the currents and/or voltages under consideration. Thévenin and Norton equivalent circuits are particularly useful: the Thévenin equivalent circuit replaces an actual complicated resistive circuit containing possibly multiple voltage and current sources by a single voltage source in series with a single resistance, whereas the Norton equivalent circuit replaces such a real circuit by a single current source in parallel with the same resistance. Equally, the 'hybrid-π' AC model of the bipolar transistor greatly simplifies the determination of, e.g., the AC voltage gain from input to output of a transistor-based amplifier.
- The concept of (complex) impedance, in terms of the complex frequency, s.

- The reciprocity of signals in the frequency and time domains: use of Laplace Transform techniques to solve (difficult) differential equations in the time domain 't' by transposing them into (simple) algebraic equations in the frequency domain, 's,' of the previous point. Algebraic solution in terms of the variable s then can be transposed straightforwardly back into the desired solutions as functions of time, t.

Three further simplifying assumptions

- The 'inputs' of integrated circuits (such as logic gates or op-amps) monitor and respond to the voltage levels applied to them by external circuitry, but these inputs draw (essentially) no current: they act like perfect voltmeters.
- The 'outputs' of integrated circuits (ICs such as logic gates or op-amps) act like ideal voltage sources: they source currents to, or sink currents from, any external, following, circuitry. For example: -

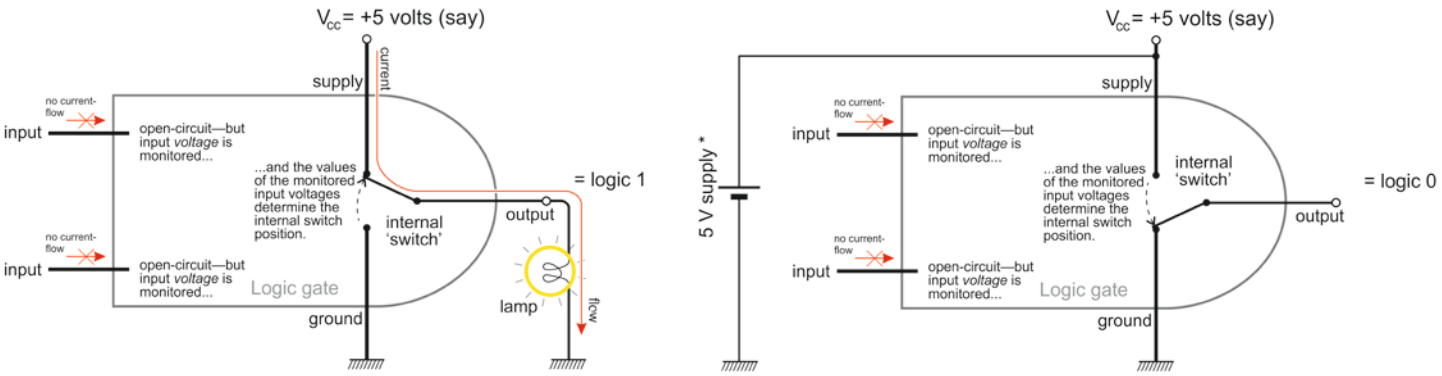


Figure 2. Digital Inputs and Outputs. Logic 1 output (≡ +5 volts, here) means the logic gate's output is connected internally to $+V_{cc}$, so current can flow to ground through an external 'load' connected to the output (here, a lamp); or, the output of the gate could be connected instead to resistor-capacitor 'RC' timing networks, or directly to the input(s) of one or more succeeding logic gates, supplying logic 1 or logic 0 input level(s) to this (these) gate(s). Logic 0 output means the logic gate's output is connected internally to ground. The internal 'switch' uses transistors. *Note that in the case of logic gates the necessary supply and ground connections frequently are not shown, explicitly.

- Negative feedback around an operational amplifier forces the op-amp's 'inverting' input (having the '–' sign) to follow the voltage applied to its non-inverting input (that having the '+' sign) by external circuitry — frequently to within microvolts !! Therefore, if an op-amp's non-inverting input is connected directly to ground, or zero volts, say, then negative feedback (from the op-amp's output to its inverting input—via a resistor connecting these two points, say) will force the inverting input also to be at zero volts, even though this node is *not* connected to ground: it is called a 'virtual Earth,' and is very useful in, e.g., optical instrumentation employing photodiodes, as shown in the following 'transimpedance amplifier' example (here, OPA is an op-amp, and 'E' is the virtual Earth point).

Transimpedance amplifier example: turning a photocurrent into a voltage

In this example the photodiode in Figure 3 is reverse biased by 15 volts. Therefore, apart from a negligible thermally- induced 'dark current', no current will flow through the photodiode (PD) in the absence of illumination (it acts like an ordinary *diode*). However, in the presence of a source of light a photocurrent i_{photo} will be generated within the photodiode detector, and this current will be directly proportional to the irradiance of the light incident on the detector. This photocurrent flows through the photodiode from the virtual Earth point 'E' to the –15V 'voltage supply rail'—which, together

with the +15V supply, also powers the op-amp, itself. Parenthetically, such a 'split power supply' allows the op-amp's (voltage source) output to swing potentially up to +15 volts, and down to –15 volts. Here, as a current of i_{photo} flows out of node E, an identical current must flow into this node—in this case flowing through the paralleled feedback components R_f and C_f. The (small) capacitor C_f is needed in practice in order to avoid potential high frequency oscillation in such a circuit, but at signal frequencies the photocurrent i_{photo} flows just through the resistor, R_f, this current being supplied by the voltage source output of the op-amp, as shown.

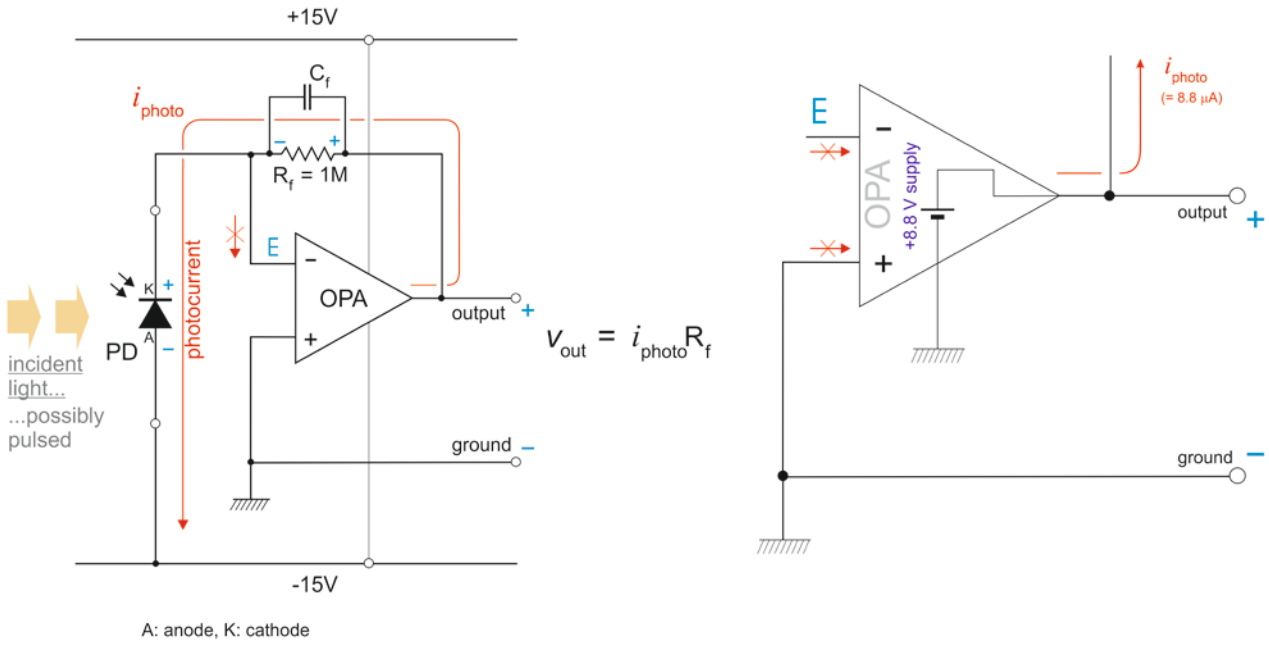


Figure 3. Analog Inputs and Outputs, and Negative feedback: which forces the voltage at the '-' to follow that at the '+' input. Transimpedance amplifier example. Left: light incident on the photodiode (PD) causes a photocurrent i_{photo} to flow, as shown. The operational amplifier (OPA) is powered here by a ±15 volt 'split' supply. As the op-amp's '+' input is connected to ground, the negative feedback (i.e., from the output to the '–' input: here, through R_f // C_f) causes the voltage at node 'E' to be held permanently at zero volts, too. Right: if the photocurrent = 8.8 μA (say), then the op-amp's internal voltage source will take up a voltage of +8.8 volts, so as to drive this level of current through R_f, the 1M feedback resistor. Therefore, the op-amp's output voltage = +8.8 volts — a direct analogue of the photocurrent.

As point E is at zero volts, the op-amp's internal voltage source must take up just that voltage which will cause a current of i_{photo} to flow (effectively to ground, at E) through the resistor R_f. Thus, if i_{photo} = 8.8 μA (say), then $V_{out} = i_{photo} R_f$, or V_{out} = 8.8 volts (since R_f = 1MΩ)—the output having the voltage polarity indicated. Alternatively, the cathode (K) of the photodiode could have been connected to the +15V rail, and its anode (A) could have been connected instead to the virtual Earth point at E. Once again, the photodiode would have a 15 volt reverse bias (useful for linearity, and speed of response). However, in this case the photocurrent i_{photo} would have flowed *into* the virtual Earth at E, it would have reversed its direction of flow through R_f, and it would have flowed into the output of the op-amp (now acting now as a current sink). Therefore, in this case the output voltage of the op-amp would have been V_{out} = –8.8 volts.

The potential divider and its Thévenin equivalent

One very important network, which is encountered very frequently in real circuits, is the *potential-divider*. Here, two (or more) resistors, connected in series, have a known total voltage-drop across them. In such a case, the voltage dropped across each resistor is in direct proportion to that

resistor's value, R (from Ohm's Law: V = IR), since the same current I flows through all of the series-connected chain of resistors. In the Figure below, part (a), the potential divider is made up from two resistors: R_A (= 20 kΩ), and R_B (= 10 kΩ), with a 12 volt supply impressed across them. Note that in what follows the 'open-circuit voltage' between the two circled nodes in the Figure means 'the voltage measured notionally between those nodes using a perfect voltmeter—*which draws no current*;' and the blue +/- signs in the Figure are reference polarities.

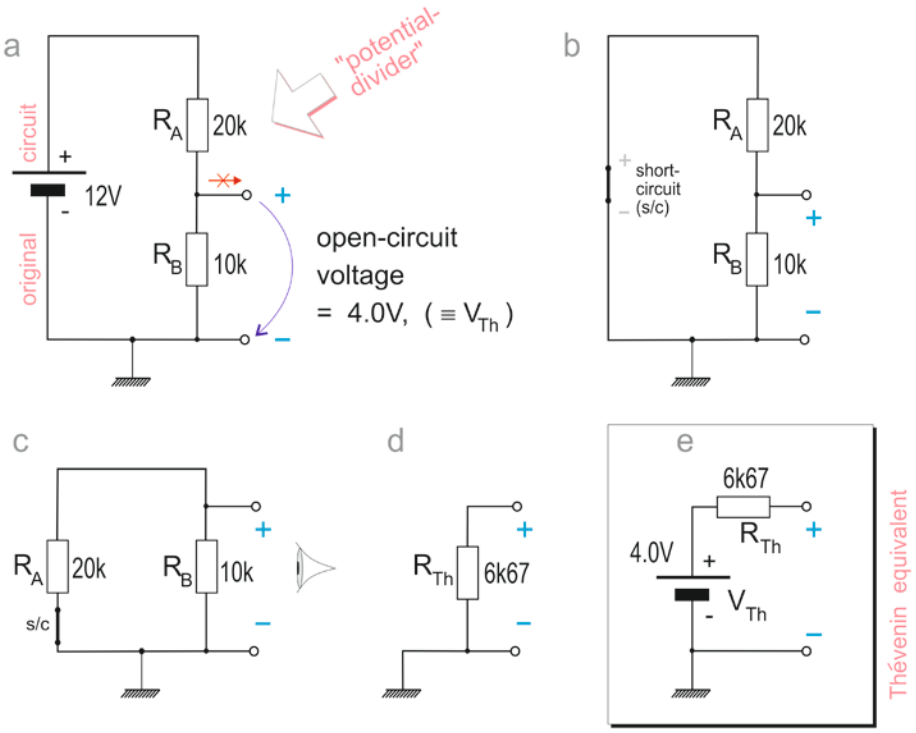


Figure 4. The potential divider circuit shown in (a) can be replaced by its simpler Thévenin equivalent, shown in (e) (please refer to the text).

Step 1. From the Thévenin equivalent circuit shown in (e): under open-circuit conditions no current can flow through the resistance R_{Th}; and so, under these conditions, neither can there be any voltage drop across R_{Th} (from Ohm's Law). Therefore, the open-circuit voltage of the Thévenin equivalent circuit (measured between the two circled nodes) must equal the voltage of the Thévenin source, V_{Th}. Since this circuit is to be the equivalent of the actual circuit, shown in (a), the open-circuit voltage of the actual circuit also must be V_{Th}. Therefore: find the open circuit voltage of the real circuit (or network) between the two nodes of interest (by using the potential-divider rule), and this voltage is equal to the value of the Thévenin equivalent voltage source, V_{Th}. In this example the potential-divider rule gives: -

$$V_{Th} = \left(\frac{10\text{k}}{10\text{k} + 20\text{k}} \right) \times 12 = 4.0 \text{ volts}.$$

Step 2. Again, from the Thévenin equivalent circuit shown in (e) above: if the Thévenin voltage source is suppressed (i.e., replaced by a short-circuit), then the resistance seen 'looking into' the two circled nodes is the Thévenin resistance, R_{Th}. Since this is to be the equivalent of the actual circuit, shown in (a), then if *all* voltage and current sources in the actual circuit are suppressed, notionally, then this action must lead to the suppression of the Thévenin equivalent voltage source, too. However, from the equivalence of the Thévenin and actual circuits, if all the voltage and current sources in the actual circuit are suppressed, then the remaining resistance that is 'seen' when looking

into the same two circled nodes must be equal in value to that of the Thévenin equivalent circuit, R_{Th}. Note that voltage sources must be replaced by short-circuits, and any current sources by open-circuits (breaks in the conductors), when notionally suppressing all of the sources in the actual circuit. So, in part (b) of the Figure, above, the single +12V source has been suppressed by replacing it with a short-circuit. This casts resistor R_A in parallel with R_B, both now being connected across the two circled nodes, as shown, redrawn, in (c). Therefore, the effective resistance seen between the nodes is: -

$$R_{Th} = \left(\frac{10\text{k} \times 20\text{k}}{10\text{k} + 20\text{k}} \right) = 6\text{k}67, \text{ or } 6.67\text{k}.$$

This is the value of the potential-divider's Thévenin equivalent resistance. Clearly, steps 1 and 2 may be reversed in order.

Thus the potential divider in (a) is actually a source of voltage V_{Th} = +4.0 volts in series with an effective resistance of R_{Th}= 6.67k, as shown in (e). The 6.67k is known, usually, as the potential-divider's *output resistance*.

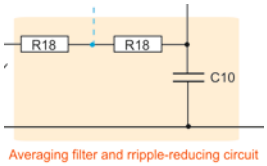
- In the Ultrasonic Rangefinder project a potential divider comprising a pair of resistors (designated R_A and R_B) may be used to set up a DC voltage (bias) at the input to a CMOS comparator—a NOR gate with its two inputs tied together, so as to form an inverter, or 'NOT' gate. The intention, here, is to provide a bias voltage slightly less than the comparator's sharp switching threshold, so that an amplified echo pulse—sitting on top of this DC level (by superposition)—will cause the *total* voltage at the input to the comparator to exceed the comparator's logic 0 –to- logic 1 switching threshold at its input, such that the NOT gate's output (normally logic 1) will make a logic 1 –to- logic 0 transition, causing the echo signal to be detected. However, since the potential divider and comparator follow the Rangefinder's (AC) echo pulse amplifier, the Thévenin equivalent circuit of the potential divider actually forms the amplifier's load. Ostensibly, this is an active load, since it comprises a resistance equal to (R_A // R_B) in series with a DC voltage source (equal to the bias voltage). However, in order to evaluate the effect of the potential divider on the AC voltage signal coming from the amplifier, the *DC bias voltage source* in the Thévenin model must be suppressed (following the concept of superposition), i.e., notionally replaced by a short circuit. Therefore, the AC load actually 'seen' by the AC echo pulse amplifier is in fact purely passive, with (here) an *input resistance* equal to (R_A // R_B). On the other hand, the AC echo pulse amplifier itself can be replaced by its own Thévenin model, which is an amplified AC echo pulse signal voltage source in series with a Thévenin output resistance (of approximately 20k). Therefore, the output resistance of the amplifier, together with the input resistance of the DC potential divider, form another potential divider—this time for the AC echo pulse signal voltage. In consequence, a much reduced level of echo signal actually may appear at the input to the comparator. For example, the recommended values of R_A = 47k and R_B = 33k, which are given in the bench notes for the Rangefinder project, effectively halve the size of the echo signal though this AC potential-division action—greatly reducing the effective range of the Rangefinder. One solution to this problem is (say) a 20-fold increase in the sizes of R_A and R_B, and so of (R_A // R_B).

RC circuits

Resistors and capacitors are frequently used together for timing purposes, the product of resistance and capacitance being a time. For example: 2 MΩ × 100 nF = 0.2 s, or 200 ms. The exponentially rising or falling waveforms generated by digital switching in logic circuits can be used, together with such RC circuits, to create 'astable' oscillators operating at a given frequency, or pulse generators of a given pulse width.

However, 'low-pass' RC circuits also can be used as averaging 'integrating' circuits, in order to generate mean (DC) values from waveforms having both DC and AC components; or 'high-pass' RC circuits can be used as 'differentiating' circuits that produce a sharp 'spike,' or pulse, from a digital switching transition—from one DC logic level to another.

RC Low-pass filter—step responses



Consider the 'RC' Resistor-Capacitor circuit below with a voltage step of amplitude V applied to its input at time t = 0. The capacitor C is assumed to be uncharged, initially.

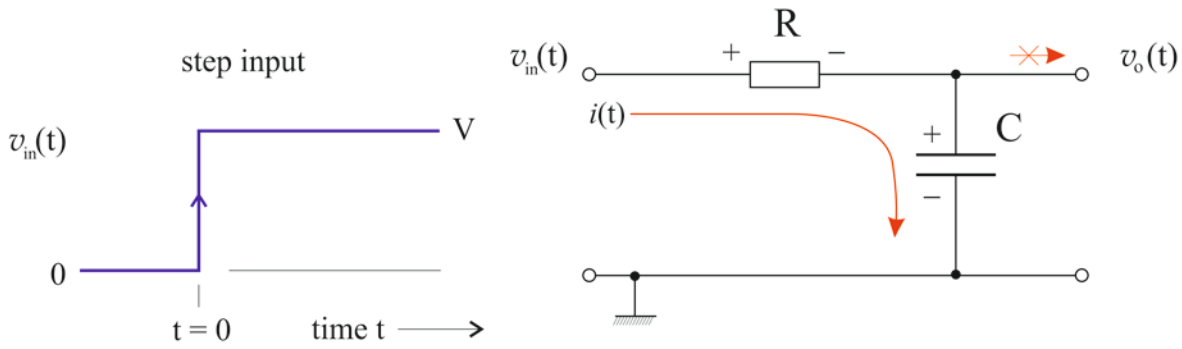


Figure 5. A voltage step input into a low-pass RC filter. $v_o(t)$ is the open-circuit output voltage (no current is drawn).

From Ohm's law the current through the resistor R is given by $i(t) = \dfrac{V - v_o(t)}{R}$, for $t \geq 0$.

This current also flows 'through' the capacitor, charging it up as shown, so that

$$i(t) = C\frac{dv_o(t)}{dt}. \quad \therefore \frac{V - v_o(t)}{R} = C\frac{dv_o(t)}{dt}, \text{ or}$$

$$RC\frac{dv_o(t)}{dt} + v_o(t) = V, \text{ for } t \geq 0. \tag{1}$$

The DE represented by eqn.(1) may be solved by first dividing through by RC, and then multiplying through by $e^{\int \frac{1}{RC} dt}$, so that the DE becomes separable.

Alternatively—and this is the more useful method for solving problems in instrumentation when a stimulus is 'switched on' (as here)—the DE may be solved using *Laplace Transform* techniques.

Let the Laplace Transform (LT) of the circuit's output voltage, $v_o(t)$, written as $\mathscr{L}\{v_o(t)\}$, be denoted by $V_0(s)$, where s is the 'complex frequency.' Then, following LT theory, we may write the following definition for the LT of the *derivative* of $v_o(t)$ with respect to time:-

$\mathscr{L}\left\{\frac{dv_o(t)}{dt}\right\} = sV_0(s) - v_o(t)\big|_{t=0}$ ...where the second term on the RHS of the equation is the initial condition (at t = 0) of the output.

Therefore the LT of both sides of equation (1) becomes:-

$RC\,\mathscr{L}\left\{\frac{dv_o(t)}{dt}\right\} + \mathscr{L}\{v_o(t)\} = \mathscr{L}\{V\}$; but for a constant (such as unity) $\mathscr{L}\{1\} = \frac{1}{s}$ (a standard LT identity), so that the LT of eqn.(1) becomes:-

$$RC\left[sV_0(s) - v_o(0)\right] + V_0(s) = \frac{V}{s} \qquad (2)$$

Since the capacitor in the circuit above is considered to be uncharged initially, the voltage across it at this time must be zero, and so $v_o(0) = 0$. Thus eqn. (2) reduces to a simple algebraic equation in the variable s, from which we find: -

$$V_0(s) = V\left[\frac{1}{s(sRC+1)}\right] \qquad (3)$$

Eqn. (3) can now be inverted to find the output voltage of the circuit as a function of time, $v_o(t)$, by taking the *inverse Laplace Transform* of $V_0(s)$. That is:-

$$\mathscr{L}^{-1}\{V_0(s)\} = v_o(t).$$

It is convenient to re-write eqn.(3) in terms of partial fractions, so that each fraction then may be inverted separately using standard LT identities. Thus:-

$$V_0(s) = V\left[\frac{1}{s} - \frac{RC}{(sRC+1)}\right] = V\left[\frac{1}{s} - \frac{1}{\left(s+\frac{1}{RC}\right)}\right]. \qquad (4)$$

Therefore, taking the inverse LT of both sides of eqn.(4):-

$\mathscr{L}^{-1}\{V_0(s)\} = v_o(t) = V\mathscr{L}^{-1}\left\{\frac{1}{s} - \frac{1}{\left(s+\frac{1}{RC}\right)}\right\}$. We may now use the LT identity $\mathscr{L}\{e^{at}\} = \frac{1}{s-a}$, or $\mathscr{L}^{-1}\left\{\frac{1}{s-a}\right\} = e^{at}$ on each of the partial fractions. Here 'a' is assumed to be a constant (with the dimensions of frequency). Noting that $\mathscr{L}\{1\} = \frac{1}{s}$, or $\mathscr{L}^{-1}\left\{\frac{1}{s}\right\} = 1$, leads to the required output voltage of the circuit as a function of time:-

$$v_o(t) = V\left[1 - e^{-t/RC}\right] \quad \text{(for } t \geq 0\text{)} \qquad (5)$$

RC is the 'time-constant' of the exponential charging curve shown in Figure 6...measured in [s]. Note that the tangent to the charging curve at t = 0 has a slope of $\left.\frac{dv_o(t)}{dt}\right|_{t=0} = \frac{V}{RC}$, from eqn. (5). Therefore the tangent construction shown in Figure 6 can be used in experiments to find the time-constant RC of the exponential. Note also that it takes approximately 5 time-constants for the exponential charging waveform to lie within 1% of its final, asymptotic, value: the capacitor charges, eventually, to the input step-voltage, V.

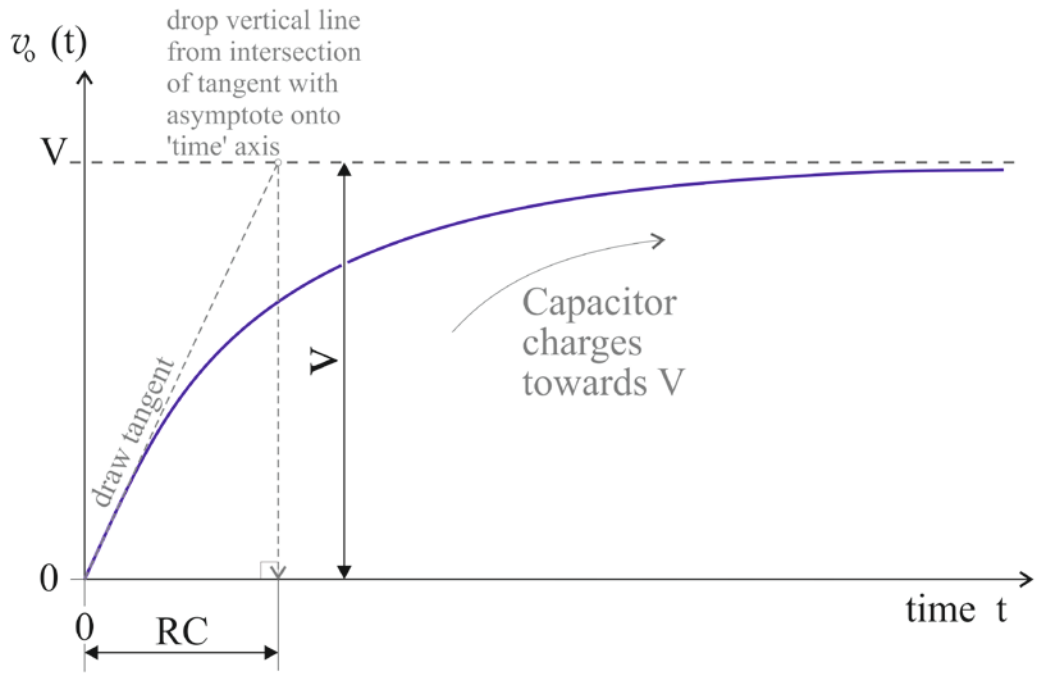


Figure 6. The output voltage response of an RC low-pass filter to a step-input of amplitude V volts, applied at time t = 0. A construction is shown for finding the time-constant (= RC) of the exponential rise towards the asymptotic limit of V volts.

For the case of a negative-step input, the input voltage has been assumed to be constant with a value of $v_{in}(t)$ = V for a period of many time-constants of the RC circuit, the step-down in voltage occurring at time t = 0.

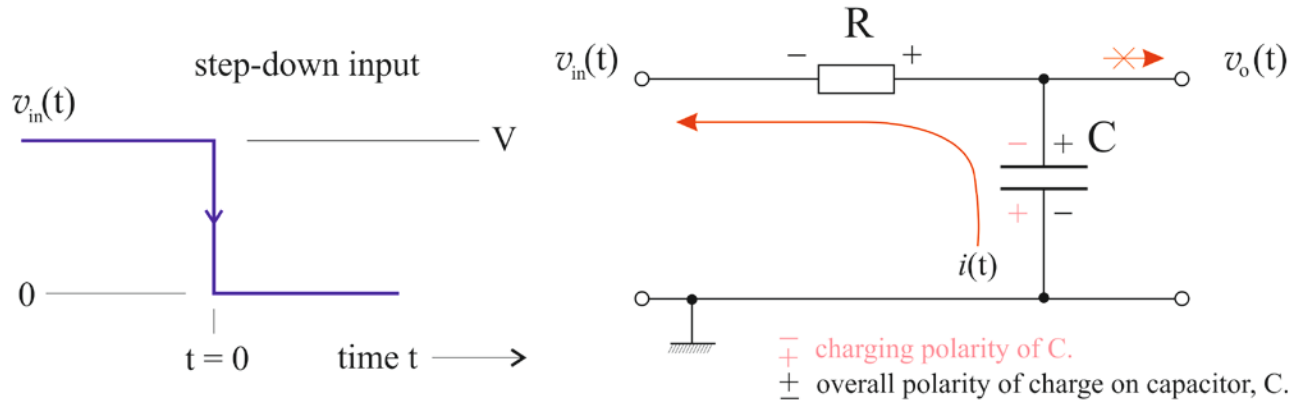


Figure 7. A step-down input into a low-pass RC filter. $v_o(t)$ is the open-circuit output voltage (no current is drawn).

Thus, the capacitor C was initially fully charged, to voltage V. Just after the step-down in input voltage to zero volts ($t = 0^+$), the left-hand side of the resistor R in Figure 7 is effectively connected to ground, whilst the right-hand side of this resistor is at a voltage $v_o(t)$ = V (the initial, charged, voltage of the capacitor). Therefore, the voltage-drop across resistor R has the polarity shown, and from Ohm's Law this causes a current $i(t)$ to flow through it [$i(t)$ = V/R, at that instant], *and so 'through' the series-connected capacitor, C, as well*.

Charge therefore accumulates on the capacitor with the polarity indicated in pink in Figure 7, which increasingly cancels the original charge, indicated in black: the capacitor is being *discharged*, and the voltage across it, and so also across resistor R, decreases over time. This process stops when there is no charge left on the capacitor, and the voltage across resistor R (and capacitor C) has reached $v_o(t)$ = 0: at this point, $i(t)$ = 0, and no further discharging current flows.

Upon taking the LT of eqn.(1), with the RHS of the eqn. (the input voltage) equal to zero for t > 0, we have

$RC[sV_0(s) - v_o(0)] + V_0(s) = 0$, with the initial condition, here, that $v_o(0) = V$—the initial voltage across the capacitor (which was fully charged to this voltage, initially). Thus

$RC[sV_0(s) - V] + V_0(s) = 0$, or $V_0(s) = \frac{VRC}{sRC+1}, = \frac{V}{s+\frac{1}{RC}}$. Taking the inverse LT of both sides of the eqn.:-

$\mathcal{L}^{-1}\{V_0(s)\} \equiv v_o(t) = V.\mathcal{L}^{-1}\left\{\frac{1}{(s+\frac{1}{RC})}\right\}$. Therefore:-

$$\boxed{v_o(t) = V.e^{-t/RC}} \quad \text{for } (t \geq 0) \qquad (6)$$

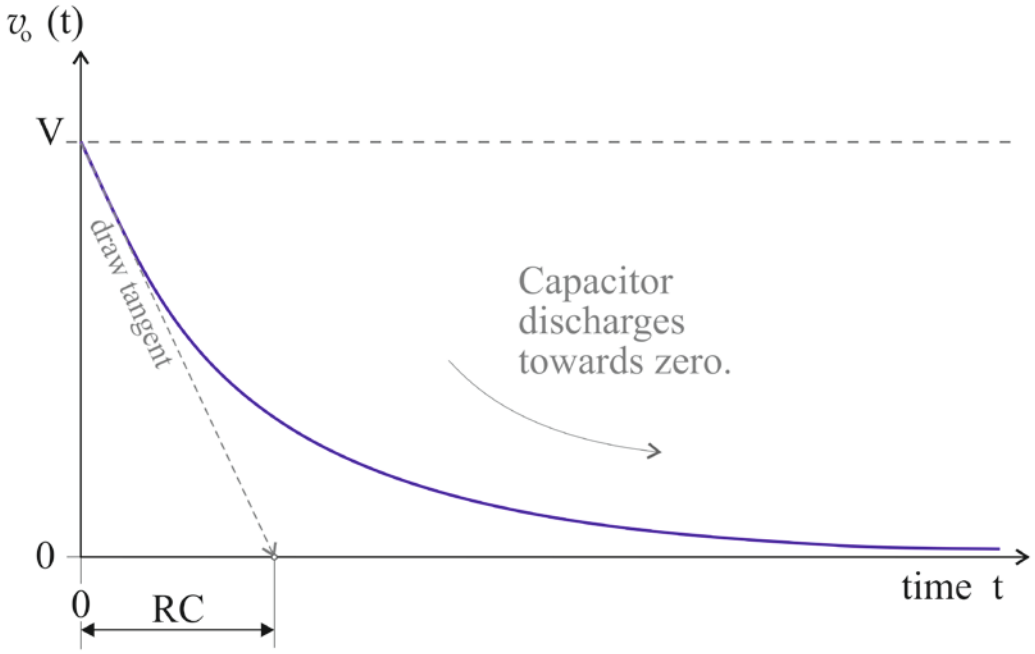


Figure 8. The output voltage response of an RC low-pass filter to a step-down input going from V to zero volts, applied at time t = 0. A construction is shown for finding the time-constant (= RC) of the exponential fall towards the asymptotic limit of zero volts.

RC High-pass filter—step responses

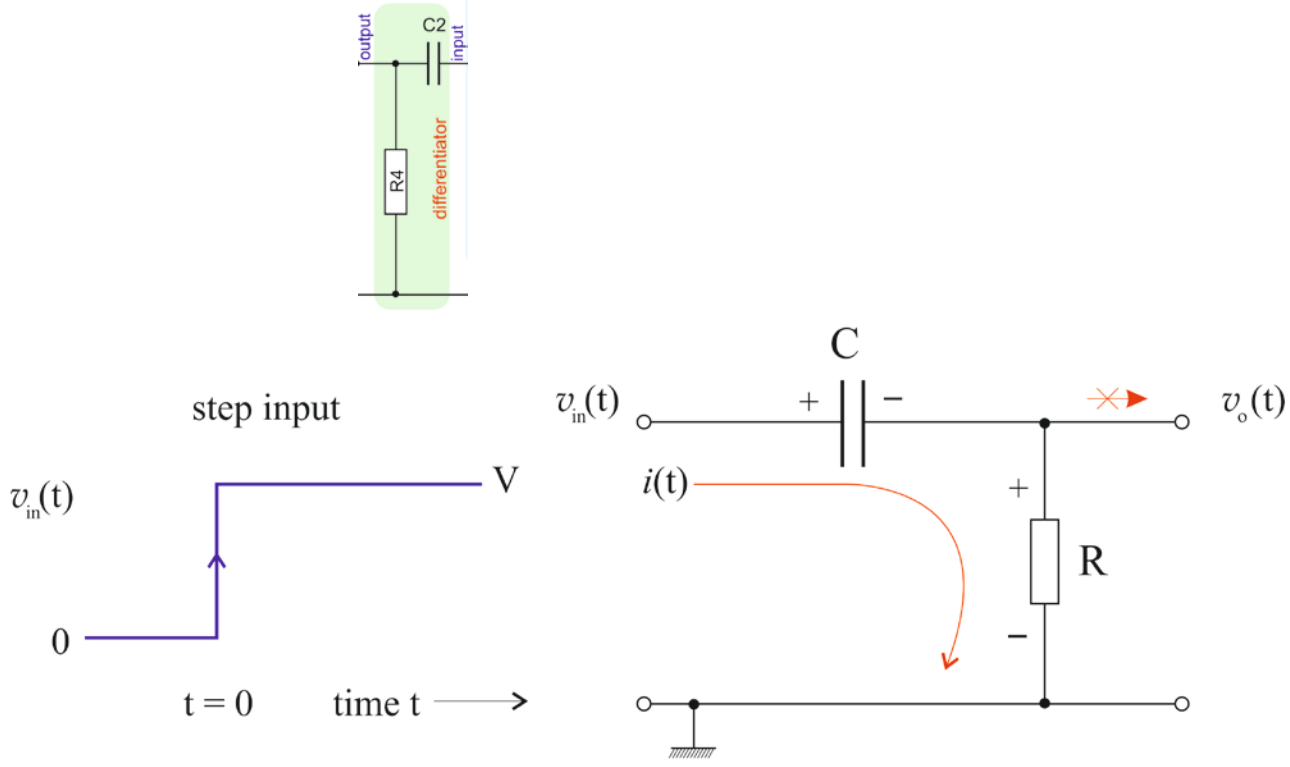


Figure 9. A voltage step input into a high-pass CR filter. v_o(t) is the open-circuit output voltage (no current is drawn).

For a positive step input: assume that the capacitor C is discharged initially. Then at time t = 0^+ the voltage *across* the capacitor = 0. Therefore, since the input voltage to the filter immediately after the step is $V_{in}(0^+) = V$, the output voltage $v_o(0^+) = V$, also. *This is the initial condition of the output.*

From Ohm's law: $v_o(t) = i(t).R$; and the current 'through' C is $i(t) = C\dfrac{d(V - v_o(t))}{dt}$.

$$\therefore \frac{v_o(t)}{R} = -C\frac{d\,v_o(t)}{dt}, \text{ or}$$

$$RC\frac{d\,v_o(t)}{dt} + v_o(t) = 0 \qquad (7)$$

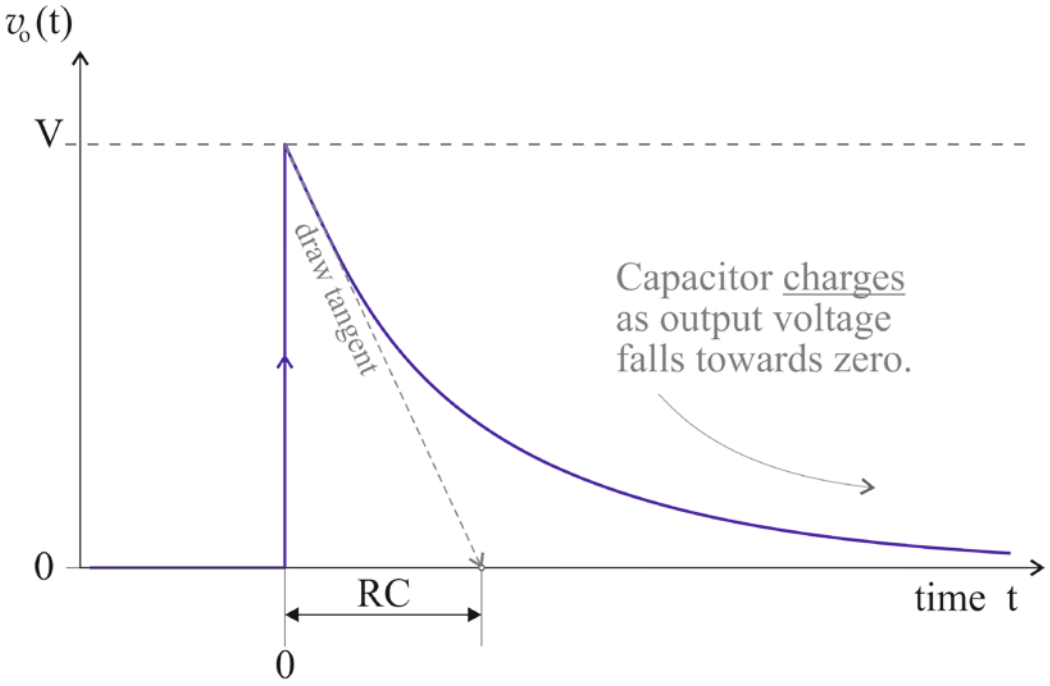


Figure 10. The output voltage response of a CR high-pass filter to a step-input of amplitude V volts, applied at time t = 0.
A construction is shown for finding the time-constant (= RC) of the exponential fall towards the asymptotic limit of zero volts.

Taking the LT of eqn.(7) leads to: $RC\left[sV_0(s) - \underbrace{v_o(0^+)}_{=V}\right] + V_0(s) = 0$

Therefore $V_0(s) = \dfrac{RC.V}{sRC+1} = \dfrac{V}{s+\frac{1}{RC}}$, and using the usual inverse LT identity $\mathscr{L}^{-1}\left\{\dfrac{1}{s-a}\right\} = e^{at}$

leads to (for $t \geq 0$): -

$$\boxed{v_o(t) = Ve^{-\frac{t}{RC}}}$$

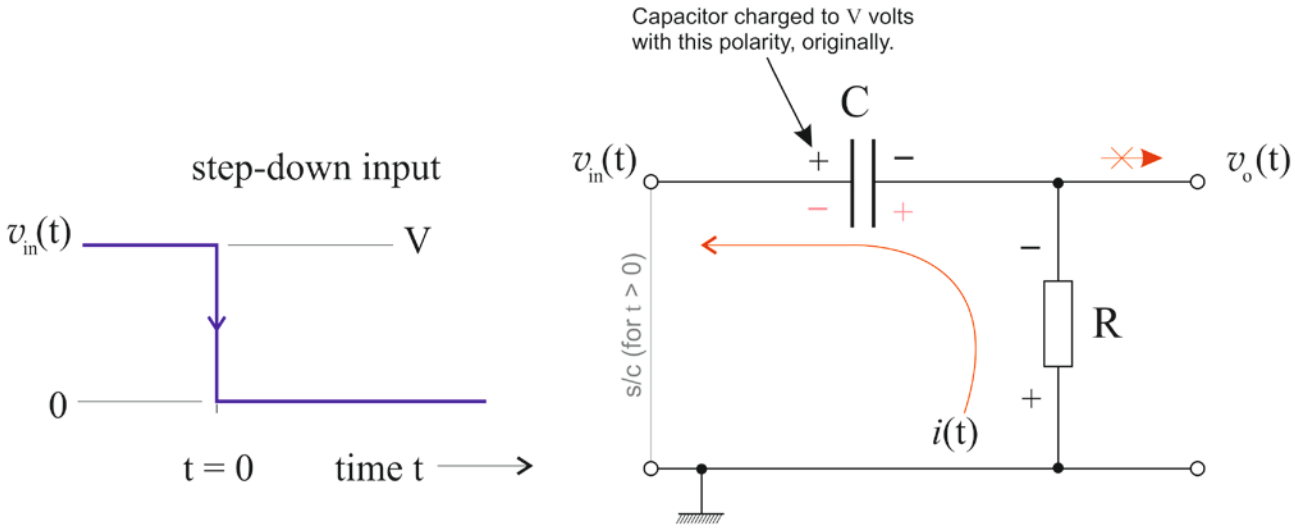


Figure 11. A voltage step-down input into a high-pass CR filter. Before the step-down input it is assumed that a voltage V was applied across the CR series-connected network for many time-constants, CR, so as to charge the capacitor C to the full input voltage, V. Therefore, immediately after the step-down input voltage (at time t = 0^+) C is still charged to voltage V (indicated by the +/- polarity signs in black), but its left-hand plate is now effectively connected to ground by a short-circuit (s/c). Consequently, the right-hand plate of the capacitor is now at voltage of $v_o(t) = -V$. Applying Ohm's law to resistor R shows that a current $i(t)$ must flow as shown, from ground (zero volts), down through resistor R due to the negative output voltage, $v_o(t)$ [instantaneously, $i(t) = V/R$], and 'through' capacitor C, as shown. This current charges the capacitor in the sense shown by the pink +/- polarity signs, such that the charge on the capacitor is steadily reduced—to zero: the capacitor is being discharged. $v_o(t)$ is the open-circuit output voltage (no current is drawn).

For a negative step ('step-down') input: assume that the capacitor is charged initially to V volts, as shown.

Then at time t = 0^+ the voltage *across* the capacitor = V (still). Therefore, since the input voltage to the filter immediately after the step is $v_{in}(0^+) = 0$, the output voltage *drops* to $v_o(0^+) = -V$. This is the initial condition of the output. Note that no charge has yet flowed either into or out of the capacitor. However, there is now a voltage V across resistor R with the polarity shown in Figure 11, so that the current $i(t)$ now flows through R and 'through' C, charging the latter with the polarity indicated by the lower (pink) ± signs. Clearly this accumulating charge is of opposite sign to that originally stored on the capacitor, so that it gradually neutralises the original charge on C. Thus the net charge on C is being reduced—the capacitor is being *discharged*. This discharging process reduces the magnitude of the voltage across the capacitor, since charge and voltage are proportional (Q = CV), and it reduces the magnitude of the voltage across R also—since R and C are effectively connected in parallel here, and always have the same voltage across them for times t > 0. Note that the voltage across resistor R $[\equiv v_o(t)]$ is zero prior to the negative step, i.e. for times t < 0.

From Ohm's law: $v_o(t) = -i(t).R$; and the current 'through' C is $i(t) = C\frac{d(v_o(t)-0)}{dt}$.

$$\therefore -\frac{v_o(t)}{R} = C\frac{d\,v_o(t)}{dt}, \text{ or}$$

$$RC\frac{dv_o(t)}{dt} + v_o(t) = 0 \quad \text{(as before)} \qquad (8)$$

But on taking the LT of eqn.(8) we use here the initial condition $v_0(0^+) = -V$, so that:-

$$RC\left[sV_0(s) - \underbrace{v_o(0^+)}_{=-V}\right] + V_0(s) = 0$$

The analysis therefore follows through, from now on, exactly as for the positive-step, except that we must replace V by $-V$, so that we find: -

$$\boxed{v_o(t) = -Ve^{-\frac{t}{RC}}}$$

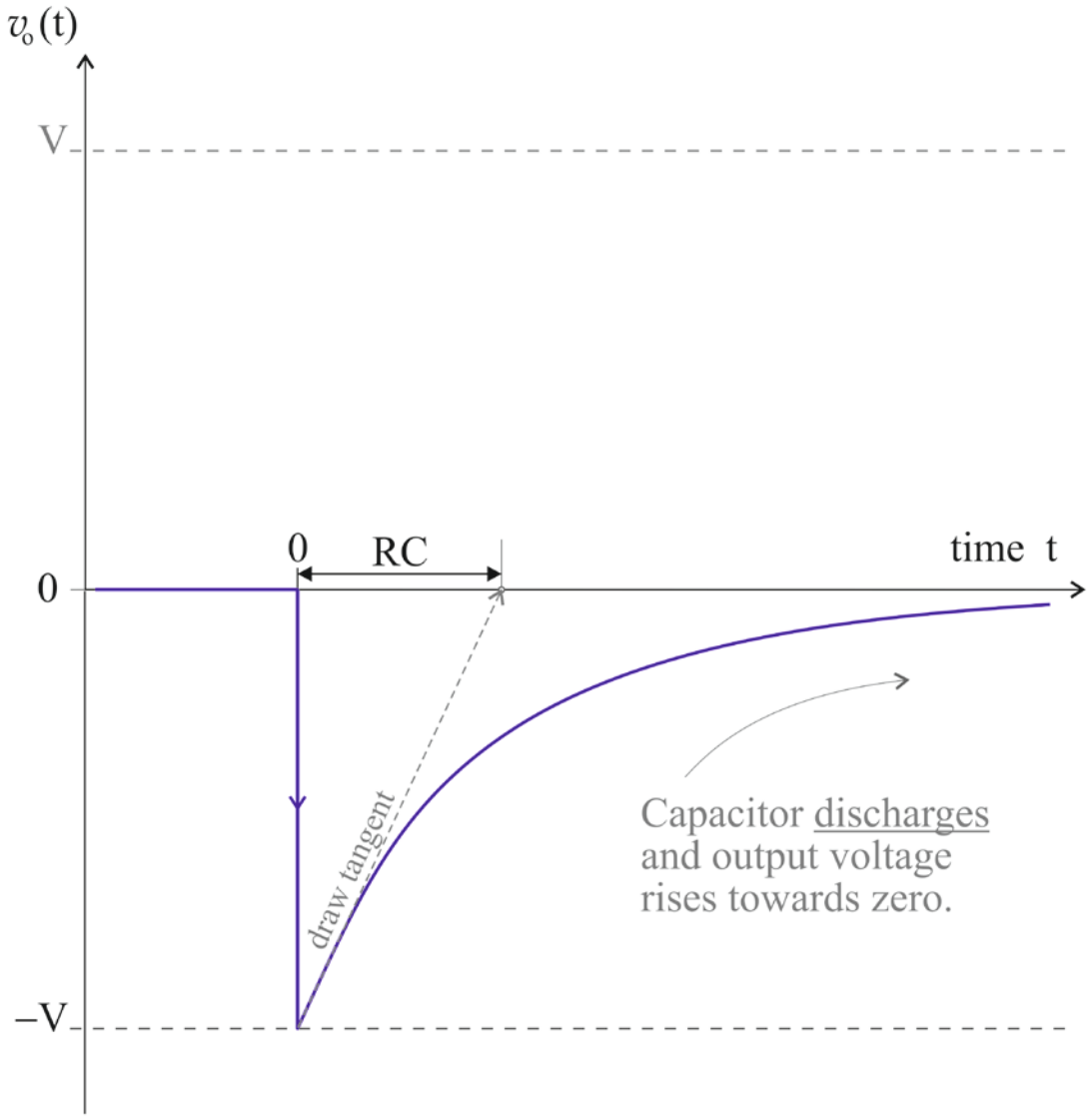
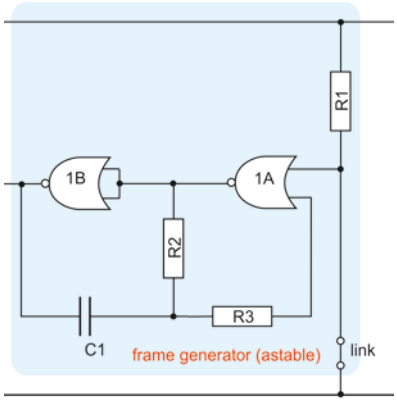


Figure 12. The output voltage response of a CR high-pass filter to a step-down input falling from V to zero volts applied at time t = 0. A construction is shown for finding the time-constant (= RC) of the exponential rise towards the asymptotic limit of zero volts.

A CMOS square-wave oscillator, or 'astable' circuit.



This useful circuit, shown in Figure 13 below, is employed in the Rangefinder project as a 'frame generator'— this having a period of approximately 34 ms (a frequency of ~ 30 Hz). In general, however, this circuit is capable of generating a square-wave output at V_{g2} with a period as short as a few microseconds, or as long as a few hundred seconds—simply by using different values for the components R and C.

NOR gate_2 is permanently connected ('wired') as an inverter, in the circuit, so that a logical 0 at its connected-together inputs produces a logical 1 at its output (V_{g2}), and vice versa. Therefore, the two logic-gate outputs V_{g1} and V_{g2} are always logical inverses of each other. Consequently, an additional square-wave output is available (potentially) from this oscillator at the output of gate_1 (V_{g1}), this being the complement of that available at V_{g2}. These two 'anti-phase' outputs can be valuable, in some applications.

Like NOR gate_2, NOR gate_1 is also an inverter—as far as input B is concerned, since input A is tied permanently to ground (logic 0) via a short-circuit link (s/c). Alternatively, a PTM switch could have been used in place of the short-circuit, as indicated in the Figure, such that pressing the switch would turn the oscillator ON (the oscillator would be turned OFF if the switch were open, since, under these conditions, the 1M 'pull-up' resistor would create a logic 1 at input A, forcing a permanent logic 0 at output V_{g1}, and a so a permanent logic 1 at output V_{g2}).

In general, no current can flow through the 'protection resistor' R_p (and so into, or out of, input B), because the input resistance of CMOS gates such as these NOR gates is of the order of 10^{12} Ω. Therefore, from Ohm's Law, there can be no voltage-drop across R_p. Consequently, the voltage sensed at input B must be identical to the indicated time-varying voltage, v(t). If voltage v(t) lies below a sharply-defined threshold for that gate (V_{Thr}), then it is seen as a logic 0 input, and $V_{g1} \rightarrow$ logic 1, $V_{g2} \rightarrow$ logic 0: conversely, if v(t) lies above V_{Thr} (by even 1 millivolt) it is seen as a logic 1 input, and $V_{g1} \rightarrow$ logic 0, $V_{g2} \rightarrow$ logic 1. Typically V_{Thr} lies between 45% and 55% of $+V_{dd}$, and for the purposes of calculation it may be taken as 0.5 V_{dd}.

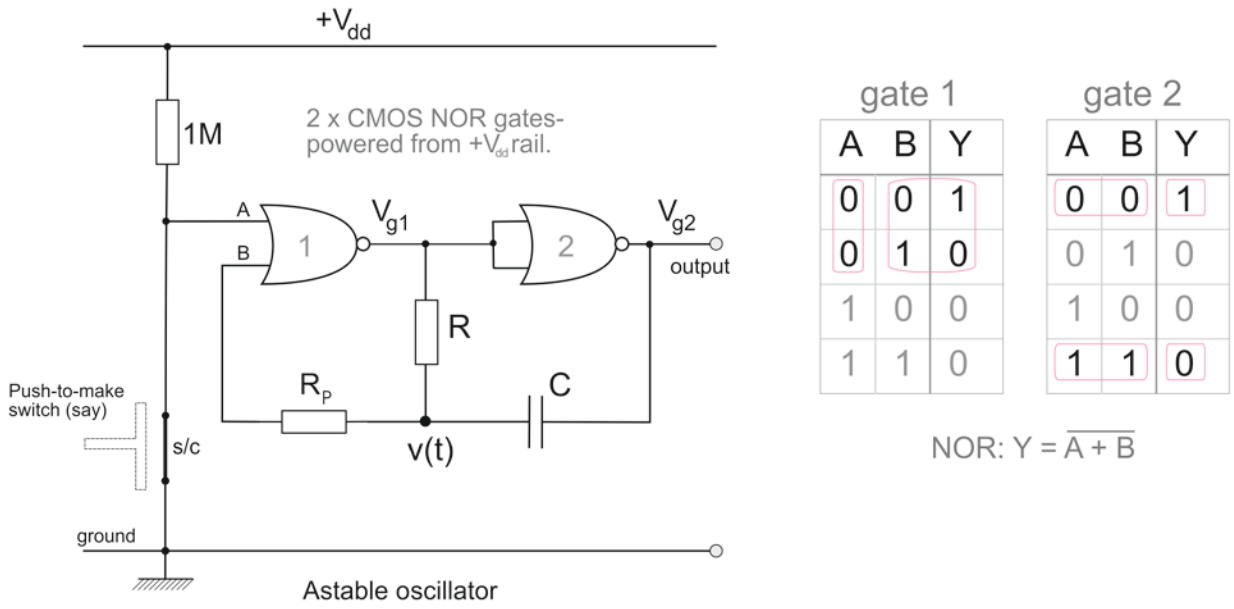


Figure 13. A CMOS (astable) square-wave oscillator. A Push-to-make (PTM) switch could be used in place of the short-circuit (s/c), in order to switch the oscillator on only when the switch is pressed. The two logical truth tables show gate 2 always to be an inverter (NOT gate) for logic levels applied by gate 1 to its wired-together inputs, and gate 1 to be an inverter for logic levels applied to input B, so long as input A is held at logic zero. Frequency of oscillation is determined by the RC time constant. R_p is a protection resistor.

Suppose that v(t) < V_{Thr}, so that V_{g1} = logic 1, V_{g2} = logic 0: i.e., point (c) on the waveform diagram in Figure 14, below. A current therefore will flow (effectively) from the +V_{dd} supply rail, through the output of gate_1 at V_{g1}, down through resistor R, and 'through' capacitor C to ground (at V_{g2}), so as to charge the capacitor. The charge on, and so the voltage across, capacitor C therefore will rise exponentially towards + V_{dd} —with a time-constant of RC seconds. This is the voltage v(t), and at some point it will rise up through the sharply-defined threshold voltage, V_{Thr} = 0.5 V_{dd}.

As this happens, $V_{g1} \rightarrow$ logic 0, and $V_{g2} \rightarrow$ logic 1. Therefore, the right-hand plate of capacitor C in the Figure will 'jump up' in voltage from V_{g2} = 0 volts (logic 0) to V_{g2} = +V_{dd} (logic 1). However, the charge on a capacitor cannot change discontinuously (it takes time for a current flowing into or out of a capacitor to alter its charge), and so the voltage *across* the capacitor after the jump-up in voltage by +V_{dd} is the same as it was just prior to the jump: 0.5 V_{dd}; and so the left-hand plate of the capacitor is now at a voltage of v(t) = +1.5 V_{dd}, i.e., at point (d) on the waveform diagram, below. Note that the voltage v(t) is now dropped across resistor R (since V_{g1} = 0 volts), and at this time an instantaneous current (from Ohm's Law) of 1.5 V_{dd} /R must flow down through resistor R, and 'through' series-connected capacitor C, too—in the process charging the capacitor in the opposite sense to that of its standing 'negative' charge: the capacitor is being discharged, and the voltage v(t) is falling exponentially towards zero volts. At point (e) on the waveform diagram, below, the net charge on C has fallen to zero, and so there is no voltage difference between the plates of the capacitor—the right-hand plate is still at V_{g2} = +V_{dd} (logic 1), and the voltage of the left hand plate now has fallen to v(t) = +V_{dd}. The diminishing current flowing down through R and 'through' C now starts to charge C in the opposite (positive) sense, i.e., point (f) on the waveform diagram, such that the voltage v(t) continues to fall exponentially towards zero (as the voltage across C rises exponentially towards +V_{dd}).

However, at some point the voltage v(t) will fall just below the threshold voltage $V_{Thr} = 0.5\ V_{dd}$, so that $V_{g1} \rightarrow$ logic 1, $V_{g2} \rightarrow$ logic 0. Therefore, the right-hand plate of capacitor C in the Figure will 'drop down' in voltage from $V_{g2} = +V_{dd}$ (logic 1) to $V_{g2} = 0$ volts (logic 0). Note that the voltage v(t) is now dropped across capacitor C once again (since $V_{g2} = 0$ volts), and, as the charge on C cannot change discontinuously, the left-hand plate of the capacitor must also drop down by a voltage of V_{dd}: from $v(t) = +0.5\ V_{dd}$ to $v(t) = -0.5\ V_{dd}$ (a voltage below ground, or zero volts) i.e., a similar situation to point (a) on the waveform diagram—and the oscillatory process then repeats, ad infinitum.

In order to prevent damage from static electricity occurring at the high impedance inputs of CMOS logic gates, all inputs are connected to the $+V_{dd}$ and ground rails via internal reverse-biased diodes. In normal operation these diodes do nothing. However, if the voltage at a gate input should fall more than 0.6V below circuit ground, or rise more than 0.6V above V_{dd} (it does both, here) then one or other of these protection-diodes will conduct, 'clamping' the gate's input voltage at the level where the diodes begin to conduct. The resistor R_p was included in the circuit above in order to allow the voltage v(t) to swing both below ground, and above $+V_{dd}$, without significant currents flowing through these diodes—which would alter the timing of the circuit.

Astable waveforms

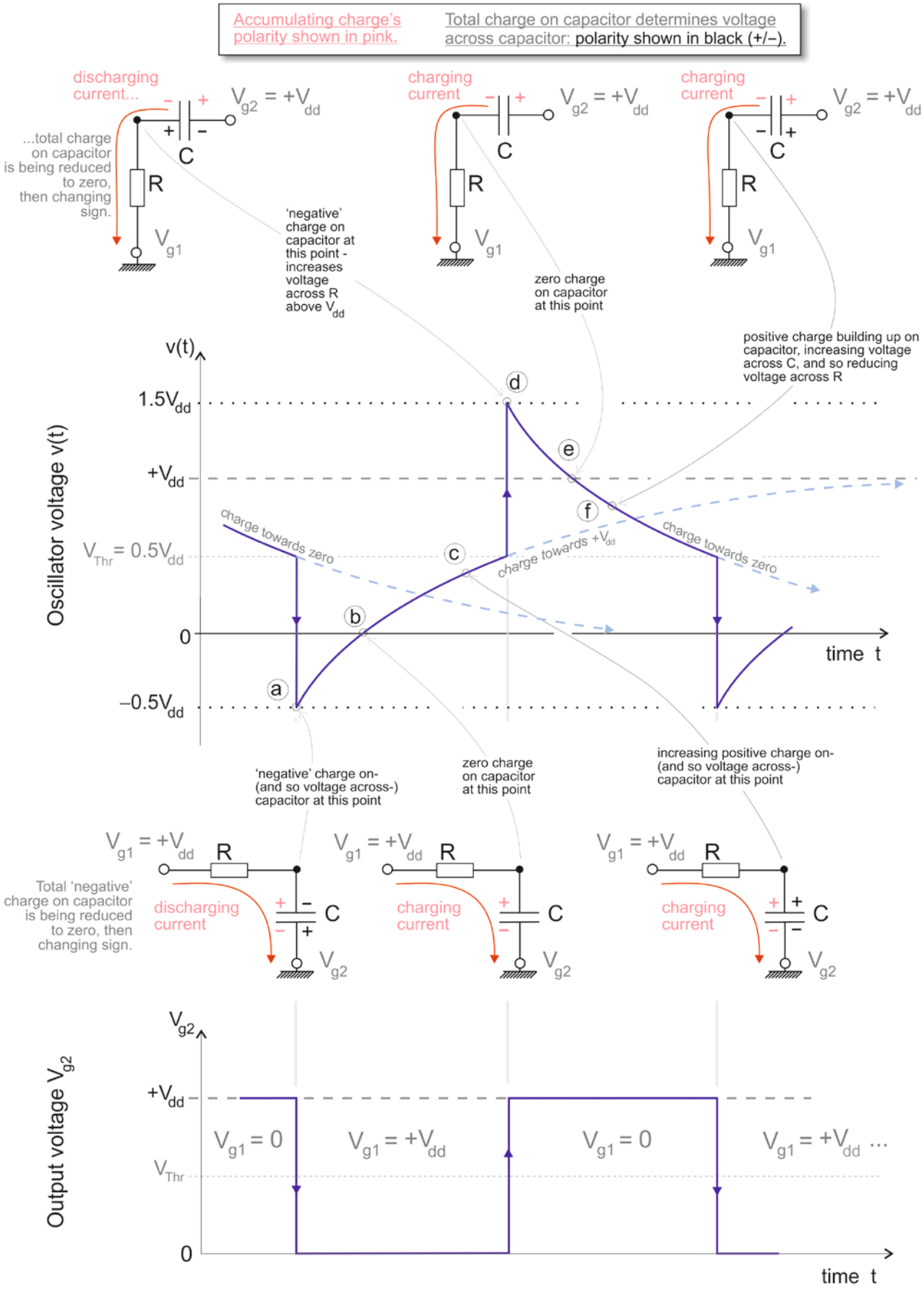
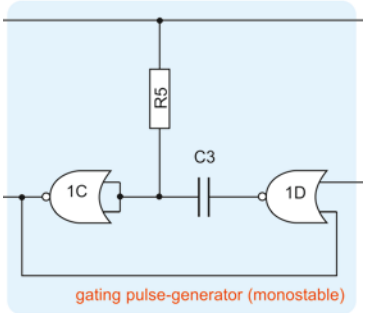


Figure 14. Astable square-wave oscillator waveforms: v(t) is the voltage at the junction of resistor R and capacitor C.

The time between point (a) and the first (positive) switching transition of the output (= one half cycle) is the time for a rising exponential to reach 2/3 of its asymptotic final value; or to put it another way (turning the waveform upside-down), it is the time for a decaying exponential to reach 1/3 of its initial value. Thus it is straightforward to show that the period of the square-wave output waveform of this oscillator is 2RC.ln(3) [seconds].

A CMOS 'monostable,' or '1 – shot' (US) circuit.



This is another very useful circuit built around CMOS logic gates: once 'triggered' by a very brief, positive, (logic-level) pulse at its input, it generates a single pulse of *fixed width* at its output. The duration of this output pulse is variable between 1 μs and several hundred seconds—simply by using different values for the components R and C (defined in Figure 15)—whilst the input trigger pulse may be sub-microsecond in duration.

The circuit is shown below in Figure 15. In its normal resting (quiescent) state, the output of the circuit (the output of gate 2 in the figure) is at logic 0, and this level is fed back to input B of gate 1. Under these quiescent conditions input A of gate 1 is also held at logic 0, either because the source of the trigger pulse driving input A is held at logic 0 (except for the brief period t_p of the trigger-pulse itself), or, if a square-wave trigger-input is to be used instead, with the differentiating network shown (R_d, C_d), because the resistor R_d 'pulls input A down' to zero volts, i.e. to logic 0. In either case both inputs of gate 1 are at logic 0, so that from the truth table the output of gate 1 (V_{g1}) will be at logic 1, i.e. at a voltage of $+V_{dd}$. The capacitor C thus sees a Thévenin voltage source between its terminals of zero Volts, and so (given a few time-constants' respite) it will be completely discharged: both of its plates are at a voltage of $+V_{dd}$. Gate 2 is configured as an inverter, and its inputs are 'pulled-up' to a logical 1 by resistor R: therefore its quiescent output (V_{g2}) will be at logic 0, as stated.

Upon receipt of the trigger-pulse, input A registers a logic 1, and the output of gate 1 therefore drops rapidly from the quiescent logical 1 to a logical 0 state, i.e. to V_{g1} = 0 volts. But capacitor C remains uncharged during this transition, so the inputs to gate 2—which is configured as an inverter—are also pulled-down instantaneously at 0 Volts, and this causes an abrupt 0-to-1 transition at gate 2's output, i.e., at the output of the monostable circuit (V_{g2}). This is the start of the output pulse.

However, the logical 1 at gate 2's output is fed back also to input B of gate 1, and this *latches* gate 1 in its present state, with its output equal to logical 0—*even if the trigger-pulse now were to be removed*. This latching action takes place extremely quickly (in less than 1 μs), and the duration of the trigger pulse t_p, (or the time-constant R_dC_d of the differentiator), need be not much longer than this for proper operation of the circuit.

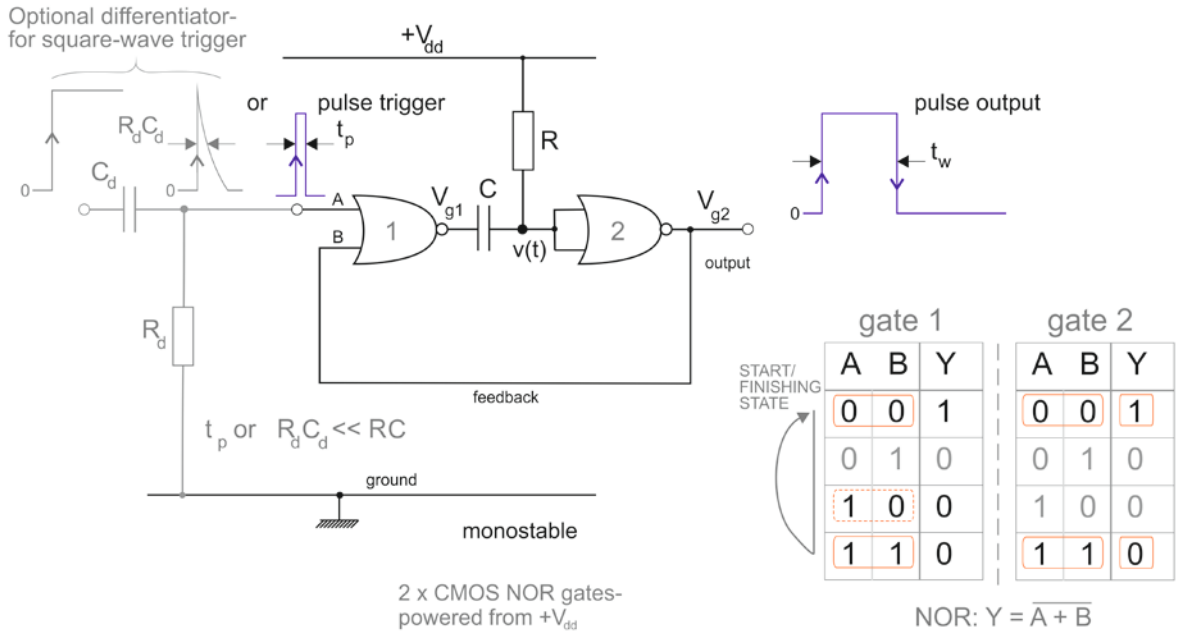


Figure 15. A CMOS monostable circuit. A brief positive (logic 0 to logic 1, and then back to logic 0) triggering pulse at input A will cause the monostable to generate a single pulse at its V_{g2} output, with a fixed width in time, t_w. The triggering pulse must have a duration t_p shorter than t_w. In the Rangefinder, the triggering pulses are generated from the rising edges of the frame generator's square-wave output, using a high-pass (C_dR_d) differentiating circuit, as indicated.

Following the negative transition at the output of gate 1, the capacitor charges up through resistor R towards a terminal voltage of v(t) = $+V_{dd}$, as shown in Figure16, below; but as v(t) crosses the switching-threshold voltage of $V_{Thr} = +0.5V_{dd}$, the inputs of gate 2 register a change from logical 0 to logical 1, and gate 2's output—the output of the monostable—terminates the output pulse with a 1-to-0 transition. Feedback action to input B of gate 1 therefore removes the previous 'latched' logical 1 state, and, *provided the original triggering pulse now has terminated*, the output of gate 1 will make an abrupt positive transition back up to logical 1, i.e., to $V_{g1} = +V_{dd}$. Positive feedback via capacitor C transmits this positive transition to gate 2's inputs, and drives them harder into a logic 1 state, the protective clamping-diodes at gate 2's inputs clamping the inputs at (V_{dd} + 0.6) Volts, and preventing them from rising (potentially) to a voltage of ($V_{dd} + V_{Thr}$). = $+1.5V_{dd}$.

The monostable's output pulse-width t_w is given by the time taken for an exponential to rise to 1/2 its final asymptotic value, or, to put it another way (turning the waveform upside-down), it is the time for a decaying exponential to reach 1/2 of its initial value. Thus it is straightforward to show that the duration of the monostable's output is given by $t_w = RC.\ln(2)$ [seconds].

In the Rangefinder, the output from its monostable is 1 ms wide, and it performs two functions: -

1. It 'gates on' the 40 kHz transmitter driving circuit, which is built around a 555 timer IC, and
2. It charges a capacitor through a diode, such that following the 1 ms pulse this capacitor discharges slowly through a resistor (RS), so as to keep 'inhibit gate' 2B closed for a period of time at the start of each measuring frame. This prevents the direct signal from transmitter to its adjacent receiver from being detected.

The monostable waveforms are shown in Figure 16, below:-

Monostable waveforms

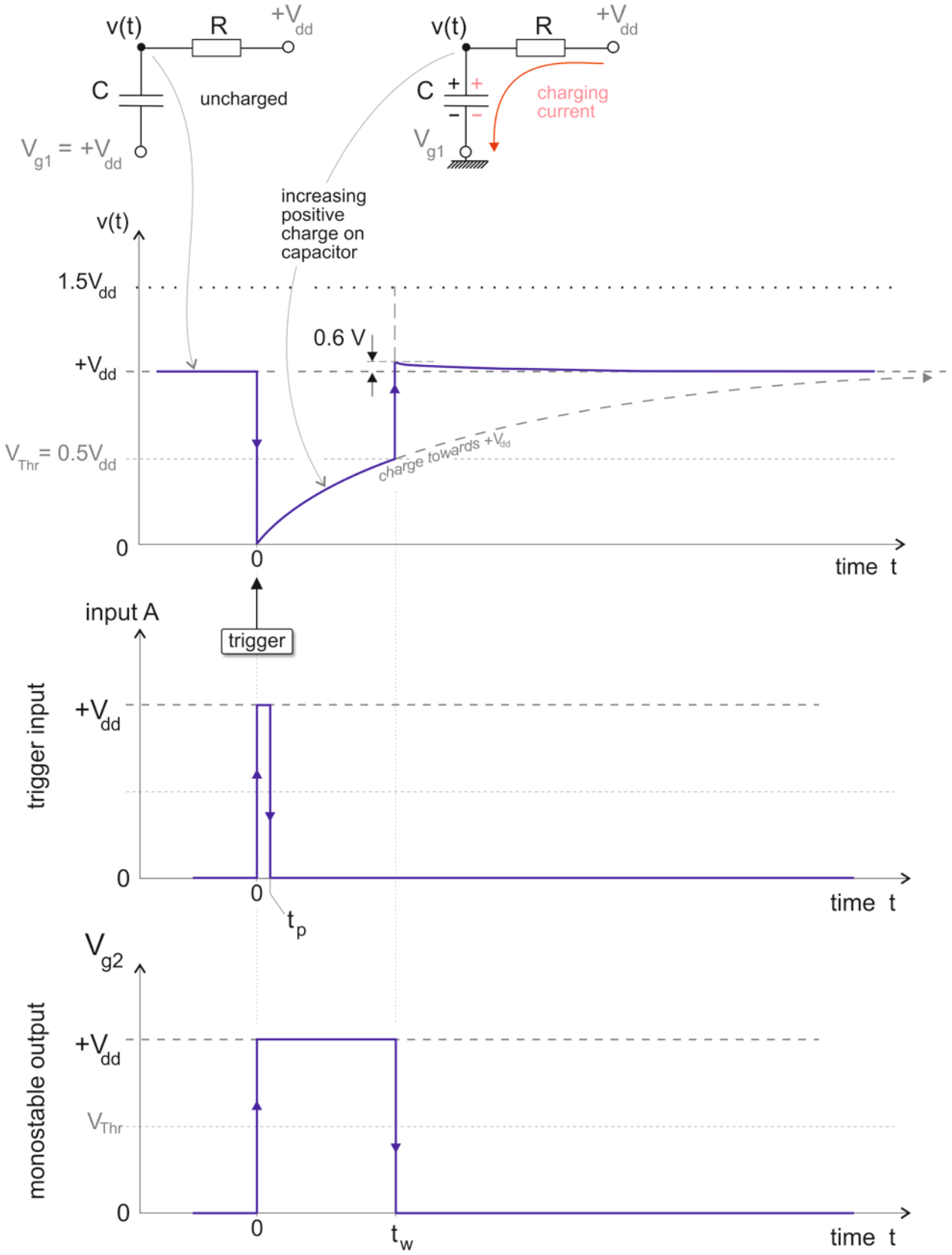
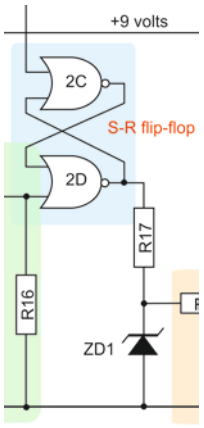


Figure 16. CMOS monostable waveforms: v(t) is the voltage at the junction of resistor R and capacitor C. A single brief trigger pulse (whose width in time might be variable) generates a wider pulse at the monostable's output whose width t_w is fixed.

S-R flip-flop



The S-R (or R-S) flip-flop is a bistable, 'sequential logic' device: that is, it can exist permanently in one of two logic states, and which of these two states it is actually in at any given time depends on the triggering-input history of the device. This flip-flop therefore possesses a 'memory.'

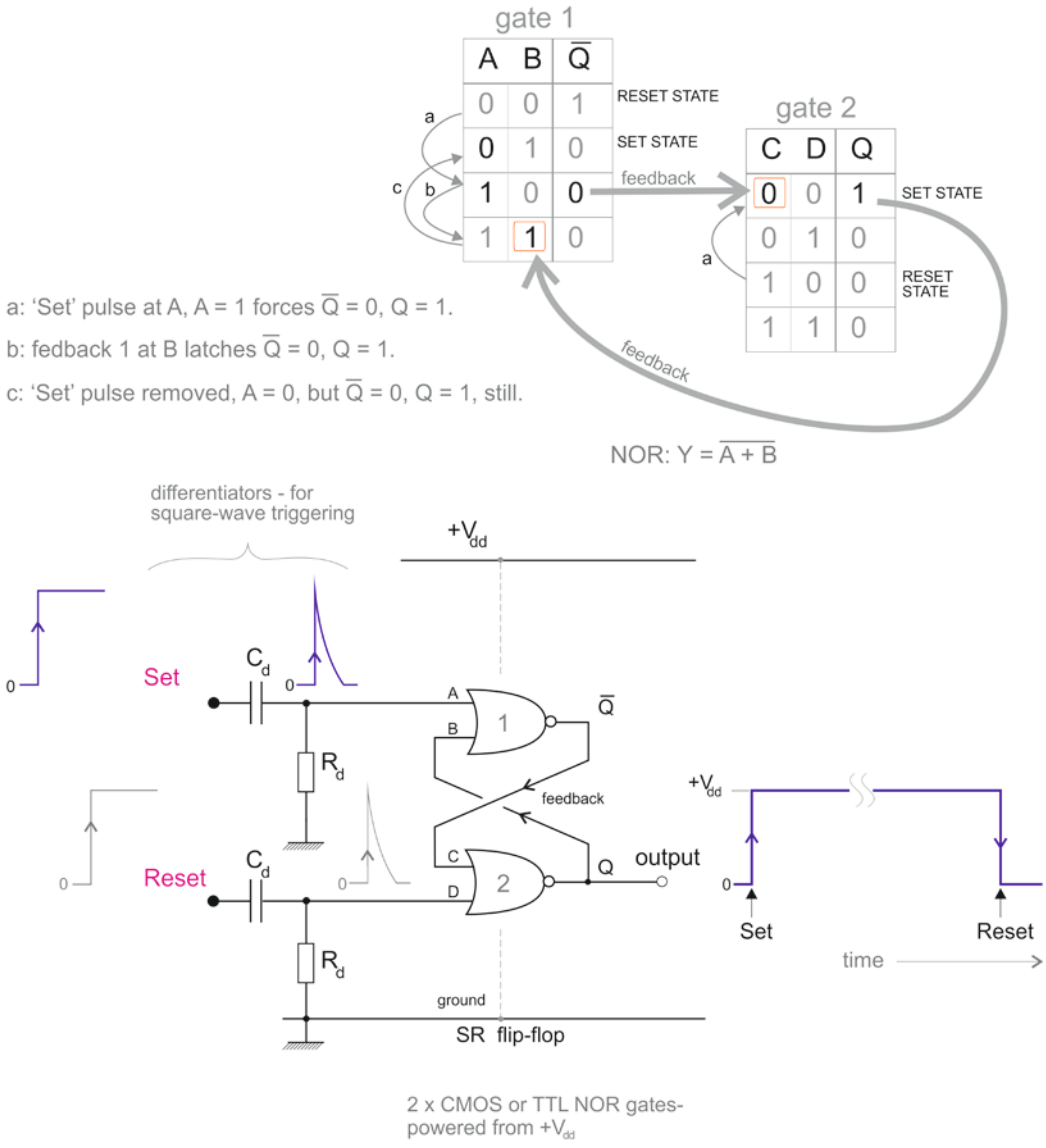


Figure 17. An S-R flip-flop. A single positive pulse to logic 1 at the Set input (input A of gate 1) latches a logic 1 at the Q output, via feedback to the B input of gate 1, and via feedback of the $\overline{Q} = 0$ output to the C input of gate 2.

The flip-flop has 2 inputs, labelled Set and Reset in Figure 17, above. A brief pulse to logical 1 on the Set input *latches* the flip-flop into the Set state, where $Q=1$, $\overline{Q}=0$. Conversely, a subsequent pulse to logical 1 at the Reset input latches the flip-flop back into the Reset state, with $Q=0$, $\overline{Q}=1$. If brief, positive, triggering-pulses were available for both Setting and Resetting the flip-flop, then these signals would be brought in directly to inputs A and D, without the use of the differentiating components C_d and R_d. In the Rangefinder, however, triggering is caused by rising edges (logic 0 to logic 1 transitions), and so these are turned into brief positive logic 1 'spikes' by the differentiating components C_d and R_d, the positive spikes decaying back down to zero volts (logic 0) with a time-constant of R_dC_d.

Example: "pulse-to-echo" time measurement.

In the example of Figure 18 an SR flip-flop is 'Set' (to logical 1) by a square-wave oscillator's, or 'frame generator's' rising-edge, which is coincident in time with the start of a transmitted ultrasonic 40kHz pulse (tone-burst). The rising edge of the detected echo 'Resets' the flip-flop back to logical 0.

- So the output of the flip-flop is at logic 1 for the pulse-to-echo flight-time—which is proportional to the range of the reflecting object. The RC filter, or Sallen & Key filter, turns this time into a voltage.

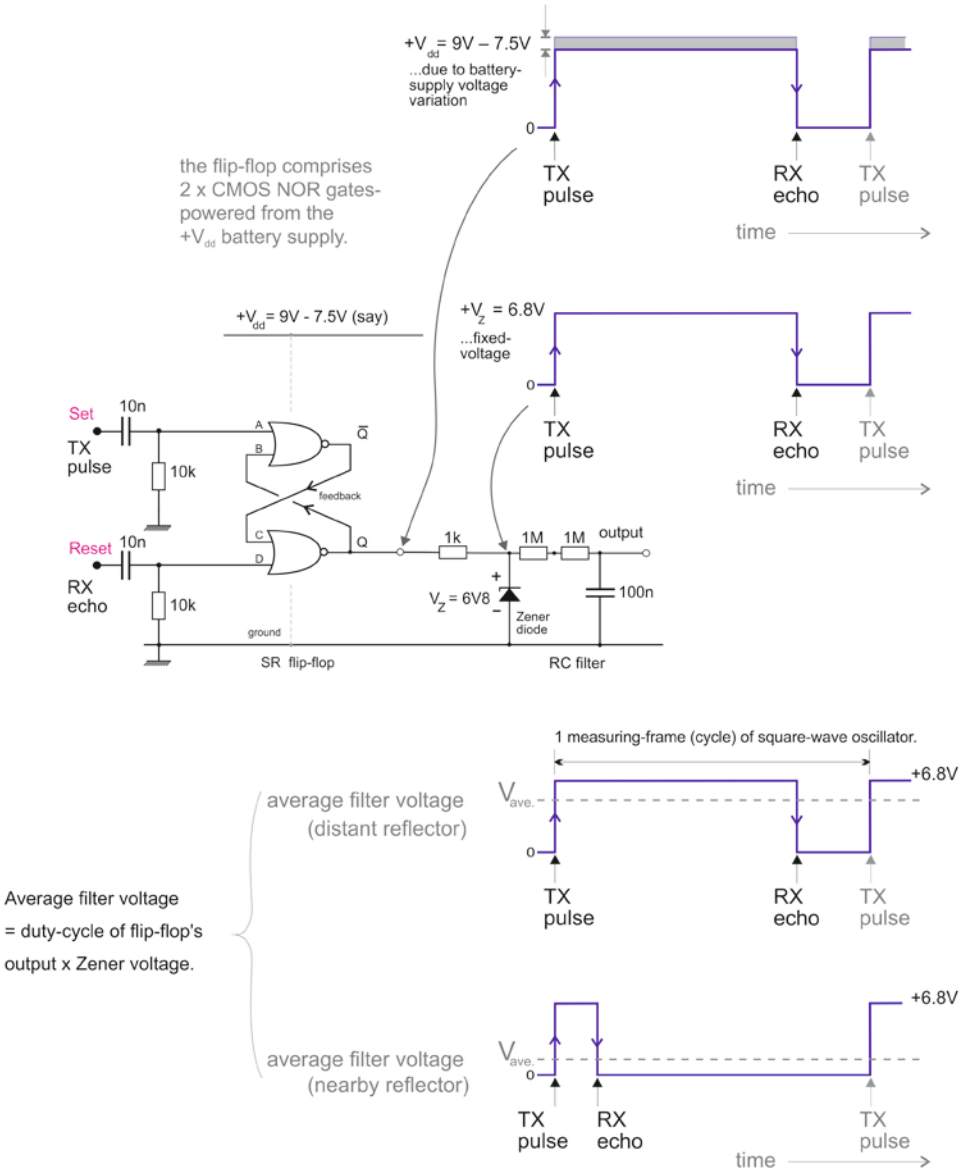


Figure 18. The Rangefinder's S-R flip-flop is used for the round-trip timing from the transmitted 'squeak' of ultrasound to the detected echo (TX pulse to RX echo).

Low-pass filter's input signal for the Ultrasonic Rangefinder

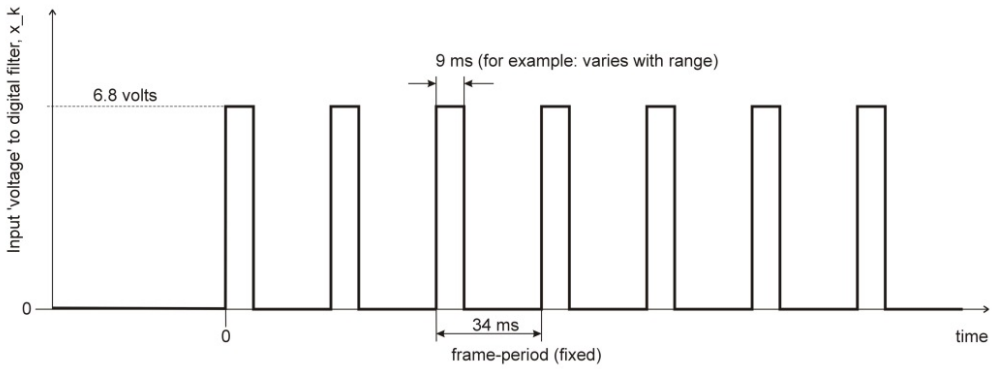


Figure 19. Averaging the repetitive output from the Rangefinder's S-R flip-flop. The frame-period (34 ms) is fixed.

The repetitive signal v(t), shown in Figure 19, above, is imagined to have been turned-on at time zero. At the start of each measuring-frame-period T (lasting for typically ~ 34 ms) the output signal from the Rangefinder's digital 'memory' circuit (S-R flip-flop) is set to logic 1, which in voltage terms is equal to the Rangefinder's battery voltage of '+9 volts'. This state is terminated (reset back to logic zero, or zero volts) by a detected echo signal. The resulting pulse to logic 1 at the flip-flop's output has a width in time here of t_p (e.g., t_p = 9 ms in Figure 19), which is equal to the round-trip time from the start of the transmitted 'squeak' of ultrasound to the detection of its returning echo from a distant target. Therefore, the time t_p spent in the logic 1 state is an analogue of the target's distance from the Rangefinder—its *range*. By placing a resistor and '6V8' zener diode (ZD1) in series at the output of the R-S flip-flop, a somewhat reduced in size, but steady, logic 1 level of V_z = 6.8 volts can be created, as shown in Figures 18 and 19, above, and also in Figure 20, below. This logic 1 level does not decrease in amplitude over time, as the Rangefinder's 9 volt battery slowly runs down.

Figure 20 focuses-in on the repetitive digital signal v(t) available across ZD1, over a single measuring-frame-period, T (aaproximately 30 such measuring frames occur per second). Here, a 40 kHz ultrasonic 'squeak' has been transmitted at time t = 0, and the echo from this signal has been detected a time t_p later. The average value, V_{ave}, of the repetitive signal is also indicated (note that V_{ave} lies at just that voltage level for which the red parallel-hatched positive area under v(t) but lying above this level '+' is equal to the blue negative area of v(t) lying below this level '-' —in one frame-period, T).

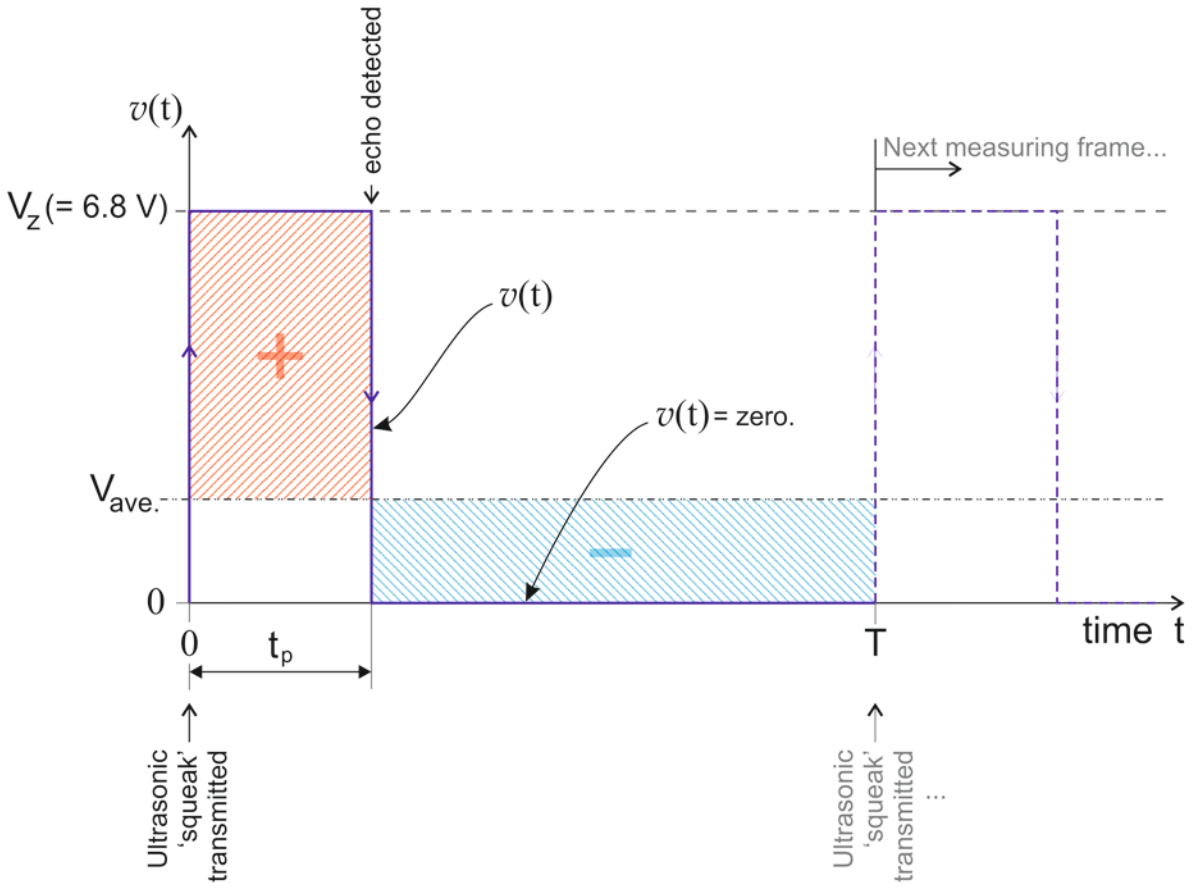


Figure 20. Averaging the repetitive output from the Rangefinder's S-R flip-flop. The frame-period (T = 34 ms) is fixed.

Formally, $V_{ave.} = \frac{1}{T}\int_0^T v(t)\ dt$, so that: -

$V_{ave.} = \frac{t_p V_z}{T}$. The ratio (t_p/T), sometimes expressed as a percentage, is known as the '*duty-cycle*' of the pulse-train. Therefore, $V_{ave.} = duty\ cycle \times V_z$.

However, $t_p = 2 \times range/c_{air}$, where *range* is the range out to the acoustically-reflective target, and c_{air} is the speed of sound in air.

$c_{air} = \sqrt{\frac{\gamma R T_A}{m}}$, where $\gamma = 1.40$ for air (N_2 and O_2 are diatomic), R (= 8.314 $JK^{-1}mol^{-1}$) is the Gas Constant, T_A (= 273.15 + ambient temperature in Celsius) is the Absolute temperature, and m is the molar mass of the air.

$m \cong (0.8 \times 28) + (0.2 \times 32)$, = 28.8 grammes, or 28.8×10^{-3} kg, where 28 and 32 are the molecular weights of N_2 and O_2, respectively.

Therefore, $V_{ave.} = \left[\frac{2V_z}{c_{air}T}\right] \times range$, and so a graph of the average voltage of the pulse-train, $V_{ave.}$, plotted against *range* to reflecting target, should be linear—with a gradient of: -

$$\left[\frac{2V_z}{c_{air}T}\right]$$

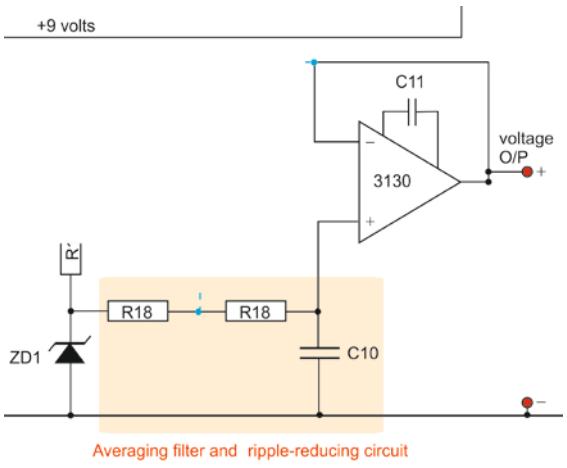
The quantities in the square brackets all can be found: V_z can be read from the Rangefinder's panel meter when the *range* is either zero, or when it is too great to have a detectable echo signal. In both cases the R-S flip-flop is never reset, and the voltage across ZD1 is equal to V_z, permanently. Finding V_z in this way also avoids a potential source of systematic error.

T, the frame-period, is measured most accurately using a digital oscilloscope.

In order to calculate c_{air} accurately, the ambient temperature must be known at the time the $V_{ave.}$ versus *range* data were taken. However, if an ambient temperature of (say) 23 Celsius were assumed for indoor measurements taken within the John Anderson building, then the resulting systematic error in the theoretical gradient of such a linear plot would not be large.

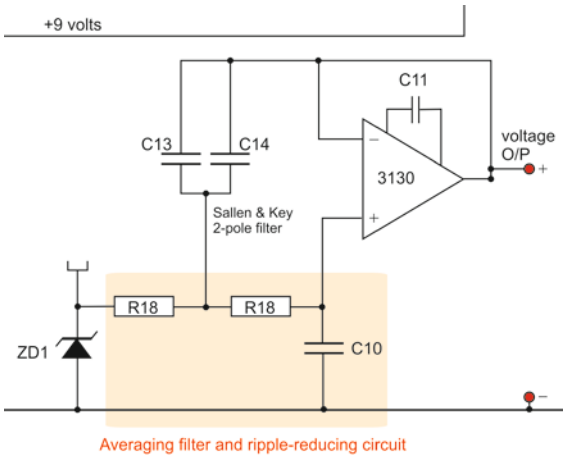
However, in order for the theory above to work, a technique for averaging (accurately) the pulse-train at the output of the R-S flip-flop must be used. Two techniques are employed in the Rangefinder project: -

- An RC (single-pole) low-pass filter, and



Averaging filter and ripple-reducing circuit

- A Sallen & Key (2-pole) low-pass filter.



Averaging filter and ripple-reducing circuit

In what follows, the pulse width has been taken to be $t_p = 9$ ms, and the frame-period to be T = 34 ms (as above), so that the filter's mean output voltage should become equal to $V_{ave.} = 6.8 \times 9/34$, = 1.80 volts.

Low-pass filters have the property that they pass DC (zero and very low frequency) voltages unmodified from input to output, but attenuate (possibly very strongly) high frequency voltage signals.

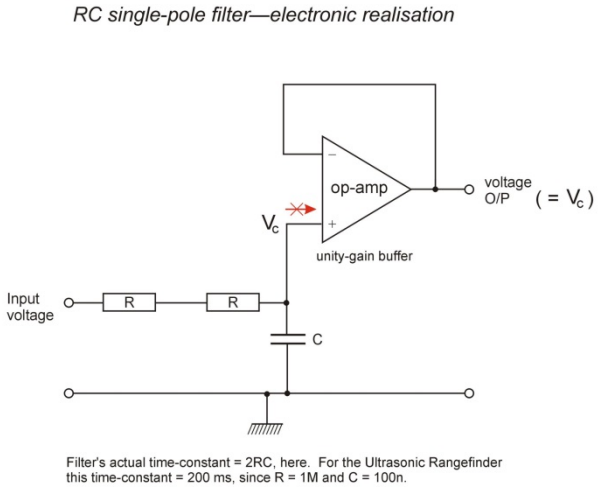
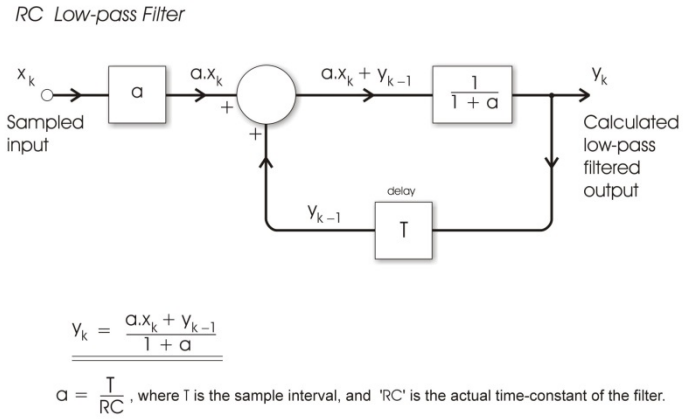
In fact, the pulse-train at the output of the R-S flip-flop, which has to be averaged, can be thought of as a true DC level, equal to $V_{ave.}$, together with a true AC signal (having zero mean)—as represented by the red

and blue parallel-hached areas in Figure 20—'sitting on-top of' the DC level, by the principle of superposition. The AC signal can be represented by a Fourier series of diminishing-amplitude harmonics, starting with the fundamental at ~ 30 Hz. Such a harmonic series, having no constant part, automatically has zero mean.

The RC low-pass filter attenuates the higher frequency harmonics of this series quite well. Unfortunately, the RC time-constant of this filter = 200 ms, and this is not very much greater than the period of the fundamental of the harmonic Fourier series (~ 34 ms): the ratio is only a factor ~ 6. Consequently, a significant level of 'saw-tooth' ripple is expected, coming from the fundamental and lower-order harmonics of the Fourier series.

The simplest way to generate, theoretically, how this filter should perform in practice is to use a 'sampled data' numerical technique, where the input pulse-train is imagined to be sampled repetitively a short sample interval T (not to be confused with the frame period) apart. The digitised (input) values are then denoted successively by: $\ldots x_{k-1}$, x_k, $x_{k+1}, \ldots$, etc. The k^{th} input (x_k) is considered to be the current input sample, and based upon this sample a simple recursive algorithm can be used to mimic very closely indeed the action of its electronic counterpart—the RC low-pass filter—so a to produce a *numerical filter* output, y_k, for each input sample, x_k. This algorithm makes use of a dimensionless time-increment parameter α (=T/RC), and a single delay of one sample interval, T (so as to make use also of the previously calculated, stored, output value, y_{k-1}).

Analog RC single-pole low-pass filter, and its Digital equivalent

Electronic Low-pass Filter	Digital version (algorithm can run in a MCU)
	

In the Analog RC filter, the negative feedback around the op-amp forces its output (O/P) voltage to follow the voltage across the capacitor (V_c)—which is applied to the op-amp's non-inverting input—without drawing any current from the filter. The op-amp acts as a 'unity gain buffer,' or a 'voltage follower.'

The results from the numerical filter are shown in Figure 21, below. They show that after (say) turning the instrument on, or changing the range, it takes ~ 1 second (5 time-constants) for the average value at the output of the filter to stabilize around the expected value of 1.80 volts. Unfortunately, the level of 'saw-tooth' ripple is severe, at 225 mV peak-peak. This level is unacceptable, and it can be reduced neither by

making the RC filter's time-constant longer (because that would impact adversely the instrument's speed of response to changing ranges), nor by making the frame period much shorter than 34 ms (because that would impact adversely the maximum target range: each echo has to arrive back during its own measuring frame—not early, say, into the next one).

However, this problem can be overcome by using a more sophisticated type of low-pass filter: the Sallen & Key, 2-pole, low-pass filter.

RC single-pole low-pass filter (output from digital algorithm)

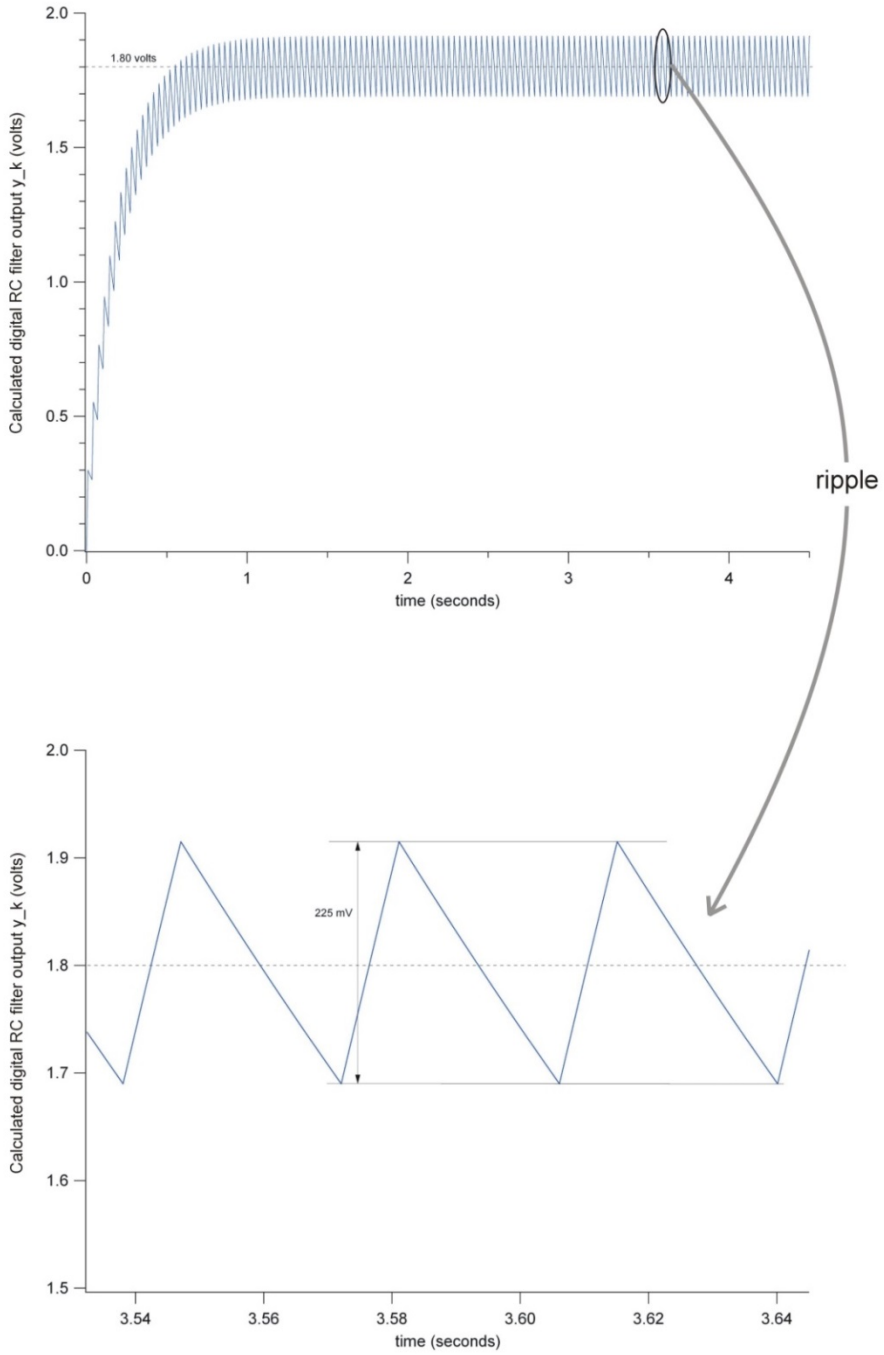
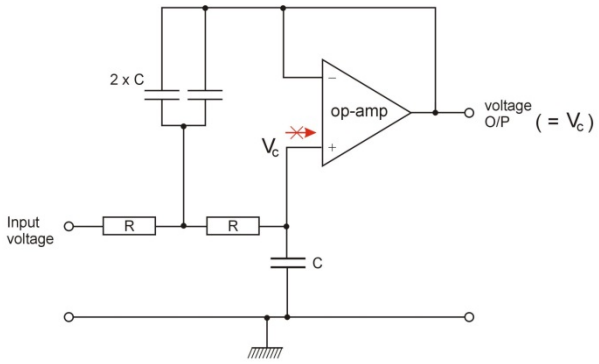
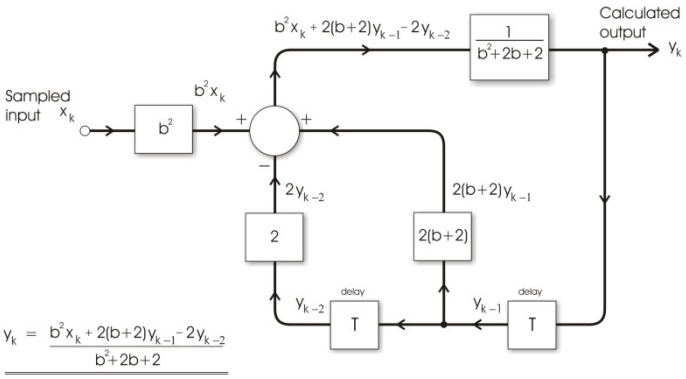


Figure 21. Numerical output from the Digital version of the RC low-pass filter. The pulse-train to be averaged was turned on at time t = 0, as in Figure 19. The anticipated average value = 1.80 volts. The lower half of the Figure shows a blown-up version of the unavoidable 'saw-tooth' ripple (please refer to the text).

Analog Sallen & Key 2-pole low-pass filter, and its Digital equivalent

Electronic Low-pass Filter	Digital version (algorithm can run in a MCU)
Sallen & Key 2-pole filter—electronic realisation 	*Sallen & Key Low-pass Filter*  $y_k = \frac{b^2x_k + 2(b+2)y_{k-1} - 2y_{k-2}}{b^2+2b+2}$ $b = \frac{T}{RC}$, where T is the sample interval and RC is the filter's time-constant.

The Analog Sallen & Key filter adds (unity gain) feedback via the two paralleled capacitors, of total capacitance 2C (capacitors labelled C13 and C14 in the Rangefiner's circuit diagram, shown in Figure 1), this feedback being applied to the mid-point of the two resistors, labelled R. This turns the filter into an 'active' filter—with greatly improved performance.

The numerical version of the Sallen & Key filter also uses the same dimensionless time increment parameter as the RC filter (here, it is called 'b'), where b = T/RC, T being the sample interval, and RC being a time-constant for the filter. However, the algorithm employs two delays of one sample interval, T, so that two previously calculated, stored, output values (y_{k-1} and y_{k-2}) can be used by the recursive algorithm, along with the current input sample, x_k. Results from the numerical Sallen & Key filter are shown in Figure 22, below. They show that after (say) turning the instrument on, or changing the range, it takes ~ 1 second for the average value at the output of the filter to stabilize around the expected value of 1.80 volts—a very similar reponse time to that of the RC filter, in fact; but here the similarities end. In the case of the Sallen & Key filter the level of ripple around the average (DC) value is very small, being just 9.6 mV peak-peak. This level is quite acceptable in the Rangefinder application.

Sallen & Key 2-pole low-pass filter (output from digital algorithm)

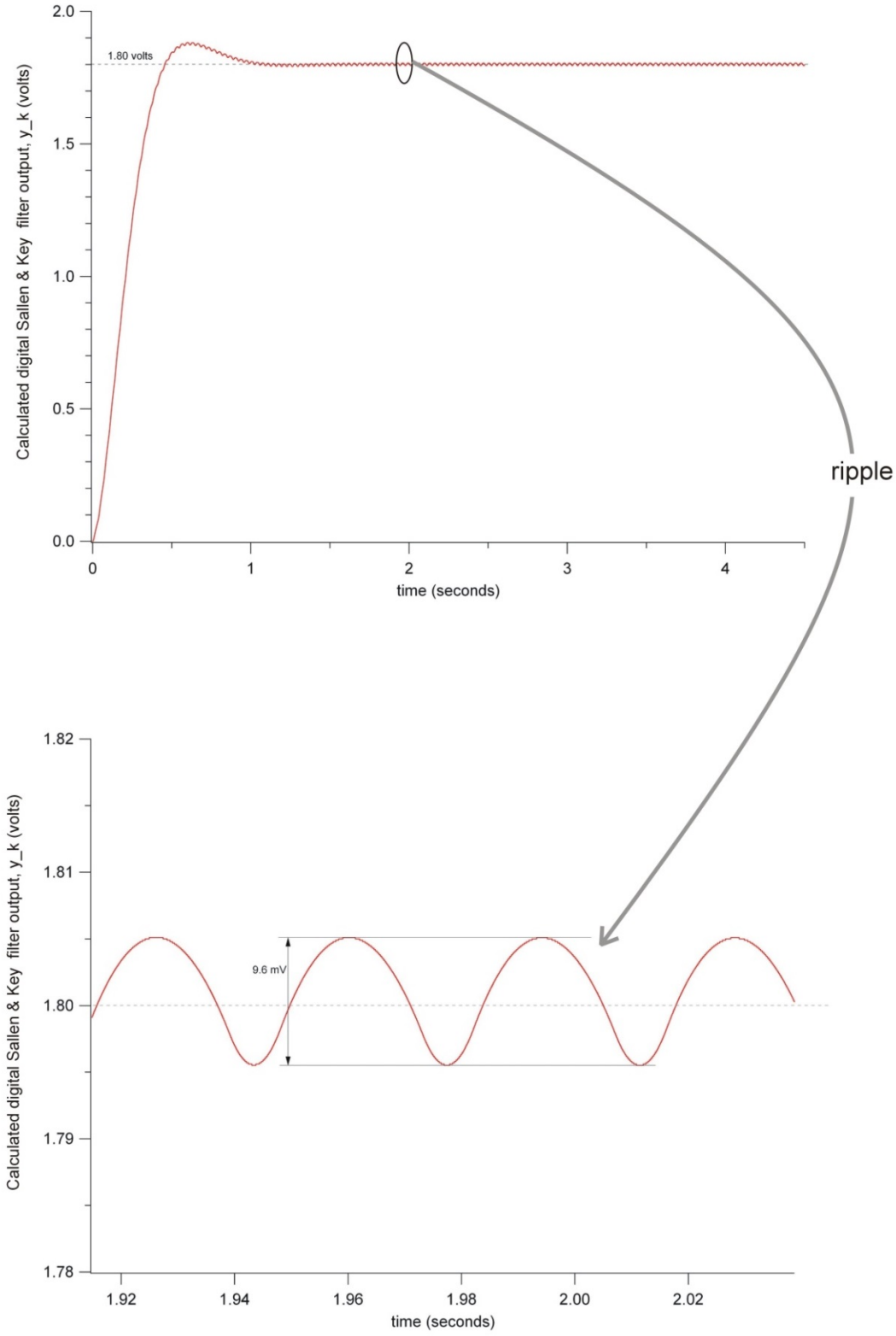


Figure 22. Numerical output from the Digital version of the Sallen & Key low-pass filter. The pulse-train to be averaged was turned on at time t = 0, as in Figure 19. The anticipated average value = 1.80 volts. The lower half of the Figure shows a blown-up version of the (now) very small ripple (please refer to the text).

Single-stage AC amplifier

Analysis of the ultrasonic Rangefinder's two-stage transistor amplifier is rather lengthy, and analysis of a simpler single-stage amplifier is given in full, below. Exactly the same approach would be used in the analysis of the Rangefinder's AC amplifier.

DC analysis

The full circuit diagram of the amplifier is shown in Figure 23. First of all, the collector current I_c must be found from a DC analysis of the amplifier circuit in the Figure, so that the AC mutual conductance g_m of the transistor can be evaluated. In this DC analysis the two 'coupling' capacitors at the amplifier's input and output are treated as open-circuits (the effect of the capacitor C, shown with dashed connections, is considered under the AC analysis section below—its presence or absence does not affect the DC analysis of the circuit in any way). Furthermore it will be assumed that the transistor is biased into its 'active' region—so that it may function as an amplifier of the AC input signal V_{in} (this will be checked, later). Sinusoidal AC signals are indicated in the Figure, but the AC analysis applies equally to other forms of AC signal, such as pulses, or tone-bursts.

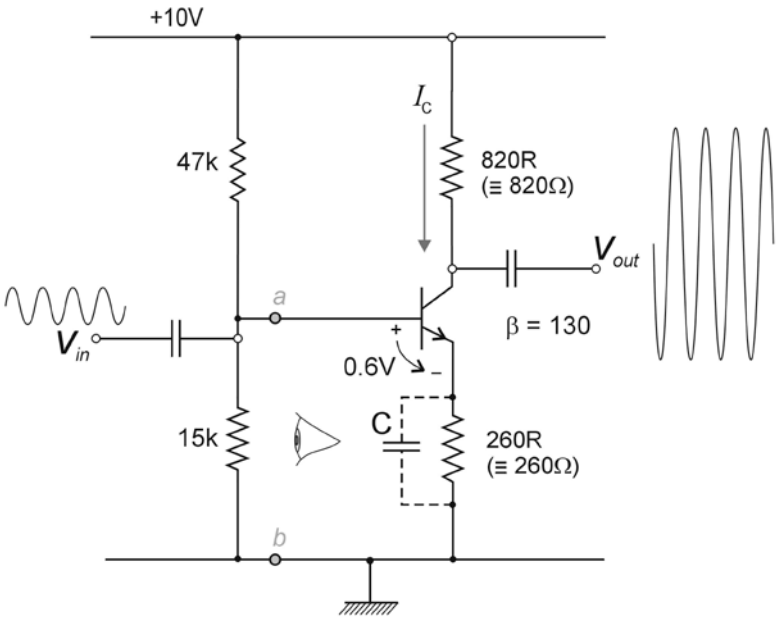


Figure 23. Circuit diagram of a single-stage transistor-based AC amplifier.

The DC Thévenin equivalent of the 47k/15k potential-divider in Figure 23 is found by 'looking into' nodes *a* and *b*, and its two components are evaluated and underlined in Figure 24. This simplifies (greatly !) the DC analysis of the circuit. The open-circuit voltage of the potential divider is the Thévenin voltage V_{Th} = 2.419 volts, as shown below, whilst 'suppressing' the 10V voltage source (notionally short-circuiting it to ground) casts the 47k resistor of the divider in parallel with the 15k resistor. Thus the resistance 'seen' between the nodes *a* and *b* under these conditions is 47k//15k = 11.371 kΩ, which is therefore the value of the Thévenin resistance, R_{Th}. Replacing the actual potential- divider by its Thévenin equivalent circuit allows the 'input circuit' of the transistor to be simplified to that shown in Figure 24. It now can be seen that it is actually a 2.419 volt source that drives current clockwise around the input circuit of the transistor. Noting that the emitter current $I_e = (1+\beta)I_b$, where β = 130, here, allows Kirchhoff's voltage law to be written for the input loop entirely in terms of the base current I_b, and in this way the current I_b may be found.

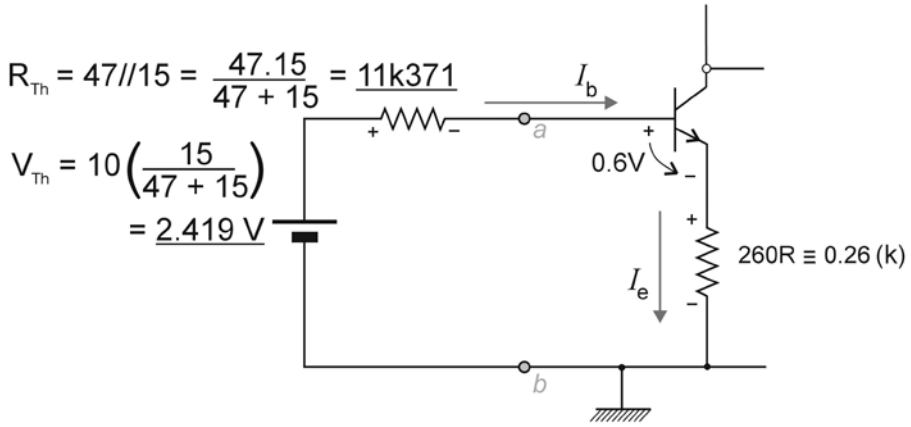


Figure 24. The transistor's DC input circuit is used to find the value of its base current, I_b. Then the desired collector current $I_c = \beta I_b$, where β is the current-gain of the transistor (at AC as well as DC). Here, $\beta = 130$. The base-emitter voltage of an npn silicon transistor may be taken to be 0.6 volts.

Equating the sum of voltage drops around the input loop to the magnitude of the driving voltage source: -

$$2.419 = I_b \times 11.371 + 0.6 + (1+130) I_b \times 0.26 \qquad (1)$$

Note that in equation 1 the resistances have all been expressed in kΩ, and the voltages all in volts (e.g., the voltage drop from base-to-emitter of a silicon transistor = 0.6 volts). Therefore, I_b will be evaluated in milliamps (mA). Re-writing equation 1 gives: -

$$1.819 = I_b \times 11.371 + I_b \times (131 \times 0.26), \text{ or} \qquad (2)$$

$$1.819 = I_b \times (11.371 + 34.060). \qquad (3)$$

Equation 2 shows that the value of the emitter resistor (R_e = 260Ω, or 0.26kΩ), is effectively increased greatly in value through multiplication by the large factor $(1+\beta)$.

From equation 3: -

$I_b = \dfrac{1.819}{45.431}, \quad = 0.040$ mA. The collector current now can be evaluated directly as

$I_c = \beta I_b, \quad = 130 \times 0.040 \text{ mA}$, or $\underline{I_c = 5.20 \text{ mA}}$. If the transistor's emitter current were also required then it could be found simply as the sum of the base and collector currents (the whole transistor acting as a single current node), or

$$I_e = I_c + I_b \quad = 5.24 \text{ mA}.$$

And if the emitter voltage were needed, then from Ohm's Law this is simply equal to the voltage developed across the emitter resistor due to the current I_e flowing it, or

Emitter voltage = 5.24 × 0.26 = 1.362 volts (N.B.: mA × kΩ ≡ volts).

In a similar way the transistor's collector voltage can be found as 10 volts (the supply voltage) minus the voltage dropped across the collector resistor R_c (820Ω, or 0.82kΩ) due to the current I_c flowing through it, or

Collector voltage = 10 – (5.20 × 0.82) = 5.736 volts.

Therefore the voltage from collector-to-emitter 'across' the transistor = (5.736 – 1.362), or 4.374 volts—verifying that the transistor here is indeed biased well into its active region, since this voltage is much greater than the typical saturation voltage for a small-signal transistor (~ 0.05 volts).

AC analysis

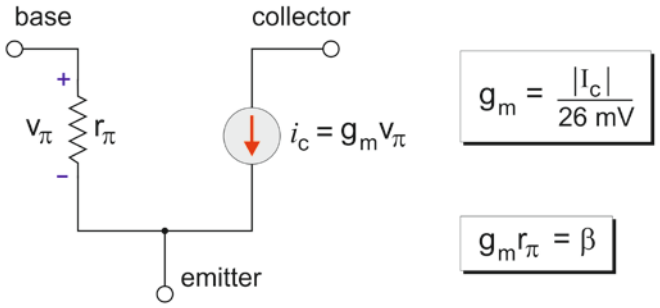


Figure 24. Hybrid-π (incremental) AC model of a bipolar transistor. $|I_c|$ is the absolute value of the transistor's DC collector current. β is the transistor's current gain (both DC and AC).

Given the collector current $I_c = 5.20\ \text{mA}$, the first of the two elements in the hybrid-π (AC) model of the transistor now may be found—the mutual conductance, g_m. This is obtained from

$$g_m = \frac{|I_c|}{26\ \text{mV}} = \frac{5.20\times10^{-3}}{26\times10^{-3}} = 0.2\ \text{S (Siemens)}.$$

Note that 26 mV = $k_B T/q_e$, where k_B is Boltzmann's constant, T is the ambient temperature (300 K), and q_e is the charge on the electron. The second element of the hybrid-π model, the dynamic input resistance of the transistor, r_π, can then be found from

$$g_m r_\pi = \beta, \text{ or } r_\pi = \frac{\beta}{g_m}, \quad = \frac{130}{0.2}, \text{ or } r_\pi = 650\,\Omega \text{ (Note that } S^{-1} \equiv \Omega).$$

Both elements of the transistor's hybrid-π model now are known, and the AC model of the amplifier can be constructed by replacing the transistor first of all by its 3-terminal hybrid-π equivalent, as shown in Figure 25, below. In this model, the AC (output) transistor collector current i_c (= $g_m v_\pi$) flows in response to an AC (input) voltage v_π developed across the dynamic input resistance of the transistor, r_π. If the polarity of v_π is positive with respect to the reference polarity indicated (±) against r_π, then the current i_c will flow in the direction of the reference arrow in the dependent current source symbol, shown in the Figure. If v_π is negative (half a cycle later, say), then i_c will flow in the opposite sense. Note that lower case variables are used conventionally for AC quantities.

The construction of the full AC model of the amplifier then proceeds by suppressing the 10 volt DC supply, so that just the effect of the *AC voltage source* at the input of the amplifier, V_{in}, may be found (then, by superposition, the *full* AC and DC voltages and currents could be found, if desired, simply by summing the separate DC and AC effects). When the 10 volt source is suppressed (by a notional short-circuit) the 'top ends' of the 47k and 820R resistors are seen to be shorted effectively to (AC) ground; and at this point the input and output capacitors are considered to be short-circuits as well for AC signals (also marked 's/c' in the figure below).

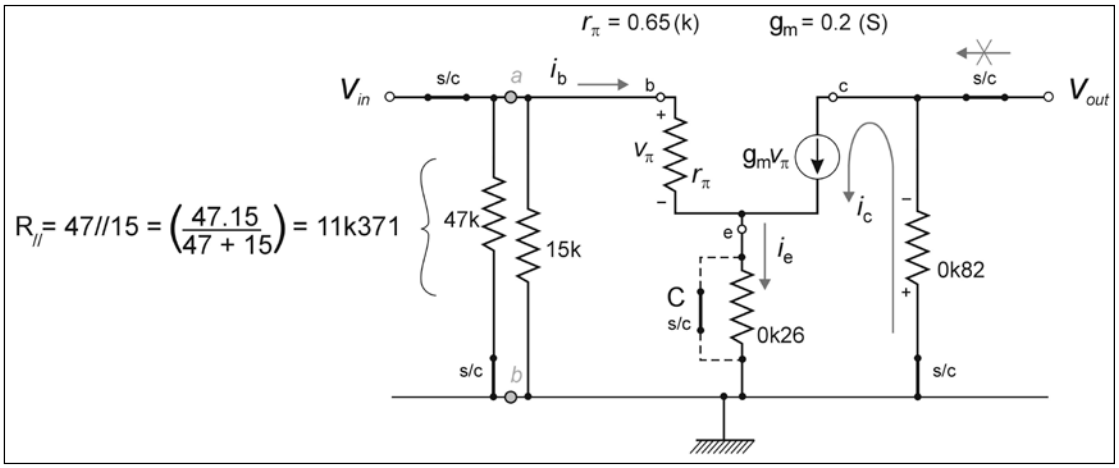


Figure 25. AC model of the transistor amplifier, incorporating the hybrid-π (incremental) model of the transistor. An AC collector current i_c flows in response to an AC voltage v_π developed across the dynamic input resistance r_π of the transistor. The amplifier's input and output capacitors have been replaced by short circuits (s/c) at AC. The 10 volt (DC) supply has been suppressed (replaced by a notional short-circuit to AC ground), and this action has connected also the 'top ends' of the 47k and 0k82 to ground, as shown. Here, R_e = 0k26, and R_c = 0k82.

In the resulting full AC circuit above the 47k and 15k resistors of the potential divider are once again seen to be connected effectively in parallel—here, as far as AC signals are concerned. Note that, as in the DC analysis, resitances have all beeen expressed in the figure in kΩ (0k82 ≡ 820 Ω, for example).

For the moment, the AC effect of capacitor C will be omitted.

Kirhhoff's voltage law for the input circuit of this AC model can be written down straightforwardly by assuming the input signal voltage V_{in} to be instantaneously positive. Therefore, with R_e = 0k26: -

$$V_{in} = i_b r_\pi + i_b(1+g_m r_\pi)R_e, \tag{4}$$

where the following facts have been used: from Ohm's Law $v_\pi = i_b r_\pi$, the signal emitter current $i_e = i_c + i_b$, and $i_c = g_m v_\pi$. However, $g_m r_\pi = \beta$, and so $i_c = \beta i_b$ for AC (cf $I_c = \beta I_b$ for DC), and equation 4 becomes

$$V_{in} = i_b\{r_\pi + (1+\beta)R_e\}, \tag{5}$$

Once again, the effective value of the emitter resistor is seen to be magnified by the large factor $(1+\beta)$. Therefore, dividing the voltage 'at' the base of the transistor (node b in the figure)—i.e. the voltage V_{in} relative to ground—by the current i_b flowing into the base, gives from equation 5 the effective AC resistance of the transistor and its emitter resistor from base to ground of

$$R_{in(trans)} = r_\pi + (1+\beta)R_e = 0.65 + (131\times 0.26), \text{ or } R_{in(trans)} = 34.71\ \text{k}\Omega.$$

As far as the AC input resistance of the amplifier is concerned (i.e., the resistance 'seen' by the voltage source V_{in}), the resistance $R_{in(trans)}$ is in parallel with the 11.371 kΩ of the potential divider. Therefore the actual input resistance of the amplifier as a whole = 34k71//11k371, or

$$R_{in} = \underline{8.565\ \text{k}\Omega.}$$

Therefore, the AC Thévenin equivalent model of the amplifier's input is purely passive—it is just a resistor connected to ground (no sources of any description), as shown in Figure 26.

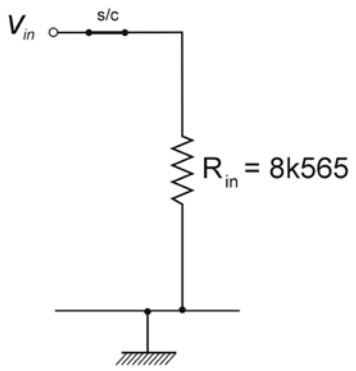


Figure 26. Input model of the AC amplifier: the input is passive (no voltage or current sources). It is just a resistance of value 8.565 kΩ.

From equation 5 the signal base current of the transistor is

$$i_b = \frac{V_{in}}{\{r_\pi + (1+\beta)R_e\}}, \tag{6}$$

And so, using equation 6, the collector current $i_c = \beta i_b$ is given by

$$i_c = \frac{\beta V_{in}}{\{r_\pi + (1+\beta)R_e\}} \tag{7}$$

From the AC model it is clear that in response to the assumed positive input voltage V_{in} this current i_c must flow *upwards* through the 820Ω collector resistor, generating a negative voltage V_{out} across this resistor, such that (with R_c = 0k82): -

$$V_{out} = -i_c R_c$$

Therefore, from equation 7 the AC voltage gain A_v of the amplifier is

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{\beta R_c}{\{r_\pi + (1+\beta)R_e\}} \tag{8}$$

Substitution of β = 130, R_c = 0k82, r_π = 0k65, and R_e = 0k26 into equation 8 leads to a voltage gain of

$$A_v = \underline{-3.071} \quad (!)$$

Not a particularly impressive amplifier. However, if the capacitor C is now added into the circuit of the amplifier, in parallel with the emitter resistor R_e, then at AC signal frequencies it shorts-out R_e. This effect can be seen by setting R_e = 0 in equation 8.

So now, with the addition of 'bypass' capacitor C, the voltage gain becomes a much more healthy

$$A_v = \underline{\underline{-164.0}}$$

The AC Thévenin equivalent model of the amplifier's output is therefore active: it comprises a (signal) voltage source of value $V_{out} = -164V_{in}$ in series with a resistor. This resistor has a value equal to the resitance to ground seen looking into the output of the amplifier, *with <u>all</u> indpendent sources suppressed*. However, when the remaining independent source V_{in} is suppressed it turns off the *dependent* current source of value $i_c = g_m v_\pi$ in the model of the transistor, since v_π is then zero. In consequence this current source also becomes suppressed; and a suppressed current source is just an open-circuit.

Therefore, the resistance seen looking into the output of the amplifier in Figure 25, above, is simply equal to the value of the resistor R_c (0k82 ≡ 820Ω). Thus, the full AC model of the amplifier becomes that shown in Figure 27, below.

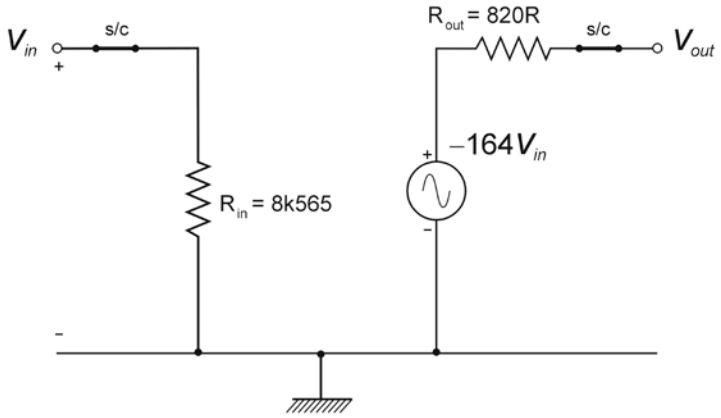


Figure 27. Full AC model of the amplifier: the output is a voltage source in anti-phase with the input signal, and with a voltage gain of 164. Thus, an AC input signal of 10 mV, peak-peak, would generate an amplifier output of 1.64 volts, peak-peak (and a 180° phase-shift from the input signal). The amplifier's output resistance = 820 Ω.

In Figure 27 the ± signs on the signal source (that represents the output of the amplifier) designate a reference polarity, relative to which the voltage gain from input to output is negative. Consequently, when the input signal V_{in} is positive relative to its own reference polarity, the output voltage source will generate a negative amplified voltage.

The complex frequency, s, and Bode analysis

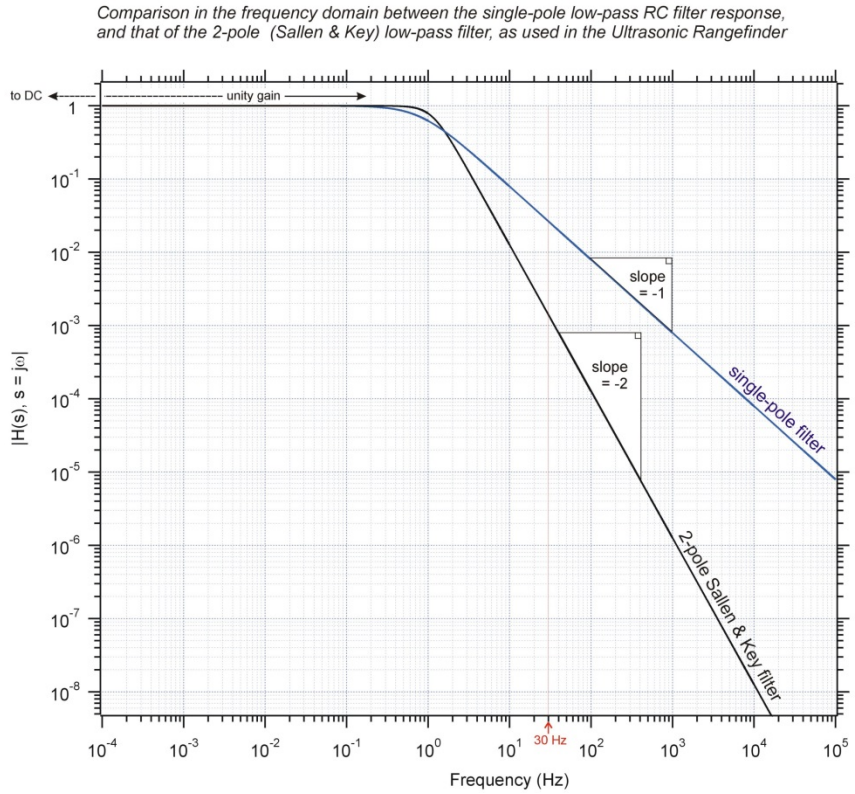


Figure 28. Bode magnitude plots: comparison in the frequency domain between the absolute magnitudes |H(s)| of the single-pole RC, and 2-pole Sallen & Key, low-pass filter gains, where s = jω. Please refer to the text.

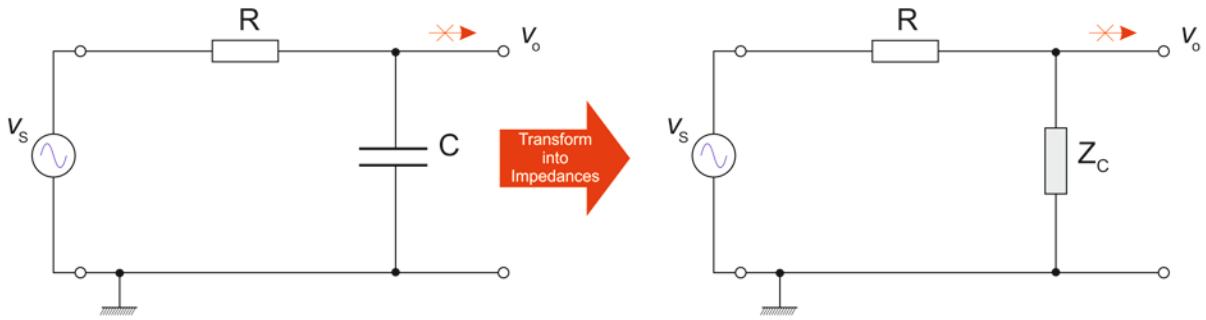


Figure 29. The output voltage of the RC low-pass filter in the left of the Figure can be found firstly by replacing the capacitor C by its impedance, $Z_C = 1/sC$, where s is the complex (angular) frequency, and then by using the potential-divider rule (Ohm's Law) to find the signal voltage appearing across the impedance Z_C (= V_o)—since the same signal current must flow through the series-connected resistance R and impedance, Z_C.

A low-pass RC filter is shown in Figure 29, with a sinusoidal source of voltage V_s applied to its input. Bode analysis involves finding the magnitude and phase of the output voltage, V_o. In what follows, just the magnitude will be considered.

In this example the 'system function' H(s) is the ratio of the output to the input signal for the low-pass filter shown in Figure 29, or: -

$$H(s) = \frac{V_o}{V_s}, = \frac{Z_C}{R + Z_C}.$$ However, by definition: $Z_C = \frac{1}{sC}$. The same 's' is used in LTs.

Therefore, $H(s) = \frac{1}{1 + sCR}$. This function has unity gain at DC (s = 0), and a single pole (hence the name used sometimes for this filter) at s = −1/RC, where the function H(s) 'blows up'. Such (complex) frequencies are the natural frequencies of the system, and all single-pole responses look the same—only the pole or 'break' frequency, ω_{pole} (= 1/RC, here) varies from one single-pole response to another.

Taking the absolute value (magnitude) of both sides of H(s): $|H(s)| = \left|\frac{1}{1 + sCR}\right|$, and this is plotted as the 'single-pole response' in the Bode magnitude plots shown in Figure 28 (here, for CR = 0.2 s). In this case the pole frequency lies at 0.796 Hz, and above this frequency the output signal is increasingly attenuated—by an additional factor of 10 for each increased factor of 10 in the input frequency. Therefore, the slope of this 'roll-off' towards high frequencies on the log-log plot is −1.

By contrast, the Sallen & Key filter has a 2-pole response, where the poles are complex conjugates of each other, at: $s = (-1 \pm j)\frac{1}{RC}$, where $j = \sqrt{-1}$. Its comparative performance also is shown in Figure 28. The two poles clearly lead to a sharper 'break point', and a much steeper attenuation with increasing frequency above the 'break point:' a factor of 100 increase in attenuation for each factor of 10 increase in frequency above this point, and so a slope of −2 on the log-log plot. However, like the single-pole RC filter, the Sallen & Key filter has unity gain at DC—and up to approximately 0.5 Hz, in fact: these filters pass low-frequency signals, undiminished (hence the name 'low-pass').

As another example, a high-pass filter is shown in Figure 30. This has no DC response, since the capacitor now lies between the input and output. However, like the low-pass RC filter, this circuit can be analysed

straightforwardly into poles and zeroes, and a Bode magnitude plot, expressing the magnitude of the frequency response (or gain) can be found for this filter, as follows.

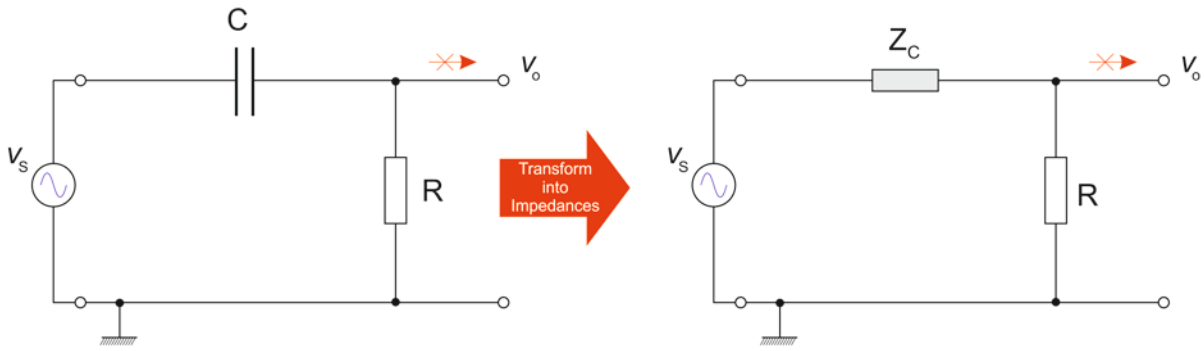


Figure 30. The output voltage of the CR high-pass filter in the left of the Figure can be found firstly by replacing the capacitor C by its impedance, 1/sC, where s is the complex (angular) frequency, and then by using the potential-divider rule to find the signal voltage appearing across the resistor R (= V_o).

From Figure 29: -

$$|H(s)| = \left|\frac{V_o}{V_s}\right|, = \left|\frac{R}{R + Z_C}\right| \text{ . However, } Z_C = \frac{1}{sC}.$$

$$\text{Therefore: } |H(s)| = \left|\frac{sCR}{1 + sCR}\right|. \qquad \text{(a)}$$

This function has a pole at s = −1/CR, like its equivalent low-pass filter, but it also has a zero at s = 0 (zeroes in the system function occur in the numerator: they are frequencies s at which there is no output at that frequency—hence the name). For a sinusoidal excitation of the system, s = jω, and so the numerator of H(s) has a magnitude of ωCR, which increases linearly across the full range of frequency, and so has a slope of +1 on a log-log Bode plot, such as that shown in Figure 31.

However, in the system function being analysed here the effects of the single pole and the single zero multiply. Therefore, their log(magnitudes) simply add when plotted in a Bode diagram, and above the pole frequency the slope of −1 from the pole is cancelled by the slope of +1 from the zero: the frequency response above the pole is therefore flat towards high frequencies. Indeed, by letting $s \rightarrow \infty$ in equation (a) above, it is clear that the magnitude of the high-pass response is unity above the pole frequency. Below the pole frequency, the high-pass response rolls-off towards low frequencies with a slope of +1, as shown in Figure 31. The passing of high frequency signals undiminished from input to output, whilst blocking (potentially different) DC levels, is why 'coupling' capacitors are often replaced by short-circuits in AC analysis, as in the analysis of the AC amplifier on p.32, et seq.

To take that example further: the input coupling capacitor of the AC amplifier shown in Figure 23 is 'looking into' an input AC resistance of R_{in} = 8.565 kΩ, as shown in Figure 26. If this capacitor has a capacitance of C_{in}, then it forms a high-pass filter with the AC input resistance of the amplifier, R_{in}—resembling the circuit on the left side of Figure 30, above. The pole of this high-pass filter is at: -

$$\omega_{pole} = 1/ C_{in}R_{in}. \qquad \text{(b)}$$

If the AC amplifier is supposed to amplify signals having frequencies above 1 kHz, say, then solving equation (b) for the required capacitance leads to C_{in} = 18.6 nF. This is the minimum acceptable value for C_{in}, and in practice a larger value would be chosen (the next larger standard value of capacitor would be 22 nF).

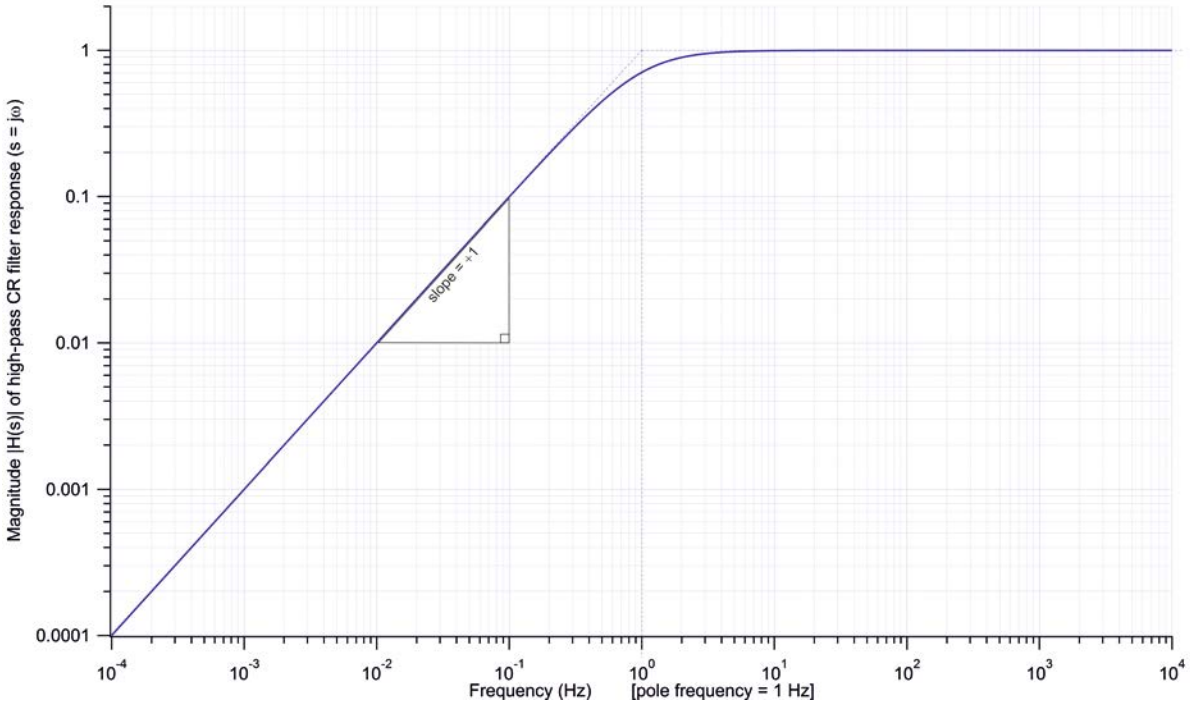


Figure 31. High-pass CR filter response, showing how high frequencies (frequencies greater than the pole, or 'break' frequency) are passed undiminished from input to output of this filter. There is no DC response, however, and the response falls away below the pole frequency due to the zero at s = 0 in the system function.