



CMOS G65SC02-A 8-BIT MICROPROCESSOR

FEATURES

- CMOS family that is compatible with NMOS 6500 series microprocessors
- Uses single +5 volt power supply
- Low power consumption (4mA @ 1 MHz) allows battery-powered operation
- Enhanced instruction set: 27 additional op codes encompassing eight new instructions enhance software performance compared to existing NMOS 6500 microprocessor instruction set
 - 64 microprocessors instructions
 - 178 operational codes
 - 15 addressing modes
- 65K-byte addressable memory
- 1, 2, 3, 4, 5 or 6 MHz operation
- Choice of external or on-board clock generator operation
- On-board clock generator/oscillator can be driven by an external single-phase clock input, an RC network, or a crystal circuit
- Early address valid allows use with slower memories
- Early write data for dynamic memories
- 8-bit parallel processing
- Decimal binary arithmetic
- Pipeline architecture
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800

GENERAL DESCRIPTION

The G65SCXX 8-bit microprocessor family is manufactured using the state-of-the-art silicon gate CMOS process. The G65SC02-A device is pin-to-pin compatible with NMOS versions of the 6500 currently on the market. The microprocessor is software compatible and provides 65K bytes of memory addressing and two interrupt inputs. It is bus compatible with MC6800 products.

As shown in Table I, the G65SC02-A clock generator circuit may be driven by an external crystal (Figure 2a), an RC network (Figure 2b) or by an external clock source. The G65SC02-A on-chip oscillator is intended for high performance, low cost operations where single phase inputs, crystals, or RC inputs provide the time base.

The microprocessor is pin-to-pin compatible with the NMOS 6500 microprocessors offered by several other manufacturers. However, the use of the leading-edge CMOS process technology ensures several software or programming enhancements not available to users of the NMOS 6500. The enhancements include two additional addressing modes, an expanded microprocessor instruction set (from 56 to 64 instructions), and expanded operational codes (from 151 to 178). In addition, a series of operational enhancements are provided which materially improve the effective use of the microprocessor. These enhancements are explained in Table V of the section of this data sheet devoted to system software and programming. This series of microprocessors provides the user an architecture and instruction set with which he is basically familiar (6502), the several operational enhancements notwithstanding, plus all of the advantages of leading edge CMOS technology; i.e., increased noise immunity, higher reliability, and greatly reduced power consumption.

In addition to enhanced software programming, the use of CMOS processing also allows several hardware enhancements that are not available to users of the NMOS 6500 products. These hardware enhancements are listed and explained in Table II.

The G65SC02-A microprocessor is available in plastic, ceramic, cerdip, or leadless chip carrier packaging. All versions are available in 1, 2, 3, 4, 5 and 6 MHz maximum operating frequencies.

Table 1. G65SC02-A Microprocessor Capabilities

Item No.	Part Number	DIP Pins	Addressable Memory (Bytes)	On-board Clock Oscillator (See Note)	External Clock Generator Required	Advanced Memory Access (φ4)	IRQ*	NMI*	SO*	DBE	BE	SYNC	RDY	ML*	RES*
1	G65SC02-A	40	65K	•			•	•	•			•	•		•

**Absolute Maximum Ratings: (See Note)**

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-55 to +150	°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating. Note: Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: $V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ Industrial, 0° to $+70^\circ\text{C}$ Commercial

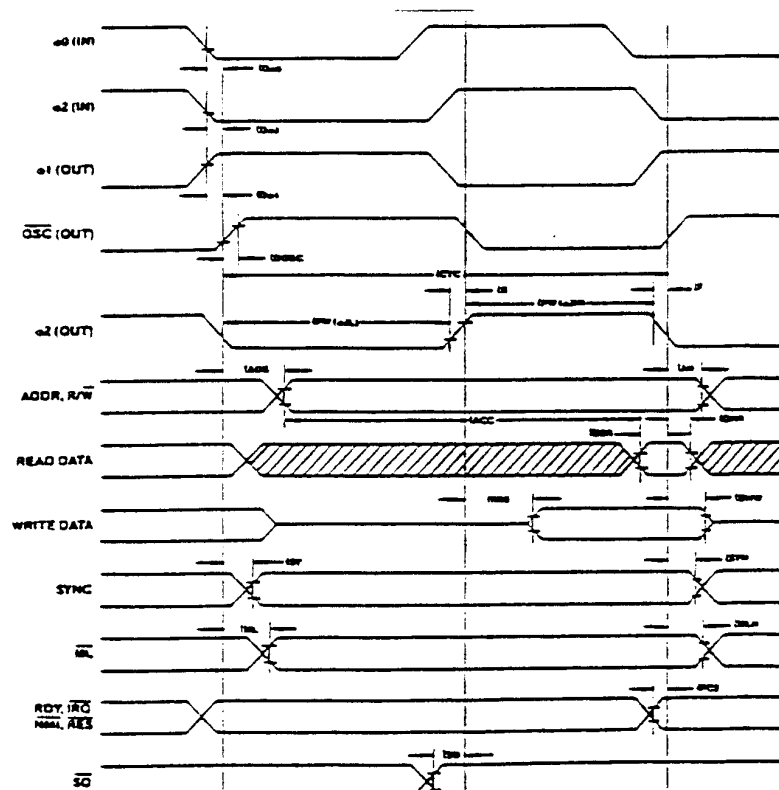
Parameter	Symbol	Min	Max	Unit
Input High Voltage $\phi 0(\text{IN})$, CLK (IN) RES*, NMI*, RDY, IRQ*, Data, SO*	V_{IH}	2.4 1.9	$V_{DD} + 0.3$ $V_{DD} + 0.3$	V V
Input Low Voltage $\phi 0$, (IN), CLK (IN) RES*, NMI*, RDY, IRQ*, Data, SO*	V_{IL}	-0.3 -0.3	0.4 0.9	V V
Input Leakage Current ($V_{IN} = 0$ to V_{DD}) RES*, NMI*, RDY, IRQ*, SO* $\phi 0$ (IN), CLK (IN) [02, 12, 112]	I_{IN}		1.0/-100 ± 1.0	μA μA
Three-State Leakage Current Address, Data, R/W*	I_{TSI}		± 10.0	μA
Output High Voltage ($I_{OH} = -100\mu\text{A}$, $V_{DD} = 4.75V$) SYNC, Data, A0-A15, R/W*	V_{OH}	2.4	-	V
Output Low Voltage ($I_{OL} = 1.6\text{mA}$, $V_{DD} = 4.5V$) SYNC, Data, A0-A15, R/W*	V_{OL}	-	0.4	V
Supply Current (No Load) $f = 1\text{ MHz}$ $f = 2\text{ MHz}$ $f = 3\text{ MHz}$ $f = 4\text{ MHz}$	I_{DD}	-	4 8 12 16	mA
Standby Power Dissipation (Inputs = V_{SS} or V_{DD} Outputs Unloaded)	P_{SBY}		50.0	μW
Capacitance ($V_{IN} = 0$, $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$) Logic, $\phi 0$ (IN), CLK (IN) A0-A15, R/W* Data (Three-State)	C_{IN} C_{TS}	- -	10 15	pF

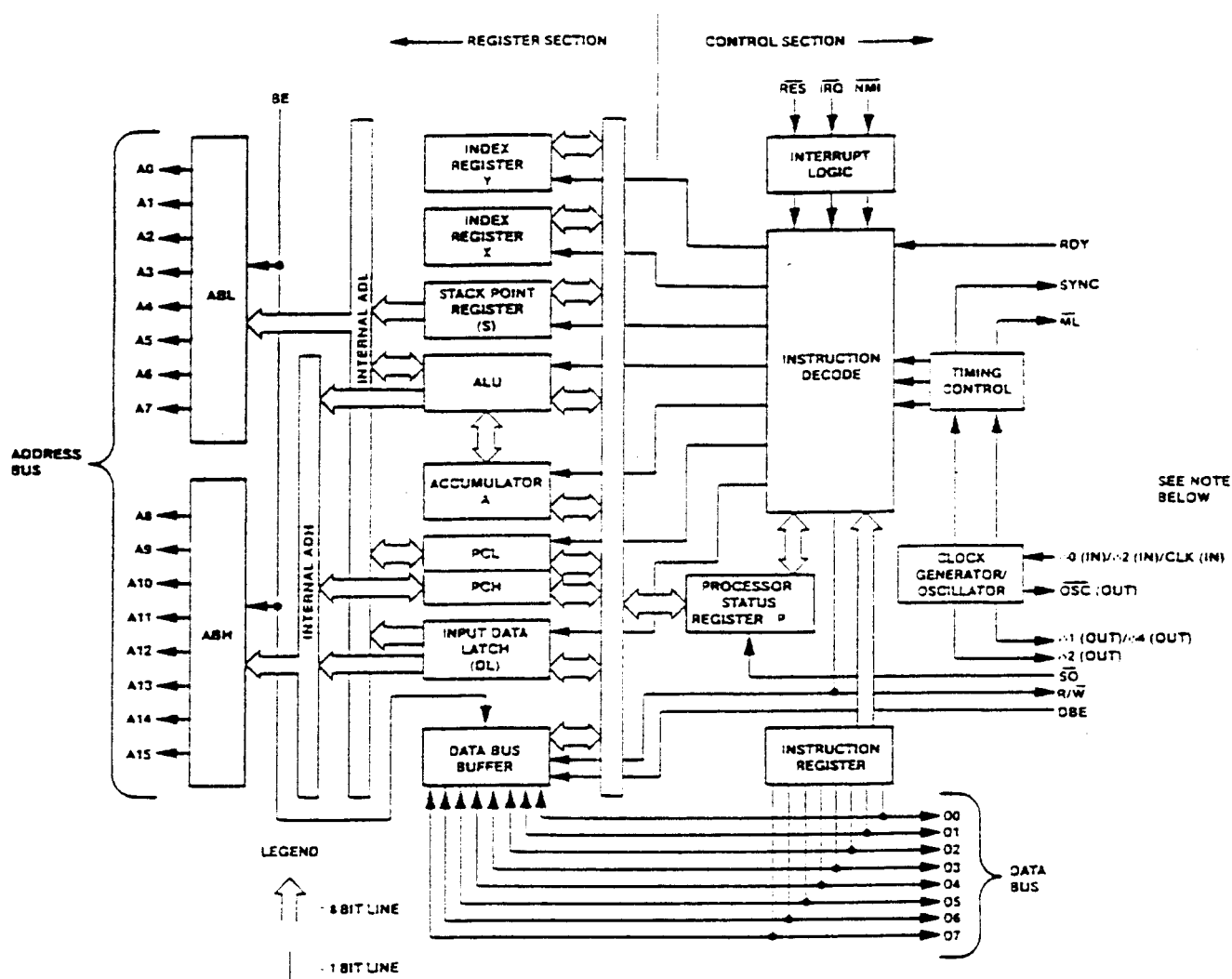


AC Characteristics: $V_{DD} = 5.0V \pm 5\%$, $T_A = -40^\circ C$ to $\pm 85^\circ C$ Industrial, $0^\circ C$ to $\pm 70^\circ C$ Commercial

		1 MHz		2 MHz		3 MHz		4 MHz		5 MHz		6 MHz		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Delay Time, $\phi 0$ (IN) to $\phi 2$ (OUT)	$t_{\phi 00}$	—	40	—	40	—	40	—	40	—	35	—	30	ns
Delay Time, $\phi 2$ (IN) to $\phi 2$ (OUT)	$t_{\phi 22}$	—	35	—	35	—	35	—	35	—	35	—	30	ns
Delay Time, $\phi 1$ (OUT) to $\phi 2$ (OUT)	$t_{\phi 01}$	—	50	—	50	—	50	—	50	—	35	—	30	ns
Delay Time, $\phi 2$ (OUT) to \overline{OSC} (OUT)	$t_{\phi 0SC}$	—	50	—	50	—	50	—	50	—	35	—	30	ns
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	0.33	DC	0.25	DC	0.20	DC	0.167	DC	ns
Clock Pulse Width Low	$t_{PW}(\phi 2L)$	430	10000	210	10000	150	10000	100	10000	90	10000	80	10000	ns
Clock Pulse Width High	$t_{PW}(\phi 2H)$	450	—	220	—	160	—	110	—	85	—	75	—	ns
Fall Time, Rise Time	t_F, t_R	—	25	—	20	—	15	—	12	—	10	—	10	ns
Address Hold Time	t_{AH}	15	—	15	—	15	—	15	—	5	—	5	—	ns
Address Setup Time	t_{AS}	—	125	—	100	—	85	—	70	—	60	—	55	ns
Access Time	t_{ACC}	775	—	340	—	200	—	140	—	110	—	85	—	ns
Read Data Hold Time	t_{DHR}	10	—	10	—	10	—	10	—	5	—	5	—	ns
Read Data Setup Time	t_{DSR}	100	—	60	—	40	—	30	—	27	—	25	—	ns
Write Data Delay Time	t_{WDS}	—	175	—	100	—	75	—	55	—	50	—	45	ns
Write Data Hold Time	t_{DHW}	30	—	30	—	30	—	30	—	15	—	15	—	ns
SYNC, \overline{ML} Setup Time	$t_{SY, \overline{ML}}$	—	125	—	100	—	85	—	70	—	60	—	55	ns
SYNC, \overline{ML} Hold Time	$t_{SYH, \overline{ML}H}$	10	—	10	—	10	—	10	—	5	—	5	—	ns
\overline{SC} Setup Time	t_{SO}	75	—	50	—	35	—	25	—	22	—	20	—	ns
Processor Control Setup Time	t_{PSC}	200	—	110	—	80	—	60	—	55	—	50	—	ns

Timing Diagram:





Note: Refer to Table I for signal input/output applicability.

Figure 1. Internal Architecture Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Timing Control

The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase one clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter

The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

**Arithmetic and Logic Unit (ALU)**

All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers

There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address,

and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts (NMI* and IRQ*). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

SIGNAL DESCRIPTION**Address Bus (A0-AXX)**

Refer to the particular package configuration for the respective number of address lines.

In both the 40-pin and 44-pin packages, A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The address lines are set (See BE below) to the high impedance state by the bus enable (BE) signal. The output of each address line is TTL compatible, capable of driving one standard TTL load and 130 pF.

Bus Enable (BE)

This signal allows external control of the data and the address output buffers and R/W*. For normal operation, BE is high causing the address buffers and R/W* to be active and the data buffers to be active during a write cycle. For external control, BE is held low to disable the buffers.

Phase 0 in ($\phi 0$ (IN))

This is the buffered clock input to the internal clock generator on the G65SC02-A series. Clock outputs $\phi 1$ (OUT) and $\phi 2$ (OUT) are derived from this signal.

Data Bus (D0-D7)

The data lines (D0-D7) constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 103 pF.

Interrupt Request (IRQ*)

This TTL compatible signal requests that an interrupt sequence begin within the microprocessor. The IRQ* is sampled during $\phi 2$ operation. If the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt

sequence begins during $\phi 1$. The program counter and processor status register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, transferring program control the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K ohm external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt (NMI*)

A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The NMI* is sampled during $\phi 2$; the current instruction is completed and the interrupt sequence begins during $\phi 1$. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. However, it should be noted this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. Also, no interrupt will occur if NMI* is low and negative-going edge has not occurred since the last non-maskable interrupt.

Phase 1 Out ($\phi 1$ (OUT))

This inverted $\phi 2$ (OUT) signal provides timing for external R/W* operations.

Phase 2 Out ($\phi 2$ (OUT))

This signal provides timing for external bus R/W* operations. Addresses are valid after the address setup time (t_{ADS}) from the falling edge of $\phi 2$ (OUT).



SIGNAL DESCRIPTION (cont.)

Ready (RDY)

This input signal allows the user to single-cycle the microprocessor on all cycles including write cycles. A negative transition to the low state during or coincident with phase one ($\phi 1$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\phi 2$) in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).

Reset (RES*)

This input is used to reset the microprocessor. Reset must be held low for at least two clock cycles after V_{DD} reaches operating voltage from a power down. A positive transition on this pin will then cause an initialization sequence to begin. After the system has been operating, a low on this line of at least two cycles will cease microprocessing activity.

When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The previous program counter and status register values are written to the stack memory area. Then the interrupt mask flag is set, the decimal mode is cleared and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the

start location for program control. This input should be high in normal operation.

Read/Write (R/W*)

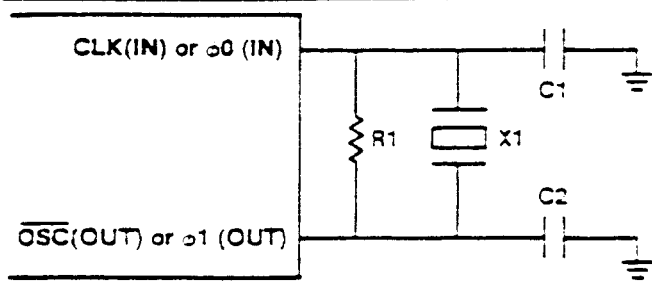
This signal is normally in the high state indicating that the microprocessor is reading data from memory or I/O bus. In the low state the data bus has valid data from the microprocessor to be stored at the addressed memory location. R/W* is set to the high impedance state by BE.

Set Overflow (SO*)

A negative transition on this line sets the overflow bit in the status code register. The signal is sampled on the trailing edge of $\phi 1$.

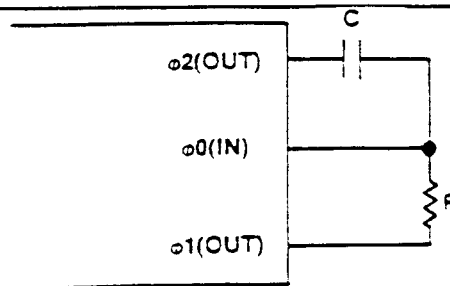
Synchronize (SYNC)

This output line is provided to identify those cycles during which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\phi 1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\phi 1$ clock awls in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.



C1, C2 = 51pF
R1 = 200K Ω
X1 = 1MHz

Figure 2(a). Crystal Circuit for Internal Oscillator



Suggested RC network configuration for internal oscillator.

1 MHz operation at $V_{DD} = 5.0V$:
C = 56pF
R = 5.6 K Ω

Figure 2(b). RC Circuit for Internal Oscillator

Table II. Microprocessor Hardware Enhancements

Function	NMOS 6500	G65SC02-A
Oscillator.	Requires external active components.	Crystal or RC network will oscillate when connected between $\phi 0$ (IN) and $\phi 1$ (OUT).
Assertion of Ready (RDY) during write operations.	Ignored.	Stops processor during $\phi 2$.
Unused input-only pins (IRQ*, NMI*, RDY, RES*, SO*, DBE, BE).	Must be connected to low impedance signal to avoid noise problems.	Connected internally by a high-resistance to V_{DD} (approximately 1 Megohm).

* Denotes inverted signal.



ADDRESSING MODES

Fifteen addressing modes are available to the user of the CMD G65SC02-A family of microprocessors. The addressing modes are described in the following paragraphs:

Implied Addressing

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

Accumulator Addressing

This form of addressing is represented with a one byte instruction and implies an operation of the accumulator.

Immediate Addressing

With immediate addressing, the operand is contained in the second byte of the instruction; no further memory addressing is required.

Absolute Addressing

For absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Therefore, this addressing mode allows access to the total 65K bytes of addressable memory.

Zero Page Addressing

Zero page addressing allows shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. The careful use of zero page addressing can result in significant increase in code efficiency.

Absolute Indexed Addressing

Absolute indexed addressing is used in conjunction with X and Y index register and is referred to as "Absolute.X." and "Absolute.Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

Zero Page Indexed Addressing

Zero page absolute addressing is used in conjunction with the index register and is referred to as "Zero Page.X" or "Zero Page.Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order eight bits of memory and crossing of page

boundaries does not occur.

Relative Addressing

Relative addressing is used only with branch instruction; it establishes a destination for the conditional branch.

Zero Page Indexed Indirect Addressing

With zero page indexed indirect addressing (usually referred to as indirect X) the second byte of the instruction is added to the contents of the X index register; the carry is discarded. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

Absolute Indexed Indirect Addressing (Jump Instruction Only)

With absolute indexed indirect addressing, the contents of the second and third instruction bytes are added to the X register. The result of this addition points to a memory location containing the lower-order eight bits of the effective address. The next memory location contains the higher-order eight bits of the effective address.

Indirect Indexed Addressing

This form of addressing is usually referred to as Indirect.Y. The second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

Zero Page Indirect Addressing

In this form of addressing, the second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits is always zero. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address.

Absolute Indirect Addressing (Jump Instruction Only)

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the 16 bits of the program counter.

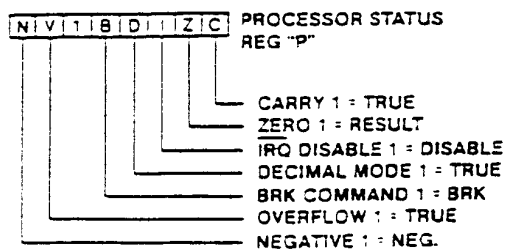
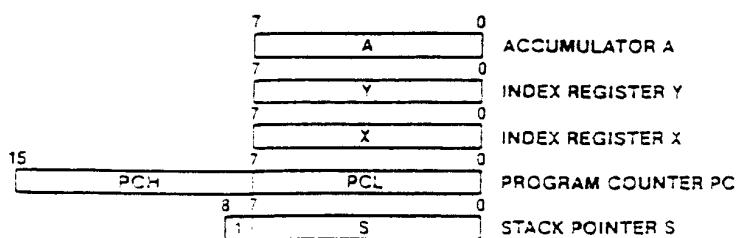


Figure 3. Microprocessor Programming Model

• Denotes inverted signal.



Table III. Instruction Set—Alphabetical Sequence

AOC	Add Memory to Accumulator with Carry	LDY	Load Index Y with Memory
AND	"AND" Memory with Accumulator	LSR	Shift One Bit Right
ASL	Shift One Bit Left	NOP	No Operation
BCC	Branch on Carry Clear	ORA	"OR" Memory with Accumulator
BCS	Branch on Carry Set	PHA	Push Accumulator on Stack
BEQ	Branch on Result Zero	PHP	Push Processor Status on Stack
BIT	Test Memory Bits with Accumulator	• PHX	Push Index X on Stack
BMI	Branch on Result Minus	• PHY	Push Index Y on Stack
BNE	Branch on Result Not Zero	PLA	Pop Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pop Processor Status from Stack
• BRA	Branch Always	• PLX	Pop Index X from Stack
BRK	Force Break	• PLY	Pop Index Y from Stack
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Left
BVS	Branch on Overflow Set	ROR	Rotate One Bit Right
CLC	Clear Carry Flag	RTI	Return from Interrupt
CLE	Clear External Mode	RTS	Return from Subroutine
CLI	Clear Interrupt Disable Bit	SBC	Subtract Memory from Accumulator with Borrow
CLV	Clear Overflow Flag	SEC	Set Carry Flag
CMP	Compare Memory and Accumulator	SED	Set External Mode
CPX	Compare Memory and Index X	SEI	Set Interrupt Disable Bit
CPY	Compare Memory and Index Y	STA	Store Accumulator in Memory
DEC	Decrement by One	STX	Store Index X in Memory
DEX	Decrement Index X by One	STY	Store Index Y in Memory
DEY	Decrement Index Y by One	• STZ	Store Zero in Memory
EOR	"Exclusive-OR" Memory with Accumulator	TAX	Transfer Accumulator to Index X
INC	Increment by One	TAY	Transfer Accumulator to Index Y
INX	Increment Index X by One	• TRB	Test and Reset Memory Bits with Accumulator
INY	Increment Index Y by One	• TSB	Test and Set Memory Bits with Accumulator
JMP	Jump to New Location	TSX	Transfer Stack Pointer to Index X
JSR	Jump to New Location Saving Return Address	TXA	Transfer Index X to Accumulator
LDA	Load Accumulator with Memory	TXS	Transfer Index X to Stack Pointer
LDX	Load Index X with Memory	TYA	Transfer Index Y to Accumulator

Note: • = New Instruction

Op Code	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	BRK ind. X	ORA ind. Y			SEI ind. X	ORA zdg. X	ASL zdg.		PHP imm	ORA imm	ASL A			ORA zds. X	ASL zds.	0
1	BPL rel	ORA ind. Y				ORA zdg. X	ASL zdg. X		CLC	ORA zds. Y				ORA zds. X	ASL zds. X	1
2	JSR zds.	AND ind. X			BIT zdg.	AND zdg.	RCL zdg.		PLP	AND imm	RCL A		BIT zds.	AND zds.	RCL zds.	2
3	BMI rel	AND ind. Y				AND zdg. X	RCL zdg. X		SEC	AND zds. Y				AND zds. X	RCL zds. X	3
4	RTI	EOR ind. X				EOR zdg.	LSR zdg.		PHA	EOR imm	LSR A		JMP zds.	EOR zds.	LSR zds.	4
5	BVC rel	EOR ind. Y				EOR zdg. X	LSR zdg. X		CLI	EOR zds. Y				EOR zds. X	LSR zds. X	5
6	RTS	ADC ind. X				ADC zdg.	ROR zdg.		PLA	ADC imm	ROR A		JMP ind.	ADC zds.	ROR zds.	6
7	BVS rel	ADC ind. Y				ADC zdg. X	ROR zdg. X		SEI	ADC zds. Y				ADC zds. X	ROR zds. X	7
8	BRA rel	STA ind. X			STY zdg.	STA zdg.	STX zdg.		DEY		TXA		STY zds.	STA zds.	STX zds.	8
9	BCC rel	STA ind. Y			STY zdg. X	STA zdg. X	STX zdg. Y		TYA	STA zds. Y	TXS			STA zds. X		9
A	LDY imm	LDA ind. X	LDX imm		LDY zdg.	LDA zdg.	LDX zdg.		TAY	LDA imm	TAX		LDY zds.	LDA zds.	LDX zds.	A
B	BCS rel	LDA ind. Y			LDY zdg. X	LDA zdg. X	LDX zdg. Y		CLV	LDA zds. Y	TSX		LDY zds. X	LDA zds. X	LDX zds. Y	B
C	CPY imm	CMP ind. X			CPY zdg.	CMP zdg.	DEC zdg.		INX	CMP imm	DEX		CPY zds.	CMP zds.	DEC zds.	C
D	BNE rel	CMP ind. Y				CMP zdg. X	DEC zdg. X		CLE	CMP zds. Y				CMP zds. X	DEC zds. X	D
E	CPX imm	SBC ind. X			CPX zdg.	SBC zdg.	INC zdg.		INX	SBC imm	NOP		CPX zds.	SBC zds.	INC zds.	E
F	BEQ rel	SBC ind. Y				SBC zdg. X	INC zdg. X		SED	SBC zds. Y				SBC zds. X	INC zds. X	F

Note: □ = New Op Codes

Figure 4. Microprocessor Op Code Table

• Denotes inverted signal.



Table IV. Operational Codes, Execution Time, and Memory Requirements

		IMME- DATE	ABS- LUTE	ZERO PAGE	(4) IMPLUED	(1) (IND. X)	(1) (IND. Y)	(1) ZPG. X	(1) ABS. X	(1) ABS. Y	REL- TIVE (2)	IND- RECT	ZPG. Y	PROCESSOR STATUS CODE								MNE- MONIC																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																				
MNE- MONIC	OPERATION	OPIN1	OPIN2	OPIN3	OPIN4	OPIN5	OPIN6	OPIN7	OPIN8	OPIN9	OPIN10	OPIN11	OPIN12	OPIN13	OPIN14	OPIN15	OPIN16	OPIN17	OPIN18	OPIN19	OPIN20	OPIN21	OPIN22	OPIN23	OPIN24	OPIN25	OPIN26	OPIN27	OPIN28	OPIN29	OPIN30	OPIN31	OPIN32	OPIN33	OPIN34	OPIN35	OPIN36	OPIN37	OPIN38	OPIN39	OPIN40	OPIN41	OPIN42	OPIN43	OPIN44	OPIN45	OPIN46	OPIN47	OPIN48	OPIN49	OPIN50	OPIN51	OPIN52	OPIN53	OPIN54	OPIN55	OPIN56	OPIN57	OPIN58	OPIN59	OPIN60	OPIN61	OPIN62	OPIN63	OPIN64	OPIN65	OPIN66	OPIN67	OPIN68	OPIN69	OPIN70	OPIN71	OPIN72	OPIN73	OPIN74	OPIN75	OPIN76	OPIN77	OPIN78	OPIN79	OPIN80	OPIN81	OPIN82	OPIN83	OPIN84	OPIN85	OPIN86	OPIN87	OPIN88	OPIN89	OPIN90	OPIN91	OPIN92	OPIN93	OPIN94	OPIN95	OPIN96	OPIN97	OPIN98	OPIN99	OPIN100	OPIN101	OPIN102	OPIN103	OPIN104	OPIN105	OPIN106	OPIN107	OPIN108	OPIN109	OPIN110	OPIN111	OPIN112	OPIN113	OPIN114	OPIN115	OPIN116	OPIN117	OPIN118	OPIN119	OPIN120	OPIN121	OPIN122	OPIN123	OPIN124	OPIN125	OPIN126	OPIN127	OPIN128	OPIN129	OPIN130	OPIN131	OPIN132	OPIN133	OPIN134	OPIN135	OPIN136	OPIN137	OPIN138	OPIN139	OPIN140	OPIN141	OPIN142	OPIN143	OPIN144	OPIN145	OPIN146	OPIN147	OPIN148	OPIN149	OPIN150	OPIN151	OPIN152	OPIN153	OPIN154	OPIN155	OPIN156	OPIN157	OPIN158	OPIN159	OPIN160	OPIN161	OPIN162	OPIN163	OPIN164	OPIN165	OPIN166	OPIN167	OPIN168	OPIN169	OPIN170	OPIN171	OPIN172	OPIN173	OPIN174	OPIN175	OPIN176	OPIN177	OPIN178	OPIN179	OPIN180	OPIN181	OPIN182	OPIN183	OPIN184	OPIN185	OPIN186	OPIN187	OPIN188	OPIN189	OPIN190	OPIN191	OPIN192	OPIN193	OPIN194	OPIN195	OPIN196	OPIN197	OPIN198	OPIN199	OPIN200	OPIN201	OPIN202	OPIN203	OPIN204	OPIN205	OPIN206	OPIN207	OPIN208	OPIN209	OPIN210	OPIN211	OPIN212	OPIN213	OPIN214	OPIN215	OPIN216	OPIN217	OPIN218	OPIN219	OPIN220	OPIN221	OPIN222	OPIN223	OPIN224	OPIN225	OPIN226	OPIN227	OPIN228	OPIN229	OPIN230	OPIN231	OPIN232	OPIN233	OPIN234	OPIN235	OPIN236	OPIN237	OPIN238	OPIN239	OPIN240	OPIN241	OPIN242	OPIN243	OPIN244	OPIN245	OPIN246	OPIN247	OPIN248	OPIN249	OPIN250	OPIN251	OPIN252	OPIN253	OPIN254	OPIN255	OPIN256	OPIN257	OPIN258	OPIN259	OPIN260	OPIN261	OPIN262	OPIN263	OPIN264	OPIN265	OPIN266	OPIN267	OPIN268	OPIN269	OPIN270	OPIN271	OPIN272	OPIN273	OPIN274	OPIN275	OPIN276	OPIN277	OPIN278	OPIN279	OPIN280	OPIN281	OPIN282	OPIN283	OPIN284	OPIN285	OPIN286	OPIN287	OPIN288	OPIN289	OPIN290	OPIN291	OPIN292	OPIN293	OPIN294	OPIN295	OPIN296	OPIN297	OPIN298	OPIN299	OPIN300	OPIN301	OPIN302	OPIN303	OPIN304	OPIN305	OPIN306	OPIN307	OPIN308	OPIN309	OPIN310	OPIN311	OPIN312	OPIN313	OPIN314	OPIN315	OPIN316	OPIN317	OPIN318	OPIN319	OPIN320	OPIN321	OPIN322	OPIN323	OPIN324	OPIN325	OPIN326	OPIN327	OPIN328	OPIN329	OPIN330	OPIN331	OPIN332	OPIN333	OPIN334	OPIN335	OPIN336	OPIN337	OPIN338	OPIN339	OPIN340	OPIN341	OPIN342	OPIN343	OPIN344	OPIN345	OPIN346	OPIN347	OPIN348	OPIN349	OPIN350	OPIN351	OPIN352	OPIN353	OPIN354	OPIN355	OPIN356	OPIN357	OPIN358	OPIN359	OPIN360	OPIN361	OPIN362	OPIN363	OPIN364	OPIN365	OPIN366	OPIN367	OPIN368	OPIN369	OPIN370	OPIN371	OPIN372	OPIN373	OPIN374	OPIN375	OPIN376	OPIN377	OPIN378	OPIN379	OPIN380	OPIN381	OPIN382	OPIN383	OPIN384	OPIN385	OPIN386	OPIN387	OPIN388	OPIN389	OPIN390	OPIN391	OPIN392	OPIN393	OPIN394	OPIN395	OPIN396	OPIN397	OPIN398	OPIN399	OPIN400	OPIN401	OPIN402	OPIN403	OPIN404	OPIN405	OPIN406	OPIN407	OPIN408	OPIN409	OPIN410	OPIN411	OPIN412	OPIN413	OPIN414	OPIN415	OPIN416	OPIN417	OPIN418	OPIN419	OPIN420	OPIN421	OPIN422	OPIN423	OPIN424	OPIN425	OPIN426	OPIN427	OPIN428	OPIN429	OPIN430	OPIN431	OPIN432	OPIN433	OPIN434	OPIN435	OPIN436	OPIN437	OPIN438	OPIN439	OPIN440	OPIN441	OPIN442	OPIN443	OPIN444	OPIN445	OPIN446	OPIN447	OPIN448	OPIN449	OPIN450	OPIN451	OPIN452	OPIN453	OPIN454	OPIN455	OPIN456	OPIN457	OPIN458	OPIN459	OPIN460	OPIN461	OPIN462	OPIN463	OPIN464	OPIN465	OPIN466	OPIN467	OPIN468	OPIN469	OPIN470	OPIN471	OPIN472	OPIN473	OPIN474	OPIN475	OPIN476	OPIN477	OPIN478	OPIN479	OPIN480	OPIN481	OPIN482	OPIN483	OPIN484	OPIN485	OPIN486	OPIN487	OPIN488	OPIN489	OPIN490	OPIN491	OPIN492	OPIN493	OPIN494	OPIN495	OPIN496	OPIN497	OPIN498	OPIN499	OPIN500	OPIN501	OPIN502	OPIN503	OPIN504	OPIN505	OPIN506	OPIN507	OPIN508	OPIN509	OPIN510	OPIN511	OPIN512	OPIN513	OPIN514	OPIN515	OPIN516	OPIN517	OPIN518	OPIN519	OPIN520	OPIN521	OPIN522	OPIN523	OPIN524	OPIN525	OPIN526	OPIN527	OPIN528	OPIN529	OPIN530	OPIN531	OPIN532	OPIN533	OPIN534	OPIN535	OPIN536	OPIN537	OPIN538	OPIN539	OPIN540	OPIN541	OPIN542	OPIN543	OPIN544	OPIN545	OPIN546	OPIN547	OPIN548	OPIN549	OPIN550	OPIN551	OPIN552	OPIN553	OPIN554	OPIN555	OPIN556	OPIN557	OPIN558	OPIN559	OPIN560	OPIN561	OPIN562	OPIN563	OPIN564	OPIN565	OPIN566	OPIN567	OPIN568	OPIN569	OPIN570	OPIN571	OPIN572	OPIN573	OPIN574	OPIN575	OPIN576	OPIN577	OPIN578	OPIN579	OPIN580	OPIN581	OPIN582	OPIN583	OPIN584	OPIN585	OPIN586	OPIN587	OPIN588	OPIN589	OPIN590	OPIN591	OPIN592	OPIN593	OPIN594	OPIN595	OPIN596	OPIN597	OPIN598	OPIN599	OPIN600	OPIN601	OPIN602	OPIN603	OPIN604	OPIN605	OPIN606	OPIN607	OPIN608	OPIN609	OPIN610	OPIN611	OPIN612	OPIN613	OPIN614	OPIN615	OPIN616	OPIN617	OPIN618	OPIN619	OPIN620	OPIN621	OPIN622	OPIN623	OPIN624	OPIN625	OPIN626	OPIN627	OPIN628	OPIN629	OPIN630	OPIN631	OPIN632	OPIN633	OPIN634	OPIN635	OPIN636	OPIN637	OPIN638	OPIN639	OPIN640	OPIN641	OPIN642	OPIN643	OPIN644	OPIN645	OPIN646	OPIN647	OPIN648	OPIN649	OPIN650	OPIN651	OPIN652	OPIN653	OPIN654	OPIN655	OPIN656	OPIN657	OPIN658	OPIN659	OPIN660	OPIN661	OPIN662	OPIN663	OPIN664	OPIN665	OPIN666	OPIN667	OPIN668	OPIN669	OPIN670	OPIN671	OPIN672	OPIN673	OPIN674	OPIN675	OPIN676	OPIN677	OPIN678	OPIN679	OPIN680	OPIN681	OPIN682	OPIN683	OPIN684	OPIN685	OPIN686	OPIN687	OPIN688	OPIN689	OPIN690	OPIN691	OPIN692	OPIN693	OPIN694	OPIN695	OPIN696	OPIN697	OPIN698	OPIN699	OPIN700	OPIN701	OPIN702	OPIN703	OPIN704	OPIN705	OPIN706	OPIN707	OPIN708	OPIN709	OPIN710	OPIN711	OPIN712	OPIN713	OPIN714	OPIN715	OPIN716	OPIN717	OPIN718	OPIN719	OPIN720	OPIN721	OPIN722	OPIN723	OPIN724	OPIN725	OPIN726	OPIN727	OPIN728	OPIN729	OPIN730	OPIN731	OPIN732	OPIN733	OPIN734	OPIN735	OPIN736	OPIN737	OPIN738	OPIN739	OPIN740	OPIN741	OPIN742	OPIN743	OPIN744	OPIN745	OPIN746	OPIN747	OPIN748	OPIN749	OPIN750	OPIN751	OPIN752	OPIN753	OPIN754	OPIN755	OPIN756	OPIN757	OPIN758	OPIN759	OPIN760	OPIN761	OPIN762	OPIN763	OPIN764	OPIN765	OPIN766	OPIN767	OPIN768	OPIN769	OPIN770	OPIN771	OPIN772	OPIN773	OPIN774	OPIN775	OPIN776	OPIN777	OPIN778	OPIN779	OPIN780	OPIN781	OPIN782	OPIN783	OPIN784	OPIN785	OPIN786	OPIN787	OPIN788	OPIN789	OPIN790	OPIN791	OPIN792	OPIN793	OPIN794	OPIN795	OPIN796	OPIN797	OPIN798	OPIN799	OPIN800	OPIN801	OPIN802	OPIN803	OPIN804	OPIN805	OPIN806	OPIN807	OPIN808	OPIN809	OPIN810	OPIN811	OPIN812	OPIN813	OPIN814	OPIN815	OPIN816	OPIN817	OPIN818	OPIN819	OPIN820	OPIN821	OPIN822	OPIN823	OPIN824	OPIN825	OPIN826	OPIN827	OPIN828	OPIN829	OPIN830	OPIN831	OPIN832	OPIN833	OPIN834	OPIN835	OPIN836	OPIN837	OPIN838	OPIN839	OPIN840	OPIN841	OPIN842	OPIN843	OPIN844	OPIN845	OPIN846	OPIN847	OPIN848	OPIN849	OPIN850	OPIN851	OPIN852	OPIN853	OPIN854	OPIN855	OPIN856	OPIN857	OPIN858	OPIN859	OPIN860	OPIN861	OPIN862	OPIN863	OPIN864	OPIN865	OPIN866	OPIN867	OPIN868	OPIN869	OPIN870	OPIN871	OPIN872	OPIN873	OPIN874	OPIN875	OPIN876	OPIN877	OPIN878	OPIN879	OPIN880	OPIN881	OPIN882	OPIN883	OPIN884	OPIN885	OPIN886	OPIN887	OPIN888	OPIN889	OPIN890	OPIN891	OPIN892	OPIN893	OPIN894	OPIN895	OPIN896	OPIN897	OPIN898	OPIN899	OPIN900	OPIN901	OPIN902	OPIN903	OPIN904	OPIN905	OPIN906	OPIN907	OPIN908	OPIN909	OPIN910	OPIN911	OPIN912	OPIN913	OPIN914	OPIN915	OPIN916	OPIN917	OPIN918	OPIN919	OPIN920	OPIN921	OPIN922	OPIN923	OPIN924	OPIN925	OPIN926	OPIN927	OPIN928	OPIN929	OPIN930	OPIN931	OPIN932	OPIN933	OPIN934	OPIN935	OPIN936	OPIN937	OPIN938	OPIN939	OPIN940	OPIN941	OPIN942	OPIN943	OPIN944	OPIN945	OPIN946	OPIN947	OPIN948	OPIN949	OPIN950	OPIN951	OPIN952	OPIN953	OPIN954	OPIN955	OPIN956	OPIN957	OPIN958	OPIN959	OPIN960	OPIN961	OPIN962	OPIN963	OPIN964	OPIN965	OPIN966	OPIN967	OPIN968	OPIN969	OPIN970	OPIN971	OPIN972	OPIN973	OPIN974	OPIN975	OPIN976	OPIN977	OPIN978	OPIN979	OPIN980	OPIN981	OPIN982	OPIN983	OPIN984	OPIN985	OPIN986	OPIN987	OPIN988	OPIN989	OPIN990	OPIN991	OPIN992	OPIN993	OPIN994	OPIN995	OPIN996	OPIN997	OPIN998	OPIN999	OPIN1000	OPIN1001	OPIN1002	OPIN1003	OPIN1004	OPIN1005	OPIN1006	OPIN1007	OPIN1008	OPIN1009	OPIN1010	OPIN1011	OPIN1012	OPIN1013	OPIN1014	OPIN1015	OPIN1016	OPIN1017	OPIN1018	OPIN1019	OPIN1020	OPIN1021	OPIN1022	OPIN1023	OPIN1024	OPIN1025	OPIN1026	OPIN1027	OPIN1028	OPIN1029	OPIN1030	OPIN1031	OPIN1032	OPIN1033	OPIN1034	OPIN1035	OPIN1036	OPIN1037	OPIN1038	OPIN1039	OPIN1040	OPIN1041	OPIN1042	OPIN1043	OPIN1044	OPIN1045	OPIN1046	OPIN1047	OPIN1048	OPIN1049	OPIN1050	OPIN1051	OPIN1052	OPIN1053	OPIN1054	OPIN1055	OPIN1056	OPIN1057	OPIN1058	OPIN1059	OPIN1060	OPIN1061	OPIN1062	OPIN1063	OPIN1064	OPIN1065	OPIN1066	OPIN1067	OPIN1068	OPIN1069	OPIN1070	OPIN1071	OPIN1072	OPIN1073	OPIN1074	OPIN1075	OPIN1076	OPIN1077	OPIN1078	OPIN1079	OPIN1080	OPIN1081	OPIN1082	OPIN1083	OPIN1084	OPIN1085	OPIN1086	OPIN1087	OPIN1088	OPIN1089	OPIN1090	OPIN1091	OPIN1092	OPIN1093	OPIN1094	OPIN1095	OPIN1096	OPIN1097	OPIN1098	OPIN1099	OPIN1100	OPIN1101	OPIN1102	OPIN1103	OPIN1104	OPIN1105	OPIN1106	OPIN1107	OPIN1108	OPIN1109	OPIN1110	OPIN1111	OPIN1112	OPIN1113	OPIN1114	OPIN1115	OPIN1116	OPIN1117	OPIN1118	OPIN1119	OPIN1120	OPIN1121	OPIN1122	OPIN1123	OPIN1124	OPIN1125	OPIN1126	OPIN1127	OPIN1128	OPIN1129	OPIN1130	OPIN1131	OPIN1132	OPIN1133	OPIN1134	OPIN1135	OPIN1136	OPIN1137	OPIN1138	OPIN1139	OPIN1140	OPIN1141	OPIN1142	OPIN1143	OPIN1144	OPIN1145	OPIN1146	OPIN1147	OPIN1148	OPIN1149	OPIN1150	OPIN1151	OPIN1152	OPIN1153	OPIN1154	OPIN1155	OPIN1156	OPIN1157	OPIN1158	OPIN1159	OPIN1160	OPIN1161	OPIN1162	OPIN1163	OPIN1164	OPIN1165	OPIN1166	OPIN1167	OPIN1168	OPIN1169	OPIN1170	OPIN1171	OPIN1172	OPIN1173	OPIN1174	OPIN1175	OPIN1176	OPIN1177	OPIN1178	OPIN1179	OPIN1180	OPIN1181	OPIN1182	OPIN1183	OPIN1184	OPIN1185	OPIN1186	OPIN1187	OPIN1188	OPIN1189	OPIN1190	OPIN1191	OPIN1192	OPIN1193	OPIN1194	OPIN1195	OPIN1196	OPIN1197	OPIN1198	OPIN1199	OPIN1200	OPIN1201	OPIN1202	OPIN1203	OPIN1204	OPIN1205	OPIN1206	OPIN1207	OPIN1208	

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates AAM result (same as BIT instruction).

X Index X

Y Index Y

A Accumulator

M Memory per effective address

MS Memory per stack pointer

+ Add

- Subtract

A And

V Or

X Exclusive Or

n No. Cycles

No. Bytes

Ms Memory Bit #6

Ms Memory Bit #7

* Denotes inverted signal.

**Enhanced Operational Characteristics**

The CMD G65SC02-A microprocessor is designed for building state-of-the-art microcomputer systems. The device utilizes the same basic software instruction set, and to be bus compatible with the MC6800 product line. Accordingly, the G65SC02-A series is pin compatible with existing NMOS 6500 type microprocessors.

However, as stated previously, the CMOS design allows several operational enhancements to be incorporated in the current product. These operational enhancements are explained in Table V.

Table V. Microprocessor Operational Enhancements

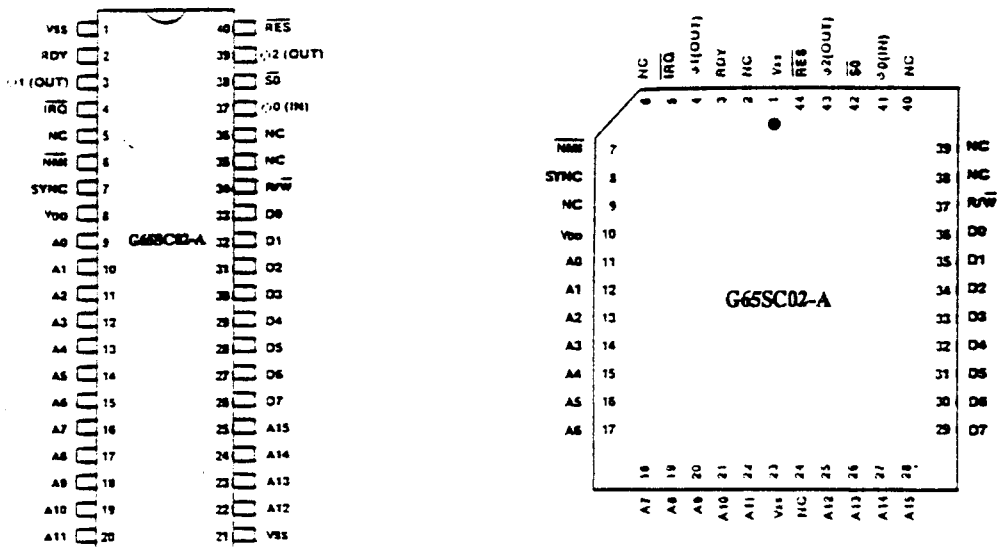
Function	NMOS 6500 Microprocessor	G65SC02-A Microprocessor																					
Indexed addressing across the page boundary.	Extra read of invalid address.	Extra read of last instruction byte.																					
Execution of invalid op codes.	Some terminate only by reset. Results are undefined.	All are NOPs (reserved for future use). <table> <tr> <td>Op Code</td><td>Bytes</td><td>Cycles</td></tr> <tr> <td>X2</td><td>2</td><td>2</td></tr> <tr> <td>X3, X7, XB, XF</td><td>1</td><td>1</td></tr> <tr> <td>44</td><td>2</td><td>3</td></tr> <tr> <td>54, D4, F4</td><td>2</td><td>4</td></tr> <tr> <td>5C</td><td>3</td><td>8</td></tr> <tr> <td>DC, FC</td><td>3</td><td>4</td></tr> </table>	Op Code	Bytes	Cycles	X2	2	2	X3, X7, XB, XF	1	1	44	2	3	54, D4, F4	2	4	5C	3	8	DC, FC	3	4
Op Code	Bytes	Cycles																					
X2	2	2																					
X3, X7, XB, XF	1	1																					
44	2	3																					
54, D4, F4	2	4																					
5C	3	8																					
DC, FC	3	4																					
Jump indirect, operand = XXFF.	Page address does not increment.	Page address increments, one additional cycle.																					
Read/modify/write instructions at effective address.	One read and two write cycles.	Two read and one write cycle.																					
Decimal flag.	Indeterminate after reset.	Initialized to binary mode (D=0) after reset and interrupts.																					
Flags after decimal operation.	Invalid N, V and Z flags.	Valid flags. One additional cycle.																					
Interrupt after fetch of BRK instruction.	Interrupt vector is loaded; BRK vector is ignored.	BRK is executed, then interrupt is executed.																					
Reset.	Reads three stack locations.	Writes program counter and status register to stack.																					
Read/Modify/Write instructions absolute indexed in same page.	Seven cycles.	Six cycles																					

Pin Function

Pin	Description
A0-Axx	Address Bus
$\phi 0$ (IN)	Phase 0 In
D0-D7	Data Bus
IRQ*	Interrupt Request
NC	No Connection
NMI*	Non-Maskable Interrupt

Pin	Description
$\phi 1$ (OUT)	Phase 1 Out
$\phi 2$ (OUT)	Phase 2 Out
RDY	Ready
RES*	Reset
R/W*	Read/Write
SO*	Set Overflow
SYNC	Synchronize
V _{DD}	Positive Power Supply (+5.0 Volts)
V _{SS}	Internal Logic Ground

* Denotes inverted signal.

**Pin Configuration****Ordering Information**

	G	65SCXXX	A	P	I	-2
Description						
C—Special G—Standard						
Product Identification Number						
Version						
Package						
P—Plastic E—Leaded Chip Carrier						
C—Ceramic L—Leadless Chip Carrier						
D—Cerdip X—Dice						
Temperature/Processing						
None— 0° C to +70° C. = 5% P.S. Tol.	S— 0° C to +70° C. = 10% P.S. Tol.					
I— -40° C to +85° C. = 5% P.S. Tol.	W— -40° C to +85° C. = 10% P.S. Tol.					
Performance Designator						
Designators selected for speed and power specifications						
-1 1MHz -3 3MHz -5 5MHz						
-2 2MHz -4 4MHz -6 6MHz						

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.