Andrew Yan

353 Brunswick Blvd.
Pointe-Claire, QC, Canada
(778) 996-4600
andrew.yan@alumni.ubc.ca

Skills

HDL Languages (VHDL, Verilog, SystemVerilog), Python, Shell Scripting, C, Microsoft Office Suite

Experience

NOVEMBER 2021 - PRESENT

MDA, Montreal, QC, Canada - *Junior VHDL Designer*

- Project 1
    - Designed 6 modules in VHDL that successfully passed verification checks and lab testing
    - Added radiation protection to 6 modules such that the effect of single-event upsets is minimized
    - Wrote a shell script that successfully combined the coverage reports of all modules in the project
    - Taught two colleagues how to use a code review tool (crucible) such that they were able to use it immediately afterwards
    - Documented module designs such that were easily understood by the customer
- Project 2
    - Designed a module in VHDL from requirements that chooses data from 4 streams based on a priority system and a round robin secondary system
    - Set up a Versal FPGA in the lab to test RTL
- Project 3
    - Wrote a python script that mimicked design logic that was used to check outputs of the device in the lab
    - Adapted a python script to write to various registers and test the device response in the lab

JANUARY 2019 - AUGUST 2019

Kardium Inc., Vancouver, BC, Canada - *Electrical Engineer Co-op*

- Created testbenches in VHDL to test the digital logic of various features of a product, resulting in the successful identification of bugs
- Developed solutions in VHDL to successfully correct bugs found through testbenches
- Performed testing on a specific feature of a product, which was used with other data to verify the design
- Designed a script in Python to perform an analysis of the errors and warnings from a VHDL build, allowing for the ability to ensure that the design met specifications.

- Built and tested multiple cables according to specifications for an upcoming feature which were successfully used in multiple animal trials

MAY 2018 - DECEMBER 2018

Intel Corporation, Vancouver, BC, Canada - *ECC RTL, Software, FPGA Design (Co-op)*

- Designed error correction RTL in Verilog and SystemVerilog such that it correctly encoded and decoded to the specifications of a specific product
- Created software models in C which were eventually used in combination with SystemVerilog testbenches to assist in the debugging of the error correction RTL

Education

SEPTEMBER 2020 - AUGUST 2021

The University of British Columbia - *M.Eng, Biomedical Engineering*

Activities and Societies: Engineers in Scrubs

SEPTEMBER 2015 - MAY 2020

The University of British Columbia - *B.A.Sc, Electrical Engineering*

Activities and Societies: UBC Biomedical Engineering Student Team, IEEE EMBS Division

Awards

- 2nd Place - Capstone Competition
- 2017 Jim and Helen Hill Memorial Service Award in Electrical Engineering

Interests

Swimming, Hiking, Skiing, Badminton, PC Building