





## Move example and add a few comments

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🔑 master (#1) 🔍 v1.3.1 ... continuous

 TheThirdOne committed on 30 May1 parent [c1ca9ee](#) commit [598d3d901dee0eed2dd84076533939742c8aaaba](#) Showing 1 **changed file** with 10 additions and 2 deletions.[Unified](#) [Split](#)▼ 12  timerTest.s → examples/timertool.s 

```
...      ...      @@ -1,22 +1,25 @@
1      -      .data
2      -      loopStr:      .asciz "Loop\n"
      1      +      .data
      2      +      loopStr:      .asciz "Loop\n"
3      3      hello:      .asciz "Hello\n"
4      4      newline:      .asciz "\n"
5      5      time:      .word 0xFFFF0018
6      6      cmp:      .word 0xFFFF0020
7      7      .text
8      8      main:
      9      +      # Set time to trigger interrupt to be 5 seconds
9      10      lw a0, cmp
10     11      li a1, 5000
11     12      sw a1, 0(a0)
12     13
      14      +      # Set the handler address and enable interrupts
```

```

13      15      la      t0, handle
14      16      csrrs   zero, 5, t0
15      17      csrrsi  zero, 4, 0x10
16      18      csrrsi  zero, 0, 0x1
17      19
18      20
19      21      loop:
20      22      +      # Output current time in loop
21      23      li      a7, 1
22      24      lw      a0, time
23      25      lw      a0, 0(a0)
24      26
25      27
26      28
27      29
28      30      handle:
29      31
30      32      +      # Save some space for temporaries
31      33      addi    sp, sp, -20
32      34      sw      t0, 16(sp)
33      35      sw      t1, 12(sp)
34      36      sw      t2, 8(sp)
35      37      sw      a0, 4(sp)
36      38      sw      a7, 0(sp)
37      39
38      40
39      41
40      42      +      # Print out hello
41      43      li      a7, 4
42      44      la      a0, hello
43      45      ecall
44      46      +
45      47      +      # Set cmp to time + 5000
46      48      lw      a0 time
47      49      lw      t2 0(a0)
48      50      li      t1 5000
49      51      add     t1 t2 t1
50      52      lw      t0 cmp

```

46	53		sw t1 0(t0)
47	54		
	55	+	# Reload the saved registers and return
48	56		lw t0, 16(sp)
49	57		lw t1, 12(sp)
50	58		lw t2, 8(sp)

0 comments on commit 598d3d9

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