Project 1: part 2

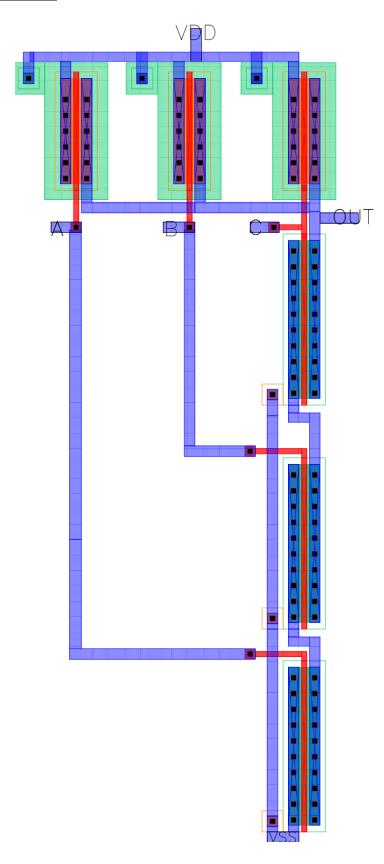
CPE 151: CMOS & amp; VLSI

Section 1

Dr. Praveen Meduri

Andrew Stich 3-20-18

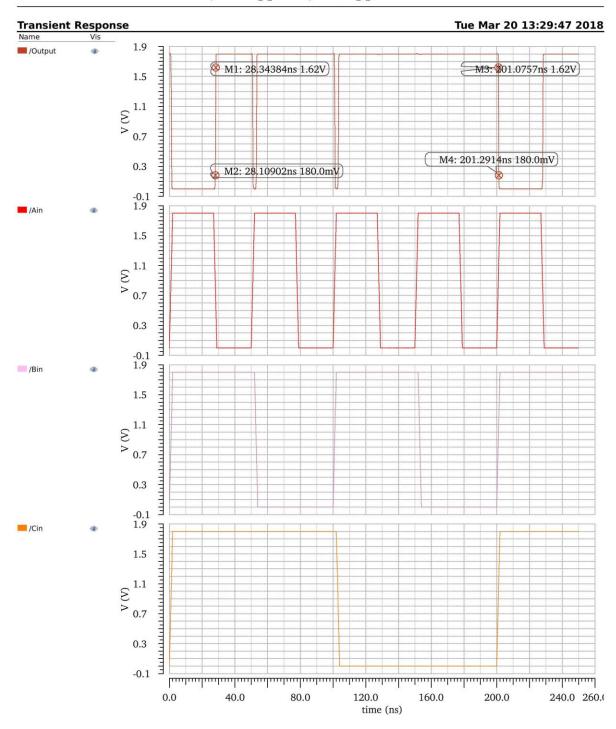
3 Input NAND: Layout



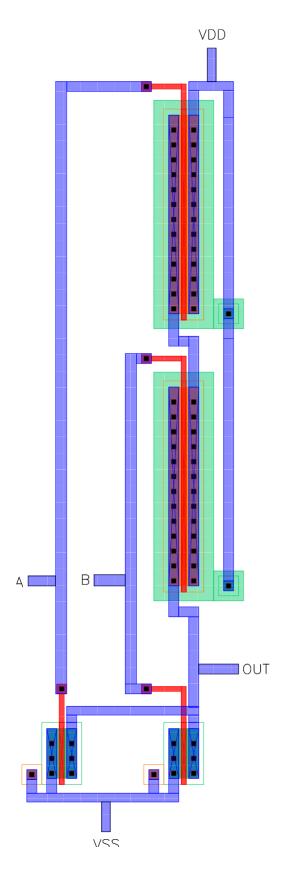
DRC Check:

```
Validating hierarchy instantiation for:
library: Project1
cell:
        NAND_3
view:
        layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Tue Mar 20 12:37:49 2018
   completed .... Tue Mar 20 12:37:49 2018
   CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
******* Summary of rule violations for cell "NAND_3 layout" *******
   Total errors found: 0
```

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$	active 6 6	
	total 6 6	
Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/sticha/CPE_151/LVS -I -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic	nets un-matched 0 0	
Like matching is enabled.	merged 0 0	
Net swapping is enabled.	pruned 0 0	
Using terminal names as correspondence points.	active 8 8	
Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist	total 8 8 terminals	
count	un-matched 0 0	
8 nets	matched but	
6 terminals	different type 0 0	
3 pmos	total 6 6	
3 nmos	Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic	
Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist	devbad.out:	
count	netbad.out:	
8 nets	mergenet.out:	
6 terminals	termbad.out:	
3 pmos	prunenet.out:	
3 nmos	prunedev.out:	
Terminal correspondence points	audit.out:	
N6 N1 A		
N5 N2 B	Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout	
N4 N6 C	devbad.out:	
N3 N7 Out	netbad.out:	
N7 N5 VDD	mergenet.out:	
N2 N4 VSS	termbad.out:	
Devices in the netlist but not in the rules: prunenet.out:		
pmos nmos		
	prunedev.out:	
The net-lists match.		
	audit.out:	
layout schematic		
instances		
un-matched 0 0		
rewired 0 0		
size errors 0 0		
pruned 0 0		



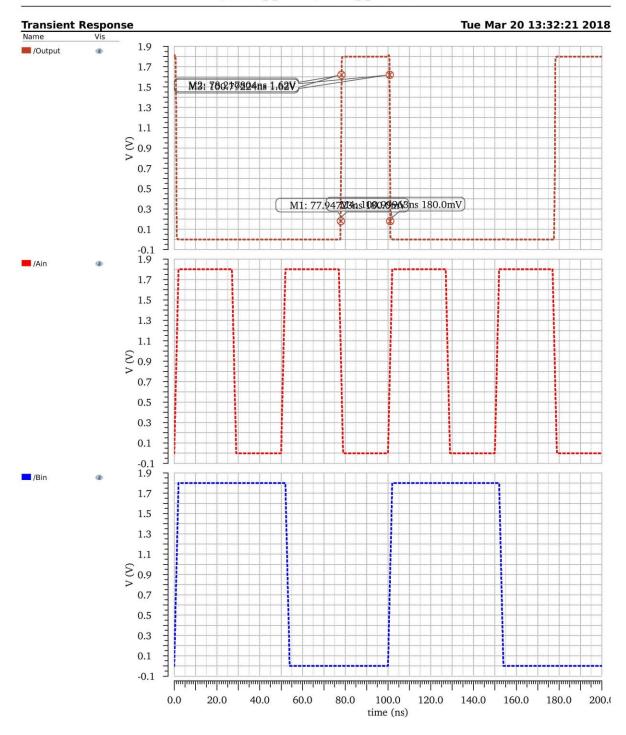
2 Input NOR: Layout



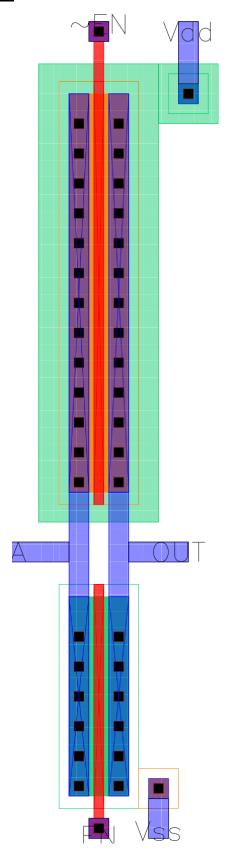
DRC Check

```
Validating hierarchy instantiation for:
library: Project1
        NOR_2
cell:
view:
         layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Tue Mar 20 12:38:55 2018
    completed .... Tue Mar 20 12:38:55 2018
    CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
******* Summary of rule violations for cell "NOR_2 layout"
                                                              ******
   Total errors found: 0
```

@(#)\$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$	size errors 0 0
	pruned 0 0
Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -	active 4 4
dir /gaia/class/student/sticha/CPE_151/LVS -l -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic	total 4 4
Like matching is enabled.	nets
Net swapping is enabled.	un-matched 0 0
Using terminal names as correspondence points.	merged 0 0
	pruned 0 0
Net-list summary for	active 6 6
/gaia/class/student/sticha/CPE_151/LVS/layout/netlist	total 6 6
count	
6 nets	terminals
5 terminals	un-matched 0 0
2 pmos	matched but
2 nmos	different type 0 0
Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist	total 5 5
count	
6 nets	
5 terminals	Probe files from
2 pmos	/gaia/class/student/sticha/CPE_151/LVS/schematic
2 nmos	devbad.out:
Terminal correspondence points	netbad.out:
N4 NO A	mergenet.out:
N3 N1 B	termbad.out:
N2 N5 OUT	prunenet.out:
N5 N2 VDD	prunedev.out:
N1 N3 VSS	audit.out:
Devices in the netlist but not in the rules:	
pmos nmos	Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout
The net-lists match.	devbad.out:
The fact lists flucture.	netbad.out:
layout schematic	mergenet.out:
	termbad.out:
instances	prunenet.out:
un-matched 0 0	prunedev.out:
rewired 0 0	audit.out:



Transmission Gate: Layout



DRC Check:

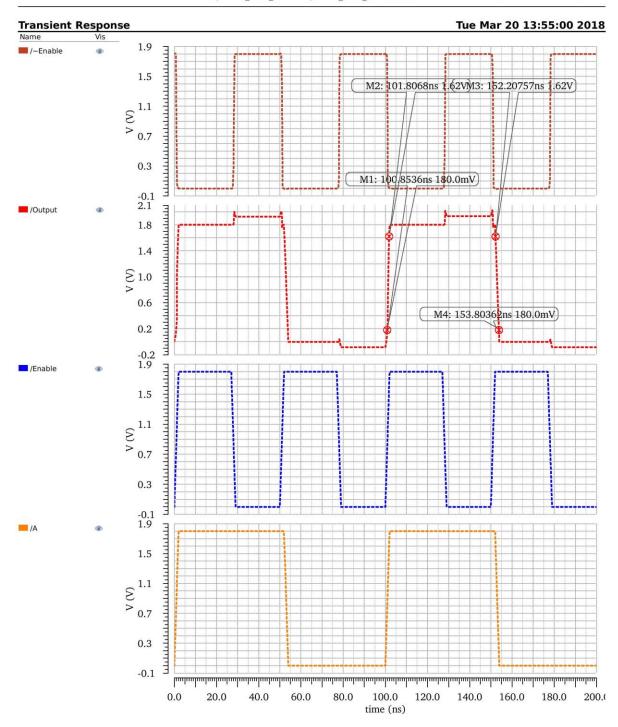
```
Validating hierarchy instantiation for:
library: Project1
        T_Gate
cell:
view:
        layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started......Tue Mar 20 12:39:31 2018
    completed .... Tue Mar 20 12:39:31 2018
    CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
          Summary of rule violations for cell "T_Gate layout" ********
*****
   Total errors found: 0
```

@(#)\$CDS: L	VS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$	pruned 0 0
		active 2 2
Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS - dir /gaia/class/student/sticha/CPE_151/LVS -I -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic		total 2 2
		un-matched 0 0
Like matchin	g is enabled.	merged 0 0
Net swappin	g is enabled.	pruned 0 0
Using termin	al names as correspondence points.	active 6 6
Net-list sur /gaia/class/s	mmary for tudent/sticha/CPE_151/LVS/layout/netlist	total 6 6 terminals
count		un-matched 0 0
6	nets	matched but
6	terminals	different type 0 0
1	pmos	total 6 6
1	nmos	
Net-list sur /gaia/class/s	mmary for tudent/sticha/CPE_151/LVS/schematic/netlist	Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic
count		devbad.out:
6	nets	netbad.out:
6	terminals	mergenet.out:
1	pmos	termbad.out:
1	nmos	prunenet.out:
Terminal c	orrespondence points	prunedev.out:
N3 N0	А	audit.out:
N2 N3	EN	
N1 N4	ОИТ	Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout
N5 N5	Vdd	devbad.out:
N0 N2	Vss	netbad.out:
N4 N1	~EN	mergenet.out:
Devices in th	e netlist but not in the rules:	termbad.out:
pmos nr		prunenet.out:
The net-lists		prunedev.out:
	layout schematic	audit.out:
	instances	
un-matched 0 0		
rewired	0 0	
size erro	ors 0 0	

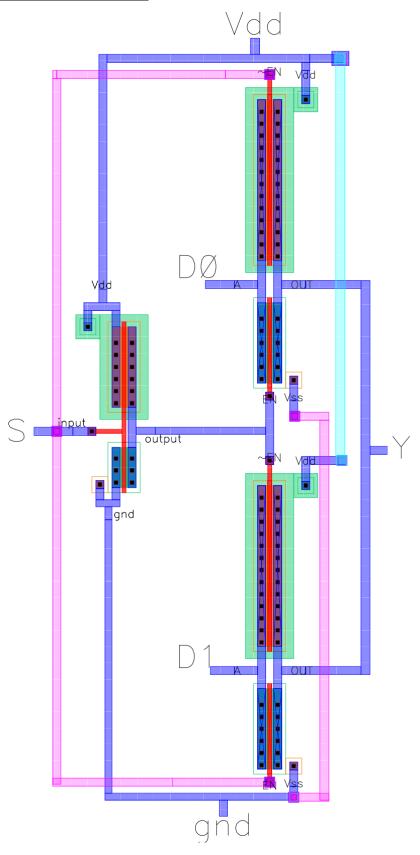
Post-Layout Simulation:



13:57:12 Tue Mar 20 2018



Two-to-one Multiplexer: Layout



DRC Check

```
Getting layout propert bagGetting layout propert bag
DRC started at Tue Mar 20 12:32:18 2018
Validating hierarchy instantiation for:
library: Project1
cell:
        MUX2_1
view:
        layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Tue Mar 20 12:32:18 2018
    completed .... Tue Mar 20 12:32:18 2018
    CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
****** Summary of rule violations for cell "MUX2_1 layout"
   Total errors found: 0
```

LV3 CII		
@(#)\$CDS: L	VS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$	size errors 0 0
		pruned 0 0
Command line:		active 6 6
	dence/installs/IC617/tools.lnx86/dfll/bin/64bit/LVS - ss/student/sticha/CPE_151/LVS -l -s -t	total 6 6
/gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic		nets
		un-matched 0 0
Like matchin		merged 0 0
Net swapping is enabled.		pruned 0 0
	al names as correspondence points.	active 7 7
Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist		total 7 7
count	, .	
7	nets	terminals
6	terminals	un-matched 0 0
		matched but
3	pmos	different type 0 0
3	nmos	total 6 6
	mmary for tudent/sticha/CPE_151/LVS/schematic/netlist	Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic
count		devbad.out:
7	nets	netbad.out:
6	terminals	mergenet.out:
3	pmos	termbad.out:
3	nmos	prunenet.out:
Terminal correspondence points		prunedev.out:
N5 N4	D0	audit.out:
N4 N0	D1	Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout
N3 N6	S	devbad.out:
N6 N3	Vdd	netbad.out:
N1 N2	Vss	mergenet.out:
N2 N1	Υ	termbad.out:
Devices in th	e netlist but not in the rules:	prunenet.out:
pmos nr	nos	prunedev.out:
The net-lists match.		audit.out:
layout schematic		
instances		
un-matched 0 0		
rewired 0 0		
rewired	U U	

13:39:27 Tue Mar 20 2018

