



CPE151

Digital IC Design

Project 2

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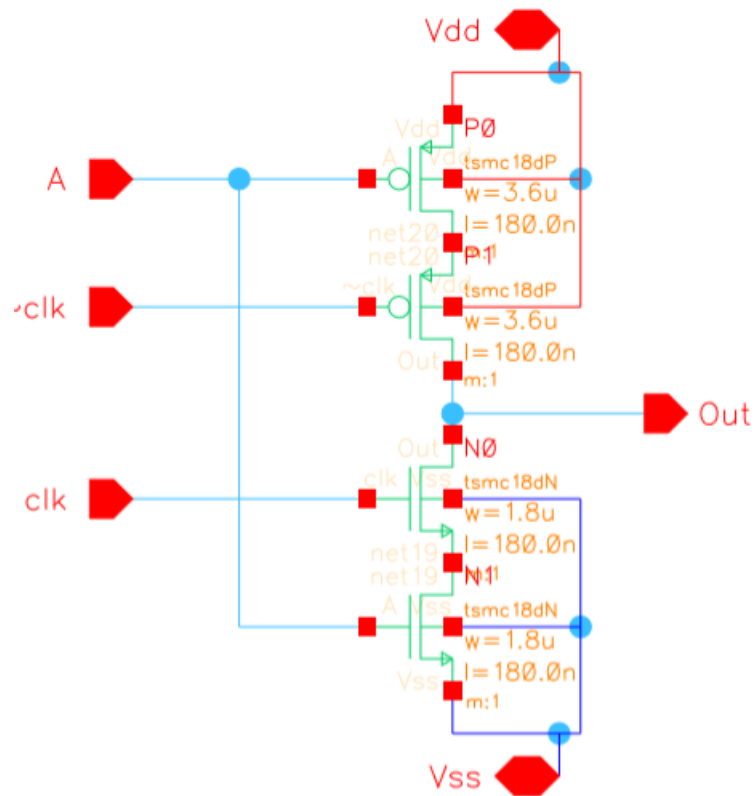
4/12/2018

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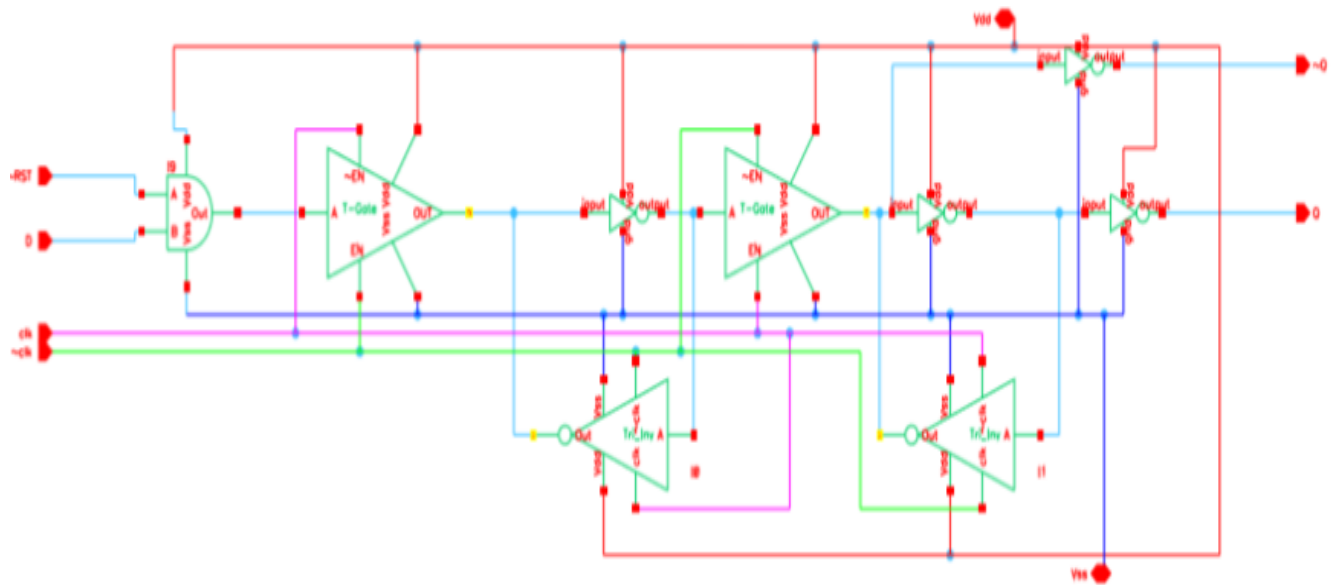
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D- Flip Flop

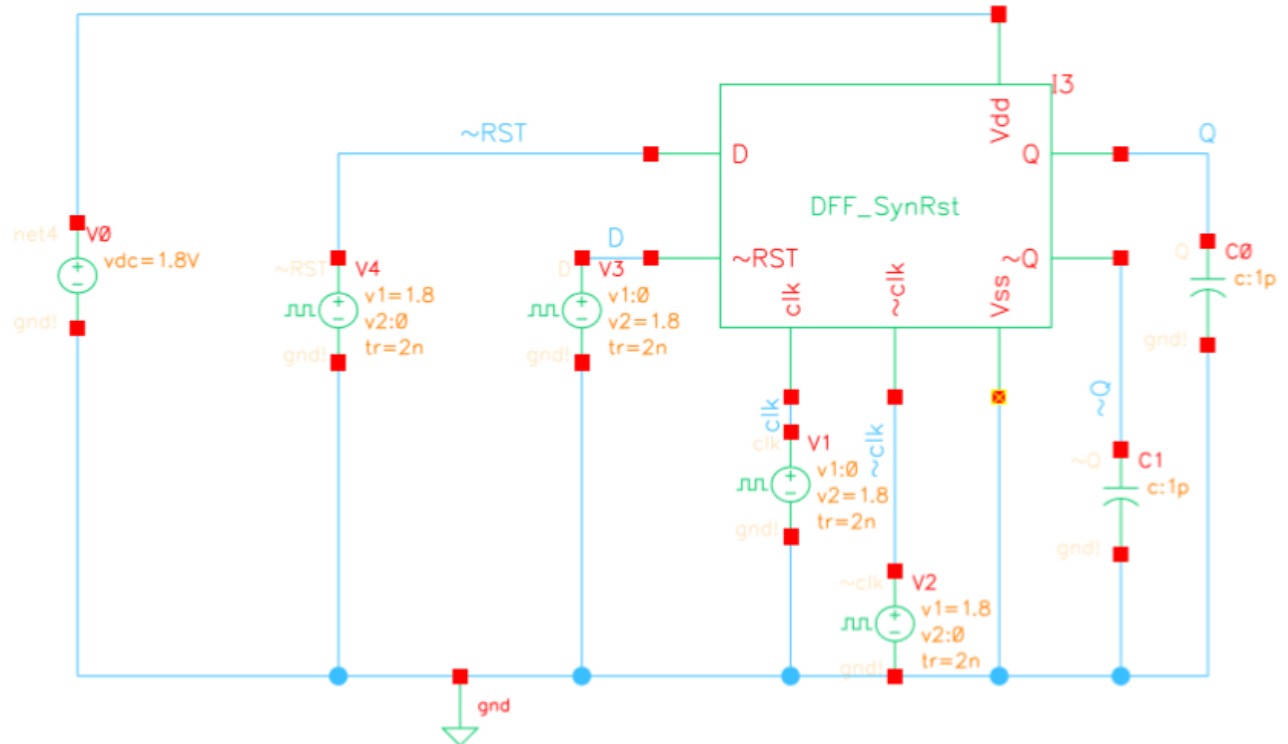
Tri-State Inverter:



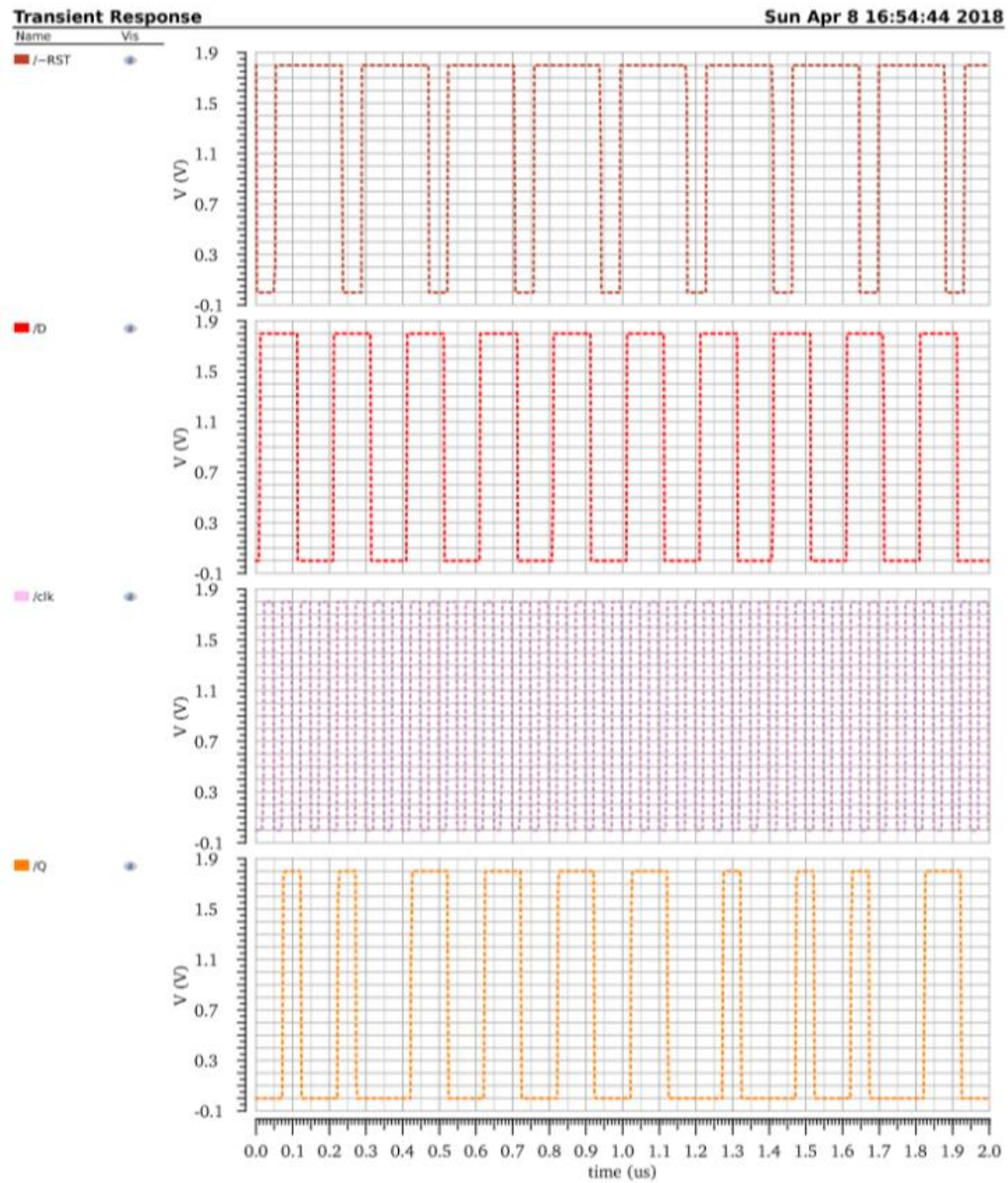
DFF Schematic:



DFF Test Bench:

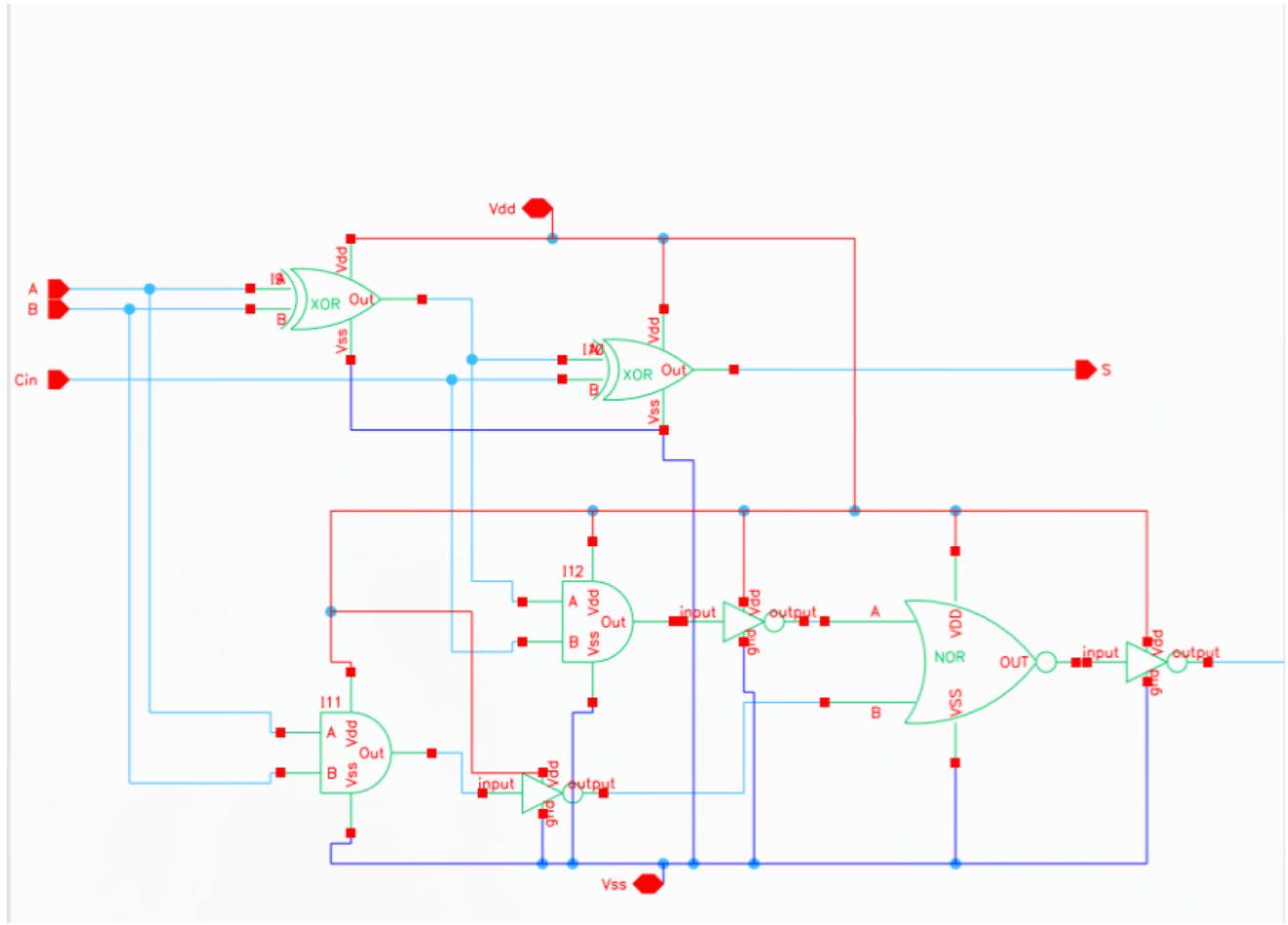


Waveform:

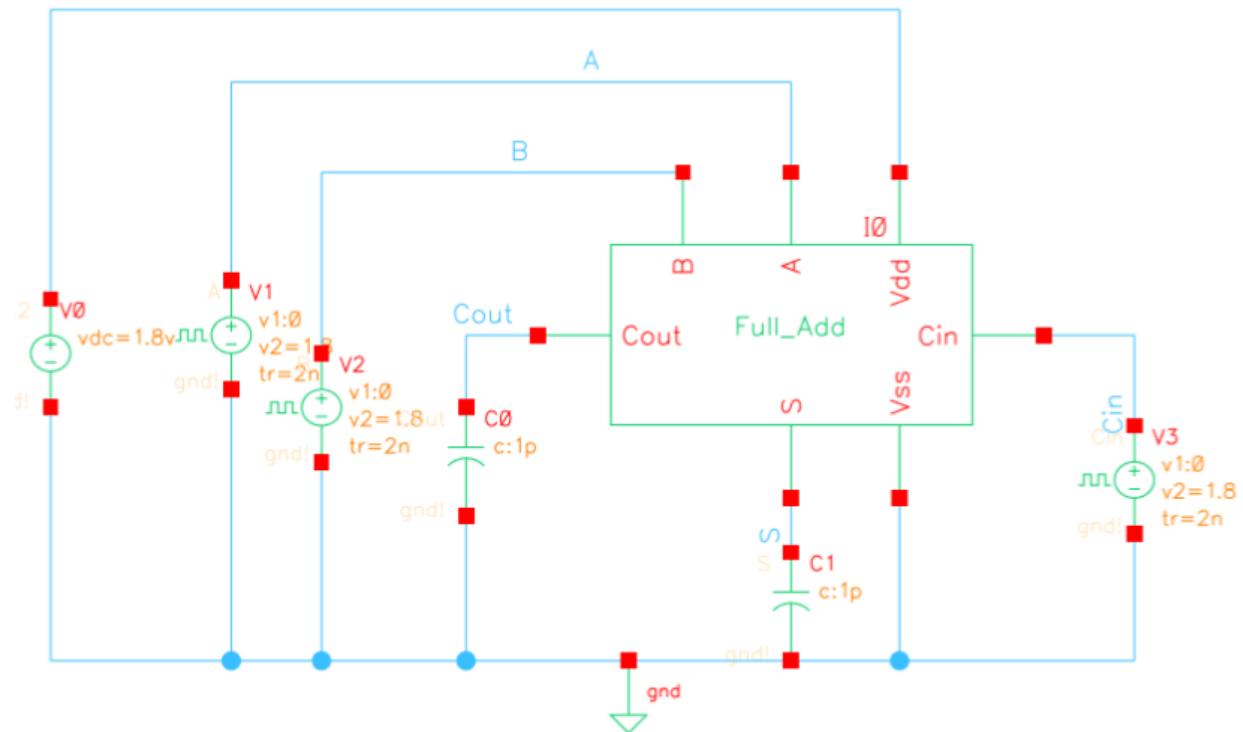


Arithmetic Logical Unit:

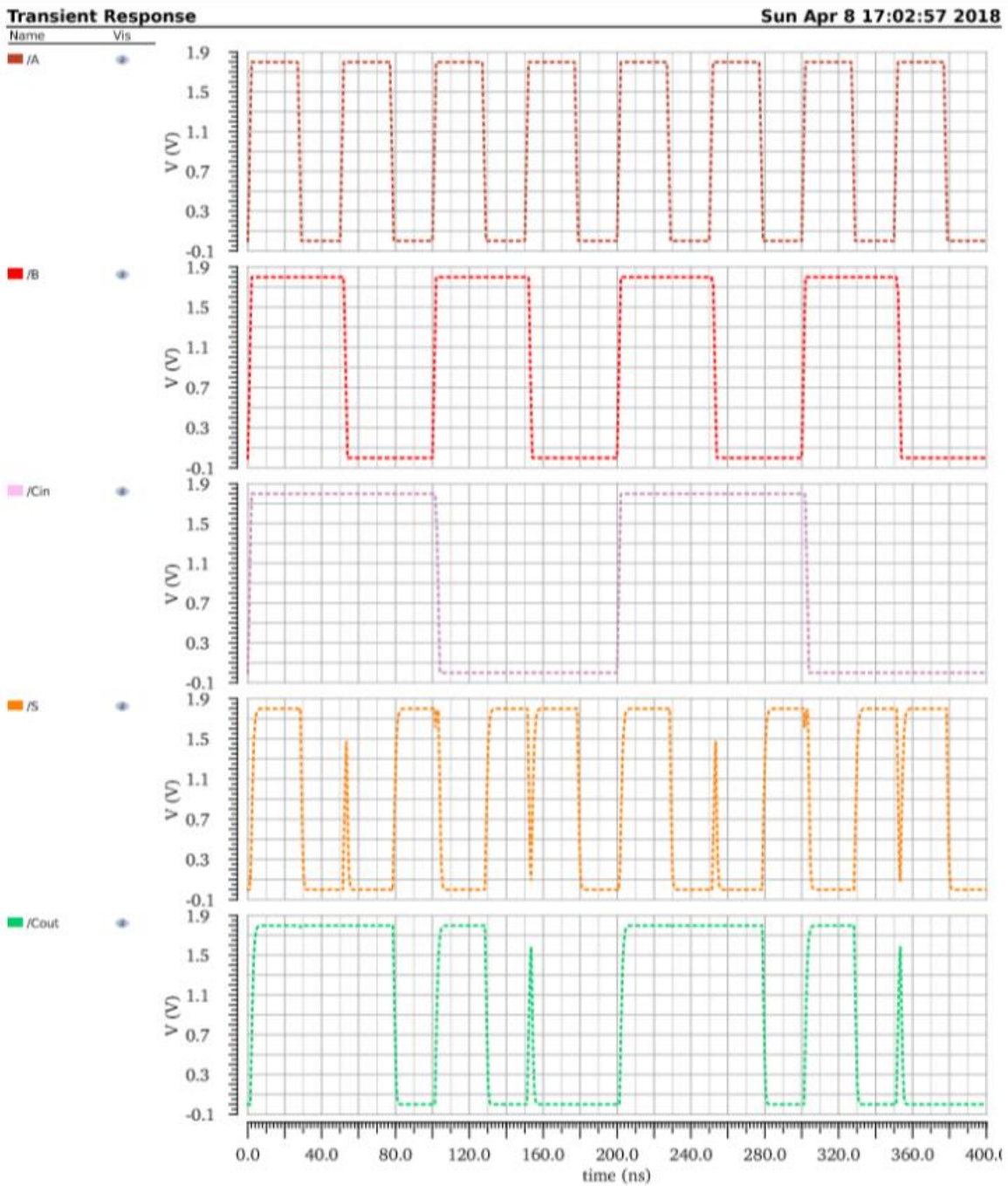
Full Adder:



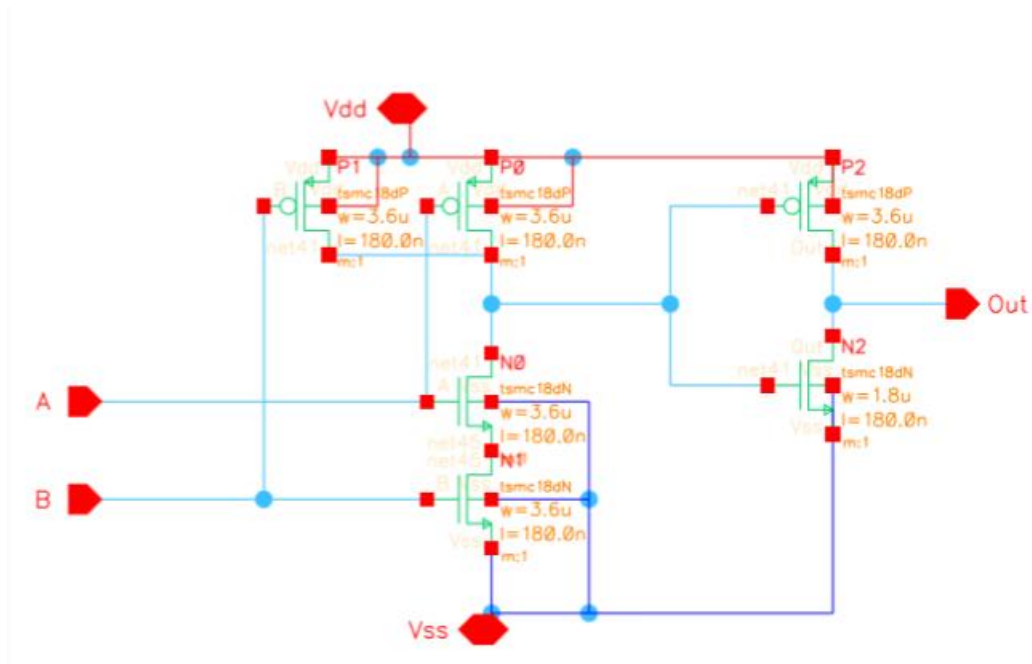
Test Bench:



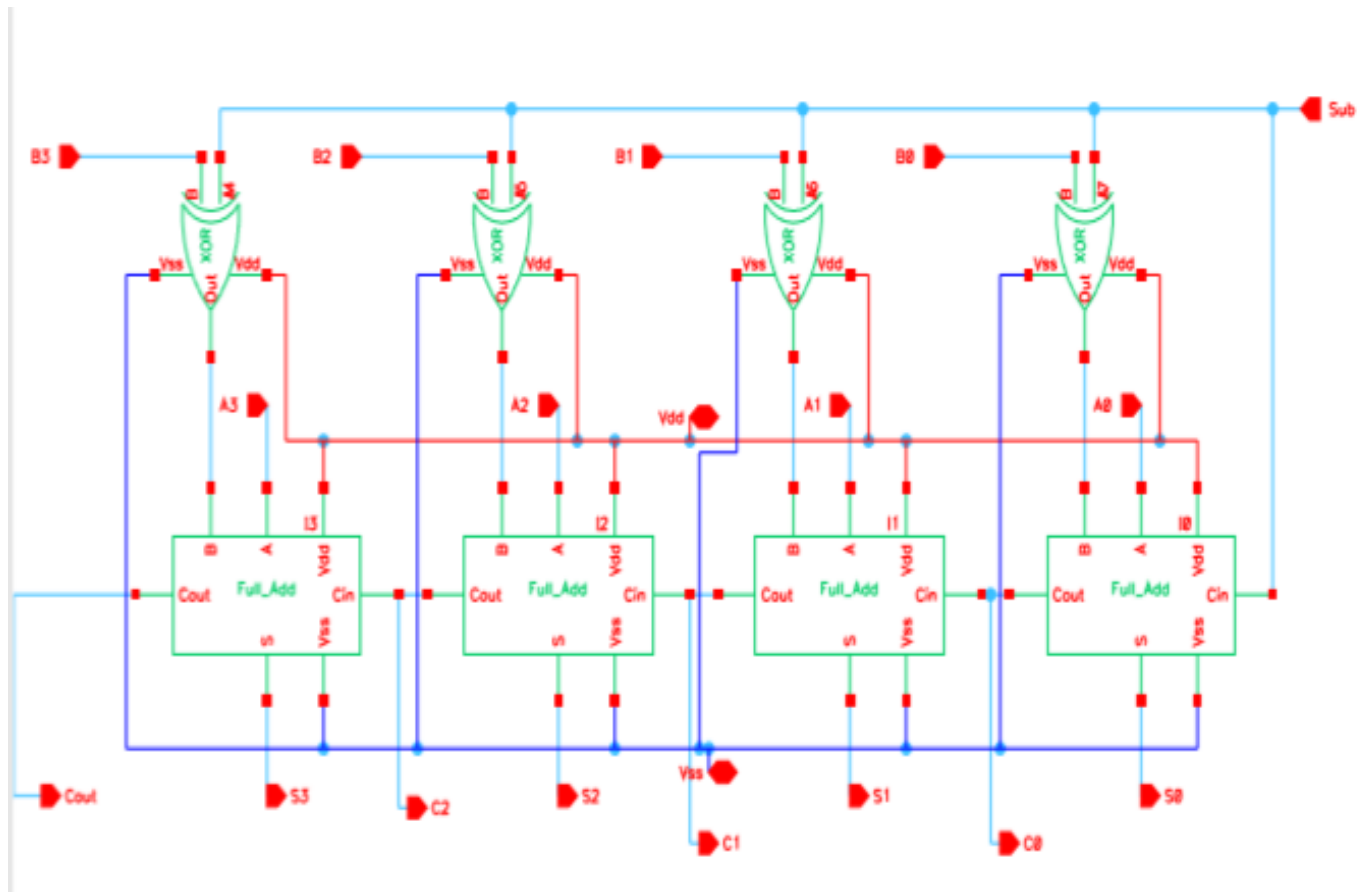
Waveform:



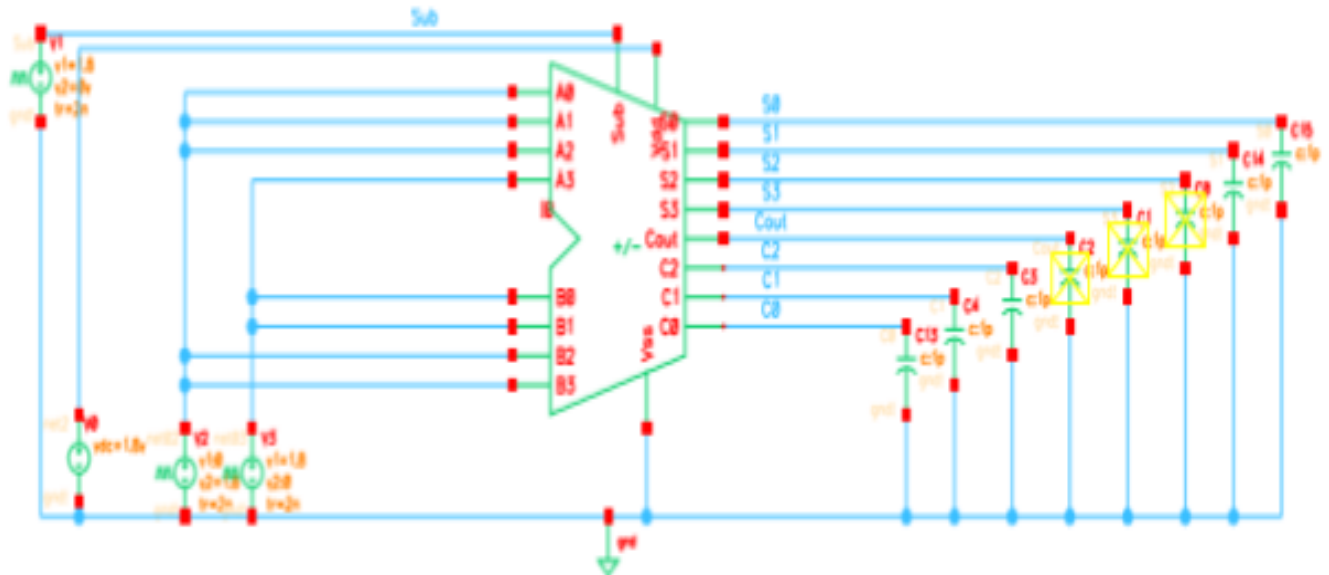
AND2_Schematic:



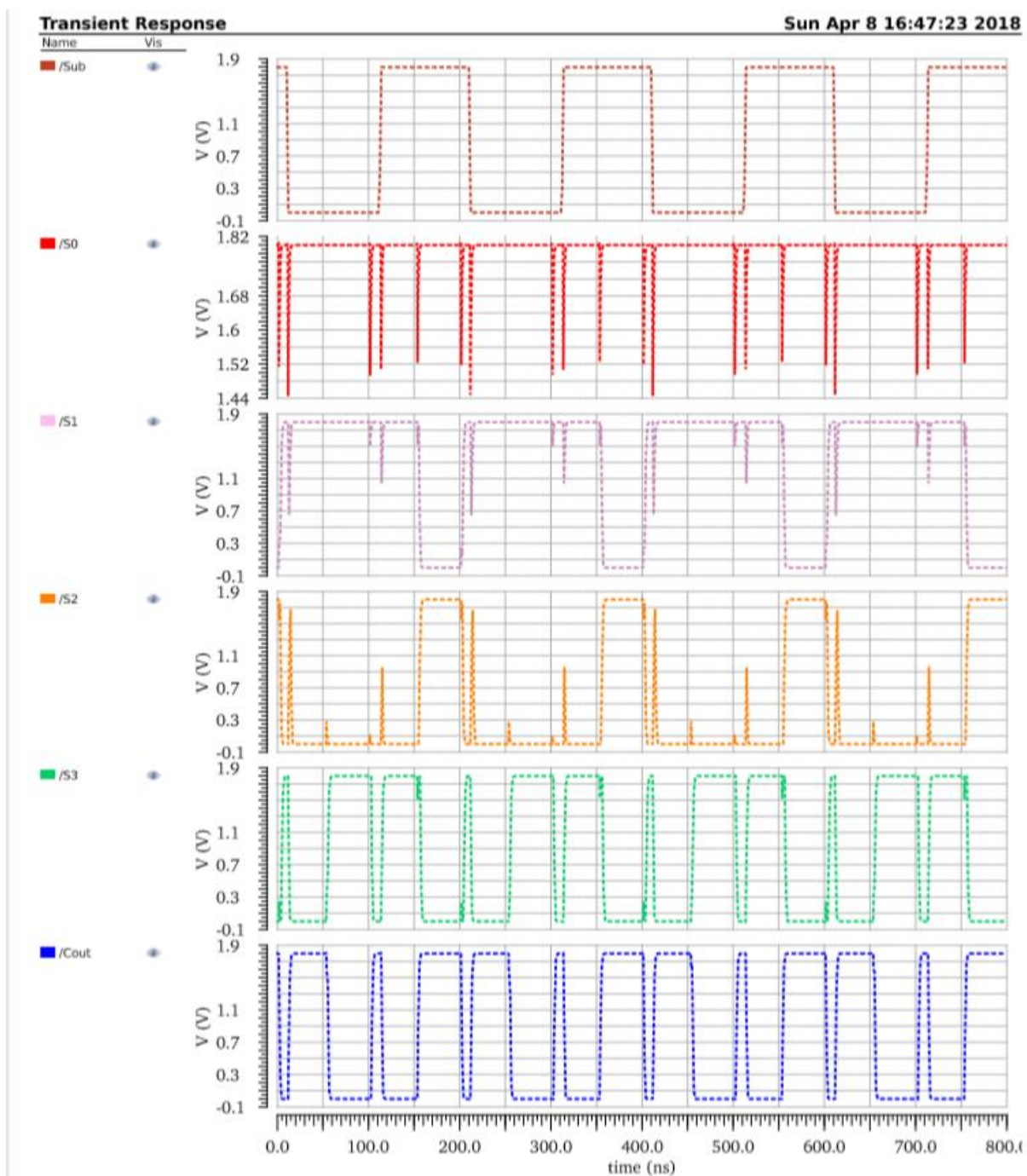
ADD/SUB Schematic:



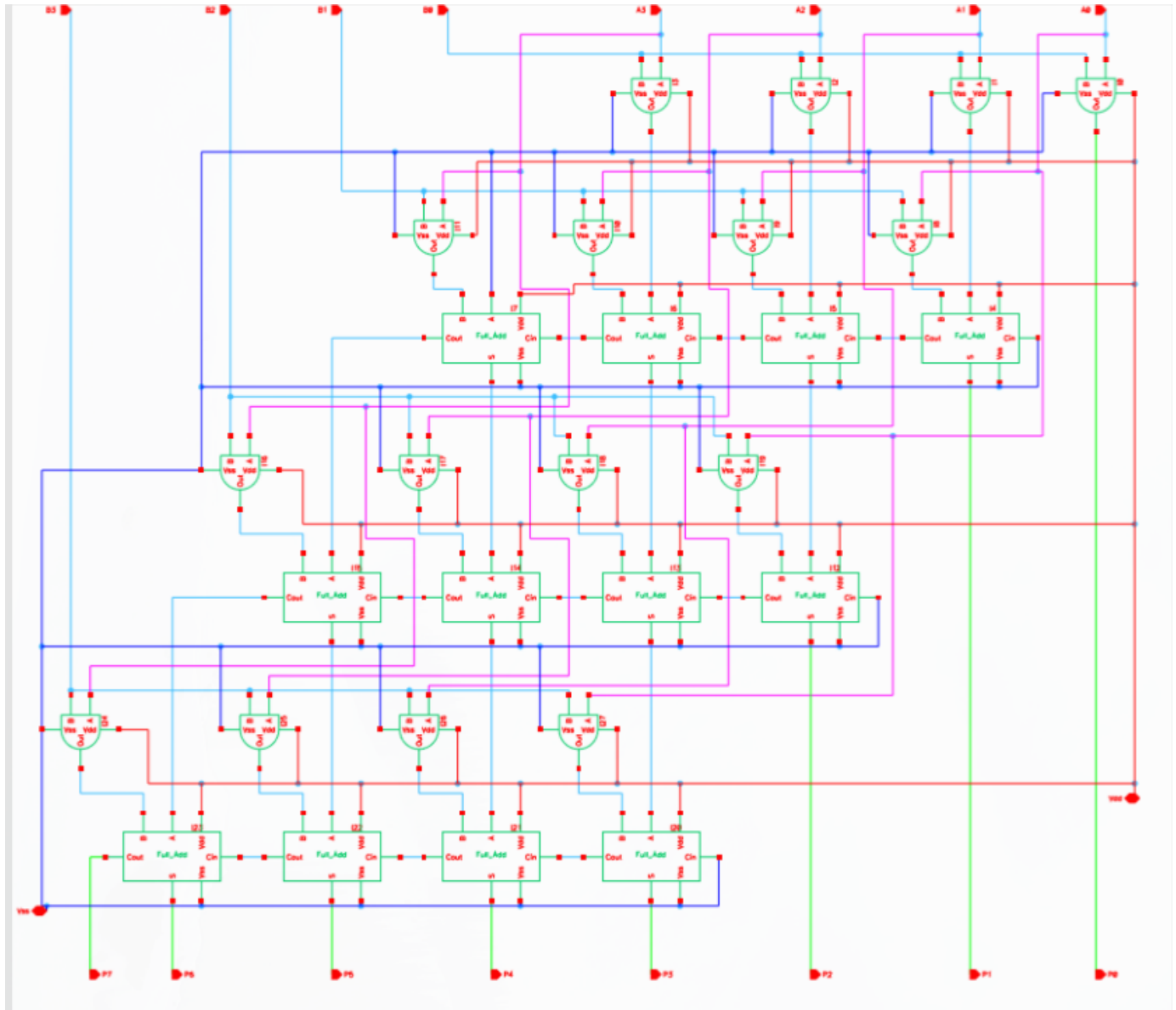
ADD/SUB test bench:



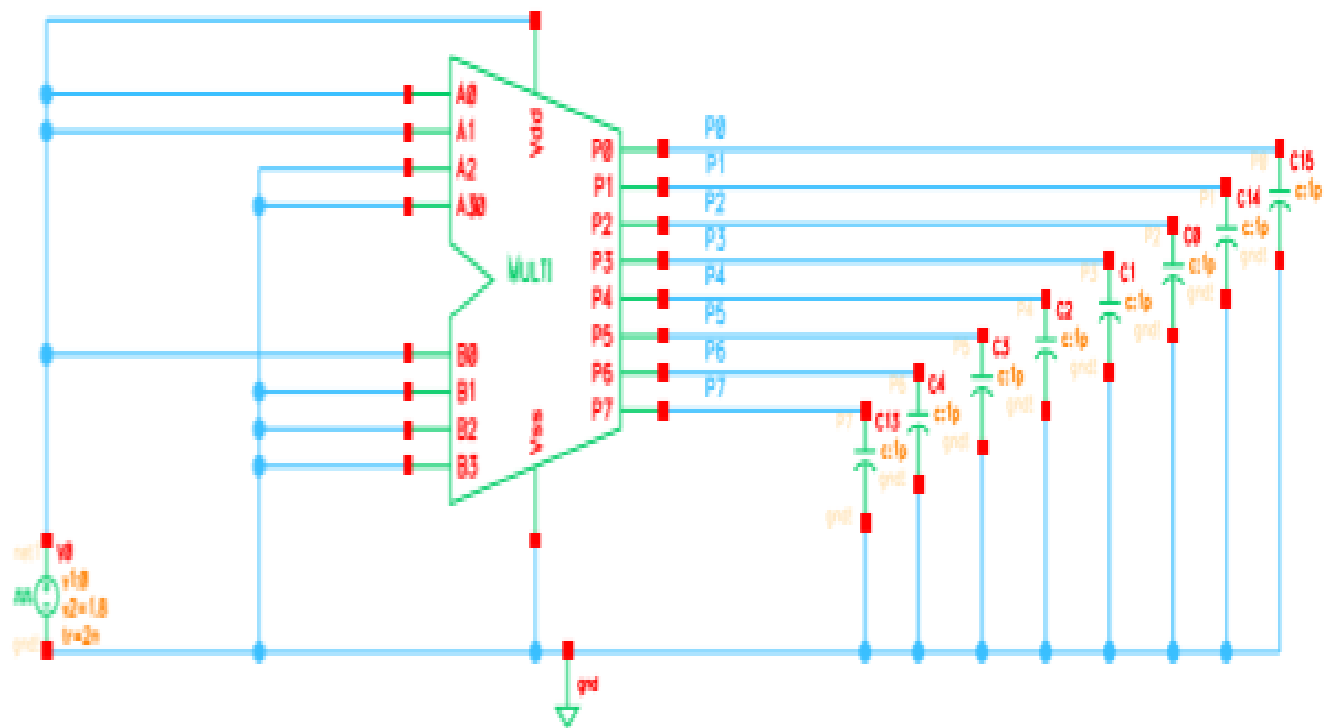
Waveform:



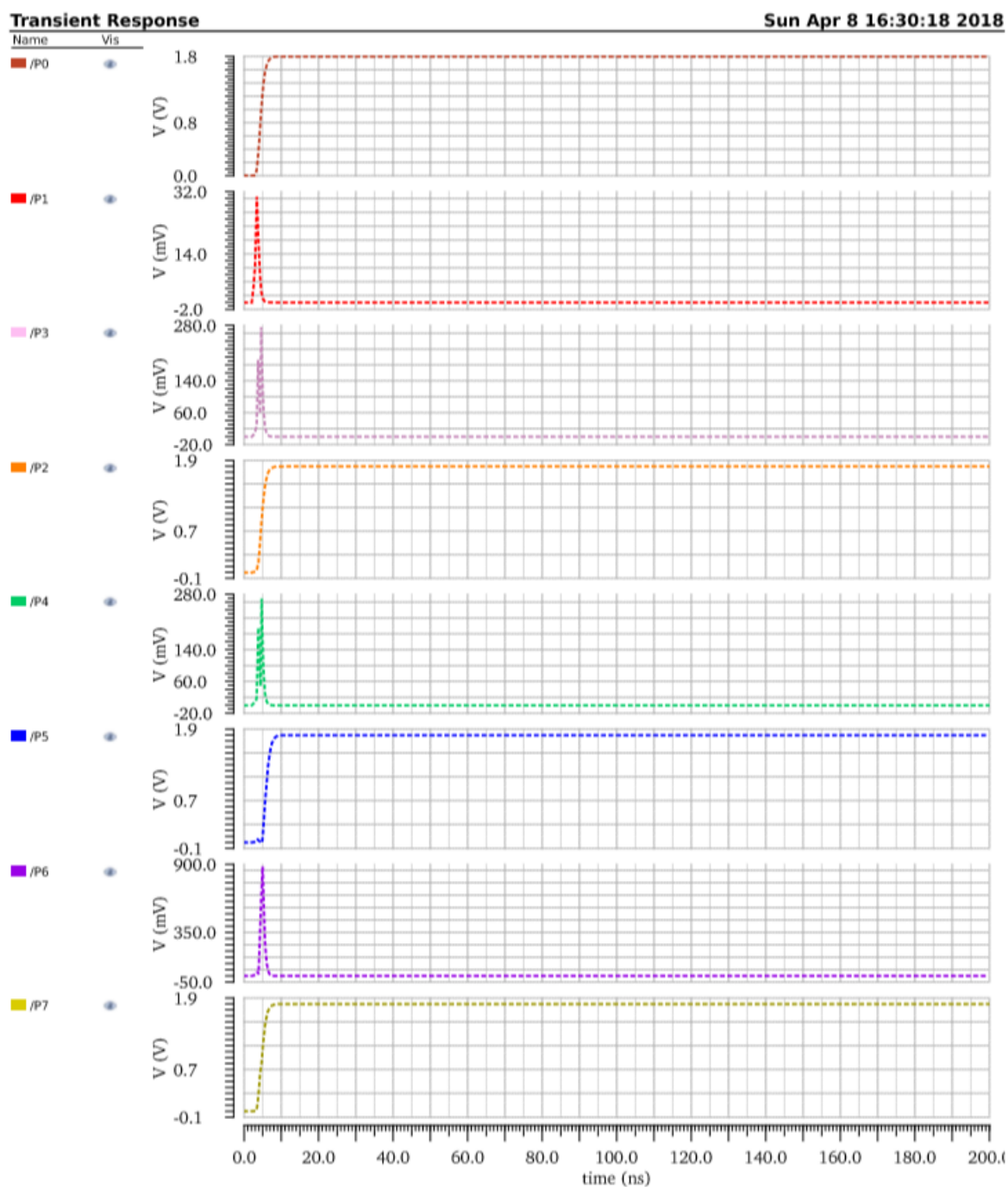
4 by 4 Multiplier Schematic:



4 by 4 Multiplier Test Bench:

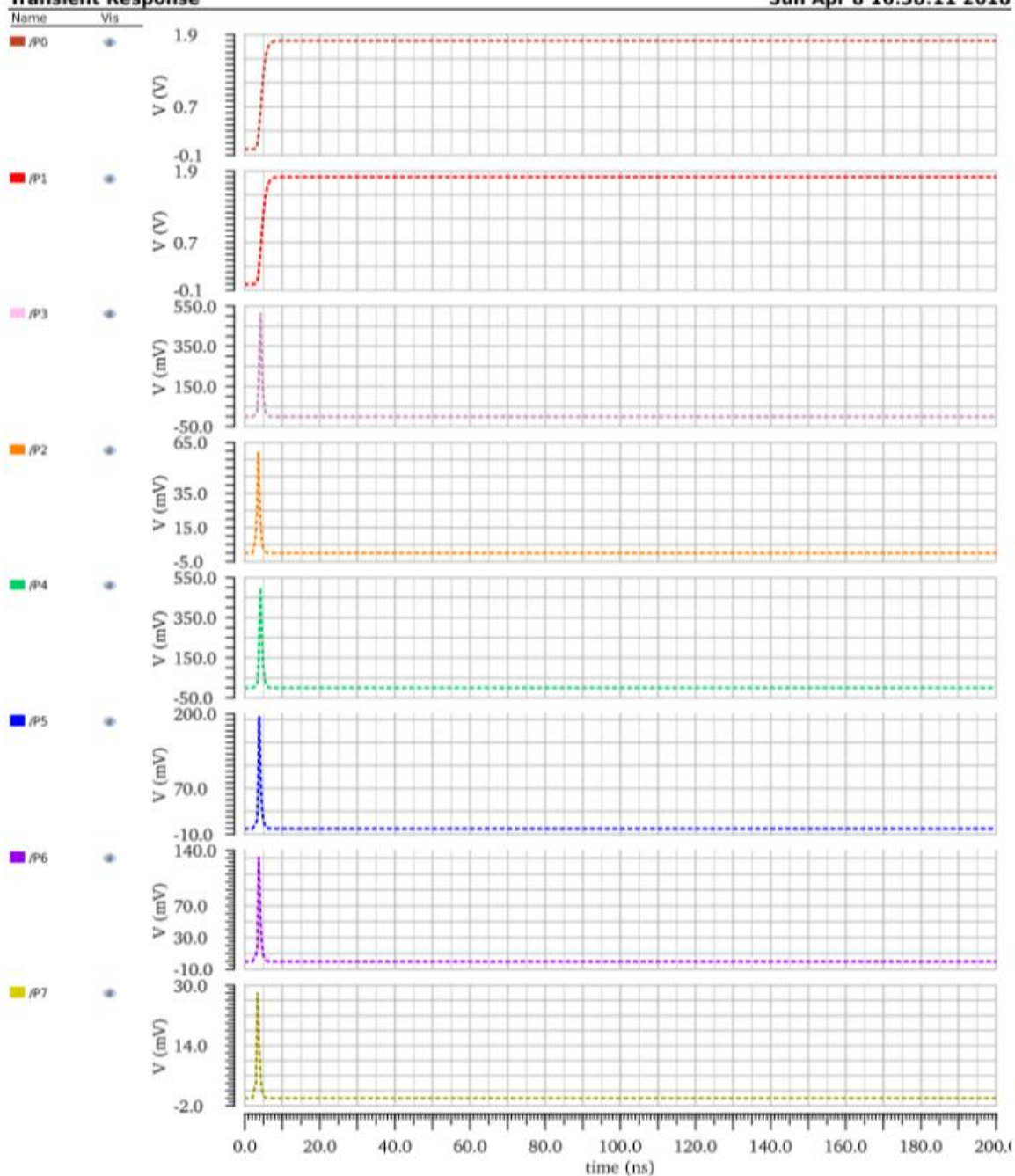


Waveform:

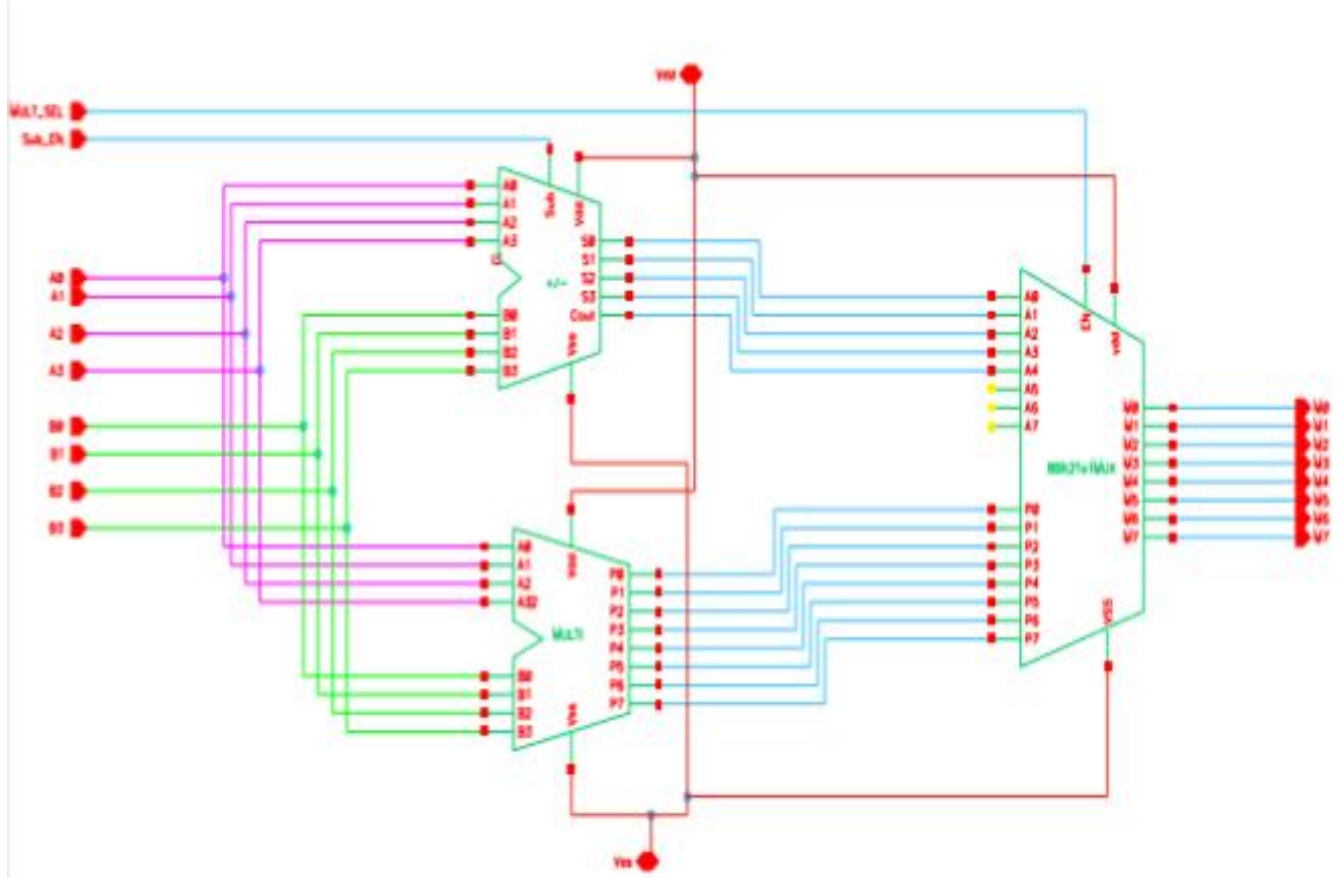


Transient Response

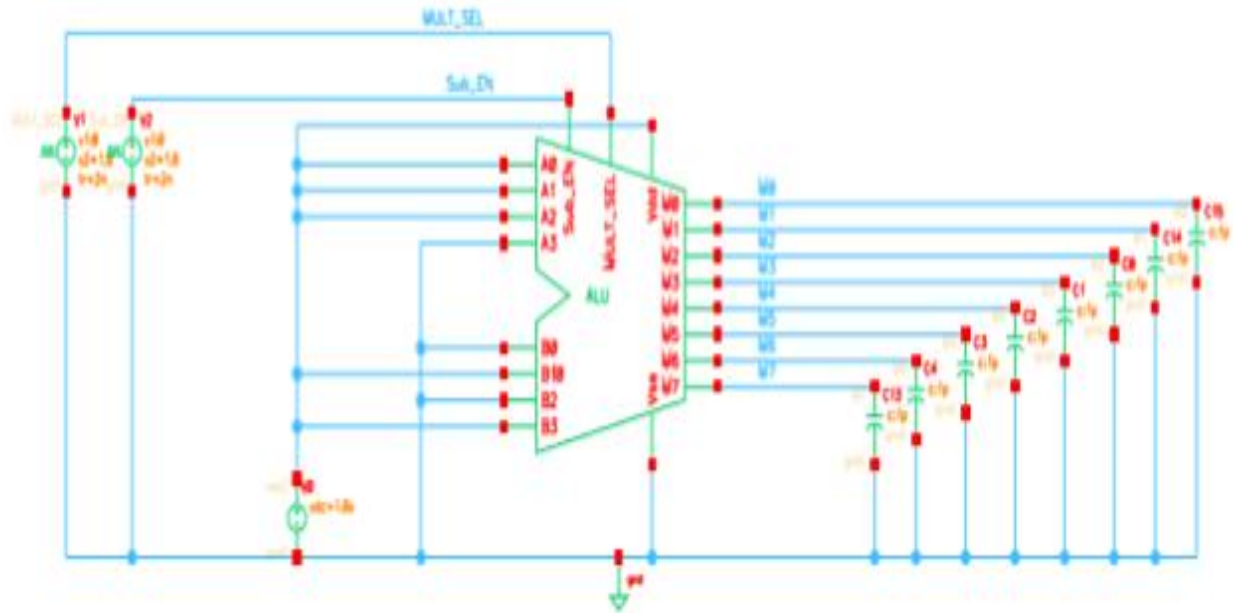
Sun Apr 8 16:38:11 2018



ALU Schematic:



ALU Test Bench:



Waveform:

