SACRAMENTO STATE

Cadence Project 2 Part 2

CPE 151: CMOS and VLSI Design

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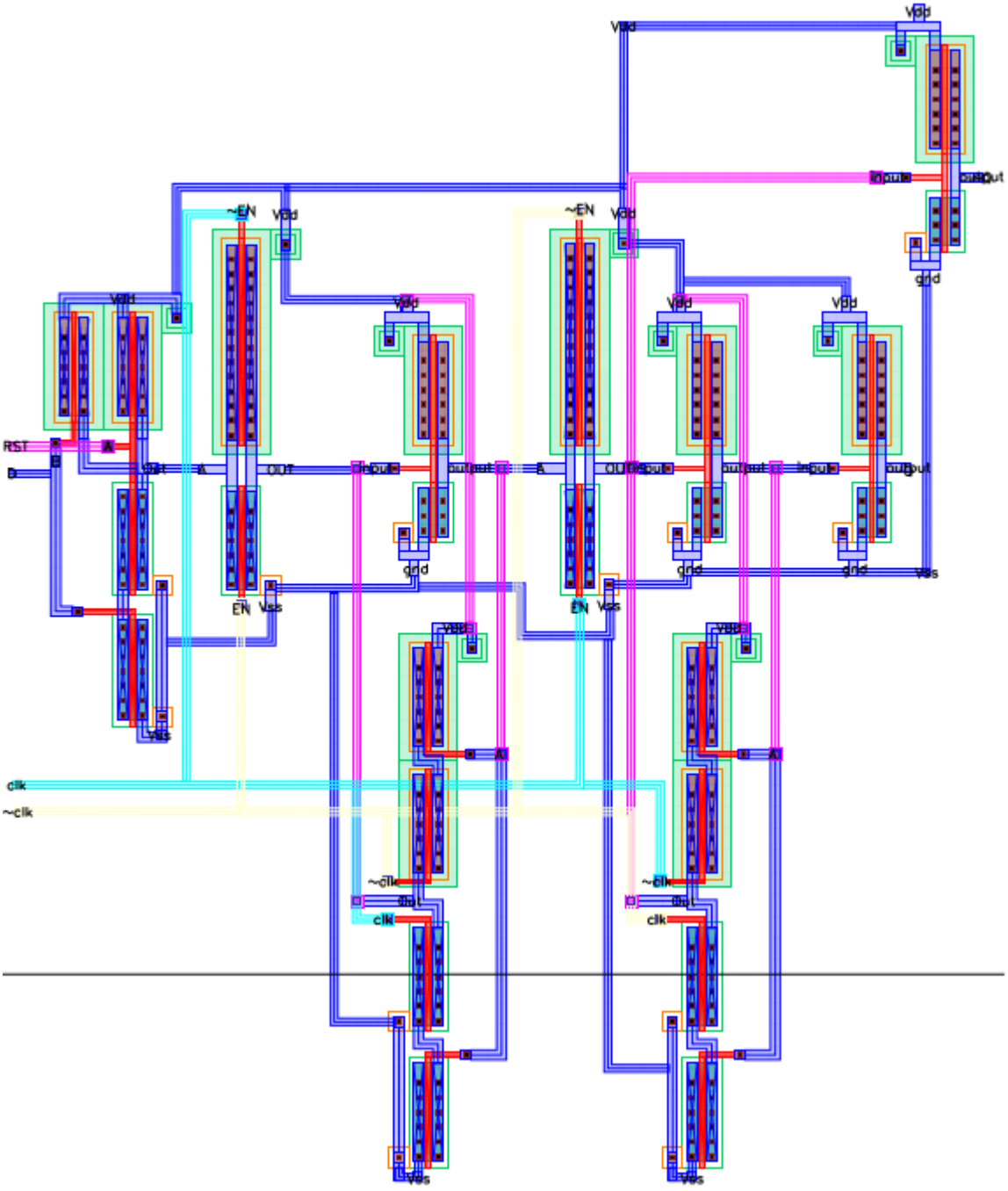
Due 5-17-18

Contents

D-Flip Flop

Layout:



LVS:

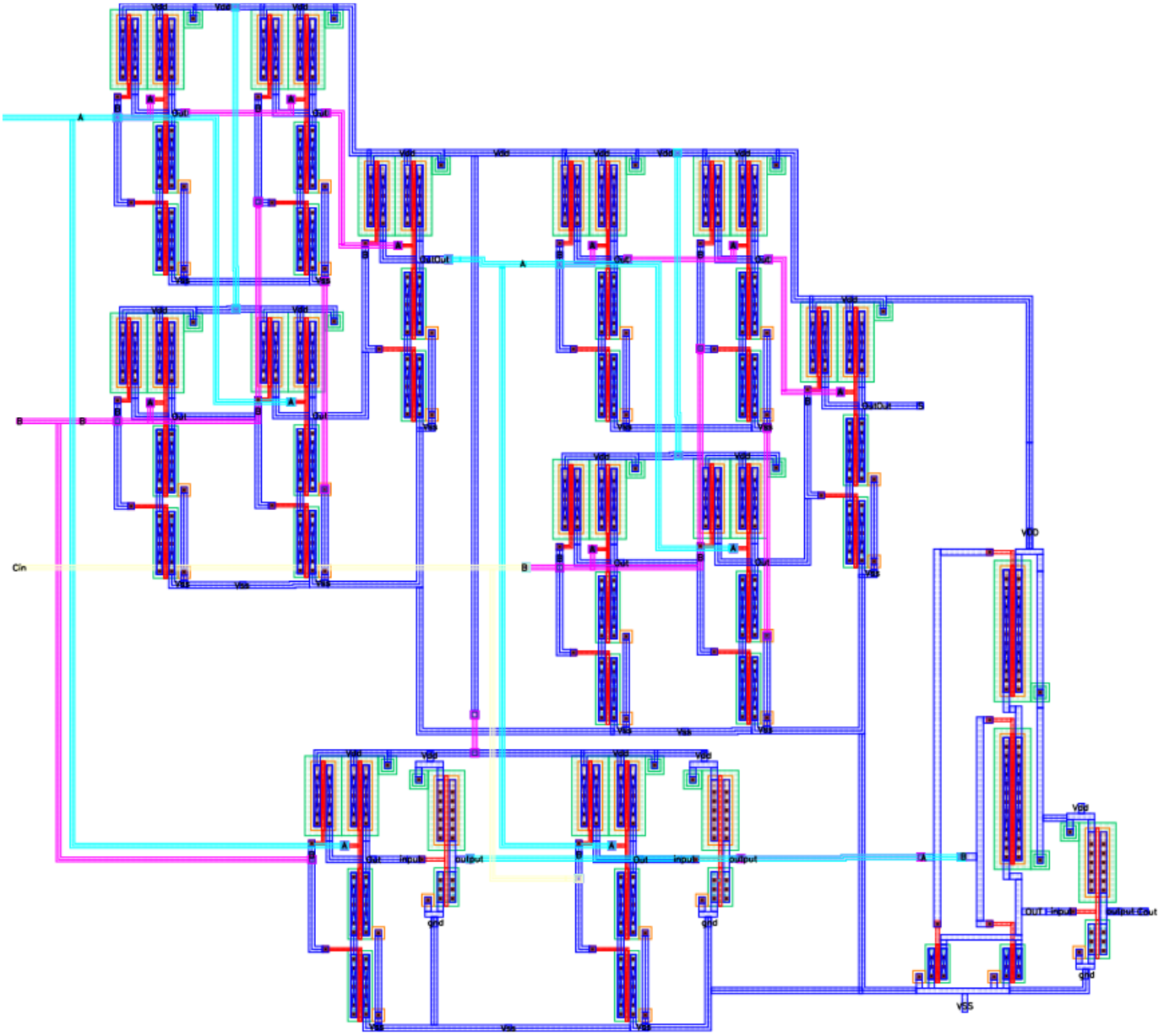
```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016

Command line:
/software/cadence/installs/IC617/tools.lnx86
/dfII/bin/64bit/LVS -dir
/gaia/class/student/sticha/CPE_151/LVS -l -s
-t
/gaia/class/student/sticha/CPE_151/LVS/layou
t
/gaia/class/student/sticha/CPE_151/LVS/schem
atic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence
points.
/gaia/class/student/sticha/CPE_151/LVS/layou
t/netlist

       count

        18              nets

        8               terminals

        12              pmos

        12              nmos

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/schem
atic/netlist

       count

        18              nets

        8               terminals

        12              pmos

        12              nmos

    Terminal correspondence points

    N13       N5        D

    N11       N4        Q

    N17       N12       Vdd

    N10       N7        Vss

    N14       N0        clk

    N15       N11       ~Q

    N12       N8        ~RST

    N16       N10       ~clk

Devices in the netlist but not in the rules:

        pcapacitor pmos nmos

The net-lists match.

          layout  schematic
                                  instances
       un-matched              0       0

       rewired                 0       0

       size errors             0       0

       pruned                  0       0

       active                  24      24

       total                   24      24

                                 nets
       un-matched              0       0

       merged                  0       0

       pruned                  0       0

       active                  18      18

       total                   18      18

                               terminals
       un-matched              0       0

       matched but

       different type          0       0

       total                   8       8

Probe files from
/gaia/class/student/sticha/CPE_151/LVS/schem
atic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from
/gaia/class/student/sticha/CPE_151/LVS/layou
t

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

DRC:

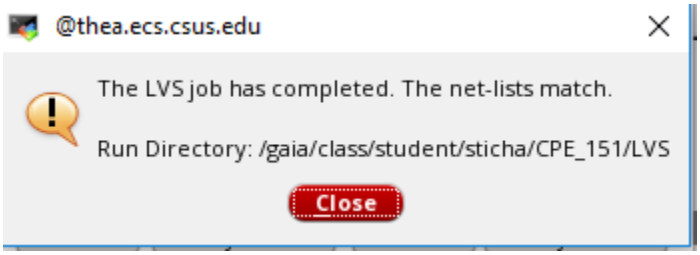
```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu May 10 11:50:36 2018
    completed ....Thu May 10 11:50:36 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "DFF_SynRst layout"   *********
   Total errors found: 0
```

Full Adder

Layout:



LVS:



@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/sticha/CPE_151/LVS -l -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist

count	
34	nets
7	terminals
29	pmos
29	nmos

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist

count	
34	nets
7	terminals
29	pmos
29	nmos

Terminal correspondence points

N30	N6	A
N29	N3	B
N31	N8	Cin
N32	N2	Cout
N28	N4	S
N33	N12	Vdd
N27	N11	Vss

Devices in the netlist but not in the rules:

pcapacitor pmos nmos

8 net-list ambiguities were resolved by random selection.

The net-lists match.

	layout	schematic
instances		
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	58	58
total	58	58
nets		
un-matched	0	0
merged	0	0

pruned	0	0
active	34	34
total	34	34

	terminals	
un-matched	0	0
matched but different type	0	0
total	7	7

Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

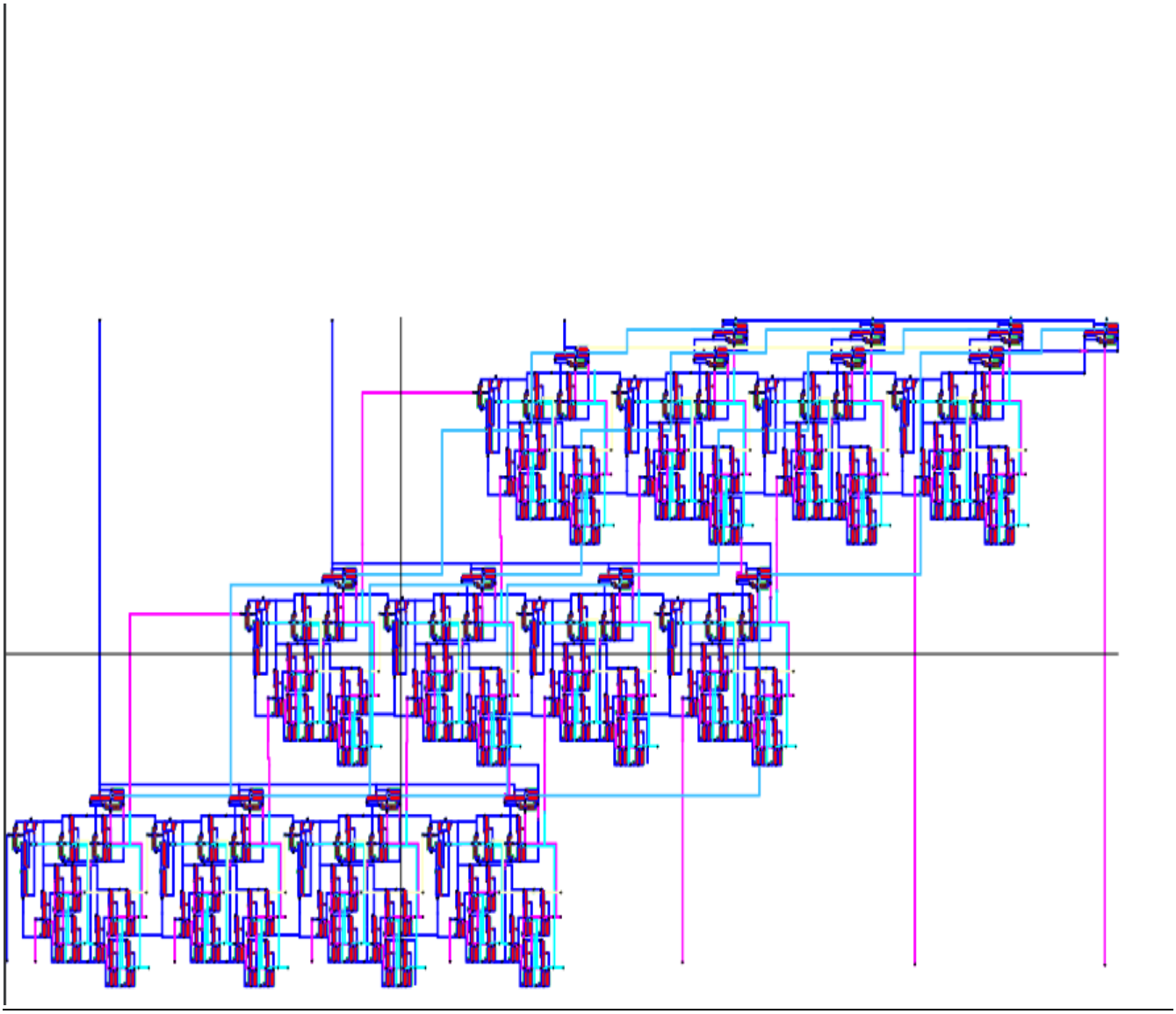
audit.out:

DRC:

```
DRC started at Thu May 17 21:29:06 2018

Validating hierarchy instantiation for:
library: CPE_151
cell:    Full_Adder
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu May 17 21:29:06 2018
    completed ....Thu May 17 21:29:06 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "Full_Adder layout"   *********
   Total errors found: 0
```

MUL_4x4

Layout:



LVS:

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/sticha/CPE_151/LVS -l -s -t
/gaia/class/student/sticha/CPE_151/LVS/layout
/gaia/class/student/sticha/CPE_151/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/layout/netlist
       count
        406             nets
        18              terminals
        396             pmos
        396             nmos

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/schematic/netlist
       count
        406             nets
        18              terminals
        396             pmos
        396             nmos


    Terminal correspondence points
    N391      N31       A0
    N390      N13       A1
    N389      N16       A2
    N388      N11       A3
    N404      N5        B0
    N403      N29       B1
    N402      N18       B2
    N401      N6        B3
    N400      N48       P0
    N399      N10       P1
    N398      N4        P2
    N397      N49       P3
    N396      N41       P4
    N395      N3        P5
    N394      N2        P6
    N393      N12       P7
    N405      N1        Vdd
    N392      N15       Vss

Devices in the netlist but not in the rules:
        pmos nmos

96 net-list ambiguities were resolved by random selection.
```

```
The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 792     792
        total                  792     792

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 406     406
        total                  406     406

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  18      18


Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
```

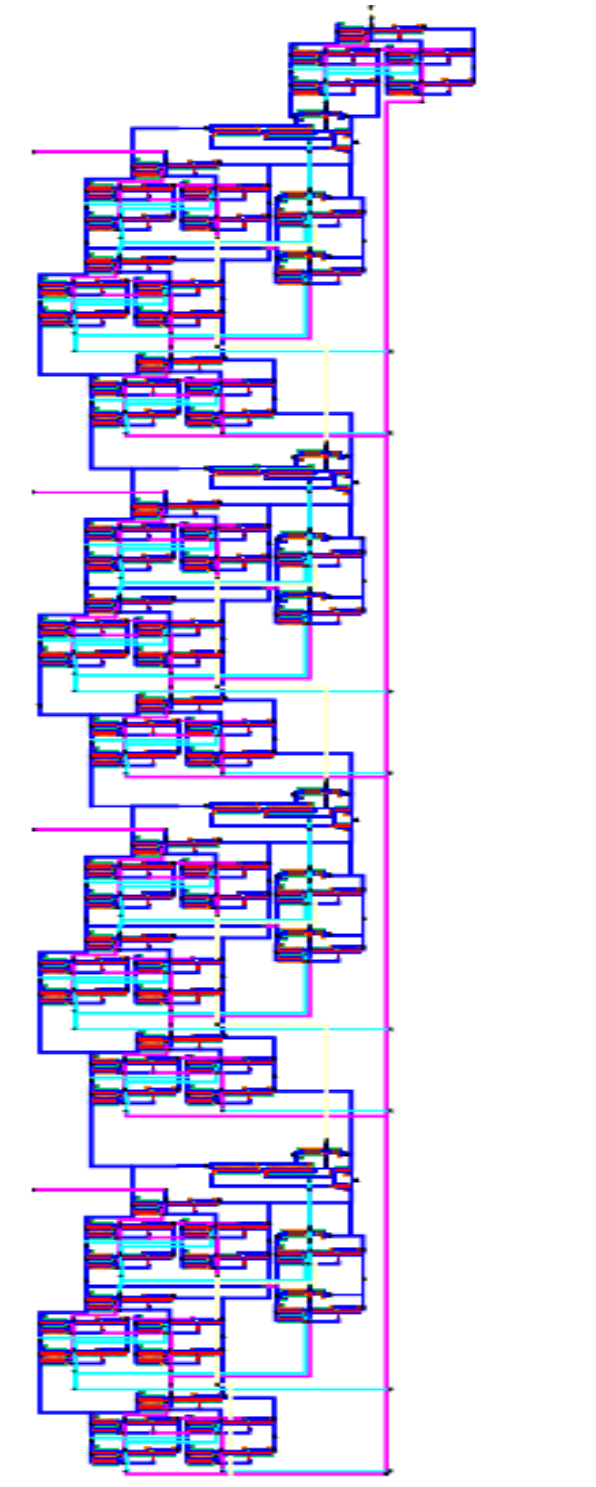
```
prunedev.out:

audit.out:
```

DRC:

```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu May 17 21:25:50 2018
    completed ....Thu May 17 21:25:52 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:02
*********   Summary of rule violations for cell "MUL_4x4 layout"   *********
   Total errors found: 0
```

Add Sub:

Layout:



LVS:

```
LVS job is now started...
The LVS job has completed. The net-lists match.
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/sticha/CPE_151/LVS -l -s -t
/gaia/class/student/sticha/CPE_151/LVS/layout
/gaia/class/student/sticha/CPE_151/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/layout/netlist
       count
        177             nets
        16              terminals
        166             pmos
        166             nmos

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/schematic/netlist
       count
        177             nets
        16              terminals
        166             pmos
        166             nmos


    Terminal correspondence points
    N167      N13       A0
    N166      N14       A1
    N165      N20       A2
    N164      N10       A3
    N174      N23       B0
    N173      N19       B1
    N172      N17       B2
    N171      N1        B3
    N170      N15       Cout
    N163      N21       S0
    N162      N11       S1
    N161      N3        S2
    N176      N16       S3
    N169      N8        Sub
    N175      N22       Vdd
```

```
    N168      N18       Vss

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 332     332
        total                  332     332

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 177     177
        total                  177     177

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  16      16


Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:
```

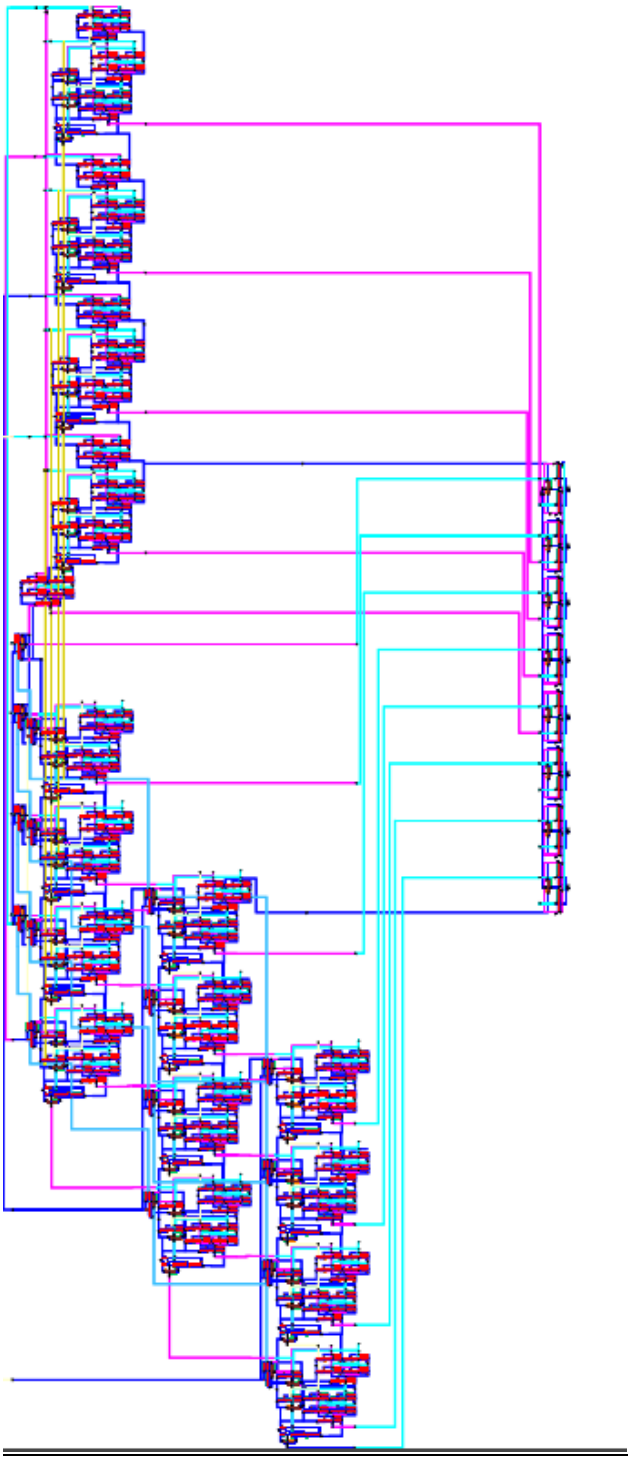
```
termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

DRC:

```
DRC started at Thu May 17 21:32:21 2018

Validating hierarchy instantiation for:
library: CPE_151
cell:    Add_Sub_4
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu May 17 21:32:21 2018
    completed ....Thu May 17 21:32:22 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:01
*********   Summary of rule violations for cell "Add_Sub_4 layout"   *********
   Total errors found: 0
```

ALU_4bit:

Layout:



LVS:

@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/sticha/CPE_151/LVS -l -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist

count

593 nets

20 terminals

586 pmos

586 nmos

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist

count

593 nets

20 terminals

586 pmos

586 nmos

Terminal correspondence points

N576 N3 A0

N575 N18 A1

N574 N19 A2

N573 N20 A3

N591 N15 B0

N590 N22 B1

N589 N24 B2

N588 N23 B3

N587 N26 M0

N586 N16 M1

N585 N29 M2

N584 N30 M3

N583 N17 M4

N582 N27 M5

N581 N12 M6

N580 N31 M7

N579 N28 MULT_SEL

N578 N34 Sub_EN

N592 N33 Vdd

N577 N21 Vss

Devices in the netlist but not in the rules:

pmos nmos

148 net-list ambiguities were resolved by random selection.

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	1172	1172
total	1172	1172

	nets	
un-matched	**0**	**0**
merged	**0**	**0**
pruned	**0**	**0**
active	**593**	**593**
total	**593**	**593**

	terminals	
un-matched	**0**	**0**
matched but		
different type	**0**	**0**
total	**20**	**20**

Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

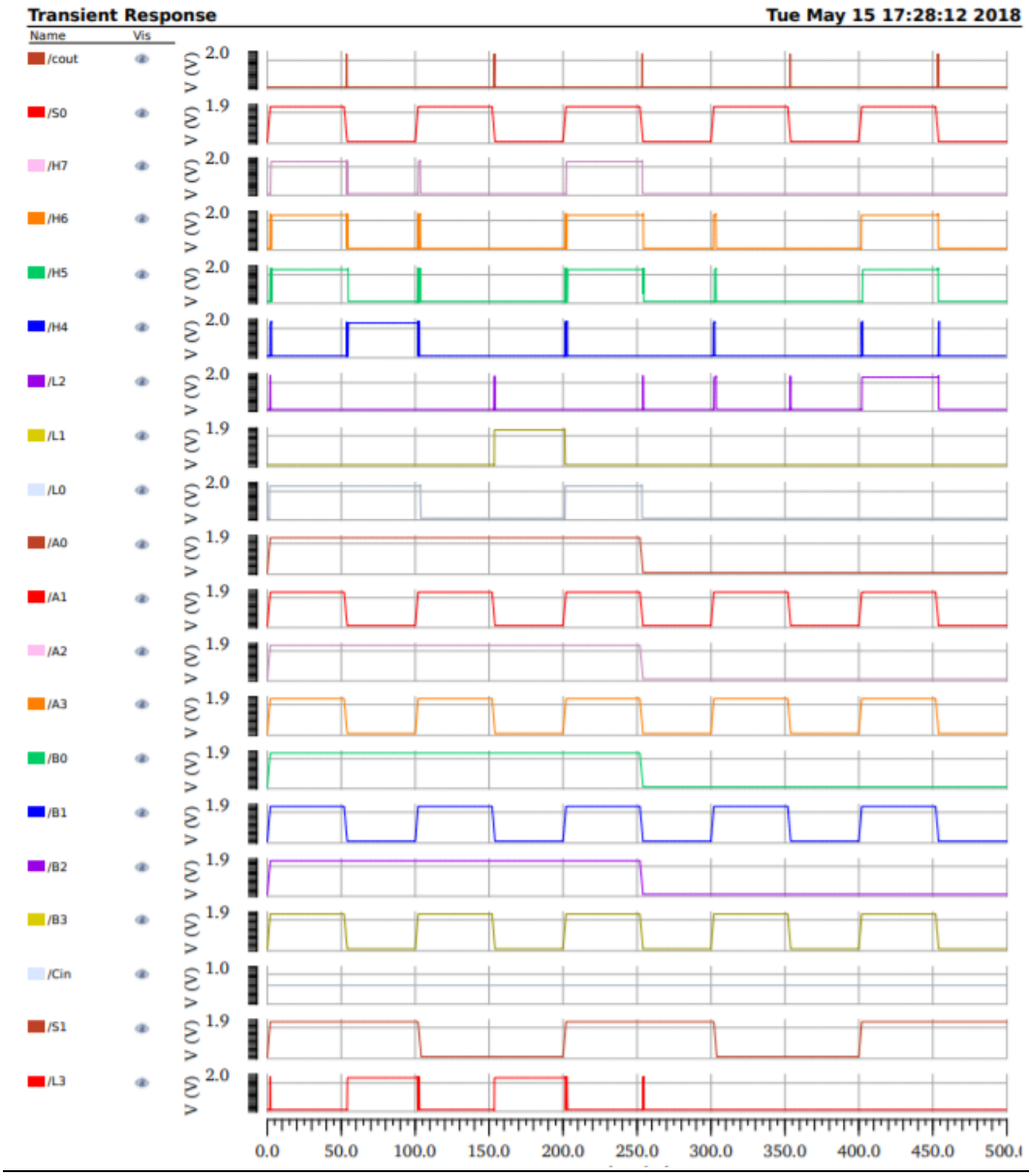
prunedev.out:

audit.out:

DRC:

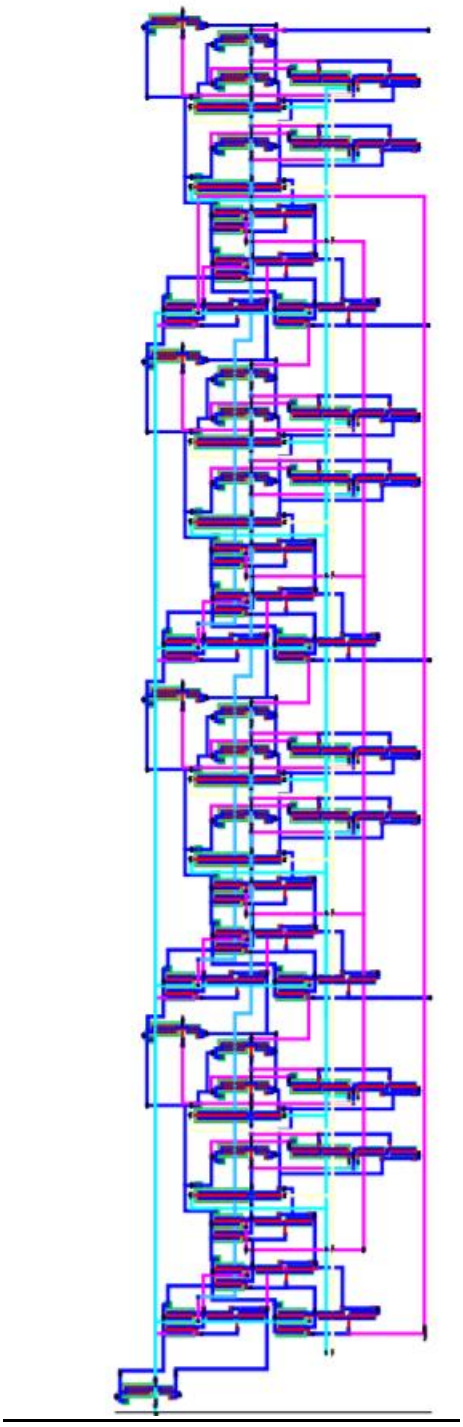
```
DRC started at Thu May 17 21:33:57 2018

Validating hierarchy instantiation for:
library: CPE_151
cell:    ALU_4bit
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu May 17 21:33:57 2018
    completed ....Thu May 17 21:33:59 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:02
*********   Summary of rule violations for cell "ALU_4bit layout"   *********
   Total errors found: 0
```

Waveform:

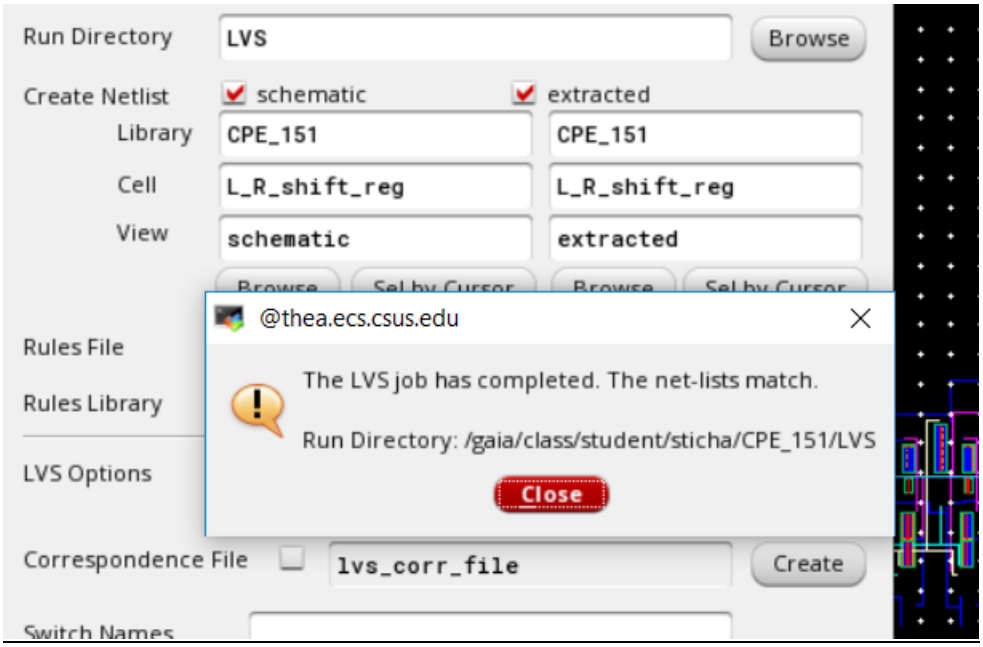

Transient Response
Tue May 15 17:28:12 2018
Name
Vis
/cout
/S0
/H7
/H6
/H5
/H4
/L2
/L1
/L0
/A0
/A1
/A2
/A3
/B0
/B1
/B2
/B3
/Cin
/S1
/L3
V (V)
2.0
1.9
1.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0

Extra Credit Shift Register:

Layout:



LVS:




```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/sticha/CPE_151/LVS -l -s -t
/gaia/class/student/sticha/CPE_151/LVS/layout
/gaia/class/student/sticha/CPE_151/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/layout/netlist
       count
        80              nets
        11              terminals
        73              pmos
        73              nmos

    Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/schematic/netlist
       count
        80              nets
        11              terminals
        73              pmos
        73              nmos


    Terminal correspondence points
    N75       N18       Q0
    N74       N24       Q1
```

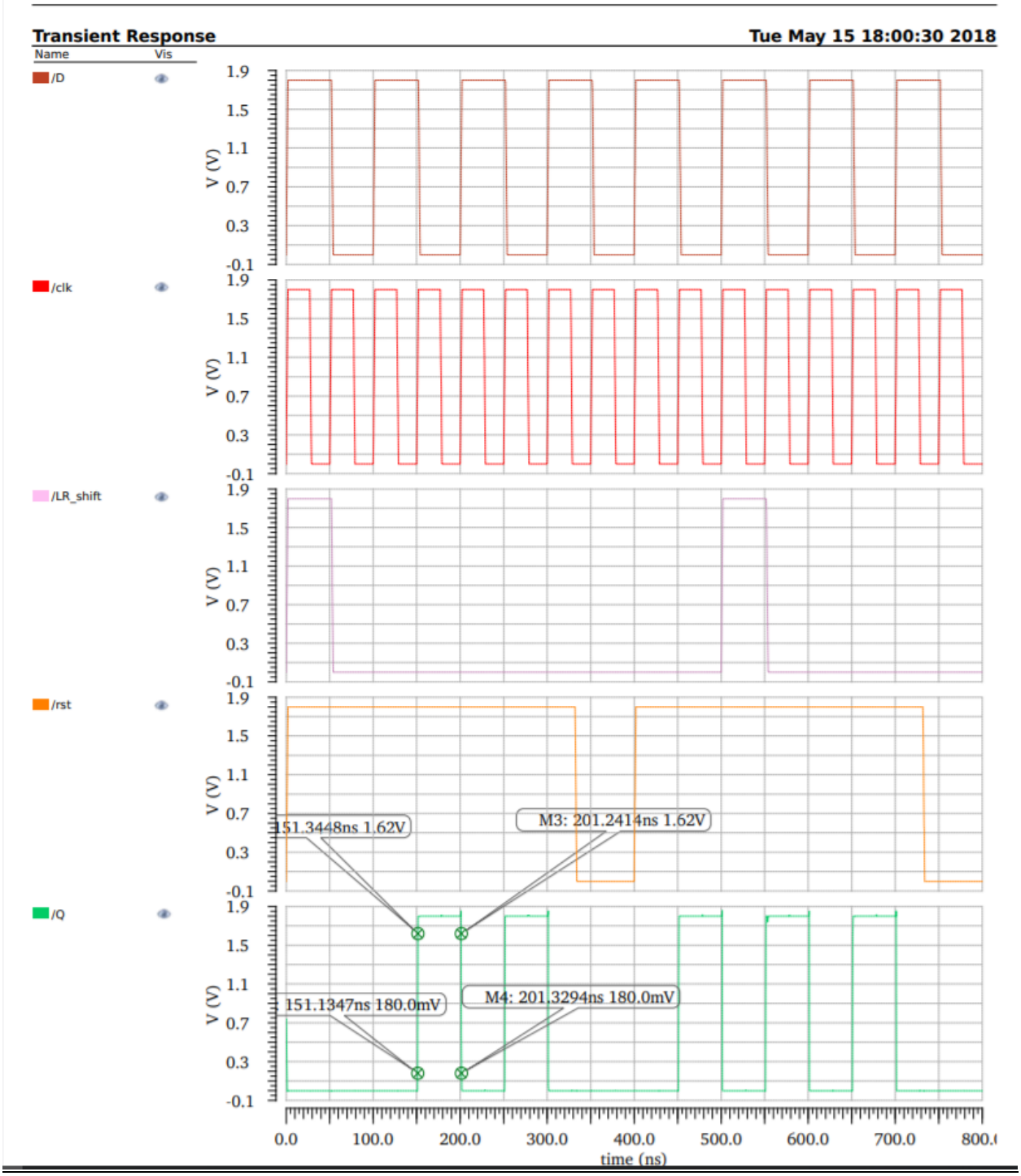
```
    N73       N25       Q2
    N72       N6        Q3
    N69       N27       RST
    N77       N4        R_L
    N79       N19       Vdd
    N71       N3        Vss
    N76       N21       clk
    N70       N1        input_data
    N78       N23       ~clk

Devices in the netlist but not in the rules:
        pmos nmos

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  146     146
        total                   146     146

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  80      80
        total                   80      80

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   11      11


Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

```
Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

DRC:

```
executing: saveDerived(geomAndNot(via5 metal6) errMesg)
DRC started.......Sun May 20 16:34:47 2018
    completed ....Sun May 20 16:34:47 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "L_R_shift_reg layout"   *********
   Total errors found: 0
```

Waveform:


Transient Response
Tue May 15 18:00:30 2018
Name
Vis
/D
/clk
/LR_shift
/rst
/Q
V (V)
1.9
1.5
1.1
0.7
0.3
-0.1
M3: 201.2414ns 1.62V
151.3448ns 1.62V
M4: 201.3294ns 180.0mV
151.1347ns 180.0mV
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
time (ns)