Project 1: part 2

CPE 151: CMOS & VLSI

Section 1

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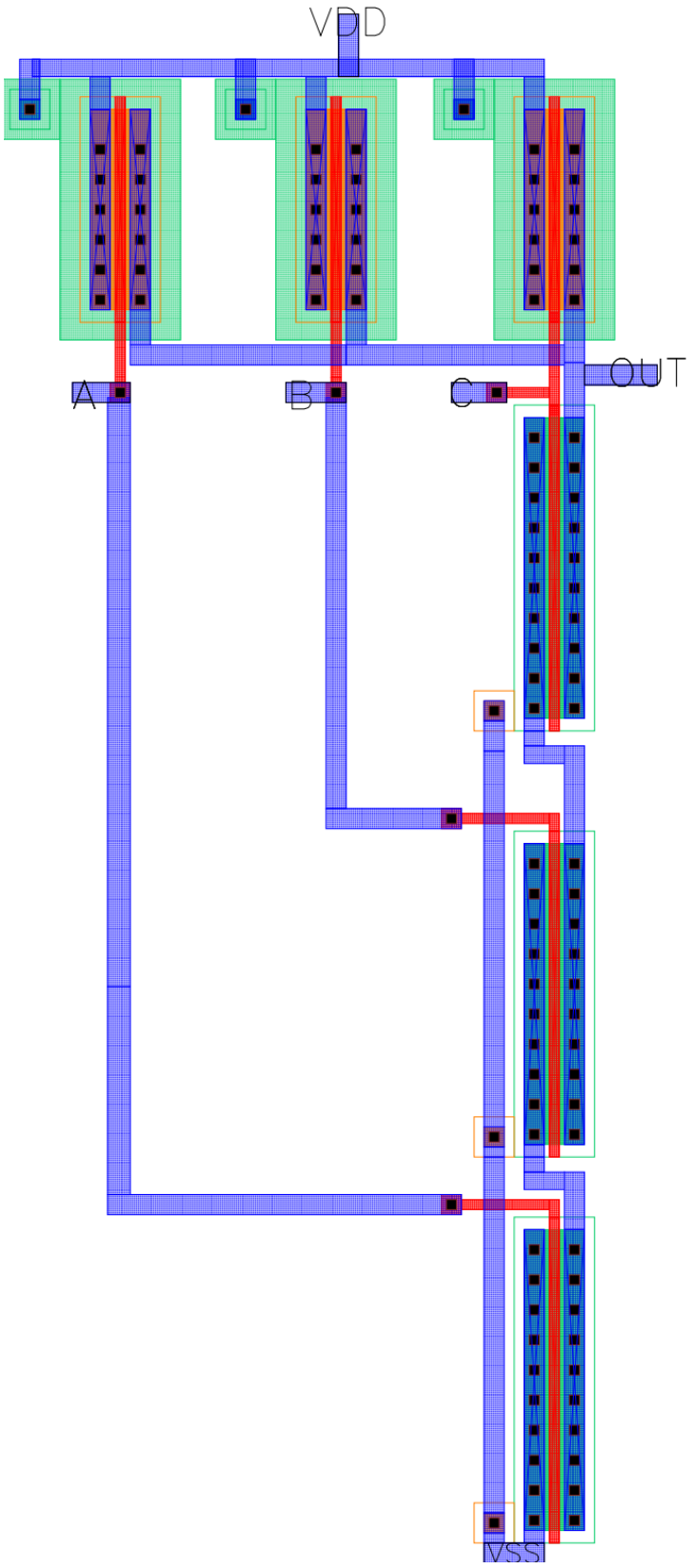
**3 Input NAND: Layout**



## DRC Check:

```
Validating hierarchy instantiation for:
library: Project1
cell:    NAND_3
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Tue Mar 20 12:37:49 2018
    completed ....Tue Mar 20 12:37:49 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "NAND_3 layout"   *********
   Total errors found: 0
```

# LVS Check:

@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/gaia/class/student/sticha/CPE_151/LVS -l -s -t
/gaia/class/student/sticha/CPE_151/LVS/layout
/gaia/class/student/sticha/CPE_151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/layout/netlist

| count | |
|---|---|
| 8 | nets |
| 6 | terminals |
| 3 | pmos |
| 3 | nmos |

Net-list summary for
/gaia/class/student/sticha/CPE_151/LVS/schematic/netlist

| count | |
|---|---|
| 8 | nets |
| 6 | terminals |
| 3 | pmos |
| 3 | nmos |

Terminal correspondence points

| | | |
|---|---|---|
| N6 | N1 | A |
| N5 | N2 | B |
| N4 | N6 | C |
| N3 | N7 | Out |
| N7 | N5 | VDD |
| N2 | N4 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|---|---|---|
| instances | | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |
| nets | | |
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 8 | 8 |
| total | 8 | 8 |
| terminals | | |
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 6 | 6 |

Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

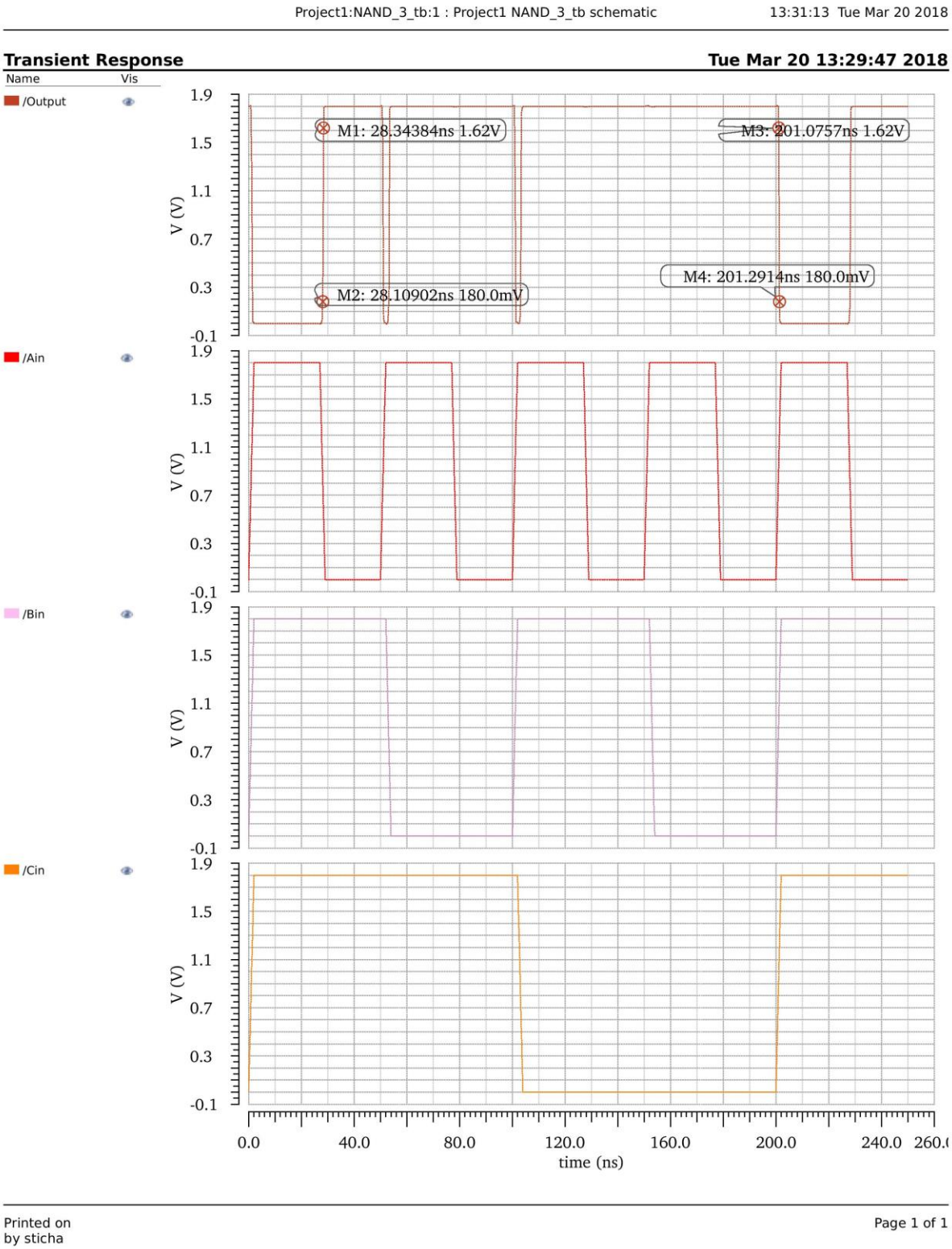
termbad.out:

prunenet.out:

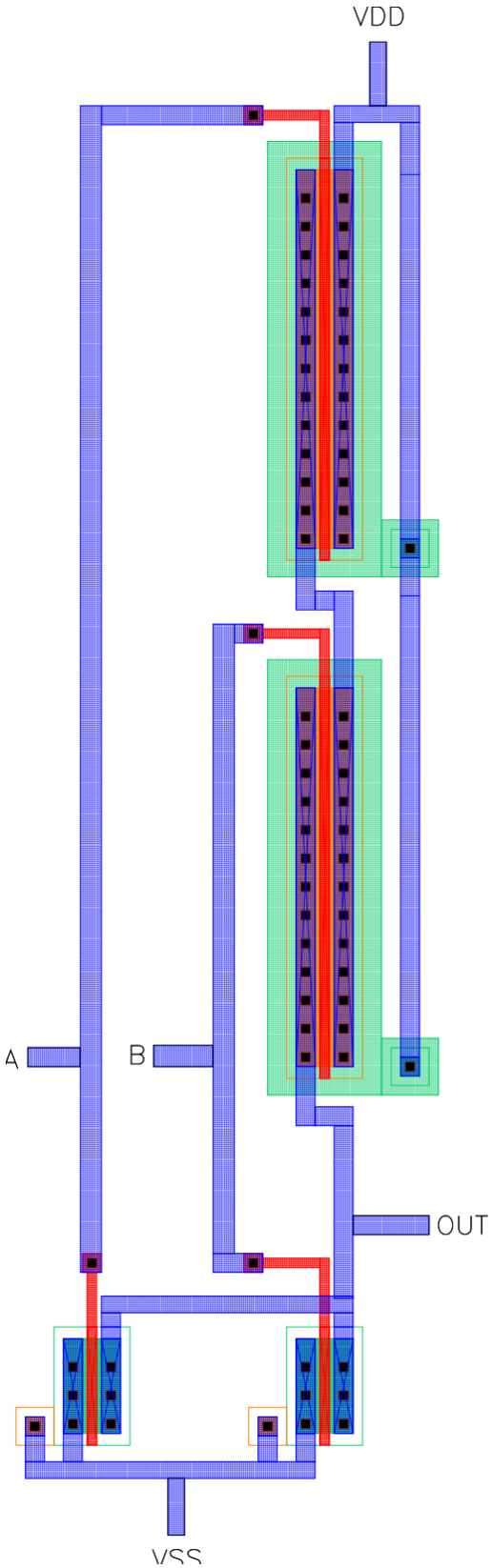
prunedev.out:

audit.out:

## Post-Layout Simulation:



## 2 Input NOR: Layout



## DRC Check

```
Validating hierarchy instantiation for:
library: Project1
cell:    NOR_2
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Tue Mar 20 12:38:55 2018
    completed ....Tue Mar 20 12:38:55 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "NOR_2 layout"   *********
   Total errors found: 0
```

# LVS Check:

@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/sticha/CPE_151/LVS -l -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist

| count | |
|---|---|
| 6 | nets |
| 5 | terminals |
| 2 | pmos |
| 2 | nmos |

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist

| count | |
|---|---|
| 6 | nets |
| 5 | terminals |
| 2 | pmos |
| 2 | nmos |

Terminal correspondence points

| | | |
|---|---|---|
| N4 | N0 | A |
| N3 | N1 | B |
| N2 | N5 | OUT |
| N5 | N2 | VDD |
| N1 | N3 | VSS |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|---|---|---|
| instances | | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 4 | 4 |
| total | 4 | 4 |

| nets | | |
|---|---|---|
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |

| terminals | | |
|---|---|---|
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 5 | 5 |

Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

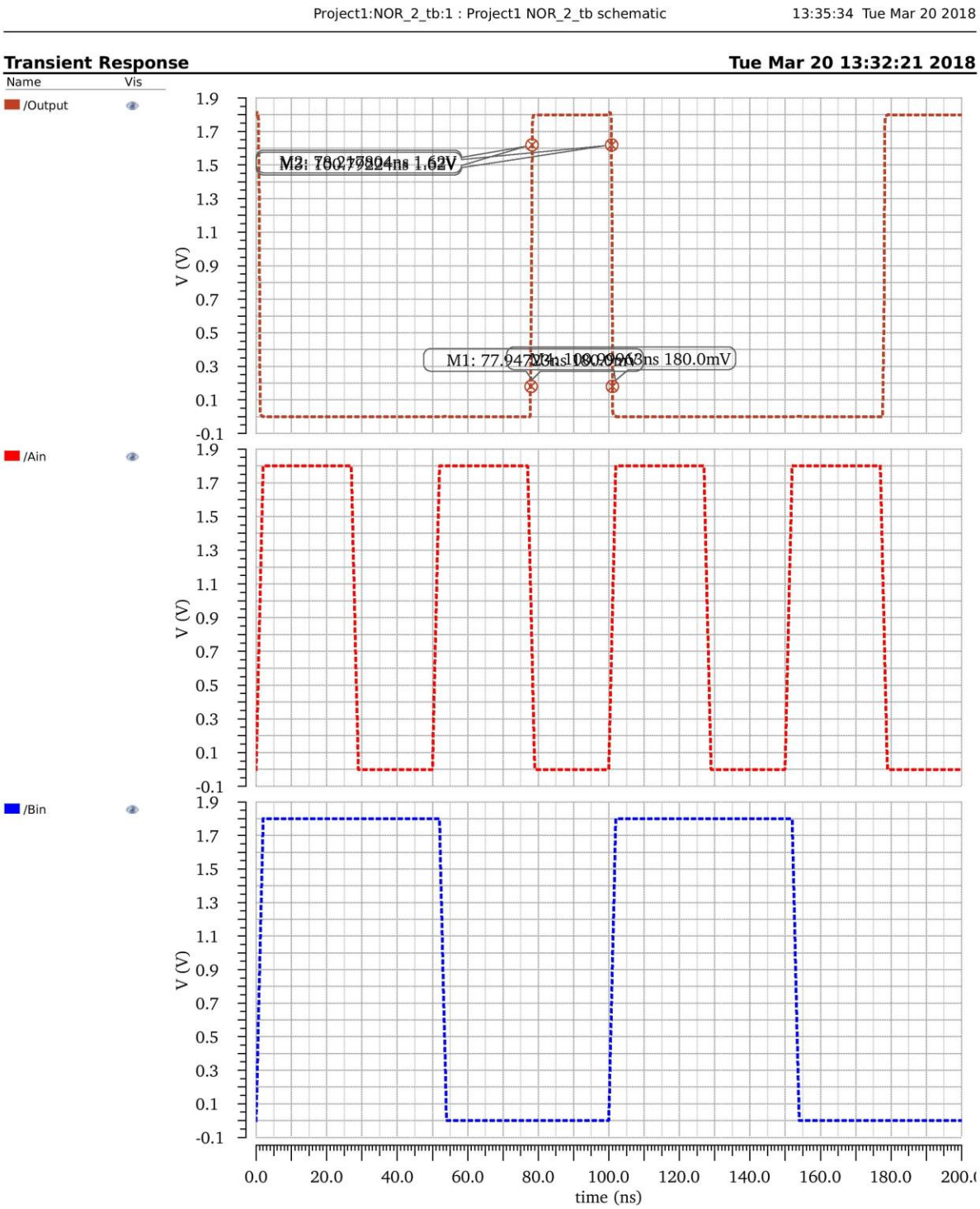
termbad.out:

prunenet.out:

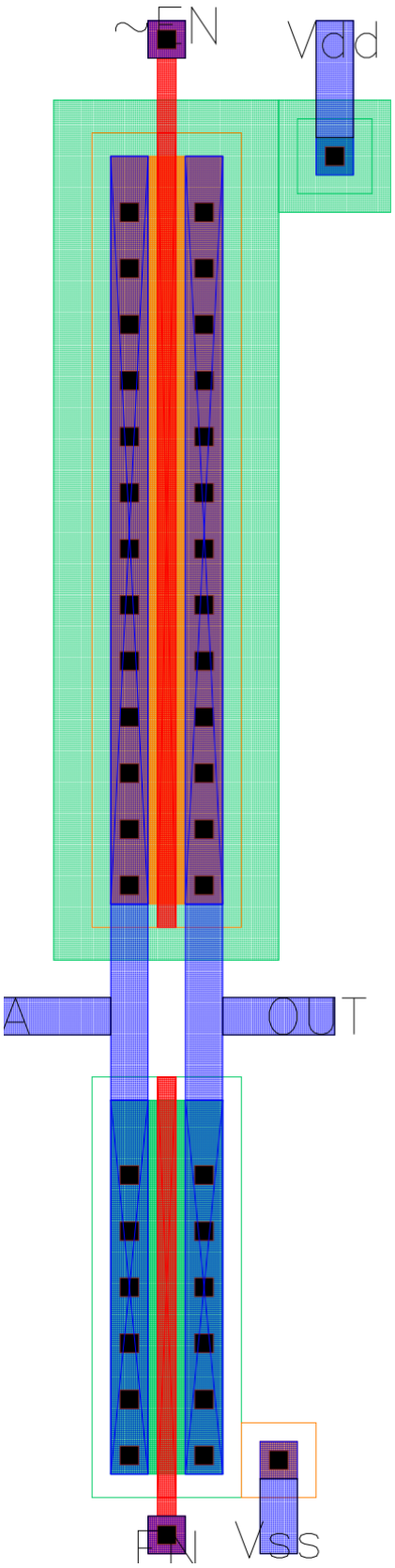
prunedev.out:

audit.out:

## Post-Layout Simulation:



**Transmission Gate: Layout**



## DRC Check:

```
Validating hierarchy instantiation for:
library: Project1
cell:    T_Gate
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Tue Mar 20 12:39:31 2018
    completed ....Tue Mar 20 12:39:31 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "T_Gate layout"   *********
   Total errors found: 0
```

# LVS Check:

@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/sticha/CPE_151/LVS -l -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist

| count | |
|---|---|
| 6 | nets |
| 6 | terminals |
| 1 | pmos |
| 1 | nmos |

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist

| count | |
|---|---|
| 6 | nets |
| 6 | terminals |
| 1 | pmos |
| 1 | nmos |

Terminal correspondence points

| | | |
|---|---|---|
| N3 | N0 | A |
| N2 | N3 | EN |
| N1 | N4 | OUT |
| N5 | N5 | Vdd |
| N0 | N2 | Vss |
| N4 | N1 | ~EN |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|---|---|---|
| instances | | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 2 | 2 |
| total | 2 | 2 |
| nets | | |
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |
| terminals | | |
| un-matched | 0 | 0 |
| matched but | | |
| different type | 0 | 0 |
| total | 6 | 6 |

Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

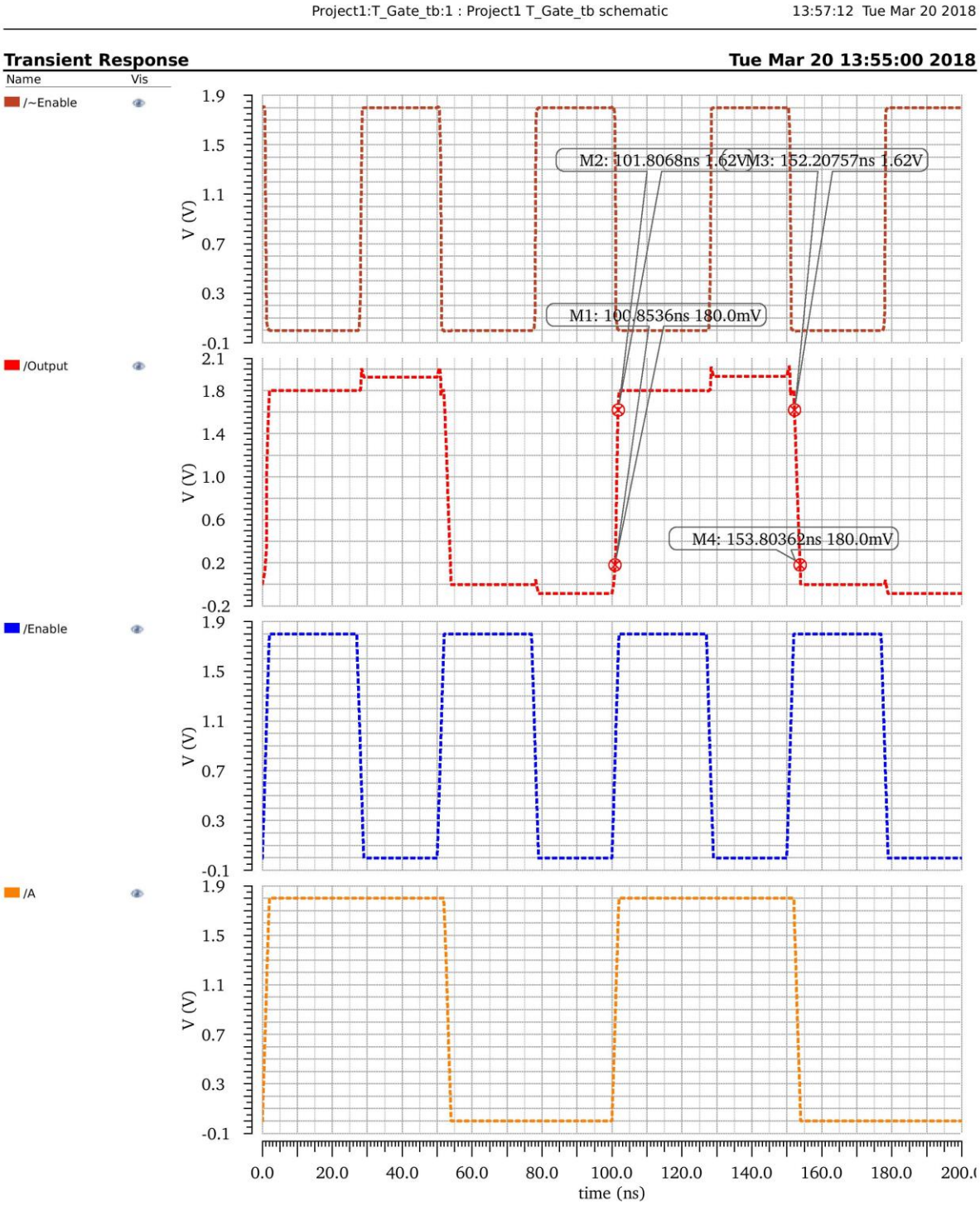
termbad.out:

prunenet.out:

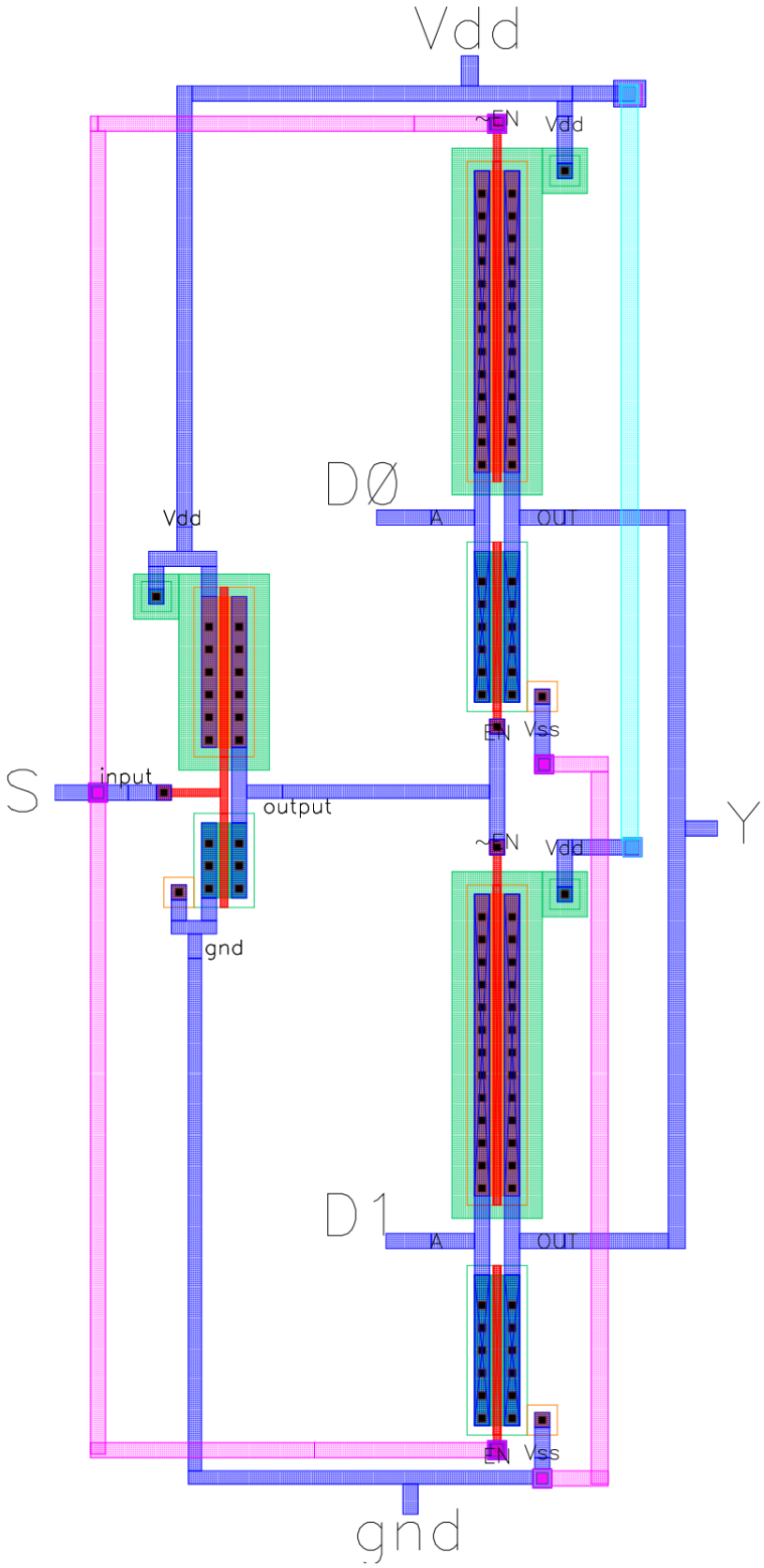
prunedev.out:

audit.out:

## Post-Layout Simulation:



## Two-to-one Multiplexer: Layout



## DRC Check

```
Getting layout propert bagGetting layout propert bag
DRC started at Tue Mar 20 12:32:18 2018

Validating hierarchy instantiation for:
library: Project1
cell:    MUX2_1
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Tue Mar 20 12:32:18 2018
    completed ....Tue Mar 20 12:32:18 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "MUX2_1 layout"   *********
   Total errors found: 0
```

# LVS Check:

@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /gaia/class/student/sticha/CPE_151/LVS -l -s -t /gaia/class/student/sticha/CPE_151/LVS/layout /gaia/class/student/sticha/CPE_151/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/layout/netlist

| count | |
|---|---|
| 7 | nets |
| 6 | terminals |
| 3 | pmos |
| 3 | nmos |

Net-list summary for /gaia/class/student/sticha/CPE_151/LVS/schematic/netlist

| count | |
|---|---|
| 7 | nets |
| 6 | terminals |
| 3 | pmos |
| 3 | nmos |

Terminal correspondence points

| | | |
|---|---|---|
| N5 | N4 | D0 |
| N4 | N0 | D1 |
| N3 | N6 | S |
| N6 | N3 | Vdd |
| N1 | N2 | Vss |
| N2 | N1 | Y |

Devices in the netlist but not in the rules:

pmos nmos

The net-lists match.

| | layout | schematic |
|---|---|---|
| instances | | |
| un-matched | 0 | 0 |
| rewired | 0 | 0 |
| size errors | 0 | 0 |
| pruned | 0 | 0 |
| active | 6 | 6 |
| total | 6 | 6 |
| nets | | |
| un-matched | 0 | 0 |
| merged | 0 | 0 |
| pruned | 0 | 0 |
| active | 7 | 7 |
| total | 7 | 7 |
| terminals | | |
| un-matched | 0 | 0 |
| matched but different type | 0 | 0 |
| total | 6 | 6 |

Probe files from /gaia/class/student/sticha/CPE_151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student/sticha/CPE_151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

# Post-Layout Simulation: (D0 tied to Ground)