# Project 1: part 1

# CPE 151: CMOS & VLSI
Section 1
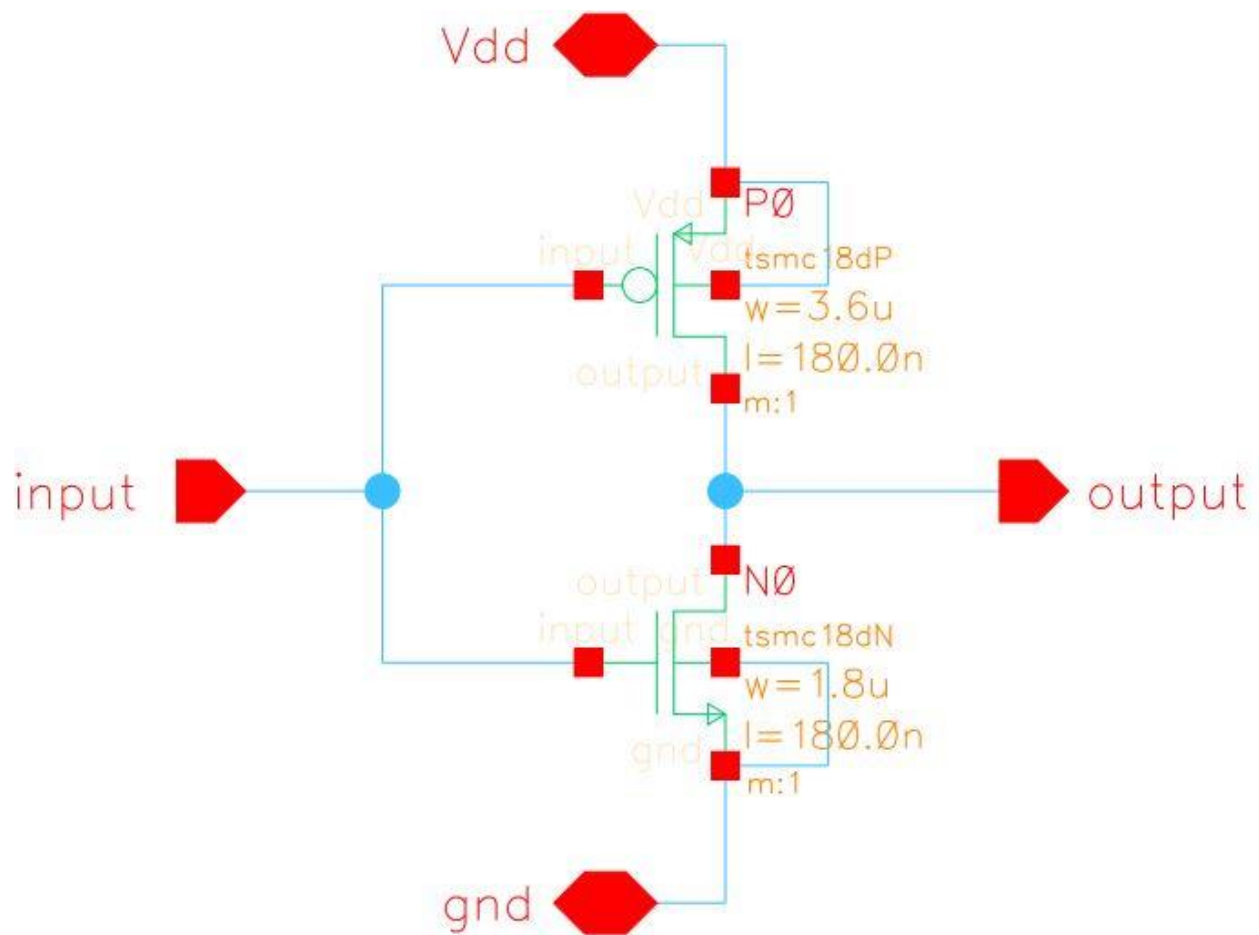Dr. Praveen Meduri

Andrew Stich
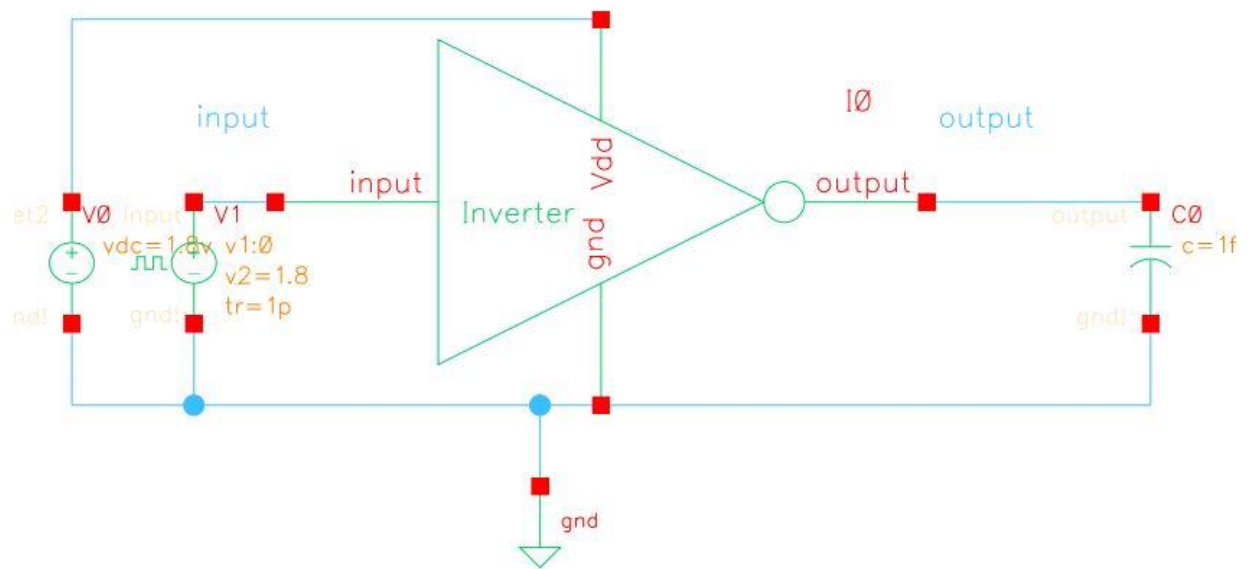3-9-18

**Inverter**
**$(W/L)_n = (1.8/0.18)$**
**$(W/L)_p = (3.6/0.18)$**

Schematic (Inverter)

Vdd

PØ
tsmc18dP
w=3.6u
l=180.0n
m:1

input

output

NØ
tsmc18dN
w=1.8u
l=180.0n
m:1

gnd

# Test-Bench (inverter)

# Inverter Test:

**Transient Response**                                    **Thu Mar 8 18:41:17 2018**

| Name | Vis |
|------|-----|
| /input | |
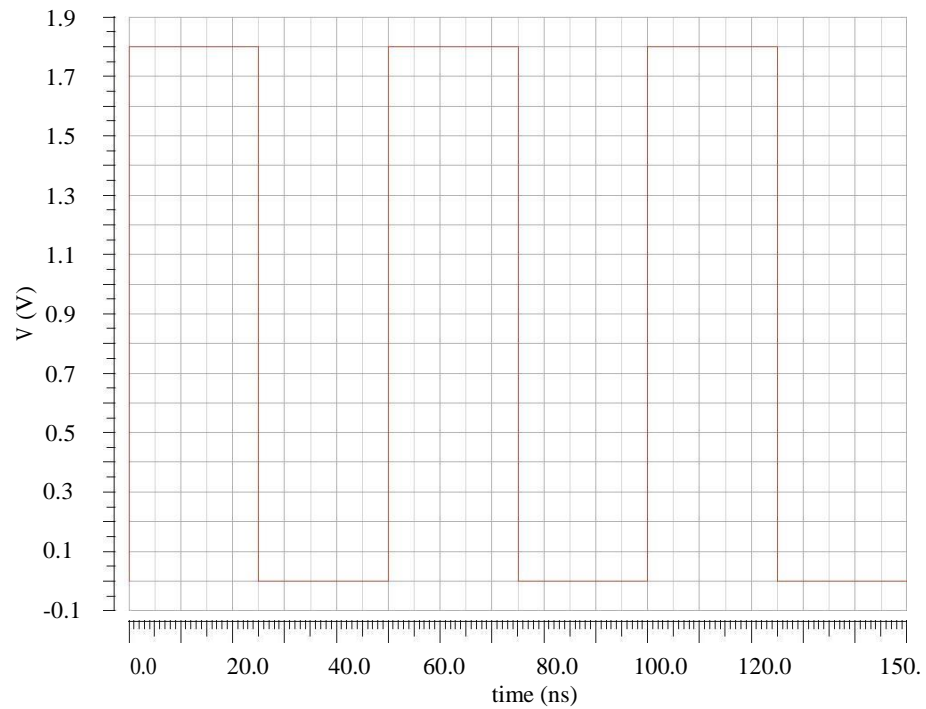


**Transient Analysis `tran': time = (0 s -> 150 ns)**
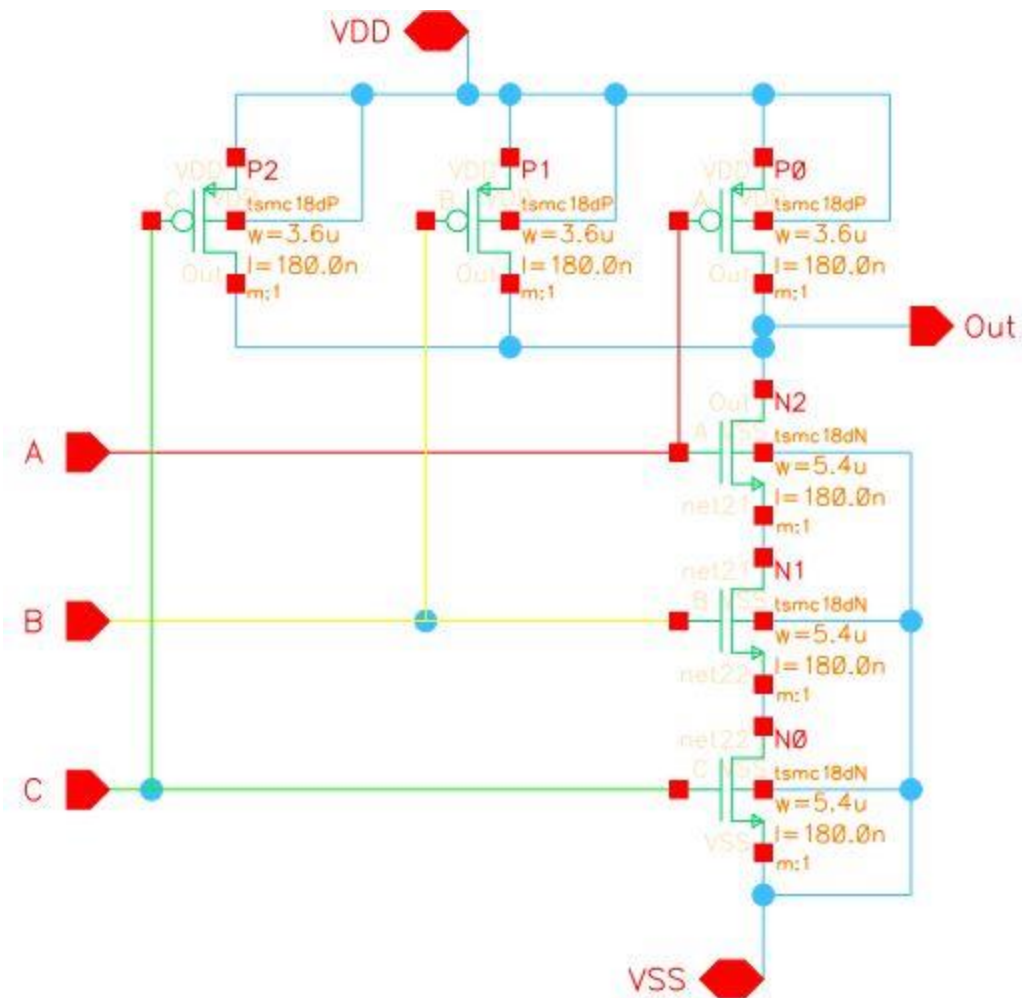
| Name |
|------|
| /output |
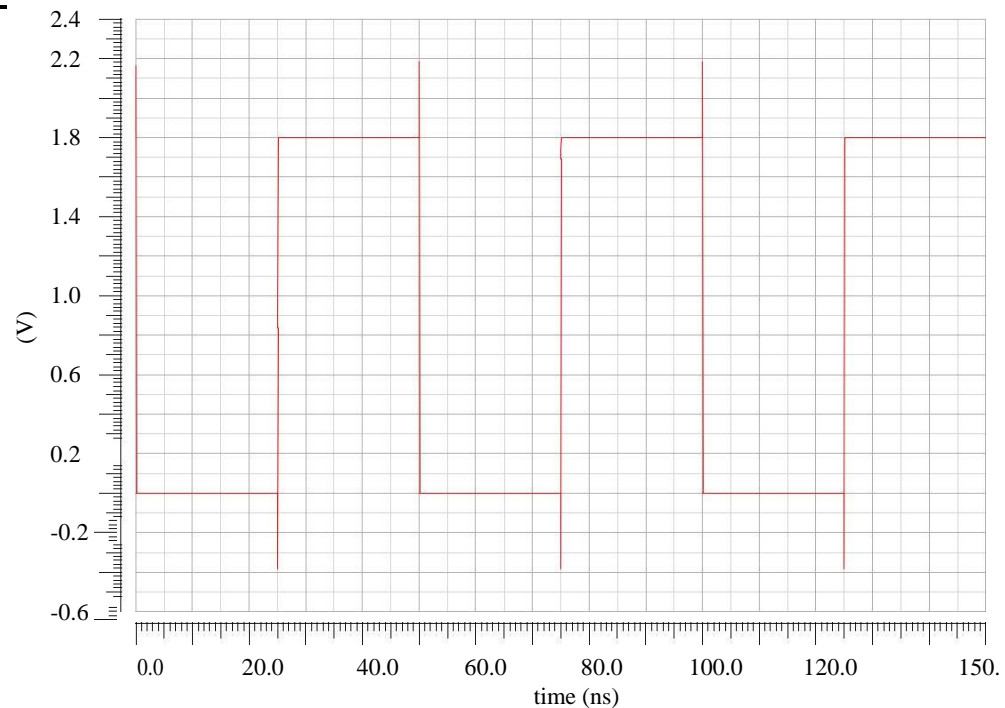
Layout (Inverter)
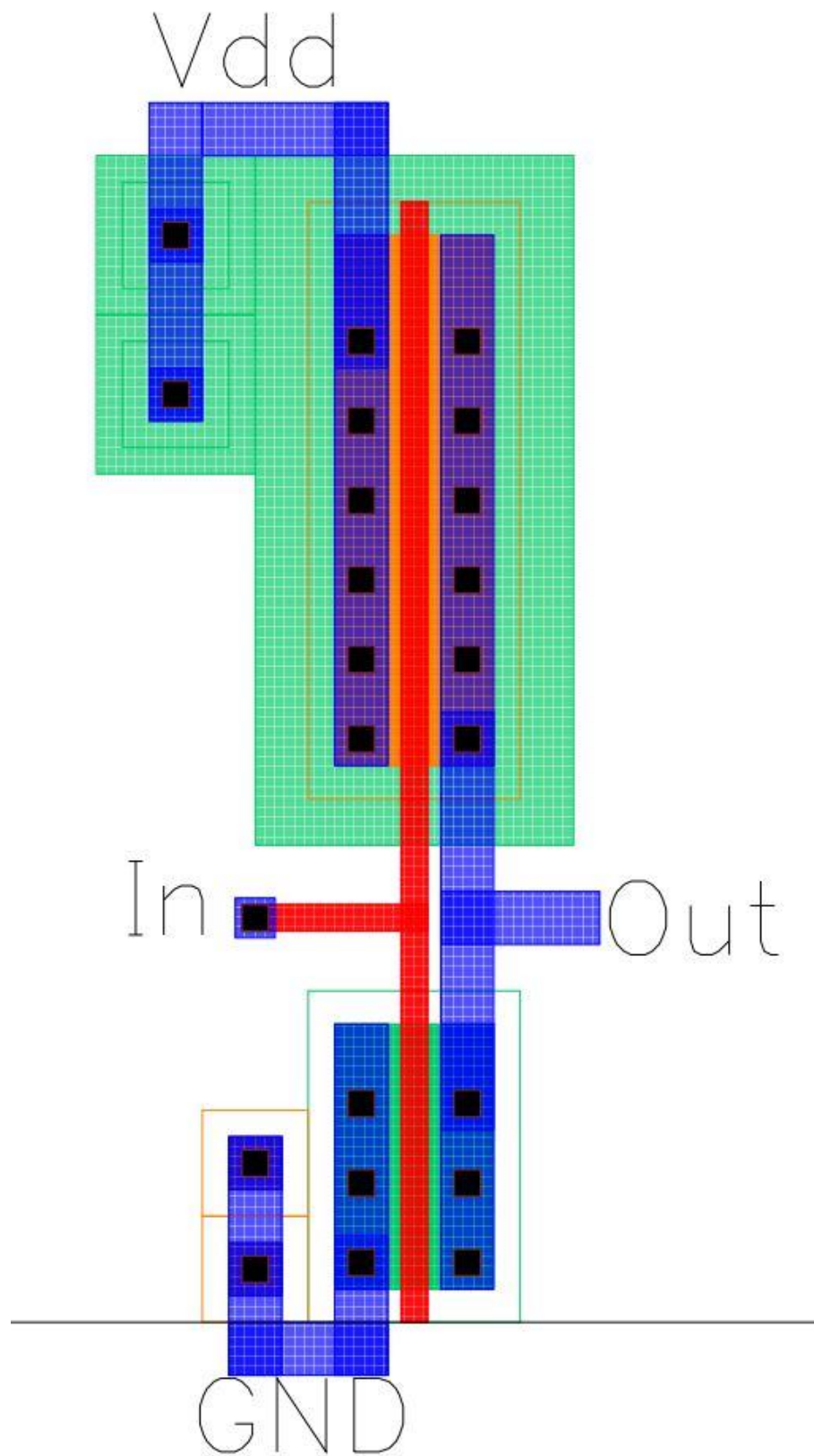
# 3-Input NAND gate
## $(W/L)_n = (5.4/0.18)$
## $(W/L)_p = (3.6/0.18)$

Schematic (NAND)

Test-bench (NAND)

# NAND test Project1:NAND_3_tb:1 : Project1 NAND_3_tb schematic 18:33:41 Thu Mar 8 2018
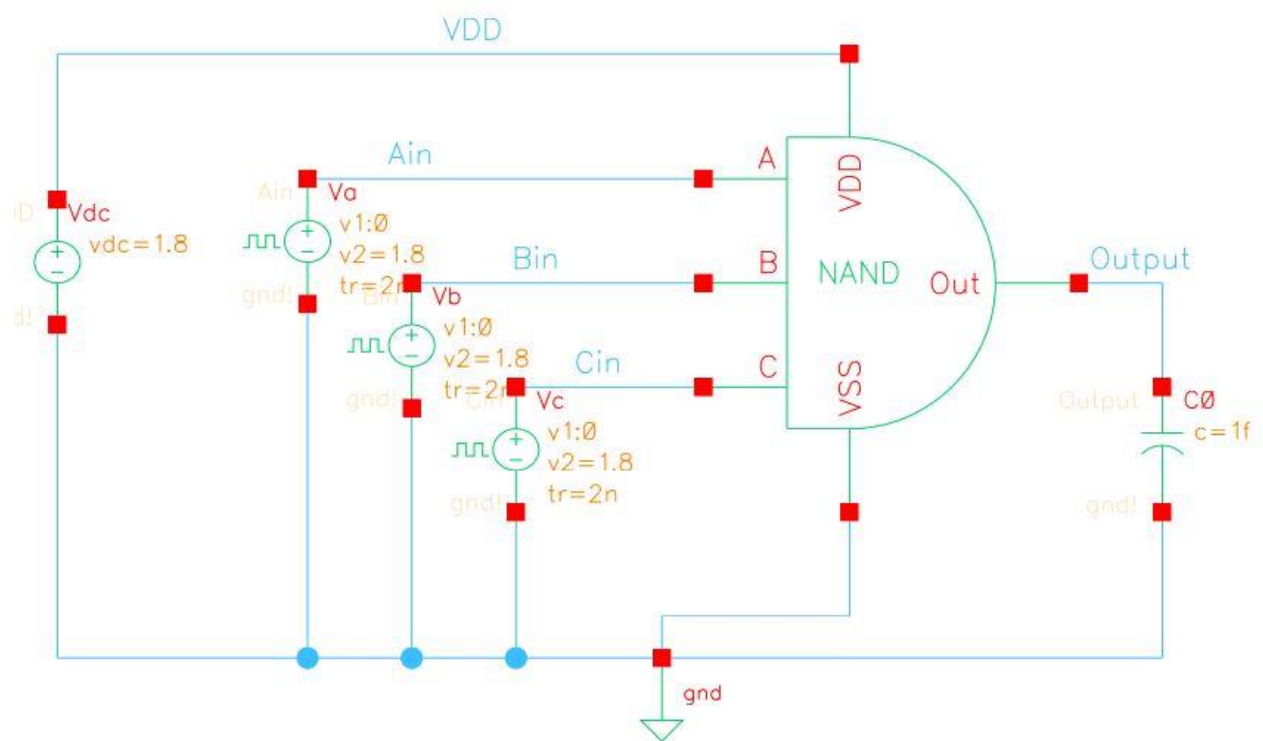
**Transient Response**                                    **Thu Mar 8 18:31:44 2018**

| Name | Vis |
|------|-----|
| /Ain | |
| /Bin | |
| /Cin | |
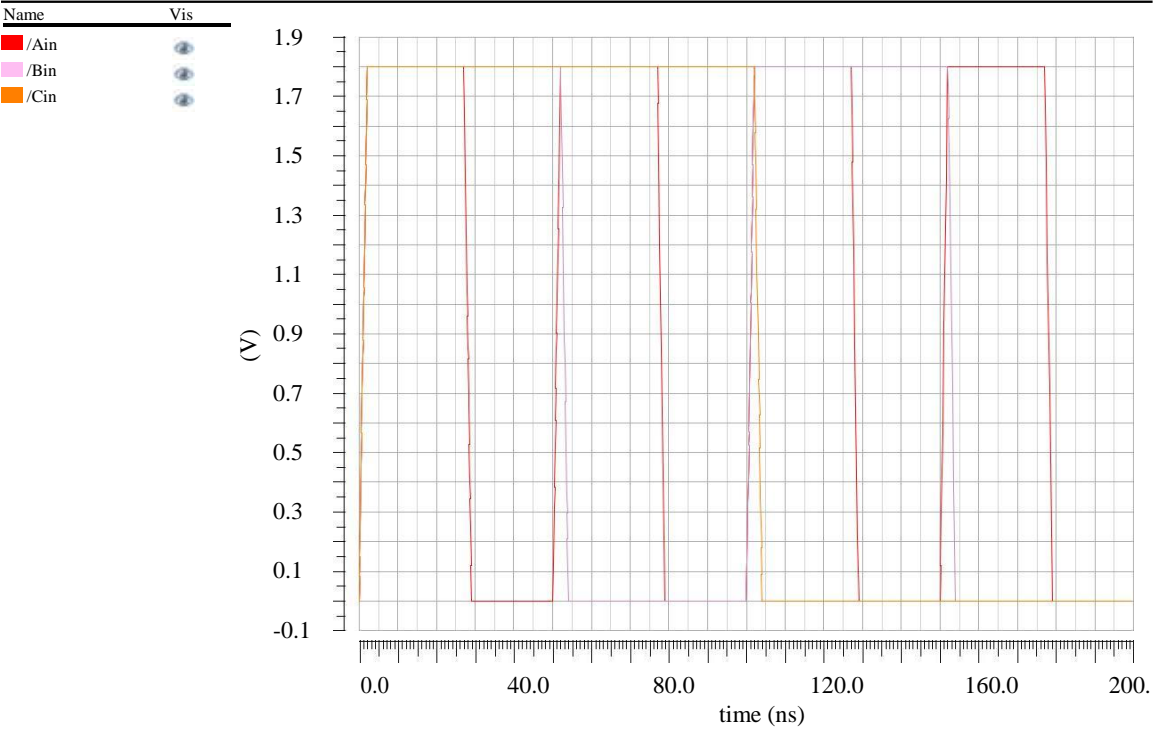


**Transient Analysis `tran': time = (0 s -> 200 ns)**
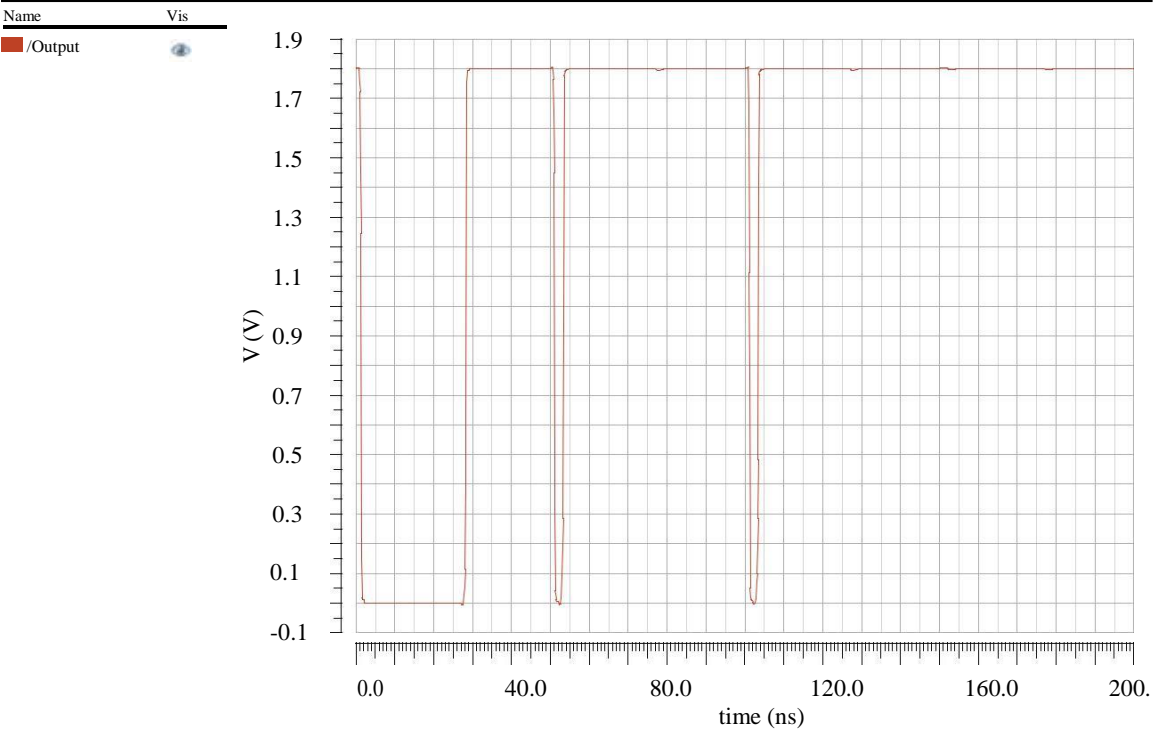
| Name | Vis |
|------|-----|
| /Output | |

**2 Input NOR gate**
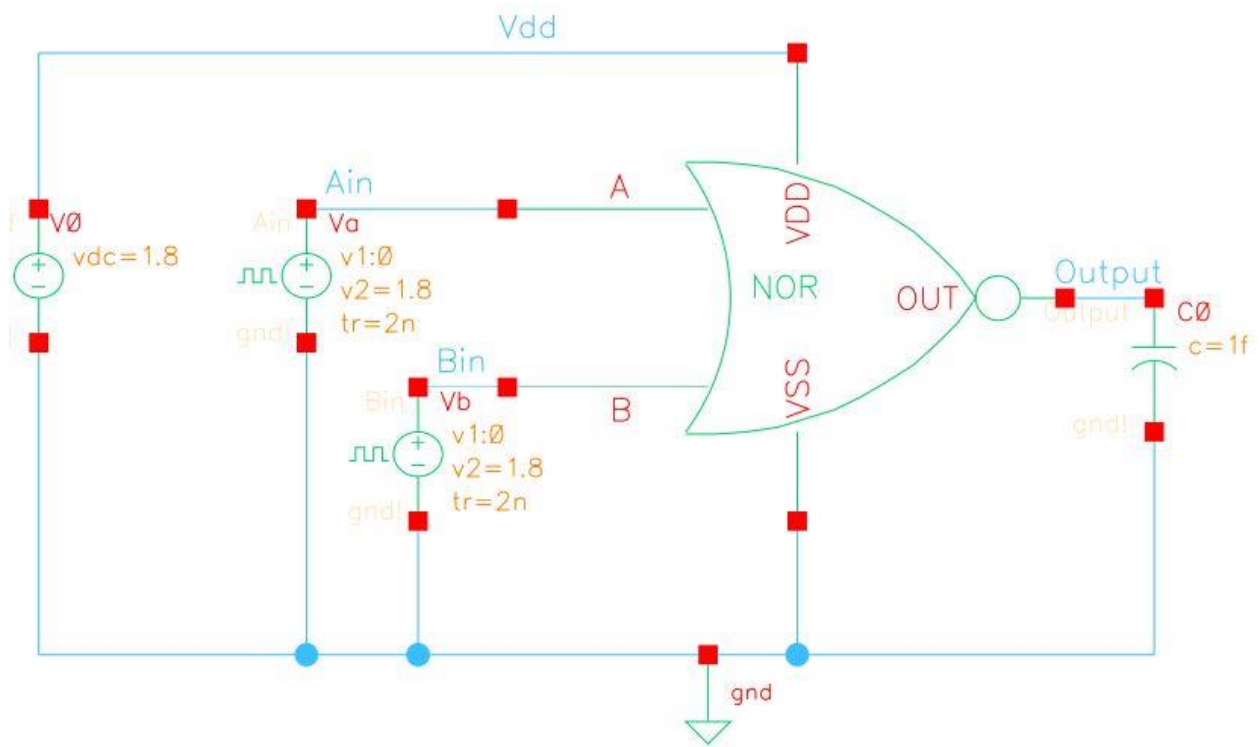**$(W/L)_n = (1.8/0.18)$**
**$(W/L)_p = (7.2/0.18)$**

Schematic (NOR)
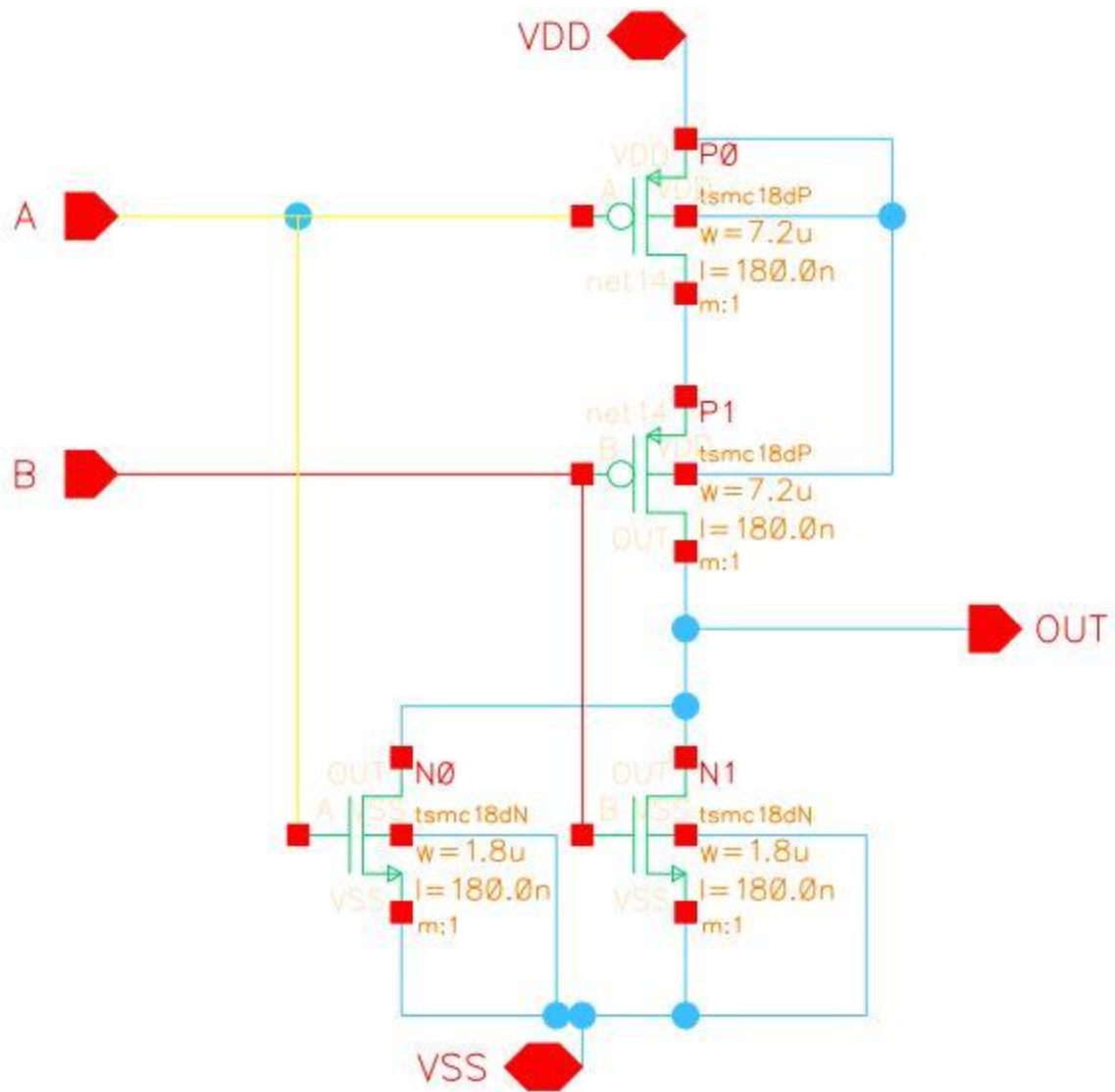
# Test-Bench (NOR)

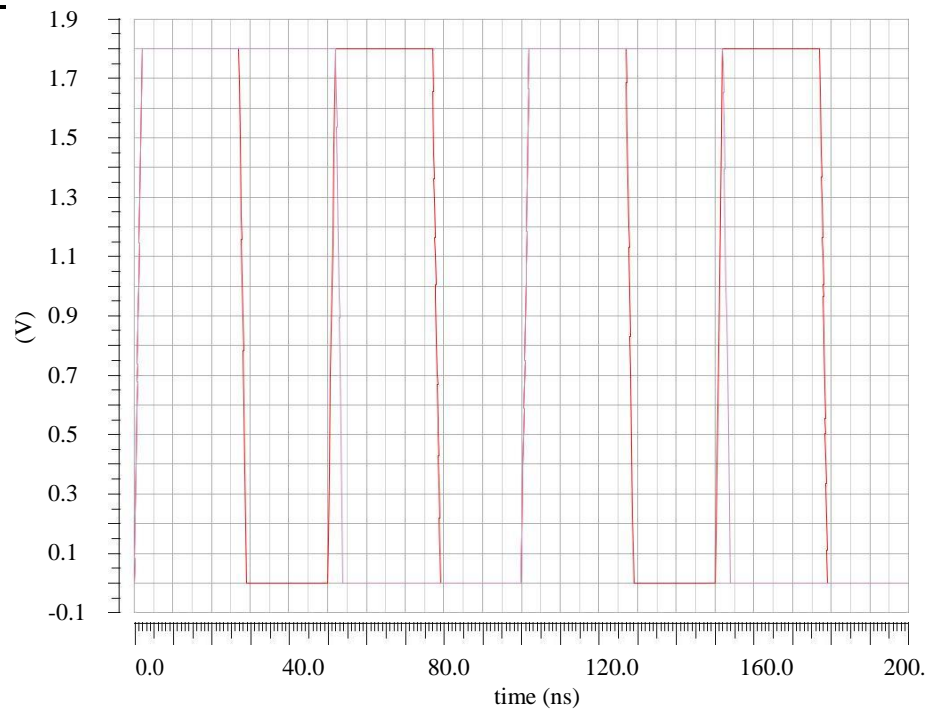# NOR test  Project1:NOR_2_tb:1 : Project1 NOR_2_tb schematic 19:34:19 Thu Mar 8 2018
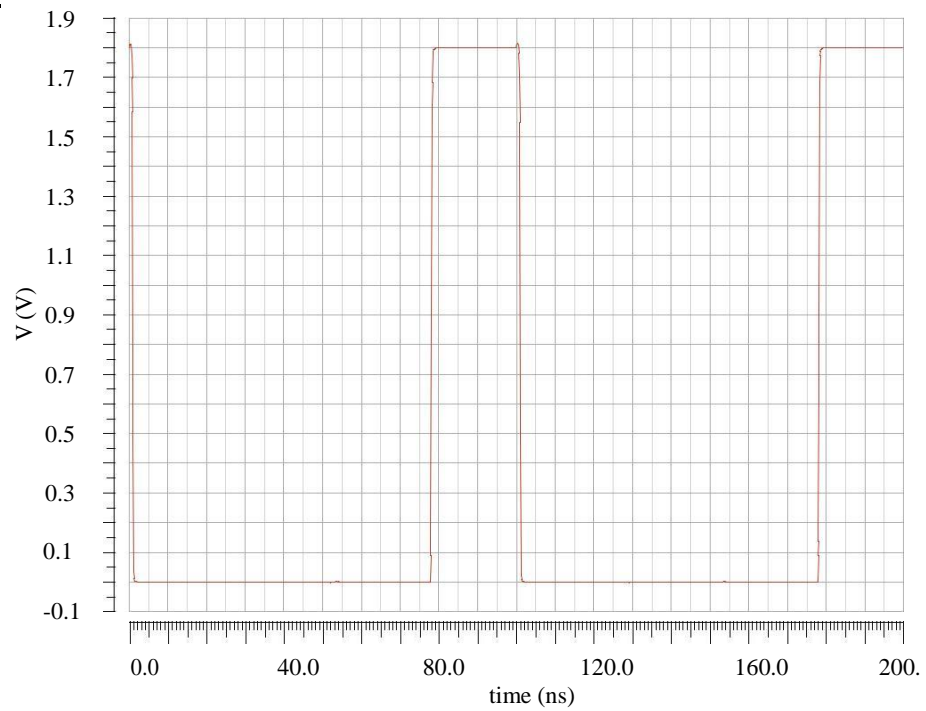
**Transient Response**                                                   **Thu Mar 8 19:32:57 2018**

| Name | Vis |
|------|-----|
| /Ain | |
| /Bin | |

(V)

time (ns)

**Transient Analysis `tran': time = (0 s -> 200 ns)**

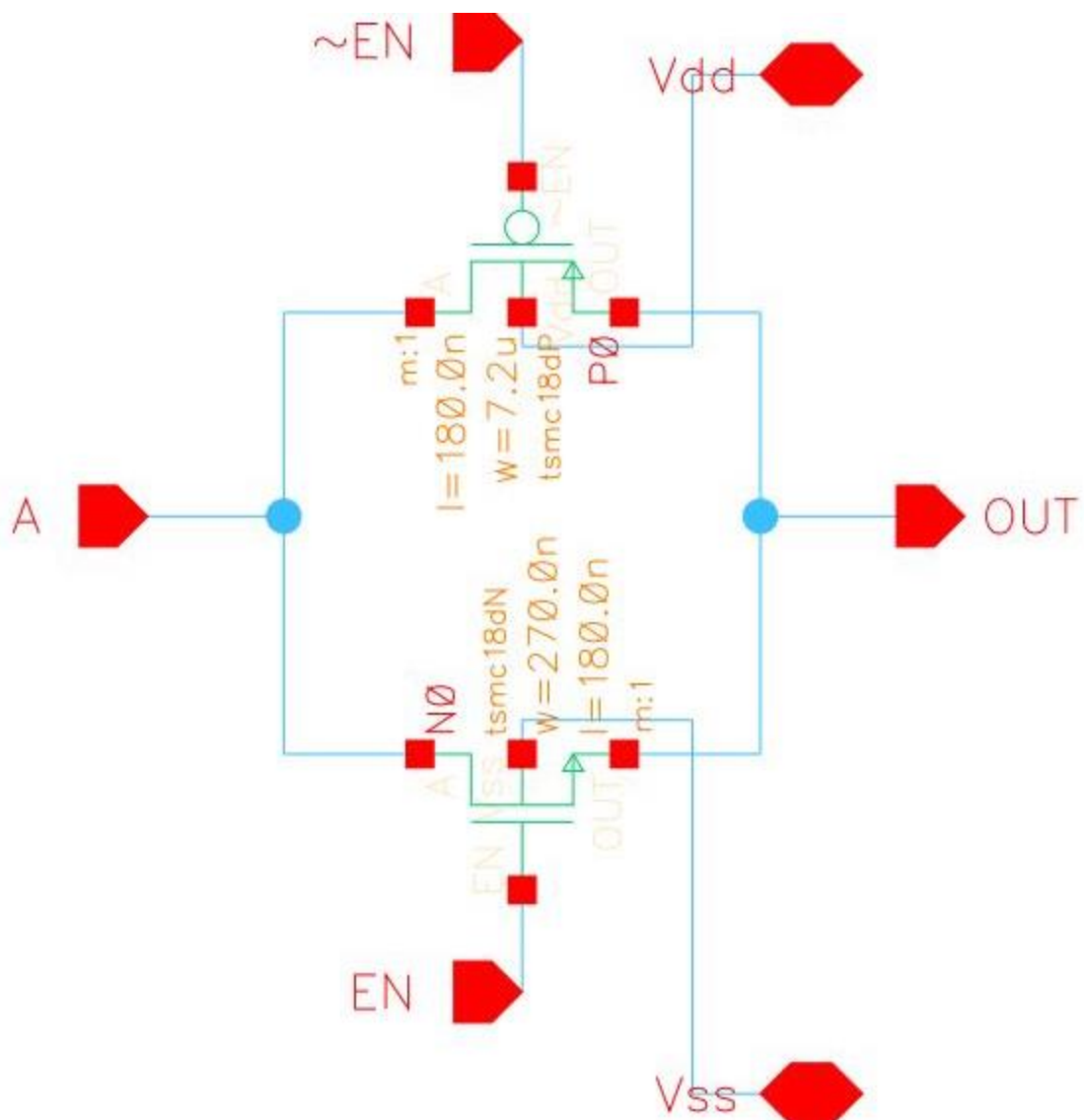| Name | Vis |
|------|-----|
| /Output | |

V (V)

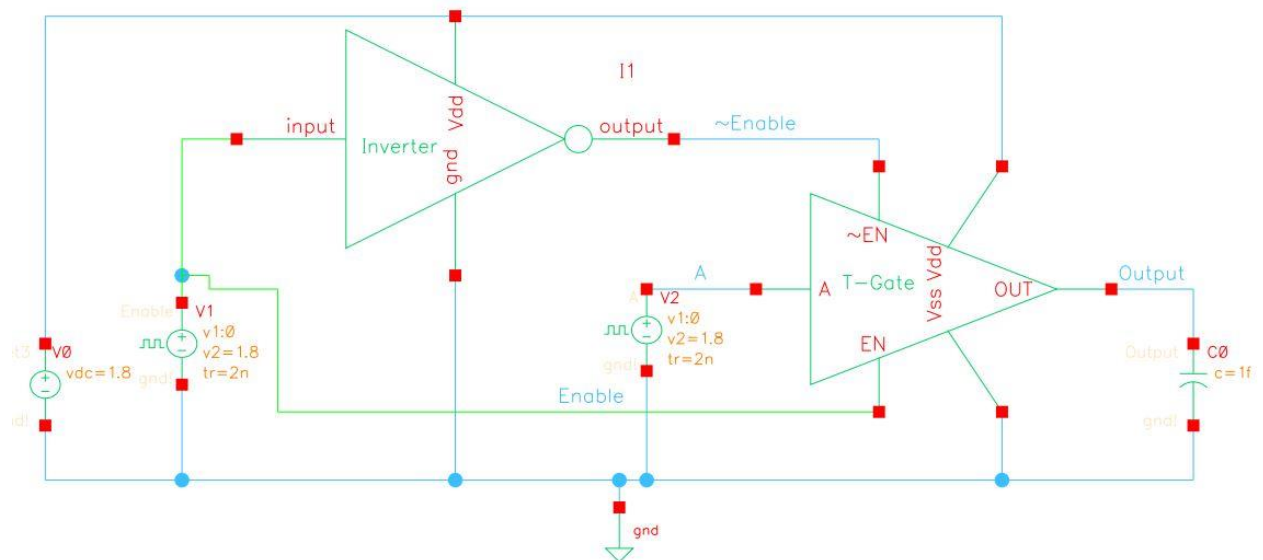time (ns)

**Transmission Gate**
**$(W/L)_n = (3.6/0.18)$**
**$(W/L)_p = (7.2/0.18)$**

Schematic (T-Gate)
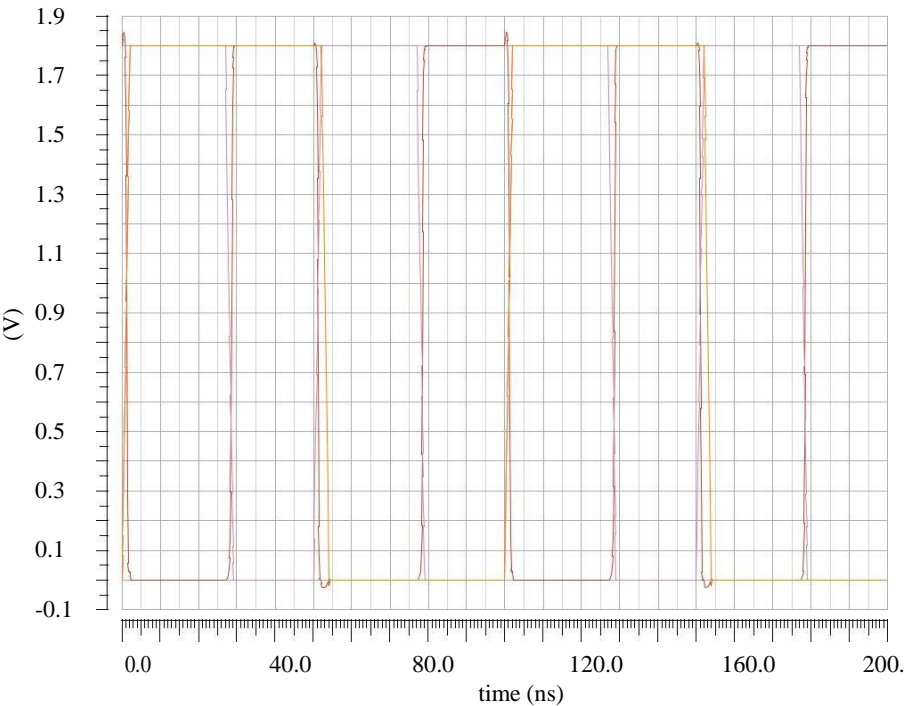
# Test-Bench (T-Gate)

# Transmission Gate Test
Project1:T_Gate_tb:1 : Project1 T_Gate_tb schematic 20:28:07 Thu Mar 8 2018
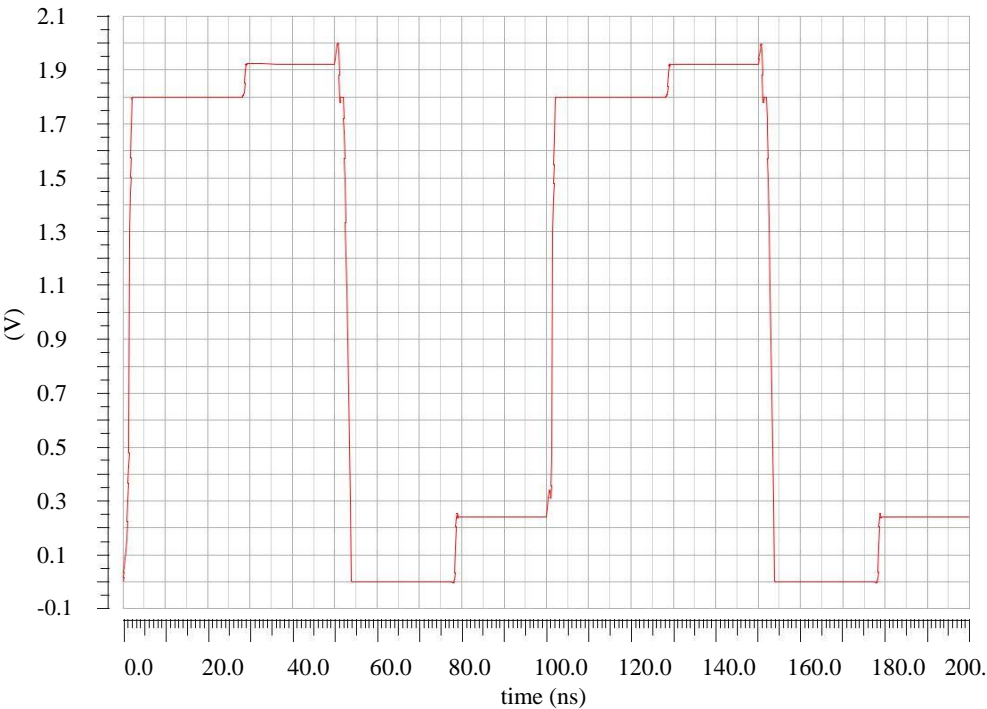
**Transient Response**                                   **Thu Mar 8 20:27:00 2018**
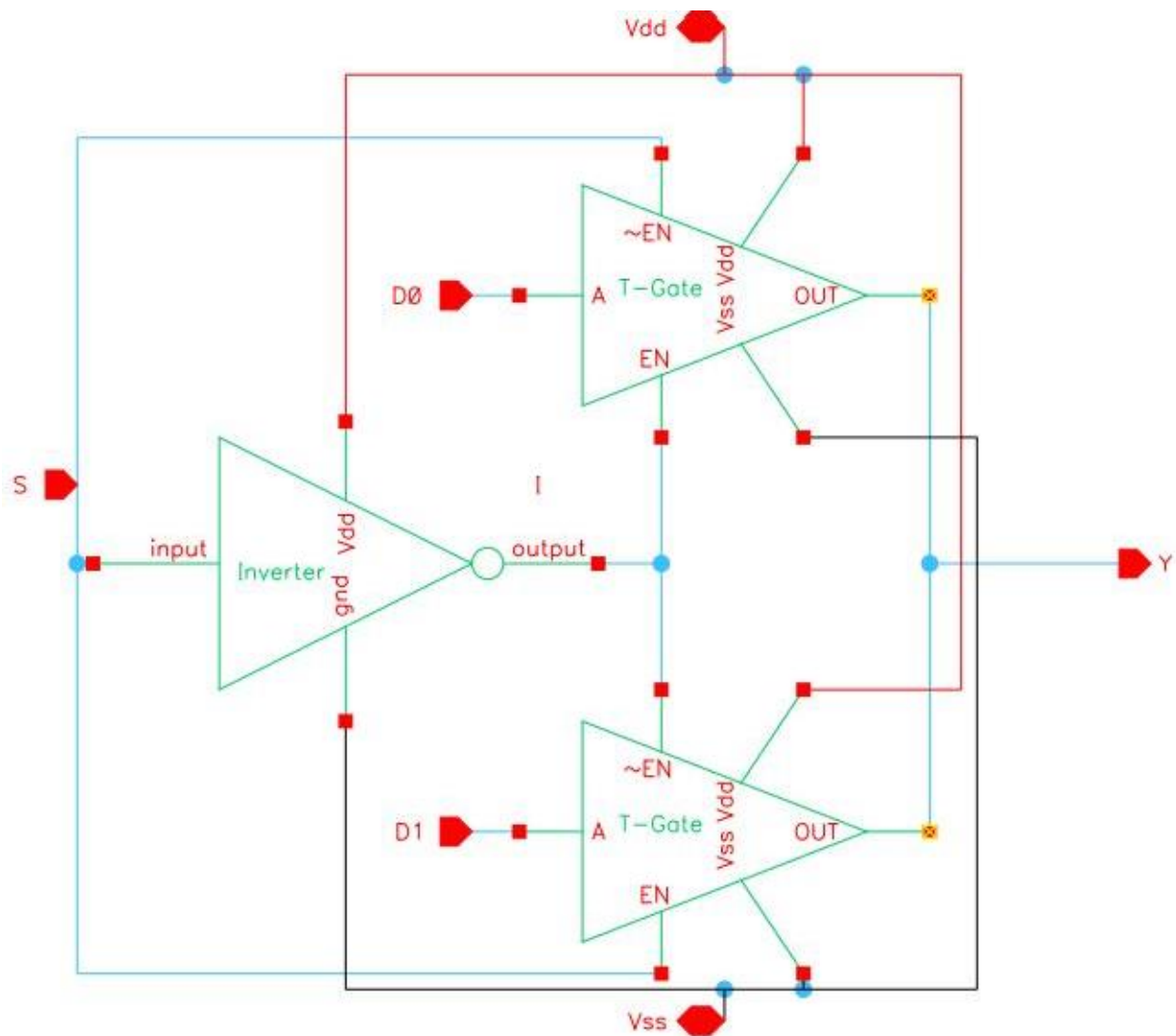
| Name | Vis |
|------|-----|
| /~Enable | |
| /Enable | |
| /A | |



**Transient Analysis `tran': time = (0 s -> 200 ns)**

| Name |
|------|
| /Output |

**2 – 1 MUX**
**Built out of**
**T-Gates**

Schematic (MUX)

# Test-Bench (MUX)

# MUX Test Project1:MUX2_1_tb:1 : Project1 MUX2_1_tb schematic 20:38:25 Thu Mar 8 2018
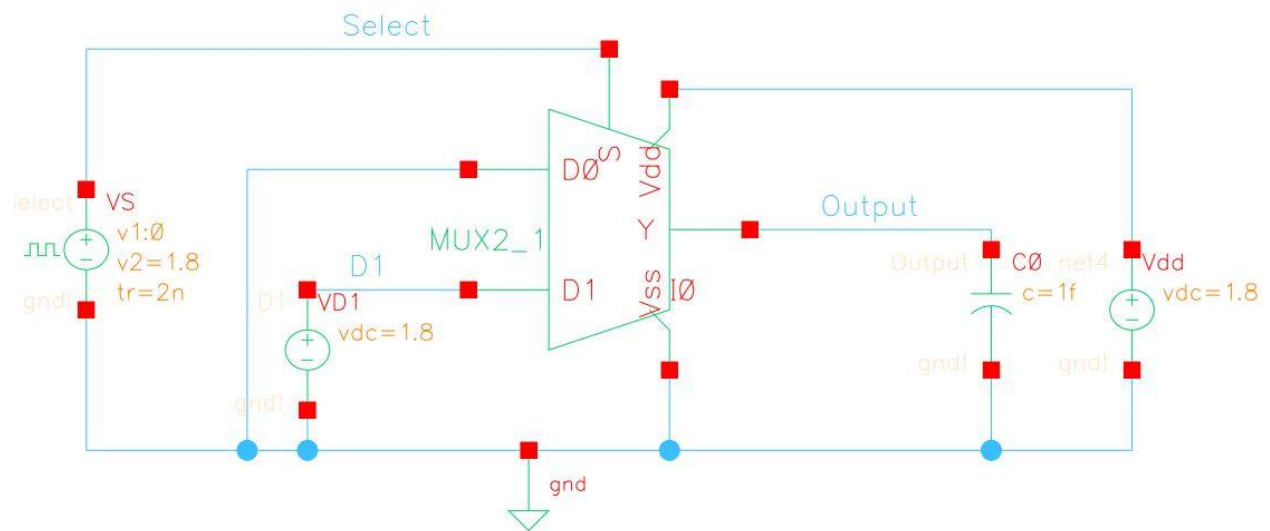
**Transient Response**                                        **Thu Mar 8 20:37:33 2018**

| Name | Vis |
|------|-----|
| /D1 | |
| /gnd! | |
| /Select | |



**Transient Analysis `tran': time = (0 s -> 200 ns)**

| Name | Vis |
|------|-----|
| /Output | |