Gold CMP Project
Part 5 – Final Technical Report
Assigned: April 13, 2016
Due: April 27, 2016, 5pm

Objective

The goal is to document your project-related activities in this course, especially capturing any steps where trade-off analyses were needed and the motivation for reaching the decision you made.

Team Policies

Continue working with your same teammate for this part of the project.

What to hand in?

Each team must prepare a short Formal Technical Report (no more than 10 pages for the main report, not including the appendix). For details of required documentation, refer to the next section. Please make sure that your report is well organized and can be easily followed by any technical reader. **Hardcopy** reports must be submitted at the beginning of the last regular class, April 27, 5pm.

Report Outline

- Introduction – introduce the report and describe the organization of the remaining sections.
- Approach/Overview – discuss how you approached each phase of the project, including tasks distribution among partners. For the Verilog coding and simulation of Parts 1 through 3, how did you partition the router, processor, and CMP design? It may be useful to show a block diagram here. Discuss your high-level approach for converting your RTL Verilog code you developed for Parts 1 through 3 to RTL that synthesized to an implementable design to achieve the Part 4 requirements.
- Trade-Offs/Choices – The purpose of this section is to demonstrate that you understand design issues and that your activity was based on sound reasoning. Describe the trade-offs and choices you made at various points in the project. What was the rationale for the modularization and hierarchy you used in your Verilog code? What was the rationale for the design of your testbenches? How confident were you that your testbenches verified the correct required functionality? Concerning Part 3, what additional testing did you perform beyond the required testbench, and what was the rationale for that testing? How confident are you that your CMP is fully functional according to the specification and would work for any assembly code or any message traffic pattern applied to the ring NoC? Concerning Part 4, what alternatives did you evaluate for attaining functioning synthesize-able code and what factors led you to choose the specific synthesizeable RTL you selected as final? What approach did you use for optimizing the area-delay product, and how do you know that your reported value is the optimal for your design? How many iterations of synthesis did you perform to attain this optimal design point? For all these discussions, include area, speed, design time considerations, etc., where it makes sense.
- Implementation – Were you able to complete all steps of the Part 4 assignment? Report any issues you encountered in implementing the design. Were you able to

perform simulation at each stage to prove your design is functional? Report the area of your synthesized design as reported from Synopsys Design Compiler. Also, report the area resulting from the Cadence Encounter place & route exercise. Based on these two areas, by what percentage did your design area increase once wiring was taken into account? (The area figures you report should be identical to what was reported in the summary reports of Part 4).

- Performance – Report the critical path delay of your design as reported by Synopsys PrimeTime. Also, report your area-delay product. (These values should be identical to that reported in the summary reports of Part 4.) Report the speed of your design as given at the end of the Cadence Encounter place & route step. Based on the post-synthesis speed and the post-p&r speed, by what percentage did wiring slow down the speed of your design?
- Conclusion – If you had more time, what would you change about your design? If you had to take power into consideration, what would you have done differently? What were the "lessons learned" from this project that you will use on future projects? What topics would you like to have seen covered in EE577b that were not covered this semester?
- Bibliography – List of references used for implementing your project or citations in this report
- Appendix – Include a copy of the following Part 4 summary reports: syn_summary.doc/pdf and ***pnrReport.txt***