Evaluation Board for the 1 MSPS 12-Bit Impedance Converter Network Analyzer

Preliminary Technical Data

EVAL-CN0217-EB1Z

FEATURES

Full-featured evaluation board for the AD5933
Graphic user interface software with frequency sweep capability for board control and data analysis
Various power supply linking options
Standalone capability with serial I²C loading from onboard Microcontroller
Selectable system clock options including Internal RC oscillator or on board 16 MHz crystal.

APPLICATIONS

Electrochemical analysis
Impedance spectroscopy
Complex impedance measurement
Corrosion monitoring and protection equipment
Biomedical and automotive sensors
Proximity sensing

GENERAL DESCRIPTION

This Application note describes the evaluation board for the AD5933 and the application software developed to interface to the device. The AD5933 is a high precision impedance converter system which combines an on board frequency generator with a 12-bit 1 MSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on board ADC, and the DFT is processed by an on board DSP engine at each excitation frequency. The AD5933 also contains an internal temperature sensor with 13-bit resolution. The part operates from a 2.7 V to 5.5 V supply. Other on board components include a ADR423 3.0 V reference to act as a stable supply voltages for the separate analog and a digital sections of the device and a ADP3303 ultrahigh precision regulator to act as a supply to the on board universal serial bus controller, which interfaces to the AD5933. The user has the option to power the entire circuitry from the USB port of a computer. The evaluation board also has a high performance trimmed 16 MHz surface-mount crystal to act as a system clock to the AD5933, if required. The various link options located around the evaluation board are explained in Table 1. Interfacing to the AD5933 is through a USB microcontroller, which generates the I²C signals necessary to communicate to the AD5933.The user interfaces to the USB microcontroller through a Visual Basic® graphic user interface located on and run from the user PC. More information on the AD5933 is available from Analog Devices at www.analog.com and should be consulted when using the evaluation board.

FUNCTIONAL BLOCK DIAGRAM

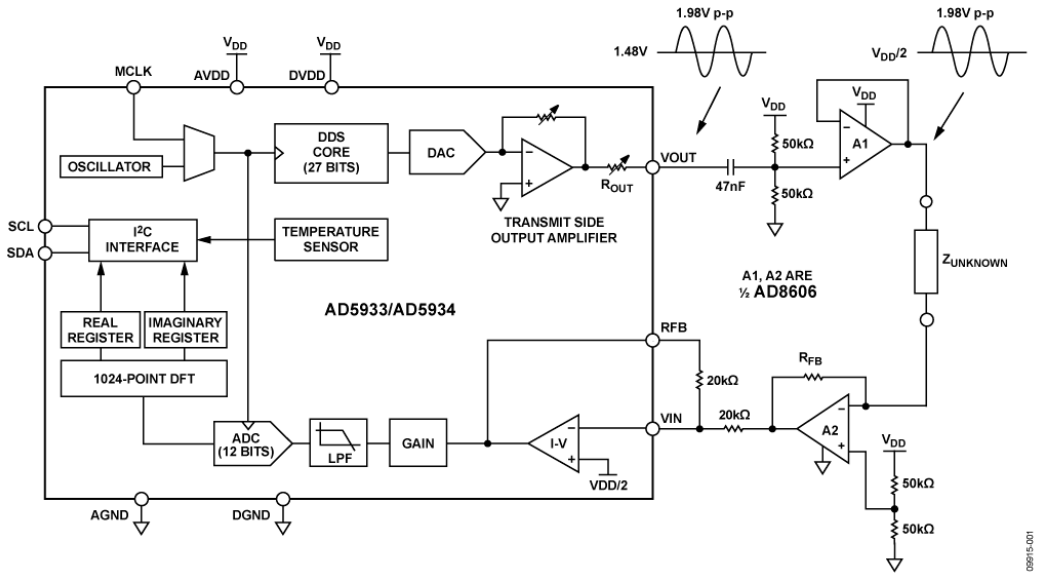

Figure 1.AD5933 Evaluation board block diagram

Rev. PrD

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REVISION HISTORY

5/08—Revision PrD

EVALUATION BOARD HARDWARE

TERMINAL BLOCK FUNCTIONS

LINK FUNCTIONS

Table 1.

Link No.	Default Location	Function
LK1	Out	Option to remove external conditioning
LK2	Out	Option to remove external conditioning
LK3	In	On-board16MHz Crystal Connection – connects toY2.
LK4	Out	SMB connected external clock.
LK5	In	Connects 5V from USB to ADP3303
LK6	A	AVDD & DVDD Power Supply Connector

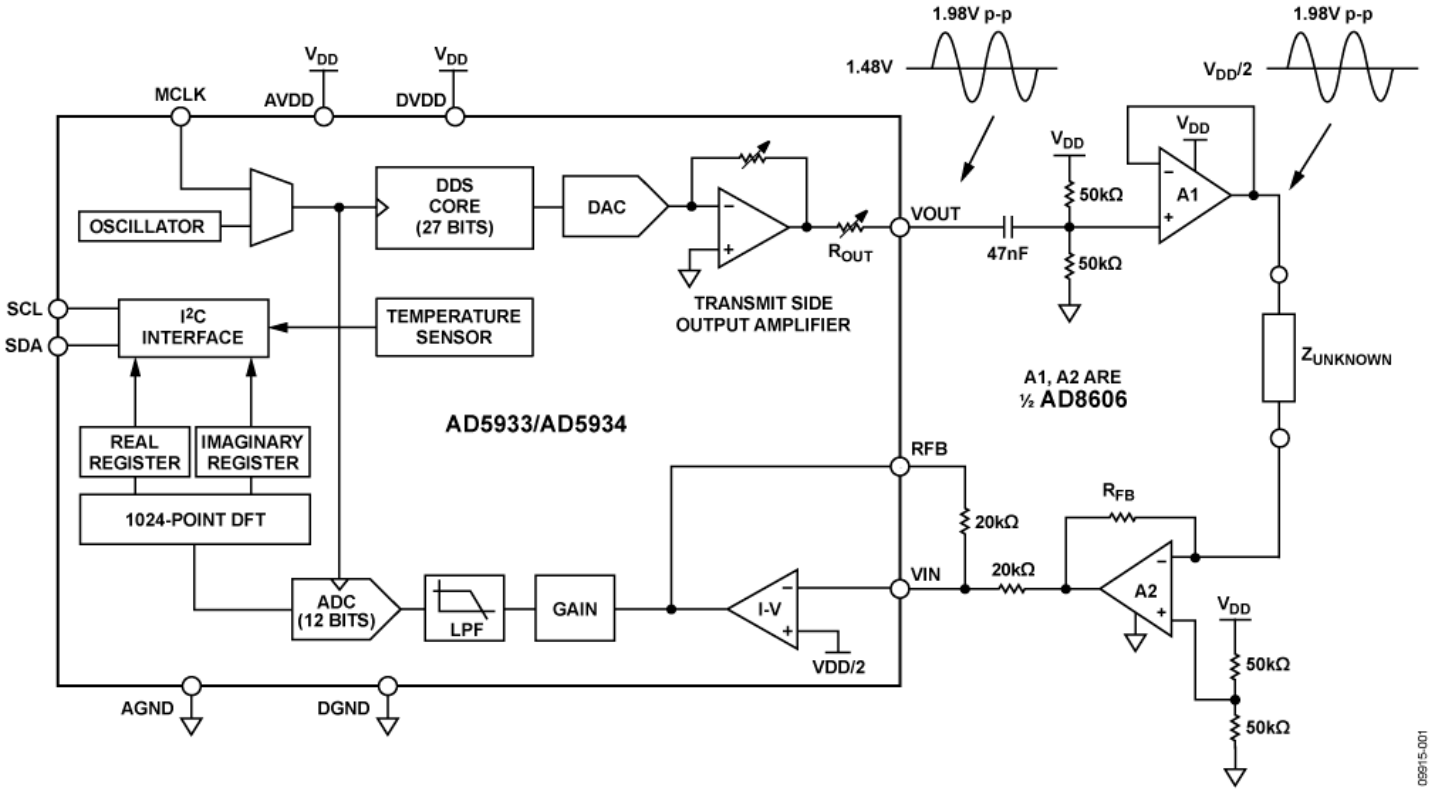


Figure 2. Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

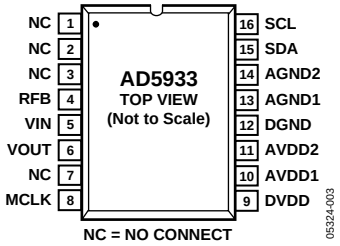


Figure 3. Pin Configuration

Table 2. Pin Connections for System

Pin No.	Mnemonic	Description/comment
1, 2, 3, 7	NC	No Connect.
4	RFB	External Feedback Resistor. Connected from Pin 4 to Pin 5 and used to set the gain of the current-to-voltage amplifier on the receive side.
5	VIN	Input to Receive Trans-impedance Amplifier. Presents a virtual earth voltage of VDD/2.
6	VOUT	Excitation Voltage Signal Output.
8	MCLK	Master Clock for the System. Supplied by user.
9	DVDD	Digital Supply Voltage.
10	AVDD1	Analog Supply Voltage 1.
11	AVDD2	Analog Supply Voltage 2.
12	DGND	Digital Ground.
13	AGND1	Analog Ground 1.
14	AGND2	Analog Ground 2.
15	SDA	I^2C Data Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.
16	SCL	I^2C Clock Input. Open-drain pins requiring 10 kΩ pull-up resistors to VDD.

It is recommended to tie all supply connections (Pins 9, 10, 11) and run from a single supply between 2.7 V and 5.5 V. Also, it is recommended to connect all ground signals together (Pins 12, 13, 14).

GETTING STARTED

SETUP SEQUENCE SUMMARY

This installation was carried out using the Windows XP® operating system with English (United States) settings. The regional and language settings of the computer can be changed in the **regional and language options** directory within the control panel (**start> control panel > regional and language options**). The installation consists of the following steps, which are described in detail in the sections that follow.

1. Install the AD5933 graphical user interface software on the compact disk (CD) which accompanies the evaluation board. Do not connect the USB cable from the AD5933 evaluation board to the computer USB hub until the evaluation software is properly installed. See Step 1—Install the Software.
2. Connect the computer USB port to the evaluation board using the USB cable provided in the evaluation kit, and run the USB hardware installation wizard after the evaluation software is correctly installed (the hardware installation may happen automatically depending upon the current operating system settings). See Step 2—Connect the USB Cable.
3. Ensure that the appropriate links are made through out the evaluation board. Power up the evaluation board appropriately prior to opening and running the evaluation software program. See Step 3—Verify the Links and Power Up.
4. Configure the evaluation board software front panel to run the required sweep function. See Step 4—Perform a Frequency Sweep.

STEP 1—INSTALL THE SOFTWARE

Place the CD accompanying the evaluation board into the CD drive of the user's computer and open the "**My Computer**" icon on the desktop. Double-click the CD disk drive icon. Go to **AD5933 Installation** > **Setup.exe** (Figure 4).

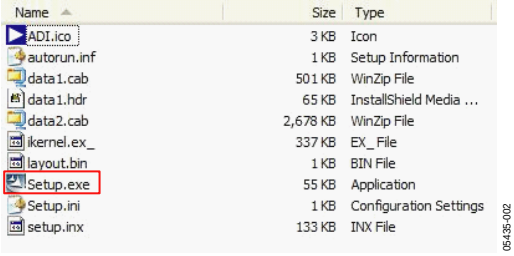


Figure 4.Evaluation Software CD contents

Double-click **Setup.exe** and install the software on the hard drive of your computer through the installation wizard (Figure 5). The CD software installation may happen automatically after the software CD is inserted into the disk drive; this may depend upon the current operating system settings.

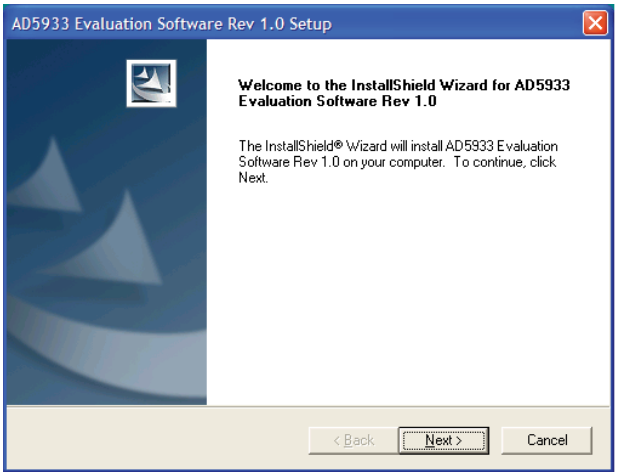


Figure 5. Installation wizard

It is recommended to install the software in the default destination folder path, **c\Program Files\Analog Devices\AD5933** (Figure 6).

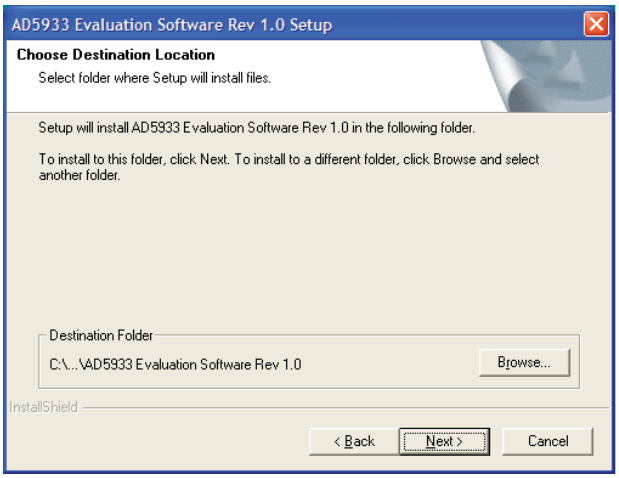


Figure 6.

Choose the **Analog Devices** directory (Figure 7). If the Analog Devices folder does not yet exist, create a folder called Analog Devices and add the program icon to this new folder.

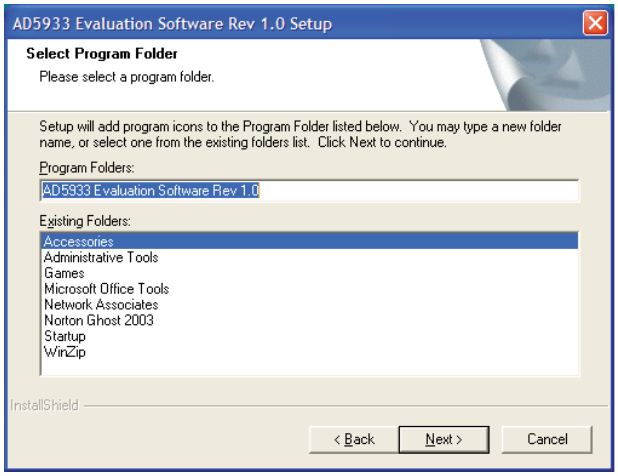


Figure 7.

After installing the software, remove the CD from the disk drive. You may be asked to re-booth the computer at this stage.

Go to **Start** > **All Programs** > **Analog Devices** > **AD5933** > **AD5933** (Figure 8).

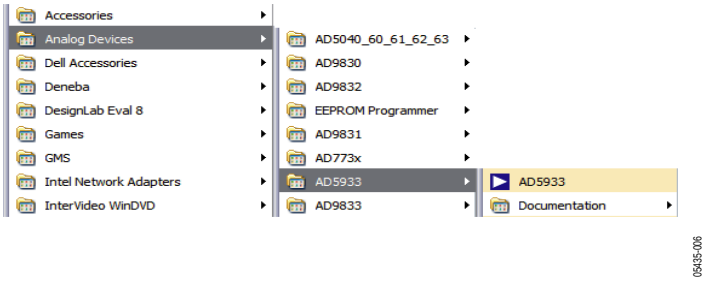


Figure 8. Opening the Evaluation software.

The following message will appear (see Figure 9) because the firmware code that the evaluation software operates from, and which needs to be downloaded to the evaluation board USB microcontroller memory each time the interface software program is opened, can not be successfully downloaded to the evaluation board. The error message will be presented because there is currently no USB connection between the computer and the AD5933 evaluation board at this stage, therefore this error message is to be expected. Click **Cancel** Proceed to Step 2.

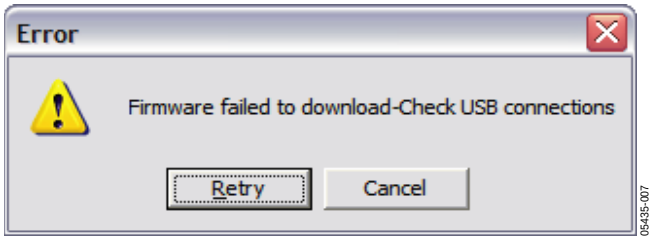


Figure 9.Expected error message.

STEP 2—CONNECT THE USB CABLE

Plug the USB cable into the computer USB hub and connect to the AD5933 evaluation board USB socket (see J1 in circuit schematic). A message may appear which will inform you that a USB device has been detected on the host computer and that new hardware has been found (Figure 10).

Figure 10.USB device detected by host computer

The **Found New Hardware Wizard** will then appear (Figure 11). This wizard locates and installs the appropriate driver files for the AD5933 evaluation kit in the operating system registry. Check the **Install the software automatically (Recommended)** option in the front panel presented **(see** Figure 11). Click **Next** to continue.

Figure 11. Hardware installation wizard.

A standard windows operating system warning message appears as shown in Figure 12. The indicates that the new hardware that is currently being installing on the windows operating system (AD5933 evaluation kit) has not passed the Windows logo testing to verify compatibility with Windows XP. This warning appears because the installation is an evaluation setup installation and is not intended to be used in a production environment. Click **Continue Anyway** and click **Finish**.

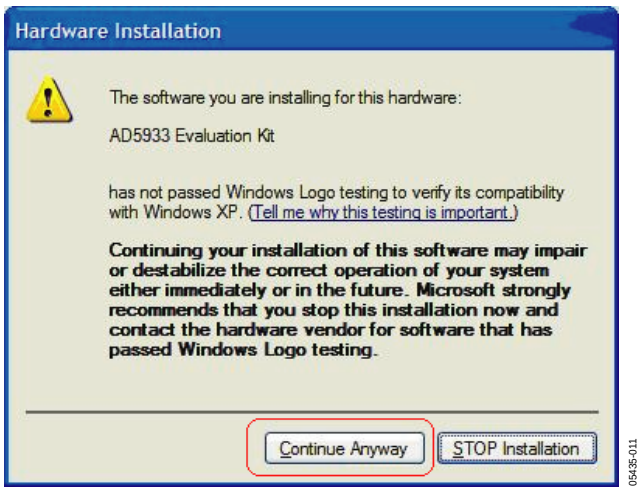


Figure 12.Expected warning message.

The message "**Found New Hardware Your new hardware is installed and ready to use "** appears as shown in Figure 13 once the hardware has been successfully installed.

Figure 13. Successfully Hardware Installation.

STEP 3—VERIFY THE LINKS AND POWER UP THE EVALUATION BOARD

Ensure that the relevant links are in place on the evaluation board (see Table 1 and **Error! Reference source not found.**) and that the proper power connections and supply values have been made to the terminal blocks before applying power to the evaluation board. The power supply terminal blocks are outlined in **Error! Reference source not found.**. Note that the USB connector will supply power only to the Cypress USB controller chip that interfaces to the AD5933. It does not act as a supply source to the AD5933 if links LK 4, 5, 10, 11, and 12 are removed. The user can provide a dedicated external voltage supply to each terminal block if required. The user must ensure that all relevant power supply connections and links are made before running the evaluation software. It is recommended that for optimum performance, the user should supply the three supply signals (A_{VDD1}, A_{VDD2} D_{VDD}) from a stable external reference supply via the power supply terminal blocks on the board as outlined in **Error! Reference source not found.**.

STEP 4—PERFORM A FREQUENCY SWEEP

The sequence for performing a linear frequency sweep across 200kΩ resistive impedance connected across the V_{OUT} and V_{IN} pins within the frequency range of 30 kHz to 30.2 kHz is outlined in this section. The default software settings for the evaluation board are shown in Figure 14 (note the user must connect a 200kΩ resistor across the Vin and Vout pins of the AD5933). The default link positions are outlined in **Error! Reference source not found.**, please read before continuing with step 4.

The sequence for opening the software is:

Go to **Start** > **Programs** > **Analog Devices** > **AD5933** and click **AD5933 Evaluation Software**.

When the graphic user interface program is opened and run successfully, it appears as shown in Figure 14. The figure shows the interface panel along with a frequency sweep impedance profile for a 200kΩ Resistive impedance (note RFB = 200kΩ).

This section describes how to set up a typical sweep across 200kΩ impedance (RFB = 200kΩ) using the installed AD5933 software. The theory of operation and the internal system architecture of the AD5933 device are described in detail in the AD5933 data sheet. This is available at www.analog.com and should be consulted when using the evaluation board.

Set the start frequency to 30000 (Hz) in the **Start Frequency** box (Arrow 1A). The start frequency is 24-bit accurate.

Set the frequency sweep step size to 2 (Hz) in the **Delta Frequency** box (Arrow 1A). The frequency step size is also 24-bit accurate.

To set the number of increments along the sweep to 200, enter **200** in the **Number Increments** box (Arrow 1A). 511 is the maximum number of increments that the device can sweep across. The value is stored in a register as a 9-bit value.

The delay between the time a frequency increment has taken place on the output of the internal DDS core and the time the ADC samples the response signal at this new frequency is determined by the contents of the **Number of settling time cycles** register (0x8Ah,0x8Bh) see the AD5933 datasheet for further details on the settling time cycle register. For example, if the user program's a value of 15 into the settling time cycles text box on the front panel and if the next output frequency is 32 kHz, the delay between the time the DDS core starts to output the 32 KHz signal and the time the ADC samples the response signal is 15 × (1/32 kHz) ≈468.7us. The maximum number of settling time cycles delay that can be programmed to the board is 511 cycles. The value is stored in a register as a 9-bit value. This value can be further multiplied by a factor of 2 or 4.

Enter **15** (cycles) in the **Number of Settling Time cycles** box (Arrow 1A).

[Aside]: If you are sweeping across a high Q structure such as resonant impedance, it is the responsibility of the user to ensure that the contents of the settling time cycles register is sufficient to ensure that the impedance under test settles before incrementing between each successive frequency in the programmed sweep. This is achieved by increasing the value within the **Number of Settling Time cycles** box.

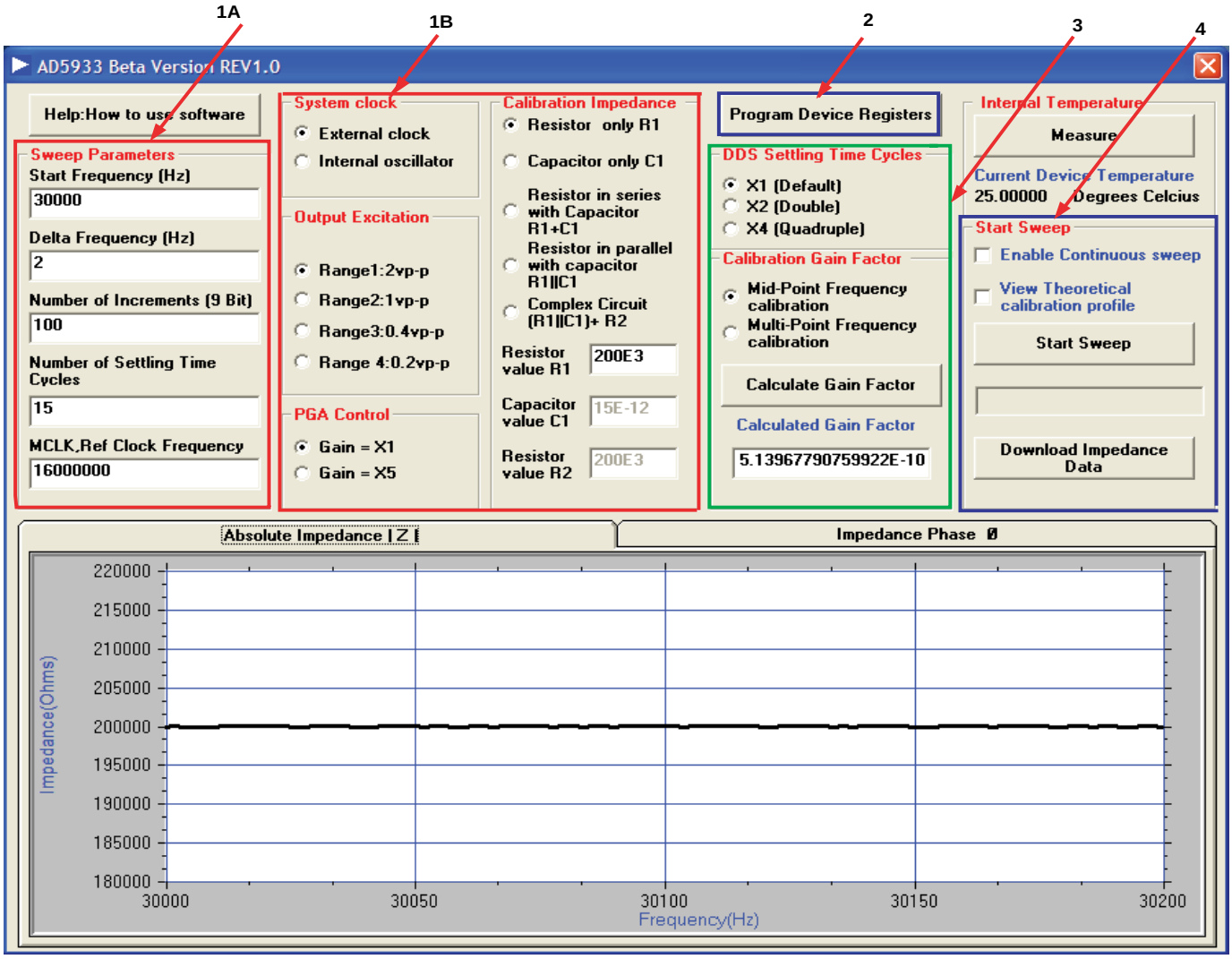


Figure 14. AD5933 Evaluation Software front panel. The impedance profile of a 200kΩ resistor is displayed.

Choose the external oscillator as the system clock. Check **External Oscillator** in the **System clock** panel (Arrow 1B).

Set the output excitation voltage range of the AD5933 at Pin 6 (Vout) to 2 V p-p (Arrow 1B). The four possible output ranges available are 2/1/0.4/0.2V p-p typically.

Set the **PGA** gain of the ADC on the receive stage (either ×1 or ×5) to **×1** (Arrow 1B).

Refer to the **Calibration Impedance** panel (Arrow 1B).Prior to making any measurements, the user must calibrate the AD5933 with a known (i.e. accurately measured) calibration impedance connected between the V_{IN} and V_{OUT} pins of the AD5933. The choice of calibration impedance topology (e.g. R1 in series with C1, R1 in parallel with C1 etc) depends upon the application in question. However the user **must** ensure that each component of the measured calibration impedance is entered correctly into each chosen topology component text box (See arrow 1B). For this example, we choose to calibrate with a **Resistor only** i.e. to measure the impedance of 200kΩ resistive impedance across frequency.

For this example, enter **200E3** (Ω) in the **Resistor Value** box.

To program the sweep parameters as chosen above into the appropriate onboard registers of the AD5933 through the I^2C interface, click **Program Registers** (Arrow 2).

The value programmed into the settling time cycles can be further multiplied by a factor of 2 or 4 for a sweep (Arrow 3A). Click the **×1** (default) button.

Now that the frequency sweep parameters and gain settings are programmed, the next step is to calibrate the AD5933 system by calculating the Gain Factor.

The explanation of the system calibration term called the "Gain Factor", a term calculated once at system calibration is provided in detail in the AD5933 data sheet. The AD5933 gain factor **must** be calibrated correctly for a **particular impedance** range before any subsequent valid impedance measurement (refer to AD5933 datasheet for further details).

The evaluation software will evaluate either a single mid point frequency gain factor or multi point frequency gain factors (i.e. a gain factor for each point in the programmed sweep) See Arrow 3. The mid point gain factor is determined at the mid point of the programmed sweep, the multi point gain factors are determined at each point in the programmed frequency sweep. The software will automatically calculate the gain factor(s) for the subsequent sweep once the **Calculate Gain Factor** button is pressed.

Once either the mid-point gain factor or the multipoint gain factors have been calculated, a message will be returned to the evaluation software front panel as show in Figure 15. The gain factor(s) returned to the evaluation software are subsequently used for the sweep across the impedance under test.

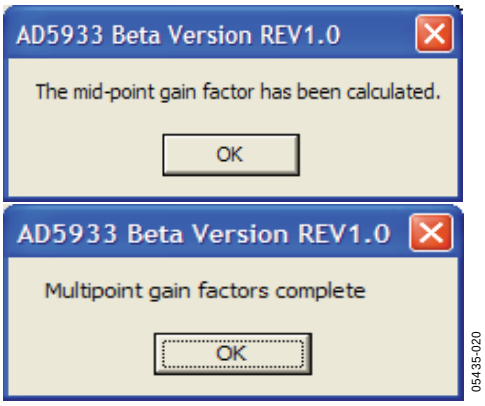


Figure 15.Confirmation of a mi-point calculation or a multipoint Gain Factors Calculation.

After the system interface software calculates the gain factor(s) for the programmed sweep parameters, it appears in the **calculated gain factor** box.

Important: Should the user change any of the system gain settings (e.g. change in output excitation range, PGA gain etc) after the system has been calibrated (i.e. gain factor(s) have been calculated) it will be necessary to recalculate the gain factor (s) in order to subsequently measure accurate impedance results. The gain factor(s) calculated in software are not programmed into the AD5933 RAM and are only valid when the evaluation software program is open and running. The gain factor(s) are not retained in the evaluation software once the software program is closed.

To begin the sweep, click **Start Sweep** (Arrow 4). Once the evaluation software completes the sweep it will automatically return both a plot of the impedance vs. frequency and phase vs. frequency for the impedance under test (see Figure 14).The progress of the sweep is outlined with a progress bar as show in Figure 16.

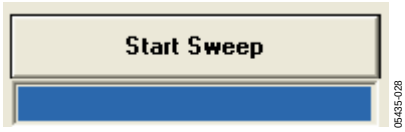


Figure 16.Sweep progress bar (blue)

To take a reading from the on board temperature sensor, click **Measure** in the internal temperature box of the front panel. This returns the 13-bit temperature of the device. See AD5933 data sheet for more information on the temperature sensor.

To download the frequency sweep data (i.e. frequency, impedance phase, real, imaginary and magnitude data) from the DFT of the sweep, click **Download Impedance Data**. The common dialog front panel will be presented as shown in Figure 17. Choose a file name in the directory of choice and click **Save File** (Figure 17) Note the file is saved in .CSV format.

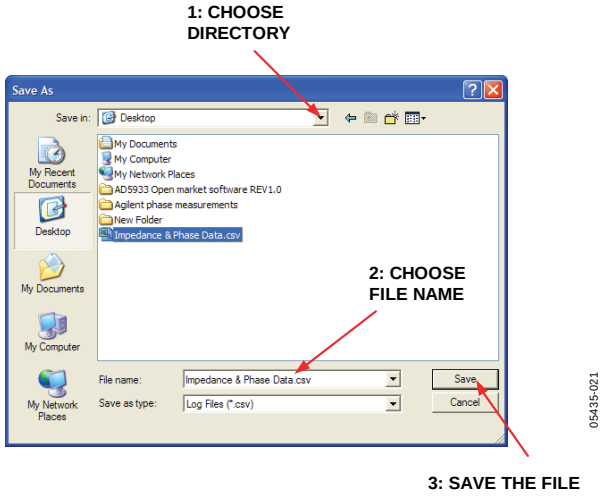
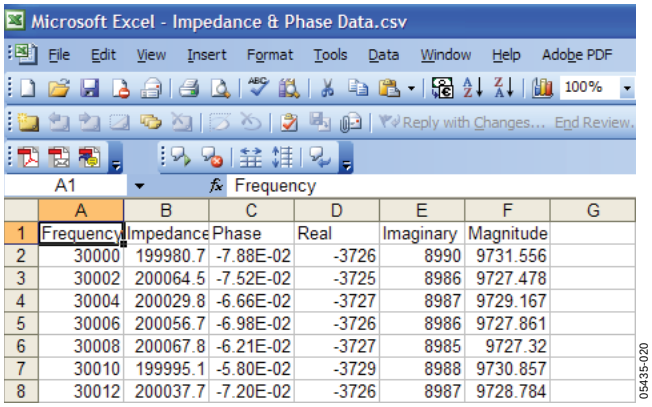


Figure 17. Saving the Sweep data

This saves the sweep data to comma separated variable file (.CSV) located in the directory of you choice.

You can access this file content by using Notepad or Microsoft Excel to plot the data. Each file contains a single column of data. The format of the downloaded data is shown in *Figure 18*



	A	B	C	D	E	F	G
1	Frequency	Impedance	Phase	Real	Imaginary	Magnitude	
2	30000	199980.7	-7.88E-02	-3726	8990	9731.556	
3	30002	200064.5	-7.52E-02	-3725	8986	9727.478	
4	30004	200029.8	-6.66E-02	-3727	8987	9729.167	
5	30006	200056.7	-6.98E-02	-3726	8986	9727.861	
6	30008	200067.8	-6.21E-02	-3727	8985	9727.32	
7	30010	199995.1	-5.80E-02	-3729	8988	9730.857	
8	30012	200037.7	-7.20E-02	-3726	8987	9728.784	

Figure 18. Opening the sweep data in excel.

Each data entry corresponds to a single measurement (frequency) point so, if you program 511 point as the value for the number of increments, the array contains a single column of data with 512 data points, starting at the start frequency and ending at stop frequency value, which is determined by

Start frequency + (*number of increments* × *delta frequency*)

The **impedance profile** and **phase profile** versus frequency appears in the evaluation software front panel after the sweep has completed. The user may switch between the impedance (|Z|) profile and phase (Ø) profile by clicking on the individual tabs. The absolute impedance |Z| tab shows how the impedance under analysis ($Z_{UNKNOWN}$) varies across the programmed frequency range. To view how the phase across the network under analysis varies, click the **Impedance phase Ø** tab as shown in *Figure 19* appears.

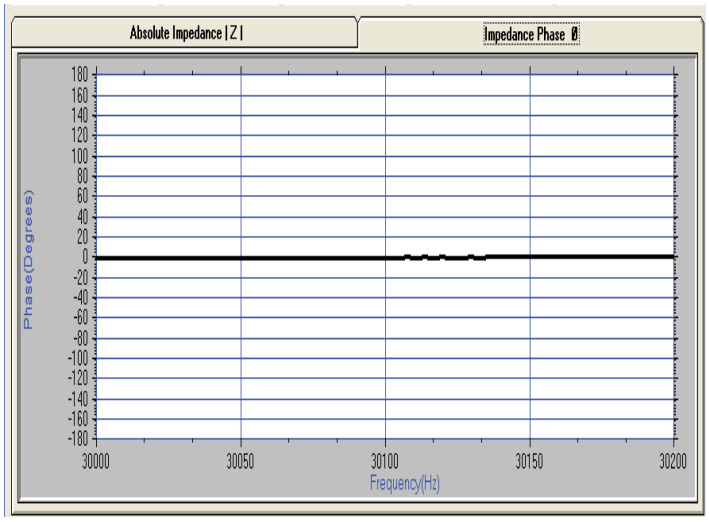


Figure 19.The Phase tab on the front panel. Phase of a 200KΩ resistor (0°) is displayed.

Note the phase measured by the AD5933 takes into account the phase introduced through the entire signal path, that is, the phase introduced through the output amplifiers, receive i-v amplifier and the low pass filter etc, along with the phase through the impedance ($Z_Ø$) under analysis connected between V_{OUT} and V_{IN} (Pin 6 and Pin 5 of the AD5933).The phase of the system needs to be calibrated out using a resistor before any subsequent impedance ($Z_Ø$) phase measurement can be calculated. The user will need to calibrate with a resistor in the evaluation software in order to calibrate the system phase correctly (refer to the section Impedance Measurement Tips. for further details)

INSTALLATION FREQUENTLY ASKED QUESTIONS

Q: How can I confirm that the hardware has been correctly installed in my computer?

A: Right-click **My Computer** and left-click **Properties**. On the **Hardware** tab, click **Device Manager**.

Figure 20.System Properties

Scroll to **Universal Serial Bus Controllers** and expand the directory root (Figure 21). When the AD5933 hardware is correctly installed, each time you plug the USB cable connecting the evaluation board to the computer, the items under the **Universal Serial Bus Controllers** root will be refreshed.

Figure 21 indicates what to expect when the AD5933 evaluation board is correctly installed and when the evaluation board and USB cable are connected correctly to the computer. The root directory is subsequently refreshed once the USB cable is unplugged from evaluation board and the AD5933 evaluation kit icon will be removed from the main root.

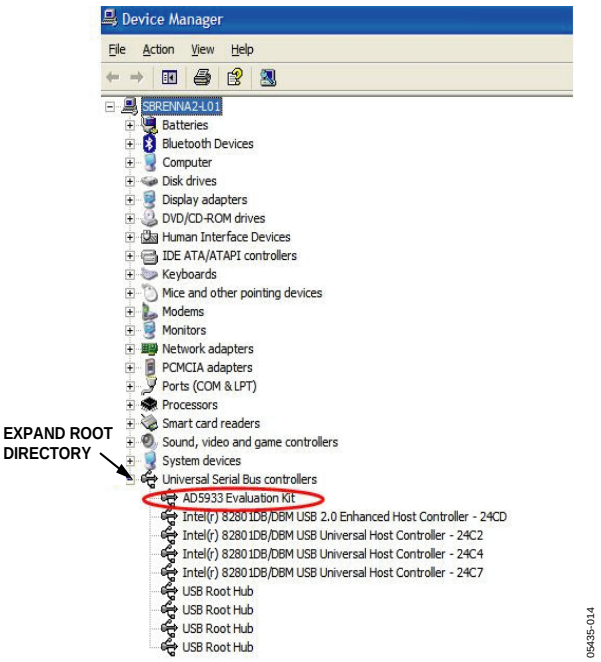


Figure 21 correctly installed hardware

Q: During the installation- when I plug in my board for the first time the following message (see Figure 22) appears.

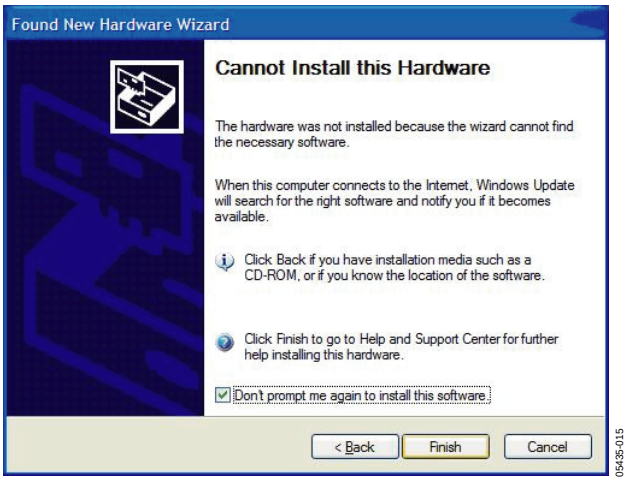


Figure 22.Error during the hardware installation

When I click **Finish**, the message in Figure 23 appears. What do I do next?

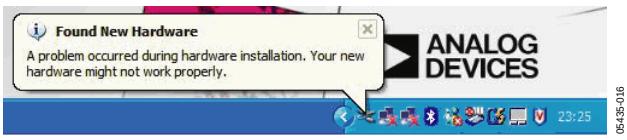


Figure 23.

A: Assuming that the evaluation software is installed correctly (you should have installed the software correctly prior to plugging in the board for the first time), this message simply indicates that the AD5933 device drivers have not been installed to the correct registry and so could not be correctly located by the install wizard. To re-install them, right-click **My Computer** and left-click **Properties**. On the **Hardware** tab, choose **Device Manager**. Expand **Other devices** (see Figure 24).

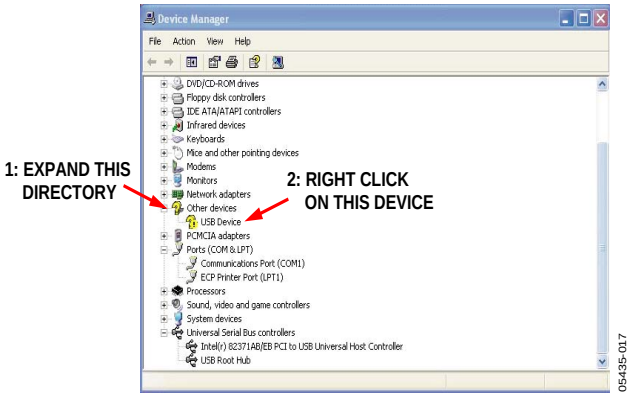


Figure 24.

The computer has not recognized the USB device, that is, the AD5933 evaluation board which is plugged in. Right-click **USB Device** and choose **Uninstall Driver**. Unplug the evaluation board and wait for approximately 30 seconds before plugging it in again. Proceed through the installation wizard a second time. A correct installation is indicated by the expanded root directory in Figure 25. If you encounter the same error message the second time, uninstall the device driver and uninstall the software and Contact the Analog Devices applications department for further instructions regarding valid driver files.

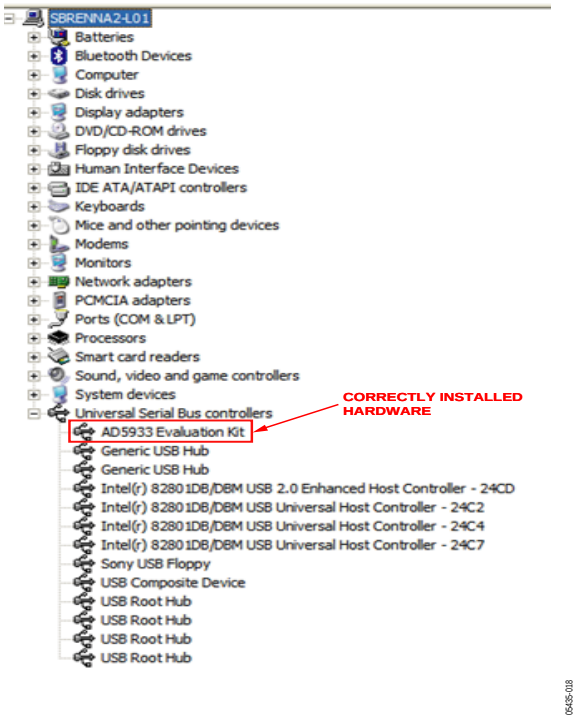


Figure 25. Correctly installed Hardware

SOURCE CODE FOR IMPEDANCE SWEEP

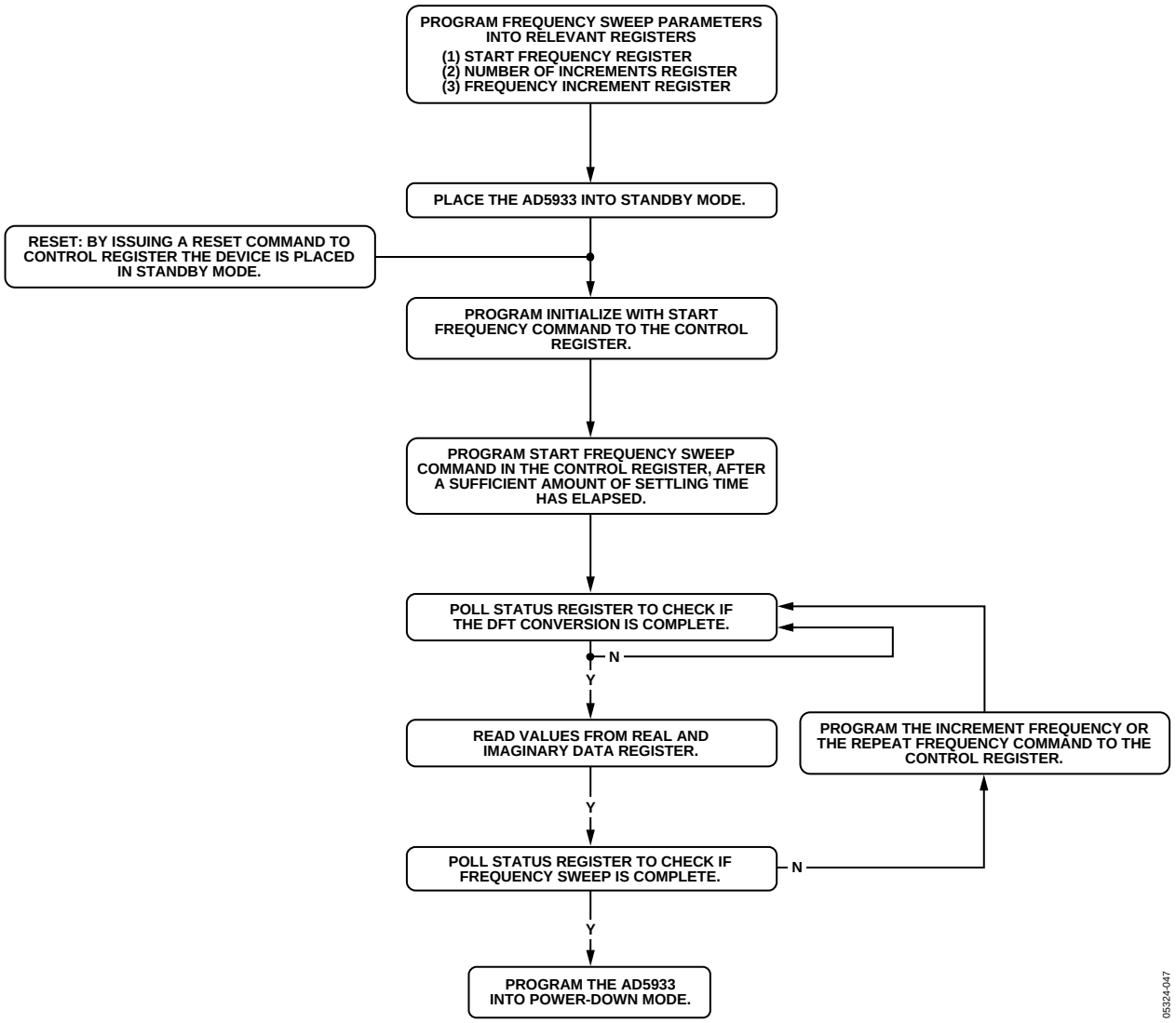


Figure 26. Sweep flow diagram

This section outlines the evaluation board code structure required to set up the AD5933 frequency sweep. The sweep flow outline is shown in Figure 26. Each section of the flow diagram will be explained with the help of the visual basic code extracts. The evaluation board source code (visual basic) is available upon request from the applications department of analog devices. The firmware code (c code), which is downloaded to the USB microcontroller connected to the AD5933, implements the low level i2c signal control (i.e. read and write vendor request).

The code extract, which is outlined below, shows how to program a single frequency sweep starting at 30K Hz, with a frequency step of 10 Hz and with 150 points in the sweep. The code assumes that a 16 MHz clock signal is connected to pin 8 (MCLK) of the AD5933 .The impedance range under test is from 90k ohm to 110k ohm The Gain Factor is calculated at the mid-point of the frequency sweep i.e. 30.750k Hz. The calibration is carried out with a 100k ohm resistor connected between Vout and Vin. The feedback resistor = 100k ohm.

The first step in Figure 26 is to program the three sweep parameters necessary to define the frequency sweep (i.e. the start frequency, the frequency step, and the number of frequency increments in the sweep).Refer to AD5933 datasheet for more details.

EVALUATION BOARD SOURCE CODE EXTRACT

```
'-------------------------------------------------------------------------------------------------------
'Code developed using visual basic® 6.
'Datatype   range
'Byte       0-255
'Double     -1.797e308 to – 4.94e-324 and 4.94e-324 to 1.7976e308
'Integer    -32,768 to 32767
'Long       -2,147,483,648 to 2,147,483,647
'Variant'...when storing numbers same range as double. When storing strings same range as string.
'------------------------------------ Variable Declarations ----------------------------------------
Dim ReadbackStatusRegister As Long   'stores the contents of the status register.
Dim RealData As Double               'used to store the 16 bit 2s complement real data.
Dim RealDataUpper As Long            'used to store the upper byte of the real data.
Dim RealDataLower As Long            'used to store the lower byte of the real data.
Dim ImagineryData As Double          'used to store the 16 bit 2s complement real data.
Dim ImagineryDataLower As Long       'used to store the upper byte of the imaginary data.
Dim ImagineryDataUpper As Long       'used to store the lower byte of the imaginary data.
Dim Magnitude As Double              'used to store the sqrt (real^2+imaginary^2).
Dim Impedance As Double              'used to store the calculated impedance.
Dim MaxMagnitude As Double           'used to store the max impedance for the y axis plot.
Dim MinMagnitude As Double           'used to store the min impedance for the y axis plot.
Dim sweep_phase As Double            'used to temporarily store the phase of each sweep point.
Dim Frequency As Double              'used to temporarily store the current sweep frequency.
Dim Increment As Long                'used as a temporary counter
Dim i As Integer                     'used as a temporary counter in (max/min) mag,phase loop
Dim xy As Variant                    'used in the stripx profile
Dim varray As Variant
Dim Gainfactor as double            'either a single mid point calibration or an array of calibration points
Dim TempStartFrequency     As Double
Dim StartFrequencybyte0    As Long
Dim StartFrequencybyte2    As Long
Dim StartFrequencybyte1A   As Long
Dim StartFrequencybyte1B   As Long
Dim DDSRefClockFrequency   As Double
Dim NumberIncrementsbyte0  As Long
Dim NumberIncrementsbyte1  As Long
Dim FrequencyIncrementbyt0 As Long
Dim FrequencyIncrementbyt1 As Long
Dim FrequencyIncrementbyt2 As Long
Dim SettlingTimebyte0      As Long
Dim SettlingTimebyte1      As Long
'------------------------------------ I^2C read/write definitions----------------------------------------
'used in the main sweep routine to read and write to AD5933.This is the vendor request routines in the
firmware

Private Sub WritetToPart(RegisterAddress As Long, RegisterData As Long)
PortWrite &HD, RegisterAddress, RegisterData
'parameters = device address register address register data
End Sub

Public Function PortWrite(DeviceAddress As Long, AddrPtr As Long, DataOut As Long) As Integer
PortWrite = VendorRequest(VRSMBus, DeviceAddress, CLng(256 * DataOut + AddrPtr), VRWRITE, 0, 0)
End Function

Public Function PortRead(DeviceAddress As Long, AddrPtr As Long) As Integer
PortRead = VendorRequest(VRSMBus, DeviceAddress, AddrPtr, VRREAD, 1, DataBuffer(0))
PortRead = DataBuffer(0)
End Function

'------------------------------------ PHASE CONVERSION FUNCTION DEFINITION -------------------------------
'This function accepts the real and imaginary data(R, I) at each measurement sweep point and converts it to
a degree
'-------------------------------------------------------------------------------------------------------
Public Function phase_sweep (ByVal img As Double, ByVal real As Double) As Double

Dim theta As Double
  Dim pi As Double
  pi = 3.141592654
```

```
  If ((real > 0) And (img > 0)) Then
     theta = Atn(img / real)             ' theta = arctan (imaginary part/real part)
     phase2 = (theta * 180) / pi              'convert from radians to degrees

ElseIf ((real > 0) And (img < 0)) Then
      theta = Atn(img / real)                 '4th quadrant theta = minus angle
      phase2 = ((theta * 180) / pi ) +360

ElseIf ((real < 0) And (img < 0)) Then
      theta = -pi + Atn(img / real)           '3rd quadrant theta img/real is positive
      phase2 = (theta * 180) / pi

ElseIf ((real < 0) And (img > 0)) Then
      theta = pi + Atn(img / real)            '2nd quadrant img/real is neg
      phase2 = (theta * 180) / pi

End If

End Function
‘-------------------------------------------------------------------------------------------------------------

Private Sub Sweep ()
’ the main sweep routine

‘This routine coordinates a frequency sweep using a mid point gain factor (see datasheet).
'The gain factor at the mid-point is determined from the real and imaginary contents returned at this mid
‘point frequency and the calibration impedance.
'The bits of the status register are polled to determine when valid data is available and when the sweep is
‘complete.
'-------------------------------------------------------------------------------------------------------------
IndexArray = 0                   'initialize counter variable.
Increment = NumberIncrements + 1 'number of increments in the sweep.
Frequency = StartFrequency       'the sweep starts from here.

‘------------------------- PROGRAM 30K Hz to the START FREQUENCY register --------------------------------

DDSRefClockFrequency = 16E6               ‘Assuming a 16M Hz clock connected to MCLK
StartFrequency = 30E3                     ‘frequency sweep starts at 30K Hz

TempStartFrequency = (StartFrequency / (DDSRefClockFrequency / 4)) * 2^27 ‘dial up code for the DDS
TempStartFrequency = Int(TempStartFrequency)  ‘30K Hz = 0F5C28 hex

StartFrequencybyte0 = 40     ‘40 DECIMAL = 28 HEX
StartFrequencybyte1 = 92     ‘92 DECIMAL = 5C HEX
StartFrequencybyte2 = 15     ’15 DECIMAL = 0F HEX

'Write in data to Start frequency register
WritetToPart &H84, StartFrequencybyte0   '84 hex lsb
WritetToPart &H83, StartFrequencybyte1   '83 hex
WritetToPart &H82, StartFrequencybyte2   '82 hex
‘-------------------------------- PROGRAM the NUMBER OF INCREMENTS register -----------------------------
‘The sweep is going to have 150 points 150 DECIMAL = 96 hex
'Write in data to Number Increments register
WritetToPart &H89, 96     ‘lsb
WritetToPart &H88, 00     ‘msb
 ‘-------------------------------- PROGRAM the FREQUENCY INCREMENT register -----------------------------
‘The sweep is going to have a frequency increment of 10Hz between successive points in the sweep

DDSRefClockFrequency = 16E6               ‘Assuming a 16M Hz clock connected to MCLK
FrequencyIncrements = 10                 ‘frequency increment of 10Hz

TempStartFrequency = (FrequencyIncrements / (DDSRefClockFrequency / 4)) * 2^27 ‘dial up code for the DDS
TempStartFrequency = Int(TempStartFrequency)  ’10 Hz =  335 decimal = 00014F hex

FrequencyIncrementbyt0 = 4F     ‘335 decimal = 14f hex
FrequencyIncrementbyt1 = 01
FrequencyIncrementbyt2 = 00

'Write in data to frequency increment register
WritetToPart &H87, FrequencyIncrementbyt0   '87 hex lsb
WritetToPart &H86, FrequencyIncrementbyt1   '86 hex
WritetToPart &H85, FrequencyIncrementbyt2   '85 hex msb
```

```
 ‘-------------------------------- PROGRAM the SETTLING TIME CYCLES register -----------------------------
‘The DDS is going to output 15 cycles of the output excitation voltage before the ADC will start sampling
‘the response signal. The settling time cycle multiplier is set to x1

SettlingTimebyte0 = 0F ‘15 cycles (decimal) = 0F hex
SettlingTimebyte1 = 00 ’00 = X1

WritetToPart &H8B, SettlingTimebyte0
WritetToPart &H8A, SettlingTimebyte1


‘------------------------------------- PLACE AD5933 IN STANDBYMODE ---------------------------------------

‘Standby mode command = B0 hex
 WritetToPart &H80, &HB0

'------------------------ Program the system clock and output excitation range and PGA setting-----------
‘Enable external Oscillator
WritetToControlRegister2 &H81, &H8
‘Set the output excitation range to be 2vp-p and the PGA setting to = x1
WritetToControlRegister2 &H80, &H1

‘-----------------------------------------------------------------------------------------------------------
‘------------- ------------ Initialize impedance under test with start frequency --------------------------
'Initialize Sensor with Start Frequency
 WritetToControlRegister &H80, &H10

msDelay 2  'this is a user determined delay dependant upon the network under analysis (2ms delay)

‘------------------------------------ Start the frequency sweep ----------------------------------------
'Start Frequency Sweep
WritetToControlRegister &H80, &H20

'Enter Frequency Sweep Loop

ReadbackStatusRegister = PortRead(&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H4 ' mask off bit D2 (i.e. is the sweep complete)

Do While ((ReadbackStatusRegister <> 4) And (Increment <> 0))
'check to see if current sweep point complete

ReadbackStatusRegister = PortRead(&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H2
'mask off bit D1 (valid real and imaginary data available)
                ’-------------------------------------------------------------------------
                If (ReadbackStatusRegister = 2) Then
                ' this sweep point has returned valid data so we can proceed with sweep
                Else
                Do
          ‘if valid data has not been returned then we need to pole stat reg until such time as valid data
          'has been returned
         ‘i.e. if point is not complete then Repeat sweep point and pole staus reg until valid data returned
                WritetToControlRegister &H80, &H40 'repeat sweep point
                       Do
                ReadbackStatusRegister = PortRead(&HD, &H8F)
                ReadbackStatusRegister = ReadbackStatusRegister And &H2
                ' mask off bit D1- Wait until dft complete
                       Loop While (ReadbackStatusRegister <> 2)

                Loop Until (ReadbackStatusRegister = 2)
                End If
                '-------------------------------------------------------------------------

                RealDataUpper = PortRead(&HD, &H94)
                RealDataLower = PortRead(&HD, &H95)
                RealData = RealDataLower + (RealDataUpper * 256)
                'The Real data is stored in a 16 bit 2's complement format.
                'In order to use this data it must be converted from 2's complement to decimal format
                If RealData <= &H7FFF Then  ' h7fff 32767
                ' Positive
                Else
```

```
                ' Negative
'                RealData = RealData And &H7FFF
                RealData = RealData - 65536
                End If
                ImagineryDataUpper = PortRead(&HD, &H96)
                ImagineryDataLower = PortRead(&HD, &H97)
                ImagineryData = ImagineryDataLower + (ImagineryDataUpper * 256)
                'The imaginary data is stored in a 16 bit 2's complement format.
                'In order to use this data it must be converted from 2's complement to decimal format
                If ImagineryData <= &H7FFF Then
                ' Positive Data.
                Else
                ' Negative
'                ImagineryData = ImagineryData And &H7FFF
                ImagineryData = ImagineryData - 65536
                End If

‘-----------------Calculate the Impedance and Phase of the data at this frequency sweep point -----------
                Magnitude = ((RealData ^ 2) + (ImagineryData ^ 2)) ^ 0.5
                'the next section calculates the phase of the dft real and imaginary components
                ‘phase_sweep calculates the phase of the sweep data.
                 sweep_phase = (phase_sweep(ImagineryData, RealData) - calibration_phase_mid_point)
                 GainFactor = xx ‘this is determined at calibration.see gain factor section and Datasheet.
                 Impedance = 1 / (Magnitude * GainFactor)

                ' Write Data to each global array.
                MagnitudeArray(IndexArray) = Impedance
                PhaseArray(IndexArray) = sweep_phase
                ImagineryDataArray(IndexArray) = ImagineryData
                code(IndexArray) = Magnitude
                RealDataArray(IndexArray) = RealData
                Increment = Increment - 1 ' increment was set to number of increments of sweep at the start
                FrequencyPoints(IndexArray) = Frequency
                Frequency = Frequency + FrequencyIncrements ' holds the current value of the sweep freq
                IndexArray = IndexArray + 1

              ------------- Check to see if sweep complete ----------------------
ReadbackStatusRegister = PortRead (&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H4 ' mask off bit D2

'Increment to next frequency point Frequency
WritetToControlRegister &H80, &H30
Loop

‘--------------------- END OF SWEEP: Place device into POWERDOWN mode-----------------------------------
'Enter Powerdown Mode,Set Bits D15,D13 in Control Register.
WritetToPart &H80, &HA0

END SUB
‘-------------------------------------------------------------------------------------------------------


‘The programmed sweep is now complete and the impedance and phase data is available to read in the two
‘arrays MagnitudeArray() = Impedance and PhaseArray() = phase.


sweepErrorMsg:
                    MsgBox "Error completing sweep check values"
End Sub


‘The programmed sweep is now complete and the impedance and phase data is available to read in the two
‘arrays MagnitudeArray() = Impedance and PhaseArray() = phase.
```

GAIN FACTOR CALCULATION

The code show above for the impedance sweep is based on a single point Gain Factor calculation. This calculation is carried out once at system calibration at the mid point sweep frequency and with a known impedance connected between Vout and Vin. The Gain Factor this example is calculated by exciting the calibration impedance with a 2vp-p sinusoid with a frequency of 30.750k Hz. The PGA setting is x1. The calibration is carried out with a 100k ohm resistor connected between Vout and Vin. The feedback resistor is 100k ohm. The magnitude of the real and imaginary component at the calibration frequency is given by the formula

$$Magnitude = \sqrt{R^2 + I^2}$$

Where R is the real component and I is the imaginary component of the calibration code.

The gain factor is then given by $$GAIN\ FACTOR = \left(\frac{ADMITTANCE}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude} = \frac{\left(\frac{1}{100k\ ohm}\right)}{Magnitude}$$

Refer to AD5933 datasheet for more details.

TEMPERATURE MEASUREMENT

Refer to the AD5933 datasheet for details on the temperature sensor. The temperature sensor data is stored in a 14 bit twos complement format. The conversion formula is given on page 15 of the AD5933 datasheet.

```
Private Sub MeasureTemperature()
' The Digital temperature Result is stored over two registers as a 14 bit twos complement number.
' 92H <D15-D8> and 93H<D7 to D0>.
Dim TemperatureUpper As Long.
Dim TemperatureLower As Long
'Write xH90  to the control register to take temperature reading.
WritetToPart &H80, &H90
msDelay 5 'nominal delay
ReadbackStatusRegister = PortRead(&HD, &H8F)
ReadbackStatusRegister = ReadbackStatusRegister And &H1
'if a valid temperature conversion is complete, ignore this.
If ReadbackStatusRegister <> 1 Then
        'loop to wait for temperature measurement to complete.
         Do
   ReadbackStatusRegister = PortRead(&HD, &H8F)
   ReadbackStatusRegister = ReadbackStatusRegister And &H1
    Loop Until (ReadbackStatusRegister = 1)
        Form1.Label10.Caption = "Current Device Temperature"
        MsgBox "Device Temperature Measurement Complete"
End If
```

```
' The Digital temperature Result is stored over two registers as a 14 bit twos complement number.
' 92H <D15-D8> and 93H<D7 to D0>.
TemperatureUpper = PortRead(&HD, &H92)
TemperatureLower = PortRead(&HD, &H93)
Temperature = TemperatureLower + (TemperatureUpper * 256)

If Temperature <= &H1FFF Then ' msb =0.
' Positive Temperature.
Label8.Caption = (Temperature / 32#)
Else
' Negative Temperature.
Label8.Caption = (Temperature - 16384) / 32#
End If
're-assign variables used.
TemperatureUpper = 0
TemperatureLower = 0
Temperature = 0
End Sub
```

IMPEDANCE MEASUREMENT TIPS

The next section outlines some of the workarounds with using the AD5933 for measuring impedance profiles under certain conditions.

Calibrating the AD5933:

When calculating the calibration term (i.e. GAIN FACTOR see AD5933 datasheet for further details), it is important that the receive stage is operating in its linear region. This requires careful selection of the system gain settings. The system gain settings are

- Output excitation voltage range
- Current-to-voltage gain setting resistor
- PGA gain

The gain through the system shown in Figure 27 is given by

- $$Output\ Excitation Voltage\ Range \times \frac{Gain\ Setting\ Resistor}{Z_{UNKNOWN}} \times PGA\ Gain$$

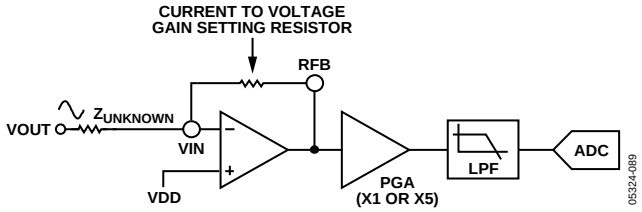


Figure 27. AD5933 System Voltage Gain

For example, assume the following system calibration settings:

VDD = 3.3 V
Gain setting resistor = 200 kΩ
$Z_{UNKNOWN}$ = 200 kΩ
PGA setting = ×1
Range 1 = 2V p-p

The peak-to-peak voltage presented to the ADC input is 2 V p-p. However had the user chosen a Programmable Gain Amplifier Setting gain of ×5, the voltage would **saturate** the ADC and the calculated calibration term (i.e. the Gain Factor) would be inaccurate due to the saturation of the ADC.

The Gain Factor should be calculated when the largest response signal is presented to the ADC whilst ensuring the signal is always maintained within the linear range of the ADC over the impedance range of interest (the reference range of the ADC is the supply AVDD).

Therefore based on the prior knowledge that the user **must** have regarding the unknown impedance span over the required frequency range of interest, the user will have to correctly configure the system gain settings (see Figure 27) i.e. the output excitation voltage range (range 1, 2, 3 or 4) , current to voltage amplifier gain setting resistor based on the un-known impedance range of interest, and Programmable Gain Amplifier Setting (either x1 or x5) which proceeds the ADC.

The user should choose a calibration impedance which is mid-value between the limits of the unknown impedance (therefore the user must know the impedance limits in order to correctly calibrate the system). The user should then choose an equal value I-V gain setting resistor to the calibration impedance. This will result in a unity gain condition about the receive side current to voltage amplifier.

For example: assume the following:

Unknown Test Impedance limits $180k\Omega \leq Zunknown \leq 220k\Omega$

Frequency Range of interest is 30 kHz and 32 KHz

The following are the system calibration gain settings:

VDD = 3.3 V
Gain setting resistor (RFB) = 200 kΩ
$Z_{CALIBRATION}$ = 200 kΩ
PGA setting = ×1
Calibration Frequency = 31 KHz (Mid-point Frequency)

The Gain factor calculated at the mid point frequency of 31 KHz can be used to calculate any impedance in the 180KΩ to 220Ω.region.Impedance results will degrade if the unknown impedance span is large or if the frequency sweep is large. If any of the calibration system gain settings change, the user will need to recalibrate the AD5933 and recalculate the Gain Factor. (See AD5933 datasheet for further details).

Measuring lower excitation frequencies

The AD5933 has a flexible internal direct digital synthesizer (DDS) core and DAC which together generate the excitation signal used to measure the impedance ($Z_{UNKNOWN}$). The DDS core has a 27 bit phase accumulator which allows sub hertz (0.1Hz) frequency resolution. The output of the phase accumulator is connected to the input of a Read Only Memory (ROM).The digital output of phase accumulator is used to address individual memory locations in the ROM. The digital contents of the ROM represent amplitude samples of a single cycle of a sinusoidal excitation waveform. The contents of each address within the ROM look up table are in turn passed to the input of a digital to analog converter (DAC) that produces the analog excitation waveform made available at the Vout pin. The DDS core (i.e. Phase accumulator and ROM look up) and the DAC are all referenced from a single system clock. The function of the phase accumulator is simply to act as a system clock divider.

The system clock for the AD5933 DDS engine can be provided in one of two ways.

- The user can provide a highly accurate and stable clock (crystal oscillator) at the external clock pin MCLK pin 8.
- Alternatively, the AD5933 provides an internal clock oscillator with a typical frequency of 16.776 MHz The internal oscillator is not available in the AD5934 and so the user must apply a clock to the external clock pin (MCLK).

The user can select the preferred system clock by programming Bit D3 in the CONTROL register (Address 81 hex, see AD5933 Datasheet).

The system clock is also used by the internal ADC to digitize the response signal. The ADC requires 16 clock periods to perform a single conversion. Therefore with a maximum system clock frequency of 16.776 MHz, the ADC can sample the response signal with a frequency of 1.0485 MHz i.e. a throughput rate of ≈1.04 MSPS. The ADC will convert 1024 samples and pass the digital results to the MAC core for processing. The AD5933 MAC core performs a 1024 point DFT to determine the peak of the response signal at the ADC input. The DFT offers excellent many advantages over conventional peak detection mechanism's including excellent dc rejection, an averaging of errors and offers phase information.

The through put rate of the AD5933 ADC will scale with the system clock i.e. lower ADC throughput rates and hence sampling frequencies can be achieved by lowering the system clock.

The conventional DFT assumes a sequence of periodic input data samples in order to determine the spectral content of the original continuous signal. In the AD5933 these samples obviously come from the 12 bit ADC for a user defined range of signal frequencies. The conventional DFT correlates the input signal against a series of test phasor frequencies in order to determine the fundamental signal frequency and its harmonics. The frequency of the test phasor is at integer multiples of a fundamental frequency given by the following formula

$$Test\ \ phasor\ \ frequency = \frac{Fs}{N}$$

Where Fs = sampling frequency of ADC and N is the number of samples taken = 1024.

The correlation is performed for each frequency integer fundamental. If the resulting correlation of the test phasor with the input sample set is non-zero, then there is signal energy at this frequency. If no energy is found in a bin then there can be no energy at that test frequency.

The DFT implemented by the AD5933 is called a ***single point DFT***; this means that the analysis or correlation frequency in the MAC core is always at the same frequency as the current output excitation frequency. Therefore when the system clock for the AD5933 is 16.776 MHz, the sample rate of the ADC is 1.04 MHz. The DSP core requires 1024 samples to perform the single point DFT. There fore the resolution of the DFT is 1.04 MHz/1024 points ≈1KHz.This calculation is based on a system clock frequency of 16 MHz being applied at MCLK. If the AD5933 tries to examine excitation frequencies below ≈1 kHz the errors introduced by spectral leakage become very significant and will result in erroneous impedance readings.

If the input signal dose not have an exact integer number of cycles over the 1024 point sample interval as shown in Figure 28 the there will not be a smooth transition from the end of one period to the next as shown in Figure 29.The leakage is a result of the discontinuities introduced by the DFT assuming a periodic input signal like that shown in Figure 29.

In order to for the AD5933 to analyze the impedance ($Z_{UNKNOWN}$) at frequencies lower than ≈1 kHz it will be necessary to scale the system clock such that the sample rate of the ADC is lowered and will cause the 1024 samples required for the single point DFT to cover an integer number of periods of the current excitation frequency.

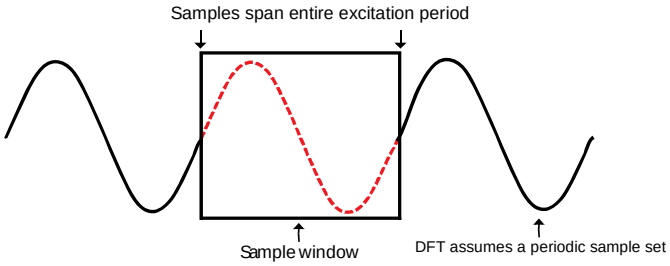


Figure 28.Sample set spanning the entire excitation period

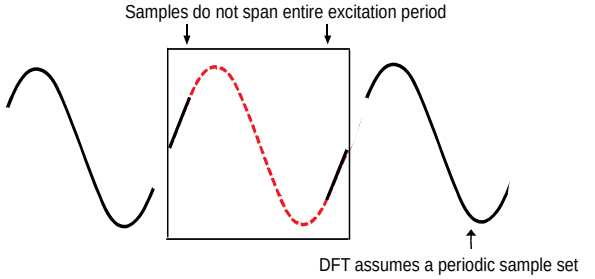


Figure 29.Sample set not spanning the entire excitation period

Q: I want to analyze frequencies in the range between 1 KHz to 10 KHz using the AD5933 using a 16 MHz crystal, will this work?

A: You will need to scale the system clock by using an external clock divider. This will reduce the sampling frequency of the ADC to a value less that 1 MHz ($F_{SAMPLING}$ =MCLK/16), however the 1024 sample set will now cover the response signal under analysis. Note by scaling the system clock you will now have reduced the maximum bandwidth of the sweep.

The user can use an additional low power DDS part like the AD9834 (see Figure 30) or an integer N divider like the ADF4001 (see Figure 31) to divide down a system clock signal before applying it to the external clock pin (MCLK) of the AD5933

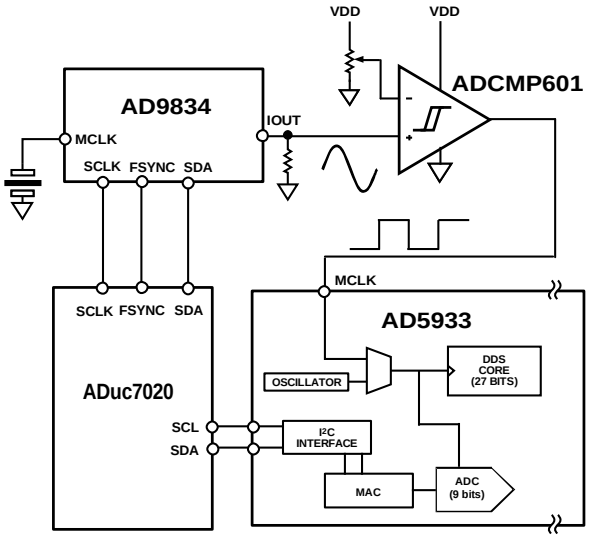


Figure 30 using an external AD9834 to scale the system clock.

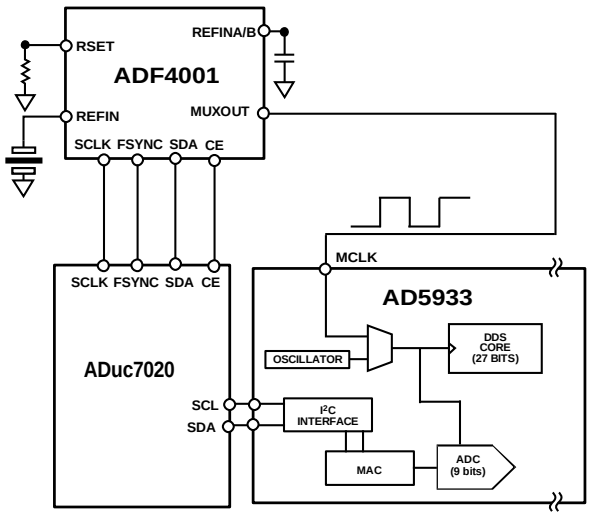


Figure 31. Using an external integer divider to scale the system clock.

Q I have scaled the system clock connected to the AD5933 in order to help me analyze lower clock frequencies. I have established the lower impedance limit (see Table 3) but my upper excitation frequency is now limited. What is the reason for this limitation?

Table 3. Experimental Lower frequency limits vs MCLK

	AD5933 lower Frequency*	Clock Frequency Applied to MCLK pin**.
1	100K Hz to-5K Hz	16 MHz
2	5K Hz to 1K Hz	4 MHz
3	5K Hz to 300 Hz	2 MHz
4	300 Hz to 200 Hz	1 MHz
5	200 Hz to 100 Hz	250 KHz
6	100 Hz to 30 Hz	100 KHz
7	30 Hz to 20 Hz	50 KHz
8	20 Hz to 10 Hz	25 KHz

*Lower Frequency sweep limit established by applying the divided clock signal to the MCLK pin of the AD5933, and by calibrating and re-measuring a nominal impedance $Z_{CALIBRATION}$ e.g. a 200KΩ resistor over a 500hz linear sweep from the programmed start frequency (I-V gain resistor setting = $Z_{CALIBRATION}$ e.g. 200kΩ, PGA = X1. Δ Frequency = 5Hz, number of points = 100).The lower frequency limit is established as the frequency at which the DFT and hence impedance vs. frequency results begins to degrade and deviate from the expected value of the measured impedance $Z_{CALIBRATION}$ e.g. 200KΩ.

**TTL clock levels applied to MCLK pin, V_{IH} = 2V, V_{IL} = 0.8V.

A: For example if the user has already established that a scaled clock frequency of 4 MHz must be applied to the external clock pin of the AD5933 in order to correctly analyze a 3 KHz signal. The applied system clock (external or internal oscillator) is divided by a factor of 4 before being routed as the reference clock to the DDS. The system clock is directly connected to the ADC without any divide so the ADC sampling clock is running at 4 times the speed of the DDS core. Therefore with a system clock of 4 MHz, the DDS reference clock is now 1/4 × 4 MHz = 1 MHz and the ADC clock is 4 MHz. The AD5933 DDS has a 27 bit phase accumulator; however the top three most significant bits are internally connected to logic zero. Therefore with the top three MSB's set to zero the max DDS output frequency is now reduced by a further factor of 1/8th.Therefore the maximum output frequency is now 1/32*1 MHz = 31.25 kHz.

In summary it is possible to accurately measure the 3 KHz signal using a lower system clock of 4Mhz however the two main tradeoffs are firstly that it will take AD5933 longer to return the impedance results due to the slower ADC conversion clock speed and secondly the upper excitation limit is now restricted to 31.25Khz.

Measuring higher excitation frequencies

The AD5933 is specified to a typical system accuracy of 0.5 % (assuming the AD5933 system is calibrated correctly for the impedance range under test) within the frequency range of 1 KHz up to 100 kHz. The lower frequency limit is determined by the value of the system clock frequency connected to the external clock pin (MCLK) of the AD5933.The lower limit can be reduced by scaling the system clock (see Measuring lower excitation frequencies).The upper frequency limit of the system is due to the finite bandwidth of the internal amplifiers coupled with the effects of the low pass filter pole locations (e.g. 200 KHz, 300 KHz) which are used to roll-off any noise signals from corrupting the DFT output on the receive side of the AD5933.Therefore the AD5933 will have a finite frequency response similar to that shown in Figure 32.

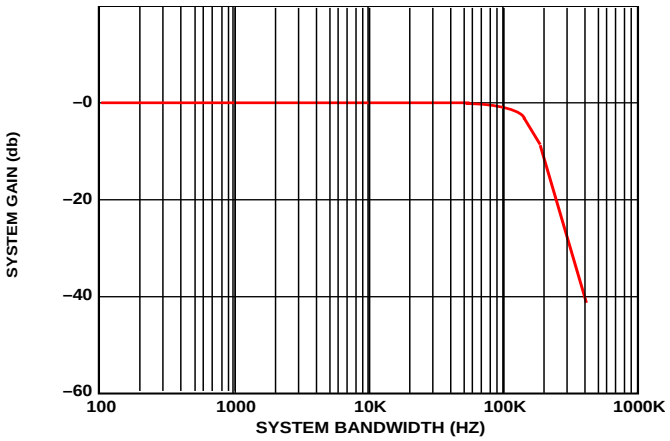


Figure 32. Typical AD5933 system bandwidth

Using the AD5933 to analyze frequencies past 100 kHz will introduce errors in impedance profile if the sweep span is large, due to the effect of the increased roll off in the finite frequency response of the system past 100Khz. However if the user is sweeping in frequency above 100 kHz it is important to ensure that the sweep range is as small as possible e.g. 120 kHz to 122 kHz .The impedance error from the calibration frequency is approximately linear over a small frequency range. The user can remove the linear error introduced by carrying out an endpoint/multipoint calibration (see AD5933 datasheet for further details on end point calibration).

Measuring the phase across an impedance

The AD5933 returns a complex output code made up of a separate real and imaginary component. The real component is stored at register address 94h 95h and an imaginary component is stored at register address 96h 97h after each sweep measurement. These correspond to the real and imaginary components of the DFT and NOT the resistive and reactive components of the impedance under test.

For example it is very common miss conception to assume that if a customer was analyzing a series RC circuit that the real value stored in 94h and 95h and the imaginary value stored at 96h and 97h corresponds to the resistance and capacitive reactance respectfully. This is incorrect; however the magnitude of the impedance (|Z|) can be calculated by calculating the magnitude of the real and imaginary components of the DFT given by the following formula

$$Magnitude = \sqrt{R^2 + I^2}$$

After each measurement multiplying it by the calibration term (see Gain Factor calculation in AD5933 datasheet) and inverting the product. The magnitude of the impedance is therefore given by the following formula.

$$Impedance = \frac{1}{GAIN\ \ FACTOR \times Magnitude}$$

Where the gain factor is given by the following formula

$$GAIN\ FACTOR = \left(\frac{ADMITTANCE}{Code}\right) = \frac{\left(\frac{1}{Impedance}\right)}{Magnitude}$$

The user must calibrate the AD5933 system for a know impedance range to determine the gain factor before any valid measurement can take place. Therefore the user of the AD5933 must know the impedance limits of the complex impedance ($Z_{UNKNOWN}$) for the sweep frequency range of interest. The gain factor is simply determined by placing known impedance between the input/output of the AD5933 and measuring the resulting magnitude of the code. The AD5933 system gain settings need to be chosen in order to place the excitation signal in the linear region of the onboard ADC. (Refer to the datasheet for further details)

Since the AD5933 returns a complex output code made up of a real and imaginary component, the user will also be able to calculate the phase of the response signal through AD5933 signal path. The phase is given by the following formula.

$$Phase\ (rads) = Tan^{-1}(I / R)$$

The phase measured by the above formula, accounts for the phase shift introduced to the DDS output signal as it passes through the internal amplifiers on the transmit and receive side of the AD5933 along with the low pass filter and also the impedance connected between the V_{OUT} and V_{IN} pins of the AD5933.

The parameters of interest for many users of the AD5933 is the magnitude of the impedance ($|Z_{UNKNOWN}|$) and the Impedance phase (ZØ).The measurement of the Impedance phase (ZØ) is a two step process.

The first step involves calculating the AD5933 system phase. The AD5933 system phase can be calculated by placing a resistor across the Vout and Vin pins of the AD5933 and calculating the phase (using the formula above) at after each measurement point in the sweep. By placing a resistor across the Vout and Vin pins, there is no additional phase lead or lag introduced to the AD5933 signal path and the resulting phase will be due entirely to the internal poles of the AD5933 i.e. the system phase.

Once the system phase has been calibrated using a resistor, the phase of any unknown impedance can be calculated by inserting the un-impedance between the Vin and Vout terminals of the AD5933 and recalculating the new phase (including the phase due to the impedance) using the same formula. The phase of the unknown impedance (ZØ) is given by the following formula.

$$ZØ = (\Phi unknown - \nabla system)$$

Where $\nabla system$ is the phase of the system with a calibration resistor connected between V_{IN} and V_{OUT}.

$\Phi unknown$ is the phase of the system with the unknown impedance connected between Vin and Vout.

And ZØ is the phase due to the impedance i.e. the impedance phase.

Note: It is possible e to calculate both the gain factor and to calibrate the system phase using the same real and imaginary component values when a resistor is connected between the Vout and Vin pins of the AD5933.

Example: measuring the Impedance phase (ZØ) of a capacitor.

The excitation signal current leads the excitation signal voltage across a capacitor by -90 degrees. So before any measurement is carried out one would intuitively expect to see an approximate -90 degree phase difference between the system phase responses measured with a resistor and that the system phase responses measured with capacitive impedance.

As outlined above, if the user would like to determine the phase angle of capacitive impedance (ZØ) the user will firstly have to determine the system phase response($\nabla system$) and subtract this from the phase calculated with the capacitor connected between Vout and Vin ($\Phi unknown$).

A plot showing the AD5933 system phase response calculated using a 220 kΩ calibration resistor (Rfb = 220KΩ, PGA = ×1) and the repeated phase measurement with a 10pf capacitive impedance is shown in Figure 33.

The phase difference (i.e. ZØ) between the phase response of a capacitor and the system phase response using a resistor is the impedance phase of the capacitor (ZØ) and is shown in Figure 34.

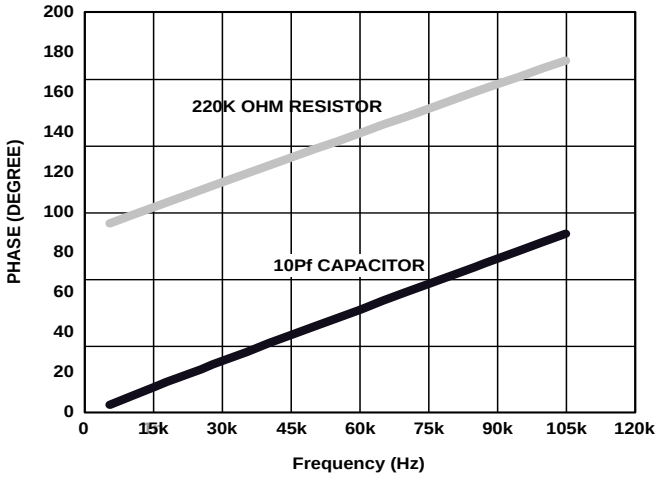


Figure 33. System phase response vs. capacitive phase

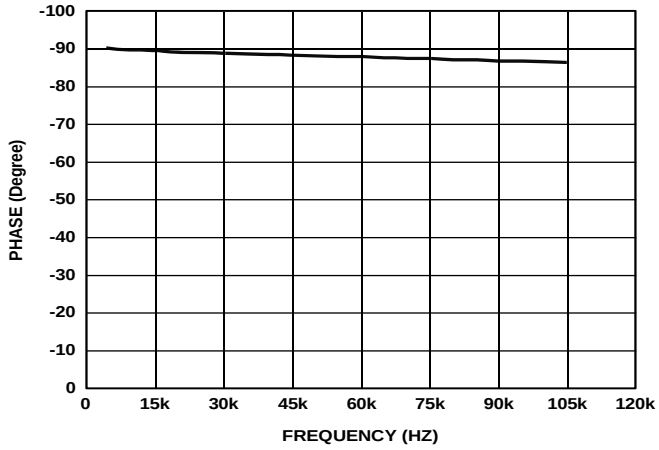


Figure 34. Phase response of a capacitor

One important point to note about the phase formula used to plot Figure 33 is that it uses the arctangent function which will return a phase angle in radians and therefore it will be necessary to convert from radians to degrees.

Also care must be taken when using the arctangent formula when using the real and imaginary values to interpret the phase at each measurement point .The arctangent function will return the correct "standard" phase angle only when the sign of the real and imaginary values are positive i.e. when the co-ordinates lie in the first quadrant. The standard angle is angle taken counter clock wise form the positive real x-axis. If the sign of the real component is positive and the sign of the imaginary component is negative i.e. the data lies in the second quadrant, then the arctangent formula will return a negative angle and it is necessary to add a further180 degrees to calculate the correct standard angle. Likewise when the real and imaginary component are both negative i.e. when the co-ordinates lie in the third quadrant, then the arctangent formula will return a positive angle it is necessary to add 180 degrees from the angle to return the correct standard phase. Finally when the real component is positive and the imaginary component is negative i.e. the data lies in the fourth quadrant then the arctangent formula will return a negative angle. It is necessary to add 360 degrees to angle in order to calculate the correct phase angle.

Therefore the correct standard phase angle is dependant upon the sign of the real and imaginary component and is summarized in **Table 4**.

Table 4. Phase angle

Real	imaginary	quadrant	Phase angle (degrees)
positive	positive	1st	$Tan^{-1}(I/R)*\frac{180}{\pi}$
positive	negative	2nd	$180+\left(Tan^{-1}(I/R)*\frac{180}{\pi}\right)$
negative	negative	3rd	$180+\left(Tan^{-1}(I/R)*\frac{180}{\pi}\right)$
positive	negative	4th	$360+\left(Tan^{-1}(I/R)*\frac{180}{\pi}\right)$

Once the magnitude of the impedance (|Z|) and the impedance phase angle (ZØ, in radians) are correctly calculated is it possible to determine the magnitude of the real (resistive) and imaginary (reactive) component of the impedance ($Z_{UNKNOWN}$) by the vector projection of the impedance magnitude onto the real and imaginary impedance axis using the following formulas.

The real component is given by $|Z_{REAL}| = |Z| \times \text{Cos}(ZØ)$.

The Imaginary component is given by $|Z_{IMAG}| = |Z| \times \text{Sin}(ZØ)$

EVALUATION BOARD SCHEMATIC

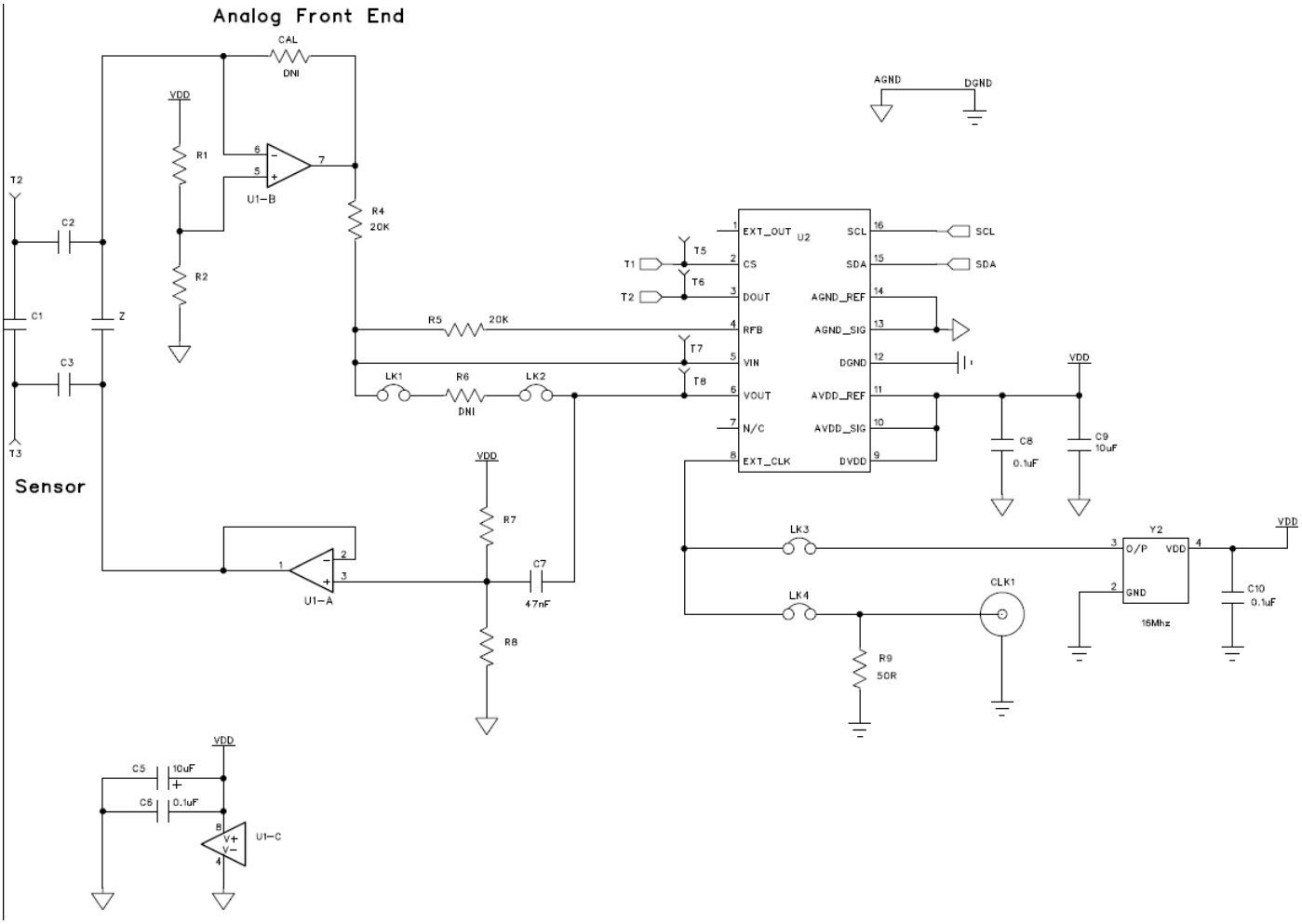


Figure 35.

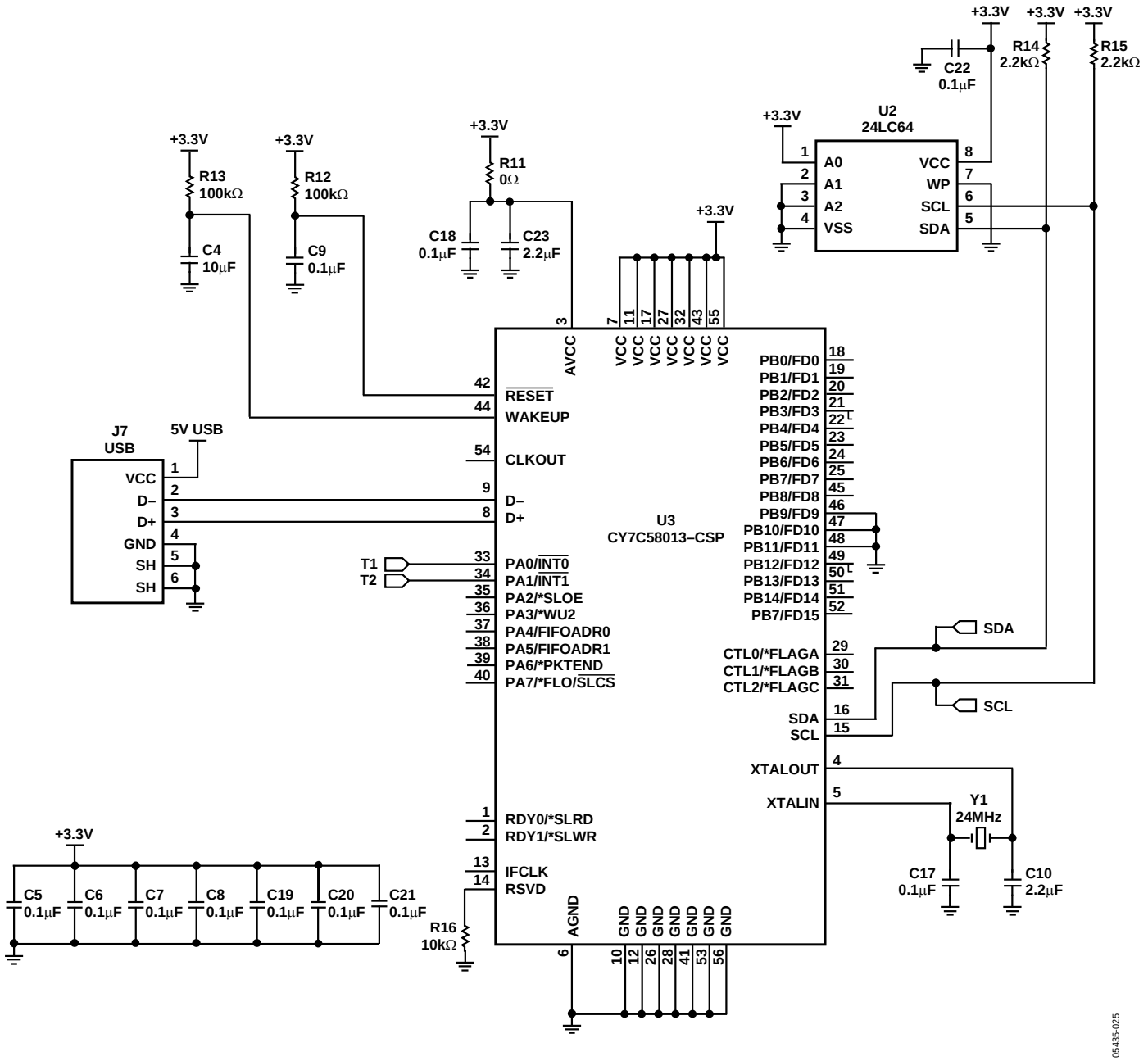

+3.3V
R13 100kΩ
C4 10µF
R12 100kΩ
C9 0.1µF
R11 0Ω
C18 0.1µF
C23 2.2µF
C22 0.1µF
R14 2.2kΩ
R15 2.2kΩ
U2 24LC64
A0
A1
A2
VSS
VCC
WP
SCL
SDA
J7 USB
5V USB
VCC
D–
D+
GND
SH
SH
U3 CY7C58013–CSP
AVCC
RESET
WAKEUP
CLKOUT
PA0/INT0
PA1/INT1
PA2/*SLOE
PA3/*WU2
PA4/FIFOADR0
PA5/FIFOADR1
PA6/*PKTEND
PA7/*FLO/SLCS
RDY0/*SLRD
RDY1/*SLWR
IFCLK
RSVD
AGND
GND
PB0/FD0
PB1/FD1
PB2/FD2
PB3/FD3
PB4/FD4
PB5/FD5
PB6/FD6
PB7/FD7
PB8/FD8
PB9/FD9
PB10/FD10
PB11/FD11
PB12/FD12
PB13/FD13
PB14/FD14
PB7/FD15
CTL0/*FLAGA
CTL1/*FLAGB
CTL2/*FLAGC
SDA
SCL
XTALOUT
XTALIN
T1
T2
Y1 24MHz
C17 0.1µF
C10 2.2µF
C5 0.1µF
C6 0.1µF
C7 0.1µF
C8 0.1µF
C19 0.1µF
C20 0.1µF
C21 0.1µF
R16 10kΩ
05435-025

Figure 36. .

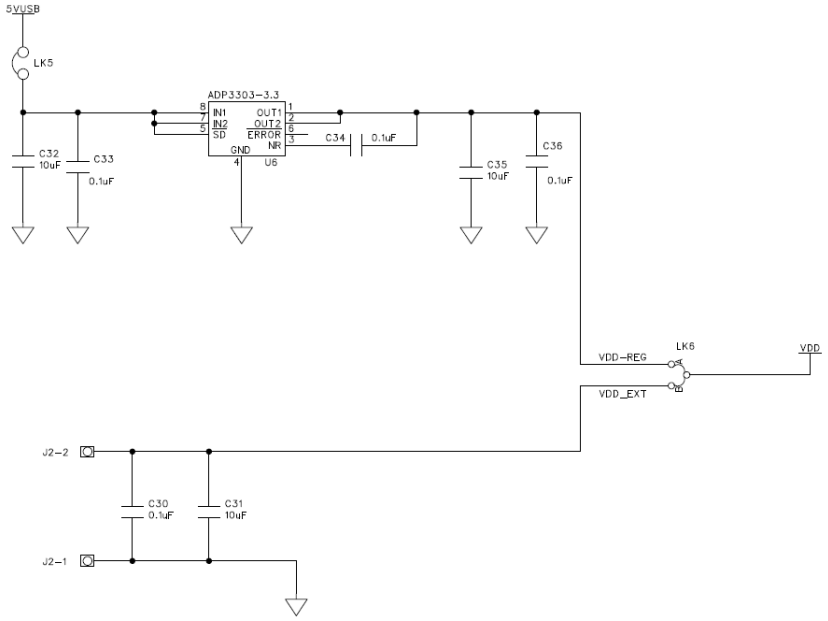
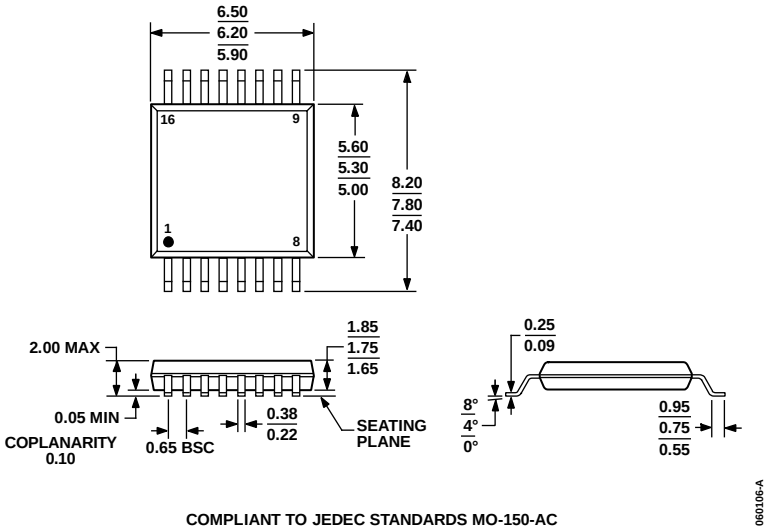

5VUSB
LK5
ADP3303-3.3
IN1
IN2
SD
OUT1
OUT2
ERROR
NR
GND
U6
C32
10uF
C33
0.1uF
C34
0.1uF
C35
10uF
C36
0.1uF
VDD-REG
LK6
VDD
VDD_EXT
J2-2
J2-1
C30
0.1uF
C31
10uF

Figure 37

BILL OF MATERIALS

c	Part Description	Value	Tolerance	PCB Decal	PART DESC	MFG #1	Part Number
C1	CAP	DNI		CAP\MR04	Place holder	n/a	n/a
C2	CAP	DNI		CAP\MR04	Place holder	n/a	n/a
C3	CAP	DNI		CAP\MR04	Place holder	n/a	n/a
Z	CAP	DNI		CAP\MR04	Place holder - Insert 2 Wire-Wrap Pins	Analog Issue	73017015
C5	CAP+	10uF		CAP\TAJ_B	10V Tantalum Capacitor	AVX	TAJB106K016R
C6	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C7	CAP	47nF	10%	R1/8W	CAPACITOR, 47NF, 50V, ThruHole	Multicomp	MCRR50473X7RK0050
C8	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C9	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C10	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C11	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C12	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C13	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C14	CAP	2.2uF		0603	6.3V X5R SMD Ceramic Capacitor	Yageo	CC0603KRX5R5BB225
C15	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C16	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C17	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C18	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C19	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C20	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C21	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C22	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C23	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C24	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C25	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C26	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C27	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C28	CAP	22pF	5%	0603	50V NPO SMD Ceramic Capacitor	Yageo	CC0603JRNPO9BN220
C29	CAP	22pF	5%	0603	50V NPO SMD Ceramic Capacitor	Yageo	CC0603JRNPO9BN220
C30	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C31	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C32	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C33	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C34	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
C35	CAP	10uF		0805	X5R Ceramic Capacitor	Yageo	CC0805KKX5R6BB106
C36	CAP	0.1uF	10%	0603	50V X7R SMD Ceramic Capacitor	AVX	06035C104KAT2A
CLK1	SMB			SMB	SMB SOCKET	Tyco	1-1337482-0
D4	LED			LED-0805	Green LED	Avago	HSMG-C170
GL1	GROUNDLINK			COMPONENTLINK	Copper Short	n/a	n/a
J1	USB-MINI-B			USB-MINI-B	USB Mini-B Connector	Molex	56579-0576
J2	CON\POWER			CON\POWER	2 Pin Terminal Block (5mm Pitch)	Camden	CTB5000/2
LK1	JUMPER			SIP-2P	Jumper Block, 2 Pins 0.1" Spacing	Harwin	M20-9990246
LK2	JUMPER			SIP-2P	Jumper Block, 2 Pins 0.1" Spacing	Harwin	M20-9990246
LK3	JUMPER			SIP-2P	Jumper Block, 2 Pins 0.1" Spacing	Harwin	M20-9990246
LK4	JUMPER			SIP-2P	Jumper Block, 2 Pins 0.1" Spacing	Harwin	M20-9990246
LK5	JUMPER			SIP-2P	Jumper Block, 2 Pins 0.1" Spacing	Harwin	M20-9990246
LK6	JUMPER2\SIP3			LINK-3P	Jumper Block, 3 Pins 0.1" Spacing	Harwin	M20-9990246
R1	RES0603	49K9	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 49K9
R2	RES0603	49K9	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 49K9
CAL	RES	DNI	n/a	R1/8W	Place holder - Insert 2 Wire-Wrap Pins	Analog Issue	73017015
R4	RES0603	20K	0.10%	0603	SMD Resistor (0.1%)	Panasonic	ERA3AEB203V
R5	RES0603	20K	0.10%	0603	SMD Resistor (0.1%)	Multicomp	MC 0.063W 0603 1% 20K
R6	RES	DNI	n/a	R1/8W	THROUGH HOLE Resistor 1/8 W	n/a	n/a
R7	RES0603	49K9	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 49K9
R8	RES0603	49K9	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 49K9
R9	RES	50R	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 49R9
R10	RES	1k		0805	SMD Resistor	Multicomp	MC 0.1W 0805 1% 1K
R11	RES	100k	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 10
R12	RES	100k	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 10
R13	RES	0R	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 0R
R14	RES	10k	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 10K
R15	RES	2k2	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 2K2
R16	RES	2k2	1%	0603	SMD Resistor	Multicomp	MC 0.063W 0603 1% 2K2
T1	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
T2	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
T3	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
T5	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
T6	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
T7	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
T8	TESTPOINT			TESTPOINT	TESTPOINT	Black Testpoint	20-2137
U1	AD8606			SO8NB	Dual Op-Amp	Analog Devices	AD8606ARZ
U2	AD5934			SSOP16		Analog Devices	AD5933BRSZ / AD5934BRS
U3	CY7C68013-CSP			LFCSP-56	USB Microcontroller	Cypress Semiconductor	CY7C68013-56LFC
U4	24LC64			SO8NB	IC SERIAL EEPROM 64K 2.5V 8-SOIC	Microchip	24LC64-I/SN
U5	ADP3303-3.3			SO8NB	Precision Low Dropout Voltage Regulato	Analog Devices	ADP3303ARZ-3.3
U6	ADP3303-3.3			SO8NB	Precision Low Dropout Voltage Regulato	Analog Devices	ADP3303ARZ-3.3
Y1	XTAL-CM309S	24 MHz		XTAL_CM309S	CM309S SMD Crystal	AEL	X24M000000S244
Y2	AEL-4303	16Mhz		AEL-4303	3.3V 16MHz Clock Oscillator	AEL	

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AC

Figure 38. 16-Lead Shrink Small Outline Package [SSOP]
(RS-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5933YRSZ[1]	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16
AD5933YRSZ-REEL7[1]	−40°C to +125°C	16-Lead Shrink Small Outline Package (SSOP)	RS-16
EVAL-AD5933EBZ[1]	−40°C to +125°C	Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

EB05435–0–3/05(PrA)