Andrew Chen (Yung-Chun Chen)

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EDUCATION

University of California, Berkeley *GPA: 4.0/4.0*

Exchange Student in Electrical Engineering & Computer Science *Jan. 2024 – June 2024*

- Coursework: Computer Architecture and Engineering, Introduction to Digital Design and Integrated Circuits, Application Specific Integrated Circuits Laboratory

National Tsing Hua University, Hsinchu, Taiwan *GPA: 4.26/4.3 (Last 2y), 3.97/4.3 (Overall)*

B.S. in Electrical Engineering: *Sep. 2020 – Jan. 2024*

- Coursework: Introduction to Integrated Circuit Design, Integrated Circuit Design Laboratory, Computer Architecture, Algorithms, Embedded System Laboratory, Machine Learning

PROFESSIONAL EXPERIENCE

SiFive, Inc. – RTL Design Engineer *Nov. 2024 – Present*

- Integrated new ISA features such as SiFive Scalar Coprocessor Interface into in-order RISC-V CPU cores for Essential, Intelligence, and Automotive series
- Built detailed instruction tracking system that monitors the complete lifecycle across all pipeline stages, enabling performance bottleneck analysis and RVWMO compliance check
- Discovered 5+ critical hang scenarios by implementing automated assertion checker using Chisel HDL
- Validated Control and Status Register functionality with automated read/write mask generation

Micron Technology – ASIC Design Engineer Intern *Jul. 2024 – Aug. 2024*

- Improved Clock-Domain-Crossing multi-flop identification by refining Spyglass report extraction, reducing analysis time by 25%
- Automated Register Models and RTL implementations comparison, cutting comparison time to 1/10
- Resolving mismatches between RTL design and specs documentation

RESEARCH & PROJECTS

A 22nm Non-Volatile ReRAM Compute-in-Memory Edge-AI Processor

National Tsing Hua University (Memory Lab) *Dec. 2025 – Apr. 2026 (Expected)*

- Designing and integrating the RISC-V CPU, DMA, DRAM interface, and on-chip bus
- Extending the RISC-V CPU with custom instructions for PE-array support and developing a CPU–PE interaction testbench, enabling functional substitution between the PE array and CIM macro

Laboratory for Computer Architecture and Engineering

University of California, Berkeley *Jan. 2024 – June 2024*

- Optimized RISC-V processors such as Rocket Core and Berkeley Out-of-Order Machine in Chisel
- Decreased 13.2% of average memory access time by implementing victim cache with LRU replacement policy
- Reduced miss rates under 15% for all benchmarks by designing branch predictors on out-of-order processors

RISC-V ISA implementation on a 3-stage CPU integrated with SRAM

University of California, Berkeley *Jan. 2024 – June 2024*

- Designed a 3-stage RISC-V CPU, including ALU design, Core implementation, and memory system implementation, and upgraded up to 5-stage for better performance
- Incorporated bypass units and stall units to reduce Cycle Per Instruction (CPI) by 12%
- Built custom 4-way I/D caches using SRAM macros, reduced 30% conflict miss and shortened critical path by 4ns through SRAM-aware placement
- Refined SRAM placement to shorten the critical path by 4ns

Five-Stage CPU for RISC-V ISA (RV32I)

National Tsing Hua University (IC Design Lab) *Sep. 2023 – Jan. 2024*

- Developed a 5-stage RISC-V CPU in Verilog and completed full ASIC flow including RTL simulation, synthesis, auto place-and-route, and post-layout simulation using Cadence 45nm
- Reduced CPI by 19% through the implementation of basic bypass and stall units
- Emulated I/D cache using registers and improved instruction memory locality by 30% by eliminating unnecessary NOPs

ReRAM Based Computing-in-Memory (CIM) Macro for CNN-Based Edge Processors

National Tsing Hua University (Memory Lab) *Sep. 2022 – May 2023*

- Developed multiply-accumulate units with CIM structure instead of conventional Von-Neumann architecture under TSMC 0.18um technology
- Reduced 1/4 power consumption by Down-Scaling Weighted Current Translator
- Increased 2x outputs possibility by integrating Triple Margin Current Sensed Amplifier and Accumulator
- Won the first prize of the TSMC research assistant fellowship with 50,000 NTD

Multiclass Image Classification on BIRDS 525 SPECIES dataset by CNN

National Tsing Hua University *Nov. 2023 – Jan. 2024*

- Implement with PyTorch and scikit-learn libraries
- Built a deep learning pipeline with pretrained ResNet-18 model to classify 525 bird species from high-variance image data, and add custom layers to improve generalization
- Applied random crop, flip and normalization on images to address class imbalance and overfitting

Full-Custom IC Design for ReRAM ROM (128x16bits) macro

National Tsing Hua University *Sep. 2022 – Jan. 2023*

- Directed the weekly meeting, assigned tasks, and proposed the ROM macro structure
- Integrated decoders, mux, sensing amplifiers, and clock generator
- Initiated from schematic entry, pre-simulation, layout, DRC/LVS, RC extraction, and post-simulation under TSMC 0.18um technology

Low Dropout Regulator (LDO) combined with Bandgap Reference

National Tsing Hua University *Sep. 2022 – Jan. 2023*

- Simulated a PMOS-based Low Dropout Regulator (LDO) with a precision Bandgap Reference using HSPICE and WaveView, delivering a stable 1.6V output from a 1.8V ±10% supply
- Met all design specifications including <100 μV/°C temperature coefficient, DC PSR <−60 dB, 100 kHz PSR <−40 dB, and LDO phase margin >65° under a 100 mA, 50 pF load
- Engineered a custom high-gain error amplifier to meet stringent PSR requirements, ensuring robust output regulation and noise rejection

CERTIFICATE & FILLOWSHIP

Professional Course Learning Honor Certificate x 2 *National Tsing Hua University*
Top 10% of the college *Sep. 2022, Sep. 2023*
NVIDIA Deep Learning Institute Certificate *NVIDIA*
Building Transformer-Based Natural Language Processing Applications *Dec. 2023*
First Prize of the TSMC Research Assistant Fellowship *TSMC*
Awarded with 50,000 NTD fellowship *May 2023*
Quality Champion Award 2025 – On-time Delivery *SiFive*
Recognized for on-time delivery and workflow excellence *Nov. 2025*

TECHNICAL SKILLS

Programming: C/C++, Python, git, RISC-V assembly, scala
IC Design Tools: Verilog, System Verilog, Chisel HDL, Hammer, Synopsys Custom WaveView, Verdi, Laker, Design Compiler, Cadence Innovus, Virtuoso, conformal LEC, HSPICE