Homework 3

Tausif Zaman
1001415041
CSE 2312

3. In no pipelining, the cycle time must allow an instruction to go through all stages in one cycle. It is the same as cycle time since it takes the instruction one cycle to go from the beginning of fetch to the end of write back

a) for R-type instructions : 350 + 150 + 175 + 500 + 200 = 1375 ps

b) For I-type instruction: for immediate type inst there is no need of register write because it will update in memory only like store inst
therefore : 350 + 150 + 175 + 500 = 1175 ps

for J-type : in jump instruction, it will go to instruction fetch to inst decode only so;
350 + 150 = 500 ps

c) In pipelining the cycle time is reduced to the length of the longest stage plus the register delay if present
therefore: 470 ps

4. a) since it is a five stage processor pipeline there is a dependancy for the first set of instructions. From register 3 is written by add instruction and same register is used as an operand by the next or instruction