5b) The 5-stage pipeline execution without forwarding:

| Instruction | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| addi $s0, $zero, 3 | F | D | X | M | W | | | | | | | | |
| LOOP: lw $t0, 0($s1) | | F | D | X | M | W | | | | | | | |
| add $t1, $t0, $t2 | | | F | D | X | M | W | | | | | | |
| add $t3, $t1, $t4 | | | | F | D | X | M | W | | | | | |
| addi $s0, $s0, -1 | | | | | F | D | X | M | W | | | | |
| bne $s0, $zero, LOOP | | | | | | F | D | - | - | X | M | W | |
| addi $s1, $zero, $zero | | | | | | | | F | D | X | D | M | W |

The number of clock cycles required is 13.

| # 1) | RegDst | Branch | MemRead | MemtoReg | MemWrite | ALUSrc | RegWrite |
|---|---|---|---|---|---|---|---|
| #1 | 1 | 0 | 1 | 0 | 0 | 10 | 1 |
| #2 | 0 | 0 | X | 1 | 0 | 00 | 1 |
| #3 | X | 0 | 0 | X | 1 | 00 | 0 |
| #4 | X | 1 | 0 | X | 0 | 01 | 0 |
| #5 | 0 | 0 | 1 | 0 | 0 | 00 | 1 |

2) Implementing one stage pipeline via pipelining.