PCB Checklist (EAGLE-centric, sorry)

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From github.com/andrewgreenberg

Pre-layout Checklist

- Create board from schematic.
- Load in your design rules using 'DRC'. Double check your rules match your manufacturer's design rules: trace/space, board edge, minimum drill size, etc. (in other words: load in the correct design rules)
- Set your grid to something reasonable (e.g., 0.1 mm grid, or 0.01 inch grid).
- Set the outline of your board in the dimension layer (if different than the default).

Lay out strategies

- Place all components that must be in a certain spot (e.g., connectors and mounting holes)
- Move components that are in a “schematic block” together, then optimally rotate and place components to reduce crossed airwires, then route.
- Optimally rotate and place grouped components to minimize airwires, then route.
- Route power lines and ground planes.

Layout checklist

- Optional but recommended: are components snapped to the grid?
- Is there enough physical space around components for assembly?
- Are your test points in easily accessible places?
- Are there any hidden traces that you can't probe?

Best Practices

- Are all of the small bypass caps right next to the power and ground leads of the ICs?
- Are the power lines as wide as reasonably possible?
- Did you use either larger drills for power lines, or multiple small vias for power lines?
- Are there ground planes (polygons with name 'GND') on both sides? (Make sure your polygons have an isolate of > design rule; e.g., with a design rule of 0.006 in, make the isolate 0.01 in).
- Are your ground planes stitched together with vias?
- Is your board as small as possible?
- Run your DRCs often

Post-layout checklist

- Turn on the 'tnames' layer (and 'bnames' if bottom silkscreen) and use 'smash' and 'size' to position component names until reasonably small and usable during component placement.
    - Avoid placing text on pads and vias.
- Verify that at least the organization name, board name, and version number are on the silkscreen (EAGLE: 'tplace' layer).

Final checkout

- Print out 1:1 PCB and lay components on printout to double check packages.
- **Run DRC; there should be no un-approved errors.**
- Re-check approved errors for mis-approved errors.
- Make sure all you either have all components in stock, or that components you specified are in stock before firing off board.