GP4020

GPS Receiver Baseband Processor

June 2005

Features

- Complete GPS correlator and Firefly MF1 microcontroller core
- ARM 7TDMI™ (Thumb®) Microprocessor, with JTAG ICEBreaker™ Debug Interface
- Fully Configurable External Data Bus
- 12 Fully Independent Correlation Channels
- Low Voltage Operation: 3·3V
- Low Current Power–Down Mode
- 1PPS UTC Aligned Timing Output
- Dual UART
- 3-wire BµILD Serial Input/Output (BSIO) Interface
- 8 General Purpose Input/Output (GPIO) Lines
- Boot ROM, allowing Software Upload via UART
- 8K Bytes Internal SRAM
- Compatible with GP2015 and GP2010 RF Front Ends

Applications

- GPS Navigation Systems
- GPS Geodetic Receivers
- Time Transfer Receivers
- Automatic Vehicle Location (AVL)
- E911 Emergency Positioning

Related Products

Part	Description	Data sheet
GP2015	GPS Receiver RF Front End (TQFP 48 package)	DS4374
GP2010	GPS Receiver RF Front End (PQFP 44 package)	DS4056

Ordering Information

GP4020/IG/GQ1N 100 Pin LQFP Trays, Bake & Drypack
GP4020/IG/GQ1Q 100 Pin LQFP Tape & Reel, Bake & Drypack
GP4020/IG/GQ2Q 100 Pin LQFP* Tape & Reel, Bake & Drypack
GP4020/iG/GQ2N 100 Pin LQFP* Trays, Bake & Drypack
*Pb Free Matte Tin

-40°C - +85°C

Description

The GP4020 is a complete digital baseband processor for a Global Positioning System (GPS) receiver. It combines the 12-channel correlator function of the GP2021 with an advanced ARM7TDMI (Thumb) microprocessor to achieve a higher level of integration, reduced system cost, reduced power consumption and added functionality. The GP4020 complements the GP2015 and GP2010 C/A code RF downconverters available from Zarlink Semiconductor.

The correlator section contains 12 identical tracking module blocks, one for each channel. Each channel contains all the components necessary for acquiring and tracking the received signal, and also contains other functional blocks, which are used to produce part of the measurement data set. Individual channels may be deactivated for systems not requiring full 12-channel operation and thus allowing for reduced power consumption and processor loading.

The microprocessor section contains the Firefly MF1 microcontroller core, which includes an ARM7TDMI with a Thumb instruction de-compressor plus the Firefly BµILD module. Also included are a second UART, BµILD Serial I/O, General I/O and Watchdog functions.

Absolute Maximum Ratings

Supply voltage (V_{DD}) from ground (GND)	-0·5V to +5·0V
Bias for 5V inputs	+7·0V max.
Input voltage (any input pin)	GND-0·5V to V_{DD}+0·5V
Output voltage (any output pin)	GND-0·5V to V_{DD}+0·5V
Storage temperature	-55°C to +150°C
Static discharge (HBM)*	2kV

*Mil Std 883 Human Body Model = discharge from 100pF through 1500Ω between any 2 pins

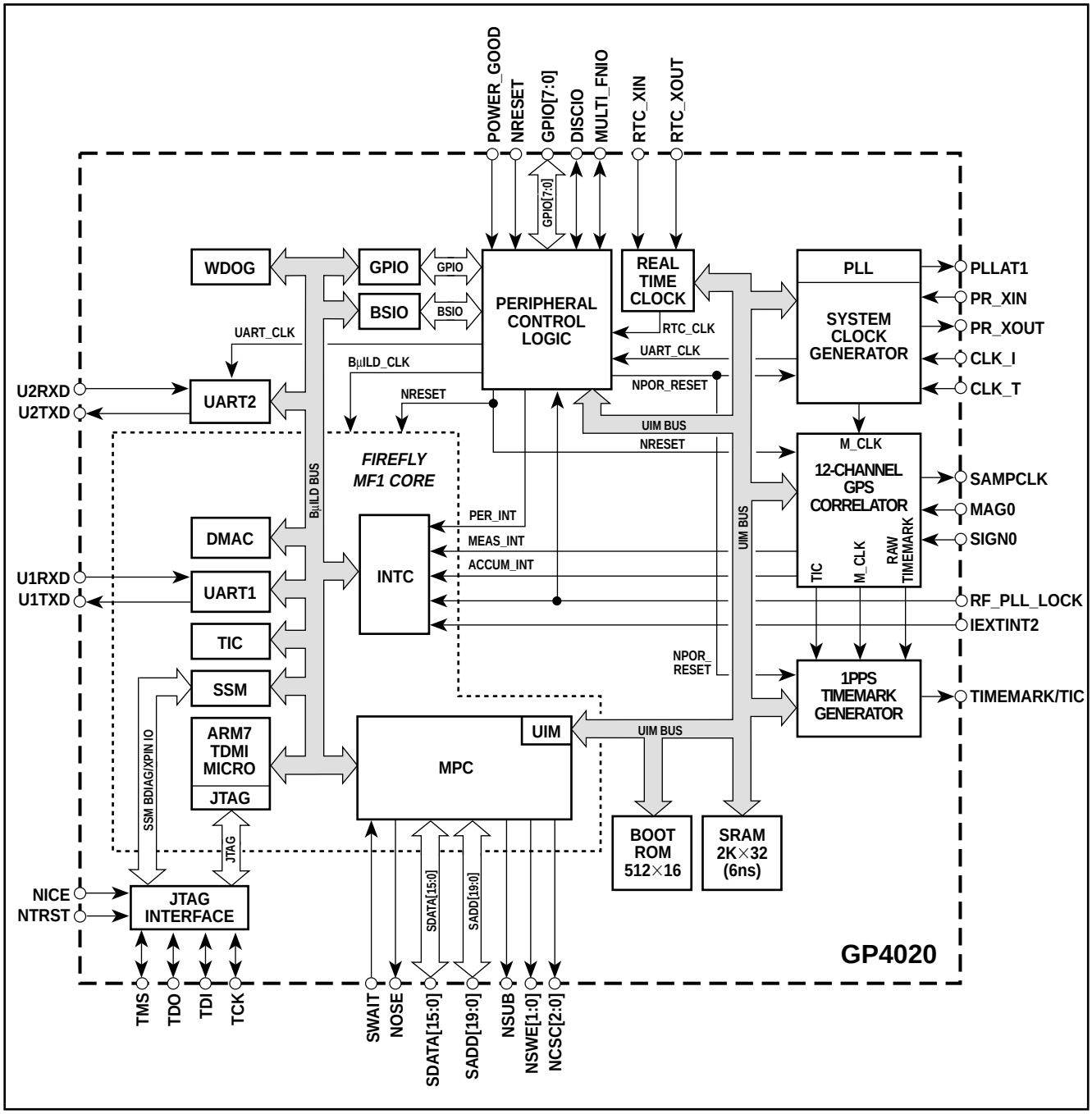


Figure 1 - Block diagram

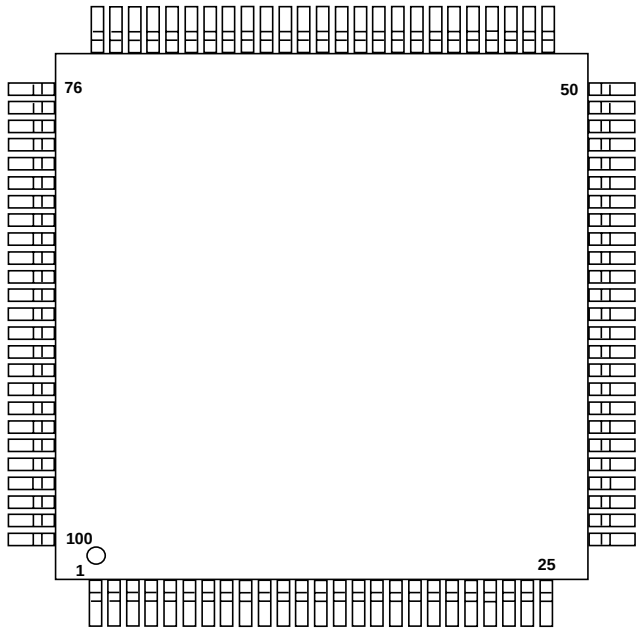


Figure 2 - Pin connections (top view)

Pin No.	Signal Name	Type	Associated circuit block	Description	Notes
1	SADD[0]	I/O	MPC	System Address bit 0	
2	SADD[1]	I/O	MPC	System Address bit 1	
3	SADD[2]	I/O	MPC	System Address bit 2	
4	SADD[3]	I/O	MPC	System Address bit 3	
5	SADD[4]	I/O	MPC	System Address bit 4	
6	SADD[5]	I/O	MPC	System Address bit 5	
7	GNDPWR				
8	SADD[6]	I/O	MPC	System Address bit 6	
9	SADD[7]	I/O	MPC	System Address bit 7	
10	V_{DD} PWR				
11	NSCS[0]	I/O	MPC	System Chip Select 0 - Active Low	1
12	NSCS[1]	O	MPC	System Chip Select 1 - Active Low	1
13	NSCS[2A]	O	MPC	System Chip Select 2A - Active Low	1
14	SADD[19]	O	MPC	System Address bit 19	
15	SDATA[0]	I/O	MPC	System Data bit 01	
16	SDATA[1]	I/O	MPC	System Data bit 11	
17	SDATA[2]	I/O	MPC	System Data bit 21	
18	SDATA[3]	I/O	MPC	System Data bit 31	
19	GNDPWR				
20	SDATA[4]	I/O	MPC	System Data bit 41	
21	SDATA[5]	I/O	MPC	System Data bit 51	
22	V_{DD} PWR				
23	SDATA[6]	I/O	MPC	System Data bit 61	

Table 1 - Pin descriptions

Cont…

All V_{DD} and GND pins must be connected to ensure reliable operation. Any unused input pins must be tied either high or low; no inputs should be left unconnected.

Pin No.	Signal Name	Type	Associated circuit block	Description	Notes
24	SDATA[7]	I/O	MPC	System Data bit 7	1
25	NSOE	I/O	MPC	System Output Enable, active low	1
26	NSWE[1]	I/O	MPC	System Write Enable bit 1, active low	1
27	NSWE[0]	I/O	MPC	System Write Enable bit 0, active low	1
28	SDATA[8]	I/O	MPC	System Data bit 8	1
29	SDATA[9]	I/O	MPC	System Data bit 9	1
30	V_{DD}	PWR			
31	SDATA[10]	I/O	MPC	System Data bit 10	1
32	SDATA[11]	I/O	MPC	System Data bit 11	1
33	GND	PWR			
34	SDATA[12]	I/O	MPC	System Data bit 12	1
35	SDATA[13]	I/O	MPC	System Data bit 13	1
36	SDATA[14]	I/O	MPC	System Data bit 14	1
37	SDATA[15]	I/O	MPC	System Data bit 15	1
38	SADD[18]	I/O	MPC	System Address bit 18	
39	SADD[17]	I/O	MPC	System Address bit 17	
40	SADD[16]	I/O	MPC	System Address bit 16	
41	GND	PWR			
42	SADD[15]	I/O	MPC	System Address bit 15	
43	SADD[14]	I/O	MPC	System Address bit 14	
44	V_{DD}	PWR			
45	SADD[13]	I/O	MPC	System Address bit 13	
46	SADD[12]	I/O	MPC	System Address bit 12	
47	SADD[11]	I/O	MPC	System Address bit 11	
48	SADD[10]	I/O	MPC	System Address bit 10	
49	SADD[9]	I/O	MPC	System Address bit 9	
50	SADD[8]	I/O	MPC	System Address bit 8	
51	SWAIT	I	MPC	System Wait input - allows wait-states to be inserted into the current Firefly clock cycle.	
52	NSUB	O	MPC	System Upper Byte, active low.	1,2
53	IEXTINT2	I	INTC	Interrupt source 2 input (for external interrupts).	
54	MULTI_FNIO	I/O	PCL	Multi-function Input / Output. Used to set Boot Up ROM area, and source either 100kHz square wave or System Clock.	
55	DISCIO	I/O	PCL	Discrete Input / Output. Used either as input or to source RF_Power_Down control signal or TIC.	3
56	RF_PLL_LOCK	I	INTC /PCL	PLL Lock Indicator input from RF section. When high this signal indicates that the PLL within the RF section is in lock and the master-clock inputs have stabilised.	
57	$A1V_{DD}$	PWR	SCG	V_{DD} Supply for CLK_T & CLK_I input block in the System Clock Generator. This pin should be well decoupled to pin 60 (GND) to ensure optimum noise immunity	
58	CLK_T	I	SCG	Master Clock Input from RF front end 40MHz 100mV rms.	4
59	CLK_I	I	SCG	Inverted Master Clock Input from RF front end: 40MHz 100mV rms.	4

Table 1 - Pin descriptions (continued)

Cont…

Pin No.	Signal name	Type	Associated circuit block	Description	Notes
60	GND	PWR			
61	SIGN0	I	CORR	Sampled Sign (polarity) data from RF front end.	
62	MAG0	I	CORR	Sampled Mag (amplitude) data from RF front end.	
63	SAMPCLK	O	CORR	Sample Clock output to the RF front end. Provides a 5·714MHz clock with a 4:3 mark to space ratio.	
64	POWER_GOOD	I	PCL	Power Monitor input, high for normal operation; low forces the GP4020 into Power Down mode.	
65	PR_XOUT	O	SCG	System Clock Oscillator - crystal output for 10 to 16MHz crystal.	
66	PR_XIN	I	SCG	System Clock Oscillator - crystal inputfor 10 to 16MHz crystal.	
67	TEST	I		*TEST select pin,used with TESTMODE (pin 74). Used for test purposes only and should be connected to GND in normal operation.*	5
68	V_{DD}	PWR			
69	TIMEMARK / TIC	O	1PPS	Timemark output. This pin can be used to produce a UTC-aligned 1 PPS output, or TIC output.	
70	IDDQTEST	I		*TEST select pin,used with TESTMODE (pin 74). Used for test purposes only and should be connected to GND in normal operation.*	
71	GND	PWR			
72	RTC_XIN	I	RTC	Real-time Clock Oscillator input for 32kHz crystal.	
73	RTC_XOUT	O	RTC	Real-time Clock Oscillator output for 32kHz crystal.	
74	TESTMODE	I		*TEST select pin,used with TEST (pin 67). Used for test purposes only and should be connected to GND in normal operation.*	5
75	NSRESET	I	PCL	System Reset input.	
76	U2TXD	O	UART2	UART 2 Transmit data output.	
77	U2RXD	I	UART2	UART 2 Receive data input.	3
78	U1TXD	O	UART1	UART 1 Transmit data output.	
79	U1RXD	I	UART1	UART 1 Receive data input.	3
80	PLLGND	PWR	SCGPLL	GND connection for PLL Block.	
81	PLLVDD	PWR	SCGPLL	V_{DD} connection for PLL Block.	
82	GND	PWR			
83	PLLAT1	O	SCGPLL	*System Clock Generator PLL Analog Test I/O. Reserved for TEST purposes only and should NOT be connected in normal operation.*	
84	NICE	I	JTAG/SSM MUTIPLEX	ARM7 operating mode and JTAG / SSM Signal Multiplex (pins 86, 87, 88, 89).	6
85	V_{DD}	PWR			
86	TCK/bdiag[0]/XReq	I/O	JTAG/SSM	JTAG Test Clock/SSM Diagnostic broadcast debug output bdiag[0]/System test control input XReq.	6
87	TDI/bdiag[1]/XWrite	I/O	JTAG/SSM	JTAG Test Data In/SSM Diagnostic broadcast debug output bdiag[1]/System Test control input X/Write.	6
88	TDO/bdiag[2]/XBurst	I/O	JTAG/SSM	JTAG Test Data Out/SSM Diagnostic broadcast debug output bdiag[2]/System test control input XBurst.	6

Cont…

Table 1 - Pin descriptions (continued)

Pin No.	Signal name	Type	Associated circuit block	Description	Notes
89	TMS/bdiag[3]/XCon	I/O	JTAG/SSM	JTAG Test Mode Select/SSM Diagnostic broadcast debug output bdiag[3]/System test control input XCon.	6
90	NTRST	I	JTAG/SSM	JTAG interface Reset or SSM debug interface multiplex (pins 86, 87, 88 and 89).	6
91	GPI0[7]/PLLDT1	I/O	GPIO/SCG PLL	General Purpose Input/Output 7. Can be multiplexed to SCG PLL Digital Test Output (PLLDT1).	3
92	GPIO[6]	I/O	GPIO	General Purpose Input/Output 6.	3
93	GPIO[5]/DISCOP	I/O	GPIO/CORR	General Purpose Input/Output 5. Can be multiplexed to DISCOP discrete output from correlator.	3
94	GND	PWR			
95	GPIO[4]/DISCIP1	I/O	GPIO/CORR	General Purpose Input/Output 4. Also directly connects to DISCIP1 on the 12-channel correlator.	3
96	GPIO[3]/BSIO_SS[1]	I/O	GPIO/BSIO	General Purpose Input/Output 3. Can be multiplexed to BSIO Slave Select[1].	3
97	GPIO[2]/BSIO_SS[0]	I/O	GPIO/BSIO	General Purpose Input/Output 2. Can be multiplexed to BSIO Slave Select[0].	3
98	V_{DD}	PWR			
99	GPIO[1]/BSIO_DATA	I/O	GPIO/BSIO	General Purpose Input/Output 1. Can be multiplexed to BSIO Data Input/Output.	3
100	GPIO[0]/BSIO_CLK	I/O	GPIO/BSIO	General Purpose Input/Output pin 0. Can be multiplexed to BSIO_CLK output.	3

Table 1 - Pin descriptions (continued)

NOTES

1. High impedance is achieved on pins 11 to 18, 20, 21, 23 to 29, 31, 32, 34 to 37 when either:
   (a) Data is not being written from GP4020.
   (b) POWER_GOOD (pin 64) is low.
   (c) Bit 1 (RF_PD) of POW_CNTL register is high.
   (d) Bit 10 (RF_SLEEP) of POW_CNTL register is high.
2. NSUB (pin 52) is the Upper Byte select output from the Memory Peripheral Controller, when single chip 16-bit memories with NUB and NLB inputs are used. NSUB maps to NUB and address line SADD[0] to NLB.
3. Input is tolerant to being driven with a +5V HIGH level, as well as +3·3V HIGH nominal level.
4. Both CLK_T (pin 58) and CLK_I (pin 59) should not have an external DC bias of GREATER than +1·7V . Direct connection from a GP2010/GP2015 RF front end is NOT possible, without bias-shift circuit (Figure 3).
5. TEST (pin 67) and TESTMODE (pin 74) are used together to set up manufacturing test modes for the GP4020, as shown in Table 2 (0 = GND, 1 = V_{DD}).

TEST (pin 67)	TESTMODE (pin 74)	Test function
0	0	Normal operation
1	0	Firefly Macrocell test mode
0	1	Firefly System test mode
1	1	UIM logic test mode

Table 2 - Test mode truth table

Details of ALL test modes are covered in section 2.10 of the Zarlink Semiconductor Firefly MF1 Core Design Manual.

NOTES (continued):

6. NICE (pin 84) and NRST (pin 90) control a number of operation modes and a debug on signal multiplex on pins 86 to 90 as follows:

NICE = low	ARM7TDMI in ICE mode. ARM7TDMI will not access memory unless instructed by the JTAG interface. NTRST (pin 90) set Low will reset the JTAG.
NICE = High	ARM7TDMI in Normal mode. ARM7TDMI does not effect the reset on the JTAG inteface. However, a reset of Firefly will also reset the JTAG.

NTRST (pin 90) has a reset and signal-multiplex function, dependent on the state of NICE (pin 84):

(i) NICE = Low:
JTAG debug signals connected to pins 86, 87, 88, 89 & 90, as follows:

Pin 86 = TCK	=	JTAG clock in
Pin 87 = TDI	=	JTAG data in
Pin 88 = TDO	=	JTAG data out
Pin 89 = TMS	=	JTAG mode select in
Pin 90 = NTRST	=	Active low reset to JTAG interface (JTAG interface also reset when Firefly MF1 is reset)

(ii) NICE = High and NTRST = High:
Normal mode of operation for GP4020. System Services Module Broadcast Diagnostic debug output signals connected to pins 86, 87, 88, 89 as follows:
Pin 86 = bdiag[0]
Pin 87 = bdiag[1]
Pin 88 = bdiag[2]
Pin 89 = bdiag[3]
Diagnostic mode must have been set-up using the Diagnostic Configuration Registers within Firefly MF1. Refer to Section 8 of Firefly MF1 Core Design Manual (DM5003), from Zarlink Semiconductor, for more information.

(iii) NICE = High & NTRST = Low:
Firefly MF1 System Test Control input signals connected to pins 86, 87, 88, 89 as follows:
Pin 86 = Xreq
Pin 87 = XWrite
Pin 88 = Xburst
Pin 89 = XCon

System test inputs are used in Firefly MF1 macrocell test mode for manufacturing test. Refer to Section 2.10 of Firefly MF1 Core Design Manual (DM5003), from Zarlink Semiconductor, for more information.

Glossary:

1PPS	1 Pulse Per Second
ARM®	Advanced RISC Machines
ARM7TDMI™	ARM7 microprocessor with Thumb, Debug, fast Multiplier and ICE Breaker Extensions
BµILD	Bus for µController Integration in Low-Power Designs
B_CLK	BµILD bus system clock
BSIO	BµILD Serial Input / Output
CORR	12-channel Correlator
DMAC	Direct Memory Access Controller
Firefly MF1	Zarlink Semiconductor microcontroller cell, based on ARM7TDMI, DMAC, INTC, MPC, SYSTIC and UART
GPIO	General Purpose Input / Output
GPS	Global Positioning System
ICE	In Circuit Emulation
INTC	Interrupt Controller
MPC	Memory Peripheral Controller
PCL	Peripheral Control Logic
PLL	Phase Locked Loop
RAM	Random Access Memory
ROM	Read Only Memory
RTC	Real Time Clock
SCG	System Clock Generator
SSM	System Services Module
SYSTIC	System Timer / Counter module
TIC	Timer / Counter
UART	Universal Asynchronous Receiver/ Transmitter
UIM	Up-Integration Module
WDOG	Watchdog

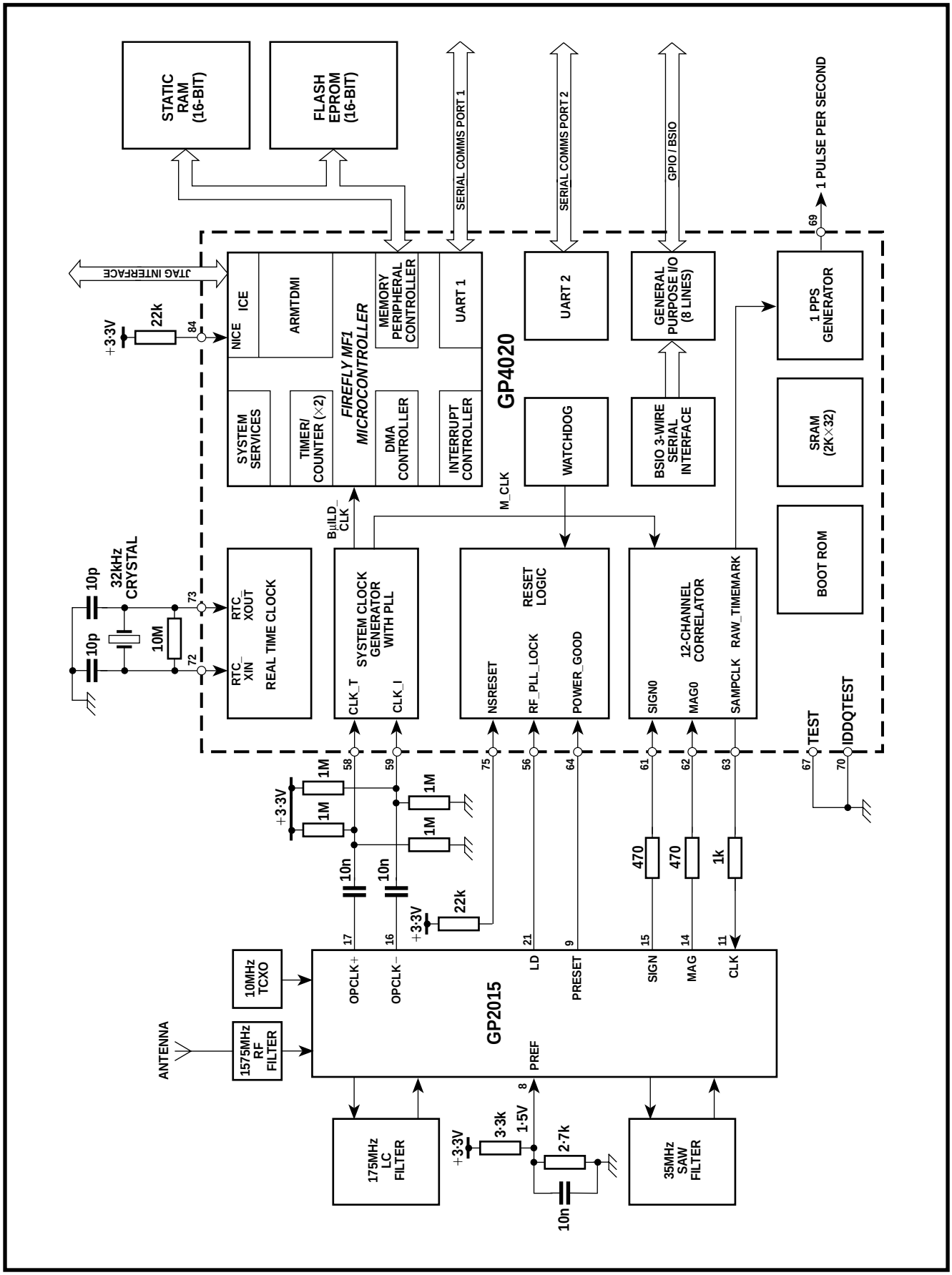


Figure 3 - Block diagram of a typical GP4020-based GPS receiver

Typical GPS Receiver

Figure 3 shows a typical GPS receiver employing a GP2015 RF front end and a GP4020 correlator.

The RF section, GP2015, performs down conversion of the L1 (1575·42MHz) signal for digital baseband processing. The resultant signal is then correlated in the GPS correlator within the GP4020 with an internally generated replica of the satellite PRN code to be received. Individual codes for each channel may be selected independently to enable acquisition and tracking of up to 12 different satellites simultaneously.

The results of the correlations form the accumulated data and are transferred to the microprocessor to give the broadcast satellite data (the Navigation Message) and to control the software signal tracking.

Device Description

The GP4020 is a complete baseband processor for Navstar GPS C/A code signals. It incorporates a 12-channel GPS correlator, a Zarlink Firefly MF1 microcontroller core (incorporating the ARM7TDMI Thumb microprocessor), Real Time Clock, 8KBytes of on-chip SRAM and a boot ROM. The GP4020 uses a fully configurable memory interface, allowing the use of 16-bit external memory. A block diagram of the GP4020 is shown in Figure 1.

The GP4020 GPS Baseband processor features:

- Firefly MF1 Core including ARM7TDMI Microprocessor
- 12-channel Navstar GPS C/A code correlator
- 1KByte Onboard Boot ROM
- 8KByte Onboard SRAM
- 8-bit General Purpose I/O
- Debugging Serial Access Ports - JTAG or SSM
- System Timer / Counters
- Real Time Clock
- BSIO: 3-wire serial interface
- Watchdog
- 1Pulse-Per-Second output, with 25ns resolution
- Flexible system Clock Generator - can use clock source from a crystal or from RF front end TCXO

ARM Processor (ARM7TDMI)

The ARM7TDMI is a 32-bit RISC microprocessor core designed by Advanced RISC Machines (ARM). It uses a series 7 microprocessor core, with the following functional extensions:

- Thumb (16-bit) instruction set
- Debug interface using J-TAG
- Fast Multiplier
- Embedded In-Circuit Emulation capability

The ARM7TDMI is object code compatible with all earlier ARM6 and ARM7 based products. The ARM7TDMI is a fully static design and as such consumes dynamic power only when clocked.

Boot ROM

The GP4020 BOOT ROM contains code which is executed every time there is a complete system reset (i.e. when main power has been removed from the GP4020).

The code installed on the BOOT ROM, allows the GP4020 to undertake either of 2 functions after a complete reset:

- Run External Flash EPROM from the EPROM base address.
- Load into the internal SRAM a unique program via the UART1 input. This could be used for test purposes, although the target use of this facility is to allow for field upgrades of GPS receiver firmware, in conjunction with a Flash EPROM.

BµILD Bus

This is a modular bus architecture and specification, via which all on-chip modules communicate with each other. These modules can either be bus masters or slaves. A bus master can initiate a bus access, generate addresses and control read or write transfers. A bus slave responds to a bus master request when selected by the system address decoder, and may, if required, assert a wait signal on the bus until the relevant data transfer has been completed. All internal data transfers on the module bus are single cycle. The Firefly MF1 micro-controller has three modules that are capable of operating as Bus masters. These are the ARM7TDMI Core, DMAC and SSM, described below.

BµILD Serial Input Output (BSIO)

This module produces a 2-channel 3-wire serial interface for up to 2 external ‘Slave’ serial interface devices (e.g. serial EEPROM). It provides both Micro-wire Interface and Serial Peripheral Interface (SPI) compatibility.

12-Channel Correlator

This module contains 12 channels of PRN code correlators for spread-spectrum correlation of 12 simultaneous signals. Each channel contains an independent carrier DCO to allow independent mix down of a satellite signal to baseband before code correlation occurs. The correlator is designed to extract data modulated at a nominal chipping rate of 1·023Mbps, and can be used on both Navstar C/A code GPS signals and Inmarsat WAAS codes.

DMA Controller (DMAC)

Two DMA engines are available on the microcontroller. These are configured as a pair to provide a memory-to-memory DMA capability between any 2 locations in the ARM7TDMI memory space. They may be used independently for high speed fly-by transfers between UART1 (or UART2) and either on-chip or off-chip locations.

Single or multiple byte transfers (Demand or Burst Mode) are supported and may be word, half word or byte wide.

Embedded Microcontroller Debug Options

The Firefly MF1 Core incorporates three sophisticated methods of hardware and software debug. The options are:

- Embedded ICE, accessed via the ARM7TDMI JTAG interface (Multi ICE access also possible)
- Angel Debug Monitor
- Logic Analyser coupled with an Inverse Assembler, accessed via the SSM debug interface

The GP4020 can use any of these options, but special emphasis has been placed on the Embedded ICE and Logic Analyser options. The JTAG and SSM debug interfaces are multiplexed onto the same pins, and can be selected by setting NICE (pin 84) high for SSM, or low for JTAG.

Firefly MF1 Microcontroller core

The Firefly MF1 Microcontroller is an Embedded Microcontroller core developed by Zarlink Semiconductor. It combines the processing power of the ARM7TDMI microprocessor with a number of peripheral components:

- Direct Memory Access Controller (DMAC)
- Interrupt Controller (INTC)
- Memory Peripheral Controller (MPC), incorporating Up-Integration Module (UIM)
- System Services Module (SSM)
- System Timer/Counter (SYSTIC)
- Universal Asynchronous Receiver / Transmitter (UART)

Interrupt Controller (INTC)

The ARM7TDMI core accepts two types of interrupt: Normal (IRQ) and Fast (FIQ). All Interrupts can be switched between types, depending upon the relative priorities required. The INTC is the central control logic that decodes the priority level and handles interrupt request signals from a total of 8 fixed pre-defined, internal sources and a number of external sources.

General Purpose Input Output (GPIO)

This module provides 8 I/O pins, which may be bit or byte addressed and configured in a latched or transparent mode.

External Interrupts can be set for edge or level sensitivity with a polarity option. To minimise interrupt latency, there is a hard-wired priority scheme for each channel for both FIQ and IRQ; alternatively this can be ignored and the priority assessment handled in software.

Memory/Peripheral Controller (MPC)

The MPC ensures the correct multiplexing of data is applied for bus transfers between 8, 16 or 32-bit on-chip or off-chip peripherals. Four different contiguous memory areas are available, each with an address range of 1 MByte, with individually programmable wait and stop state generation. A SWAP function allows memory area 1, which is addressed at system reset, to be switched with memory area 4. This allows, for example, booting from ROM and then switching memory area 1 to address SRAM so that time-critical software and interrupt routines can operate from fast memory.

Peripheral Control Logic (PCL)

The GP4020 incorporates some specific control logic, which is used to control a number of functions:

- System Reset Control
- System Power-down, Sleep and Wake-up Control
- System Status and Control Registers
- Signal input/output multiplex control

RAM

The GP4020 contains 8KBytes (configured as 2K332-bit) of high-speed (6ns) Static RAM. This can be used for either:

- Non-volatile storage of GPS data (Almanac, Ephemeris, Position and Receiver Clock Offset), while the receiver power is disabled

- A High-speed Interrupt Service Routine, while the GP4020 is powered up

The internal SRAM appears at GP4020 Base Address 0x60000000, served by the MPC Memory Area 4. An MPC SWAP function can swap this memory space with 0x00000000 if required.

Since the memory is high-speed, it can be accessed with Zero wait-states through the Memory Peripheral Controller. Refer to section on the Memory Peripheral Controller for more information.

Real Time Clock (RTC)

The GP4020 Real Time Clock uses an external 32kHz crystal to give an indication of time to the GP4020 chip, when the device is in Reset / Power Down. If a backup battery is included in a GPS receiver using the GP4020, the RTC will continue to operate regardless of the reset state of the rest of the device.

The RTC is incremental, which means that the number of seconds from a reset point are accumulated, rather than a record of Gregorian date.

System Clock Generator (SCG)

The GP4020 System Clock Generator is used to provide 2 system clocks:

- The M_CLK for the 12-channel Correlator; this is derived from the CLK_T and CLK_I inputs from the RF front end device and MUST be 40MHz. This clock is fundamental to the correlator function, and must be phase-locked to the RF front end.

- The BµILD_CLK for ALL components on the BµILD Bus; this can be derived from M_CLK (see above) in conjunction with a PLL and a divider to generate a wide range of clock frequencies. In this way, the BµILD_CLK can be phase-locked to the RF front end. The clock can also be derived from an independent crystal source.

System Services Module (SSM)

The System Services Module (SSM) ensures correct bus operation through a number of modes (reset, initialisation, debug, etc). It provides diagnostic broadcast of address and data for internal transfers along with information about the current operating mode.

Additionally the SSM System Configuration Register controls the operating mode of the GP4020.

Specifically the System Services Module performs the following functions:

- Control the BµILD bus operational mode
- Arbitrate amongst competing resources for BµILD bus mastership
- Interface to external bus masters and manufacturing testers
- Control the activities of all BµILD bus modules during system debug activity.
- Broadcast information about BµILD bus activity for external diagnostics
- Hold BµILD bus logic levels when no other bus-master is driving
- Register System Configuration data

System Timer/Counters (SYSTIC)

Two dual independent 32-bit timer/counters, with an 8-bit pre-scaler capability for each counter, are provided (Timers 1A, 1B, 2A and 2B). These are synchronous to the system clock and may be polled, or set-up to generate interrupts on over-run, with auto-reload.

The TIC functions provided by this module are part of the Firefly MF1 core. Timer 1 (TIC1) appears at GP4020 Base Address 0xE000 E000, and Timer 2 (TIC2) appears at Address 0xE000 F000. TIC enable (TEN) lines are not available externally on this version of the GP4020, but are tied low on-chip. The TIC functions can be made available by setting the External enable polarity bit of the TIC Control/Status register to a logic ‘0’.

Whilst these timer/counters are NOT required by the GPS function in a GP4020 based GPS receiver, full programming details of the programming of the System Timer/Counter can be found in Section 7 of the Firefly MF1 Core Design Manual.

1PPS Timemark Generator

The GP4020 Timemark generator is used in conjunction with software to produce a 1 Pulse Per Second (1PPS) output pulse, which is aligned to Universal Time Co-ordinated (UTC) to a resolution of 25ns. The accuracy of time transmitted from the Navstar GPS space segment is very high, and this can be used to provide a mobile timing reference to a similar accuracy.

Up Integration Module (UIM)

The Up Integration Module provides a series of internal connection ports, which mimic the MPC external interface. This allows the Firefly MF1 to communicate with the Application Specific Logic used in the GP4020, as though it was external to the chip, hence it acts as a transparent interface.

Universal Asynchronous Receive/Transmit (UART1 and UART2)

The full duplex asynchronous channels of UART1 and UART2 provide RS232 type interfaces, which support an XON/XOFF software protocol. The Receive and Transmit channels are double buffered. The UARTs may be polled, or may use an interrupt scheme for module bus transfers. An internal Baud rate generator in each UART can provide selectable data rates, derived from on-chip sources for an Rx/Tx pair.

Directly-triggered DMA transfers with each UART are also possible without the need for CPU intervention.

Watchdog (WDOG)

The GP4020 Watchdog can be used to detect hardware or software run-time errors, and reset the system. The processor is required to reset the watchdog periodically; failure to do so will result in a chip-wide reset.

Electrical Characteristics

T_{AMB} = -40°C to +85°C, V_{DD} = +3·0V to +3·6V (+3·3V nominal). The input thresholds and output voltage limits for the logic signal pins are tested and guaranteed by production test. All other parameters are guaranteed by characterisation and design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise specified. Use in conjunction with the GP4020 GPS Baseband Processor Design Manual (DM5280).

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range		3·0		3·6	V	
Battery backup voltage	V_{BATT}	2·7			V	
Supply Current						
Full chip	I_{DD}			100	mA	Simulated. Firefly BµlLD_CLK = 30MHz, outputs loaded with 50pF, 12 tracking correlator channels
40MHz low level differential input	I_{LLDI}			4·4	mA	Enabled
				100	nA	Disabled
Processor clock oscillator	I_{PRX}			0·9	mA	Enabled
			< 1 0 0		nA	Disabled
Phase locked loop	I_{PLL}			1·0	µA	Disabled
			2·9		mA	Enabled - F_{OUT} = 30MHz, Mult Factor = 3
			3·4		mA	Enabled - F_{OUT} = 60MHz, Mult Factor = 6
			4·5		mA	Enabled - F_{OUT} = 1 20MHz, Mult Factor = 12
			6·2		mA	Enabled - F_{OUT} = 240MHz, Mult Factor = 24
Real time clock	I_{RTC}		3·27	7·75	µA	
Firefly MF1 microcontroller	I_{FMF1}		0·7		mA/MHz	
Firefly MF1 microcontroller						
Operating frequency	$F_{BµILD}$		20	31·25	MHz	Bµild_CLK – external memory at >1 wait state or internal memory at 0 wait state.
Operating frequency	$F_{BµILD}$		20	27.5	MHz	Bµild_CLK – external memory access at 0 wait state.
Output capacitance				50	pF	Total external load, all outputs and I/Os

Cont…

Electrical Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
40MHz Low Level Differential Input						
Input voltage bias	V_{DBIAS}	0		1·715	V	Min. V_{DD} = 3·0V Note 1
Differential input voltage	V_{DIFIN}	100			mV	
Input differential hysteresis	V_{DIFHYS}	12		24	mV	
Input clock frequency	F_{DIFIN}		40	150	MHz	40MHz from RF front end
Input capacitance	C_{DIFIN}		5		pF	Not including package
Power-on delay				150	ns	
Processor Clock Oscillator						
Frequency	F_{PRXIN}	10		16	MHz	Correct external components
Start up time	T_{PRXSU}		10		ms	Across frequency range
Mark:space		45	50	55	%	Across all conditions
Transconductance	g_m	1·0	2·24	4·4	mA/V	
Output impedance	Z_O		93		kΩ	
Feedback resistance	R_F		220		kΩ	
Phase Locked Loop						
Input frequency	F_{PLLIN}	10		20	MHz	
Output frequency	F_{PLLOUT}	10		250	MHz	Can be divided down by 1,2,4 or 8 for optimal BµILD_CLK freq.
Duty cycle		45	50	55	%	
Phase alignment offset (falling edges of CLKINB, CLKFBKB)				+-0·2	ns	
Phase Alignment Jitter				+-0·25	ns	Note 2
Phase Jitter				+-0·15	ns	Cycle-cycle edge jitter Note 2
CLKINB to CLKOUTB delay			0·43		ns	In clock bypass mode
PLL Settling Time	T_{PLLSET}		147		µs	In clock synchronisation mode
Real Time Clock						
Crystal frequency	F_{RTC}		32·768		kHz	Correct external components
Start up time	$T_{RTCSTART}$		400		ms	Across frequency range
Transconductance	G_{MRTC}		9·56		µA/V	
Output impedance	Z_{ORTC}		422		MΩ	
Feedback resistance	R_{FRTC}		10		MΩ	External component
BµILD Serial Input / Output (BSIO) 3-wire Bus Interface						
BSIO_CLK output frequency	F_{SEROF}			10	MHz	
Serial clock output low period	T_{SERCL}	40			ns	
Serial clock output high period	T_{SERCH}	40			ns	
Serial clock output rise time	T_{SERCR}			10	ns	
Serial clock output fall time	T_{SERCF}			10	ns	
Serial data output delay	T_{SERDOD}	-20		20	ns	SEROUT ref SERCLK
Serial enable output delay	T_{SEREOD}	-20		20	ns	SERSEL ref SERCLK
Serial chip select enable to first clock edge delay	T_{SERCDC}	70			ns	
Serial last clock edge delay to chip select disable	T_{SERCEC}	70			ns	

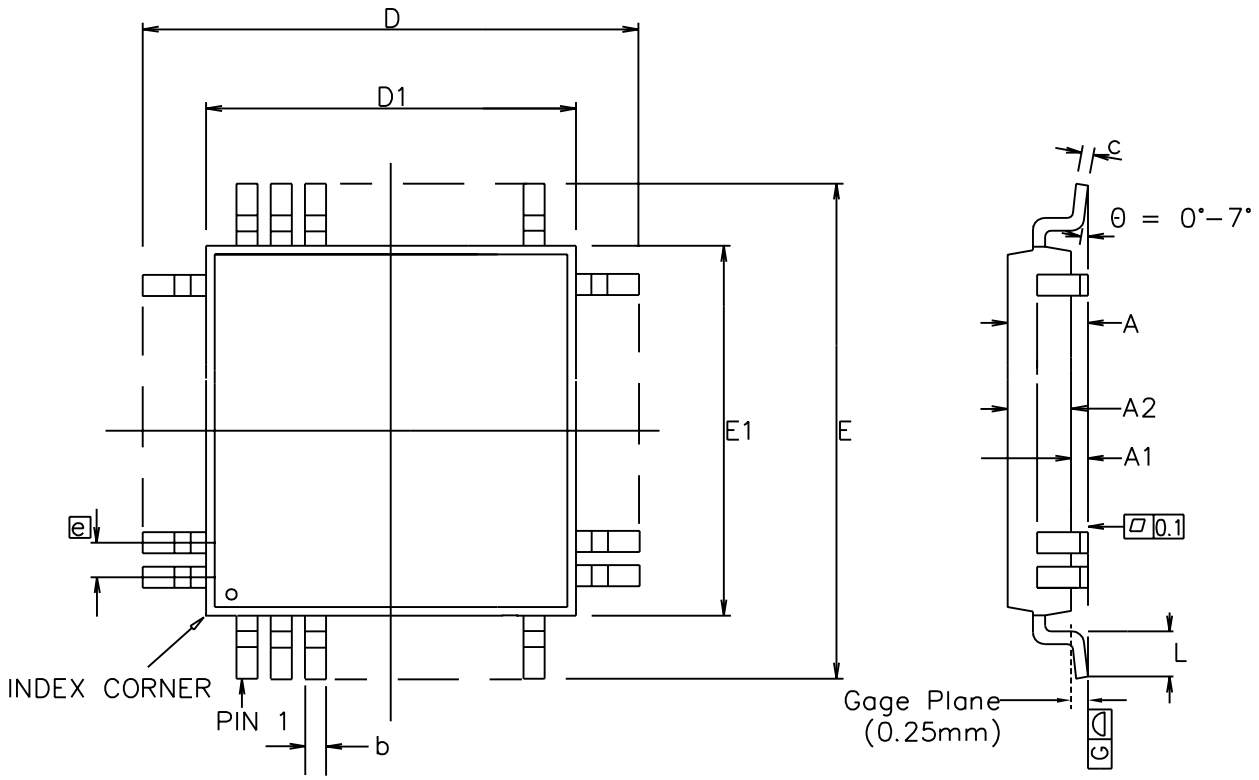
Cont…

NOTES

1. The input pair CLK_T, CLK_I may be driven by a low amplitude differential sinewave from an RF Front-end. Direct DC connection to a GP2010 or GP2015 RF front end is NOT possible, as the maximum DC bias from these devices is in excess of maximum input bias limit.
2. Jitter is dominated by supply-noise effects. Users must keep on-chip supply noise below 1Vp-p by the use of low noise outputs and as many supply pins as possible.

Electrical Characteristics (continued)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
General Purpose Input/Output (GPIO)						
Output delay	T_{GPOD}			20	ns	GPIO[7:0]
Input set-up time	T_{GPIS}	20			ns	GPIO[7:0]
Input hold time	T_{GPIH}	10			ns	GPIO[7:0]
UARTs						
Standard Baud rate	B_{DPUS}	1·2		115·2	kBaud	U1/2TXD, U1/2RXD
Reset logic						
Input reset pulse width		100			ns	NSRESET input to cause reset of whole chip



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	1.60		– – –	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	16.00 BSC			0.630 BSC	
D1	14.00 BSC			0.551 BSC	
E	16.00 BSC			0.630 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	100				
ND	25				
NE	25				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BED Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/023 (Swindon)

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APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

GP / B

Package Code QC

Package Outline for 100 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint

GPD00253

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