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# ECE 153B Lab 1

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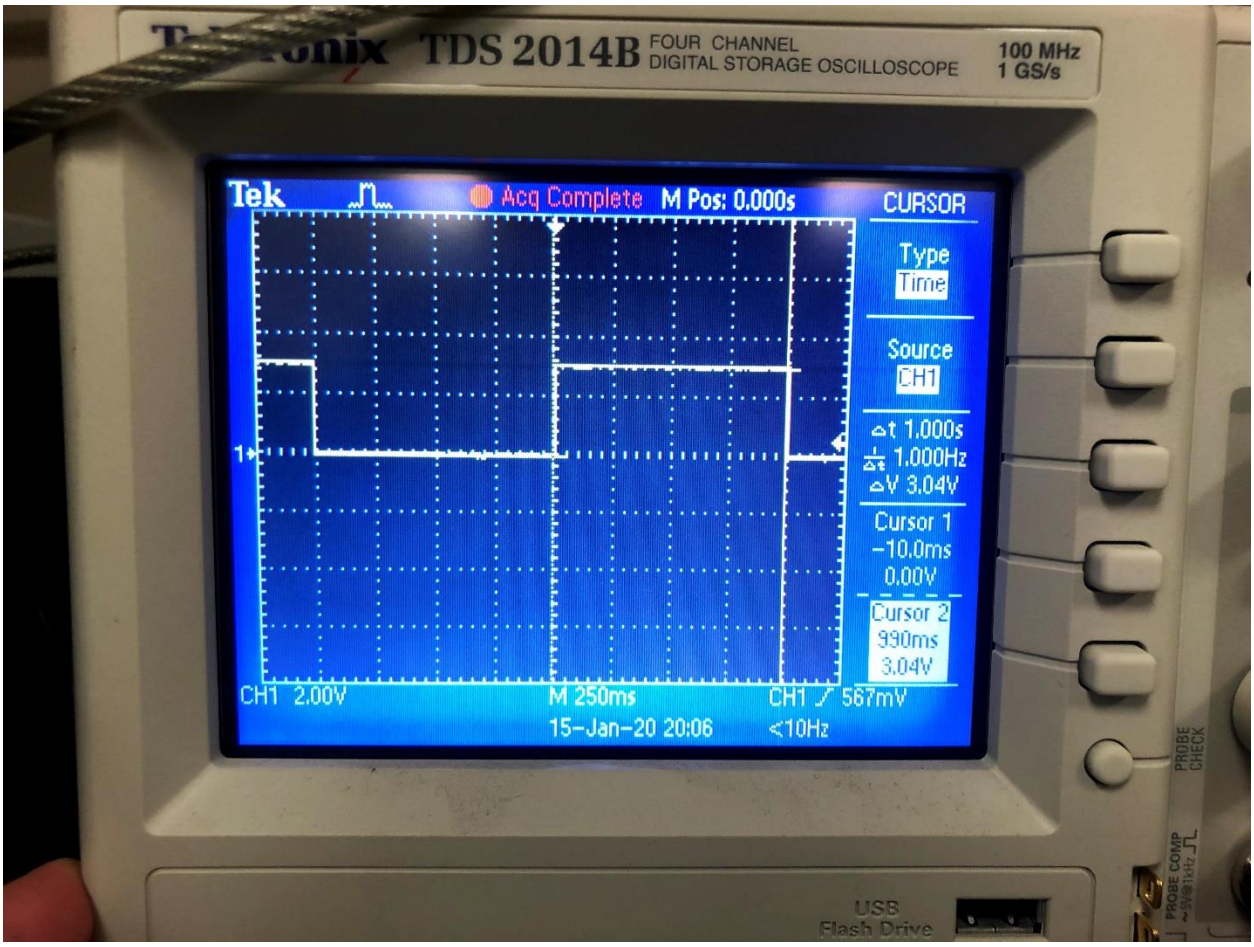
Question 1:

The time delay measured on the oscilloscope is exactly 1 second, accurate to the tenth of a millisecond. (-10 ms to 990 ms on oscilloscope)




Question 2:

Because the measured value and the expected value are both 1 second, the percent error in our RC oscillator is 0%.

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Question 3:

The address of the SysTick_Handler() function is 0x080003A4.

```
    42:          ++msTicks;
0x080003A4 4802      LDR           r0,[pc,#8]   ; @0x080003B0
```

Keil Debug Environment

Question 4:

The exception number of the SysTick_Handler() function is 15, as shown by the ISR field. This number represents the entry in the interrupt vector table that contains the address of the SysTick_Handler() interrupt.

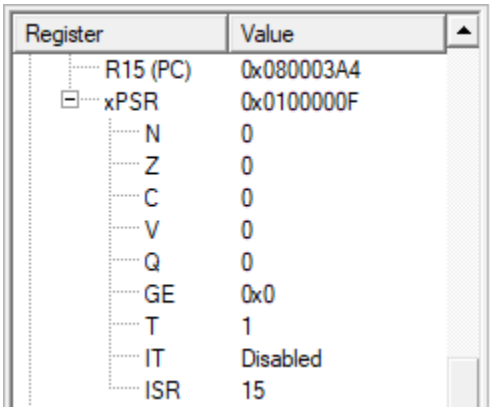


**Table 2-5 IPSR bit assignments**

| Bits | Name | Function |
|---|---|---|
| [31:9] | - | Reserved |
| [8:0] | ISR_NUMBER | This is the number of the current exception:<br>0 = Thread mode<br>1 = Reserved<br>2 = NMI<br>3 = HardFault<br>4 = MemManage<br>5 = BusFault<br>6 = UsageFault<br>7-10 = Reserved<br>11 = SVCall<br>12 = Reserved for Debug<br>13 = Reserved<br>14 = PendSV<br>15 = SysTick<br>16 = IRQ0. |

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Question 5:

The interrupt number of the SysTick function, as described in CMSIS, is -1.

```
84  typedef enum
85  {
86  /******  Cortex-M4 Processor Exceptions Numbers ***********************************************************/
87    NonMaskableInt_IRQn        = -14,    /*!< 2 Cortex-M4 Non Maskable Interrupt                                */
88    HardFault_IRQn             = -13,    /*!< 3 Cortex-M4 Hard Fault Interrupt                                  */
89    MemoryManagement_IRQn      = -12,    /*!< 4 Cortex-M4 Memory Management Interrupt                           */
90    BusFault_IRQn              = -11,    /*!< 5 Cortex-M4 Bus Fault Interrupt                                   */
91    UsageFault_IRQn            = -10,    /*!< 6 Cortex-M4 Usage Fault Interrupt                                 */
92    SVCall_IRQn                = -5,     /*!< 11 Cortex-M4 SV Call Interrupt                                    */
93    DebugMonitor_IRQn          = -4,     /*!< 12 Cortex-M4 Debug Monitor Interrupt                              */
94    PendSV_IRQn                = -2,     /*!< 14 Cortex-M4 Pend SV Interrupt                                    */
95    SysTick_IRQn               = -1,     /*!< 15 Cortex-M4 System Tick Interrupt                                */
```

stm32l476xx.h

Question 6:

The default priority for interrupts that are configurable, including SysTick_Handler(), is 0. A lower priority value indicates higher urgency.

If software does not configure any priorities, then all exceptions with a configurable priority have a priority of 0. For information about configuring exception priorities see

- *System Handler Priority Registers* on page 4-21
- *Interrupt Priority Registers* on page 4-7.

Question 7:

No, the SysTick interrupt is not enabled by default.

Question 8:

The maximum interrupt time interval between two consecutive SysTick interrupts is 8.39 seconds.

$$\left| \frac{1}{\frac{16 \cdot 10^6}{8}} \cdot \left(2^{24}\right) \right|$$

$$= 8.388608$$

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Question 9:

The GPIO Output Speed determines the slew rate being used for the port. The default GPIO speed is 00 = Low Speed. As the output speed increases, the slew rate increases as well.



### 9.4.3 GPIO port output speed register (GPIOx_OSPEEDR) (x = A..H)

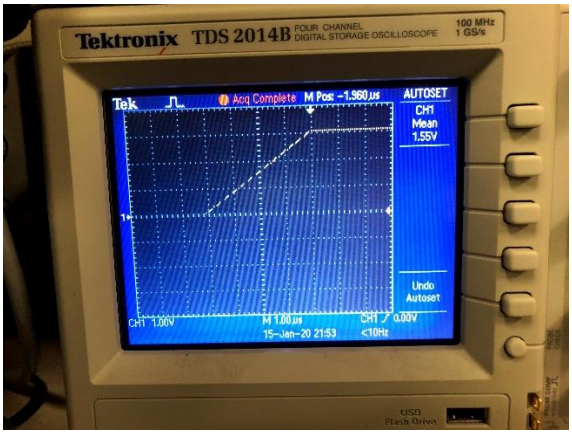
Address offset: 0x08

Reset value:

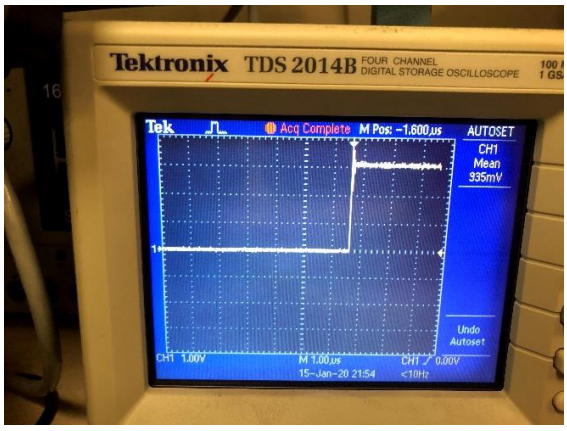
- 0x0C00 0000 for port A
- 0x0000 0000 for the other ports

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OSPEED15 [1:0] | | OSPEED14 [1:0] | | OSPEED13 [1:0] | | OSPEED12 [1:0] | | OSPEED11 [1:0] | | OSPEED10 [1:0] | | OSPEED9 [1:0] | | OSPEED8 [1:0] | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OSPEED7 [1:0] | | OSPEED6 [1:0] | | OSPEED5 [1:0] | | OSPEED4 [1:0] | | OSPEED3 [1:0] | | OSPEED2 [1:0] | | OSPEED1 [1:0] | | OSPEED0 [1:0] | |
| rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw | rw |

Bits 2y+1:2y **OSPEEDy[1:0]**: Port x configuration bits (y = 0..15)
These bits are written by software to configure the I/O output speed.
00: Low speed
01: Medium speed
10: Fast speed
11: High speed
*Note: Refer to the device datasheet for the frequency specifications and the power supply and load conditions for each speed.*




GPIO Speed 00 (Low Speed) shows a lower slew rate.




GPIO Speed 11 (High Speed) shows a higher slew rate.