Analysis

Using the method described above, these were the I_{DS} versus V_{DS} curves obtained for the NMOS circuit using V_{GS} values ranging from V_{GS} = 0 V to V_{GS} = 8 V in 2 V intervals.

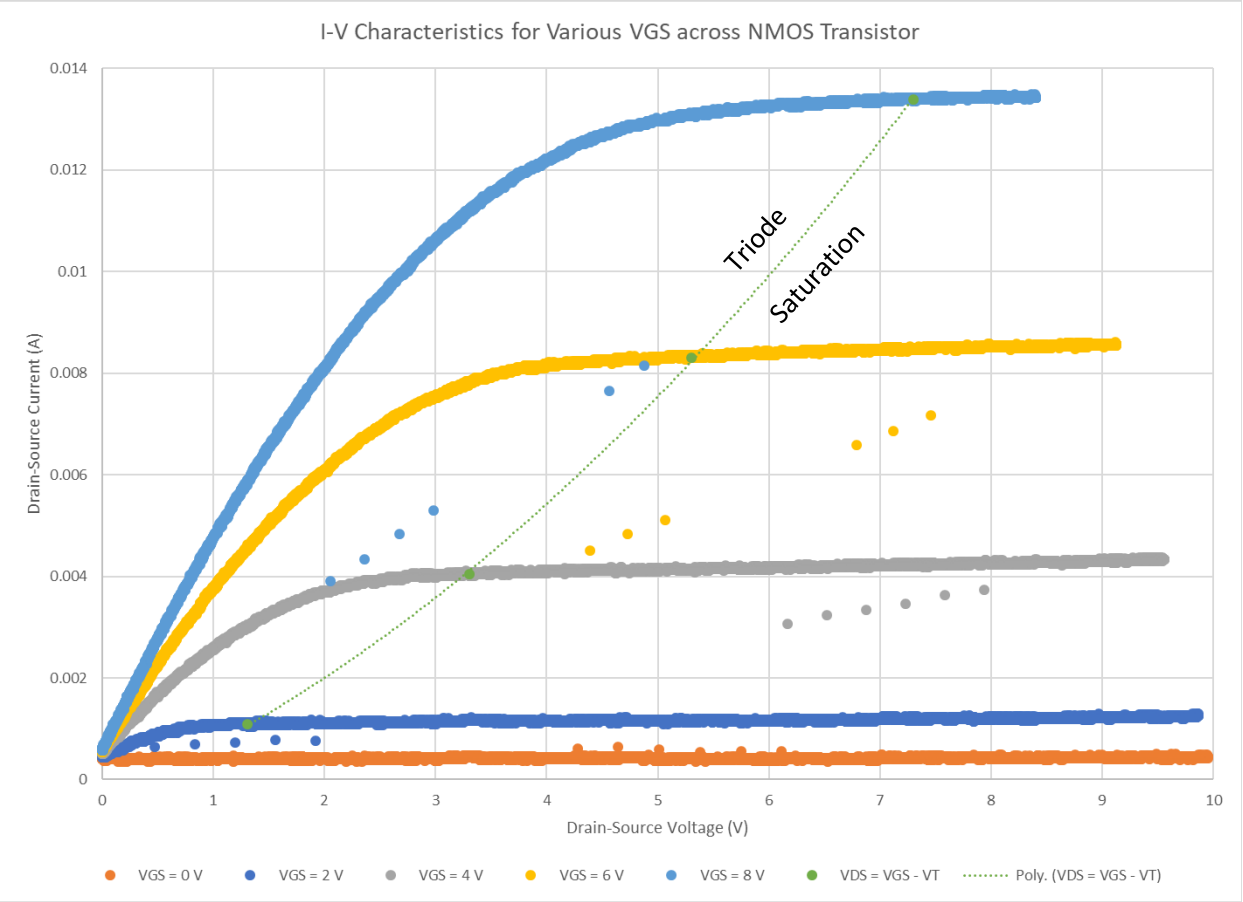

Figure 4: I-V Characteristics for Various Gate-Source Voltages (0V to 8V) across NMOS Transistor

We can observe all three MOSFET operation modes in this graph.

Cutoff occurs when the gate-source voltage is less than the threshold voltage, as shown in Table 1. In this scenario, the case where V_{GS} = 0 V exhibits this behavior, since 0 V is less than the NMOS's V_T value of 0.7 V. This is shown in Figure 4 as a horizontal line of zero current.

The triode region is any point to the left of the triode-saturation border, denoted by the green line in Figure 4. We can see that current in the triode region is parabolic, confirming the behavior modeled by the current equation in Table 1.

The saturation region is any point to the right of the triode-saturation border. We can see that the current is almost horizontal for all curves in this region, confirming the assumption that the MOSFET does not have any dependence (in this case, very little) on the drain-source voltage.

These were the I_{DS} versus V_{DS} curves obtained for the NMOS circuit using V_{GS} values ranging from V_{GS} = 0 V to V_{GS} = 2 V in 0.2 V intervals.

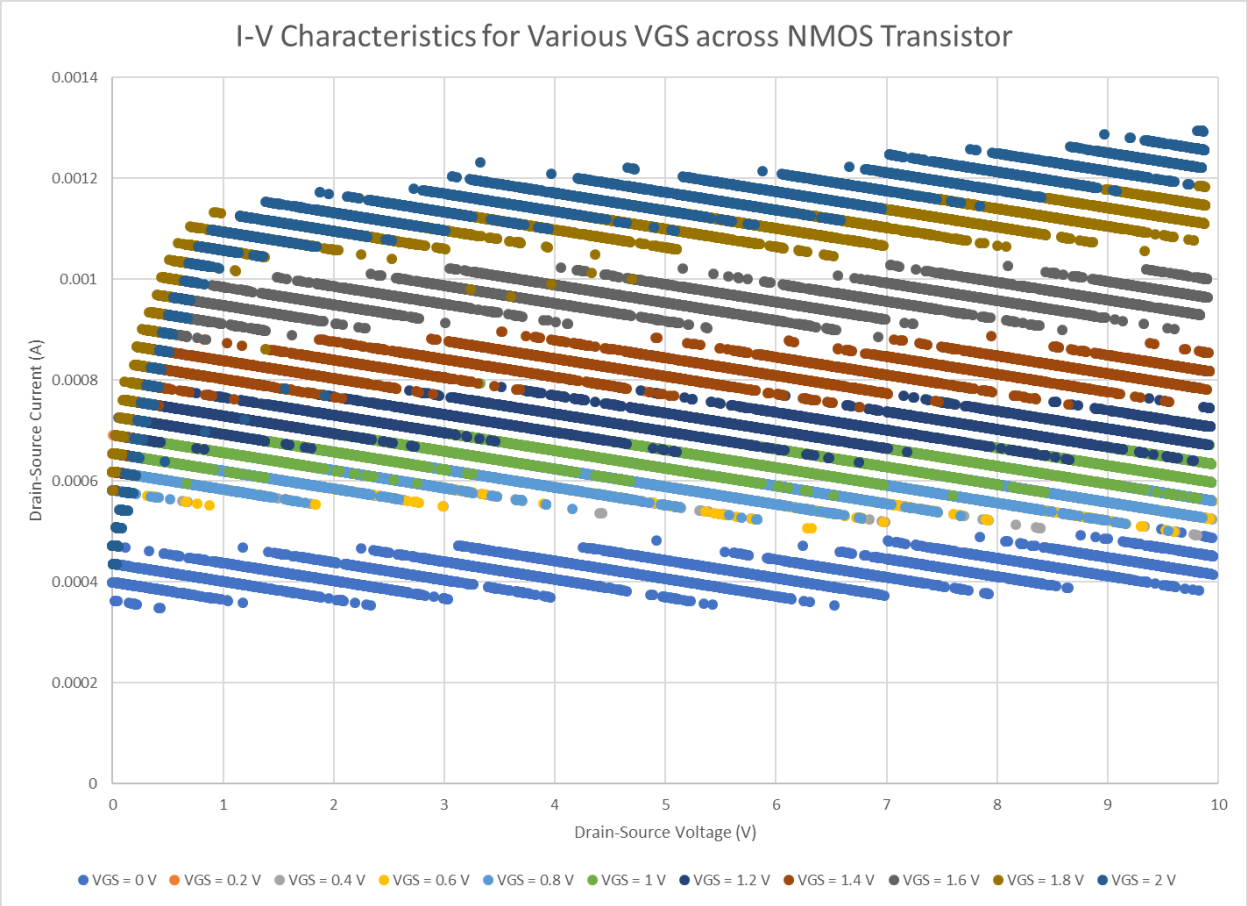

Figure 5: I-V Characteristics for Various Gate-Source Voltages (0V to 2V) across NMOS Transistor

Although these curves exhibited much more noise compared to those in Figure 4, the MOSFET operation modes can also be observed here.

We can notice that the curves for V_{GS} = 0.2 V, V_{GS} = 0.4 V, V_{GS} = 0.6 V, and V_{GS} = 0.8 V, overlay each other around I = 0.0006 A. This is because most of the V_{GS} values fall under the threshold voltage, and the graph is just starting to rise for V_{GS} = 0.8 V. The other curves confirm the trend that increasing V_{GS} values result in larger I_{DS} values at all points.

These were the I_{DS} versus V_{DS} curves obtained for the PMOS circuit using V_{GS} values ranging from V_{GS} = 0 V to V_{GS} = 8 V in 2 V intervals.

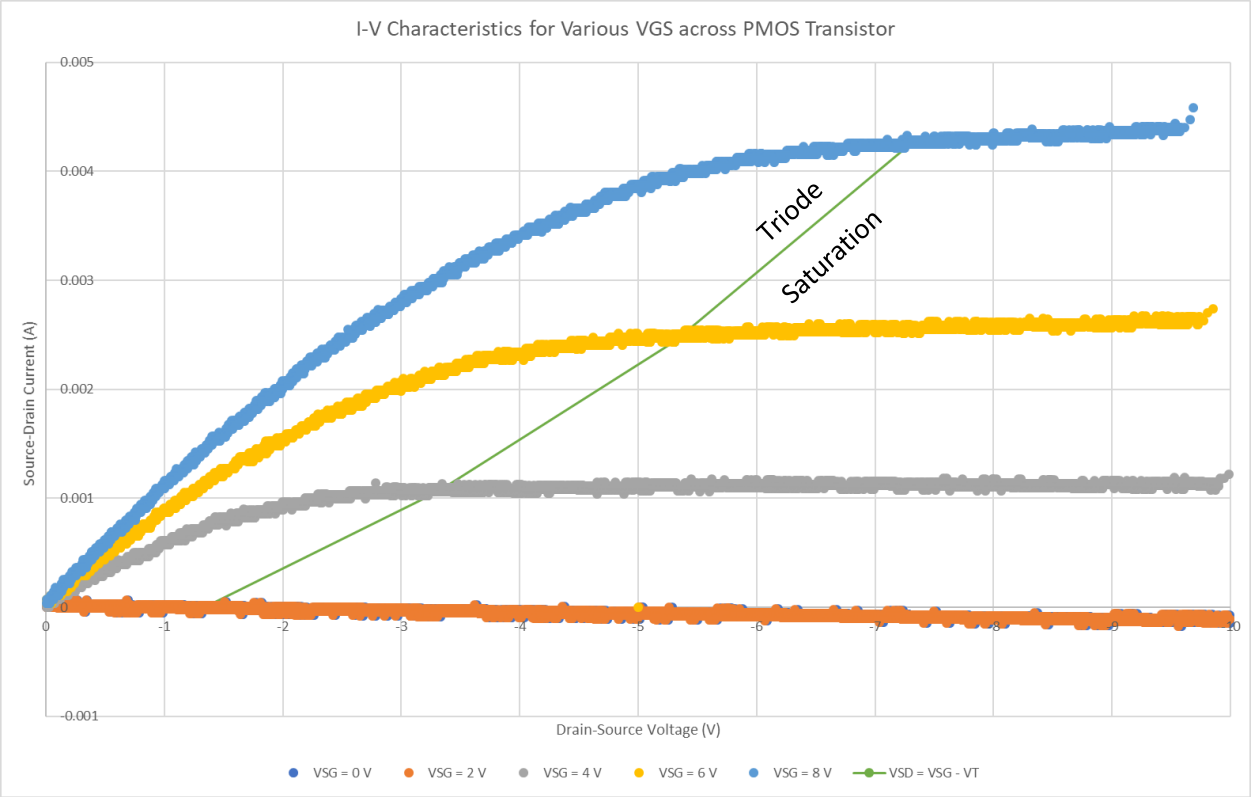

Figure 6: I-V Characteristics for Various Gate-Source Voltages (0V to 8V) across PMOS Transistor

Again, we can observe all three MOSFET operation modes in this graph.

Cutoff occurs when the magnitude of the gate-source voltage is less than the magnitude of the threshold voltage, as shown in Table 1. In this scenario, the case where V_{GS} = 0 V exhibits this behavior, since 0 V is less than the PMOS's $|V_T|$ value of 0.7 V. This is shown in Figure 6 as a horizontal line of zero current.

The triode region is any point to the left of the triode-saturation border, denoted by the green line in Figure 6. We can again see that current in the triode region is parabolic, confirming the behavior modeled by the current equation in Table 1.

The saturation region is any point to the right of the triode-saturation border. We can again see that the current is almost horizontal for all curves in this region, confirming the assumption that the MOSFET does not have any dependence (in this case, very little) on the drain-source voltage.

These were the I_{DS} versus V_{DS} curves obtained for the PMOS circuit using V_{GS} values ranging from V_{GS} = 0 V to V_{GS} = 2 V in 0.2 V intervals.

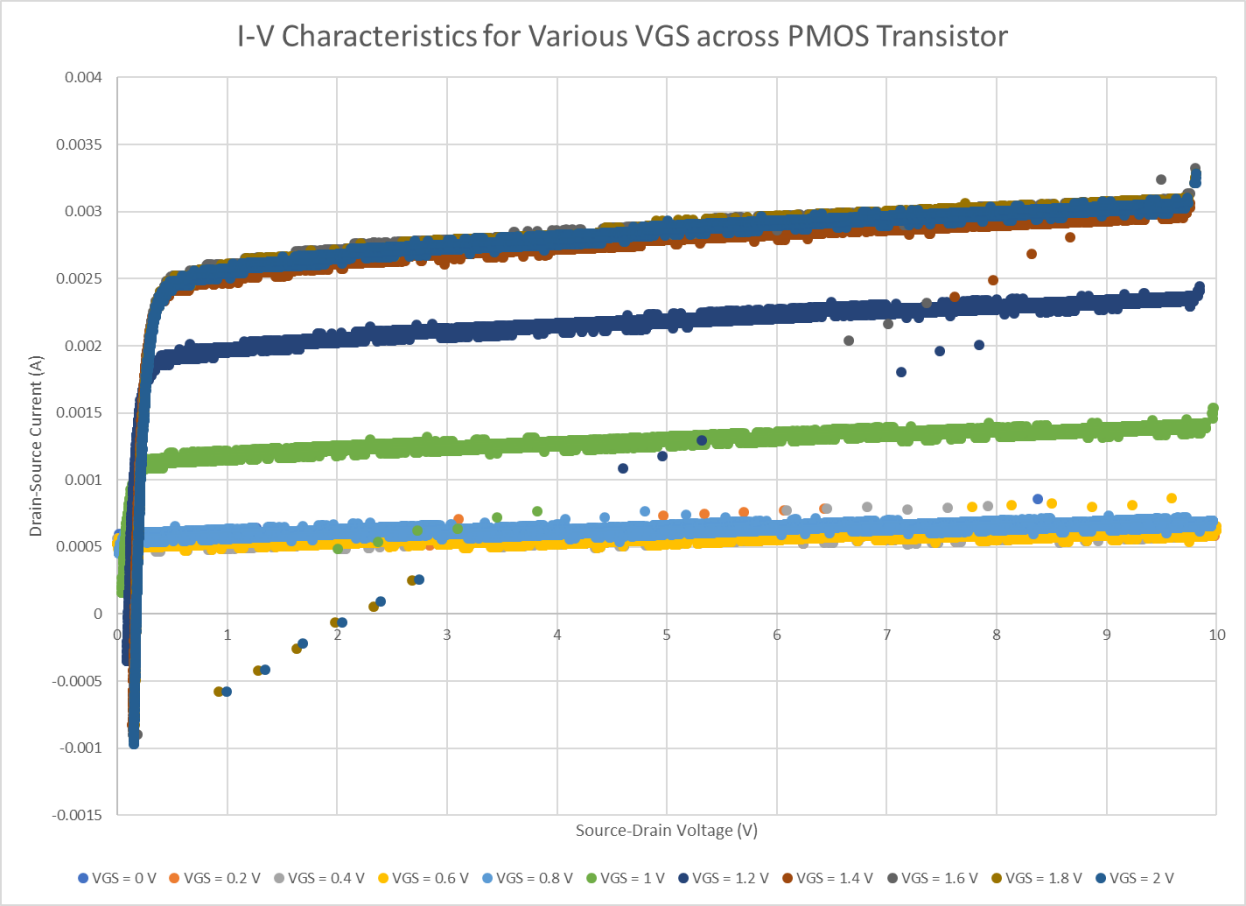

Figure 7: I-V Characteristics for Various Gate-Source Voltages (0V to 2V) across PMOS Transistor

*Correction: In Figure 7 above, the labels displayed in the legend should all say V_{SG} instead of V_{GS}, since V_{GS} values are negative for a PMOS I-V curve. In addition, the label for the Y-axis should display "Source-Drain Current (A)", since current values are negative for a PMOS I-V curve.

The data for these curves mostly holds true for values near the cutoff region, but the curves for V_{GS} values greater than or equal to 1.2 V can be seen to overlap. This is most likely due to an error in the Digilent programming during these data collection points (perhaps we failed to successfully change our output gate voltage in between trials).