Background

The objective of this lab is to familiarize ourselves with the various operation modes of a CMOS transistor and determine the effect that adding additional PMOS and NMOS transistors has on the CMOS inverter's transfer characteristic. To observe this effect, we built a CMOS inverter consisting of three PMOS and NMOS connections in parallel, with two of the branches featuring switches on the transistors allowing us to control their states. This report will show the transfer characteristics, curves, and static discipline of all nine PMOS / NMOS combinations and analyze the effect of adding additional PMOS and NMOS transistors.

Procedure

A basic CMOS inverter circuit (shown in Figure 1 to the right) involves one PMOS and one NMOS transistor with a common input (gate) voltage connected at the drains of the two transistors to form the output voltage. A low input voltage corresponds to a high output voltage, and vice versa. The switch between high and low output occurs at a threshold voltage, a point where the input voltage V_{in} equals output voltage V_{out} and both transistors operate at their saturation modes.

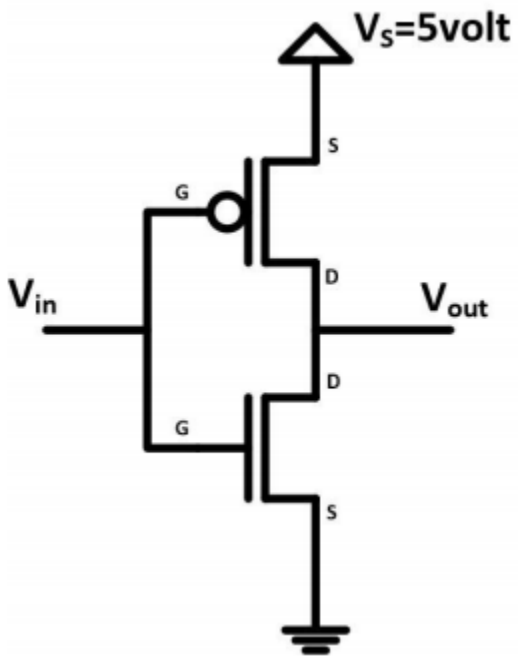

Figure 1: Circuit Diagram for CMOS Inverter

The threshold voltage is dependent on the value of a constant "k" for the transistors. This constant is determined by the physical properties of the PMOS and NMOS transistors, particularly their width and length.

If we connect additional transistors in parallel, we change their equivalent width in the larger transistor. For example, if we put two NMOS in parallel, we can treat the resultant transistor as one larger transistor with double the width. This change in width will affect the value of the constant "k" of the transistors, resulting in a change in the threshold voltage as well.

If we derive an equation for the threshold voltage V_{TH} (which is done in the Analysis), we will observe that V_{TH} is proportional to the ratio of k_p / k_n. From this, we can infer that an increase in k_p, which occurs through the addition of PMOS transistors, will increase V_{TH}, and an increase in k_n will decrease V_{TH}.

We will test the assumption that more PMOS transistors increase V_{TH} and more NMOS transistors decrease V_{TH} by setting up a large CMOS inverter consisting of three branches, each with one PMOS and one NMOS. To control the number of PMOS and NMOS transistors turned on, we will utilize additional MOSFETS to act as switches for our PMOS and NMOS transistors. Each of the MOSFETS acting as switches will have their gate voltages fixed to either 5V or GND to turn the switches on and off. Figure 2 shows the complete circuit used for this lab.

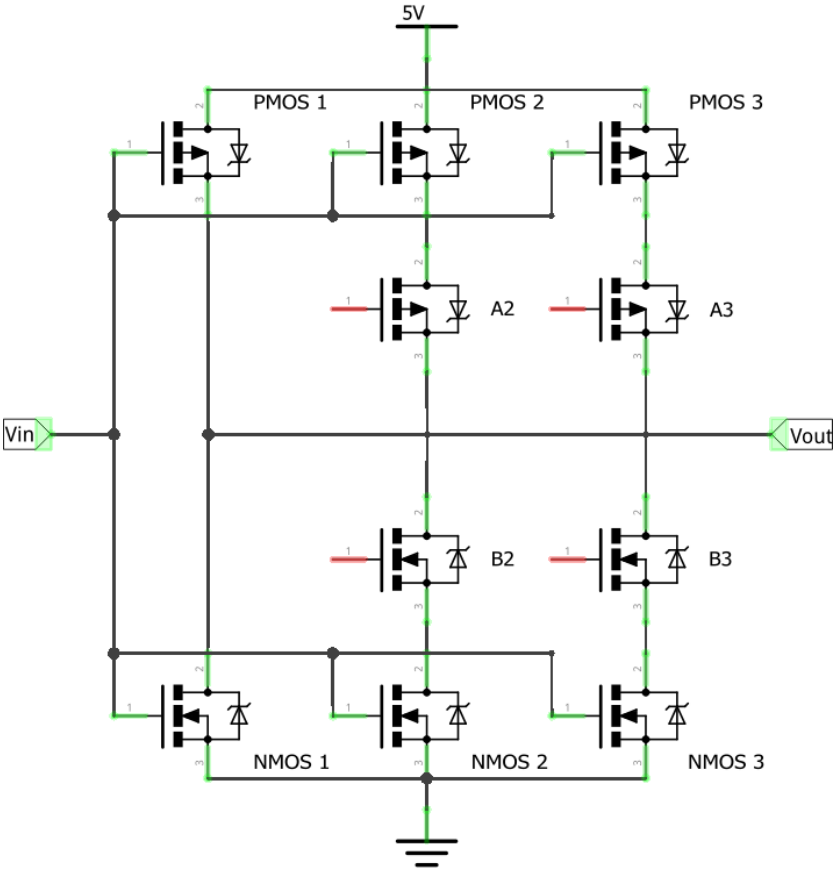

Figure 2: Schematic for CMOS Inverter containing 3 PMOS and 3 NMOS