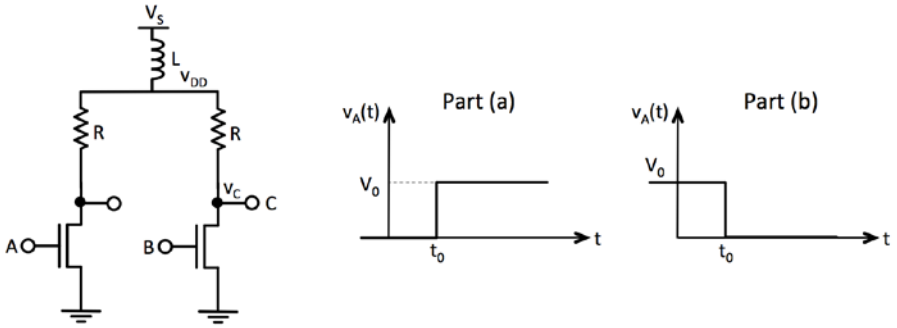
1. Consider two inverters on a chip connected to the same local power supply, V_{DD}. Perhaps due to a poor layout, the local power supply has an inductive connection to the external source that powers the chip, V_S. Use the SR model for the MOSFETs in this problem, ignoring C_{GS}, and assume that both FETs have the same $R_{ON} = 0.1R$. Part (b) is on the next page.



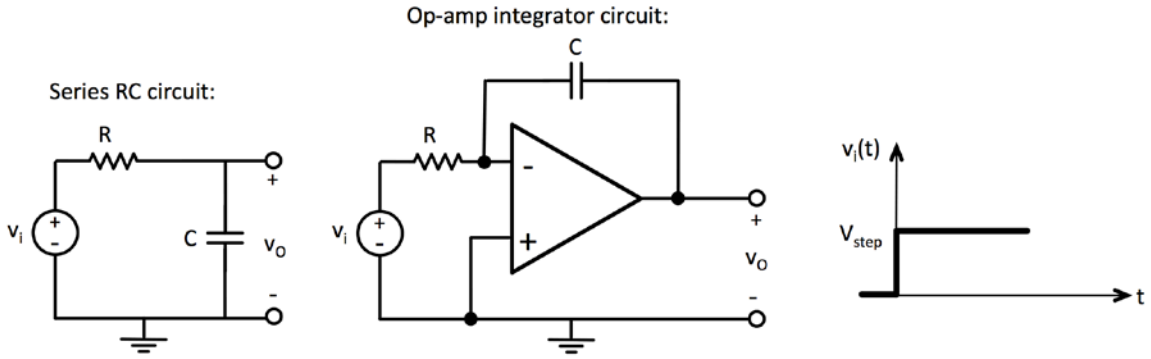
a) Input *B* is held at 0V. Input *A* has 0V applied to it initially, and at $t = t_0$, a step of $+V_0$ is applied to input *A*. Assume that $V_0 > V_T$ and that $V_S > V_T$.
   i. Draw the equivalent circuit for $t > t_0$ and write down the initial current through the inductor (just after $t = t_0$).
   ii. Derive an expression for the voltages $v_{DD}(t)$ and $v_C(t)$ (the voltage at node C = the output of the second inverter). Plot $v_{DD}(t)$ and $v_C(t)$.

b) Input B is now held at 5V. Input *A* has V_0 applied to it initially, and at $t = t_0$, a step of $-V_0$ is applied to input *A* so that its voltage goes to 0V. Again assume that $V_0 > V_T$ and that $V_S > V_T$.

i. Draw the equivalent circuit for $t > t_0$ and write down the initial current through the inductor (at $t = t_0$).

ii. Derive an expression for the voltages $v_{DD}(t)$ and $v_C(t)$ (the voltage at node C = the output of the second inverter). Plot $v_{DD}(t)$ and $v_C(t)$.

2. Two different integrators to measure capacitance… Consider the two circuits shown below with a step voltage input applied at $t = 0$. Assume that V_{step} is small enough that the op-amp stays in the active region, avoiding saturation.



a) Find $v_O(t)$ for both circuits. The general form of the solution should be the same for both circuits. Note that while the op-amp circuit is different from the differentiator you used in lab, don't be scared, the analysis is pretty straightforward. (*Hint:* for the op-amp circuit, don't make the simplifying assumption that $v^+ \approx v^-$, instead use $v_O = A(v^+ - v^-)$ and draw the equivalent circuit model).

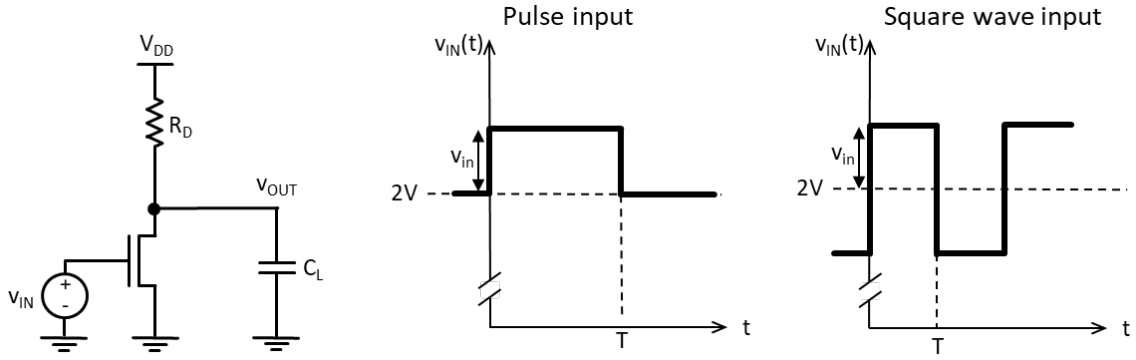
b) Compare the effective time constants for the circuits based on your answer to (a).

c) Assume that we measure v_O at a time, t_0, that is much less than RC. Remember from class that this means we can simplify the expressions from part (a) using the expansion: $e^{-x} = 1 - x + \frac{x^2}{2!}$ (neglect the x^2 term, *why is this reasonable?*) Compare the magnitude of the output voltages of the two circuits at $t = t_0$.

d) Based on your answers to (b) and (c), why would the op-amp integrator be better for measuring capacitance?

3) Consider the common-source amplifier driving a capacitive load as shown below. Assume that the circuit is properly biased such that the MOSFET operates in saturation. A voltage pulse is applied at the input with amplitude v_{in} that is small enough that the circuit operates in the small-signal regime.

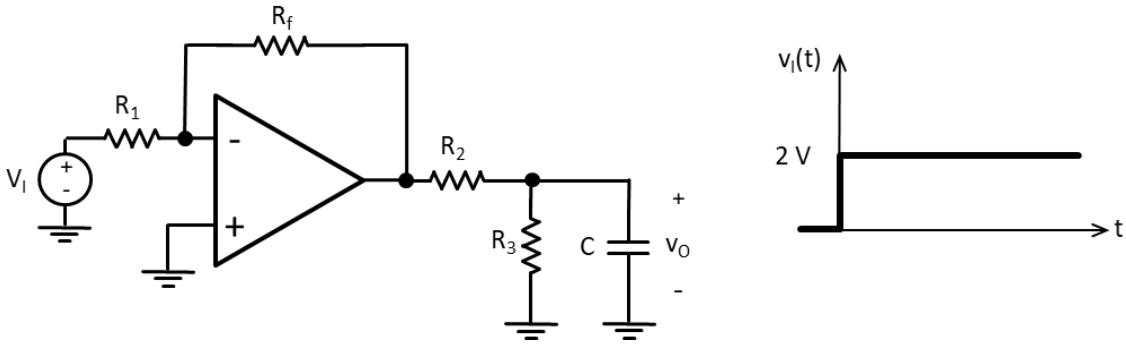
R_D = 2kΩ, V_T= 1V, K = 2mA/V², V_{IN} = 2V and V_{DD} = 5V, C = 0.5x10^{-9} F, v_{in} = 25mV



a) Find the DC voltage at V_{OUT} and the DC drain current, I_D.
b) Draw the small-signal model and find an expression for $v_{out}(t)$.
c) If T = 5μs, draw the corresponding $v_{OUT}(t)$ waveform (note this is the total variable = DC + small signal).
d) If T = 1μs, what is the value of $v_{OUT}(T)$?
e) If a square wave is now applied to the input with amplitude $2v_{in}$ (still small enough to keep the circuit in small-signal operation), sketch the corresponding waveforms of $v_{OUT}(t)$ for square-wave frequencies of 100KHz, 500kHz, and 50MHz.

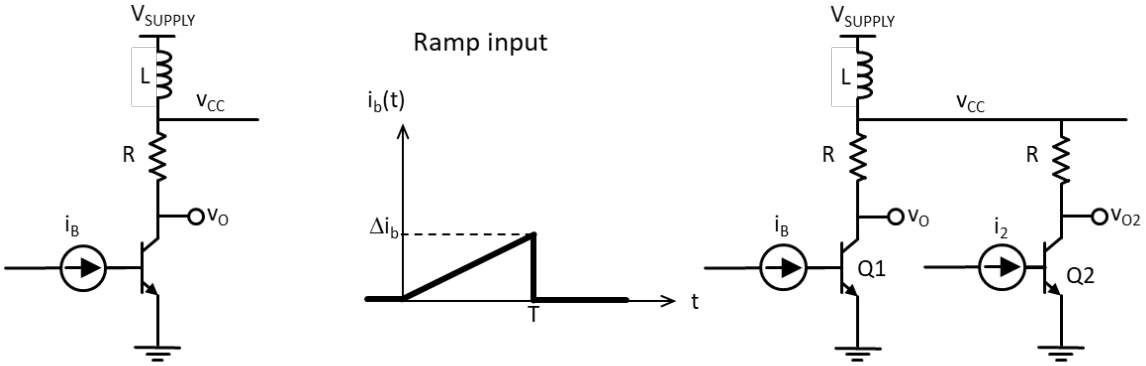
4) Assume the op-amps are all ideal in the circuit shown below.

$R_1 = 20\text{k}\Omega$, $R_f = 50\text{k}\Omega$, $R_2 = R_3 = 10\text{k}\Omega$, $C = 2\mu\text{F}$



a) Find the step response, $v_o(t)$, for $t > 0$. Sketch $v_o(t)$ with clear labels.
b) After the circuit has been operating for 100ms, all power is completely cut off to the circuit: the op-amp power supplies go to zero volts as does v_I. Sketch $v_o(t)$for $t > 100$ms with clear labels. Assume all op-amp terminals behave as open circuits.

5) Consider the circuit shown below. Perhaps due to a poor layout, the local power supply, v_{CC}, for a common-emitter amplifier has an inductive connection to the external source that powers the chip, V_{SUPPLY}.



(a) (b)

(a) If the small-signal current ramp shown above is applied to the input of the circuit (a), find the response of the local supply $v_{cc}(t)$ and $v_o(t)$.

(b) If $\beta = 100$, $R = 1\text{k}\Omega$, $\Delta i_b = 10\mu\text{A}$, $L = 1\mu\text{H}$, and $T = 10^{-9}\text{s}$, sketch and clearly label the corresponding small-signal waveforms: $v_{cc}(t)$ and $v_o(t)$. Repeat for L =0.

(c) Now consider the case where another common-emitter amplifier shares the local power supply connection as shown in (b). Assuming that no small-signal input is present for the second amplifier Q2 (but that it is properly biased in Forward Active operation), sketch the waveform for $v_{O2}(t)$ when the ramp input is applied to the original first amplifier as in parts (a) and (b). If $L = 0$ what would the $v_{O2}(t)$ waveform look like?

(d) Concisely explain the effect of the inductive power connection.