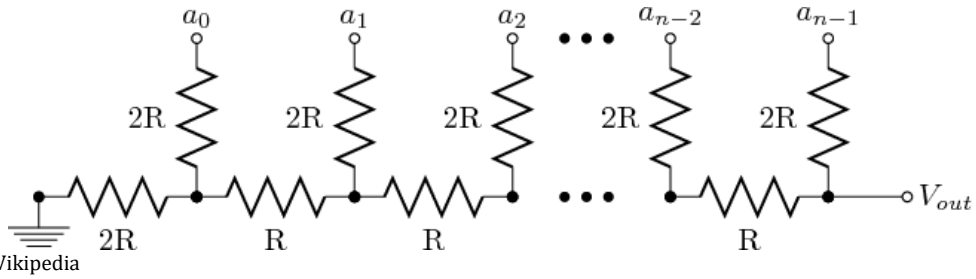
Lab 4: Digital to Analog Conversion

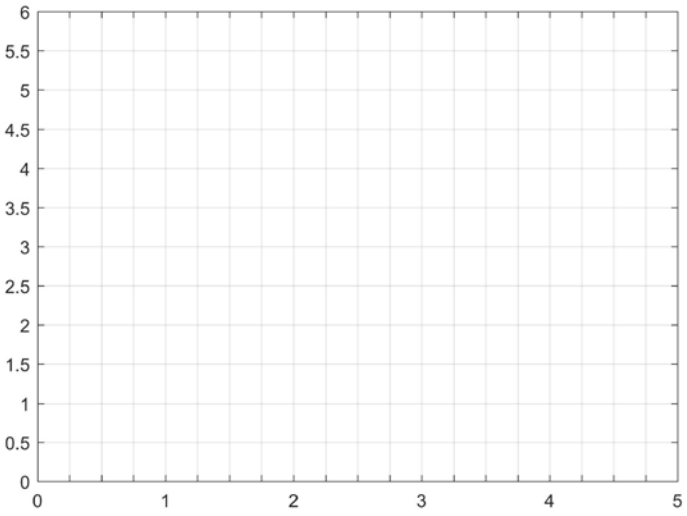
Digital-to-analog converters (DACs) are extremely important circuits that allow digital systems to synthesize "real-world" analog signals. Google "DAC" and you will find many examples of these circuits because they are used everywhere! In this lab, you will use the Digilent Discovery 2 (DD2) to build a DAC circuit. One approach to a DAC is to use the R-2R ladder network shown below. This network should look familiar. The values a_k come from a digital signal source that produces a voltage. We will consider the set of values ($a_0 a_{1...} a_{n-1}$) to be a digital "word" where a_0 is the LSB.

Required Parts: 10 500Ω resistors and 10 1kΩ resistors You could also get 30 500 Ω resistors and use 2 to make a 1 kΩ.



Source: Wikipedia

Step 1: In this laboratory, you are going to use the digital outputs of the DD2 rather than the DC supply. Connect the output of the digital line to a 1 kΩ resistor and toggle the digital output from 0 to 1 and back. Use pattern -> add pin -> clock. Draw a plot of your digital output on the graph below. Use a 1s period. (6 pts)



Step 2: Now, calculate the maximum V_{out} and the voltage step size ΔV that result from the operation of the DAC. You solved a similar problem on HW4. $V_{out,max}$ occurs

when all a_k inputs are "high". Use your measured step response from Step 1 to calculate the voltage value. The step size might be calculated by considering stepping from all of the inputs as "low" and toggling the a_0 input to "high". (10 pts)

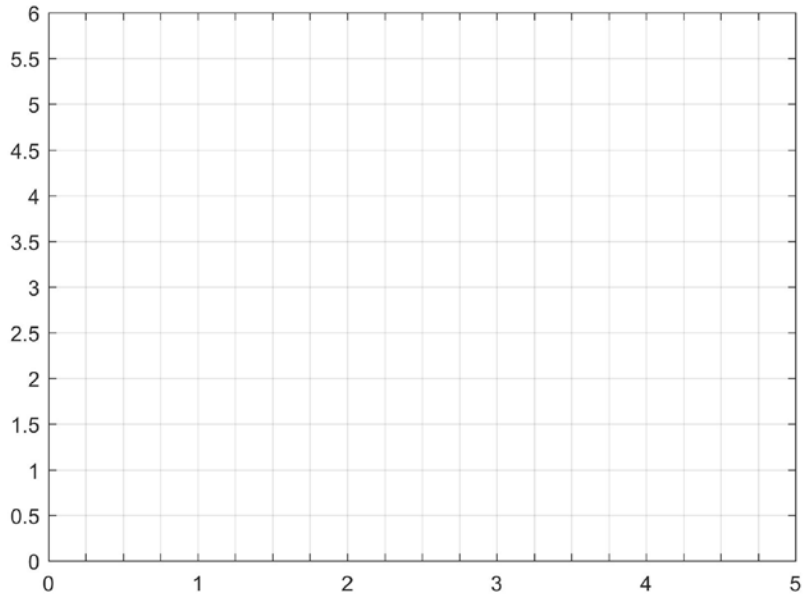
N	$V_{out,max}$	ΔV
4		
8		
16		

Step 3: Consider using N = 4 bits. On the breadboard, construct the R-2R ladder with R of 500 Ohms. Connect each of the a_k inputs to ground.

What resistance would you expect from your earlier calculations? (4 pts)

What resistance do you measure at the output? (2 pts)

Step 4: Connect each of the a_k to the digital outputs of the DD2 and program the digital words to increase sequentially for 0.25 seconds. In other words, the word will increase from 0 to 1 to 2 and so on until you reach 15 and then start over again. Plot the voltage V_{out} as a function of time over one entire cycle of sequences. (10 pts)

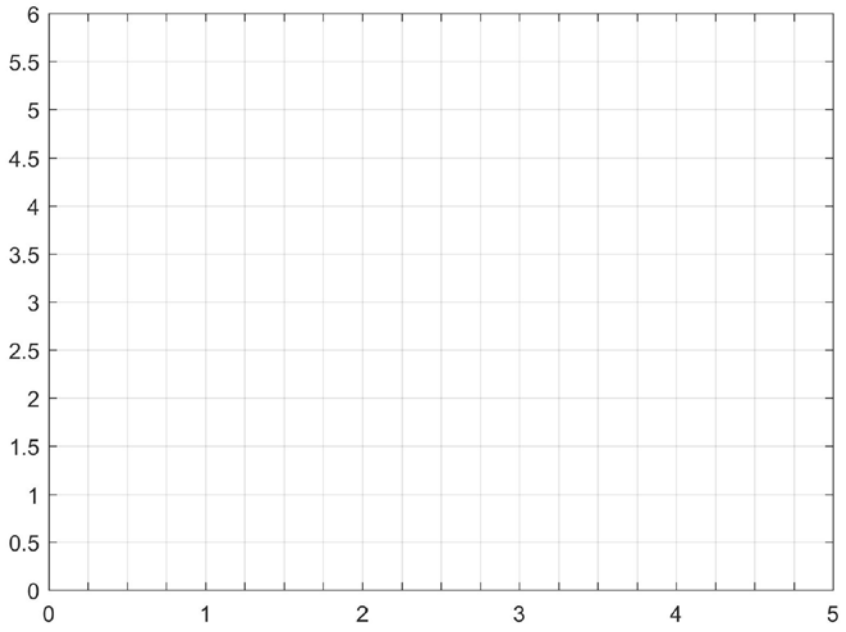


Step 5: Continuing from Step 4, record the voltage V_{out} for each digital word value. It is easiest to do this by statically setting the digital values to be constant. (10 pts)

a_k	V_{out}	ΔV_{out}	a_k	V_{out}	ΔV_{out}
0			8		
1			9		
2			10		
3			11		
4			12		
5			13		
6			14		
7			15		

Does the result agree with your prediction for the voltages from Step 2?

Step 6: Now consider using N = 8 bits and R = 500 Ohms. Rebuild the ADC on the breadboard with these specifications. Connect each of the a_k to the digital outputs of the DD2 and program the word sequence to change every 15.625 ms to generate the ramp. Plot the voltage V_{out} as a function of time over one entire cycle of sequences. (You don't have to capture every value. Try to approximate it. Does this curve look more like a ramp? (10 pts)



Step 7: Continuing from Step 5, plot the step size at a few sample points listed below. In other words, take the difference between the voltage listed on the table below and the "previous" digital sequence. Is the step constant for all digital values? (10 pts)

a_k	ΔV_{out}	a_k	ΔV_{out}
1		128	
16		144	
32		160	
48		176	
64		192	
80		208	
96		224	
112		240	

Does the result agree with your prediction for the voltages from Step 2?

Step 8: Observations (10 pts)

A) Are the steps smaller or larger for the N = 4 or the N = 8?

B) Which did you expect to be smaller from your calculation?

C) Calculate the ratio of the standard deviation for the step size you measured against the average step size value. Is this ratio greater for the N = 4 or the N= 8 DAC?

	Mean (μ) of ΔV_{out}	STD (σ) of ΔV_{out}	μ/σ
N = 4			
N = 8			

D) The "uneven" step sizes cause differential nonlinearity (DNL) in ADCs is must be minimized for good performance. How would you consider reducing the deviation in the step size?

Step 9: Before you take everything apart, let's try to figure out how to program the digital word sequence to generate a sine wave at 1 kHz. You are welcome to use N = 4 (easy) or N= 8 (hard). The challenge is to determine the sequence of words. To help you out, you might consider a function like

$$WORD_k = round\left\{\frac{2^N - 1}{2}\left(1 + \sin\left(\frac{2\pi k}{K}\right)\right)\right\}$$

The round function is used to quantize the value to an integer. *K* is the period of the sine. For example, for *N* = 4, I have completed some of the table for you.

Time step (t_k)	$WORD_k$	a_k	Time step	$WORD_k$	a_k
0	8	1000	8		
1	10	1010	9		
2	13	1101	10		
3	14	1110	11		
4	15	1111	12	0	0000
5			13		
6			14		
7			15	5	0101

Draw your resulting sine wave on the graph below.