These were the resistor and current values we measured when building the current mirror circuit and making modifications to obtain certain currents.

Table 2: Resistor and Current Values for Various Resistance / MOSFET conditions in Current Mirror

	Zero resistance Matching MOSFETs	Resistance R_p Matching MOSFETs	Zero resistance M2 is 2 NMOS in | |
Expected Outcome	$I_{OUT} = I_{REF}$	$I_{OUT} = \frac{1}{2} I_{REF}$	$I_{OUT} = 2I_{REF}$
R_P (Ω)	0	452	0
I_{REF} (A)	4.59	4.59	4.57
I_{OUT} (A)	4.64	2.29	9.13

For all the cases listed in Table 2, we can see that the expected outcome relatively matches the actual outcomes predicted via the equations.

Recalling equation 8, we know that:

$$i_{OUT} = i_{REF}\left(\frac{L_1 W_2}{L_2 W_1}\right) \quad (8)$$

In the first case, where there is zero resistance and the MOSFETs match, the ratio of lengths to widths equals 1, since the lengths and the widths of the MOSFETs are consistent. This results in an output current equivalent to the input current, and the measured output current was almost the same as the input current.

In the second case, we applied a variable resistance to the output MOSFET source, causing voltage to drop across the resistor. V_{GS} is no longer equal, so equation 8 no longer holds true. However, we know from equation 6 that:

$$i_{DS} = \frac{k}{2}(V_{GS} - V_T)^2 \quad (6)$$

V_{GS} will decrease in the output branch to account for the new resistance, and we can see that the current will similarly decrease as a result. The measured output current decreased relative to the input current.

In the last case, we switched the output MOSFET with a parallel connection of two NMOS transistors that match the NMOS in the input branch. We know that putting similar MOSFETS in parallel effectively doubles their width, so from equation 8, we get:

$$i_{OUT} = i_{REF}\left(\frac{2LW}{LW}\right) = 2i_{REF} \quad (9)$$

The measured output current was almost double that of the measured input current, so we can confirm this relationship as well.

Conclusion

In this lab, we built an NMOS and PMOS circuit, each containing one transistor connected in series with a resistor, swept the input voltage, varied the gate voltage, and measured the voltage across the resistor for all trials. The objective for building these two circuits was to observe the various operation modes of a MOSFET and observe the effect that increasing V_{GS} has on the I-V curve. We were able to conclude that the MOSFETs output no current if in the cutoff region, a current parabolic to the drain-source voltage if in triode, and a constant current if in saturation. We also built a current mirror using two NMOS transistors, each in their own branch, with their gate voltages connected to the drain of the input NMOS. The objective of this circuit was to observe the relationship between the input and output currents given varying K parameters. We were able to conclude that if the NMOS are equivalent, then the current will be mirrored one-to-one. In addition, output current can be reduced by adding a resistance to the source of the output NMOS, and output current can be increased by connecting MOSFETs in parallel to effectively double their width.

We encountered problems with our PMOS data collection during this lab, as our original data resulted in overlapping I-V curves for most cases that were not in the cutoff region. This can partially be seen in Figure 7. We were unable to resolve this during our lab session and had to ask another lab group for their data points to plot Figure 6. To help prevent this in the future, I would recommend reducing the number of curves we are required to collect so data collection and graphing are much easier to accomplish during the lab session (Excel slows down significantly when working with data sets containing tens of thousands of points, and when you try to overlay ten of them, things stop working).