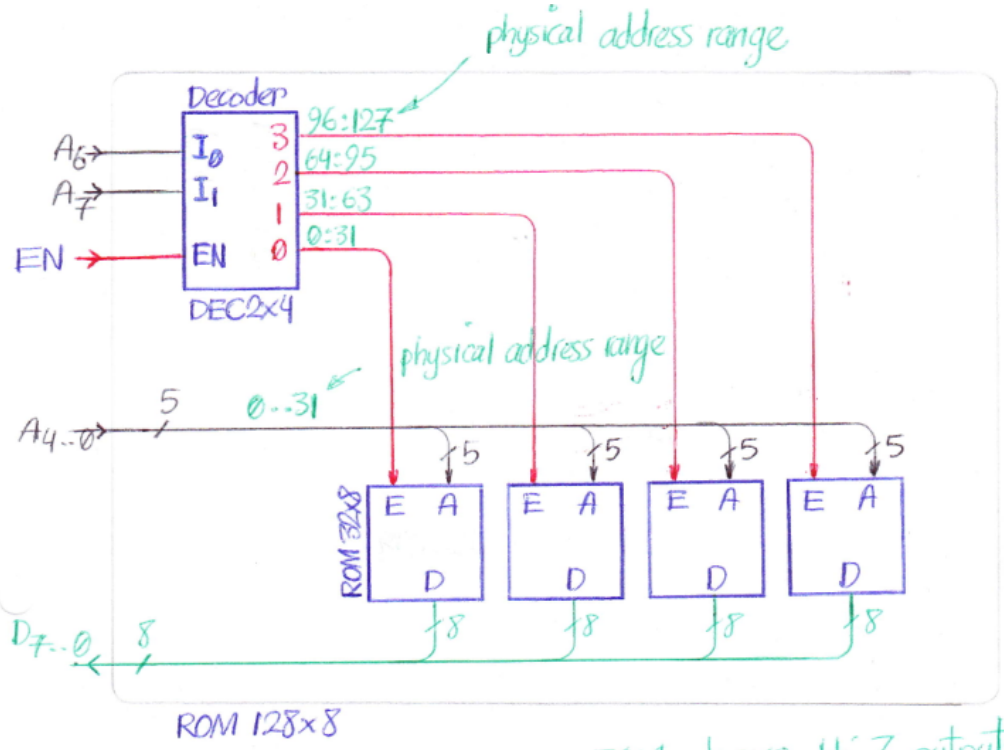
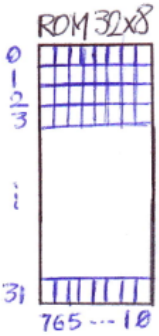
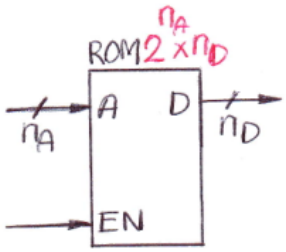
Problem 1. Given a 32x8 ROM chip with an enable input, show the block level required connections to construct a 128x8 ROM with above ROM chips and a decoder. How many data and address lines do these ROMs have?

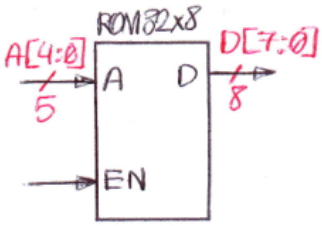
Solution:



ROMs have Hi-Z outputs





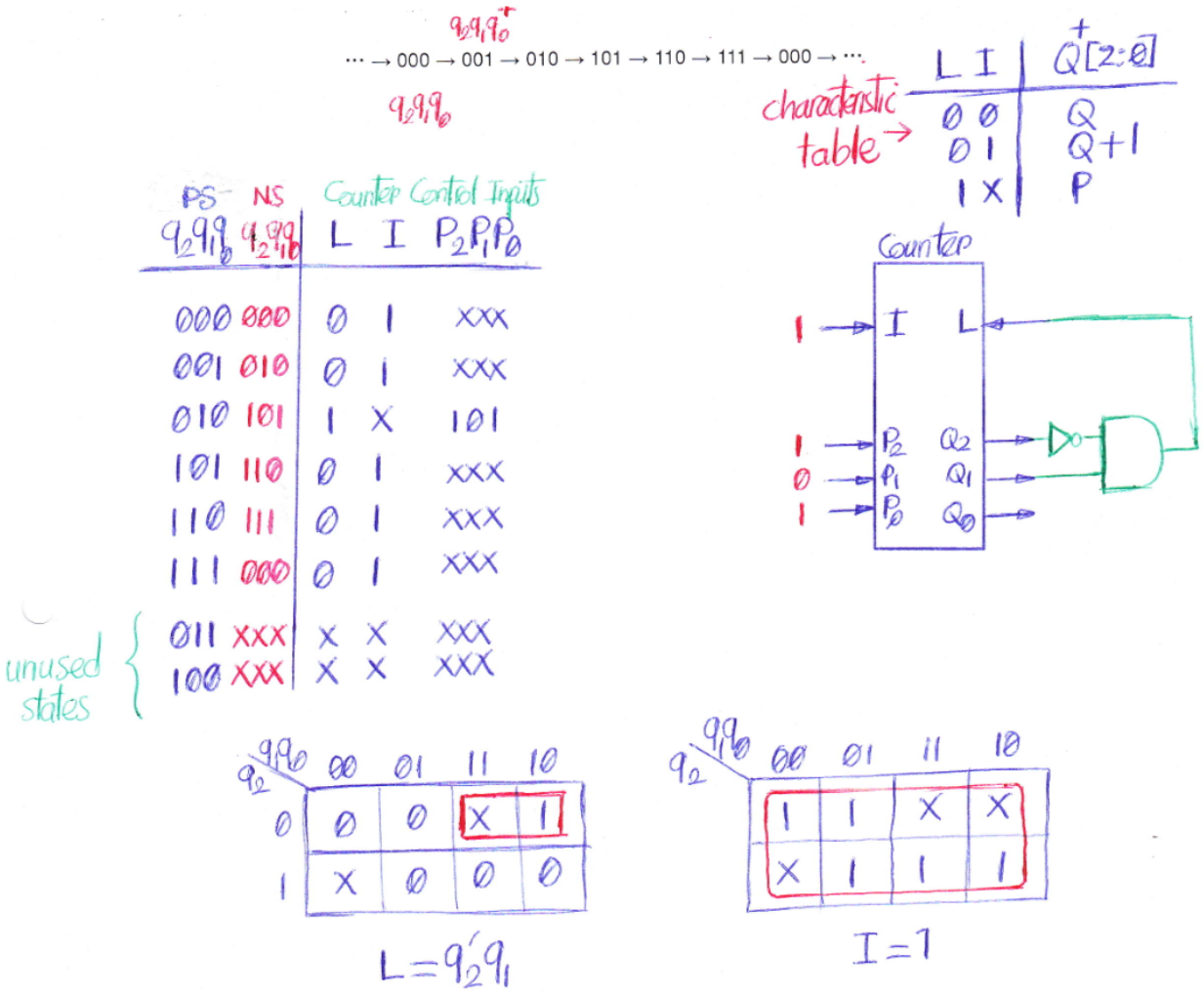


ROM-Size = $2^{(\#\text{of address bits})} \times (\#\text{of data bits})$

$= 2^{n_A} \times n_D$ bits

Problem 2. Use a 3-bit binary counter with active-high load (L) and Increment (I) control inputs (load has higher priority than increment) and implement a circuit (draw) to generate and repeat the following sequence at the output of the counter. Initial counter value is 000.

Solution:



Problem 3. Design a digital circuit that takes two 4-bit numbers A and B as input and generates output Z as follows:

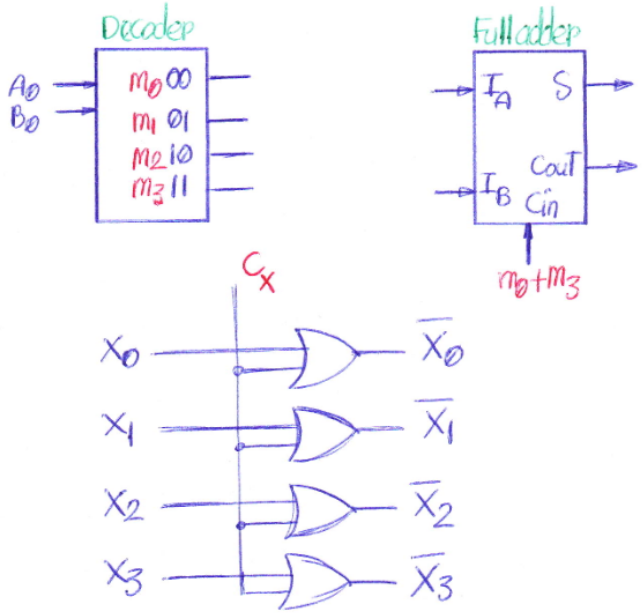
- If A and B are odd numbers then Z=A-B
- If A and B are even numbers then Z=B-A
- If A is an even number and B is an odd number then Z=A+B
- If A is an odd number and B is an even number then Z=A-B-1

Assume that you have access to as many as you need of AND, OR, INV, XOR gates and only one FULL-ADDER, DECODER and MULTIPLEXER of any size.

Solution:

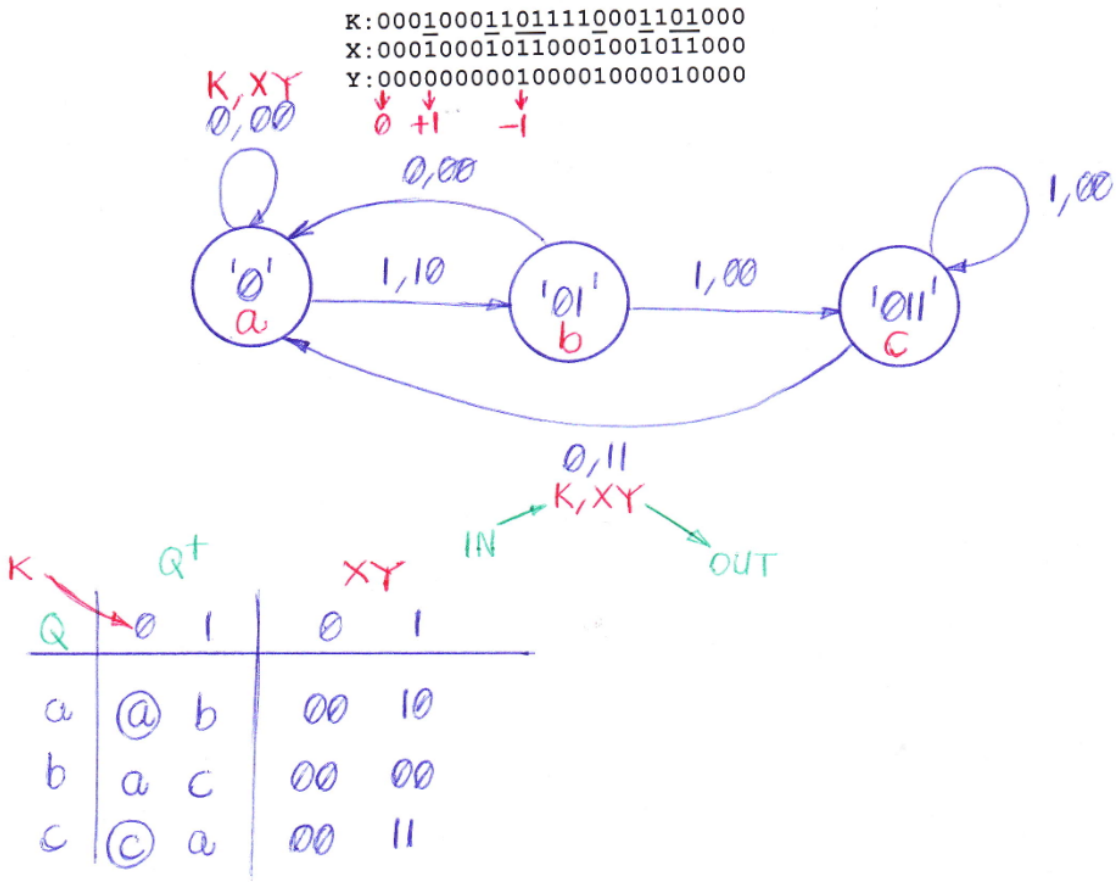
odd even A_0B_0		function Z	Full adder inputs I_A I_B C_{in}			Control Commands
m_0	00	B-A	~A	B	1	$C_{in} = m_0 + m_3$
m_1	01	A+B	A	B	0	$C_A = m_0$
m_2	10	A-B-1	A	~B	0	$C_B = m_2 + m_3$
m_3	11	A-B	A	~B	1	

} Complement circuit input



Problem 4. A crypto module which transforms a secret key bit stream, K, into two other bit streams, X and Y has to be designed. It works as follows: if the secret key bit stream contains 011, then its replaced with 10(-1). This transformation reduces the number of 1 bits in the key (which has significant impact on subsequent processing times in elliptic curve algorithms). However since we cannot represent 0, 1 and -1 with a one bit output, we use two output signals, X and Y. Whenever a m-bit sequence of 1s is detected (where m¿1), X is set to 1 for the first K=1 in the sequence and when a K=0 is detected after the m th 1 bit both X and Y are set to 1. Construct a sequential state table for this module.

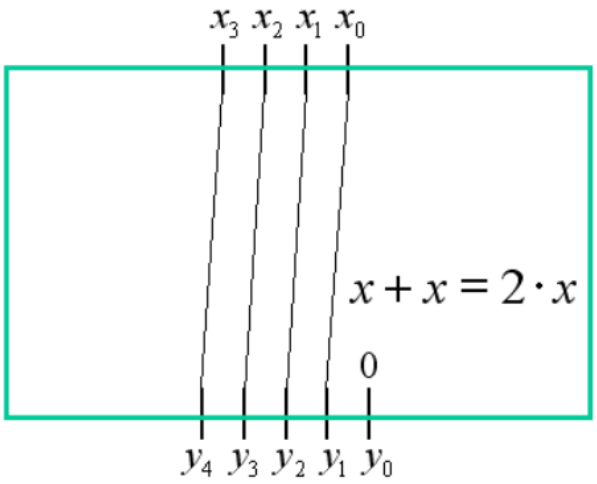
Solution:



K	Q+		XY	
Q	0	1	0	1
a	@	b	00	10
b	a	c	00	00
c	©	a	00	11

Problem 5. A four bit unsigned integer x ($x_3x_2x_1x_0$) is connected to an 4-bit adder as in the figure. The result is a 5-bit number y ($y_4y_3y_2y_1y_0$). Draw the figure to the right how the same results can be obtained **without using the adder.** There are also bits with the values 0 and 1 if needed.

Solution:



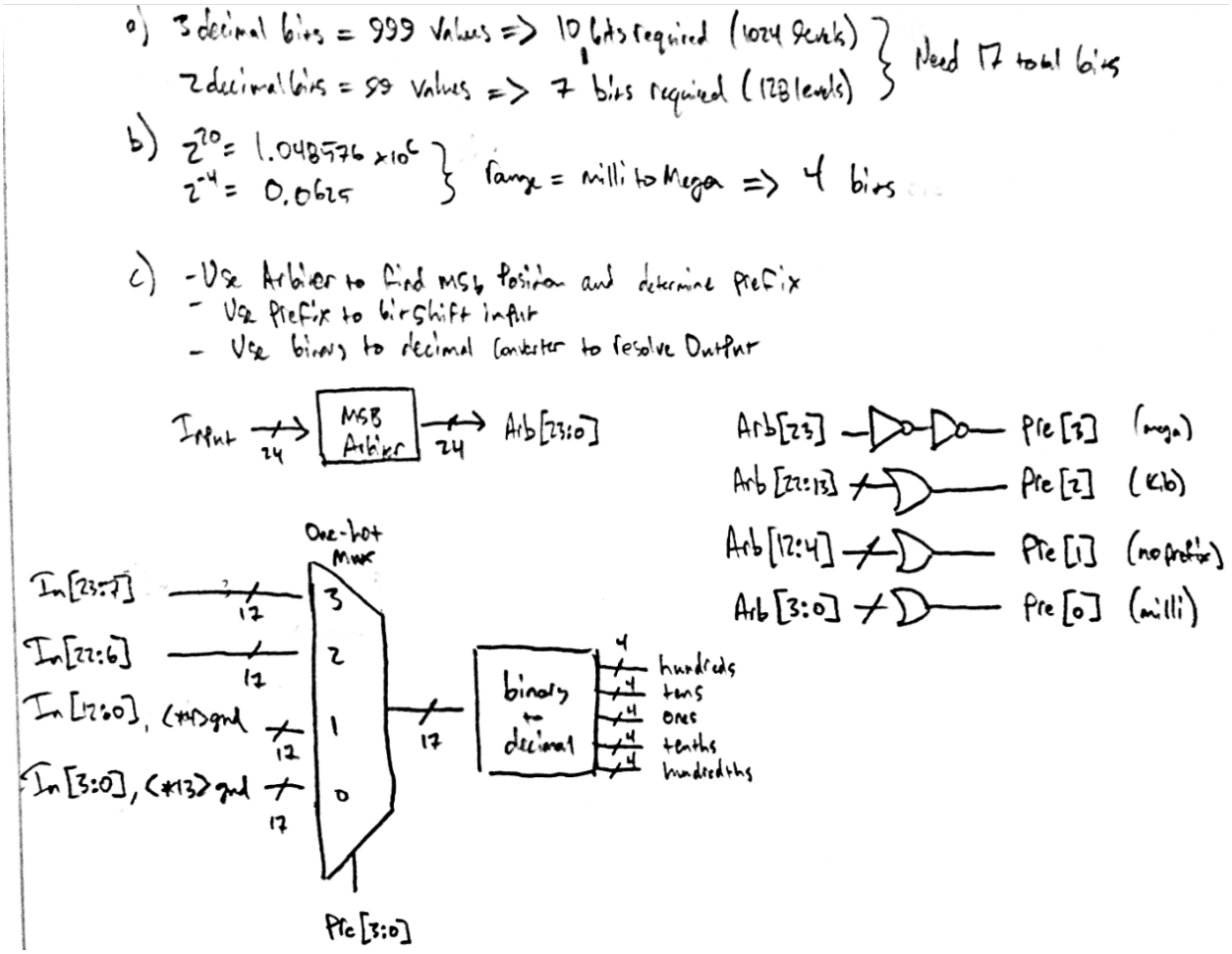
Problem 6. You have probably noticed in your 10 labs that the multimeter has an auto-ranging function. It always uses a fixed-point format, for example 100.23 (a 3.2 format) and only changes the units from M to k. Another example is a scientific balance, which automatically switches from milligrams to grams to kilograms. Given a 24 bit input (from the measuring unit) in a 20.4 format (20 bits before the decimal point, 4 after), answer the following:

a) If you wanted to represent the answer after scaling in a 3.2 Decimal format. How many bits do you need? Specify it in x.y format

b) Additionally you need a binary output indicating the unit scale (i.e. M,k). How many bits does this output need if the encoding is 1-hot binary?

c) Design a logic block using building blocks such as binary adders, comparators, multiplexers, decoders, encoders, and arbiters, as well as logic gates, that will automatically scale the 24 bit input into the x.y representation from the previous question, along with a units scale output in 1-hot encoding.

Solution:

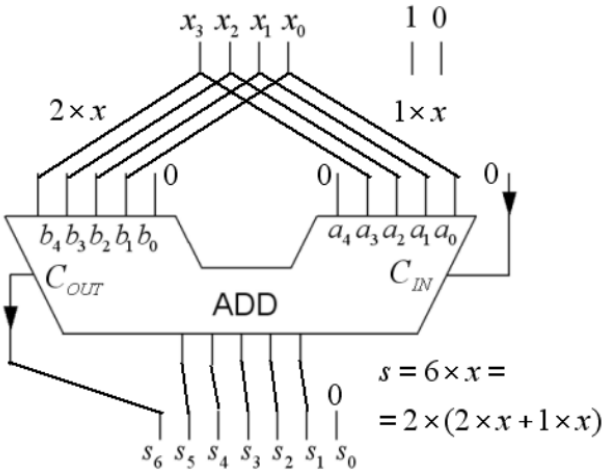


Problem 7. A four bit number $x(x_3x_2x_1x_0)$ is to be multiplied by the constant 6.The number x is fed into a five bit adder which is configured for the operation $6 \cdot x = 2 \cdot (2 \cdot x + 1 \cdot x)$.

a) Draw how the adder has to be configured. Apart from the four bits in x, constants with the values 0 and 1 are also available

b) Which is the greatest binary number s $(s_6s_5s_4s_3s_2s_1s_0)$ that can appear on the output when the circuit is configured for this operation? Answer with a binary number.

Solution:

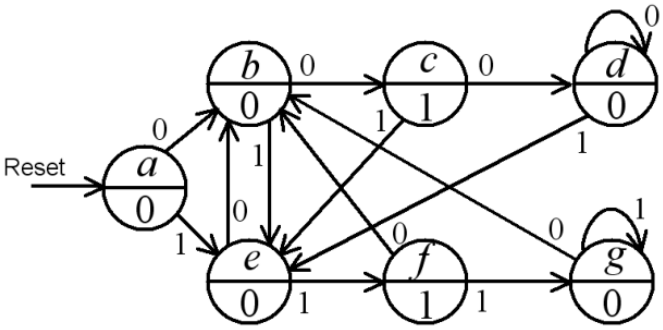


b) The greatest number will be $s_{max} = 6 \cdot 15 = 90$. Since the calculator is not allowed at the exam, this time we can choose to transform 90 to at **binary number** in the same way as in a)
(also other conversion method are ok):

$$
\begin{array}{rcccccc}
 & \underline{1} & \underline{1} & \underline{1} & \underline{1} & \underline{0} & \underline{0} & \\
 & 0 & 1 & 1 & 1 & 1 & 0 & 15\times 2 \\
+ & 0 & 0 & 1 & 1 & 1 & 1 & 15\times 1 \\
\hline
 & 1 & 0 & 1 & 1 & 0 & 1 & \\
1 & 0 & 1 & 1 & 0 & 1 & 0 & \times 2
\end{array}
$$

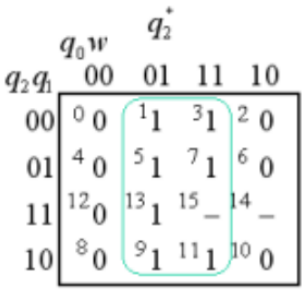
Problem 8. Design a synchronous state machine for the following problem: The input signal w is synchronized with the clock pulses C. The output signal z should become 1 each time the value of the input signal w had not changed for two clock pulses. This change in the output value will appear at the clock pulse following the two pulses with the identical w values. See the example below for clarification.

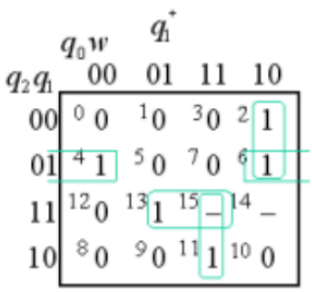
Solution:

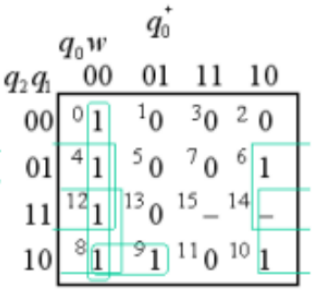


state	next w=0	next w=1	out
a	b	e	0
b	c	e	0
c	d	e	1
d	d	e	0
e	b	f	0
f	b	g	1
g	b	g	0

$q_2q_1q_0$	$q_2^+q_1^+q_0^+$ $w=0$	$w=1$	y
a : 000	001	100	0
b : 001	010	100	0
c : 010	011	100	1
d : 011	011	100	0
e : 100	001	101	0
f : 101	001	110	1
g : 110	001	110	0
	14	15	







$$q_2^+ = w$$

$$q_1^+ = \bar{q}_2 q_0 \bar{w} + \bar{q}_2 q_1 \bar{w} + q_2 q_1 w + q_2 q_0 w$$

$$q_0^+ = \bar{q}_0 \bar{w} + q_1 \bar{w} + q_2 \bar{w} + q_2 \bar{q}_1 \bar{q}_0$$

$$y = \bar{q}_2 q_1 \bar{q}_0 + q_2 \bar{q}_1 q_0$$