Homework #1

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By

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1) Find instruction count, CPI, and clocks

A)

Instruction	Count	CPI	Clocks
Or $16,$16,$0	1	1	1
Lw $21, ($20)	10	3	30
Loop: Lw $19,($18)	10	3	30
Add $21,$21,$19	10	1	10
Addi $16,$16,1	10	3	30
Addi $18,$18,4	10	1	10
Slti $17,$16,10	10	1	10
Bne $17,$0,loop	10	1	10
Sw $21,($20)	10	2	20
Sum of Count, CPI, and Clocks	81	16	151

B1) On CPU_base with the given values, It will take the program exactly 151 clock cycles to be executed.

B2) Calculating the number of cycles it takes for this code fragment to execute on CPU_base is exactly 81.

2) Recreating problem 1…

Instruction	Count	CPI	Clocks
Or $16,$16,$0	1	1	1
Lw $21, ($20)	1	3	3
Loop: Lw $19,($18)	10	3	30
Add $21,$21,$19	10	1	10
Addi $16,$16,1	10	1	10
Addi $18,$18,4	10	1	10
Slti $17,$16,10	10	1	10
Bne $17,$0,loop	10	2	20
Sw $21,($20)	1	3	3
Sum of Count, CPI, and Clocks	63	16	97

We now have a count of 63, CPI of 16, and Clocks of 97.

157/97, there is a 1.56 speed up in the program time which is pretty substantial.

3) Exercise 1.5 on page 55

1.5 [4] <§1.6> Consider three diff erent processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

Work)

$$x = \frac{\text{speed}}{\text{CPI}}$$

1)P1=(3x10^9)/1.5=2.0x10^9
2)P2=(2.5x10^9)/1=2.5x10^9
3)P3=(4.0x10^9)/2.2=1.8x10^9

Answer)
And so we know that P2 has the highest performance expressed in instructions per second.

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

Work / Answer)

$$Instructions\ for\ ten\ sec = \text{Part A x } 10$$
$$Cycles\ for\ ten\ sec = Speed\ x\ 10$$

Instructions for ten sec
P1= (3x10^9 x10=3x10^10
P2=(2.5x10^9 x10)=2.5x10^10
P3=(4.0x10^9 x10)=4.0x10^10

Cycles for ten sec
P1= (2.0x10^9 x10) = 2 x10^10
P2=(2.5x10^9 x10) = 2.5x10^10
P3=(1.8x10^9 x10) = 1.8x10^10

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Work)

(Execution time x **0.7** = (# of instructions x CPI x **1.2**) / (Clock rate)

Clock rate = Clock rate * 1.2/0.7 = 1.71 x Clock rate

Apply this following eq to find the answers…

Answer)

P1: 3 Ghz x 1.71 = 5.13 Ghz

P2: 2.5 Ghz x 1.71 = 4.27 Ghz

P3: 4 Ghz x 1.71 = 6.84 Ghz

4)

1.6 [20] <§1.6> Consider two diff erent implementations of the same instruction set architecture. Th e instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.
Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?
Work)

$$\frac{clock\ cycles}{total\ \#\ of\ instructions}$$

(10^6x((1x.1)+(2x.2)+(3x.5)+(3x.2))/10^6 = 2.6

Global CPI P1=2.6

(10^6x((2x.1)+(2x.2)+(2x.5)+(2x.2))/10^6 = 2

Global CPI P2=2

b. Find the clock cycles required in both cases.

P1: (10^6 ((1x.1)+(2x.2)+(3x.5)+(3x.2)) = 2.6 x10^6
P2: (10^6x((2x.1)+(2x.2)+(2x.5)+(2x.2)) = 2 x 10^6

5)

The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.
Th e Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

5a)

Find for each processor the average capacitive loads.

$$Cap\ Load = \frac{2xPower}{Freq\ x\ Volt^2}$$

$$\frac{2x90}{3.6\ x\ 10^9\ \ x\ 1.25^2} = 2.9x10^{-8}$$

5b)

[5] <§1.7> Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

First processor:

$$Total\ Power = Static\ Power + Dynamic\ Power = 10 + 90 = 100\ Watts$$

$$\%\ of\ dissipation = \frac{10}{100} = 10\%$$

$$Ratio = \frac{10}{90} = \frac{1}{9}$$

Second processor:

$$Total\ power = 30 + 40 = 70W$$

$$\%\ of\ disappation = \frac{30}{70} = 42.8\%$$

$$Ratio = \frac{30}{40} = \frac{3}{4}$$

5c)

[15] <§1.7> If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defi ned as the product of voltage and current.

First processor

$$P = V * C$$

$$C = \frac{P}{V}$$

$$\frac{100}{1.25} = 80$$

$$And\ so\ power = 100 - \left(\frac{10}{100} x\ 100\right) = 100 - 10 = 90$$

$$Account\ for\ leakage \ldots P = VxC$$

$$V = \frac{P}{C}$$

$$\frac{\frac{90}{100}}{1.25} = 1.125$$

Check for errors:

$$Reduction = \frac{1.25 - 1.125}{1.25} * 100 = 10\%$$

Second Processor

$$C = \frac{P}{V}$$

$$Current = \frac{70}{0.9}$$

$$Reduced\ power = 70 - \left(\frac{10}{100} x70\right) = 70 - 7 = 63$$

$$Leakage = Voltage = \frac{P}{v}$$

$$\frac{\frac{63}{70}}{0.9} = 0.81$$

Check for errors:

$$Reduction = \frac{0.91 - 0.81}{0.9} x\ 100 = 10\%$$

6)

Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm2.

6a)

Find the yield for both wafers.

Wafer 1:

$$area = pi\ x\ \left(\frac{15}{2}\right)^2 = 176.625\ cm^2$$

$$defects = area * defects\ per\ unit = 176.625x0.02 = 3.53$$

$$good\ dies\ in\ Wafter\ 1 = Total\ dies - defect\ dies = 84 - 3.53 = 80.47$$

$$Wafer\ 1\ yield = \frac{80.47}{84} = 95.8\%$$

Wafter 2:

$$area = pi\ x\ \left(\frac{20}{2}\right)^2 = 314\ cm^2$$

$$defects = area * defects\ per\ unit = 314x0.031 = 9.74$$

$$good\ dies\ in\ wafter\ 2 = Total\ dies - defect\ dies = 100 - 9.74 = 90.26$$

$$Wafer\ 2\ yield = \frac{90.26}{100} = 90.26\%$$

6b)

Find the cost per die for both wafers.

Cost per die:

Cost per die for wafer 1= $\frac{Total\ cost}{Number\ of\ good\ dies} = \frac{12}{80.47} = 0.15$

Cost per die for wafer 2 = $\frac{Total\ cost}{Number\ of\ good\ dies} = \frac{15}{90.26} = 0.17$

6c)

If the number of dies per wafer is increased by 10% and the
defects per area unit increases by 15%, fi nd the die area and yield.

Wafer 1

8.4x1.1 = 94.4 dies per wafer

0.02x1.15=0.023 Defects

$$area * defects = 176.625x0.023 = 4.06$$
$$good\ dies\ in\ Wafer\ 1 = Total\ dies - defect\ dies = 92.4 - 4.06 = 88.34$$
$$Wafer\ 1\ yield = \frac{88.34}{92.4} = 95.6\%$$
$$Wafer\ 1\ die\ area = \frac{176.62}{92.4} = 1.9\ cm^2$$

Wafer 2

$$Wafer\ 2 = 100x1.1 = 110\ dies\ per\ wafer$$
$$Defects\ percentage = 0.031x1.15 = 0.036$$
$$Defects = 314x0.036 = 11.2$$
$$Good\ dies\ in\ Wafter\ 2 = Total\ dies - defect\ dies = 110 - 11.2 = 98.8$$
$$Wafer\ 2\ yield = \frac{98.8}{110} = 89.8\%$$
$$Wafer\ 2\ die\ area = \frac{314}{110} = 2.85\ cm^2$$

6d)

Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm^2.

$$0.92\ to\ 0.95 = 103.3\%\ increase$$

Wafer 1

$$Wafer\ 1\ yield = 95.6\ x\ 1.033 = 98.75$$
$$Wafer\ 1\ die\ area = \frac{176.62}{2} = 88.3$$
$$Wafer\ 1\ good\ dies = Yield * die\ area = .9875\ x\ 88.36 = 87.26$$
$$Wafer\ 1\ defects = Total\ dies - good\ dies = 88.3 - 87.26 = 1.04$$

Wafer 2

$$Wafer\ 2\ yield = 89.8\ x\ 1.033 = 92.78$$
$$Wafer\ 2\ die\ area = \frac{176.62}{2} = 88.3$$
$$Wafer\ 2\ good\ dies = .9278x157 = 145$$
$$Wafer\ 2\ defects = 157 - 145.74 = 11.26$$