ELLIOTT 900

Volume 4: ENGINEERING MAINTENANCE

Part 1: BASIC EQUIPMENT

Section 5: ON LINE ADAPTOR FOR PAPER TAPE AND TELEPRINTER CONTROLLER (DPA 212)

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END-OF-TEXT FIGURES

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Chapter 1: DESCRIPTION

1.1 Introduction

The On Line Adaptor consists of one logic board which is used to modify the action of the interface timing chain. If, when the processor attempts to carry out a data transfer, the device required is already busy, the processor is held up until the device is available. In certain circumstances e.g. tape replacement, the hold up time is undesirable. The On Line Adaptor ensures that in the event of a device being busy, the processor is not held up for longer than 2μs. If, within 2μs of a data transfer signal being output from the processor, the device becomes available, then the instruction is carried out normally. If the device remains busy, a pseudo reply is sent to the processor and the control logic is inhibited from making a data transfer.

The On Line Adaptor board also includes a set of lines which indicate the availablility of the devices and may be used in conjunction with an interrupt scanner.

The board is a type DP4 and is inserted in position 17 of the logic rack.

NOTE: When converting a system for use with an On Line Adaptor, the backwiring link between 16/25 and 16/57 must be removed.

1.2 On Line Operation.

The logic diagram of the board is shown in Figure 1, together with the component details.

With the On Line switch set to ON, a false signal is applied to 14/3B13 causing ON LINE to go true. This signal is inverted by 17/4B13 causing $\overline{\text{ON LINE}}$ to go false.

When an On Line Adaptor is not used, a link is inserted in the backwiring of board 16 and the output of 16/1A12 must go false before the interface timing chain is primed. This condition occurs when the device becomes not busy and the transfer signal is accepted.

When a data transfer is required SELECT goes true. With the On Line Adaptor present and the associated switch set to ON, SELECT and ON LINE being true causes the output of 17/1A13 to go false and trigger the monostable 17/2B/3A. This produces a 2μs TEST pulse at the end of which, pulse generator 17/3B13 is triggered to produce a 680 ns pulse. This pulse is inverted by 17/3A13 causing $\overline{\text{SET ACT}}$ to go false for 680 ns. The pulse sets the bistable 16/4A/4A to start the interface timing chain and cause [RTR] to go true. The bistable 17/2A/2A is reset by ON LINE such that $\overline{\text{INV}}$ is false. The signal applied to 15/3B13 and 16/4B13 causes the control logic to be inhibited when the interface timing chain signals occur.

If, during the 2μs TEST pulse, the device becomes available, the output of 16/1A12 goes false. This signal is inverted by 17/1A11 and then gated with TEST to set the bistable 17/2A/2A causing $\overline{\text{INV}}$ to go true, and remove its inhibit action. $\overline{\text{ON LINE}}$ prevents direct triggering of the timing chain at 17/1A12. $\overline{\text{SET ACT}}$ primes the timing chain at the end of the TEST pulse and a normal data transfer takes place. The bistable 17/2A/2A is reset when SELECT goes false.

1.3 Off Line Operation

If the On Line switch is set to OFF, $\overline{\text{ON LINE}}$ is true. In this case the processor is held up until a device becomes available and the output of 16/1A12 goes false. This signal is inverted by 17/1A11 and gated with $\overline{\text{ON LINE}}$ at 17/1A12. The resultant false signal sets the bistable 16/4A/4A to start the timing chain. ON LINE being false and applied to 17/2A13 ensures that $\overline{\text{INV}}$ is true and the inhibit action is removed. ON LINE also prevents generation of the TEST pulse.

1.4 READY Lines

1.4.1 T/P OUTPUT READY

The signal from 17/5B11 is normally true due to CLOCK BUSY being false and holding the bistable 17/4A/4A in a reset state. When a data output is sent to the teleprinter, CLOCK BUSY goes true and when the ACT** pulse occurs the bistable is set and T/P OUTPUT READY goes false. The false level is maintained until the transfer is completed and CLOCK BUSY goes false.

1.4.2 T/P INPUT READY

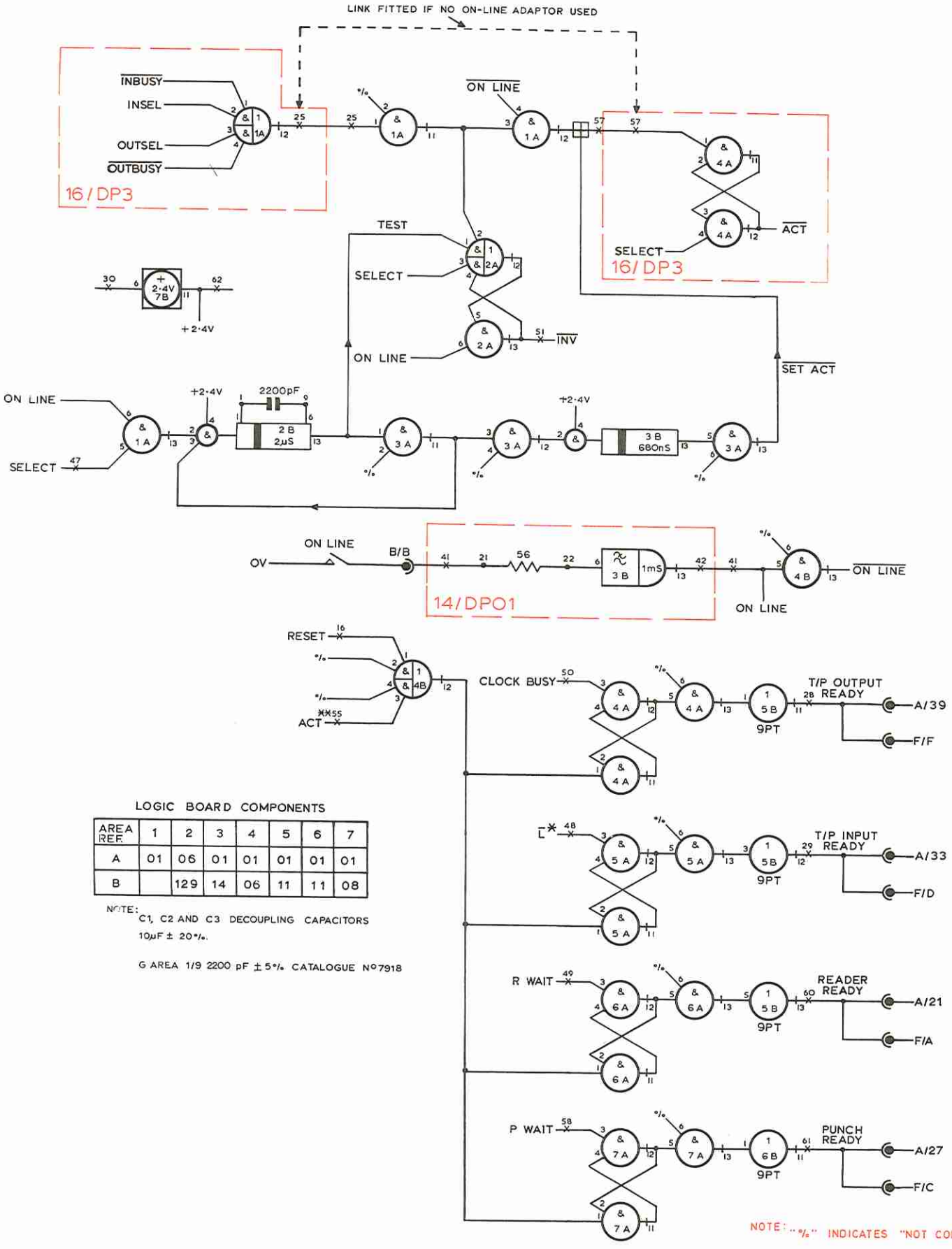
The signal $\overline{L*}$ applied to bistable 17/5A/5A is normally true so that when the first data transfer occurs and ACT** is produced, the bistable is set such that T/P INPUT READY is false. This condition can only be changed by pressing a key on the teleprinter or starting the printer reader. When the buffer register is loaded $\overline{L*}$ goes false to reset the bistable 17/5A/5A causing T/P INPUT READY to go true. After the character has been accepted by the processor $\overline{L*}$ goes true and with ACT** sets the bistable again. If a teleprinter output occurs before the character is taken from the buffer register, the character is overwritten by the processor output. $\overline{L*}$ goes true and the bistable 17/5A/5A set so that T/P INPUT READY is false.

1.4.3 READER READY

This signal from 17/5B13 is normally true due to RWAIT being false and holding the bistable 17/6A/6A in a reset state. When a data input is required RWAIT goes true and when the ACT** pulse occurs the bistable is set and READER READY goes false. The false level is maintained until the tape is advanced and the buffer register reloaded, RWAIT then goes false.

1.4.4 PUNCH READY

This signal from 17/6B11 is normally true due to P WAIT being false and holding the bistable 17/7A/7A in a reset state. When data is output to the punch, P WAIT goes true and with ACT** sets the bistable causing PUNCH READY to go false. The false level is maintained until punching has been completed and P WAIT goes false.



LOGIC BOARD COMPONENTS

AREA REF.	1	2	3	4	5	6	7
A	01	06	01	01	01	01	01
B		129	14	06	11	11	08

NOTE:
C1, C2 AND C3 DECOUPLING CAPACITORS 10μF ± 20%.

G AREA 1/9 2200 pF ± 5% CATALOGUE Nº7918

ON-LINE ADAPTOR DP4

Figure 1 (Issue 3)