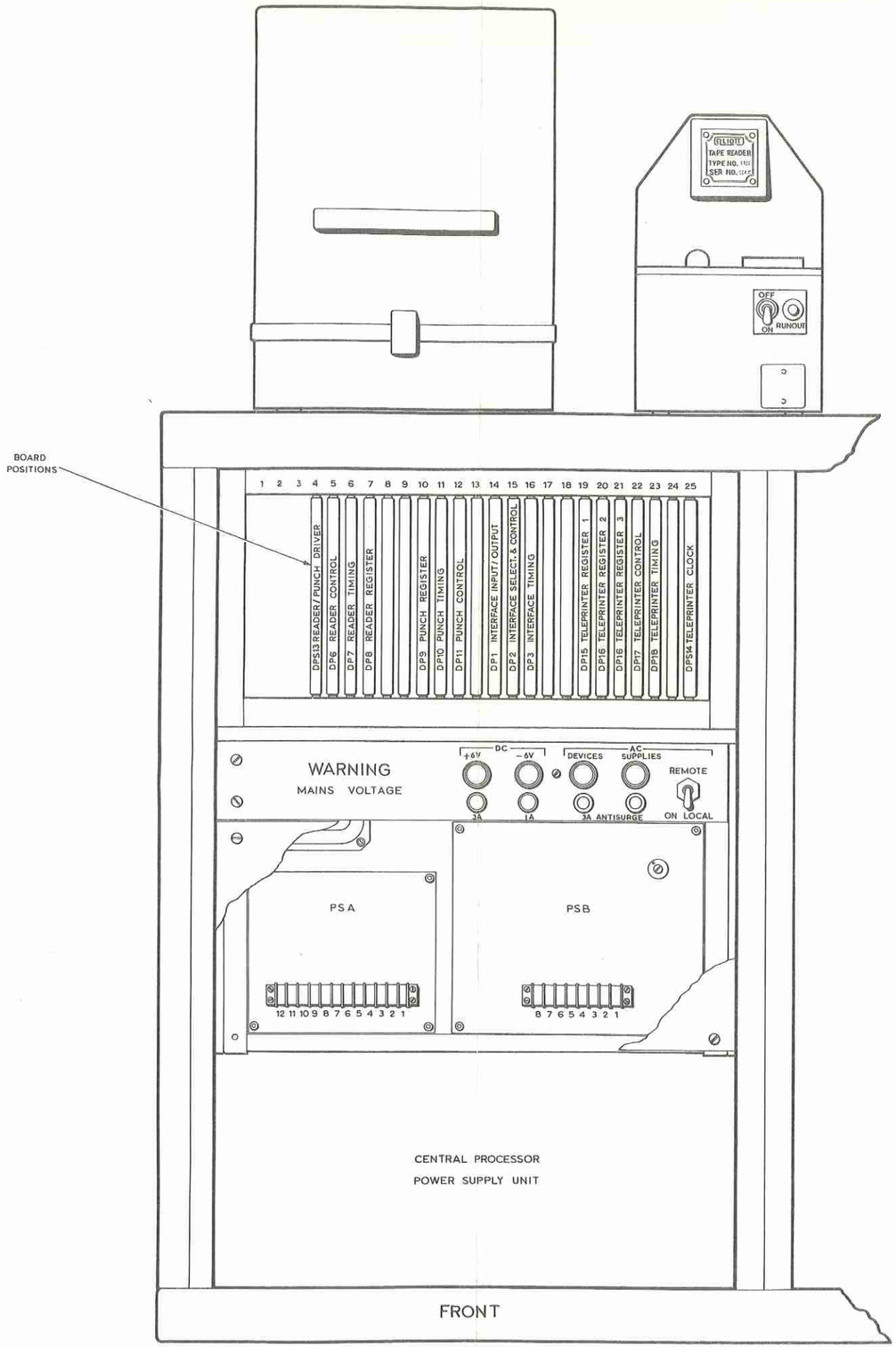
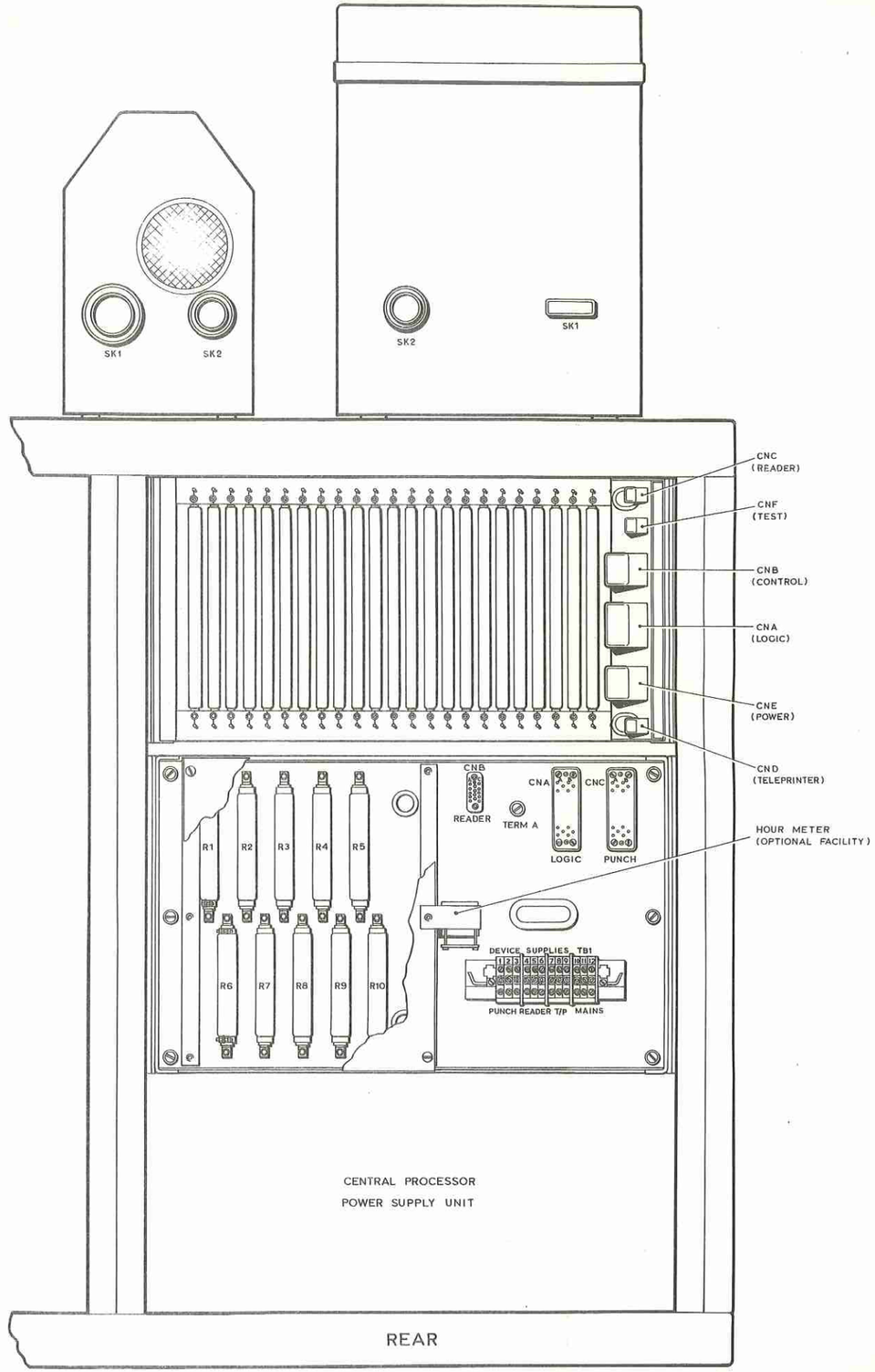




ure 1 *(ISSUE 3)*

PAPER TAPE STATION — LAYOUT

PAPER TAPE STATION CONNECTIONS

Figure 2 (ISSUE 2)

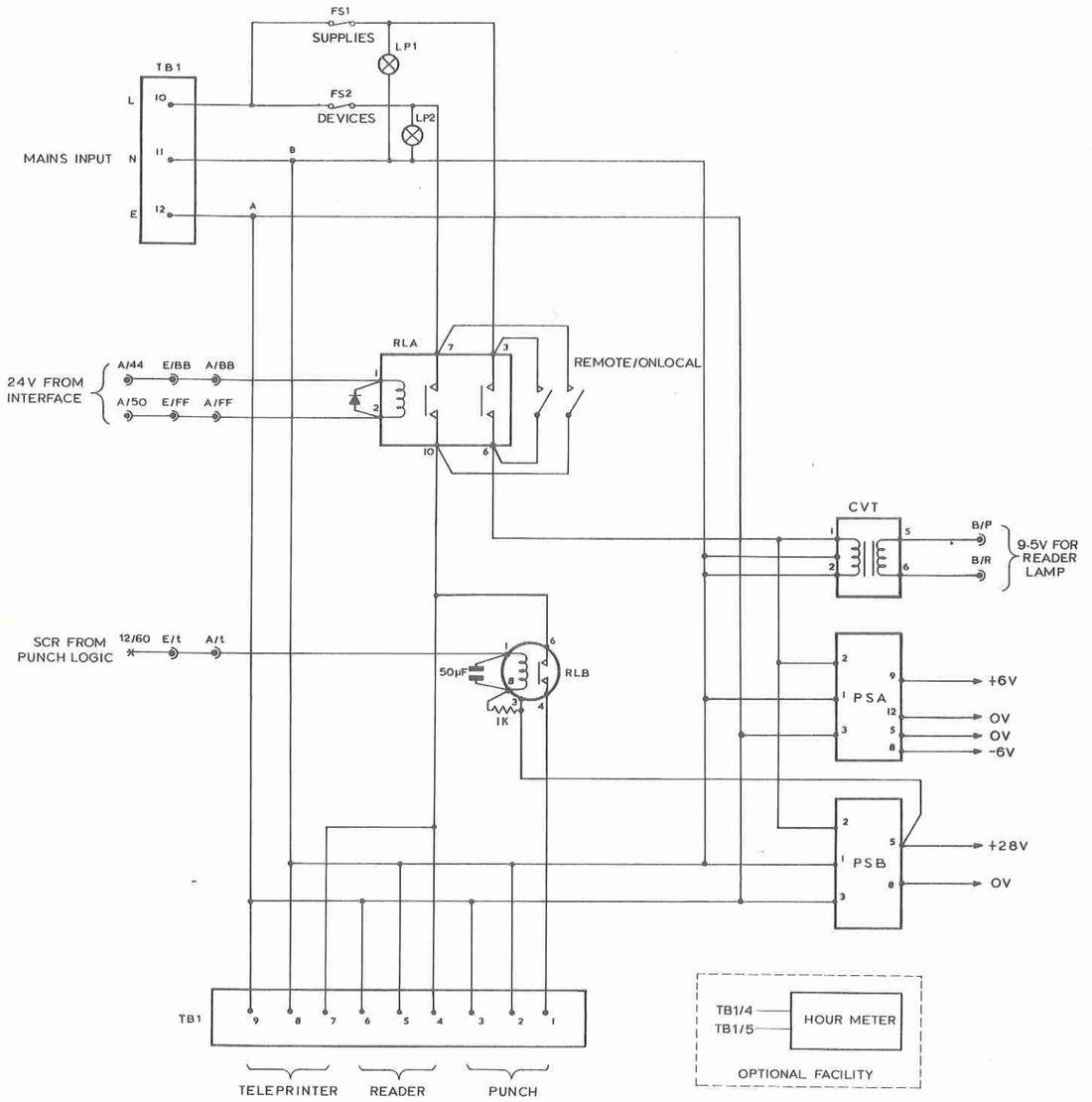
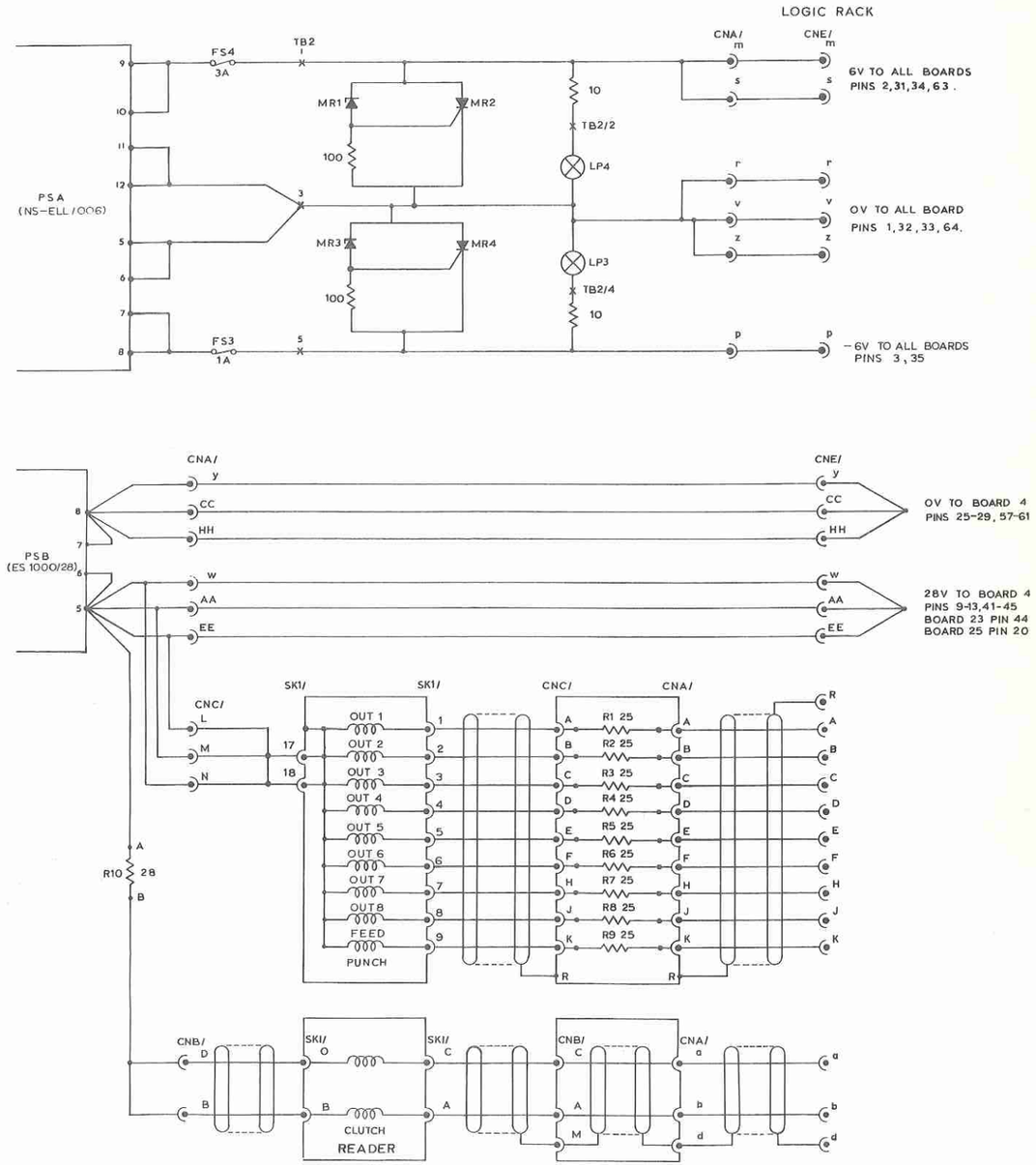


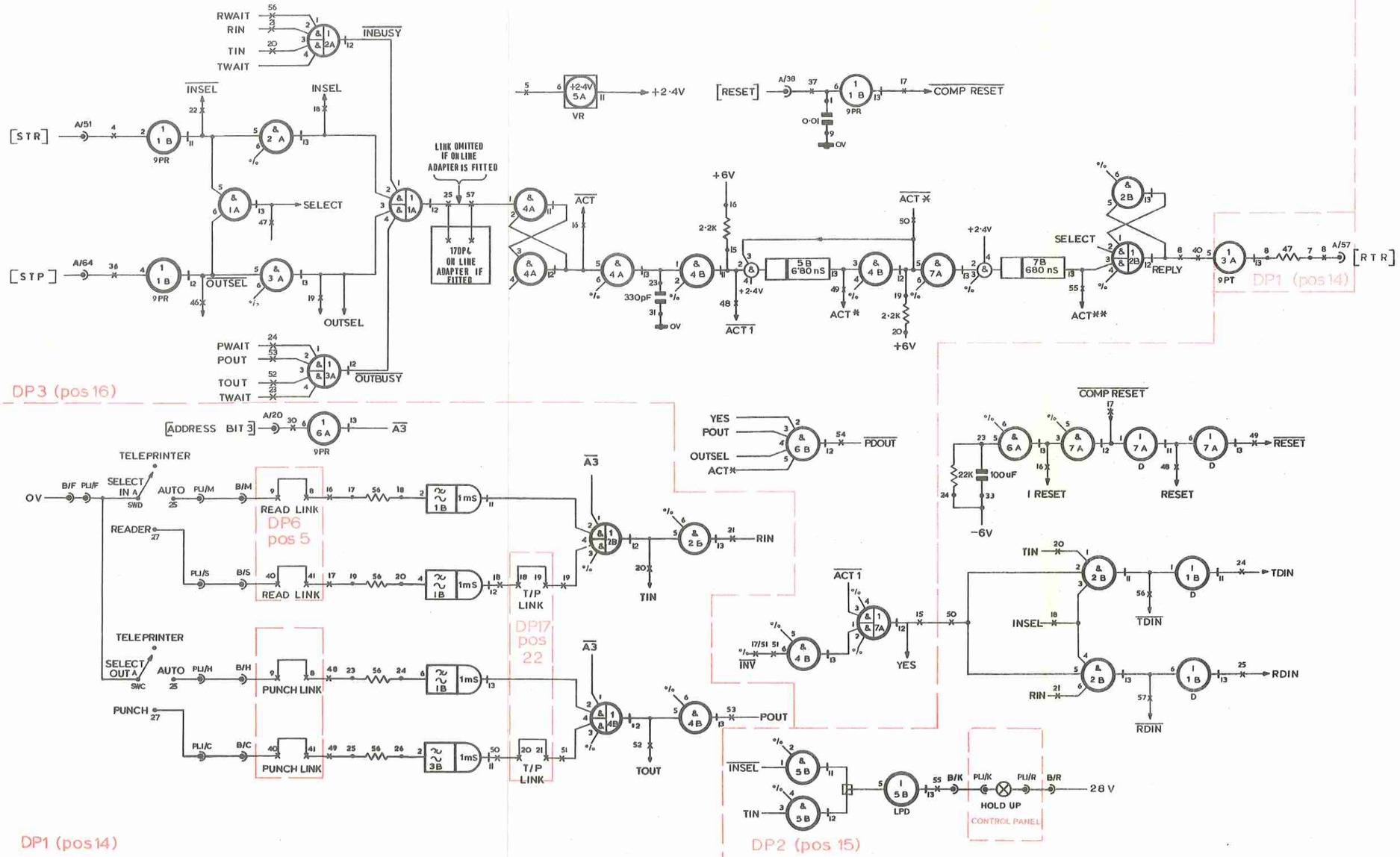
Figure 3 *(Issue 3)*

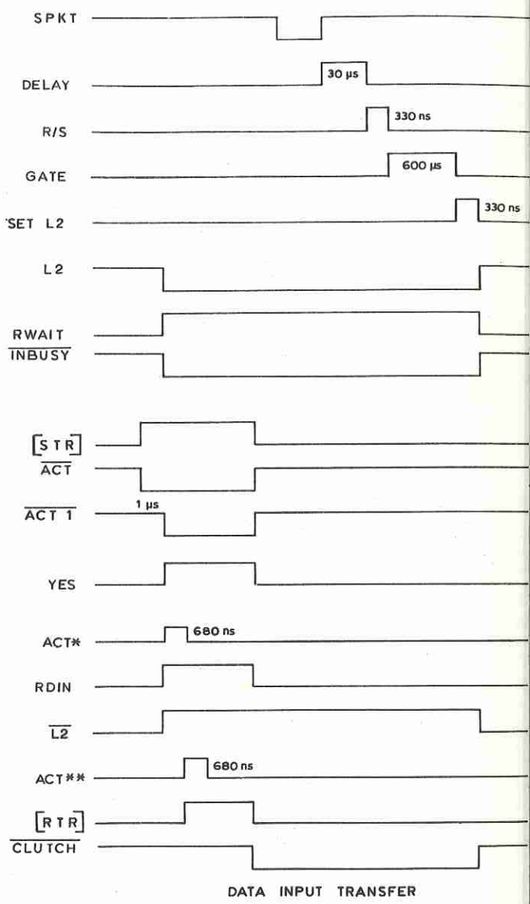
A.C. DISTRIBUTION



D.C. DISTRIBUTION

Figure 4 *(Issue 3)*

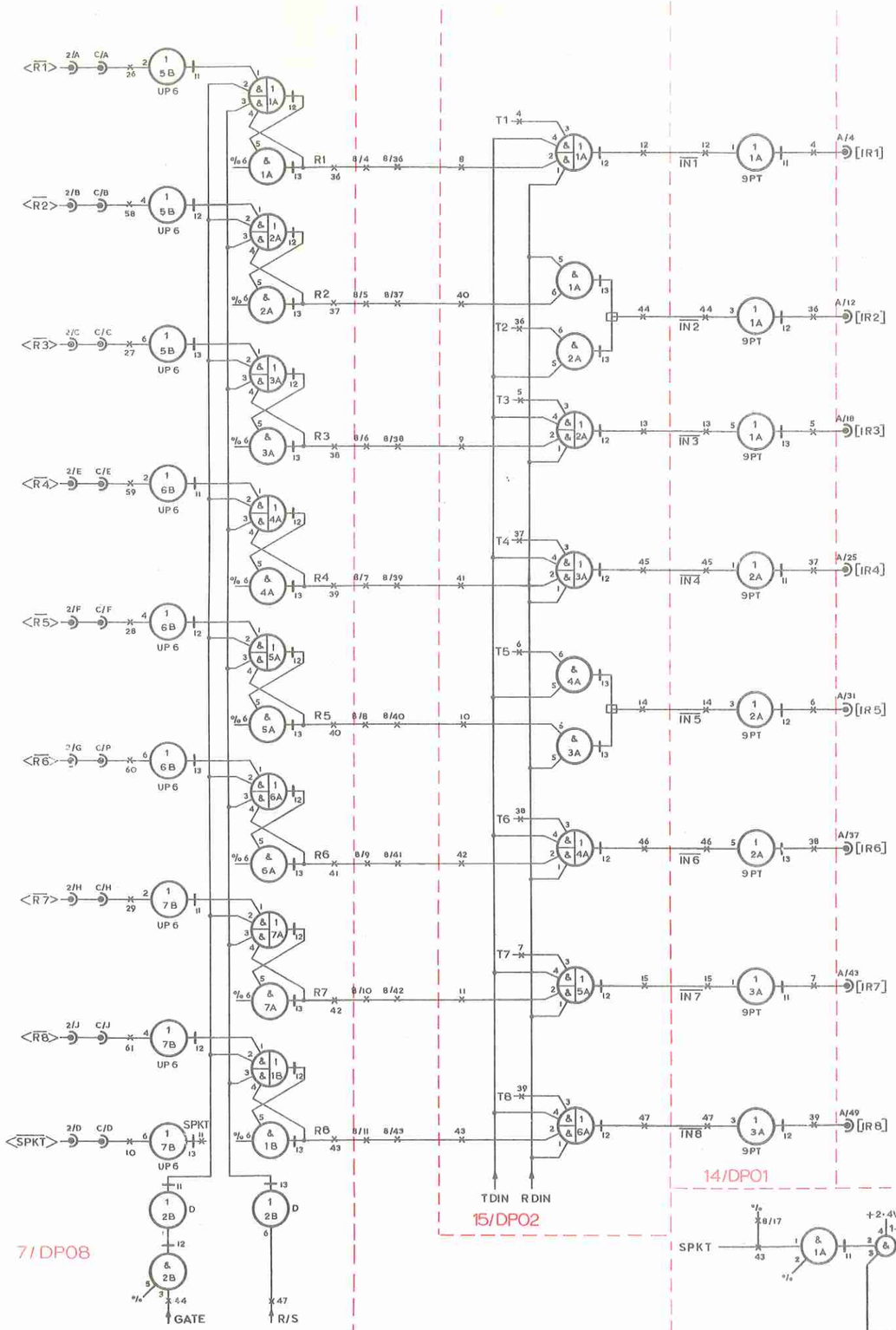




NOTE: "*/*" INDICATES "NOT CON

Figure 5 *(Issue 3)*

SELECTION AND TIMING



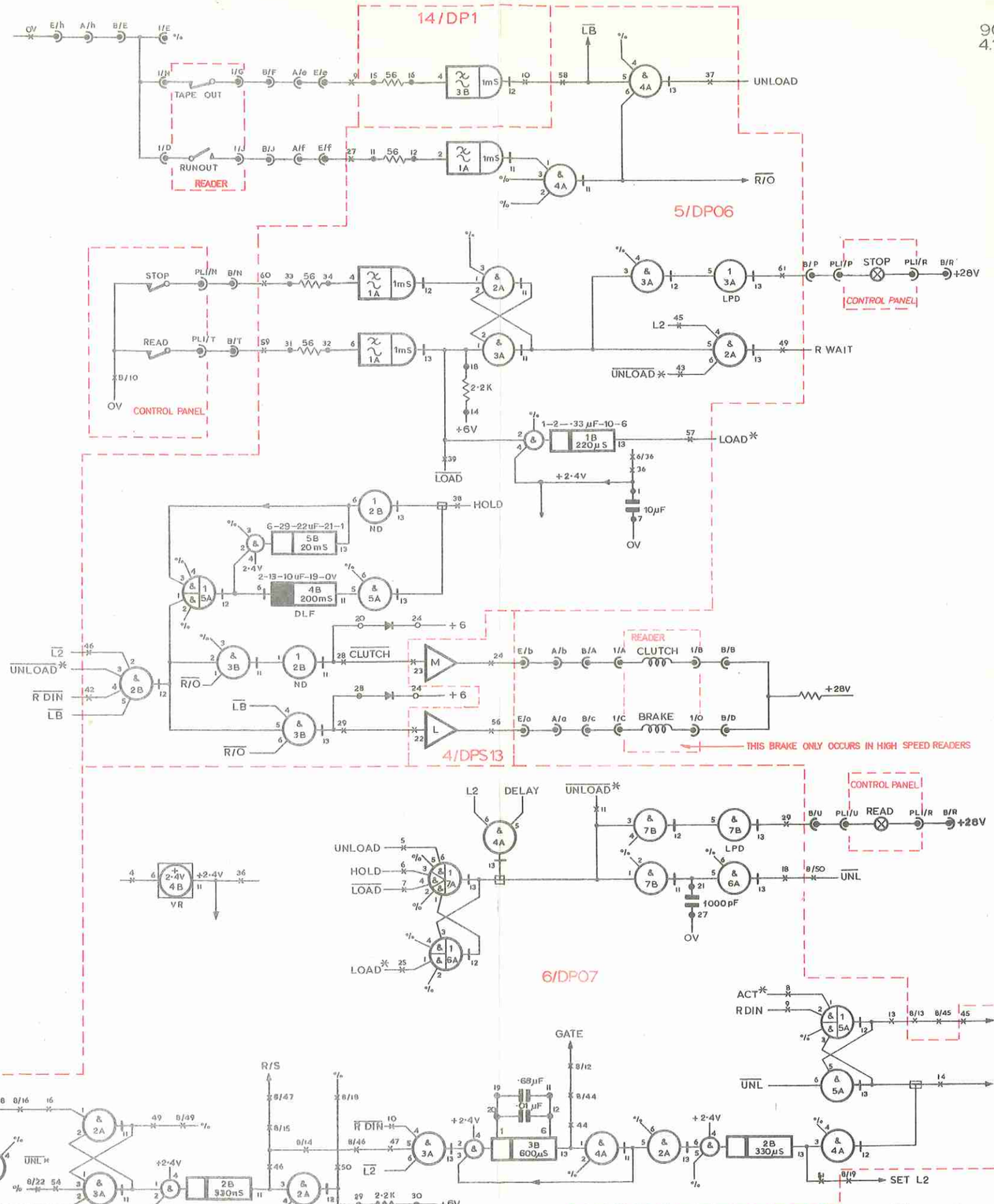


Figure 6 *(Issue 3)*

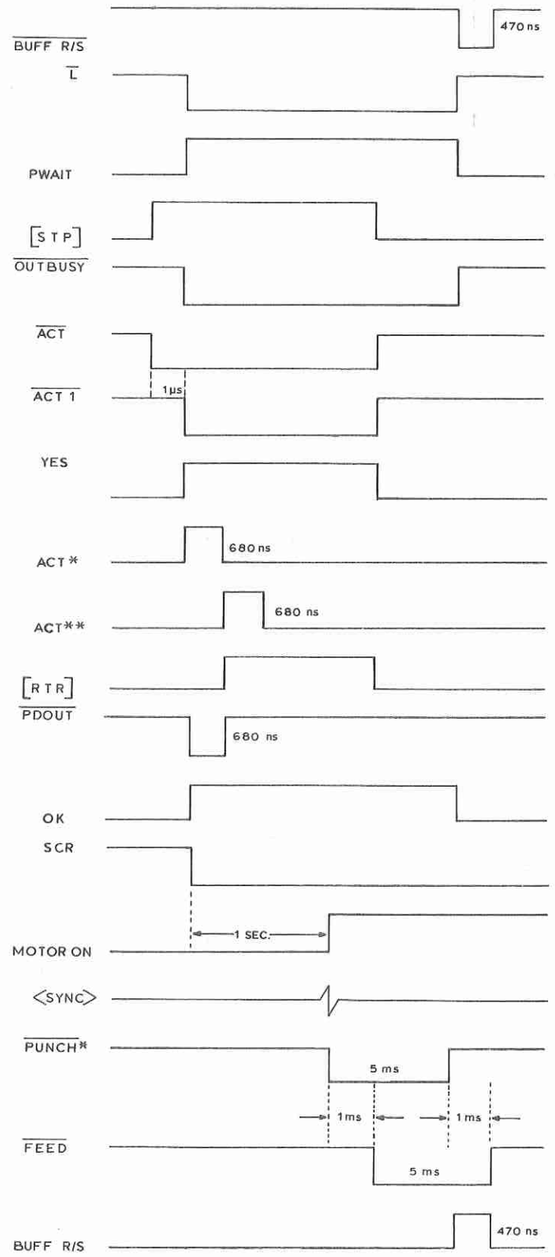
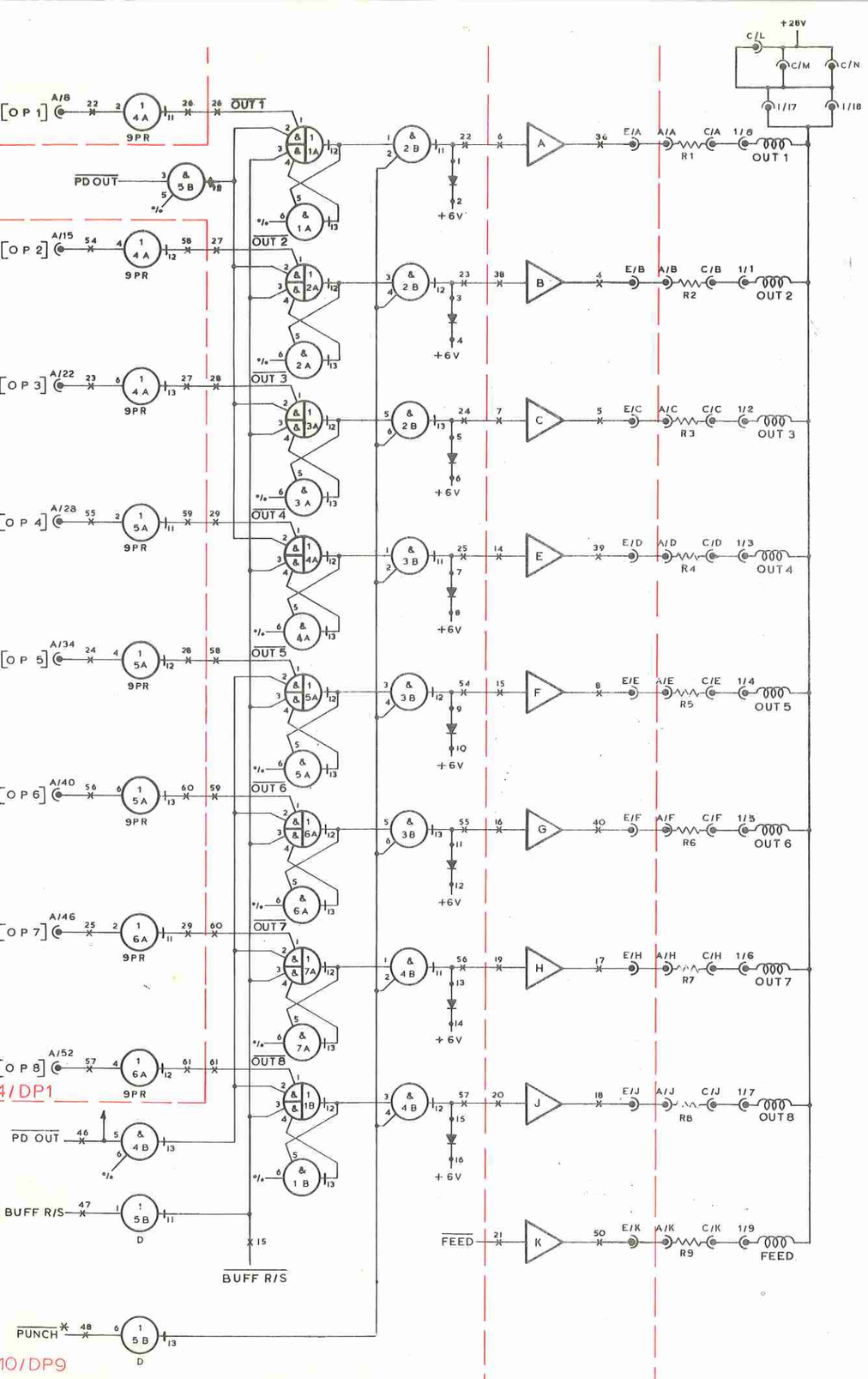


Figure 7 *(Issue 3)*

DATA OUTPUT TRANSFER

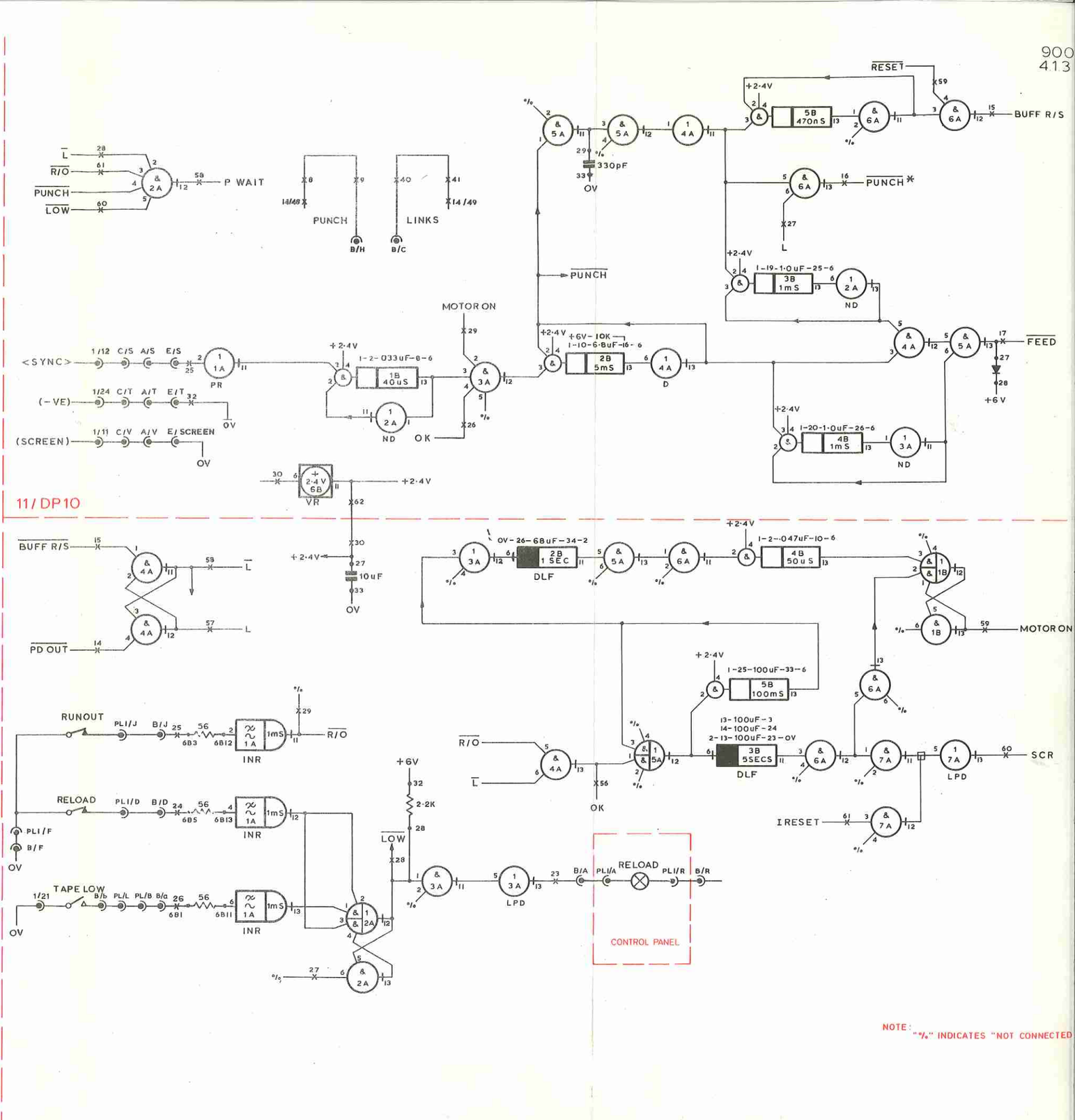


PUNCH CONTROL LOGIC

4/DPS 13

TAPE PUNCH

12/DP11



NOTE: "*" INDICATES "NOT CONNECTED"

Figure 8 *(Issue 31)*

Board Type	Board Position	G Area Pad Location	Value	Tolerance %	Cat No.
DP1	14	7/8	47Ω	5	9219
		15/16, 17/18, 19/20, 21/22, 23/24, 25/26	56Ω	5	9941
DP2	15	23/24	22K	5	9196
		23/33	100µF	5	9151
DP3	16	15/16, 19/20	2·2K	5	9160
		23/31	330pF	5	8479
		1/9	0·01µF	20	7610
DP6	5	1/7, 13/19	10µF	5	9309
		2/10	0·33µF	5	9369
		11/12, 31/32, 33/34	56Ω	5	9941
		21/29	22µF	5	9385
		14/18	2·2K	5	9160
		20/24 24/28	DIODE		11010 (PS226)
DP7	6	2/10	0·033µF	5	7720
		11/19	0·68µF	5	9430
		12/20	0·01µF	5	7922
		21/27	1000pF	5	7917
		29/30	2·2K	5	9160
DP9	10	1/2, 3/4, 5/6, 7/8, 9/10, 11/12, 13/14, 15/16	DIODE		11010 (P.S. 226)
DP10	11	2/8	0·033µF	5	7720
		10/16	6·8µF	5	9398
		17/18	10K	5	
		19/25, 20/26	1·0µF	5	9386
		27/28	DIODE		11010 (P.S.226)
		29/33	330pF	5	8479
DP11	12	2/10	0·047uF	5	7044
		3/13, 13/23, 14/24, 25/33	100µF	5	9151
		26/34	68µF	5	9308
		27/33	10µF	5	9309
		6B1/6B11, 6B3/6B12, 6B5/6B13	56Ω	5	9941
		28/32	2·2K	5	9160

Board Type	Board Position	Area Reference											
		1A	1B	2A	2B	3A	3B	4A	4B	5A	5B	6A	6B	7A	7B
DP 1	14	11	18	11	06	11	18	12	06	12		12			
DP 2	15	06	15	06	02	06	02	06	26	06	26	06		15	
DP 3	16	06	12	06	06	06		01	01	08	14		03	06	14
DP 6	5	18	129	02	03	26	02	02	27	06	129				
DP 7	6	01	129	01	13	02	129	01	08	06		06		05	26
DP 8	7	06	06	06	15	06		06		06	33	06	33	06	33
DP 9	10	06	06	06	01	06	01	06	01	06	15	06		06	
DP10	11	17	129	03	129	03	129	15	129	01	09	01	08		
DP11	12	18	06	06	27	26	27	01	129	06	129	01		26	

NOTE

1 On all boards decoupling capacitors C1, C2 & C3 are 10µF ± 20%. Catalogue Nº 9137

2 D.C. Supplies to all boards

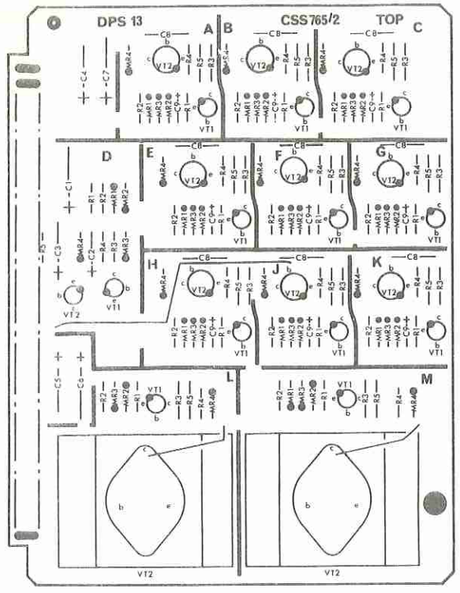
+ 6V pins 2, 31, 34, 63

− 6V pins 3, 35

0V pins 1, 32, 33, 64

LOGIC BOARD COMPONENTS

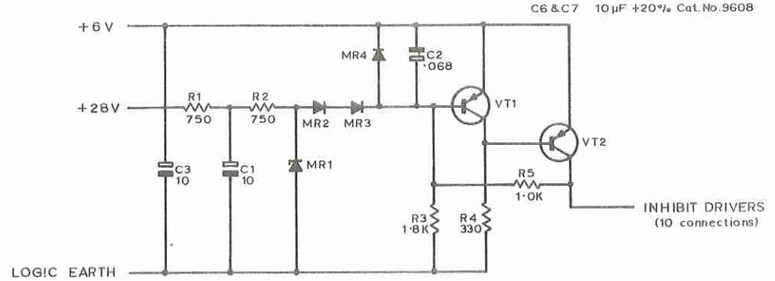
Figure 9 (Issue 3)



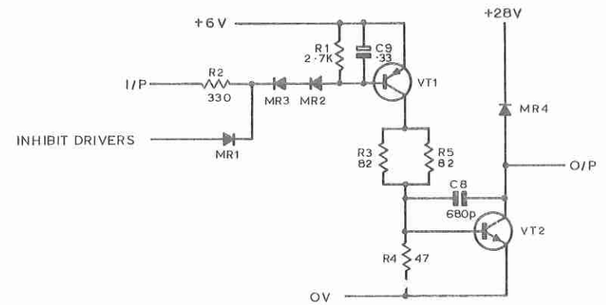
UNDER VOLTAGE PROTECTION CIRCUIT COMPONENT TABLE				
R	Value	Tol ± %	Voltage	Cat. No.
1, 2	750	5		10913
3	1.8K	5		6304
4	330	5		9186
5	1.0K	5		9159
C				
1	10µF	20		9608
2	0.068µF	5		8481
3	10µF	20		9137
MR		P.S. No.		
1	ZENER DIODE			7606
2 to 4		221		8846
VT				
1 2		219		11009

DRIVER CIRCUIT COMPONENT TABLE				
R	Value	Tol ± %	Voltage	Cat. No.
1	2.7K	5		9186
2	330	5		9161
3 5	82	5		6388
4	47	5		9219
MR		P.S. No.		
1 to 3		221		8846
4				9434
VT				
1		219		11009
2	AREA A to C			
	E to K	200		9135
	AREA L, M			9333
C9	0·33µF	5		
8	680pF	5		

Decoupling Capacitors
C4 & C5 10µF ±20% Cat. No. 9137
C6 & C7 10µF ±20% Cat. No. 9608



UNDER VOLTAGE PROTECTION CIRCUIT (AREA D)



DRIVER CIRCUIT (AREAS A,B,C,E to M)
(MR1 absent on circuit in area L)

Appendix 1: 500 c.p.s. TAPE READER (DPA 222)

1.1 Introduction

An optional facility for the 900 system is the use of a tape reader which can operate at a rate of 500 c.p.s.

The installation of this facility requires the fitting of one extra logic board and several back wiring changes. The sockets on the two readers are identical so that no new connecting cables are required.

The extra board is a type DP12 and is fitted into position 8 of the PTS logic rack. The inclusion of this board introduces a second buffer register stage into the data path from the reader to the central processor interface lines.

The control logic for the fast reader is shown in Figure 2 of this Appendix and should be used in place of Figure 6 in the end-of-text figures. A timing diagram to replace the one shown on Figure 5 of the end-of-text figures is located on Figure 1 of this Appendix. Component details of the board are also shown on Figure 1.

1.2 Data Flow

Data from the reader, in the form of an 8 bit character, is gated into the first buffer and then into the second buffer for storage until a request is sent by the central processor.

When the tape is first loaded and the Read button operated, the first character detected is passed to the second buffer. Due to the speed of the reader, the brake does not stop the tape before the next character appears under the read head. This character is gated into the first buffer.

On receipt of a data input request from the central processor, the contents of the second buffer are gated onto the interface lines. When the request signal is terminated the contents of the first buffer are transferred to the second buffer and tape movement is commenced. The period of the tape drive is short enough for the brake to stop the tape within the next character. This character is entered into the first buffer.

1.3 Read Button

The Read button is operated to reset the reader logic after a new tape has been loaded or to restart after a stop action. The logic associated with this button is unchanged from that used for the 250 c.p.s. reader. Operation of the button causes the Unload bistable 6/7A13, 6/6A12 to be set such that $\overline{\text{UNLOAD*}}$ is true. $\overline{\text{CLUTCH}}$ goes false and tape movement is commenced. Tape is advanced until a sprocket hole is detected when <$\overline{\text{SPKT}}$> goes false.

1.4 Initial Buffer Loading

The data lines <$\overline{\text{R1}}$> to <$\overline{\text{R8}}$> go false before <$\overline{\text{SPKT}}$> is detected. When <$\overline{\text{SPKT}}$> goes false the monostable 6/1B13, 6/1A12 is triggered, the 30 µs pulse R/S1 being fed to 7/2B13 to reset the bistables in the first buffer register. The monostable output sets the bistable 6/2A11, 6/3A11 causing GATE 1 to go true. At the end of the R/S1 pulse, GATE 1 fed to 7/2B12 loads the data from the reader into the first buffer register.

When the character has passed the read head, <$\overline{\text{SPKT}}$> goes true and resets the bistable 6/2A11, 6/3A11 causing GATE 1 to go false. The monostable 6/2B11, 6/2A12 is triggered to produce a 330 ns pulse to set the bistable 8/7B13, 8/7B12 causing L1 to

go true to indicate that the first buffer is loaded. L1 gated with $\overline{\text{RDIN}}$ and $\overline{\text{L2}}$, which are both true, causes the monostable 6/3B13, 6/4A11 to be triggered and a 10 µs R/S2 pulse to be fed to 8/2B13. The second buffer register is reset. At the end of the R/S2 pulse, the 330 ns pulse GATE 2 is generated by 6/2B13 and fed to 8/2B12 to gate the data from the first to the second buffer. GATE 2 also sets the bistable 6/5A13, 6/5A12 causing L2 to go true to indicate that the second buffer is loaded and resets the bistable making L1 false. $\overline{\text{L2}}$ going false causes $\overline{\text{CLUTCH}}$ to go true and $\overline{\text{BRAKE}}$ false and tape movement is stopped.

Due to the speed of the tape, movement will not stop until the next character has reached the read position and <$\overline{\text{SPKT}}$> goes false again. As previously described the data is loaded into the first buffer and L1 set true. Since $\overline{\text{L2}}$ is false, the gate 6/3A13 is inhibited and the data remains in the two buffer registers.

1.5 Data Input

When a data input is required, the central processor makes the interface signal [STR] true. The data transfer is then as described in paragraph 3.5.1 of this section. $\overline{\text{RDIN}}$ going false during the transfer maintains the inhibit on gate 6/3A13.

At the end of the transfer when [STR] goes false, $\overline{\text{RDIN}}$ goes true. Since the data has been gated from the second buffer, $\overline{\text{L2}}$ has been reset true and the output of 6/3A13 goes false to generate the R/S2 and GATE 2 pulses. The next character is transferred from the first to the second buffer register and $\overline{\text{L2}}$ is set false.

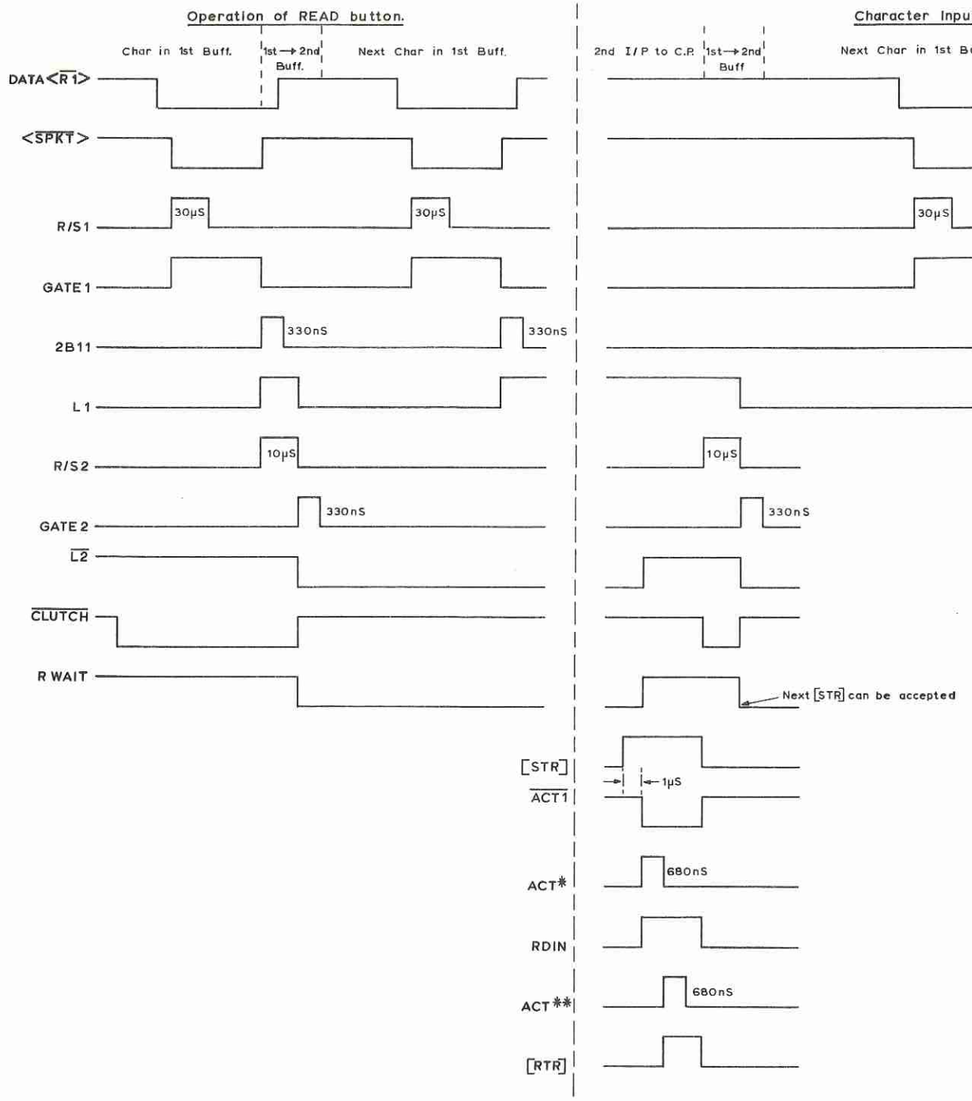
During this transfer time $\overline{\text{CLUTCH}}$ is also false and tape is advanced. The movement is initiated by $\overline{\text{RDIN}}$ going true

and terminated when $\overline{L2}$ goes false. $\overline{CLUTCH}$ is therefore false for 10 µs and allows only one character to pass under the read head. The tape is stopped within this character which is loaded into the first buffer and L1 is set true.

The next [STR] signal can be accepted as soon as the second buffer has been loaded and L2 goes true causing RWAIT to go false. This allows for data to be output to the central processor at the same time as the first buffer is being loaded with the next character.

1.6 Creep Error

In the event of excess tape movement the next character appears under the read head when the first buffer is still loaded and L1 is true. <$\overline{SPKT}$> goes false and generates the R/S1 pulse. L1 and R/S1 gated at 6/4A13 cause the Unload bistable to be reset and $\overline{UNLOAD}$* to go false. Further reading of the tape is prevented until the fault has been cleared.



BOARD TYPE DP12 CAT No B25248
LOGIC BOARD COMPONENTS

AREA REF.	1	2	3	4	5	6	7
A	06	06	06	06	06	06	06
B	06	15					06

C1, C2 and C3 decoupling capacitors 10μF ± 20% Cat. No. 9137

500. C.P. S. TIMING DIAGRAM.

Appendix 1.
Figure 1 (ISSUE 2)

500 c.p.s READER CONTROL LOGIC

Appendix 1
Figure 2 (ISSUE 2)