



L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX FAN OUT LOAD IN UNIT INPUTS	GENERAL			REMARKS.
				0 - 80°C	-20 - 80°C	-40 - 80°C	
O1 2 INPUT NAND GATES		1.2	11	9	8	8	I INPUT = 1 UNIT INPUT TYPICAL SWITCH ON TIME = 10ns. (O/P -VE GOING) FROM +2V TYPICAL SWITCH OFF TIME = 16ns. (O/P + VE GOING) TO +1.2V.
O2 3 INPUT NAND GATES		1.2	11	9	8	8	SPEED OF +VE GOING EDGE DETERMINED BY NO. OF FAN OUT, STRAY CAPACITY, CAPACITY OF BACK BIASED DIODES & UNSELECTED LOADS. CAPACITIVE LOADING COULD TOTAL 200 PF. AND CAUSE 50ns. DELAY, THIS MAY BE REDUCED BY ADDING AN R TO +6V.
O3 4 I/P NAND GATE PLUS 2 INVERTERS		1.2	11	9	8	8	BUT AVAILABLE FAN OUT IS REDUCED. E.G. PULL UP OF 2K REDUCES FAN OUT BY 1 UNIT.
O4 CONTROL MATRIX WAVEFORM AMPLIFIERS		2.5	3	2	2	2	USED FOLLOWING A MATRIX DIODE. 1 INPUT = 0.6 UNIT INPUTS.
O5		1.2	11	9	8	8	AS FOR L.S.A'S O1, O2 AND O3.

DRAWN C.A.C.  
CHECKED CS 456  
APPR. VERD. ERK  
DATE 26-4-66  
INITIALS C.A.C.  
15/5/66

ISSU. NO 1374  
A.R. NO 1374  
DATE 26-4-66  
INITIALS C.A.C.

ELLIOTT BROTHERS

(LONDON) LTD.

L.S.A. DESIGN NOTES.

INSTRUCTION SHEET  
322A7191

SHEET NO 2  
OF

L.S.A. No. AND NAME.	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX FAN OUT LOAD IN UNIT INPUTS.	GENERAL +6V RAIL	REMARKS		
					AT 0-80°C	AT -20-80°C	AT -40-80°C
06		1.2	11		9	8	AS FOR LSA'S 01, 02, AND 03.
07		2.4	17	16	14		$\Delta = 100\text{n.s.} \pm 10\%$ I INPUT = 3 UNIT INPUTS. USED WITH LSA 08 (2.4 V. REF.QEN) LEADS SHOULD BE KEPT SHORT TO AVOID +VE QINQ O/P PULSES BEING SHORTENED. SEE NOTES ON C. LOADING IN LSA'S 01, 02 AND 03.
08		—	50	50	50	50	USED AS 2.4 V REFERENCE. SUPPLIER TO PULSERS 07, 09, 13 AND 14. A PULSER INPUT FOR THIS LSA = 2.0 UNIT INPUTS.
09		2.4	17	16	14		I INPUT = 3 UNIT INPUTS. $\Delta = 470\text{n.s.} \pm 10\%$ USED WITH LSA 08.
11		1.2	6	4	3		I INPUT = 1 UNIT INPUT. USED PRECEDING LSA 12 OR LSA 17.

DRAWN C.A.C.  
CHECKED CS 456  
APPROVED Edt  
DATE 10/5/66  
INITIALS C.A.C.

ISSUE NO. 1  
AR. No. 1374  
DATE 26-4-66  
C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

INSTRUCTION SHEET

L.S.A. DESIGN NOTES

322A 7191

SHEET NO. 3  
OF

L.S.A.	B.S.	I/P	MAX.FAN OUT LOAD	GENERAL	+6V RAIL	REMARKS
DRAWN BY C.H.E. FD CS 456	ISSUE NO. 1	THRESHOLD VOLTAGE AT 25°C	IN UNIT INPUTS 0 - 80°C -20 - 80°C -40 - 80°C	A UNIT INPUT - DIODE PURCHASED	2.2kΩ ± 5%	
NO. AND NAME	C.A.C.	LOGIC SYMBOL				USED FOLLOWING LSA II - FAN OUT CALC. WHEN CONNECTED TO LSA II.
12 CABLE RECEIVERS		1 + 1 + 1 +	2.0	31	30	26
13 PULSE GENERATORS		1 + 1 +	2.4	17	16	1 INPUT = 3 UNIT INPUTS. Δ = 330 ns ± 10% USED WITH LSA 08.
14 PULSE GENERATOR		1 + 1 +	2.4	17	16	1 INPUT = 3 UNIT INPUTS. Δ = 680 ns ± 10% USED WITH LSA 08
15 2 I/P NAND GATE PLUS 2 INVERTING DRIVERS.		1 + 1 + 1 +	1.2	19	16	1 INPUT = 2.2 UNIT INPUTS. LARGER FAN OUT THAN LSA II. PROVIDES GOOD +VE EDGES. SUITABLE FOR GATING LOONS. PULSE INTO REGISTERS. AS FOR LSA'S O1, O2 AND O3.
16 F-MINIMOSI LOG DRIVERS.		1 + 1 + 1 +	1.2	9	8	1 INPUT = 1 UNIT INPUT.

APPROVED: J.R.W.  
DATE: 10/5/66  
INITIALS: C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

INSTRUCTION SHEET

LSA DESIGN NOTES.

322A7191

SHEET No 4  
OF

L.S.A. No. AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX FAN OUT LOAD IN UNIT INPUTS.	GENERAL +6V RAIL	REMARKS.
17 PAPER TAPE RECEIVER.	—○— —○—	2.0	30 29 25	A UNIT INPUT: —► Diode Purch 101	USED FOLLOWING LSA 11 - FAN OUT CALC. WHEN CONNECTED TO LSA 11.
18 SINGLE I/P NOISE REJECTION INVERTORS	-☒△+ -☒△+ -☒△+	2.0	28 26 23	INPUT = 2.2 UNIT INPUTS. USUALLY USED FOLLOWING A KEY SWITCH TO AVOID SWITCH NOISE. $\Delta \approx 1\text{ms}$ .	
19 & 20 DELAY	+☒△-	3.0	20 19 17	INPUT = 1 UNIT INPUT. USUALLY USED IN POWER SUPPLY LOGIC. $\Delta \approx 94\text{ms}$ .	
19 & 21 DELAY	+☒△-	3.0	20 19 17	INPUT = 1 UNIT INPUT. USUALLY USED IN POWER SUPPLY LOGIC. $\Delta \approx 22\text{ms}$ .	
22 TWO I/P TRANSMI- TTERS.	○ ○ ○	0		INPUT = 2.2 UNIT INPUTS. USED PRECEDING LSA 23. DATA O/P TO 50Ω COAX. MAY DRIVE UP TO 2 SELECTED AND 10 UNSELECTED LSA 23's.	

DRAWN C.S. 456  
CHECKED C.S. 456  
APPR. VED C.S. 456  
DATE 10/5/66  
INITIALS C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

L.S.A. DESIGN NOTES.

INSTRUCTION SHEET

322A 7191

SHEET No 5  
OF

L.S.A. No AND NAME	B.S. LOGIC SYMBOL	I/P THRESHOLD VOLTAGE AT 25°C	MAX. FAN OUT LOAD IN UNIT INPUTS.	GENERAL. +6V RAIL	REMARKS
21 CATED RECEIVERS		2.0	9	6	A UNIT INPUT =  DIODE PURCHASED
24-27 USED BY D.P.D.					
28 2 I/P NAND GATES.		1.2	28	23	INPUT = 2:2 UNIT INPUTS. USED AS A SELECTION DRIVER FOR LSA 23. IN O/P LOADING CALC. A SELECTED LSA 23 = 4.0 UNIT INPUTS AND ANY O/P LOAD ON THE LSA 23 SHOULD BE ADDED TO LSA 28 TOTAL.
43 VOLTAGE RAIL SENSING			1	1	
44 2 I/P NAND GATES		1.9 1.2	//	9	AS FOR LSA 21, O/P = O3 INPUTS 1, 2 & 5 HAVE A HIGH THRESHOLD FOR USE FOLLOWING AN L.S.A 23

DRAWN C.A.C. ISSUE NO. 1 2 3  
 CHECKED CS456 A.R. No. 1374 1588 1796  
 APPROVED DRH DATE 26-4-66 26-8-66 26-11-66  
 DATE 16/5/66 INITIALS C.A.C. KG

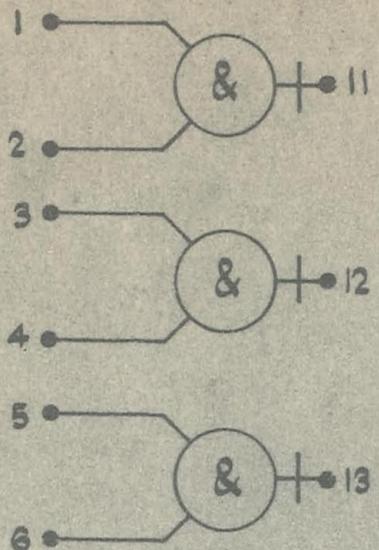
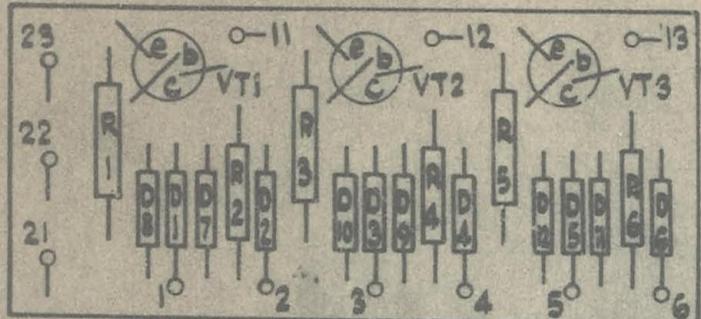
ELLIOTT BROTHERS (LONDON) LTD.

TITLE  
L.S.A. DESIGN NOTES.

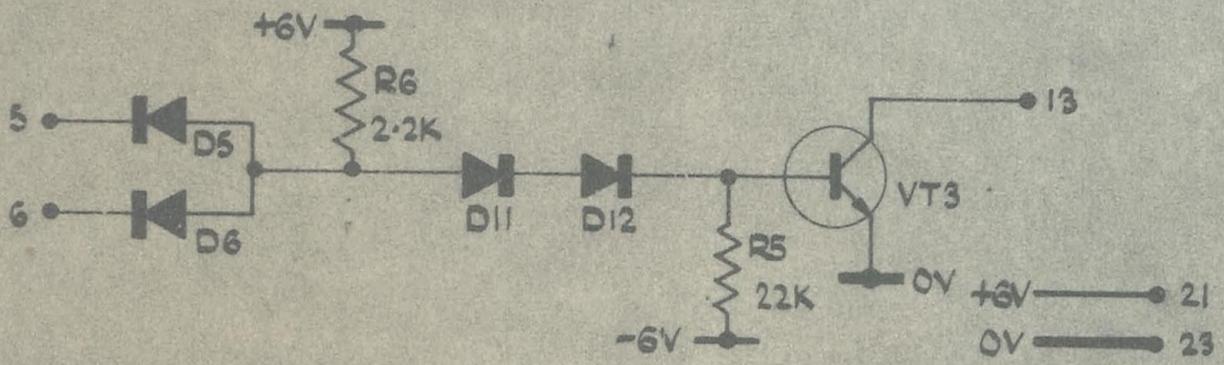
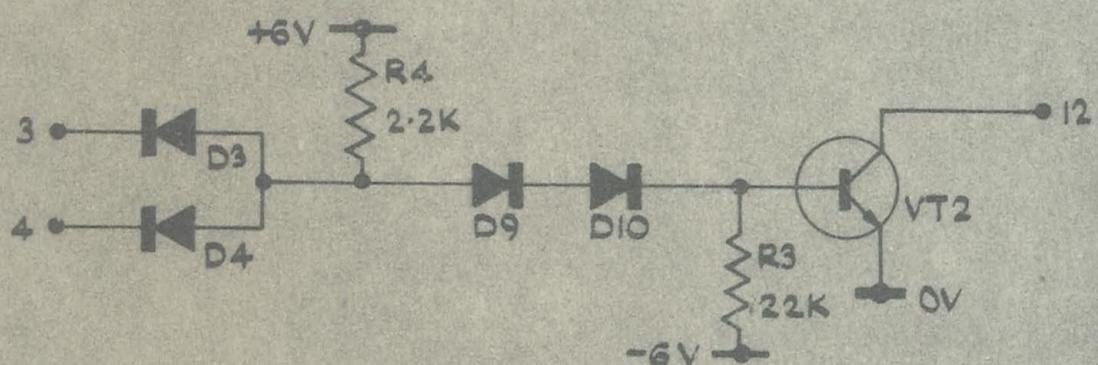
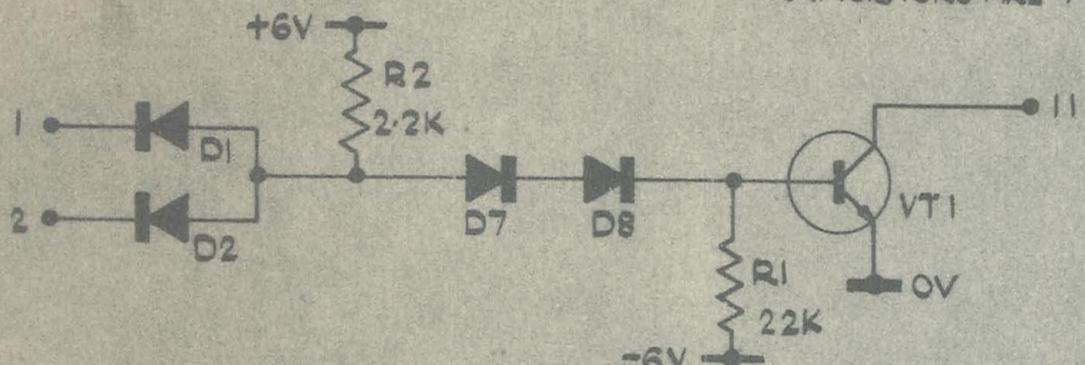
INSTRUCTION SHEET

322A 7191

SHEET NO 6  
OF



DIODES ARE PURCH. 101  
TRANSISTORS ARE PURCH. 100



DRAWN	C.A.C.	ISSUE NO.	1
CHECKED	CS 456	A.R.N.	1374
APPROVED	E.R.H.	DATE	26-4-66
TYPE	10256	INITIAL	C.A.C.

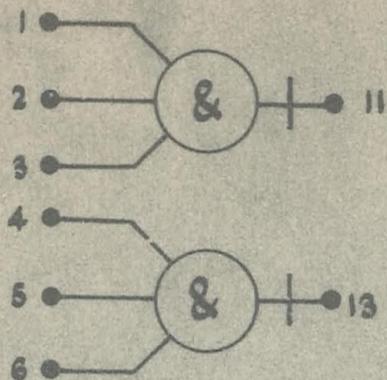
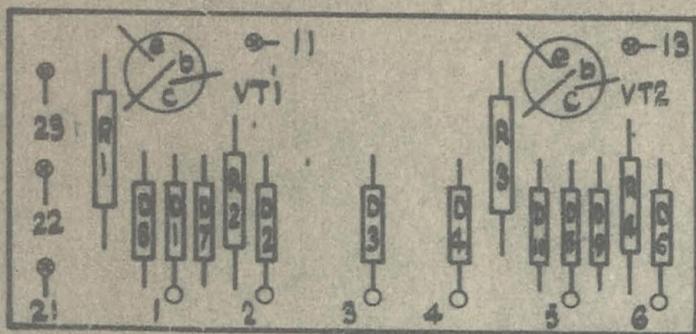
ELLIOTT BROTHERS (LONDON) LTD.

TLF LSA 01  
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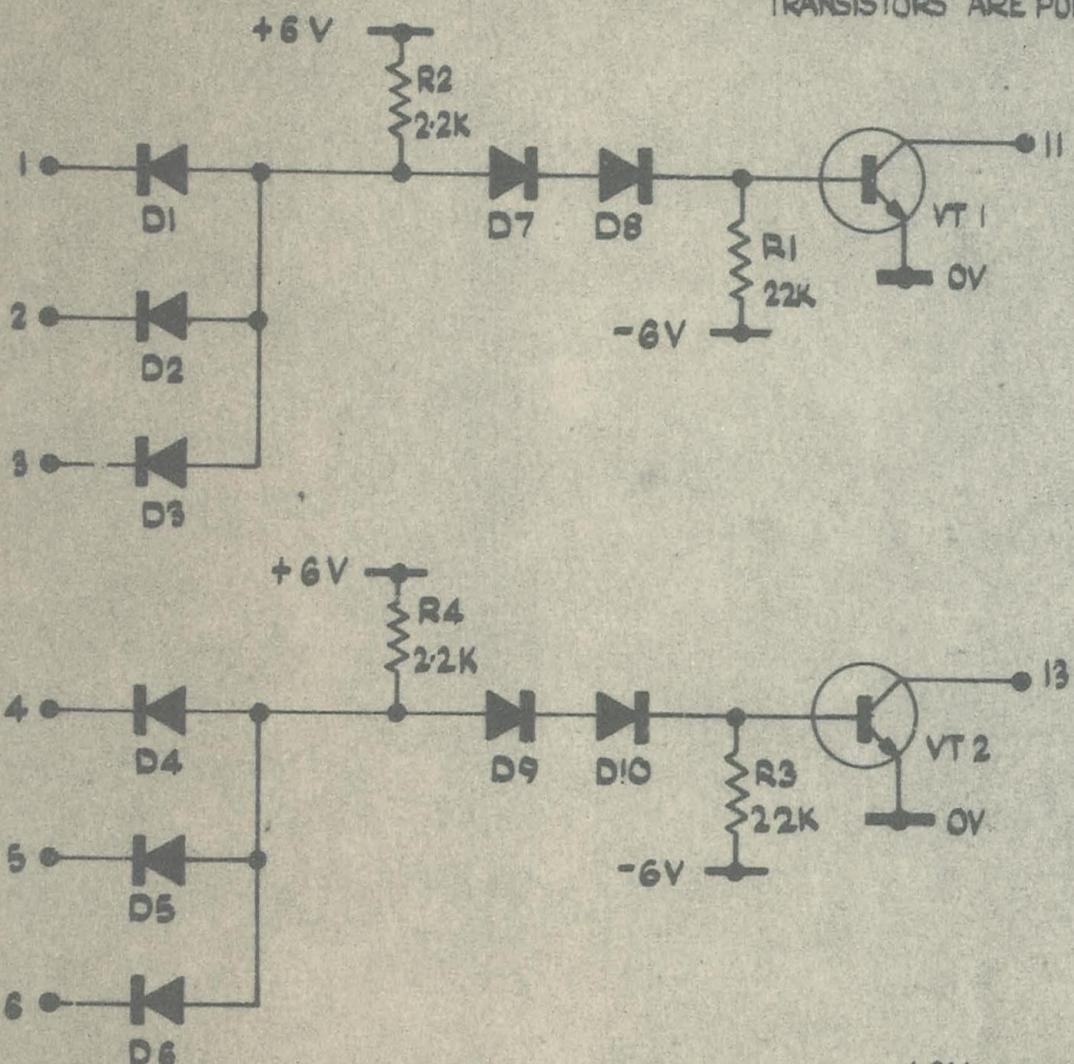
INSTRUCTION SHEET

322A7191

SHEET NO. 7  
OF



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100.



+6V —————— 21  
0V —————— 23  
-6V —————— 22

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPROVED	E.R.M.	DATE	26-4-66
DATE	10/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

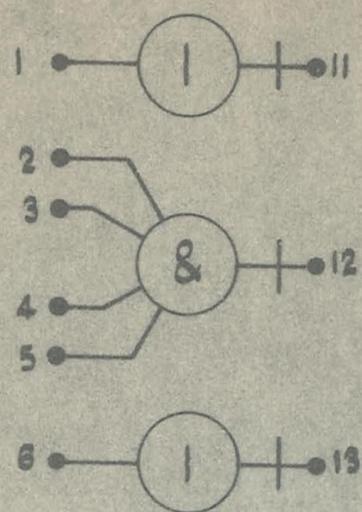
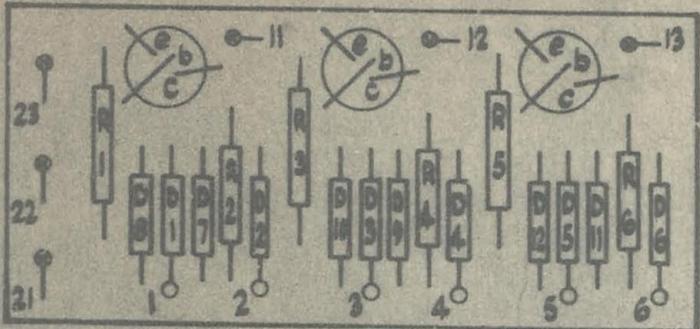
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L.S.A. 02.  
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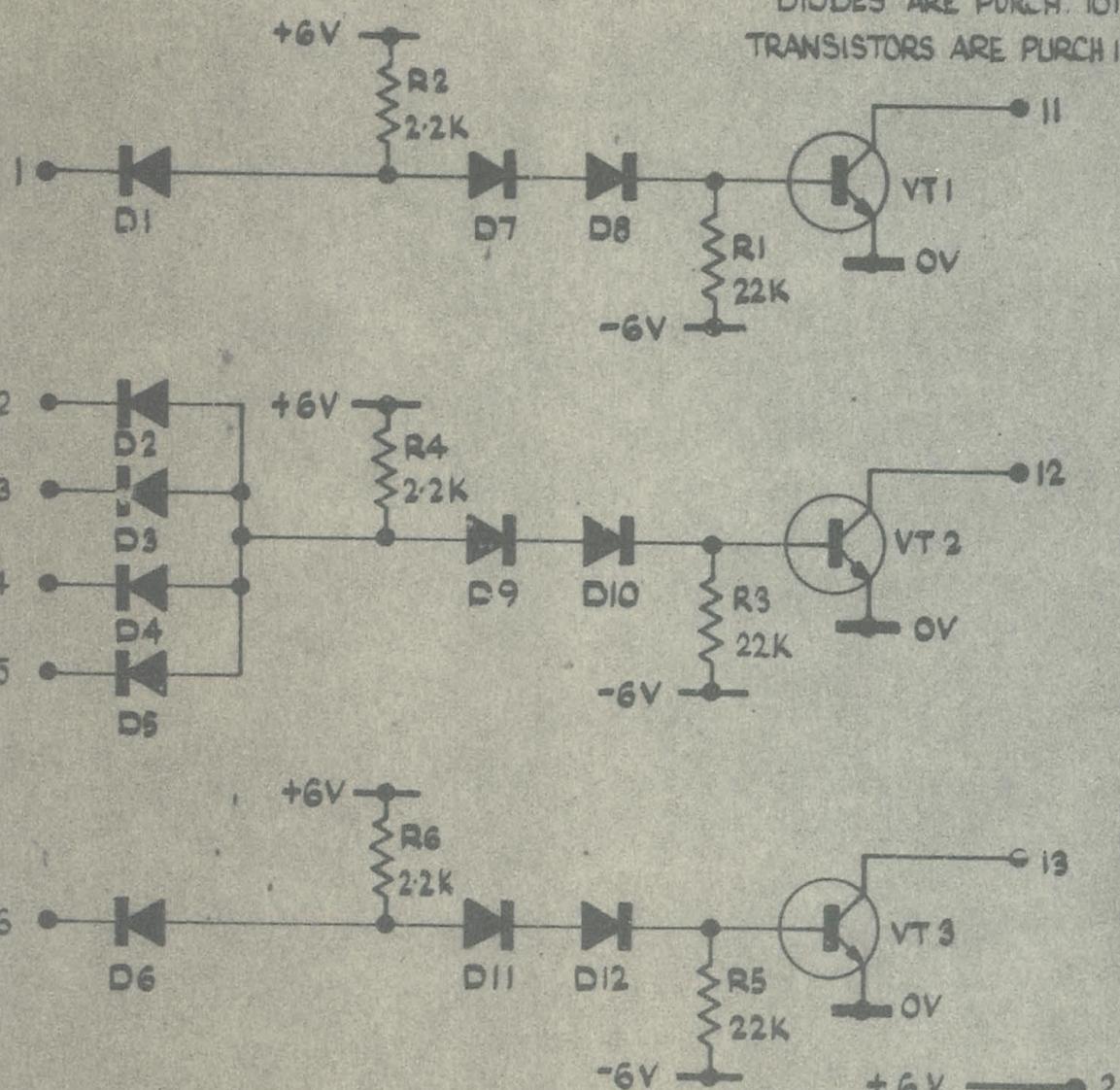
INSTRUCTION SHEET

322A7191

SHEET NO 8  
OF



DIODES ARE PURCH. 101  
TRANSISTORS ARE PURCH. 100



+6V —————— 21  
0V —————— 23  
-6V —————— 22

DRAWN C.A.C. ISSUE No. 1  
CHECKED CS 456 A.R. No. 1374  
APPR'ED G.H.W. DATE 26-4-66  
DATE 6/5/66 INITIALS C.A.C.

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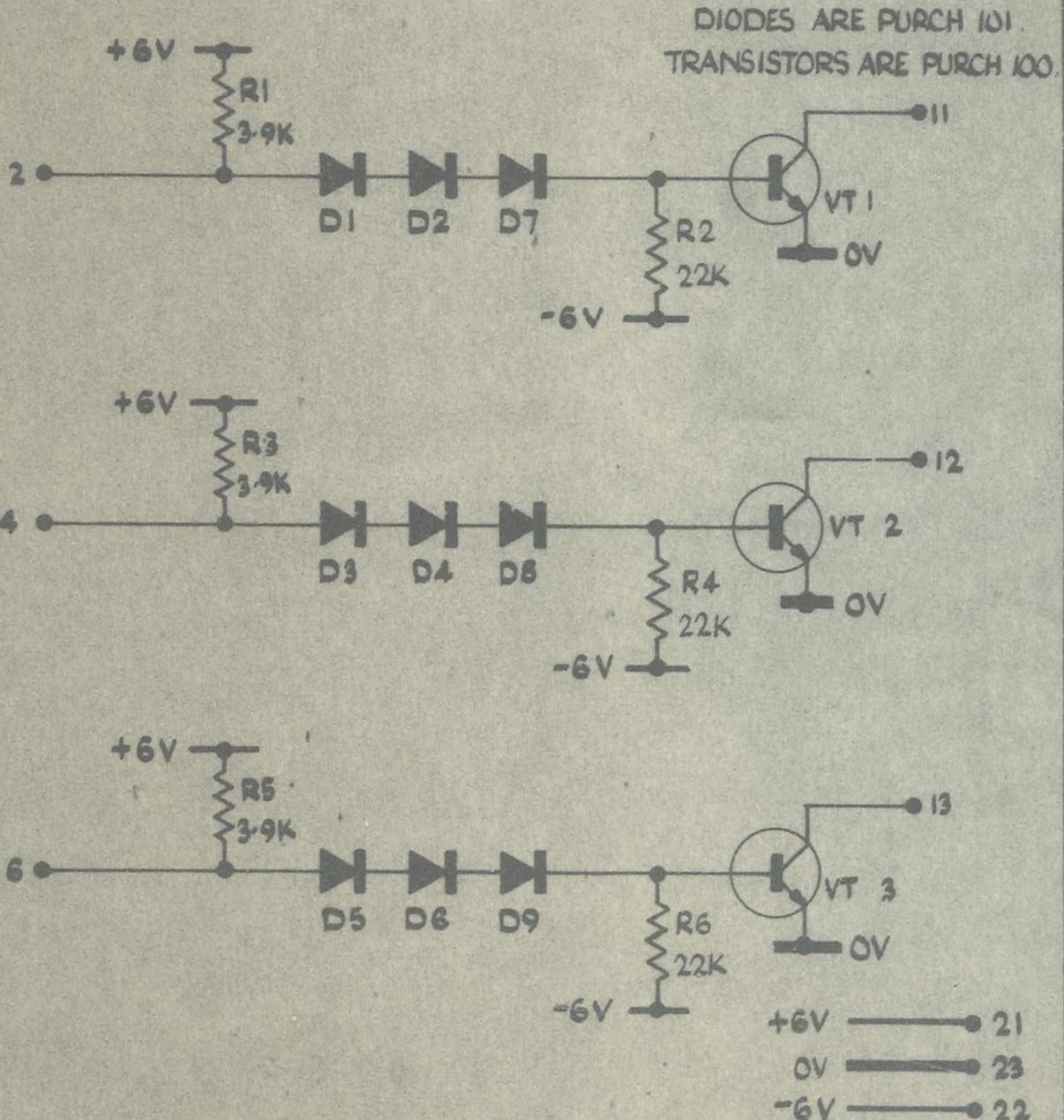
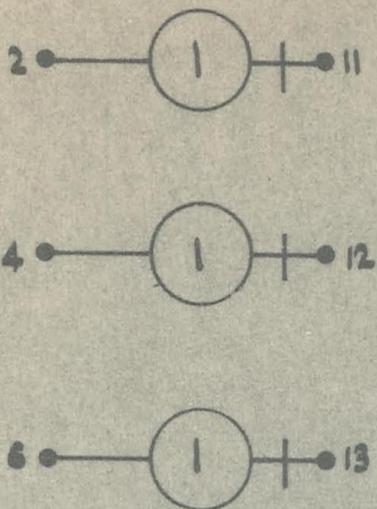
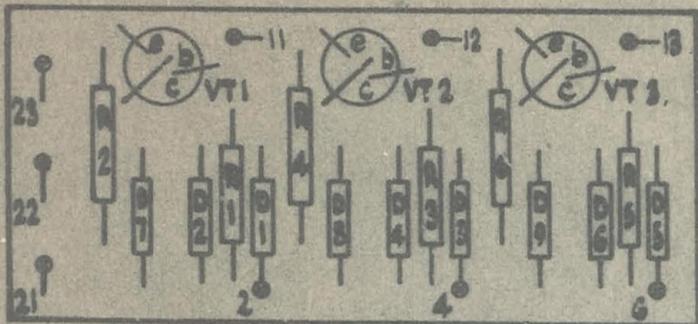
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L.S.A. 03  
4-INPUT NAND GATE + 2 INVERTERS 920B

INSTRUCTION SHEET

322A7191

SHEET NO 9  
OF



DRAWN C.A.C. ISSUE No. 1  
CHECKED CS 456 A.R. No. 1374  
APPROVED E.R. DATE 26-4-66.  
DATE 10/5/66 INITIALS C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

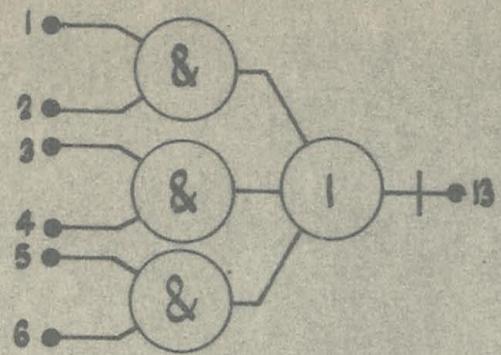
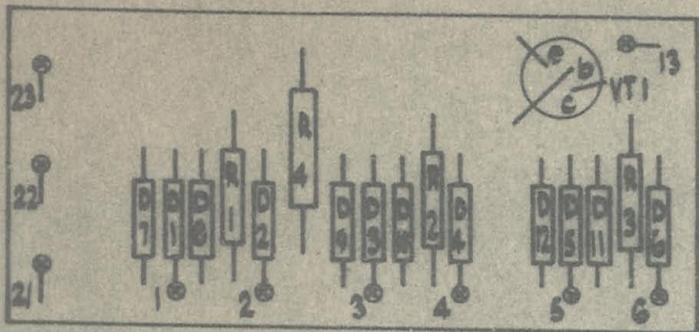
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L.S.A. 04  
CONTROL MATRIX WAVEFORM AMPLIFIERS 920B

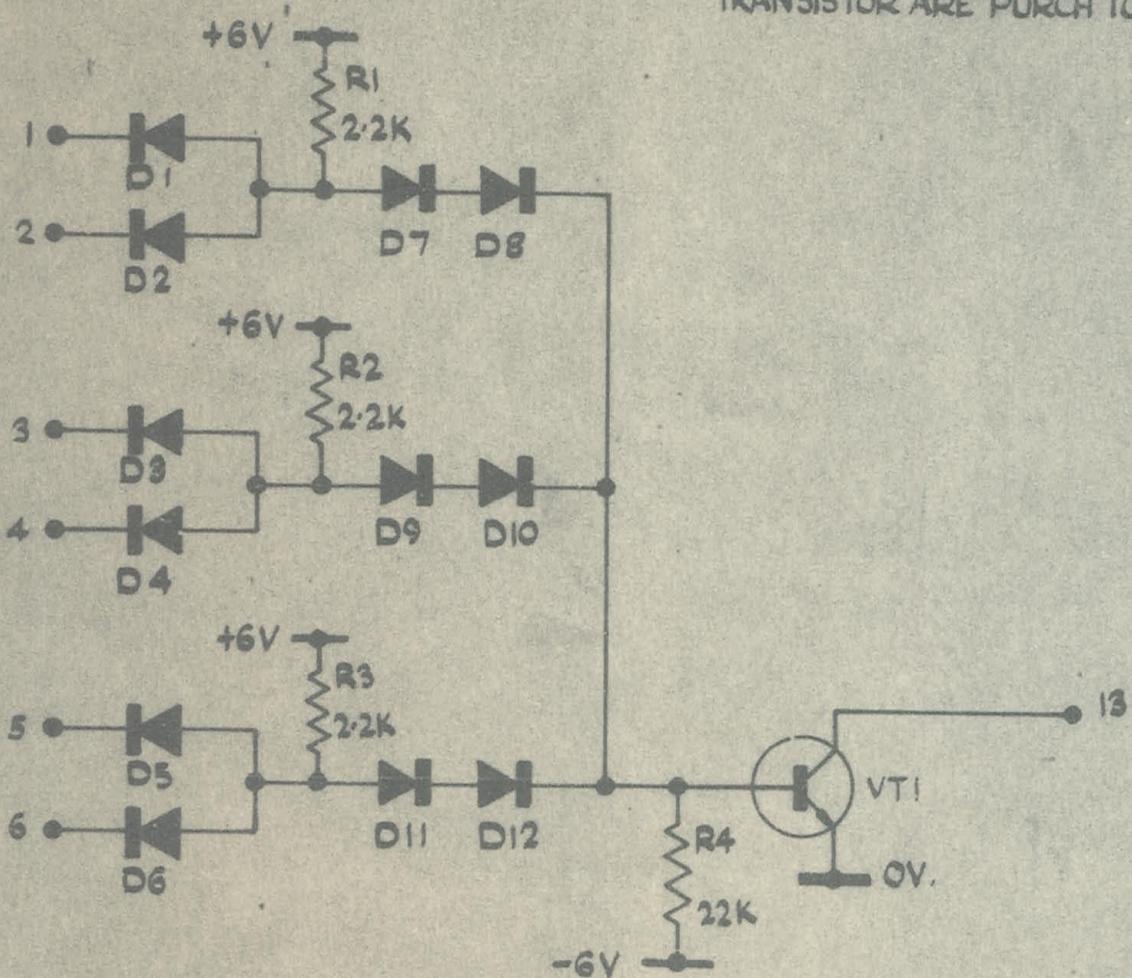
INSTRUCTION SHEET

322 A7191

SHEET NO 10  
OF



DIODES ARE PURCH 101  
TRANSISTOR ARE PURCH 100.



+6V —————— 21  
OV —————— 23  
-6V —————— 22

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No.	1374
APPR VED	E.H.	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

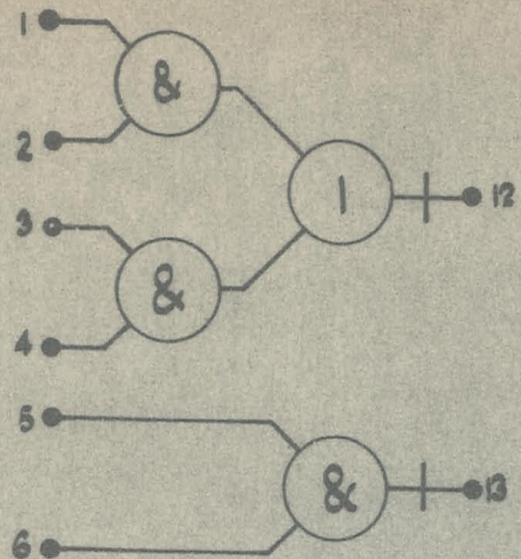
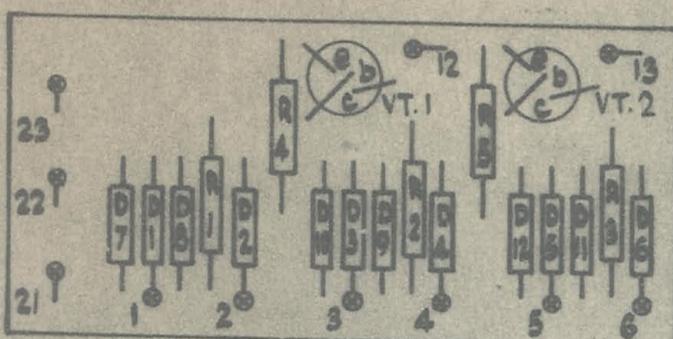
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L.S.A. 05  
920B.

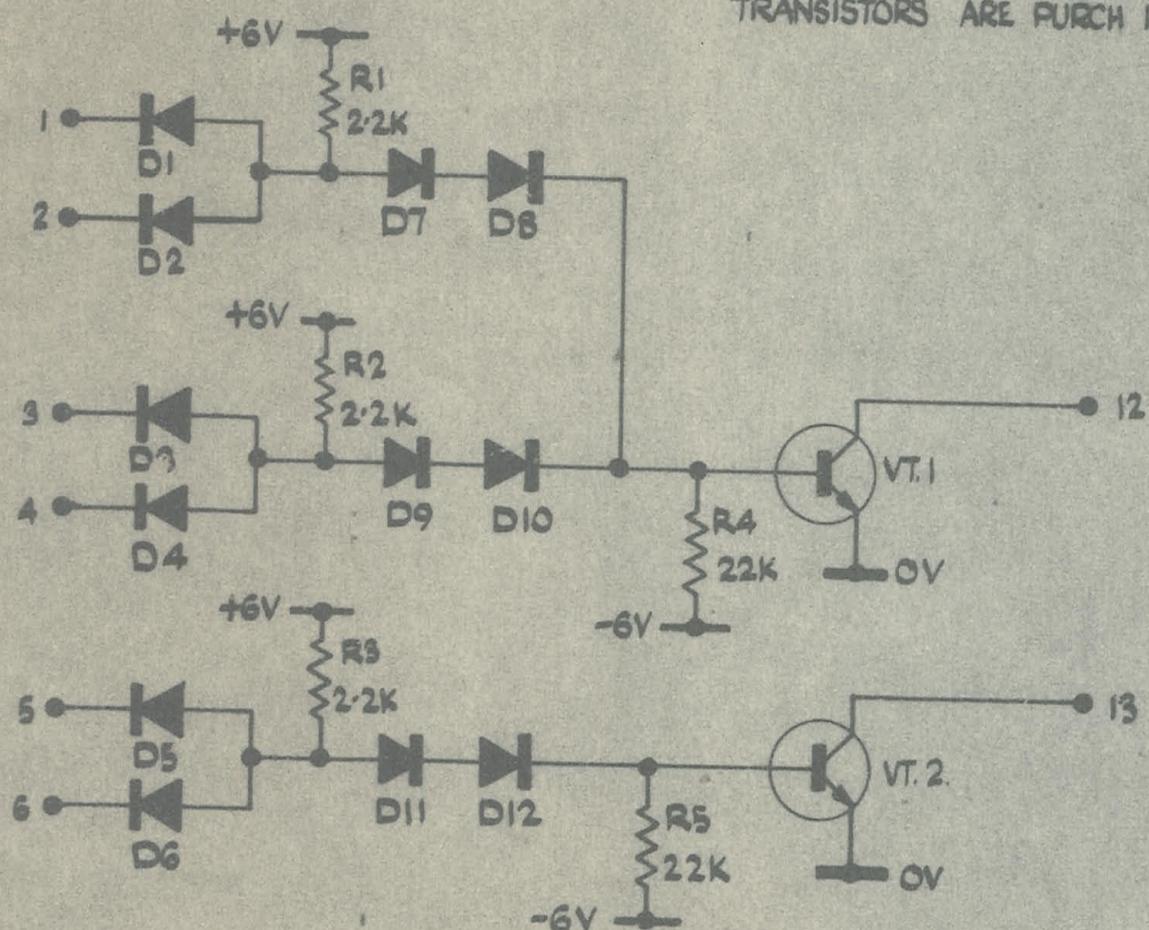
INSTRUCTION SHEET

322A 7191

SHEET NO. 11  
OF



DIODES ARE PURCH 101.  
TRANSISTORS ARE PURCH 100.



+6V —— 21  
0V —— 23  
-6V —— 22

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPR VED	<i>J.M.</i>	DATE	20-4-66
DATE	<i>10/5/66</i>	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

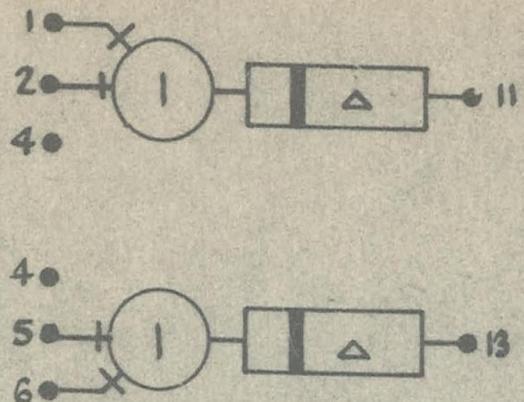
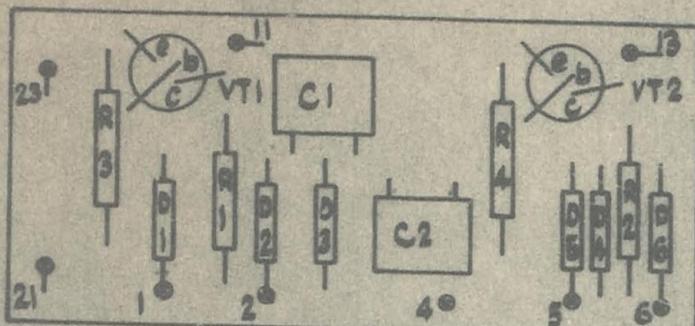
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L.S.A. 06  
920 B

INSTRUCTION SHEET

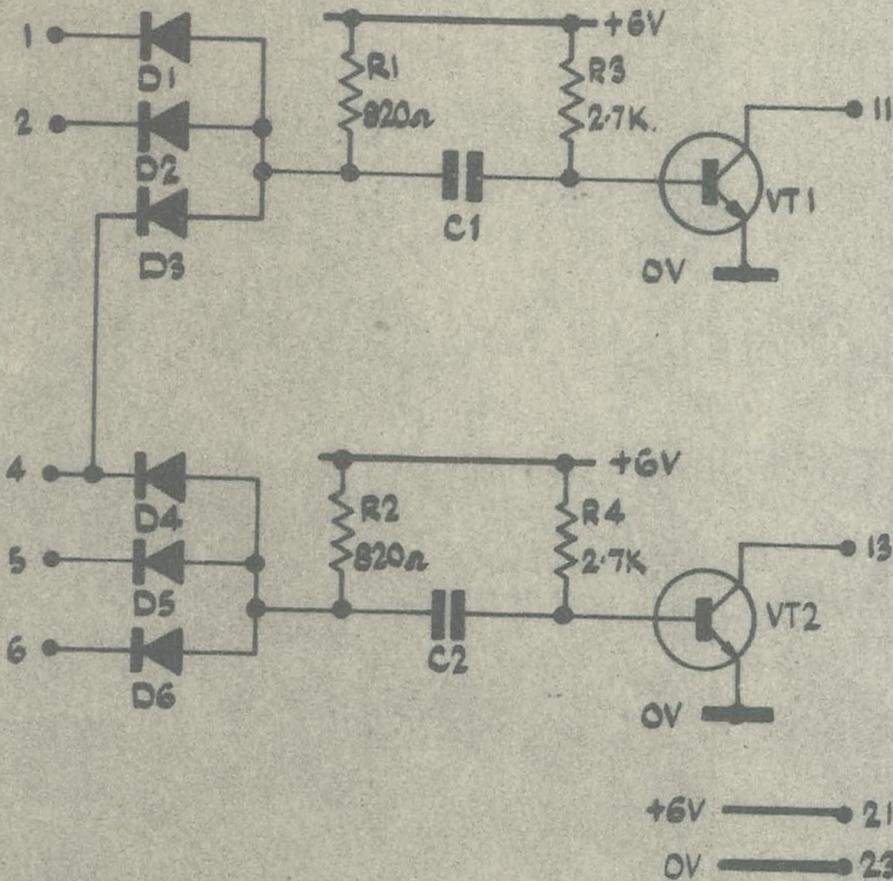
322A7191

SHEET NO. 12  
OF



PULSE WIDTH ( $\Delta$ ) = Cns (WHERE C = CAPACITANCE IN  $\mu$ F.)

DIODES ARE PURCH 101,  
TRANSISTORS ARE PURCH 100



**NOTE:-**

PULSE WIDTH (+VE). PULSE TRIGGERED BY ANY INPUT  
REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR  
GREATER THAN  $\frac{N}{2}$  SEC.

**1/P 4.—2.4 V. REFERENCE VOLTAGE.**

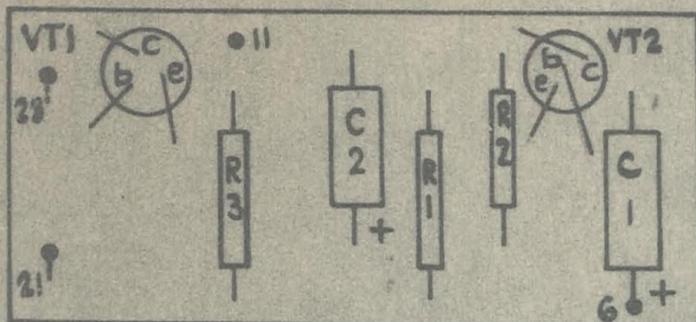
DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1314	1505
APPR VED	Edd H	DATE	26-4-6629-666	
DATE	16/5/66	INITIALS	C.A.C. R.W.C.	

# **ELLIOTT BROTHERS (LONDON) LTD**

L.S.A. 07, 13, 34  
PULSE GENERATORS. 920B

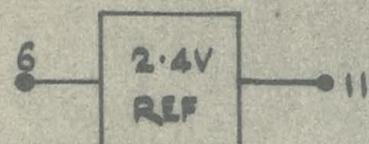
INSTRUCTION SHEET

SHEET NO 13  
OF

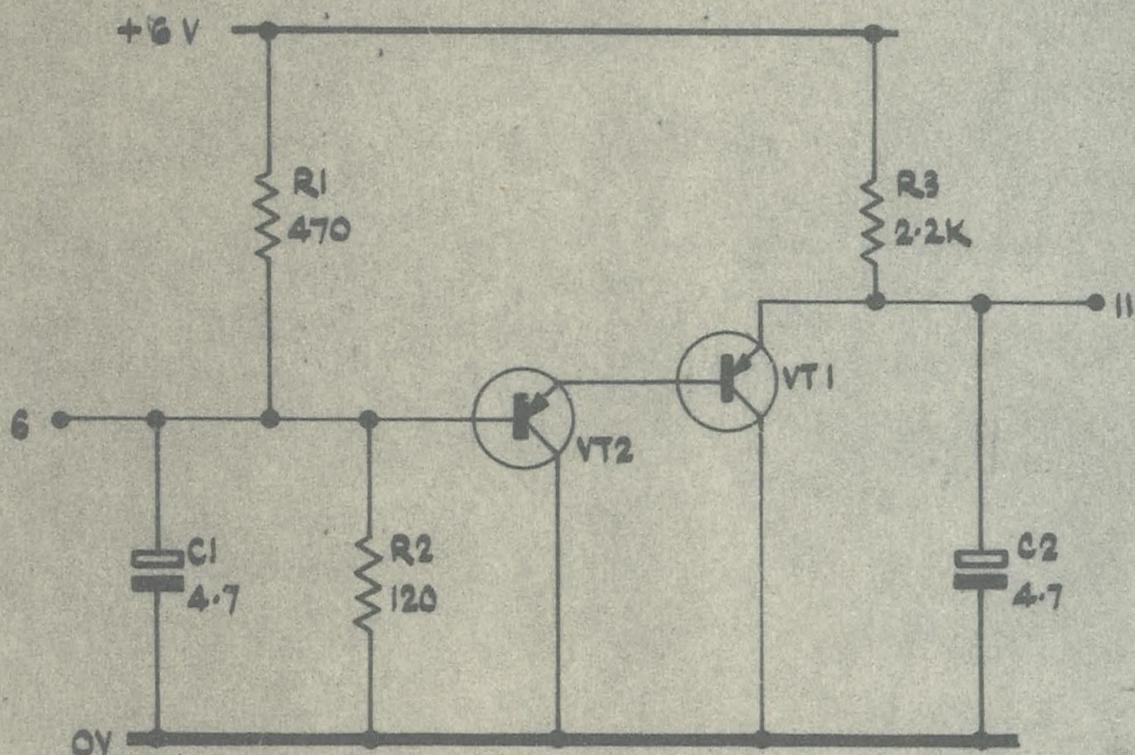


I/P 6 VARIES O/P 11 VOLTAGE  
FOR MARGINAL TEST.

O/P 11 PROVIDES 2.4V REF.



TRANSISTORS ARE MM 2712



+6V —— 21  
OV —— 23

DRAWN C.A.C.  
CHECKED CS 456  
APPR'D BY J.N.V.  
DATE 16/5/66

ISSUE No. 1 2  
A.R. No 1374 1505  
DATE 26-4-66 29-6-66  
INITIALS C.A.C. C.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

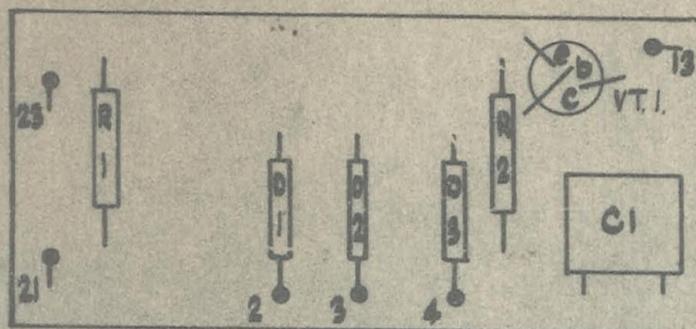
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L.S.A. 08  
VOLTAGE REFERENCE 9208

INSTRUCTION SHEET

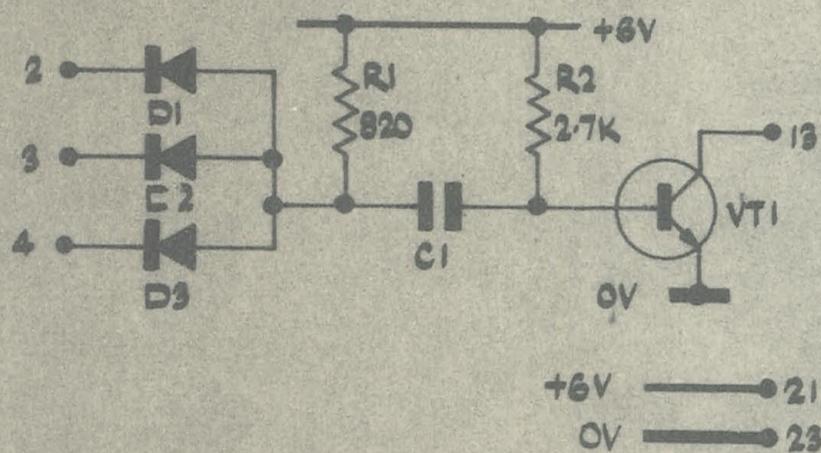
322A7191

SHEET NO 14  
OF



PULSE WIDTH ( $\Delta$ ) =  $C \pi f_s$ . (WHERE  
 $C$  = CAPACITANCE IN  $\mu F$ .)

DIODES ARE PURCH 101.  
TRANSISTORS ARE PURCH 100.



**NOTE:-**

PULSE WIDTH (+VE), PULSE TRIGGERED BY ANY INPUT  
REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1'  
FOR  $\geq \frac{N}{3}$  SEC.

I/P 4 - 2.4V REFERENCE VOLTAGE.

DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No	1374	1505
APPROVED	E.P.W.	DATE	26-4-66	29-6-66
DATE	16-5-66	INITIALS	C.A.C.	R.W.C.

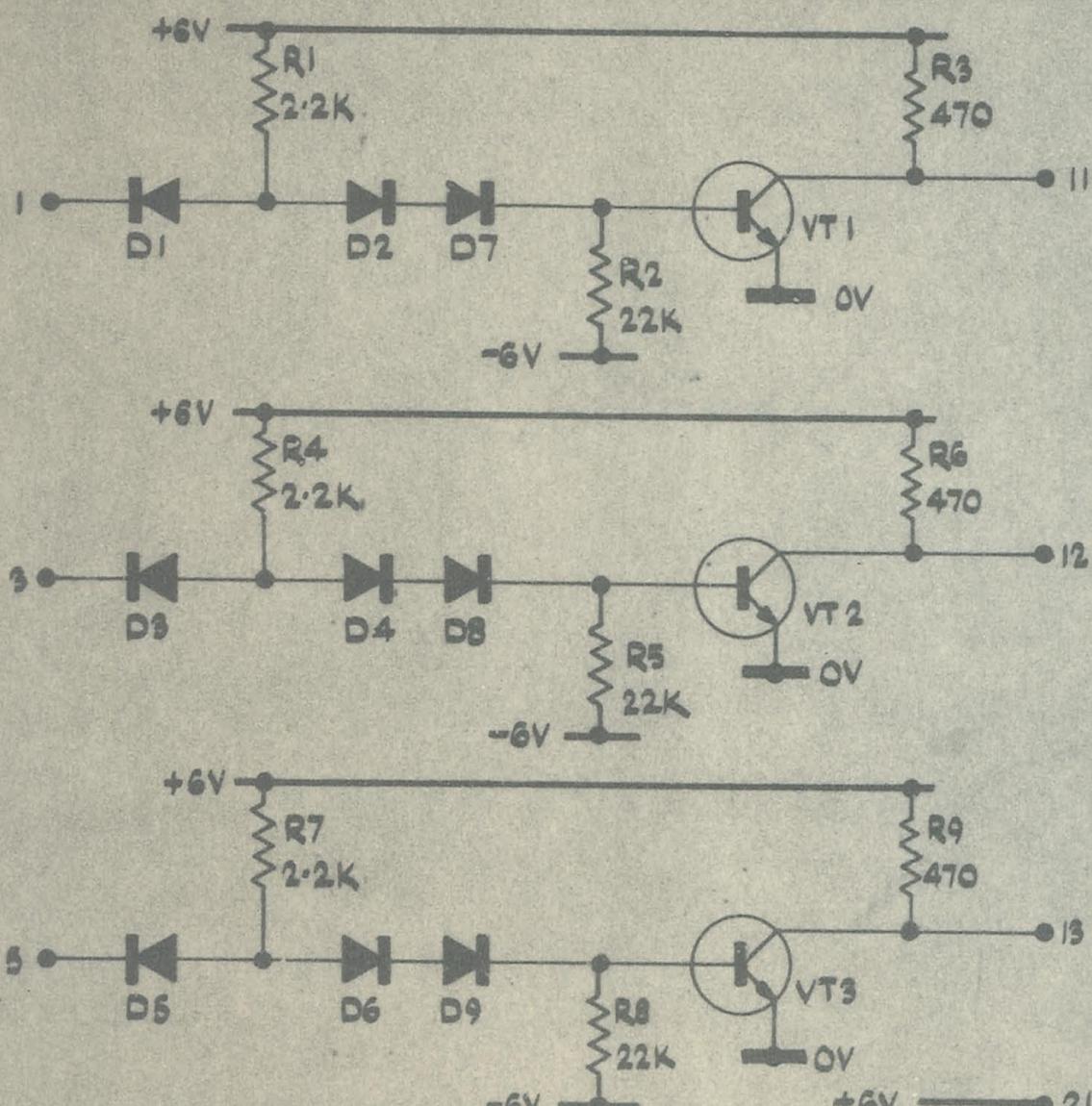
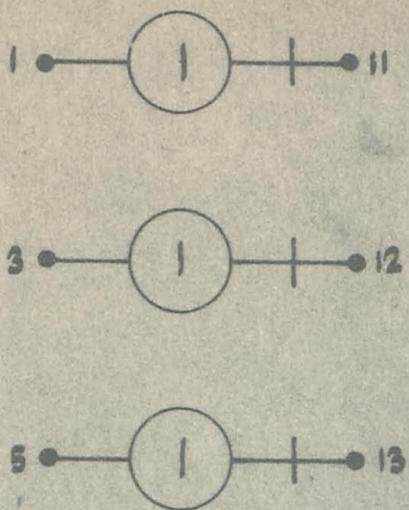
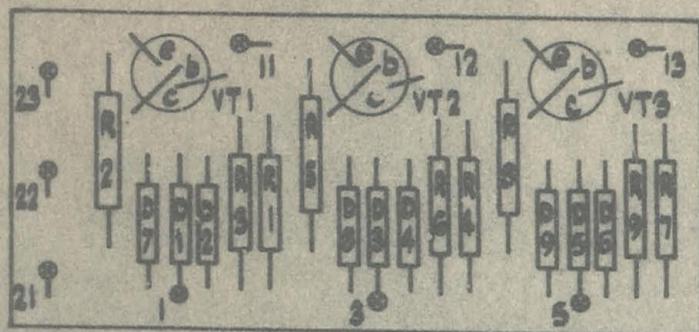
**ELLIOTT BROTHERS (LONDON) LTD.**

L.S.A. 09, 14,  
PULSE GENERATOR 920B

**INSTRUCTION SHEET**

322A 7191

SHEET NO 15  
OF



DIODES ARE PURCH 101.

TRANSISTORS ARE PURCH 100.

DRAWN	C.A.C.	ISSUE NO.	1
CHECKED	CS 456	A.R. No.	1374
APPR' VED	E.R.L.	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

+6V —————— 21  
0V —————— 23  
-6V —————— 22

ELLIOTT BROTHERS (LONDON) LTD.

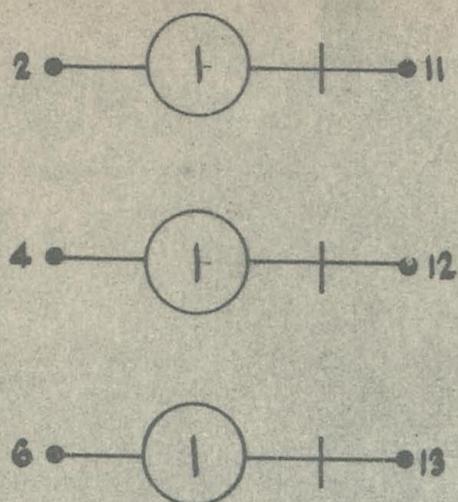
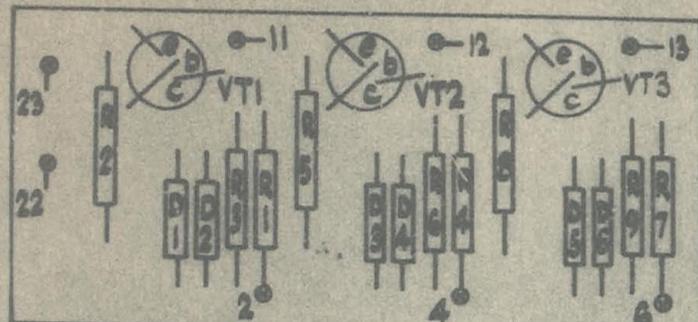
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L.S.A. II  
CABLE TRANSMITTERS '9208

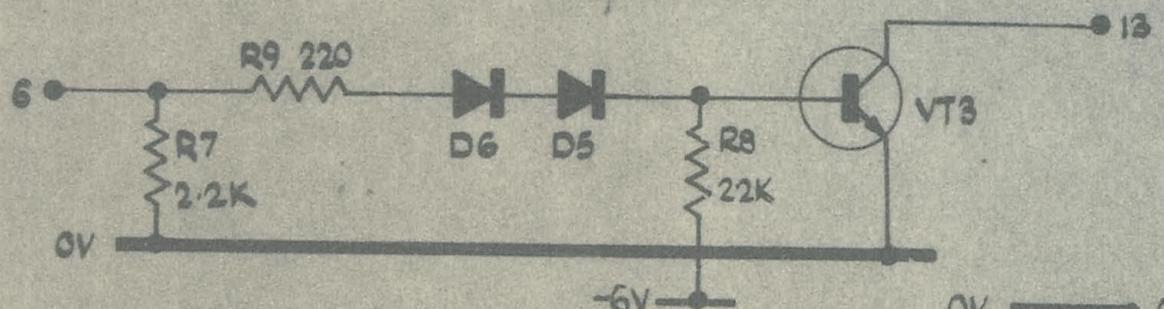
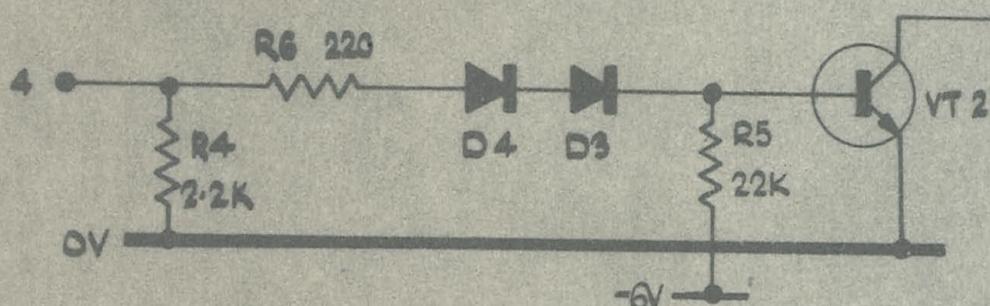
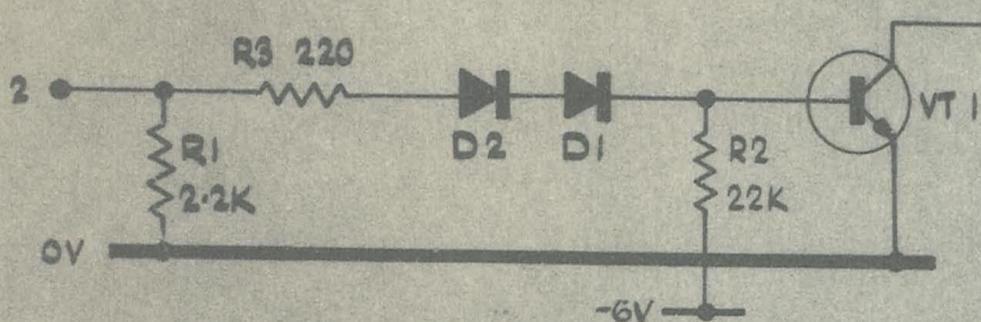
INSTRUCTION SHEET

322A7191

SHEET NO 16  
OF



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100



OV —————— 23  
-6V —————— 22

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 453	A.R. No	1374
APPR VED	E.D.W.	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

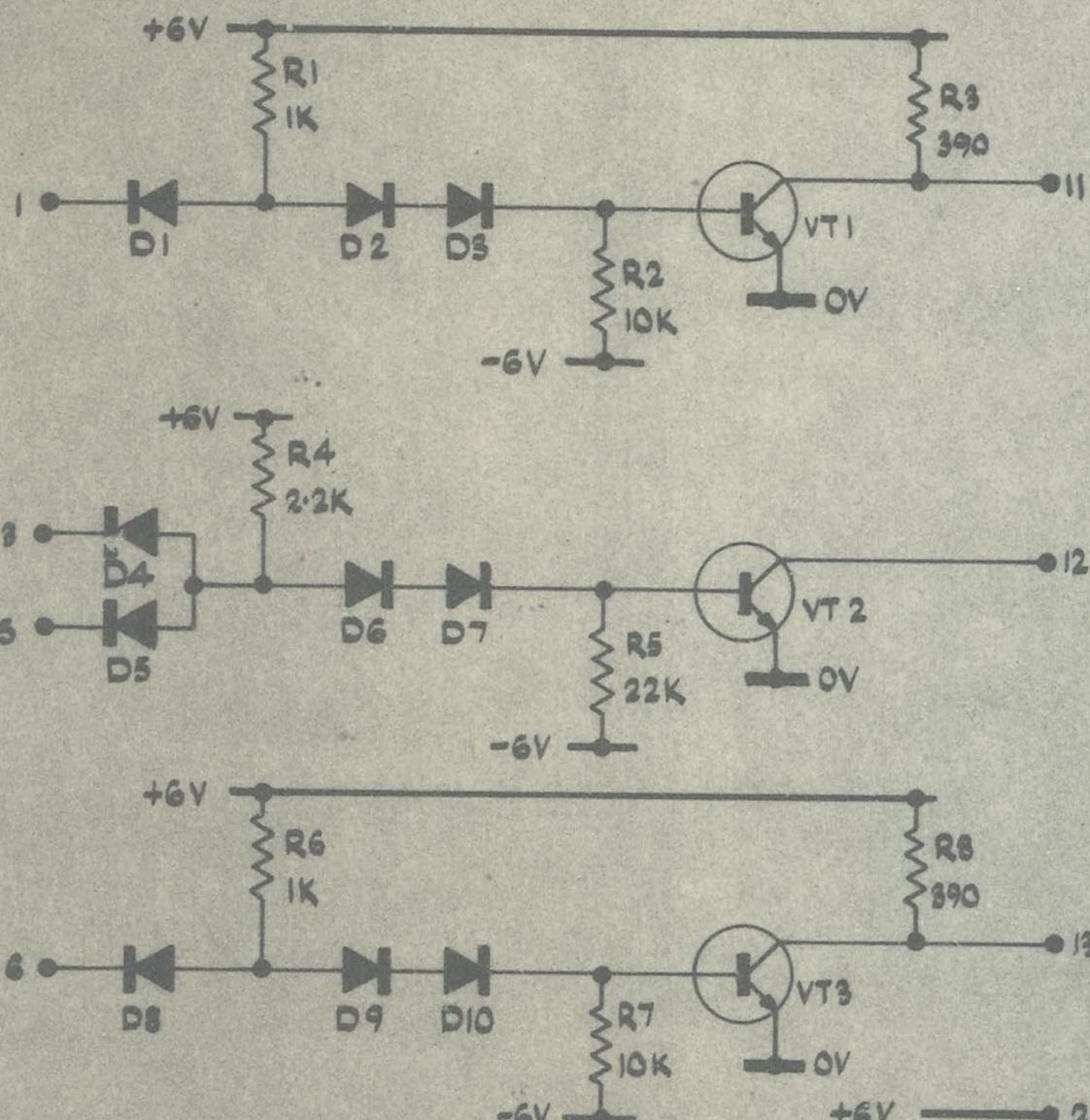
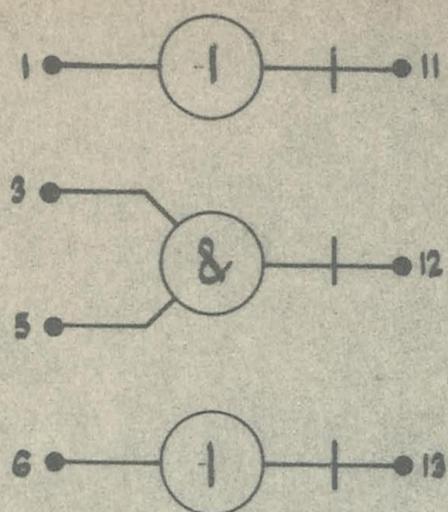
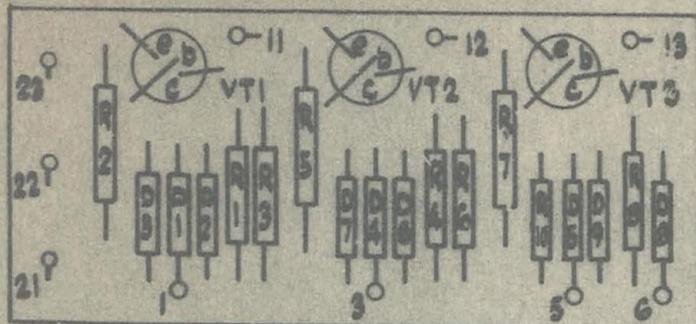
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L.S.A. 12/  
CABLE RECEIVERS 920B

INSTRUCTION SHEET

322A 7191

SHEET NO 17  
OF



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100

DRAWN	C.A.C.	ISSUE NO.	1
CHECKED	CS 456	A.R. No	1314
APPR VED	S.E.M.	DATE	26-4-66
DATE	16/7/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

L.S.A. 15

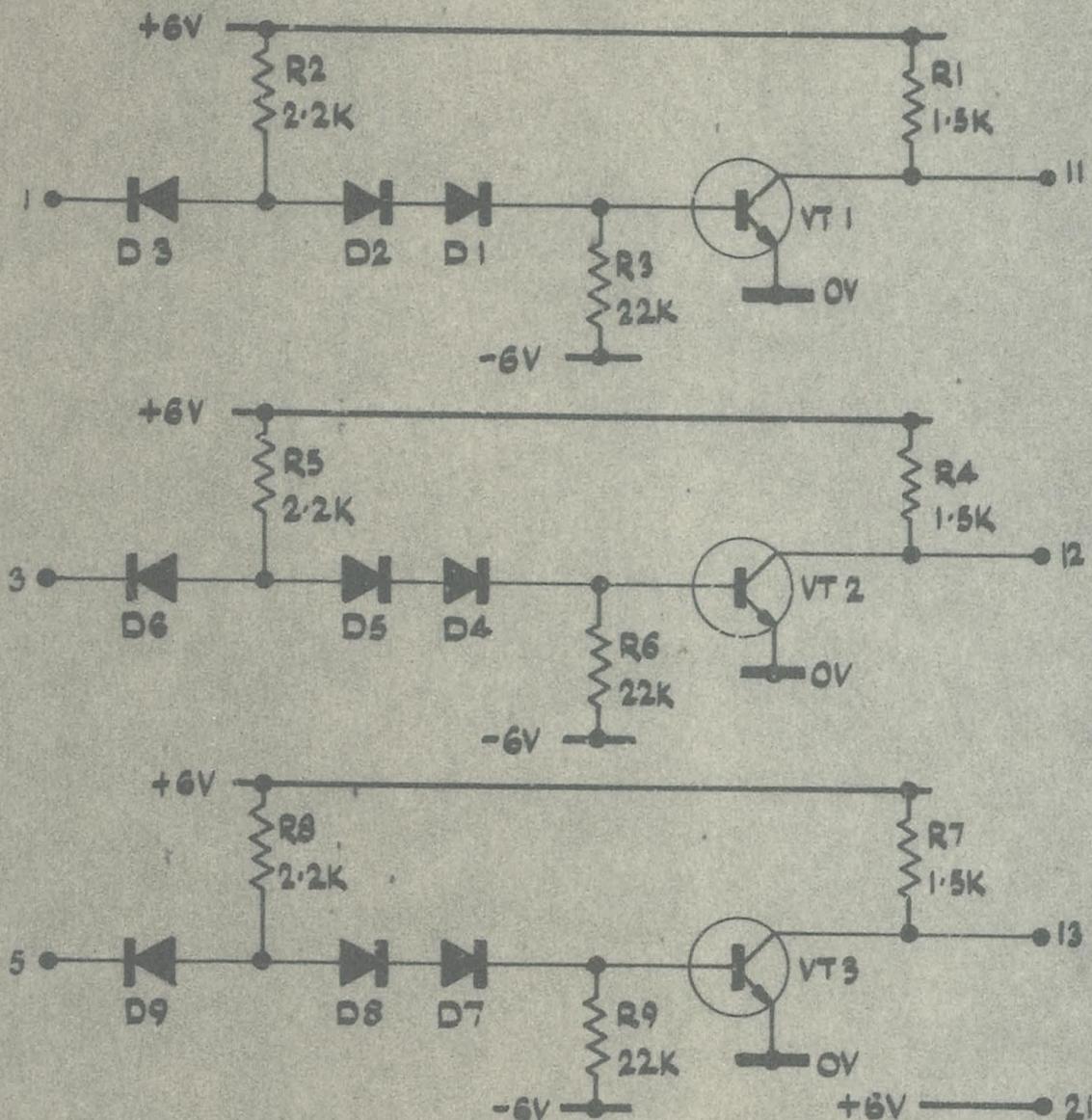
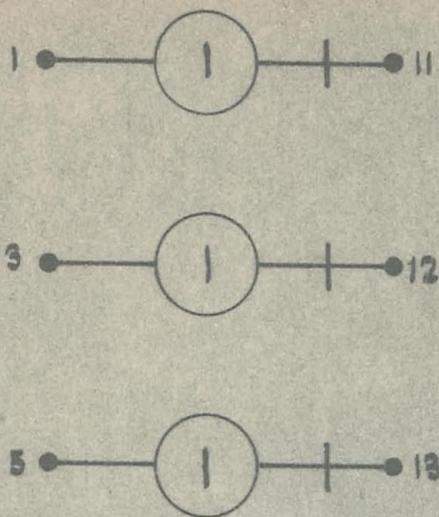
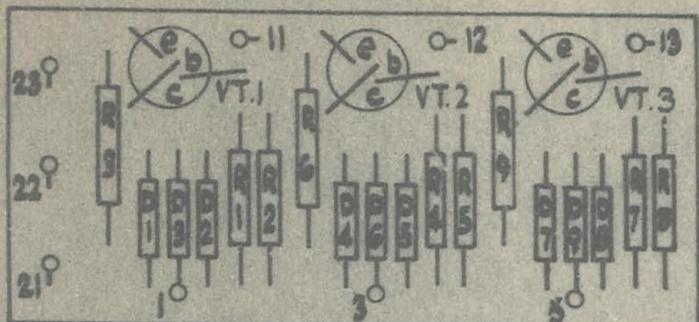
920B

INSTRUCTION SHEET

2-INPUT NAND GATE + 2 INVERTING DRIVERS

322A7191

SHEET NO 18  
OF



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100.

DRAWN C.A.C. ISSUE NO. 1  
CHECKED CS 466 A.R. No. 1374  
APPR'VED E.P. DATE 26-4-66  
DATE 16/5/66 INITIALS C.A.C.

+6V —————— 21  
0V —————— 23  
-6V —————— 22

ELLIOTT BROTHERS (LONDON) LTD.

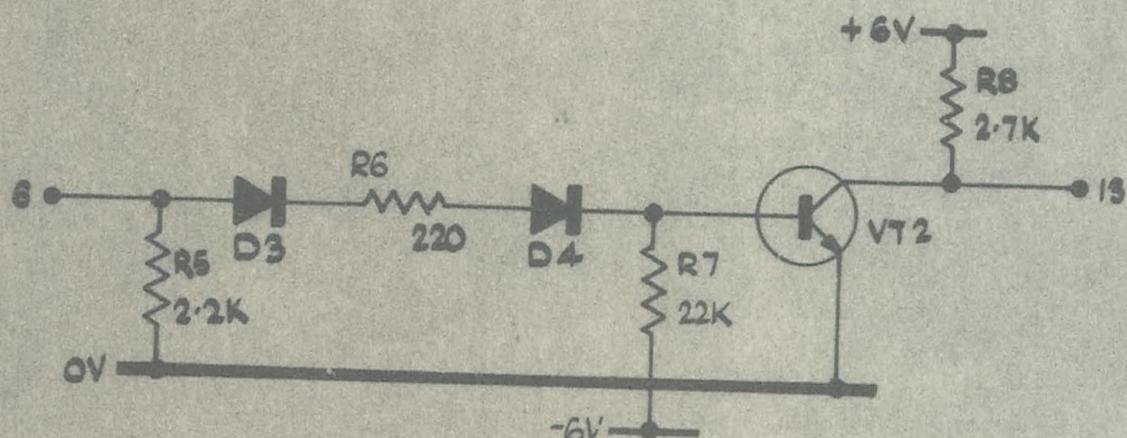
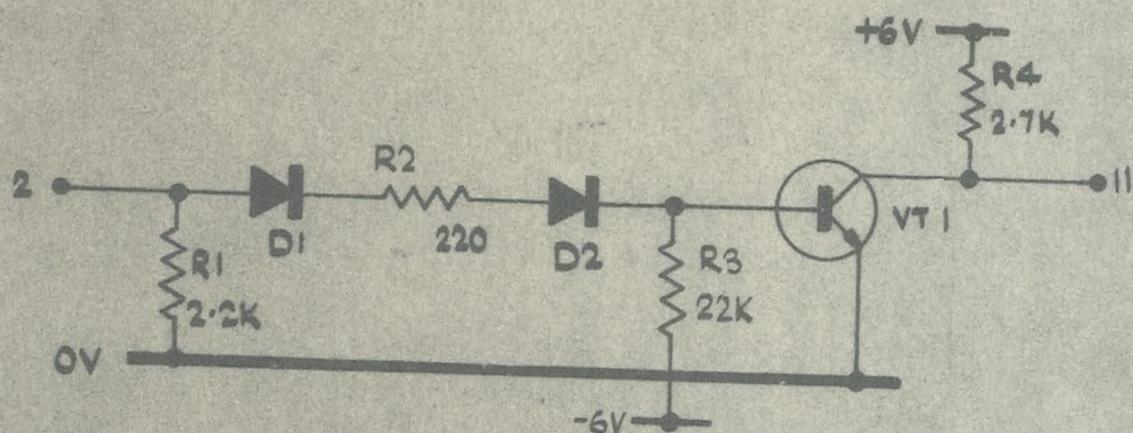
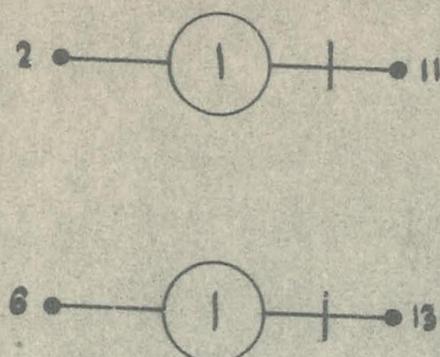
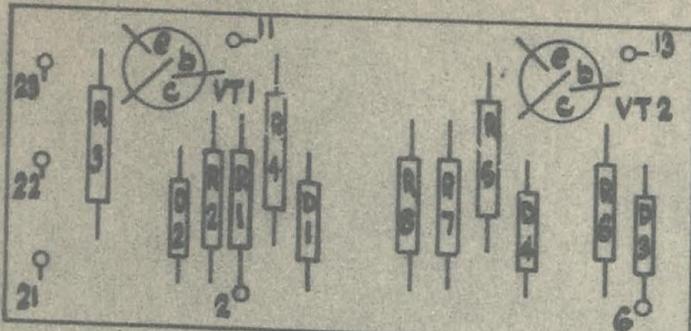
TITLE

L.S.A.16.  
F-MINilog DRIVERS 9206

INSTRUCTION SHEET

322A7191

SHEET NO 19  
OF



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100.

DRAVN C.A.C. ISSUE No. 1 2  
CHECKED CS 456 A.R. No. 1374 1505  
APPR VED E.D.W. DATE 26-4-66 29-6-66  
DATE 16/1/70 INITIALS C.A.C. R.W.C.

+6V —— 21  
OV —— 23  
-6V —— 22

ELLIOTT BROTHERS (LONDON) LTD.

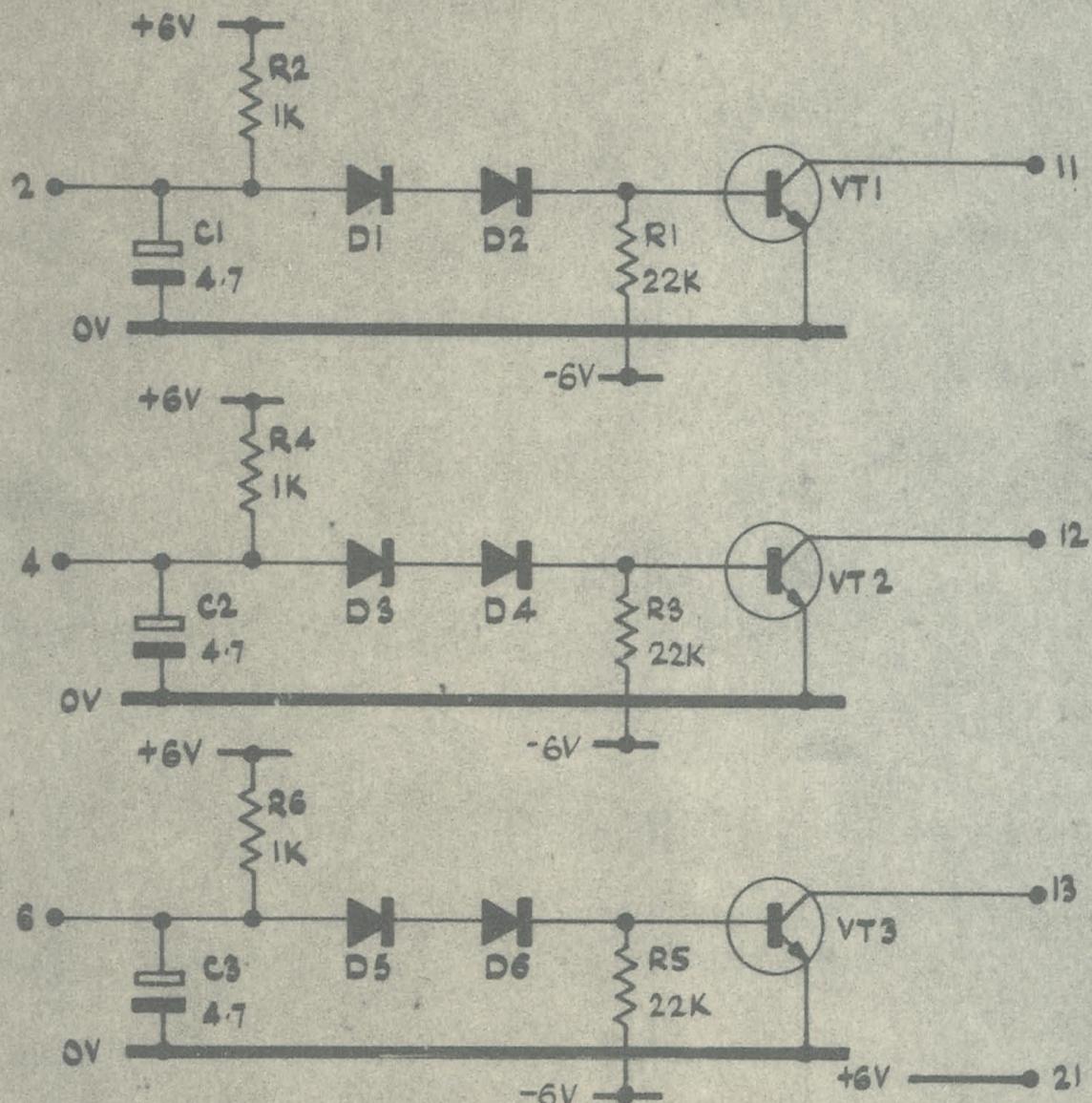
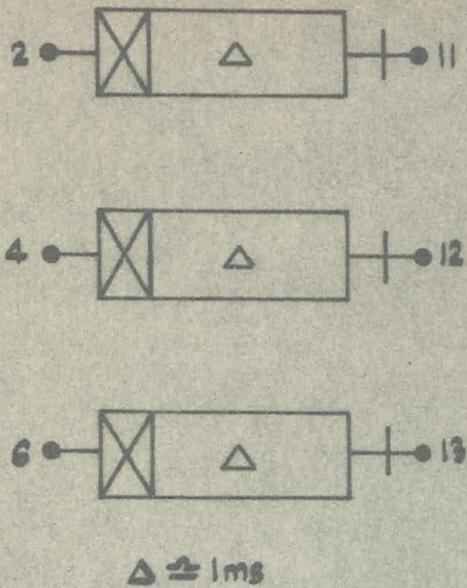
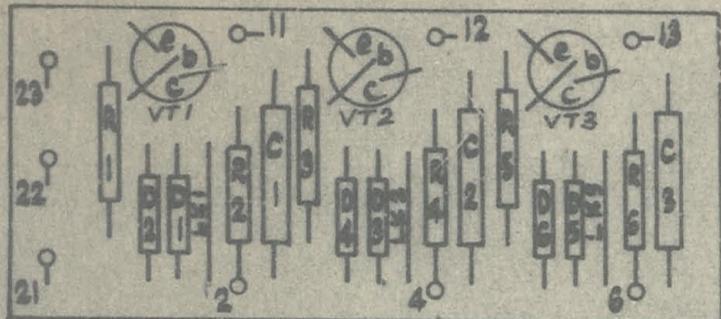
TITLE

L.S.A. 17.  
PAPER TAPE RECEIVER 9208.

INSTRUCTION SHEET

322A 7191

SHEET NO 20  
OF



DIODES ARE PURCH 101

TRANSISTORS ARE PURCH 100

DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No.	1374	1505
APPR VED	G.R.W.	DATE	26-4-66	29-6-66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.

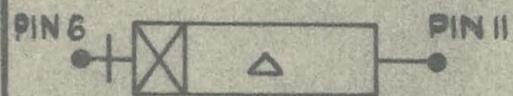
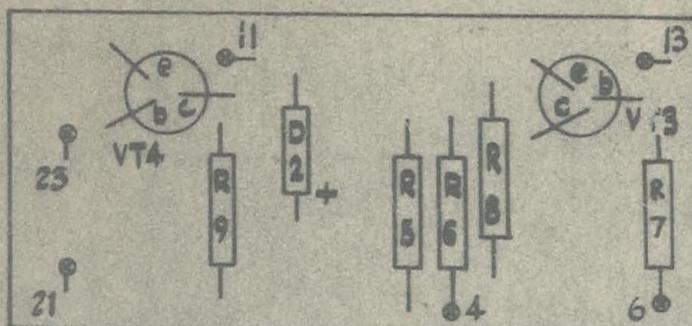
ELLIOTT BROTHERS (LONDON) LTD.

TITLE  
L.S.A. 18.  
SINGLE I/P NOISE REJECTION INVERTER. 9208

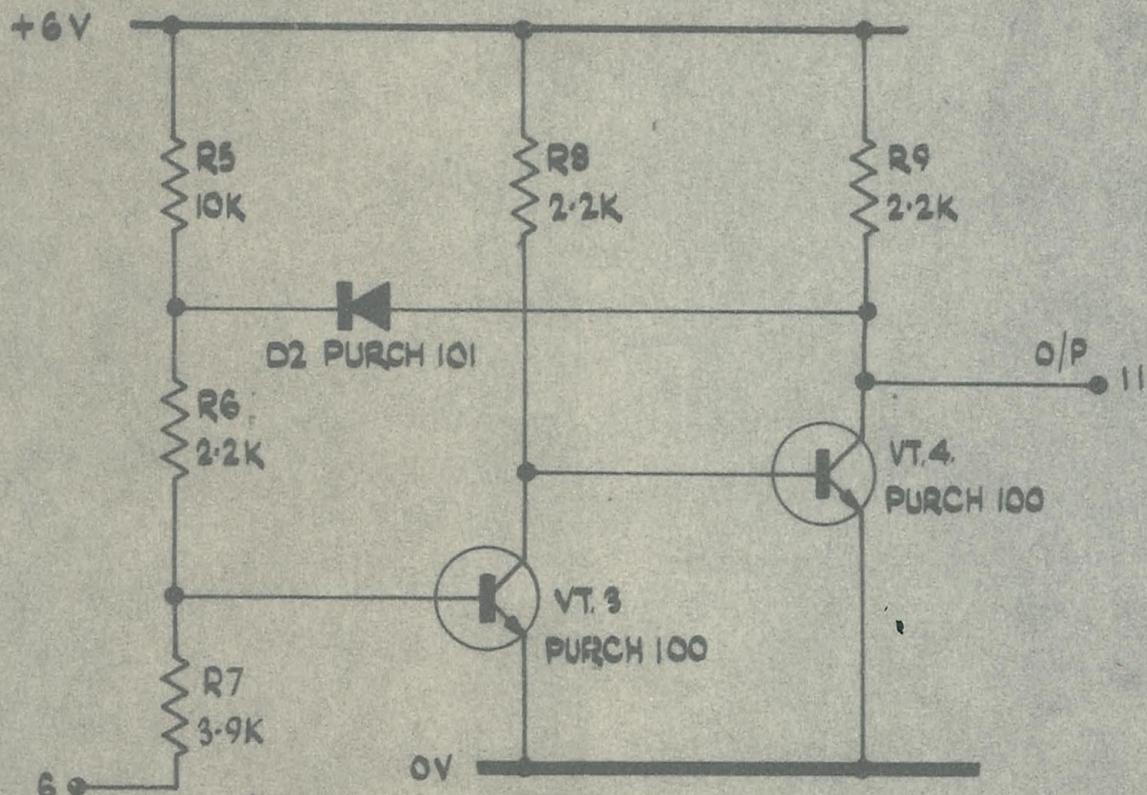
INSTRUCTION SHEET

322A7191

SHEET NO 21  
OF



ONLY USED FOLLOWING LSA. 20  
OR 21. COMBINATION CIRCUIT  
GIVES DELAY ( $\Delta$ )  $\approx 10\text{ms}/\mu\text{F}$   
WHERE  $\mu\text{F}$  IS CAPACITANCE OF  
LSA 20 OR LSA 21.



DIODE IS PURCH 101  
TRANSISTORS ARE PURCH 100

+6V —————— 21  
0V —————— 23

DRAWN	C.A.C.	ISSUE NO.	1	2
CHECKED	CS 456	A.R. No	1374	1505
APPR VFD	DRR	DATE	26-1-66 87-66	
DATE	16/5/66	INITIALS	C.A.C. R.W.C.	

ELLIOTT BROTHERS (LONDON) LTD.

TITLE

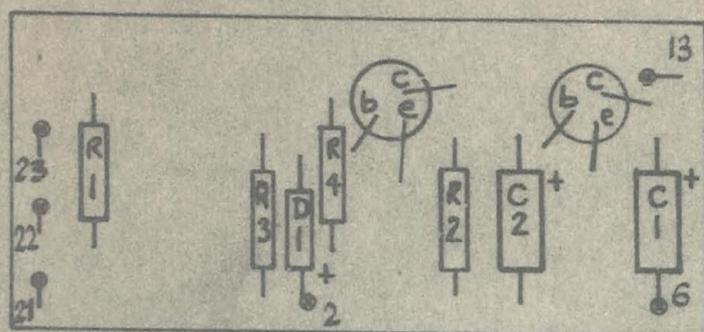
L.S.A. 19

DELAY 920B

INSTRUCTION SHEET

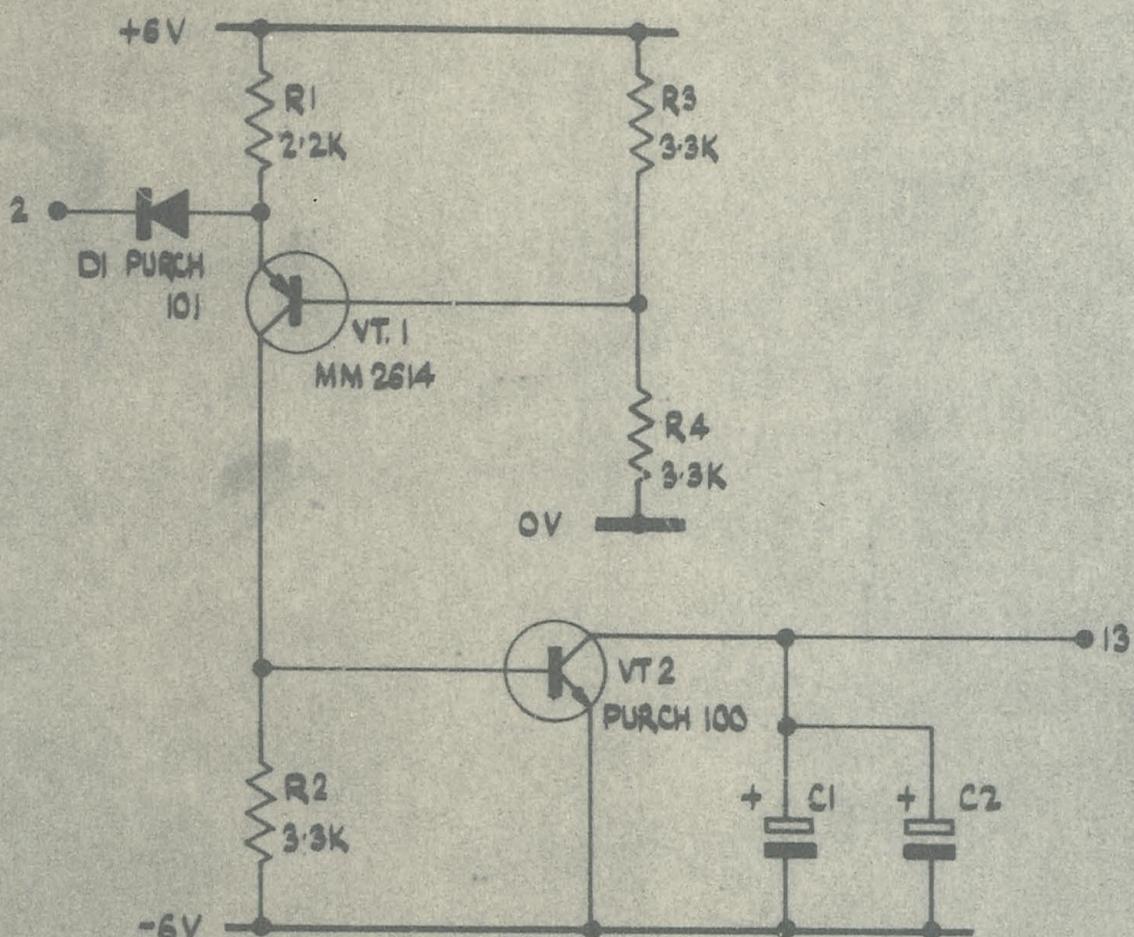
322A7191

SHEET NO 22  
OF



ONLY USED PRECEDING L.S.A.  
19. OVERALL DELAY  $\leq 10 \text{ ms}/\mu\text{F}$   
WHERE  $\mu\text{F}$  IS CAPACITANCE OF  
 $C_1 + C_2$

2 —————— 13



ELEMENT	C1	C2
LSA 20	4.7μF	4.7μF
LSA 24	2.2μF	1.0μF
LSA 25	2.2μF	0.47μF

+6V —————— 21  
0V —————— 23  
-6V —————— 22

DRAWN	C.A.C.	ISSUE No.	1	2
CHECKED	CS 456	A.R. No	1374	1505
APPR. VED	S.R.M.	DATE	26-1-66 20-6-66	
DATE	6/5/66	INITIALS	C.A.C. R.W.C.	

ELLIOTT BROTHERS (LONDON) LTD.

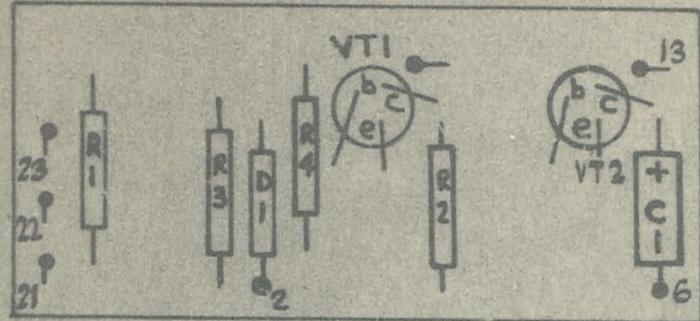
TITLE:

L.S.A. 20, 24, 25,  
DELAY.

INSTRUCTION SHEET

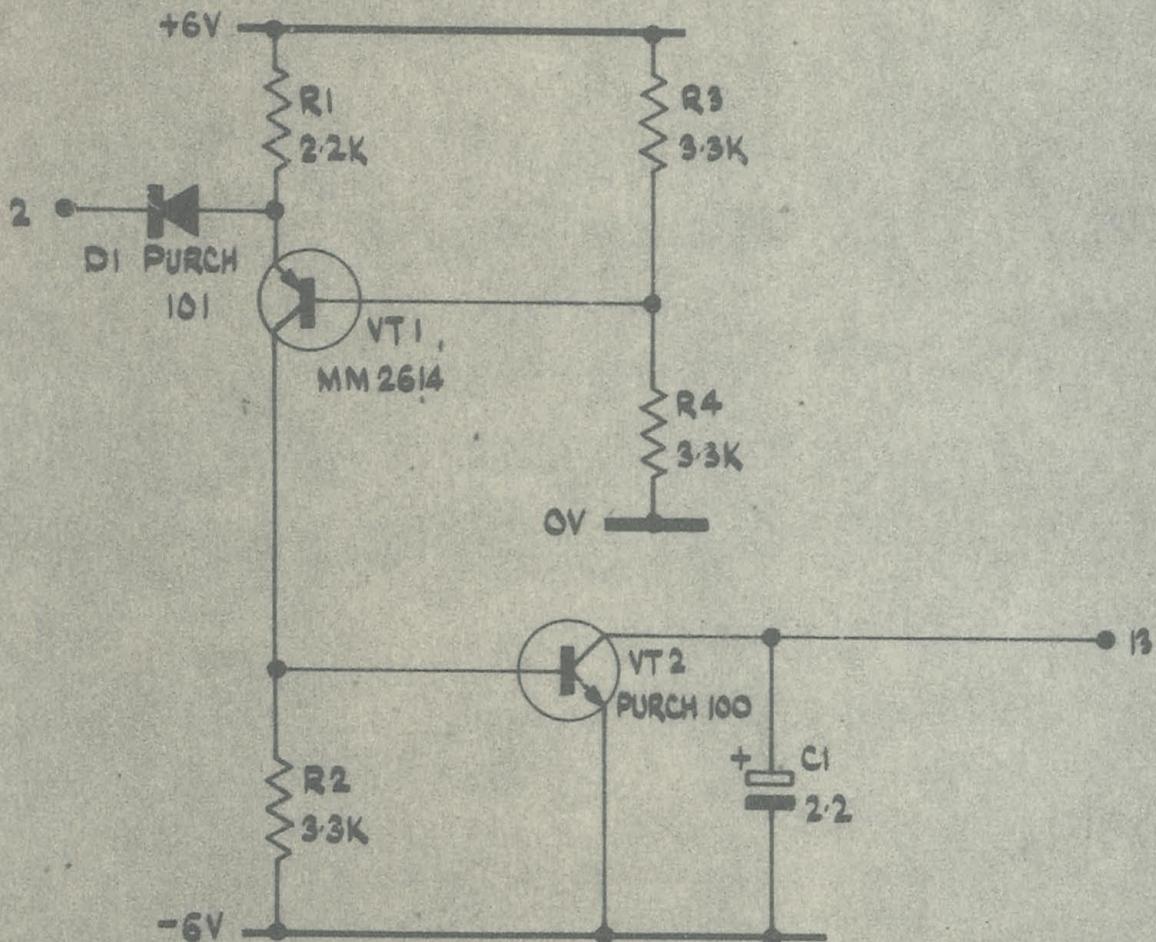
322A 7191

SHEET NO. 23  
OF



ONLY USED PRECEDING L.S.A  
19. OVERALL DELAY  $\approx 10 \text{ m.s}/\mu\text{F}$   
WHERE  $\mu\text{F}$  IS CAPACITANCE OF  
 $C_1$

2 → 13



+6V → 21  
OV → 23  
-6V → 22

DRAWN	C.A.C.	ISSUE NO.	1	2
CHECKED	CS 456	A.R. No	1374	1505
APPROVED	E.R.W.	DATE	26-4-66	29-6-66
DATE	16/5/66	INITIALS	C.A.C.	R.W.C.

ELLIOTT BROTHERS (LONDON) LTD.

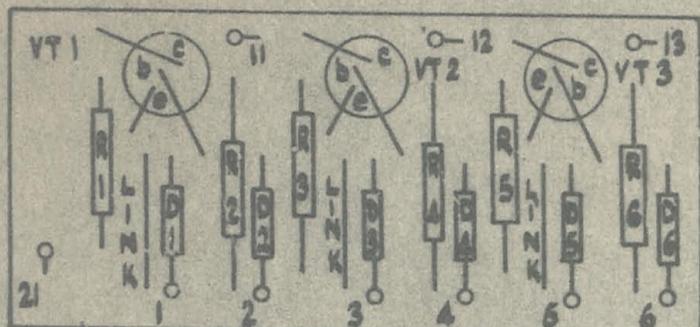
TITLE

L.S.A. 21.  
DELAY.

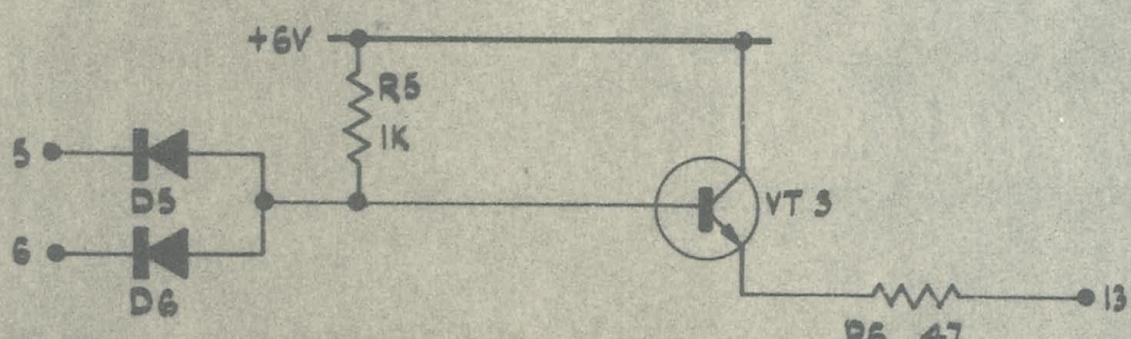
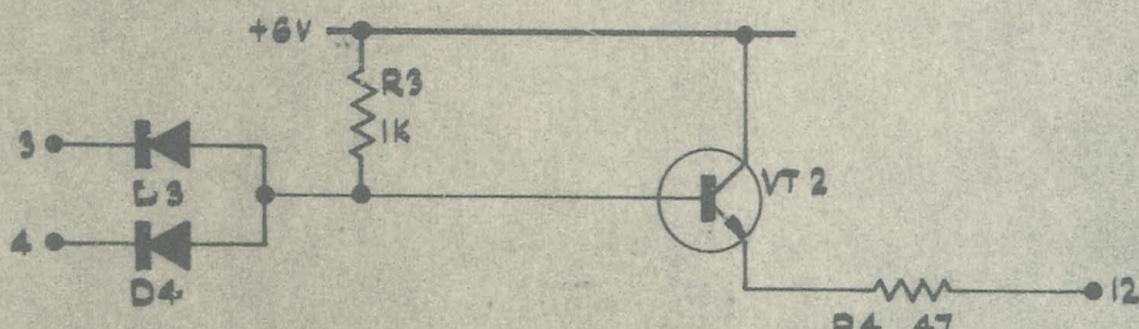
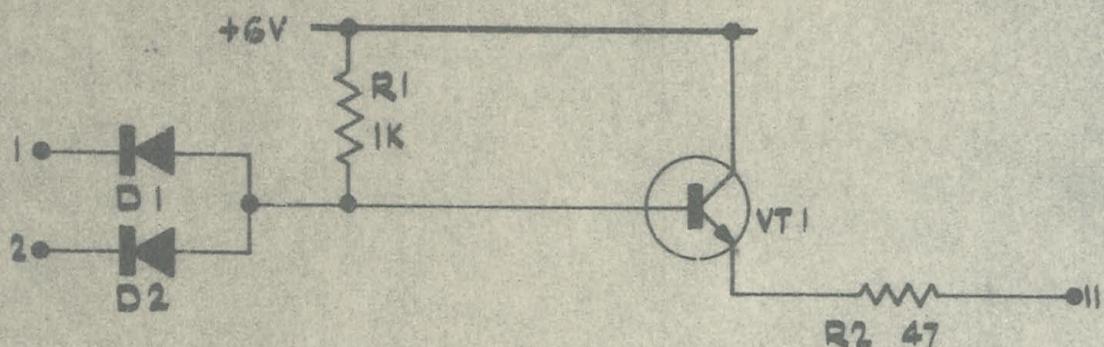
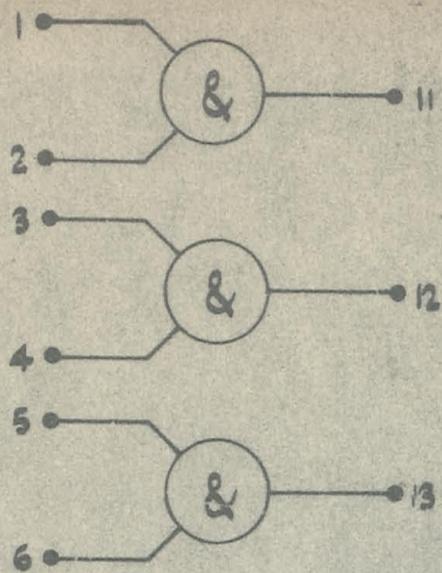
INSTRUCTION SHEET

322A7191

SHEET NO 24  
OF



O/P'S 11, 12, 13, TO 50  $\mu$  COAX.



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100

+6V —————— 21

DRAWN	C.A.C.	ISSUE No.	1
CHECKED	CS 456	A.R. No	1374
APPROVED	E.R.M.	DATE	26-4-66
DATE	16/5/66	INITIALS	C.A.C.

ELLIOTT BROTHERS (LONDON) LTD.

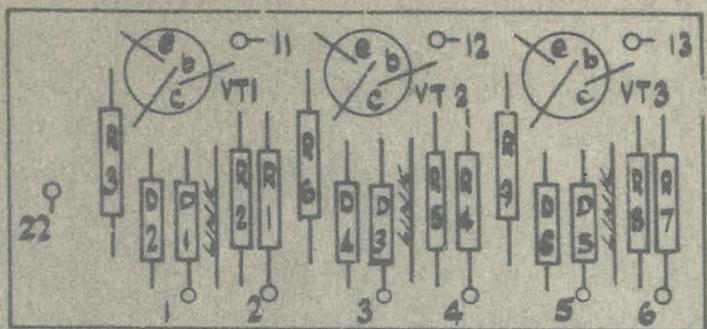
TITLE

L.S.A. 22.  
TWO INPUT TRANSMITTERS.

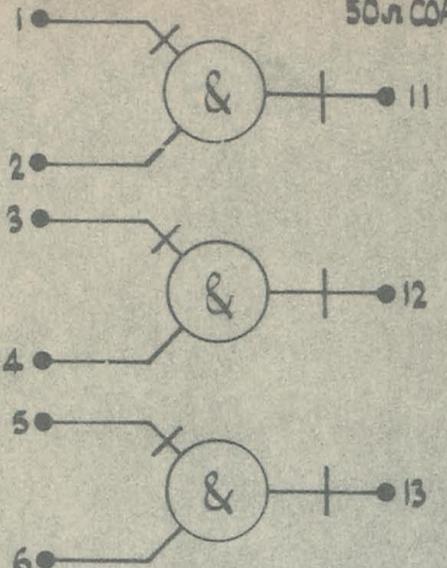
INSTRUCTION SHEET

322 A 7191

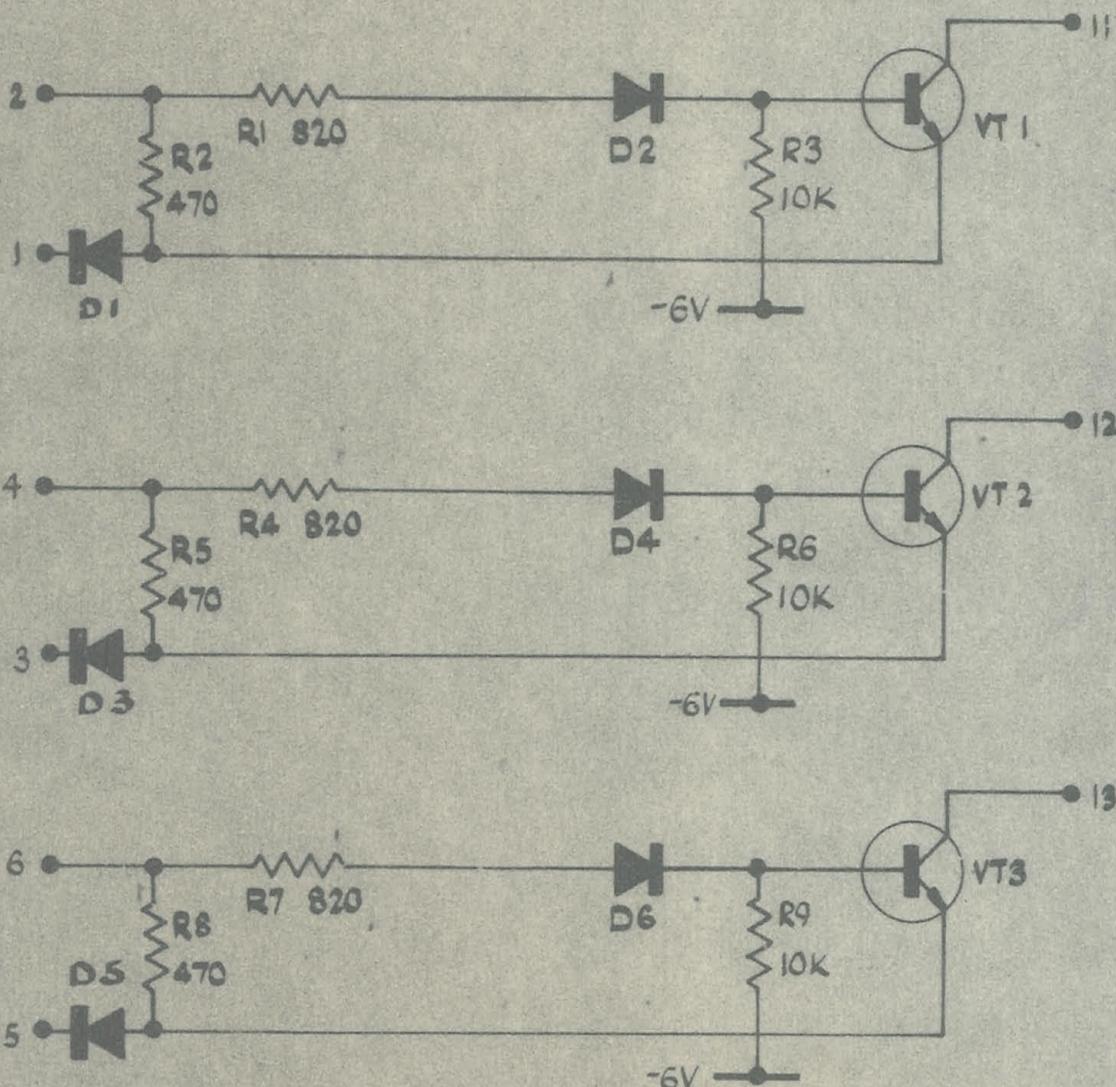
SHEET NO. 25  
OF



I/P'S 2,4,6. - DATA INPUTS FROM  
50 $\Omega$  COAX



I/P'S 1,3,5. CONNECTED TO AN  
O/P OF AN LSA 28.



DIODES ARE PURCH 101

TRANSISTORS ARE PURCH 100

PRINTED	C.A.C.	ISSUE No	1	2
REMOVED	CS 456	AR No	1374	1796
DATE	ZR/11/66	DATE	26-4-66	26-11-66
INITIALS		C.A.C.		

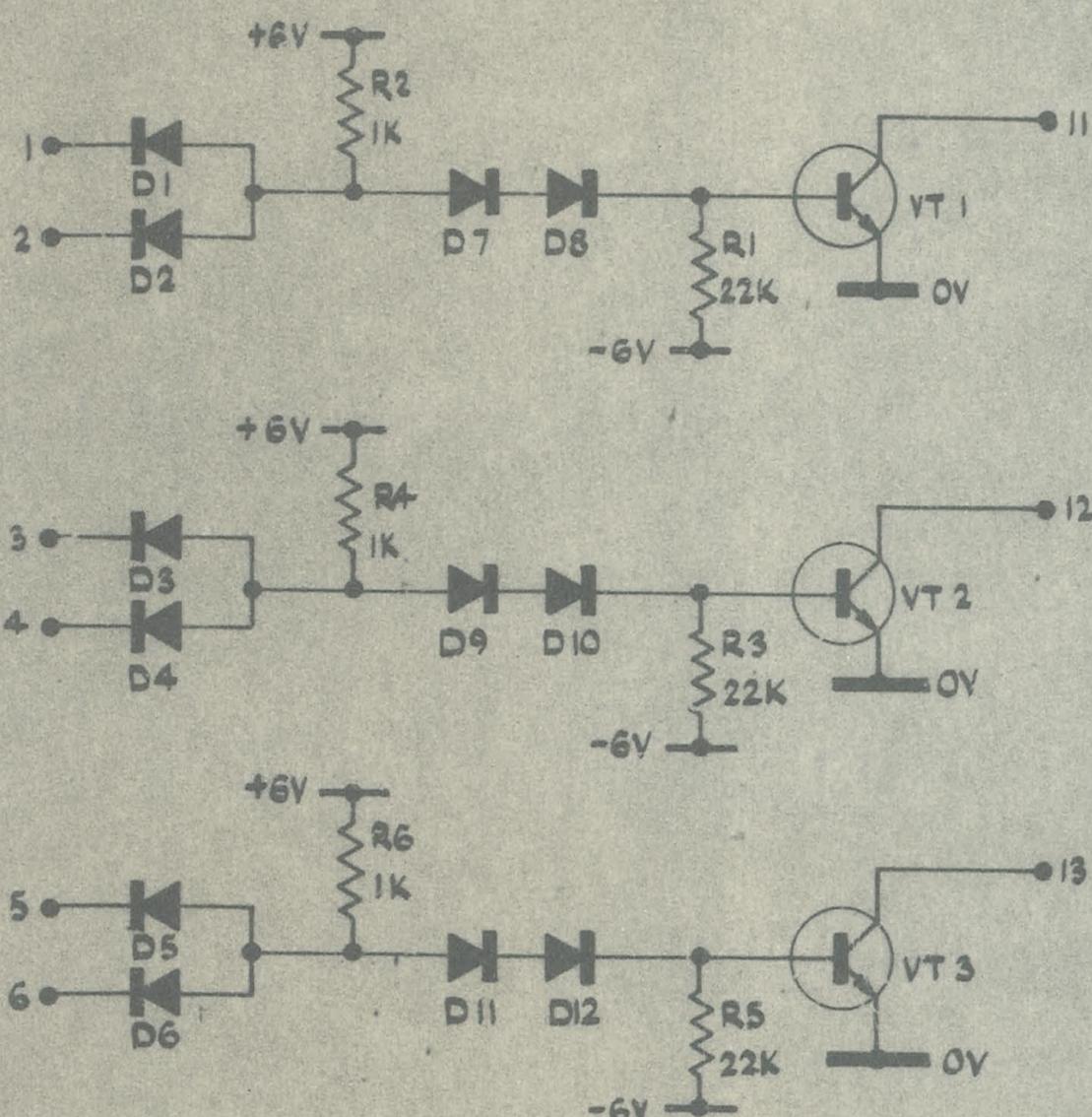
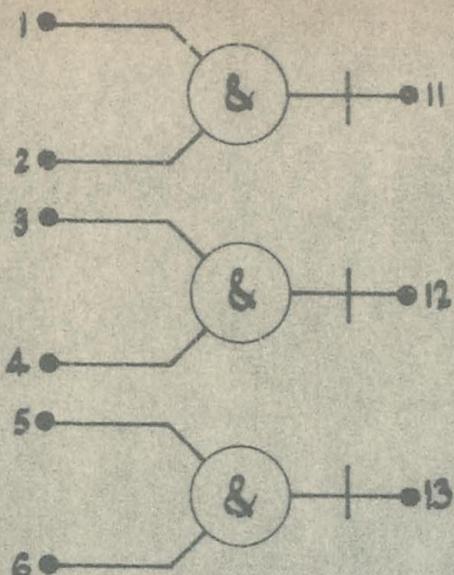
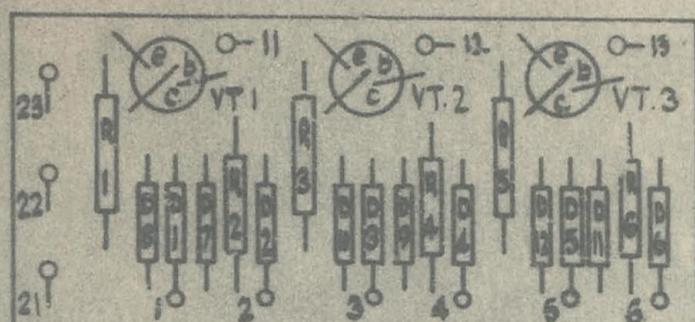
ELLIOTT BROTHERS (LONDON) LTD.

L.S.A. 23  
GATED RECEIVERS.

INSTRUCTION SHEET

322 A 7191

SHEET NO 26  
OF



DIODES ARE PURCH 101  
TRANSISTORS ARE PURCH 100.

+6V —— 21  
OV —— 23  
-6V —— 22

DRAWN C.A.C. ISSUE No. 1  
CHECKED CS456 AR. No. 1374  
APPROVED E.P. DATE 26-4-66  
DATE 16/5/66 INITIALS C.A.C.

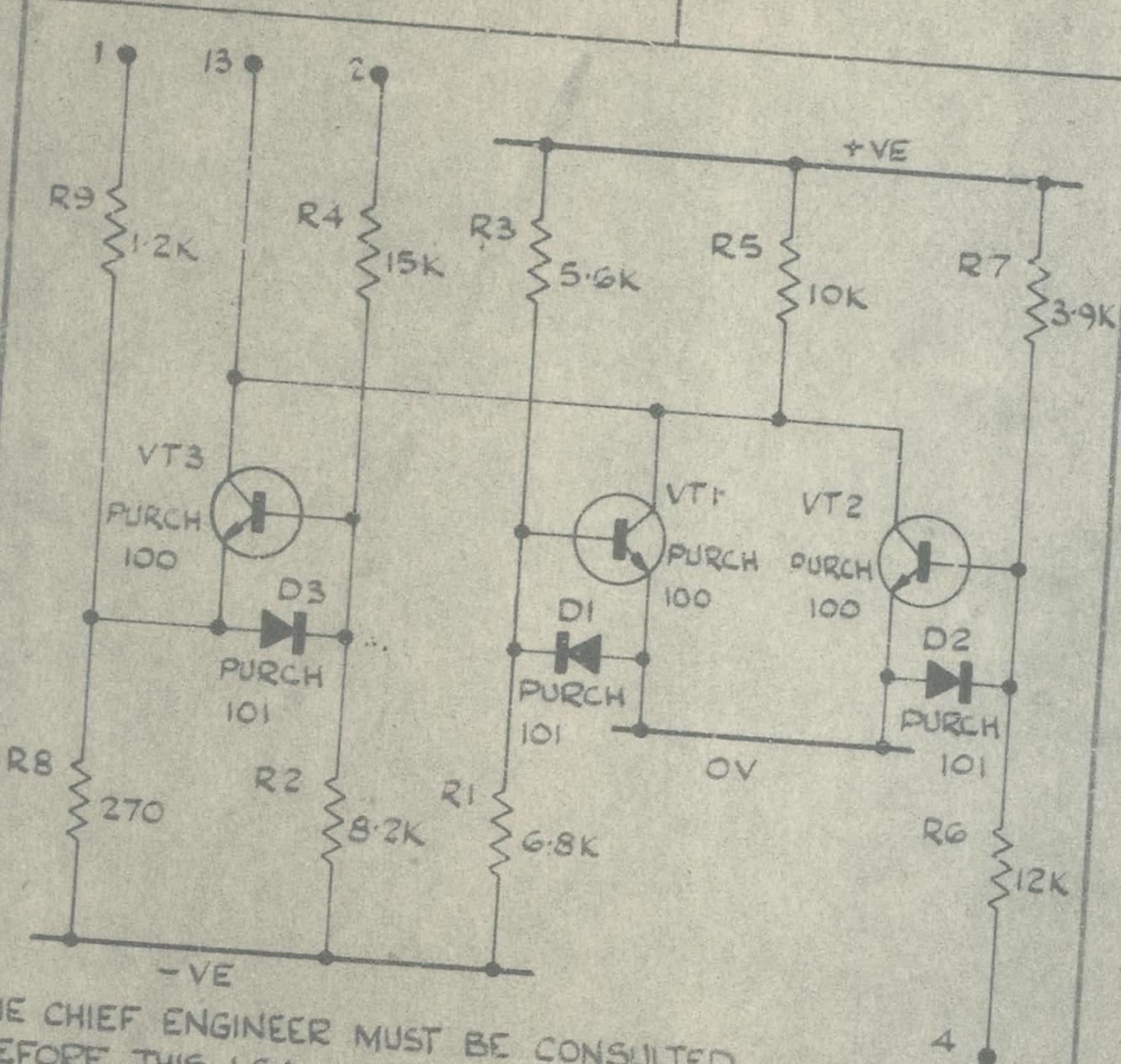
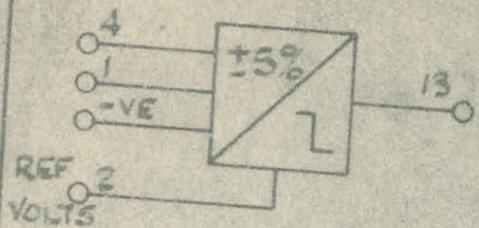
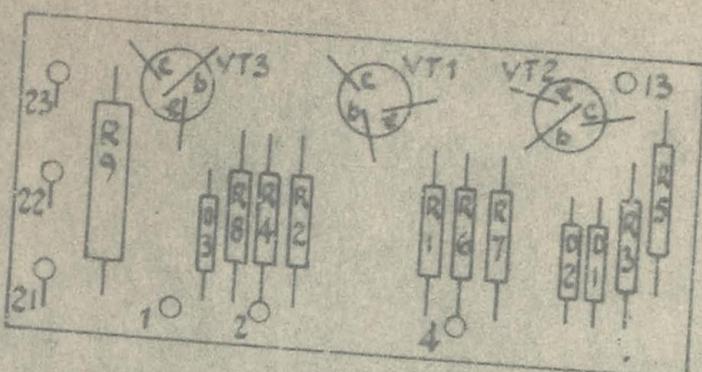
ELLIOTT BROTHERS (LONDON) LTD.

TITLE  
LSA. 28  
2-INPUT NAND GATES.

INSTRUCTION SHEET

322A7191

SHEET NO. 27  
OF



THE CHIEF ENGINEER MUST BE CONSULTED  
BEFORE THIS LSA IS USED ON ANY PROJECT  
OTHER THAN THE MARITIME STORE.

DRAWN K.G.

ISSUE NO. 1

CHECKED

AP. NO 1588

APPROVED

DATE 26-8-66

INITIALS

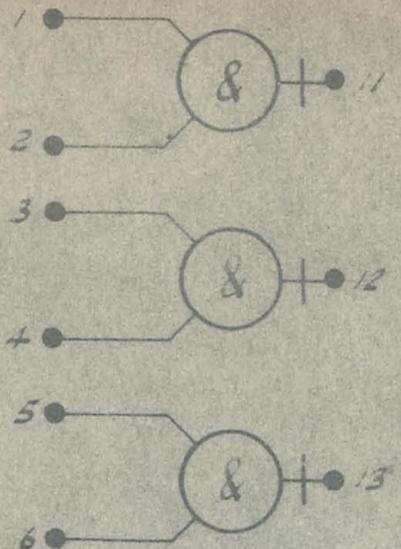
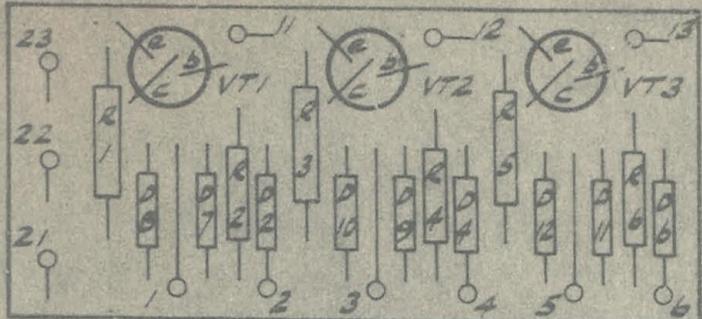
K.G.

ELLIOTT BROTHERS (LONDON) LTD.  
LSA 43  
VOLTAGE RAIL SENSING

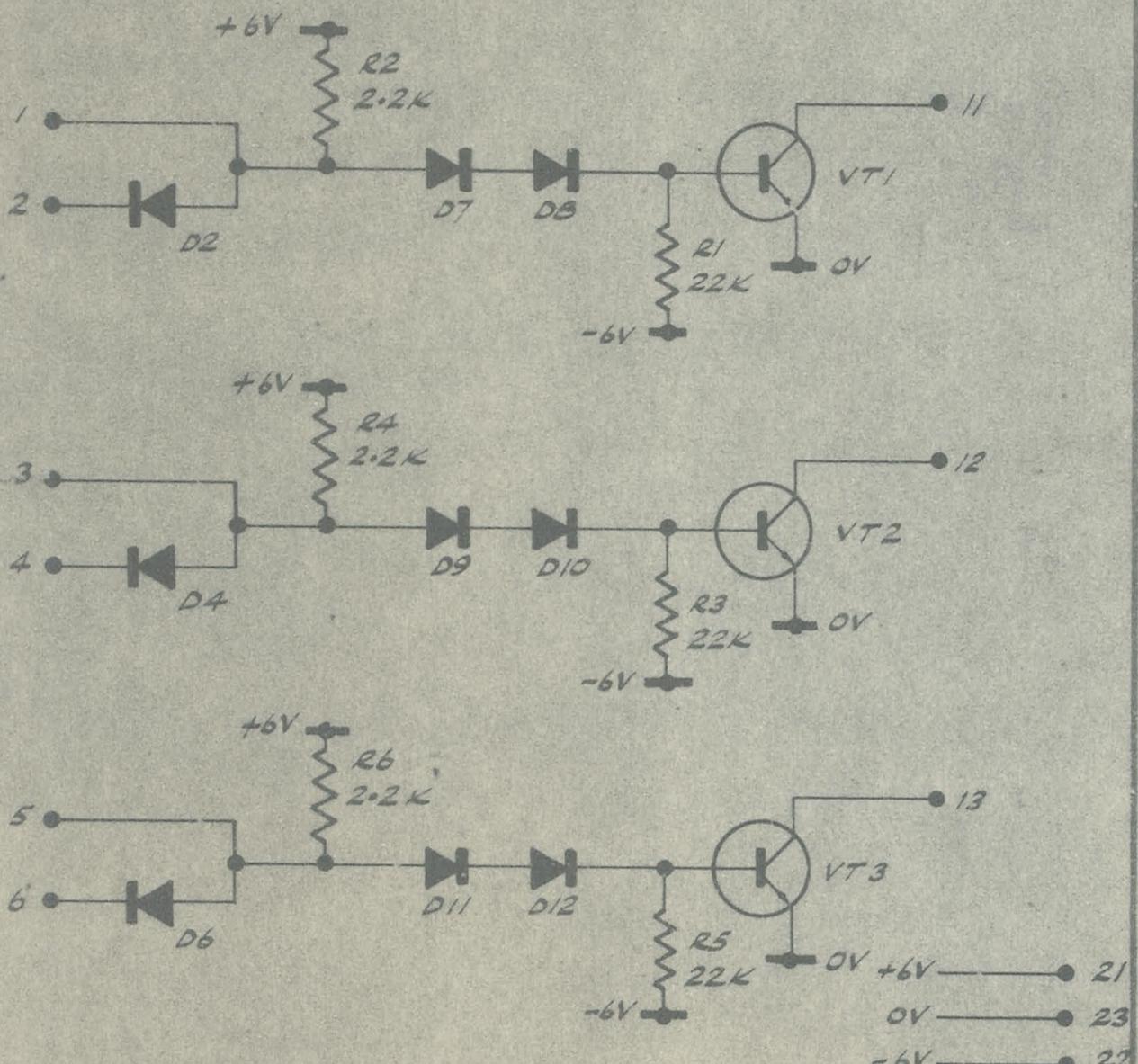
INSTRUCTION SHEET

322A 7191

HEET NO. 28  
OF



DIODES ARE PURCH-101  
TRANSISTORS ARE PURCH-100



N.G.R.H. ISSUE NO. /  
CS P.H.S. A.R. NO.  
DATE 26.11.66  
INSTAL. 111

ELLIOTT BROTHERS (LONDON) LTD.

LSA 44  
2- INPUT NANDGATE 920B  
(USED IN CONJUNCTION WITH LSA 23)

INSTRUCTION SHEET

322A7191

SHEET No. 29  
OF