905 Digital Computer

Note: original had coloured cardboard section dividers not included in this scan.

The 905 is a powerful 18-bit digital computer using advanced integrated circuit technology backed by full 900 Series software support and including as standard such features as four program levels, hardware multiply and divide and initial instructions. Optional extensions such as multiplexers, autonomous transfer and dual program units provide facilities for a large number of peripheral devices to time-share the processor or memory. These extensions permit the economical assembly of a wide variety of single and multi-computer configurations. This machine of high reliability was designed primarily for on-line applications, but also has very good off-line capabilities. Programs and interfaces for the 903 Computer are fully compatible with the 905.

Features of the 905 include:

18-bit parallel arithmetic.

Core store with 1-microsecond cycle time, and capacity from 8192 to 131072 words.

Flexible and powerful order code, including 35-bit multiply and divide.

Fast and simple interface with four program levels under interrupt control.

Direct transfer of data between peripherals and store.

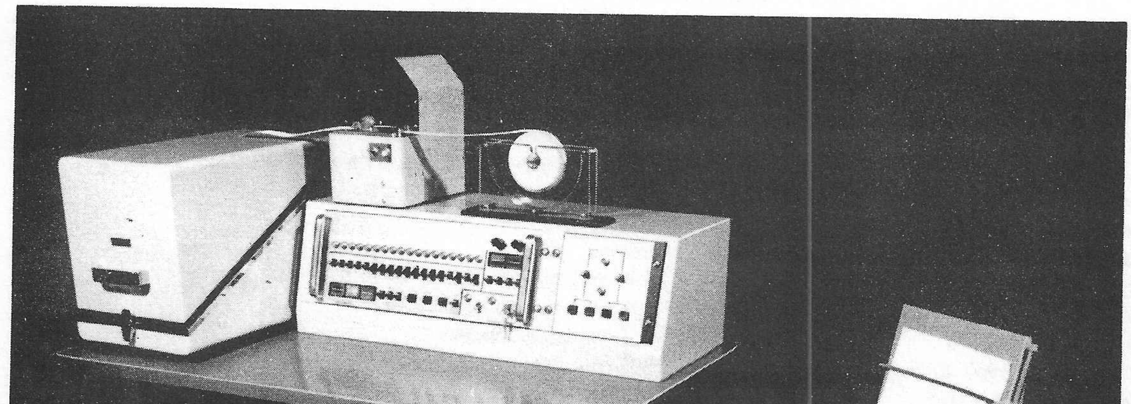
Wide range of peripherals, including magnetic disc and visual input-output devices.

Word formats

Each 18-bit word may be used to hold:

An instruction.

A fixed point fraction in the range -1 to $+1-2^{-17}$



905 Digital Computer

An integer in the range −131 072 to +131 071.

Three alphanumeric characters.

Eighteen individual Boolean (Yes/No) variables.

With the exception of an instruction, combinations of these words with ranges modified as necessary.

Software Packages are provided to allow:

Double-length fixed-point working on fractions, mixed numbers or integers.

Floating-point arithmetic.

Two formats are available for floating-point number representation; packed format in which two words represent a mantissa of 28 bits (including sign) and an exponent of 7 bits, and unpacked format in which three words are used to represent a mantissa of 35 bits (including sign) and an exponent of 16 bits. In packed format the range of numbers is approximately -10^{18} to $+10^{18}$, with an accuracy of 8 significant decimal digits. In the unpacked format the range of numbers is approximately $-10^{20,000}$ to $+10^{20,000}$ and an accuracy of 10 significant decimal digits.

Instructions

When a word represents an instruction the 18 digits are divided as follows:

bit 18	B, modifier flag.
bits 17–14	F, function.
bits 13–1	N, store address, or a further specification of the function.

There are 14 store reference instructions, including read from store and write to store, add, subtract, collate, increment store, multiply, divide, and conditional and unconditional jump. These instructions can also be used for addressing the registers which are held in store, such as the B-registers. There are two further instruction groups (F=14 and F=15) in which the address part of the instruction is used to specify the function further. These two groups are used for such purposes as shifting the accumulator, input-output instructions, inter-register transfers and conditional skips. The resulting instruction set is most comprehensive and contains some 67 functions excluding input-output variants.

Registers

The following registers are accessible to the programmer:

A-register (18 bits) Accumulator. This holds the results of operations.

Q-register (18 bits) An extension accumulator, or can be used as a second arithmetic register.

B-register (18 bits) Modifier register. There is one of these for each of the four program levels, held in locations 1, 3, 5 and 7 in store.

S-register (17 bits) Sequence control register. There is one of these for each of the four program levels. When an S-register is not in use, it is held in one of locations 0, 2, 4 and 6 in store. The current S-register is held in hardware for speed of access.

H-register (1 bit) Sector flag. There is one of these for each of the four program levels, held in bit 18 of one of locations 0, 2, 4 and 6 in store, when not in use. The current H-register is held in hardware for speed of access.

Switch-register (18 bits) Contains the word set up on the word generator keys.

Address modes

There are 14 store reference instructions. The store address is given by N (bits 1–13 of the instruction word). This is interpreted according to the values of the H-register (1 bit) and the modifier flag (bit 18 of the instruction word).

If H=0 or if the instruction is a jump instruction, the address is relative to the base of the current 8192-word block of store.

If H=1 and the instruction is not a jump instruction, the address is relative to the base of the first 8192-word block of store. (This is the block which holds the B-registers, the inactive S-registers and the Intitial Instructions when they are activated).

If the modifier flag is zero the operand address is as described above. If the modifier flag is 1 this address is modified by adding to it bits 1–17 of the current B-register. Thus locations which are in neither the current block of store nor in the first block can be addressed. Modified instructions do not affect the current instruction as stored. They normally take 1·2 microseconds longer than unmodified instructions.

Typical function times:

Add	2·4 microseconds.
Collate	2·4 microseconds.
Multiply	10·2 microseconds.
Divide	19·0 microseconds.
Jump if Zero	1·2 microseconds.
Input/Output	5·5 microseconds (typical) for one 18-bit word. (Dependent on device response time).

Program levels and interrupt facility

Provision is made for four program priority levels, which are arranged to operate on an interrupt basis. An interrupt occurs as a result of a signal received from peripheral equipment. When a group of peripheral devices share an interrupt level, it is common practice to associate a status word with them, which will indicate the peripheral which has caused the interrupt and, in appropriate cases, to indicate further the reason for the interrupt.

Initial instructions

These instructions form a fixed program for loading programs into store using paper tape as the input medium. They operate on the highest priority program level (level 1). The instructions are activated by the JUMP/ INITIAL INSTRUCTIONS key on the control panel and are de-activated by leaving level 1 or setting the H-register to 1. When de-activated the locations they occupy are available for program use.

Store

The basic 905 computer has 16384 words of 1 microsecond core store. This may be extended in modules of 16384 words, to a total of 131 072 words. A minimal version with 8192 words of 1 microsecond core store is also available. Instructions may be placed in any location in store. Each store unit incorporates a parity checking facility. If the parity of a word read from store is wrong an external indication is given and, according to a switch on the control panel, the processor may stop. This facility is a valuable aid to fault location.

A preselected area of store may be protected under the control of the LOCK-OUT switch on the control panel. Use of this switch causes a LOCK-OUT lamp to light. The selected locations of store are then protected. This means that the contents of the selected locations can still be read and used as instructions or operands, but they cannot be altered or overwritten in any way. Any attempt to alter the contents of protected store locations causes an error signal to be sent to the central processor, which stops if the ERROR STOP switch on the control panel has been set. In this case the ERROR lamp in the LOCK-OUT switch will be lit.

Each word unit of store is divided into blocks of 1024 words. Any combination of these blocks may be selected for lock-out; selection is performed by wiring the store in a specified way.

In addition to this facility an optional unit called the Dual Program Unit is available which provides protection of a pre-selected area of store, during on-line program development. This facility is controlled by the Executive Software.

Peripherals

A wide range of peripherals is available for use with the 905 computer which operate from a 900 Series Standard Peripheral Interface.

Information may be transferred between a peripheral device and the store or the processor in one of the following three ways:

Single word tranfer: One 18-bit word is transferred by a single instruction to or from the accumulator via the Standard Peripheral Interface.

Block transfer: A series of 18-bit words is transferred to or from a series of consecutive store via the Standard Peripheral Interface by a single instruction. This process uses both the A and the Q registers.

Autonomous transfer: A series of 18-bit words is transferred to or from a series of consecutive store locations via the Autonomous Transfer Unit, while the central processor continues with other words.

The teleprinter, paper tape reader and paper tape punch are connected to the processor by a special interface which transfers 8-bit characters to or from peripherals, selected according to a 4-bit address.

The Marconi-Elliott 900 standard peripheral interface

Transfer of information between the central processor of a 900 Series computer and its peripheral devices is effected across the 900 Standard Peripheral Interface. Any peripheral device designed to match the 900 Standard Peripheral Interface may be connected direct. Peripherals with other interfaces, such as the BS 4421 interface, may be connected via the appropriate 900 Interface Matching Unit.

The peripheral interface signal lines operate one peripheral cluster. When more than one peripheral is required a 900 Multiplexer Unit is connected to the interface. Sockets are provided for up to seven peripheral clusters.

The Standard Peripheral Interface transfers 18-bit words in parallel between the accumulator and the peripheral. Each of the 900 Series peripherals is assigned a number within the range 0 to 15 which is known as the 'peripheral class number'. The sixteen classes of peripheral are normally selected according to bits 7 to 11 of the input-output instructions, while bits 1 and 2 are used to indicate the nature of the operation (e.g. data transfer or control/status). When the Interface is used in this way, one or more control words are frequently used to specify the operation further. Certain classes of peripherals use all of bits 1 to 6 to indicate the nature of the operation. They may, in addition, require control words. The Interface has three interrupt lines, which are used by the peripheral to interrupt the processor on a priority basis.

Autonomous access facility

There are four autonomous store access channels which are connected to the "data bus" lines interconnecting store and processor. An Autonomous Transfer Unit (ATU) may be connected to any of these four channels. This provides facilities for up to eight peripherals to transfer information to and from the store, without using valuable processor time. Information is extracted from, and placed in, store by 'stealing' store cycles, thus interleaving data transfers with normal computing. Control logic in the processor regulates the use of the 'data bus' system. The autonomous access channel requiring to perform a transfer, sends a 'request' signal to the control logic, which then allocates the next complete store cycle for the channel's use.

If simultaneous 'requests' are received from more than one autonomous access channel, the control logic accepts them on a fixed priority basis. If no requests are waiting the processor can access the store.

Total time for transfer of one 18-bit word into or out of store is between 1·5 microseconds and 2·7 microseconds on the highest priority channel. The maximum possible data transfer rate is 833333 words per second.

Among the units which use the autonomous access facility the most important is the Autonomous Transfer Unit, which can drive up to six Standard 900 Series peripherals. The standard ATU is controlled via reserved store locations and is suitable for controlling peripherals whose data transfer rate does not exceed 200000 words per second.

Mains power failure protection

Should mains power failure occur, the power supplies are sequenced off in such a manner as to retain store contents.

In addition, a level 1 (top priority) interrupt occurs about 9·9 milliseconds after the mains fail. About 100 microseconds later the computer goes into the RESET state. This gives time for an interrupt routine to store the registers, including the sequence control register, thus preserving vital information. The computer remains at RESET for a suitable minimum period. This is intended to minimise the effects of transients prior to the restoration of the supply voltage to a normal working level, the program and data stored in the core store will still be correct.

Control and monitor panel

The control and monitor panel normally stands on the basic computer desk.
It provides the following facilities:

Loud-speaker. This gives audible indication that the computer is operating.

Word generator. A set of 18 two-position keys corresponding to the 18 bits of the computer word. The word set up on these keys may be interpreted as a starting address, as an input word, or as an instruction.

Operator's Controls. Controls providing sufficient facilities for program check-out and running.

Engineer's Controls. Controls providing additional facilities for fault location.

Monitor Lamps and Selector Switch. A set of lamps which may be switched to monitor any of the registers or control bistables within the processor.

On/off Master Control Switch. This switch, which is key operated, has four positions, namely: off, auto, operate and test. According to its position, only the relevant control switches are operative.

Construction

The Marconi-Elliott 905 central processor is constructed using integrated circuits throughout. These integrated circuits are general purpose digital logic and are noted for low power consumption, high packing density, high noise rejection and high reliability throughout the operating temperatures range. Components are used well below their maximum ratings. 905 computing systems are packaged to simplify maintenance, with the logic mounted on plug-in boards in standard racks measuring 48·25cm (19 inches) wide; backwiring is partly printed and partly wirewrapped.

The structure is designed for easy access, all units of the processor are mounted in such a way as to be easily removed, so that all components and wiring are easily accessible.

The standard computer may be supplied either as a series of 48·25cm (19 in.) rack-mounting units, or in a free-standing cabinet.

Standard Configurations

In order to simplify the choice available to the user, certain standard configurations have been evolved, which give optimum facilities. These are:

905/C20 Basic System
16384 word store, Paper Tape Station, Teleprinter, Software – the operating system with this configuration is the EX 900. Options – Digital Plotter.

905/C30 Basic ATU System
16384 or 32768 word store, Paper Tape Station. Teleprinter. 2 or 6 channel ATU. Software – the operating system with this configuration is the EX 900. Options – Digital Plotter, Line Printer.

905/C50 Disc Based Systems
16384 or 32768 word store. Paper Tape Station. Teleprinter. 2 or 6 channel ATU. 890 Kilo word Disc with Controller. Software– the operating system with this configuration is RADOS. Options – Digital Plotter, Line Printer.

These standard configurations are designed to allow optimum use to be made of standard software and operating systems. Other configurations with additional peripherals are, of course, available.

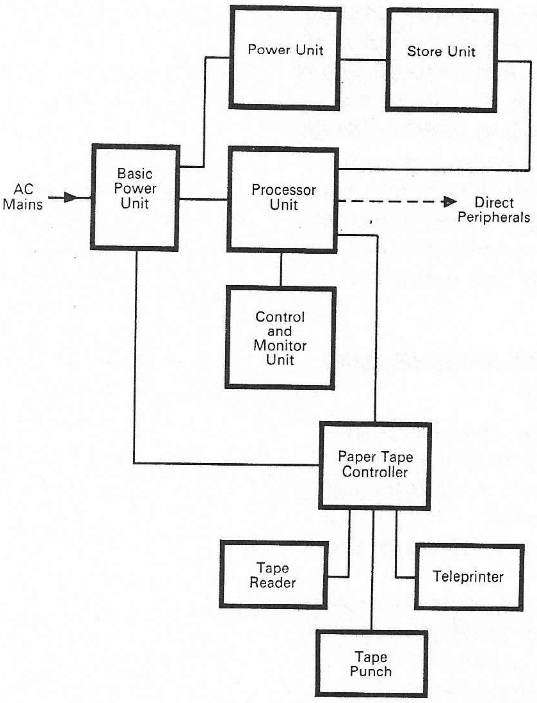
Marconi-Elliott Computer Systems Limited
A GEC-English Electric Company

Elstree Way, Borehamwood, Hertfordshire
Telegrams and Cables: Elliotauto Borehamwood
Telex: 22777 Answerback: Ellauto Borhwd
Telephone: 01–953 2030

Basic 905 System

CONFIGURATION

A basic 905 system comprises a Processor unit, a 1·2 μs or 2 μs store units, Power unit, Control and monitor panel, Paper tape control unit, Teleprinter, Tape reader and Tape punch.



Configuration Diagram-Basic 905 System

WORD LENGTH AND FORMAT

Numbers and instructions in the 905 system are each 18 bits in length. Numbers are represented in fractional form, negative numbers being held in 'two's complement' form. They will thus be in the range −1 to $1-2^{-17}$. The significance of individual bits in a number are shown below:

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
-12^{-1}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}

Instructions are of the single address type, one instruction being represented by an 18-bit word. An instruction word consists of three parts:

Modifier (B)—1 bit—specifies whether modification is required

Function (F)—4 bits—specifies the operation to be carried out

Address (N)—13 bits—specifies, generally, the store address of one operand.

The instruction format is as shown below:

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
B		F								N							

STORE

The store of a 905 system may hold 8192, 16384, 24576 or 32768 words each of 18 bits; these are referred to by addresses in the ranges 0 to 8191, 16383, 24575 or 32767 respectively. The following types of store may be fitted:

(a) An 8192 word unit having a cycle time of 1.2 μs. Up to 4 such units may be fitted.

(b) A 16384 word unit having a cycle time of 1.2 μs. 2 such units may be fitted.

(c) A 16384 word unit with a cycle time of 2.0 μs. 2 such units may be fitted.

In the case of (a) and (b) above, store operation is checked by means of a parity bit which is stored with each word; on writing into the store this bit is set to give the whole word odd parity. If even parity is detected on reading from the store the computer may stop (see the description of the Control and Monitor Unit).

The standard 905 has addressing facilities for up to 65536 words of store; may be modified to address up to 131072 words of store. The connection of stores of these sizes requires the use of special ancillary units.

REGISTERS

The following registers are used by instructions:

A Register: This is an accumulator with a capacity of 18 bits which is used to hold the result of most operations.

Q Register: This a register with a capacity of 18 bits which is used to hold information temporarily during a computation and also as an extension of the accumulator for numbers containing more than 18 significant bits. In this case it extends the less significant end of the accumulator by 17 bits, using bits 2 to 18 of the Q register. The register used in this way is known as the Auxiliary register.

B Register: This 18 bit register holds the number which is added to the N bits of the instruction to form the address if the B bit of the instruction is a 'one'.

S Register: This register, with a capacity of 17 bits, controls the extraction of instructions from the store: it is incremented as each instruction is extracted from the store so that instructions are obeyed in numerical sequence. In the standard system, having 8192 words of store, only 13 bits of S are used.

H Register: This register, of one bit only, controls the manner in which instructions address locations of the store. It is only relevant when the store is extended beyond 8192 words.

PROGRAM LEVELS AND INTERRUPT FACILITY

Provision is made for four program priority levels, which are arranged to operate on an interrupt basis. If, while the computer is running, an interrupt signal is received for a higher priority program, the program currently being obeyed will be temporarily suspended as soon as the instruction (other than function O) currently being obeyed is completed and the higher level program will be obeyed. When this higher level program is terminated by a program terminate instruction the computer will revert to the lower level program and continue from the point at which it was interrupted.

A sequence control register (S register), an address mode indicator (H) and modification register (B register) are provided for each program level. These registers are held in the computer store in location 0 to 7 as follows:

	S Register	*H Register*	*B Register*
Program level 1	0 (digits 1–17)	0 (digit 18)	1
2	2 as above	2 as above	3
3	4 as above	4 as above	5
4	6 as above	6 as above	7

Program level 1 is the highest priority and cannot be interrupted.
Program level 2 may be interrupted only by level 1.
Program level 3 may be interruptde by levels 1 and 2.
Program level 4 may be interrupted by levels 1, 2 and 3.

Interruption occurs as a result of a signal received from a peripheral equipment.

The S and H registers corresponding to the program level currently in use are held in the processor for fast access, being automatically stored and replaced by previously stored values when interruption or termination occurs.

The A and Q registers must be stored by program instructions at the beginning of the higher priority program, and restored before termination. At the initial start-up of the program system the starting address for the appropriate programs must be placed in locations 2, 4 and 6. This is normally done by a program operating on level 1 entered by the 'Jump' control described under Manual Group Controls and Indicators.

INSTRUCTION REPERTOIRE AND OPERATION TIMES

In the tables that follow, the effects of instructions are defined in terms of the initial and final contents of registers and store locations as follows:

S, A, Q, B refer to the contents of the various registers.

AQ refers to the contents of A and Q regarded as a double-length number.

B, F, N refer to the parts of the instruction word being obeyed.

Numbers in square brackets indicate particular bits of registers, e.g. A [1–8] means bits 1–8 of register A.

Primes indicate the contents of store locations specified, e.g. N' means the contents of store location N.

M means the address of the modifier register of the current program level, i.e., location 1, 3, 5 or 7 depending on which priority level is currently operating.

: = means 'is made equal to'.

The instruction times quoted are nominal figures subject to a tolerance of ±15%.

UN-MODIFIED INSTRUCTIONS (B = 0) (a) Inter-register transfers

Name	*Operation*	*Other effects*	*Time*		*Instruction*	
			1·2 μs store	*2 μs store*	*F*	*N*
A to B	B: = A		4·0	5·6	15	7174
			3·2	4·8	5	M
A to Aux.	Q[2–18]: = A[1–17]		3·6	4·4	15	7172
B to Q	Q: = B		3·6	6·0	0	M
S to B	B[1–13]: = S[1–13] B[14–18]: = 0	Q[14–17]: = S[14–17] Q[1–13]: = 0	3·2	4·8	11	M
B to A	A: = B		4·1	6·0	15	7175
			2·4	4·0	4	M
Aux. to A	A[1–17]: = Q[2–18] A[18]: = 0		3·6	4·4	15	7173
Aux. to B	B[1–17]: = Q[2–18] B[18]: = 0		3·2	4·8	3	M

(b) Transfers between registers and store

Name	*Operation*	*Other effects*	*Time*		*Instruction*	
			1·2 μs store	*2 μs store*	*F*	*N*
Read	A: = N′		2·4	4·0	4	N
Load B	B: = N′	Q: = N′ (no interrupt following this instruction)	3·6	6·0	0	N
Load Q	Q: = N′	B: = N′ (no interrupt following this instruction) OR	3·6	6·0	0	N
		A: = N′−A	3·2	4·8	2	N
Write	N′: = A		3·2	4·8	5	N
Store S	N′[1–13]: = S[1–13] N′[14–17]: = 0	Q[14–17]: = S[14–17]	3·2	4·8	11	N
Store Aux.	N′[1–17]: = Q[2–18] N′[18]: = 0		3·2	4·8	3	N

(c) Arithmetic between Accumulator and B register

Name	*Operation*	*Other effects*	*Time*		*Instruction*	
			1·2 μs store	*2 μs store*	*F*	*N*
Add A to B	A: = A+B		2·4	4·0	1	M
Subtract A from B	A: = B−A	Q: = B	3·2	4·8	2	M
Multiply A by B	AQ: = A×B	Q[1] altered	9·6	11·2	12	M
Divide by B	A: = AQ÷B	Q: = AQ÷B	18·4	20·2	13	M
Collate A with B	A: = A and B		2·4	4·0	6	M

(d) Arithmetic between Accumulator and Store

Name	*Operation*	*Other effects*	*Time*		*Instruction*	
			1·2 μs store	*2 μs store*	*F*	*N*
Add	A: = A+N′		2·4	4·4	1	N
Negate and add	A: = N′−A	Q: = N′	3·2	5·3	2	N
Multiply	AQ: = A×N′	Q[1] altered	10·2	12·2	12	N
Divide	A: = AQ÷N′	Q: = AQ÷N′	19·3	21·3	13	N
Collate	A: = A and N′		2·4	4·4	6	N

(e) Transfer control

Name	*Operation*	*Other effects*	*Time*		*Instruction*	
			1·2 μs store	*2 μs store*	*F*	*N*
Jump zero	if A = 0 then S: = N		1·2	2·0	7	N
Jump	S: = N		1·2	2·0	8	N
Jump negative	if A < 0 then S: = N		1·2	2·0	9	N
Count and test	B: = B+1 if B[1–13] = 0 then S: = S+2		6·0 (B ≠ 0) 6·8 (B = 0)	8·4 (B ≠ 0) 9·2 (B = 0)	15	7170
Test standard	if A > +½ or A < −½ or A = 0 then S: = S+2		2·8 (not standard) 3·6 (standard)	3·6 (not standard) 4·4 (standard)	15	7169

(f) Miscellaneous

			Time		Instruction		
Name	*Operation*	*Other effects*	*1·2 μs store*	*2 μs store*	*F*	*N*	*Notes*
Count in B	B: = B+1		3·6	6·0	10	M	
Count in store	N′: = N′+2^{-17}		3·6	6·0	10	N	
Shift left	AQ: = AQ×2^{N}		2·8+0·8n	3·6+0·8n	14	0 to 36	
Shift right	AQ: = AQ×2^{N-8192}		2·8+0·8n	3·6+0·8n	14	8156 to 8191	i.e. shift right 8192−N (= n) places
Terminate	Current program level terminated		7·2	10·4	15	7168	
Set relative	H: = 0		3·6	4·4	15	7176	used only in conjunction with extended store
Set absolute	H: = 1		3·6	4·4	15	7177	

(g) Input and Output

			Time		Instruction		
Name	*Operation*	*Other effects*	*1·2 μs store*	*2 μs store*	*F*	*N*	*Notes*
Key input	A: = word generator		3·6	4·4	15	7171	
Tape input	A[9–18]: = A[2–11] A[8]: = A[1] or character [8] A[1–7]: = character [1–7]		5·2 (min.)	6·0 (min.)	15	2048	Acc-shifted left 7 places and 8 bit character logically mixed in
Teleprinter input	A[9–18]: = A[2–11] A[8]: = A[1] or character [8] A[1–7]: = character [1–7]		5·2 (min.)	6·0 (min)	15	2052	do. Input from tape reader when teleprinter not fitted
Word input	A: = input word		5·2 (min.)	6·0 (min.)	15	0 to 2047	Input device and action selected externally by N[1–11]
Block input	A′: = 1st input word (A+1)′: = 2nd input word etc. (A+Q[1–12]−1)′: = last input word	A,Q altered	4·4+ 5·2n (min.)	5·2+ 6·0n (min.)	14	2048 to 4095	Input device and action selected externally by N[1–11] No. of words input = Q[1–12] (= n)
Tape output	Character: = A[1–8]		5·2 (min.)	6·0 (min.)	15	6144	
Teleprinter output	Character: = A[1–8]		5·2 (min.)	6·0 (min.)	15	6148	
Word output	Output word: = A		5·2 (min.)	6·0 (min.)	15	4096 to 6143	Output device and action selected externally by N[1–11]
Block output	1st output word: = A′ 2nd output word: = (A+1)′ etc. Last output word: = (A+Q[1–12]−1)′	A,Q altered	4·4+ 5·2n (min.)	5·2+ 6·0n (min.)	14	4096 to 6143	do. No. of words outputQ[=1–12](=n)

MODIFIED INSTRUCTIONS

When the B digit of an instruction is 1, the instruction is said to be "modified"; the effect of this is that the address of the instruction is altered by the addition to it of the contents of the B register. In the standard system, with 8192 words of store, the resulting address must not be outside the range 0 to 8191.

In the following tables all useful modified instructions are listed.

X is used to mean B+N.

(a) Transfers between registers and store

			Time		Instruction	
Name	*Operation*	*Other effects*	*1·2 μs store*	*2 μs store*	*F*	*N*
Read	A: = X′	Q altered	3·6	6·0	4	N
Load B	B: = X′	Q: = X′	4·8	8·0	0	N
Load Q	Q: = X′	B: = X′	4·8	8·0	0	N
		A: = X′−A	4·4	6·8	2	N
Write	X′: = A	Q altered	4·4	6·8	5	N
Store S	X′: = S[1–13]	Q: = S[14–17]	4·4	6·8	11	N

(b) Arithmetic between registers and store

Name	Operation	Other effects	Time 1·2 μs store	 2 μs store	Instruction F	 N
Add	A: = A+X′	Q altered	3·6	6·0	1	N
Negate and Add	A: = X′−A	Q: = X′	4·4	6·8	2	N
Multiply	AQ: = A×X′		10·8	13·2	12	N
Collate	A: = A and X′	Q altered	3·6	6·0	6	N

(c) Transfer control

Name	Operation	Other effects	Time 1·2 μs store	 2 μs store	Instruction F	 N
Jump zero	if A = 0 then S: = X	Q altered	1·2 (A ≠ 0) 2·4 (A = 0)	2·0 (A ≠ 0) 4·0 (A = 0)	7	N
Jump	S: = X	Q altered	2·4	4·0	8	N
Jump negative	if A < 0 then S: = X	Q altered	1·2 (A ⩾ 0) 2·4 (A < 0)	2·0 (A ⩾ 0) 4·0 (A < 0)	9	N

(d) Miscellaneous

Name	Operation	Other effects	Time 1·2 μs store	 2 μs store	Instruction F	 N	Notes
Count in store	X′: = X′+2^{-17}	Q altered	4·4	8·0	10	N	
Word input	A: = input word	Q altered	6·4 (min.)	8·0 (min.)	15	N	X in range 0–2047, device and action selected by X[1–11]
Word output	Output word: = A	Q altered	6·4 (min.)	8·0 (min.)	15	N	X in range 4096–6143, device and action selected by X[1–11]

Notes on Instruction code

(i) All arithmetic operations are exact except division where the results are as follows:

The quotient placed in A is rounded such that it is correct to $\pm 2^{-17}$ i.e.

$$A := \frac{AQ}{N'} \pm 2^{-17}$$

A[1] is always 1

The quantity placed in Q by a divide instruction is always 2^{-17} less than the quotient placed in A i.e.

$$Q := \frac{AQ}{N'} - 2^{-17} \pm 2^{-71}$$, Q[1] is always 0.

(ii) Modified shift instructions are not listed as the contents of Q are altered in an undefined manner before the shift operation takes place. They may however be used in situations where no account is subsequently taken of the altered bits.

(iii) An interrupt cannot take place between a function 0 instruction (i.e. Load B or Load Q) and the following instruction unless the latter is also function 0. In the latter case the contents of Q after the interrupt are undefined.

(iv) Q[1] may be changed from 1 to 0 by the action of a program interrupt. For this reason a block input or output instruction must be immediately preceded by a further 0 instruction setting the required contents of Q.

Program Compatibility

Programs written for the 903 computer using the instruction code defined in the 903 Manual can be accepted unchanged by the 905. This applies to the Symbolic Input Routine (SIR), the ALGOL and FORTRAN compilers and all other standard 903 software.

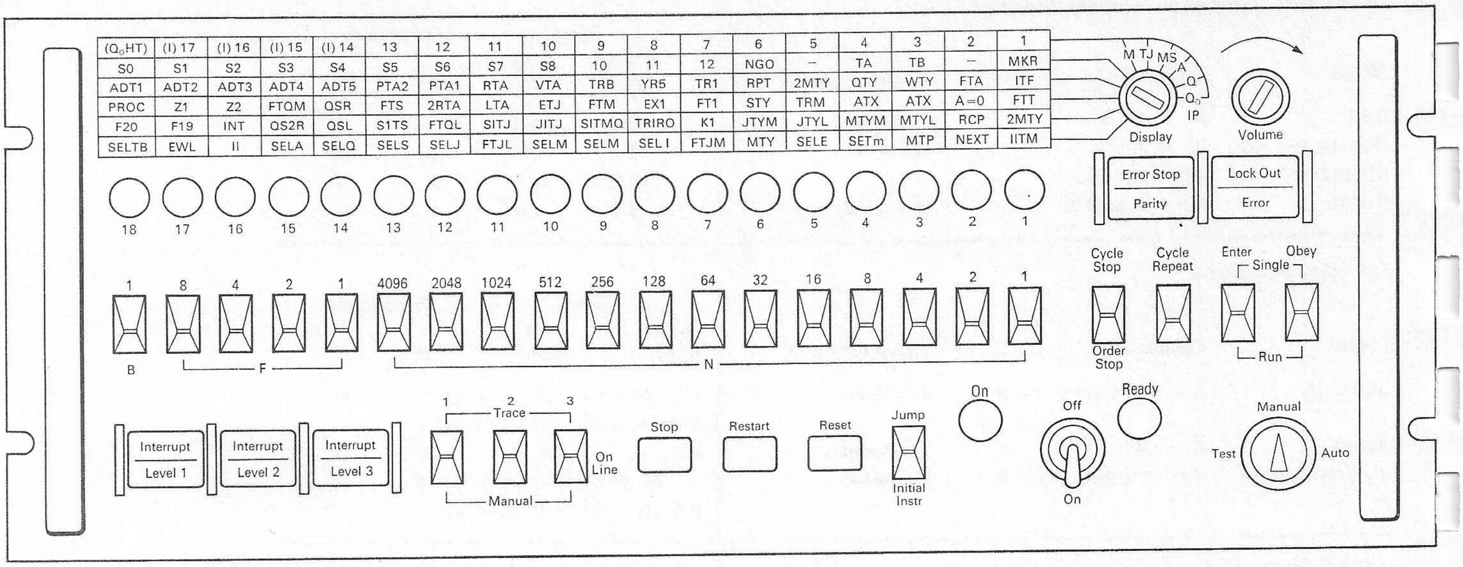
CONTROL AND MONITOR UNIT

Master Switch

This switch, operated by a Yale-type key, has three positions—AUTO, MANUAL and TEST. When it is in the AUTO position only the on/off switch is operative, when in the MANUAL position sufficient controls for the routine operating of developed programs are operative. When in the TEST position, all controls are operative.

Power Controls and Indicators

The ON/OFF switch controls the power switching for 905 and associated equipment. When switched on or off the power supplies are sequentially operated to retain store contents: the computer then either if the master switch is in MANUAL or TEST enters the RESET (quiescent) state described under Manual Group Controls and Indicators, or if the master switch is in AUTO starts obeying program, on level 1, at location 8177.
The POWER ON lamp is illuminated (colour green) whenever the ON/OFF switch is in the ON position and the mains supply is connected. The READY lamp is illuminated (colour green) when the power supplies have sequenced on correctly.


(Q$_0$HT) (I) 17 (I) 16 (I) 15 (I) 14 13 12 11 10 9 8 7 6 5 4 3 2 1
S0 S1 S2 S3 S4 S5 S6 S7 S8 10 11 12 NGO – TA TB – MKR
ADT1 ADT2 ADT3 ADT4 ADT5 PTA2 PTA1 RTA VTA TRB YR5 TR1 RPT 2MTY QTY WTY FTA ITF
PROC Z1 Z2 FTQM QSR FTS 2RTA LTA ETJ FTM EX1 FT1 STY TRM ATX ATX A=0 FTT
F20 F19 INT QS2R QSL S1TS FTQL SITJ JITJ SITMQ TRIRO K1 JTYM JTYL MTYM MTYL RCP 2MTY
SELTB EWL II SELA SELQ SELS SELJ FTJL SELM SELM SEL I FTJM MTY SELE SETm MTP NEXT IITM
M TJ MS A Q Q$_0$ IP
Display
Volume
Error Stop
Parity
Lock Out
Error
18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
1 8 4 2 1 4096 2048 1024 512 256 128 64 32 16 8 4 2 1
B
F
N
Cycle Stop
Cycle Repeat
Enter
Obey
Single
Order Stop
Run
Interrupt Level 1
Interrupt Level 2
Interrupt Level 3
1 2 3
Trace
On Line
Manual
Stop
Restart
Reset
On
Jump
Initial Instr
Off
On
Ready
Manual
Test
Auto

905 Computer Control and Monitor Panel

Manual Group Controls and Indicators

These controls are operative in the MANUAL and TEST positions of the master switch: the indicators are always operative.

The NUMBER GENERATOR switches comprise 18 two-position switches which may be set to represent the binary digits of a computer word. This word may be used:

As a computer input, read by a 15 7171 instruction.

As a starting address (in the range 0 to 8191) in conjunction with the JUMP control.

As a word to be placed in the A register described under Test Group Controls and Indicators.

As an instruction to be obeyed, described under Test Group Controls and Indicators.

The RESET push button is used to restore the computer and associated equipment to their initial state, referred to as the 'reset' state. The RESET lamp, incorporated in the push button, is lit as long as the state persists. The RESET state is terminated as follows: when the master switch is set to AUTO the state is terminated automatically in the switch-on sequence: when the switch is set to MANUAL the state is terminated by use of the JUMP control. When the master switch is set to TEST, the state is terminated:

by use of the JUMP control or by use of the RESTART control when either of the ENTER or OBEY switches are set to 'single' or 'run', described under Test Group Controls and Indicators.

The JUMP control is a three-position switch biassed to its central position. When raised instantaneously from its central position it causes the computer to start obeying program, on level 1, at the address set on NUMBER GENERATOR keys Nos. 1–13. When lowered it causes the computer to start obeying the INITIAL INSTRUCTIONS at location 8181. The H register is cleared when this control is used.

The STOP push button allows the computer to be stopped at the completion of an instruction. The STOP lamp, incorporated in the push button, is lit when this happens and remains lit until the computer resumes operation.

The RESTART push button causes the computer to resume obeying the program at the point where it was stopped.

INTERRUPT CONTROLS: These controls comprise three illuminated push button microswitches and three associated level key switches. One push button switch and one key are associated with each of the three program levels, 1, 2 and 3.

When a key switch is down, the associated level will be set to Manual and external interrupt signals will not be recognised. When set to the up position, a permanent interrupt condition will be generated for use with the TRACE program. In the intermediate position, the switches will allow on-line operation of the computer, i.e., it will recognise external interrupt signals.

The push buttons will only be effective when the corresponding level is set to 'manual'. In this case operation of the button will generate one interrupt condition.

The upper half (red) of a push button is lit when the computer receives an interrupt demand on that level. The lower half (green) will light when the corresponding program level is in operation.

NOTE: The master switch has the following effects when in the AUTO position:

Number generator—inoperative. An input instruction which reads the number generator will place a constant (non zero) in the accumulator.

Reset
Jump
Stop
Restart } —inoperative.

Interrupt switches and push buttons—inoperative.

External interrupt signals—enabled (i.e. as normal position of switch).

Test Group Controls and Indicators

These six controls are only operative in the TEST position of the master switch: the indicators are always operative.

ENTER switch. This is a three-position switch, locking in each position, it permits a word set up on the NUMBER GENERATOR to be copied into the A register, the computer performing this operation instead of obeying an instruction.

When the switch is in the 'run' position the operation is performed continuously, once initiated by the RESTART button: when the switch is in the 'single' position the operation is performed once each time the RESTART button is operated.

OBEY switch. This is a three-position switch locking in each position: it permits a word set up on the NUMBER GENERATOR to be obeyed as an instruction by the computer. When the switch is in the 'run' position the instruction is obeyed continuously, once initiated by the RESTART button: when the switch is in the 'single 'position the operation is performed once each time the RESTART button is pressed.

STOP MODE switch. In the lowered position of this control the computer will be set to the 'Order Stop' state, in which it will obey a stored program one instruction at a time. Each successive order is initiated by operation of the 'RESTART' button.

In the raised position, the computer will be set in the 'Cycle Stop' state, in which the computer obeys successive steps in the microprogram each time 'RESTART' is operated. The 'STOP' lamp will be illuminated when the control switch is raised or lowered, remaining alight until normal operation is resumed, on selecting the centre switch position.

CYCLE REPEAT switch. When this key is set to the raised position, the computer will obey a single instruction in the microprogram repeatedly. If 'Cycle Stop' is set, repetition will occur each time the RESTART control is operated. If 'Cycle Stop' is not set, repetition occurs concontinuously.

ERROR STOP switch and lamp. This is an alternate action push button switch. When the push button is depressed and the lamp (upper half, yellow) is illuminated the processor will stop if a store parity error is detected. When the lamp is not illuminated the processor will not stop on errors.

PARITY LAMP. This is illuminated (lower half, red) when the computer stops on a store parity error.

NOTE: The master switch has the following effects when in the AUTO or MANUAL positions:

Enter
Obey
Stop Mode
Cycle Repeat
}—inoperative.

Lockout—inoperative (store protection operative).

Error Stop—inoperative. The computer will continue to run in the event of a parity error.

Monitor Facilities

These are available in any position of the master switch.

MONITOR DISPLAY switch and indicator lamp. The eighteen indicator lamps, in conjunction with the eleven position selector switch, enable the state of all central processor registers, important staticisers, and control logic waveforms to be displayed to the operator.

The waveforms available are:

Display Switch Position	Waveform Groups Displayed
1	Register Bits P1–P13, I14–17, Qo
2	Register Bits Q1–18
3	Register Bits A1–18
4	Register Bits S1–17, H staticiser
5	Register Bits J1–17, T staticiser
6	Register Bits M1–18
7	16 Control matrix steps and Timer Waveforms
8	In each position 18 control output waveforms for computation and store access
9	
10	
11	

A VOLUME CONTROL and LOUDSPEAKER are provided. The loudspeaker emits an audible indication that the computer is running, the pitch of the note is controlled by the rate at which jump instructions are obeyed by the processor.

Operation without Control and Monitor Unit

The processor will operate without the Control Unit connected, automatically obeying previously stored program, after power has been correctly applied to the system. During the period of time from the instant of switch-on until all interlocks have cleared (indicating that power has been correctly applied) a 'Reset' Signal will be applied to the processor and transmitted over the store and peripheral interfaces.

INITIAL INSTRUCTIONS

These instructions form a fixed program which is permanently available as a means of loading programs into the store using paper tape as the input medium. The instructions are brought into use by the JUMP control: when in use they occupy locations 8180 to 8191 of the store. They operate on program level 1, once a program has been loaded and a 15 7168 or 7176 instruction obeyed the locations become available for normal use. For full details see Appendix A.

PAPER TAPE INPUT

The tape reader is a photo-electric mechanism operating at 250 or 500 characters per second. It is connected to a special 8-bit interface by means of a paper tape and teleprinter control unit which contains the instruction routing and control logic.

Characters are read from the paper tape into an 8-bit buffer register. The tape input instruction causes the contents of this buffer to be transferred into the A register. Eight track tape 1 in. wide is normally used but it is also possible to use five track (0·687 in.) or seven track (0.875 in.) tape.

TELEPRINTER INPUT AND OUTPUT

General

A teleprinter, comprising keyboard, page printer, tape reader and tape punch, may be added to the standard 905 system via the paper tape and teleprinter controller. Speed of operation of the printer, reader and punch is 10 characters/second: the teleprinter can be used both for input and output, all inputs are recorded by the page printer or tape punch. The teleprinter operates on an 8-level code, details of which are given in Appendix B on page 25.

Mode of Operation

Input from the teleprinter utilizes the 15 2052 instruction: the effect of this is to shift the accumulator contents 7 places left and to logically mix the 8-bit character into the eight least significant digit positions of the accumulator.

Output to the teleprinter uses the 15 6148 instruction, this transfers the eight least significant bits of the accumulator to the teleprinter which prints and/or punches the appropriate character.

The control circuits incorporate a single 8-bit buffer, used for input and output. The buffer may at any time be empty, busy, or full.

PAPER TAPE OUTPUT

General

A paper tape punch operating at maximum speed of 110 character/second with necessary control circuits, can be added to the system via the paper tape and teleprinter controller.

Mode of Operation

Output to the tape punch utilizes the instruction 15 6144: this sends the eight least significant bits of the accumulator to the tape punch control where they are held in a buffer register until the corresponding tape row has been punched. If five or seven track tape is used then the bits corresponding to the absent tracks must be zeros.

ON-LINE PROGRAM FACILITY

Introduction

The 'On-line Program Facility' allows the tape reader, tape punch and teleprinter to be operated in either an 'on line' or 'off line' mode. The mode of operation is determined by program control. When operating in an 'off line' mode the processor is held up until the device required is ready. In the 'on line' mode, the processor will not be held up for more than 2 µs whatever the state of the device required.

An instruction is available to input a status word from the paper tape station (PTS) to determine whether the selected devices are ready. A further instruction will output a control word to put the PTS 'on line' or 'off line'. In the 'on line' mode, if a device is addressed when it is busy the characters input to the processor are undefined and any characters output (including the character which caused the device to become busy) may be corrupted or lost.

Status signals, indicating at all times the states of the selected devices, are available at outlet sockets of the PTS.

PERIPHERAL INTERFACE

General

The 905 Peripheral Interface has 59 signal lines which are:
INFORMATION OUT, 18 lines, used to transfer complete 18-bit words from the computer to the peripheral.
INFORMATION IN, 18 signal lines, used to transfer complete 18 bit words from the peripheral to the computer.
CODE, 11 signal lines, these carry the less significant binary digits of the address part of the input or output instructions. They select a peripheral and detail the operations to be performed.
SELECT, two signal lines, these specify input or output transfer and are set by the central processor as specified by bit 13 of the instruction address.
INTERRUPT, three signal lines, used by the peripheral to interrupt the computer on a priority system.
REPLY, used by the peripheral to indicate when the data lines have been served.
BLOCK TRANSFER and LAST WORD, signals from the computer associated with input/output transfers.
Miscellaneous, four signal lines.
The operation of the interface is described in outline below; further details are published separately.

Transfers

Two types of transfer are provided for:
Single word; one 18-bit word is transferred by a single instruction (Function 15, address range 0 to 6159) to or from the accumulator register.
Block transfer; a series of 18-bit words is transferred by a single instruction (Function 14, address range 2048 to 6143) to or from a series of consecutive store locations. The first store location used and the number of words to be transferred are programmed into the A and Q registers respectively prior to the block transfer instruction. The contents of Q are integers within the range 0 to 4095.

Interface Signal Lines

All interface lines carry binary signals, the states of these are described as 1 or 0 if the line carries a digit of a binary number and as true or false if the signal has a logic function.

INF. IN lines

There are 18 INF. IN lines which carry complete 18-bit words transferred from the peripheral to the accumulator by input instructions. The peripheral must place data on the INF. IN lines only when ADDRESS, in conjunction with INPUT SELECT or BLOCK TRANSFER, indicate that it is addressed by the current instruction. The INF. IN lines will be zero when the peripheral is not selected by the CODE lines, also they will be zero when the peripheral sets REPLY true when INPUT SELECT is false (i.e. for an output function).

INF. OUT lines

There are 18 INF. OUT lines, these carry complete 18-bit words transferred from the accumulator to the peripheral by output instructions. They are significant only while OUTPUT SELECT is true. Their significance at all other times is undefined.

CODE lines

There are 11 code lines, these carry bits 1 to 11 of the address part of the instruction and are used to select the peripheral device and to detail the operation to be performed.

The address lines are significant only while OUTPUT SELECT, INPUT SELECT OR BLOCK TRANSFER is true. Their significance at all other times is undefined. The central processor determines from the instruction function bits 17–14 and address bit 13 whether it is:

> an input or output instruction or a single or block transfer, and from address bit 12 whether it is a peripheral or paper tape instruction.

Using this information the central processor sets true the relevant interface signals.

INPUT SELECT

This signal is set true by the central processor when an input transfer instruction is performed. The peripheral selected by the instructions address bits 1–11 places a word on the INF. IN lines when this line is set true. Having done this the peripheral sets true the REPLY line to the central processor. INPUT SELECT is set false by the central processor when it has received REPLY true and has read the INF. IN lines. It remains false at all other times.

OUTPUT SELECT

This signal is set true by the central processor when an output transfer instruction is performed. The peripheral selected by the instruction address bits 1–11 will read the word on the INF. OUT lines and then set true the REPLY line to the central processor.

OUTPUT SELECT is set false by the central processor when it receives REPLY true. It remains false at all other times.

REPLY

This signal to the central processor is set true by the peripheral when:

> For an input transfer, the peripheral has placed a word on the INF. IN lines. The central processor will not read the INF. IN lines until REPLY is set true. For an output transfer, the peripheral has read the word on the INF. OUT lines.

In both cases the central processor will stop, with the relevant SELECT signal true, until the peripheral sets REPLY true.

REPLY is set false by the peripheral as soon as possible after the SELECT signal becomes false and remains so at all other times.

The peripheral can only set REPLY true if the ADDRESS lines indicate that it is the particular device addressed by the current instruction.

BLOCK TRANSFER

This signal is set true by the central processor to indicate the commencement of a block transfer operation. It is set true before the relevant SELECT signal is set true for the first transfer. It remains true until the end of a block transfer, i.e. until after SELECT has become false after the LAST WORD transfer.

LAST WORD

This signal is set true by the central processor when the last word of a block transfer is being transferred. It is true for the duration of the relevant SELECT signal for this transfer, and false while SELECT is true for all other transfers in the block transfer. Its significance when SELECT is false and for a single transfer is undefined.

INTERRUPTS

There are three INTERRUPT lines from the peripheral to the central processor, they are INTERRUPT 1, INTERRUPT 2, and INTERRUPT 3. One (or more) is made true when the peripheral requires the central processor to enter the program at that level (1, 2 or 3 respectively), the higher priority program being entered if more than one level of INTERRUPT is given. The relevant

INTERRUPT line must be made false before the termination of the entered program. If it is not made false the program will be re-entered.

RESET

This line from the central processor carries the logic signal RESET, which becomes true when the computer is switched on, and if operating in the AUTO mode will become false when the power supply lines are established. In MANUAL or TEST modes the line is made true on switching on or after operating the RESET control until the JUMP control is operated. The line will normally be false but will become true when switching off or if any power supply line or store temperature fault occurs. The signal may be used to reset the peripheral device to its initial state.

POWER ON

This line is energised when power is applied to the central processor logical circuitry and de-energised when power is removed.

MAINS INTERRUPT

This line is set false when the computer is switched on and will become true at least 100 μs before RESET is made true during switch off or because of mains failure. It can be linked directly to an interrupt line to enable any mains failure program to store the register contents which would otherwise be lost.

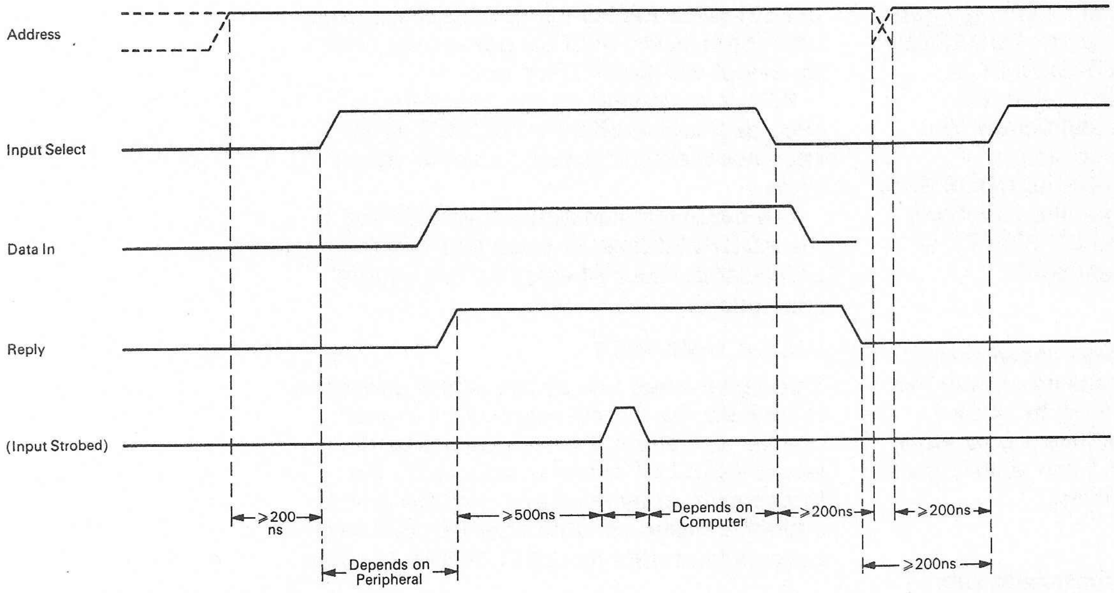
AUTO

This line is true in the 'AUTO' mode and false in the 'MANUAL' or 'TEST' modes.

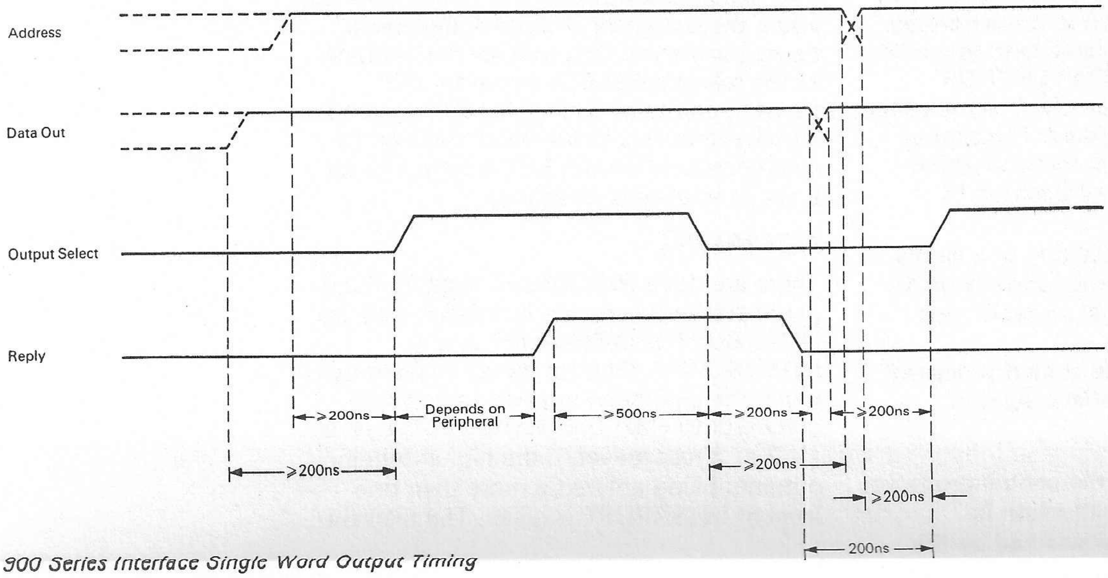
Equipment Design Timing Requirements

These timing requirements do not refer to any particular 900 series computer or peripheral, they are limiting design requirements which all 900 Series peripherals and computers must meet. In the case of synchronously operated devices, which will fail if a response is not received within a limited time, the performance of the particular computer concerned must also be considered, as a minimum data transfer rate is not specified or implied.

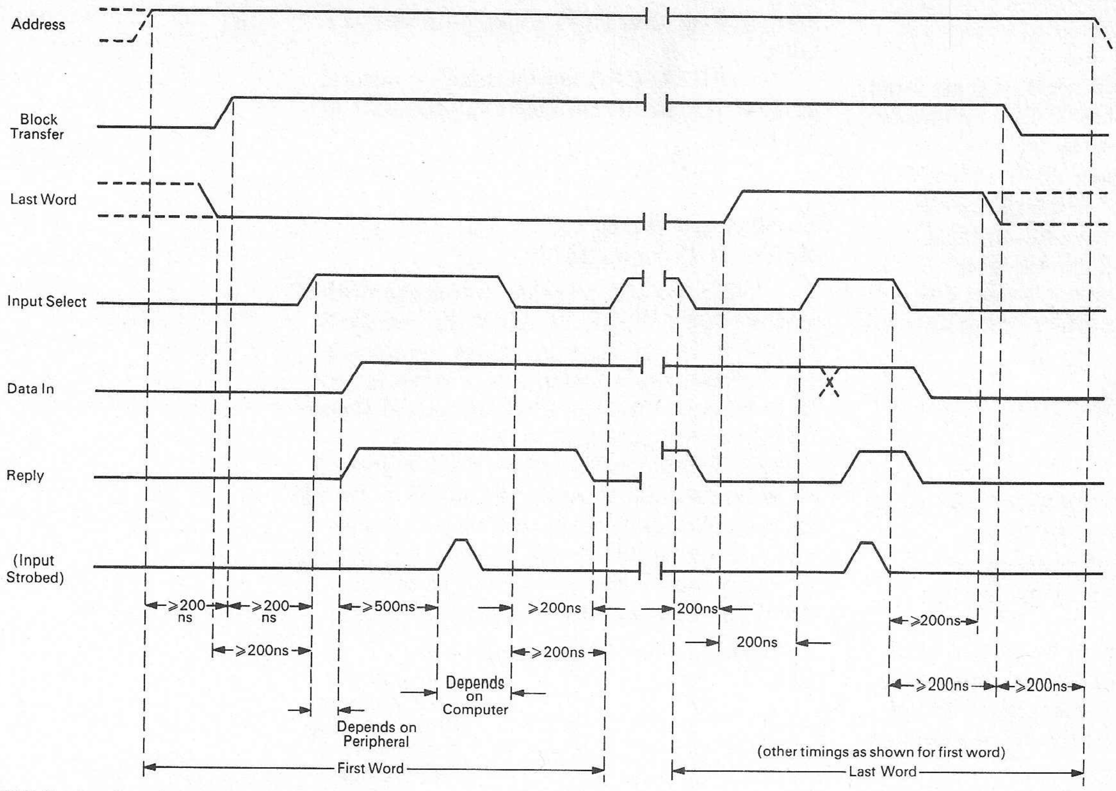
Equipment should be designed to meet these requirements and to work satisfactorily



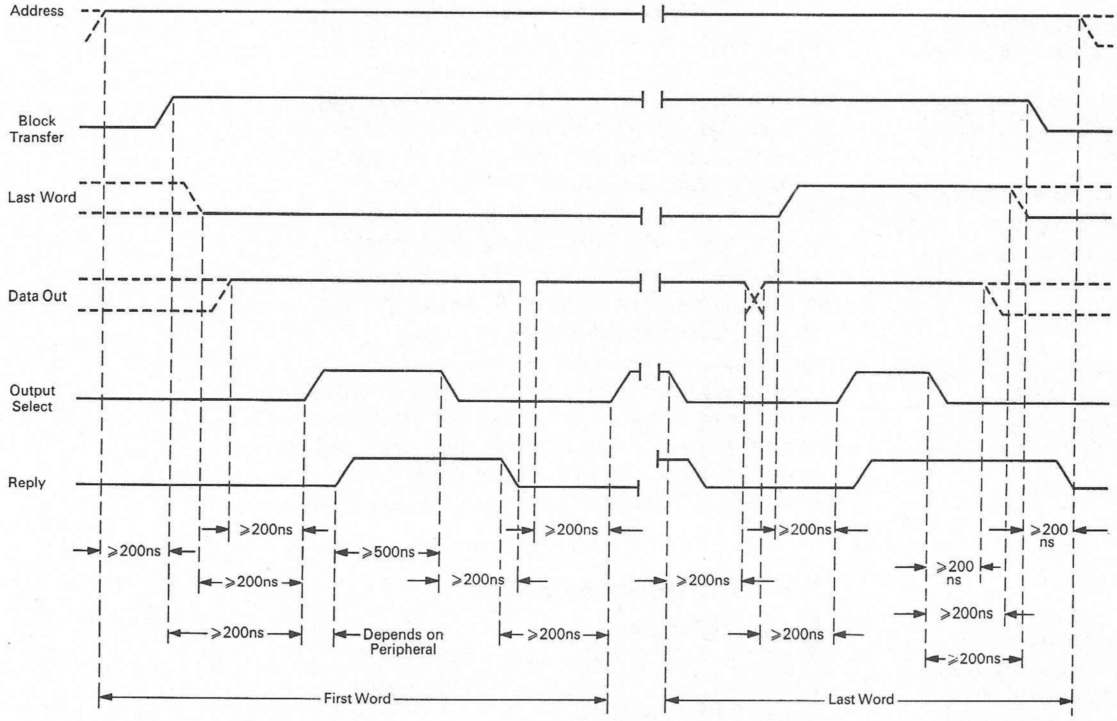
900 Series Interface Single Word Input Timing



900 Series Interface Single Word Output Timing



900 Series Interface Block Input Timing



900 Series Interface Block Output Timing

with other equipment designed to meet these requirements.

Single Word Input

Computer

The ADDRESS signals must be in the correct state at least 200 ns before INPUT SELECT is set true and must remain correct until 200 ns after INPUT SELECT has become false.

The DATA IN signals must not be assumed to be correct until at least 500 ns after REPLY becomes true: INPUT SELECT must not be set false until the DATA IN signals have been staticized within the computer.

INPUT SELECT must not be set true until at least 200 ns after REPLY has returned to FALSE.

Peripheral

REPLY must not be set true until the DATA IN signals have been set correctly. DATA IN must be set ZERO by the time REPLY is set false.

Single Word Output

Computer

The ADDRESS and DATA OUT signals must be in the correct state at least 200 ns before OUTPUT SELECT is set true and must remain correct until at least 200 ns after OUTPUT SELECT is set false again. The latter event must not occur until at least 500 ns after REPLY has become true.

OUTPUT SELECT must not be set true until at least 200 ns after REPLY has become false.

Block Input

Computer

The ADDRESS signals must be in the correct state at least 200 ns before BLOCK TRANSFER is set true and must remain correct until at least 200 ns after BLOCK TRANSFER is set false.

BLOCK TRANSFER must be true at least 200 ns before INPUT SELECT is set true for the first word and must remain true until at least 200 ns after INPUT SELECT is set false after the last word transfer.

The DATA IN signals must not be assumed to be correct until at least 500 ns after REPLY becomes true.

INPUT SELECT must not be again set true until at least 200 ns after REPLY has returned false.

The LAST WORD signal must be again set true until at least 200 ns after REPLY has returned false.

The LAST WORD signal must be correct at least 200 ns before INPUT SELECT goes true and must remain correct until at least 200 ns after INPUT SELECT becomes false again.

Peripheral

REPLY must not be set true until the DATA IN signals have been set correctly.

DATA IN lines must be set to zero not more than 200 ns after BLOCK TRANSFER has been set false.

Block Output

Computer

The ADDRESS signals must be in the correct state at least 200 ns before BLOCK TRANSFER is set true and must remain correct until at least 200 ns after BLOCK TRANSFER is set false.

OUTPUT SELECT must not be set true for the first word until at least 200 ns after BLOCK TRANSFER has been made true: BLOCK TRANSFER must not be set false until at least 200 ns after OUTPUT SELECT has been set false for the last time.

The DATA OUT lines must be correct at least 200 ns before OUTPUT SELECT is set true and must remain correct until at least 200 ns after OUTPUT SELECT has been set false again.

OUTPUT SELECT must not be set false until at least 500 ns after REPLY has become true, and must not be set true again until at least 200 ns after REPLY has returned to false.

The LAST WORD signal must be correct at least 200 ns before OUTPUT SELECT is set true.

Equipment design: Address Conventions

The following conventions in the use of the address lines should be observed. Address lines 7 to 11 are used to define the device (or in some cases the group of devices) to be selected. A unique combination of these digits (which, interpreted as a binary integer, is referred to as the 'class number') must be asigned to each peripheral. A list of class assignments for standard peripherals and recommendations is available on request. Address lines 1 and 2 are used to define the type of instruction as follows:

Operation	Address 1	Address 2	Type
OUTPUT	0	0	Data output
	1	0	Control output
	0	1	Date Terminate
INPUT	0	0	Date input
	1	0	Status input

The control output type of instruction outputs a control word (or words) to the peripheral. The control word defines the action required of a peripheral: this action may involve the transfer of data words to or from it by means of data input or data output types of instruction. The Data Terminate instruction is used to signal the end of a series of data inputs or data outputs to the peripheral if this is required. (This duplicates the effect of the 'last word' indication during block transfers). The status input type instruction is used when it is required to determine the state of a peripheral device (e.g. busy indication, error indication, etc.).

Address lines 3 to 7 are generally not used. In some circumstances it may be necessary to use these to further define the peripheral action. Preferably, this should be done by means of a control word whenever possible.

905 EXTENDED SYSTEMS

Store Extension

Both the 1·2 µs and 2 µs stores may be extended from the standard 8192 words to a total of 131 072 words.

Instructions can be placed in any locations in the store: to allow this the S register (described on page 2) contains 17 bits thus allowing instructions to be extracted automatically from locations numbered 0 to 131 071.

Since the address part of an instruction is 13 digits in length, allowing a range of 0 to 8191, additional features are necessary to allow operand addresses in a store of more than 8192 words to be defined. The actual address referred to by an instruction varies with the instruction type and the contents of the 1 bit Address Mode register (H) as follows:

In the tables the full range of operations available with extended store is listed; V is used to mean S[14–17]+N

UN-MODIFIED INSTRUCTIONS (B = 0)

(a) Inter-register transfers

Name	Operation	Other effects	Time		Instruction		Notes
			1·2 µs store	2 µs store	F	N	
A to B	B: = A		4·0	5·6	15	7174	
			3·2	4·8	5	M	Only valid when H = 1 or S[14–17] = 0
A to Aux.	Q[2–18]: = A[1–17]		3·6	4·4	15	7172	
B to Q	Q: = B	No interrupt	3·6	6·0	0	M	Only valid when H = 1 or S[14–17] = 0
S to B	B[1–13]: = S[1–13] B[14–18]: = 0	Q[14–17]: = S[14–17] Q[1–13]: = 0	3·2	4·8	11	M	
B to A	A: = B		4·0	5·6	15	7175	
			2·4	4·0	4	M	Only valid when H = 1 or S[14–17] = 0
Aux. to A	A[1–17]: = A[2–18] A [18] : = 0		3·6	4·4	15	7173	
Aux. to B	B[1–17]: = Q[2–18] B[18]: = 0		3·2	4·8	3	M	Only valid when H = 1 or S[14–17] = 0

(b) Transfers between registers and store (locations in same area as instruction)

Name	Operation	Other effects	Time		Instruction		Notes
			1·2 µs store	2 µs store	F	N	
Read	A: = V′		2·4	4·0	4	N	H = 0
Load B	B: = V′	Q: = V′ No interrupt possible after this instruction	3·6	6·0	0	N	
Load O	Q: = V′	B: = V′ (No interrupt possible)	3·6	6·0	0	N	
		(Or A: = V′−A)	3·2	4·8	2	N	
Write	V′: = A		3·2	4·8	5	N	
Store S	V′[1–13]: = S[1–13] V[14–17]: = 0	Q[14–17]: = S [14–17]	3·2	4·8	11	N	
Store Aux.	V′[1–17]: = Q[2–18] V′[18]: = 0		3·2	4·8	3	N	

(c) Transfers between registers and store (locations 0–8191)

Name	Operation	Other effects	Time		Instruction		Notes
			1·2 µs store	2 µs store	F	N	
Read	A: = N′		2·4	4·4	4	N	H = 1 or S[14–17] = 0
Load B	B: = N′	Q: = N′ (No interrupt after this instruction	3·6	6·6	0	N	
Load Q	Q: = N′	B: = N′ No interrupt after this instruction OR	3·6	6·6	0	N	
		A: = N′−A	3·4	4·8	2	N	
Write	N′: = A		3·4	4·8	5	N	
Store	N′[1–13]: = S[1–13] N′[14–17]: = 0	Q[14–17]: = S[14–17]	3·4	4·8	11	N	
Store Aux.	N′[1–17]: = Q[2–18] N′[18]: = 0		3·4	4·8	3	N	

(d) Arithmetic between Accumulator and B register

Name	Operation	Other effects	Time		Instruction		Notes
			1·2 µs store	2 µs store	F	N	
Add A to B	A: = A+B		2·4	4·0	1	M	H = 1 or S[14–17] = 0
Subtract A from B	A: = B−A	Q: = B	3·2	4·8	2	M	
Multiply A by B	AQ: = A×B	Q[1] altered	9·1	11·2	12	M	
Divide by B	A: = AQ÷B	Q: = AQ÷B	18·0	20·2	13	M	
Collate A with B	A: = A and B		2·4	4·0	6	M	

(e) Arithmetic between Accumulator and store (locations in same area instruction)

Name	*Operation*	*Other effects*	*Time* *1·2 μs store*	 *2 μs store*	*Instruction* *F*	 *N*	*Notes*
Add	A: = A+V′		2·4	4·0	1	N	H = 0
Negate and Add	A: = V′−A	Q: = V′	3·2	4·8	2	N	
Multiply	AQ: = A×V′	Q[1] altered	9·1	11·2	12	N	
Divide	A: = AQ÷V′	Q: = AQ÷V′	18·0	20·2	13	N	
Collate	A: = A and V′		2·4	4·0	6	N	

(f) Arithmetic between Accumulator and store (locations 0 to 8191)

Name	*Operation*	*Other effects*	*Time* *1·2 μs store*	 *2 μs store*	*Instruction* *F*	 *N*	*Notes*
Add	A: = A+N′		2·4	4·4	1	N	H = 1 or S[14–17] = 0
Negate and Add	A: = N′−A	Q: = N′	3·2	5·3	2	N	
Multiply	AQ: = A×N′	Q[1] altered	9·6	11·2	12	N	
Divide	A: = AQ−N′	Q = AQ÷N′	18·0	20·2	13	N	
Collate	A: = A and N′		2·4	4·0	6	N	

(g) Transfer Control

Name	*Operation*	*Other effects*	*Time* *1·2 μs store*	 *2 μs store*	*Instruction* *F*	 *N*	*Notes*
Jump zero	if A = 0 then S: = V		1·2	2·0	7	N	
Jump	S: = V		1·2	2·0	8	N	
Jump negative	if A < 0 then S: = V		1·2	2·0	9	N	
Count and Test	B: = B+1		5·3	8·4	15	7170	
	if B[1–13] = 0 then						
	S: = S+2		6·2	9·2			
Test standard	if A ⩾ +½ or A < −½		2·8	3·6	15	7169	
	or A = 0 then S = S+2		3·6	6·4			

(h) Miscellaneous

Name	*Operation*	*Other effects*	*Time* *1·2 μs store*	 *2 μs store*	*Instruction* *F*	 *N*	*Notes*
Count in B	B: = B+1		3·6	6·0	10	M	H = 1 or S[14–17] = 0
Count in store	N′: = N′+2^{-17}		3·6	6·0	10	N	H = 1 or S[14–17] = 0
Count in store	V′: = V′+2^{-17}		3·6	6·0	10	N	H = 0
Shift left	AQ: = AQ×2^{N}		2·8+0·8n	3·6+0·8n	14	0 to 36	
Shift right	AQ: = AQ×2^{N-8192}		2·8+0·8n	3·6+0·8n	14	8156 to 8191	i.e. shift right 8192–N (= n) places
Terminate	Current program level terminated		7·2	10·4	15	7168	
Set relative	H: = 0		3·6	4·4	15	7176	
Set absolute	H: = 1		3·6	4·4	15	7177	

(i) Input and output

Name	Operation	Other effects	Time 1·2µs store	Time 2µs store	Instruction F	Instruction N	Notes
Key input	A: = word generator		3·6	4·4	15	7171	
Tape input	A [9–18]: = A [2–11] A [8]: = A [1] or character [8] A[1–7]: = character [1–7]		5·2 (min)	6·0 (min)	15	2048	Acc shifted left 7 places and 8 bit character. logically mixed in
Teleprinter Input	A[9–18]: = A[2–11] A[8]: = A[1] or character [8] A[1–7]: = character [1–7]		5·2 (min.)	6·0 (min)	15	2052	do. Input from tape reader when teleprinter not fitted
Word input	A: = input word		5·2 (min.)	6·0 (min)	15	0 to 2047	Input device and action selected externally by N[1–11]
Block input	A′: = 1st input word (A+1)′: = 2nd input word etc. (A+Q[1–12]–1)′: = last word input	A,Q altered	4·4+5·2 n (min.)	5·2+6·0 n (min)	14	2048 to 4095	Input device and action selected externally by N[1–11] No. of words input = Q[1–12] (= n)
Tape output	Character: = A[1–8]		5·2 (min.)	6·0 (min)	15	6144	
Teleprinter Output	Character: = A[1–8]		5·2 (min.)	6·0 (min)	15	6148	
Word output	Output word: = A		5·2 (min.)	6·0 (min)	15	4096 to 6143	Output device and action selected externally by N[1–11]
Block output	1st output word: = A′ 2nd output word: = (A+1′) etc. Last output word: = (A+Q[1–12]–1)′	A,Q altered	4·4+5·2 n (min.)	4·2+6·0 n (min)	14	4096	do. No. of words output = Q[1–12]

MODIFIED INSTRUCTIONS (B=1)

Modified instructions are not limited in respect of the store locations referred to. The modifier needed to refer to a particular location varies with the contents of H.

NOTE: X is used to mean B+N
Y is used to mean B+S[14–17]+N

Name	Operation	Other effects	Time 1·2 µs store	Time 2 µs store	Instruction F	Instruction N	Notes
Read	A: = X′	Q altered	3·6	6·0	4	N	H = 1 or S[14–17] = 0
	A: = Y′	Q altered	3·6	6·0	4	N	H = 0
Load B	B: = X′	Q: = X′	4·8	8·0	0	N	H = 1 or S[14–17] = 0
	B: = Y′	Q: = Y′	4·8	8·0	0	N	H = 0
Load Q	Q: = X′	B: = X′	4·8	8·0	0	N	H = 1 or S[14–17] = 0
		A: = X′–A	4·4	6·8	2	N	
	Q: = Y′	B: = Y′	4·8	8·0	0	N	H = 0
		A: = Y′–A	4·4	6·8	2	N	
Write	X′: = A	Q altered	4·4	6·8	5	N	H = 1 or S[14–17] = 0
	Y′: = A	Q altered	4·4	6·8	5	N	H = 0
Store S	X′: = S[1–13]	Q: = S[14–17]	4·4	6·8	11	N	H = 1 or S[14–17] = 0
	Y′: = S[1–13]	Q: = S[14–17]	4·4	6·8	11	N	H = 0

(b) Arithmetic between accumulator and store

Name	Operation	Other effects	Time 1·2 µs store	Time 2 µs store	Instruction F	Instruction N	Notes
Add	A: = A+X′	Q altered	3·6	6·0	1	N	H = 1 or S[14–17] = 0
	A: = A+Y′	Q altered	3·6	6·0	1	N	H = 0
Negate and add	A: = X′–A	Q: = X′	4·4	6·8	2	N	H = 1 or S[14–17] = 0
	A: = Y′–A	Q: = Y,	4·4	6·8	2	N	H = 0
Multiply	AQ: = A×X′	—	10·8	13·2	12	N	H = 1 or S[14–17] = 0
	AQ: = A×Y′	—	10·8	13·2	12	N	H = 0
Collate	A: = A and X′	Q altered	3·6	6·0	6	N	H = 1 or S[14–17] = 0
	A: = A and Y′	Q altered	3·6	6·0	6	N	H = 0

(c) Transfer Control

Name	*Operation*	*Other effects*	*Time* *1·2 µs store*	 *2 µs store*	*Instruction* *F*	 *N*
Jump zero	if A = 0 then S: = Y	Q altered	1·2 (A ≠ 0) 2·4 (A = 0)	2·0 (A ≠ 0) 4·0 (A = 0)	7	N
Jump	S: = Y	Q altered	2·4	4·0	8	N
Jump negative	if A < 0 then S: = Y	Q altered	1·2 (A ⩾ 0) 2·4 (A < 0)	2·0 (A ⩾ 0) 4·0 (A < 0)	9	N

(d) Miscellaneous

Name	*Operation*	*Other effects*	*Time* *1·2 µs store*	 *2 µs store*	*Instruction* *F*	 *N*	*Notes*
Count in store	X′: = X′+2^{-17}	Q altered	4·8	8·0	10	N	
Word input	A: = input word	Q altered	6·4 (min.)	8·0 (min.)	15	N	X in range 0–2047 device and action selected by X[1–11]
Word output	Output word: = A	Q altered	6·4 (min.)	8·0 (min.)	15	N	X in range 4096–6143, device and action selected by X[1–11]

Instruction type	Store Address (unmodified) H = 0	 H = 1
Transfers between registers and store	S[14–17]+N	N
Arithmetic between registers and store		
Count in store		
Transfer control	S[14–17]+N	S[14–17]+N

The above can be summarised by saying that when H = 0 the N digits of an instruction specify the address of a location in the same unit as the instruction itself and when H = 1 the N digits specify an address in the first 8192 words (locations 0–8191) except for jump instructions which are as for H = 0. In the case of modified instructions, the effect of modification is to add the B register contents to the address defined above: since the B register contains 18 bits a full-length address can always be generated and thus a modified instruction can always address any location in the store. Functions 14 and 15, when N does not define a store location, are not affected by the contents of H and only the 13 least significant bits of a modified address are meaningful.

Program Compatibility

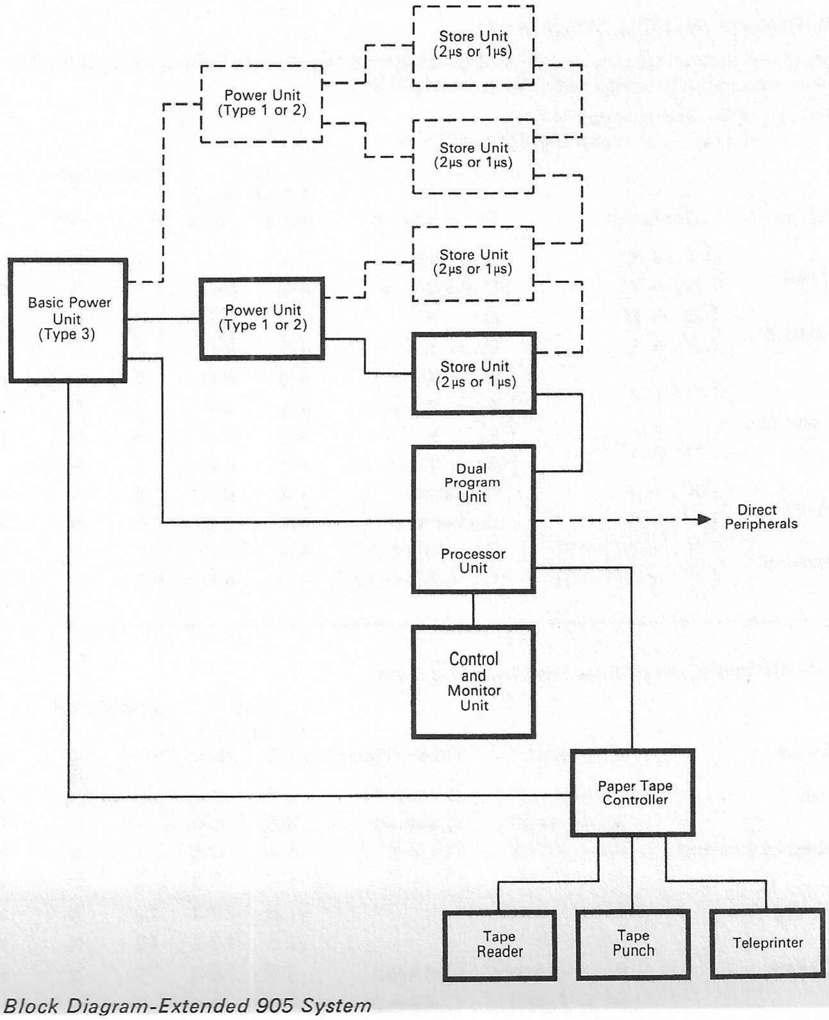
The 905 with extended store can accept all programs written for 903 computers with extended store if the H register contents are zero. For convenience of operating such programs the H register is automtically cleared when the Jump control is used. The appropriate version of the Symbolic Input Routine (SIR) and the ALGOL and FORTRAN compilers may thus be used.

MULTIPLEX INTERRUPT UNIT

The MIU allows up to seven peripheral devices to be multiplexed on to the direct interface outlet of the 905 and provides facilities for accepting and controlling up to 12 interrupt sources, grouped on to one program level, originating from the multiplexed peripherals or other external devices.

Peripheral Multiplexing

The unit is connected to the 905 direct interface outlet and provides up to seven outlets for the connection of peripherals. These outlets are in effect replicas of the processor direct outlet as regards signalling system, signal levels and physical details so



Block Diagram-Extended 905 System

that any peripheral may be used either on its own, connected directly to the processor or, in conjunction with others, connected via the MIU.

Interface Details

The signals available on each peripheral outlet are listed below, together with the corresponding signals of the processor interface.

Signals from the processor to peripherals are simply repeated by the MIU on each outlet where specified. Signals from peripherals (except interrupts and readies) are 'OR-ed' together in the MIU and the resulting signal transmitted to the processor. The design requirements for peripheral signals are as stated for the processor interface described on page 8.

Central Processor	MIU	
	Outlet A	Outlets B–G
Data in 1–18	Date in 1–18	Date in 1–18
Date out 1–18	Date out 1–18	Data out 1–18
Address 1–2	Address 1–2	Address 1–2
Address 3–6	Address 3–6	—
Address 7–11	Address 7–11	Address 7–11
Input select	Input select	Input select
Output select	Output select	Output select
Reply	Reply	Reply
Block transfer	Block transfer	Block transfer B
Last word	Last word	Last word
Interrupt 1	Ready X	Ready X
Interrupt 2	Ready Y	Ready Y
Interrupt 3	Ready Z	Ready Z
Reset	Reset	Reset
Power on	Power on	Power on
Auto	Auto	—
Mains failure	Mains failure	—

Interrupt Facilities

The MIU contains facilities to allow up to 12 ready signals to be grouped via a 'masking' register, through an OR gate onto one of the central processor interrupts. In addition a further seven ready signals may be grouped through another OR gate onto a central processor interrupt line.

The mask register, on the first group of 12 ready lines, can be set by program to inhibit or enable any of the individual ready lines, and facilities are included to enable the program to determine the source of interrupt.

The program facilities take the form of the following instructions:

Function	*Instruction*	
Read states of ready lines 1–12 into corresponding bits of the Accumulator (1 = ready, 0 = not ready;	15	64
Place number of highest priority signal causing interrupt into Accumulator. (Note: Priorities are assigned in numerical order, No. 1 having the highest priority and No. 12 the lowest. If no signals are present the Accumulator is cleared.	15	65
Set bits of mask register to the 'one' state (i.e. allow interrupts from corresponding signals) if corresponding bits of Accumulator are 'ones'.	15	4360
Set bits of mask register to the 'zero' state (i.e. inhibit interrupts from corresponding signals) if corresponding bits of Accumulator are 'ones'.	15	4161

Note that bits of the mask register in positions corresponding to zeros in the accumulator are not altered by the 15 4160 or 4161 instructions. The mask register is cleared when the computer is reset.

A program interrupt signal will be sent to the processor as a result of a signal on any of the 12 lines, provided that the corresponding mask register bit is set to 'one'. Use of the 15 65 instruction allows the processor to determine directly the source of the signal: signals which are 'masked off' do not affect the number read by this instruction. The 15 64 instruction, however, reads the actual state of all signals, irrespective of the mask register contents. For systems using two MIU's the above instruction addresses are increased by two for control of the second unit.

Patching Facility

The interrupt signals to the processor and the ready signals from the peripheral outlets, are all grouped on an additional connector: this enables the allocation of levels and priorities to be 'patched if necessary, and additional external signals connected where desired. The signals available on the connector and the standard connections are as follows:

From	To
Ready X Outlet A	Interrupt 1—Processor
Ready X Outlets B–C	
Ready Y Outlet A	
Ready Y Outlet B	
Ready Y Outlet C	OR inputs
Ready Y Outlet D	
Ready Y Outlet E	
Ready Y Outlet F	
Ready Y Outlet G	
OR output	Interrupt 2—Processor
Ready Z Outlet A	Interrupt extension, signal 4
Ready Z Outlet B	Interrupt extension, signal 5
Ready Z Outlet C	Interrupt extension, signal 6
Ready Z Outlet D	Interrupt extension, signal 7
Ready Z Outlet E	Interrupt extension, signal 8
Ready Z Outlet F	Interrupt extension, signal 9
Ready Z Outlet G	Interrupt extension, signal 10
Interrupt extension output	Interrupt 3—processor
Mains failure—processor	—
—	Interrupt extension, signal 1
—	Interrupt extension, signal 2
—	Interrupt extension, signal 3
—	Interrupt extension, signal 11
—	Interrupt extension, signal 12

AUTONOMOUS TRANSFER UNIT

General

The A.T.U. permits up to 6 peripherals to transfer words autonomously to and from the store. Connections between the peripherals and the A.T.U. use the 900 Series Autonomous Interface (which is similar to the 900 Series Peripheral Interface). An A.T.U.is connected to the Computer Store Highway and to Direct Input-Output Interface of the Computer. Up to four A.T.U.'s can be connected to one computer allowing the connection of up to 24 automonous peripherals. A direct channel is also available from the A.T.U. for connection of a direct peripheral.

The unit has hardware address register, counter register and output data register for each peripheral channel, thus allowing transfers to proceed simultaneously on all channels. Interleaving taking place on the store bus by a 'cycle stealing' mechanism.

Sequence of Operations

A sequence of transfers to and from a peripheral is initiated by an instruction obeyed by the processor. Thereafter the sequence proceeds autonomously (unless a terminate sequence instruction is obeyed), until all transfers specified have been completed. If the peripheral is then ready for a new sequence of transfers the A.T.U. may interrupt the processor.

The sequence can consist of any or all of the following:

(a) 0 to 3 control word transfers to peripheral.
(b) 0 to 4095 data word transfers to or from peripheral.
(c) A status word transfer from peripheral.

Channel Priorities

At the end of each store cycle the peripheral channel signals are examined and the peripheral having the highest priority (i.e. connected to the lowest numbered channel) is serviced. In this way transfers on each channel may be interleaved.

Store Locations

Each peripheral attached to the A.T.U. has associated with it four locations in the store; the contents of these are used in the sequence of transfers as detailed below. The actual locations assigned to each peripheral are defined below.

Location	*Bits*	*Function*
P	1–17	Data Pointer
	18	Output Indicator
P+1	1–12	Data Count
	15	Cyclic Indicator
	13–14	Control Count
	16	Status Word Indicator
	17–18	(spare)
P+2	1–17	Control Pointer
P+3	1–18	Status Word

The hardware count and address registers are automatically loaded from store when a sequence is initiated; the count register is loaded from location P+1 and the address register from location P+2. At the start of the data transfer part of the sequence the address register is loaded automatically from location P. (If no control outputs are required the address register is loaded from P when the transfer is initiated.)

Cyclic Operation

At the end of data transfer if bit 15 of the count register is a 1 the address and count registers are automatically reloaded from locations P+1 and P, and the data transfer part of the sequence thus repeated. The loop is broken when the peripheral raises CONTROL READY in place of DATA READY thus causing a termination. Note however that if zero Data words are specitied in this mode then the cyclic Indicator and the Status Word Indicator are treated as if they were zero.

Control of Transfers

Control Word Transfers take place from store locations whose addresses are given by the contents of the address register, this register is incremented each time a control word is transferred so that words may be transferred from consecutive store locations. The number of control word transfers in a sequence is controlled by bits 13 and 14 of location P+1 ; these bits represent a count of the number of control words to be transferred as follows:

Bits 14	*Bit 13*	*No. of transfers*
1	1	3
1	0	2
0	1	1
0	0	0

During the last word of a control word transfer LAST WORD is not sent to the peripheral.

Data Transfers take place to or from locations whose addresses are given by the contents of the address register. This register is incremented each time a data word is transferred so that words are transferred to or from consecutive store locations. Bit 18 of location P is a one to indicte output and a zero to indicate input. The number of data words transferred is controlled by bits 1–12 of location P+1 ; if the number represented by these bits is X the number of words to be transferred is X. The count register is decremented each time a data word is transferred. When the count register=0 no further data transfers take place.

During the last word of a data transfer a Last Word Signal is sent to the peripheral to indicate the end of the sequence.

A Status word input takes place if bit 16 of location P+1 is a one; the status word is placed in location P+3.

Program Control

As previously mentioned, each peripheral may cause an interrupt if it is ready for a new sequence. These interrupts are connected to an interrupt 'patch' connector so that they may be linked to interrupt extension inputs. These inputs are connected together to produce an interrupt, normally on level 3. Instructions are provided to enable or inhibit interrupts on the interrupt extension inputs by means of a mask register and to determine which channel originated the interrupt. The Interrupt is cancelled by an Initiate Sequence instruction.

Instructions

15 5279+N Initiate sequence on channel N (N = 1 to 6)

15 5311+N Terminate sequence on channel N (N = 1 to 6)

15 5248 Allow interrupts on interrupt extension inputs as indicated by ones in Accumulator bits 1–12.

15 5249 Prohibit interrupts on interrupt extension inputs as indicated by ones in Accumulator bits 1–12.

15 1152 Place status of interrupt extension inputs into bits 1–12 of Accumulator.

15 1153 Place into Accumulator bits 1–4 identification number of interrupt extension input causing interrupt. If more than one source of interrupt is simultaneously present the source connected via the patching connector to the lowest interrupt extension is indicated, the Accumulator is cleared if no interrupts are present.

15 1183+N Place Address Register of channel N (N=1–6) into the accumulator, including output indicator.

15 1215+N Place Count Register of channel N (N = 1–6) into the accumulator, including status and cyclic indicators.

15 1157–59 Undefined.

15 5252–55 Undefined.

The mask register is cleared (i.e. all interrupts are inhibited) when the computer is reset.

On completion of a data transfer sequence the contents of the channel address register point to the next free store location thus –

$A=A_i+T$ where A_i = start address specified and T equals number of transfers that have taken place.

Also the content of the count register shows $K_i - T$ where K_i is the number of transfers specified initially and T is the number of transfers actually occurring. Thus the count register is zero when a transfer is completed normally. Note that on a premature termination T includes the data word transferred in response to the termination control ready.

When the Terminate Sequence instruction is obeyed it immediately stops transfers of any type on the specified channel, by issuing a RESET for that particular channel.

When more than one A.T.U. is used the interrupt signal from the second is treated as an external signal for the first, and so on for subsequent units. Instructions referring to the second, third and fourth A.T.U.'s have 8, 16 and 24 respectively added to all the above addresses.

Store Locations

	Channel No.					
	1	2	3	4	5	6
Data pointer	32	36	40	44	48	52
Indicators	33	37	41	45	49	53
Control pointer	34	38	42	46	50	54
Status word	35	39	43	47	51	55

For the second, third and fourth A.T.U.'s 32, 64 and 96 respectively are added to the above addresses.

Interfaces and Connections

A.T.U. to Peripheral Interface

The Interface lines provided are listed below together with the equivalent 900 Series Direct Interface lines.

Autonomous Interface	*Direct Interface*
Data in 1–18	Data in 1–18
Data out 1–18	Data out 1–18
Address 1	Address 1–2
—	Addresses 3–7
	Addresses 8–11
Input select	Input select
Output select	Output select
Reply	Reply
—	Block transfer
Last Word	Last word
—	Interrupt 1
Data ready	Interrupt 2
Control ready (use optional)	Interrupt 3
Reset	Reset
Power On	Power On
—	Auto
—	Mains failure
Mask	—

Since each channel is separately controlled the Autonomous Interface signals are unique to each channel (e.g. during input on a channel it does not matter what is occurring on the other channel input lines).

The 'ready' lines are used by each peripheral to initiate a transfer. 'Data ready' initiates either a transfer of a Data word or of a control word. 'Control ready' can only initiate a status input or control output transfer. If 'Control ready' is made true during a data input or output sequence when a 'Data ready' is expected it causes premature termination of the sequence, by remaining true until the next Status Word Input or Control Output transfer when it is reset. When this occurs the next transfer is a Data Word followed by a Status Word Input (if the Status Word Indicator is true). The one bit cyclic indicator register is also cleared. Note that if zero control words are specified for a transfer sequence initiated when 'Control ready' is true, one Data Word will be output before termination occurs.

The mask line is intended to inform the peripheral that it is connected to an Autonomous Interface and not the Direct Interface. Address bits 2–11 are always zero on an A.T.U. interface. Address bit 1 denotes Data Input or Output if false and Control Output or status Input if true.

Interface Timing
Control Output
If the next transfer on a particular channel is a control output, the 'control ready' and the 'data ready' signals are examined at the end of the store cycle. If either 'ready' is true and the channel has highest priority (i.e. is the lowest numbered channel) the next store cycle is assigned to that channel. When information is available, from the store, it is loaded into the data register (one for each channel), and 'output select' is made true. Thereafter the peripheral responds by making 'reply' true and then false when 'output select' returns false.

Data Output
If the next transfer on a particular channel is a data output, the sequence is similar to that for control output above except that only 'Data ready' can initiate the sequence.

Data Input
If the next transfer on a particular channel is a data input, 'input select' is made true when 'data ready' is made true. When the peripheral responds with 'reply' the next store cycle is assigned to that peripheral (provided it has highest priority). At the end of the store cycle 'input select' is made false hence the peripheral makes 'reply' false.

Termination
When the data word count is zero the A.T.U. inputs device status if status word indicator is true. In this case 'input select' is made true when either 'control ready' or 'data ready' is made true, and the sequence proceeds as for Data Input above.

If the Status Word Indicator is false or when Status has been input the A.T.U. waits for the next 'ready', either 'Data or Control' and passes this onto the processor as an Interrupt, via the Interrupt 'Patching' connector.

Note: If 'Control ready' is made true when a 'data ready' is expected during a data transfer sequence the termination sequence is entered after transferring one more data word regardless of the data word count.

The 'data ready' signal is ignored when 'input select' or 'output select' is made true until 'reply' is made false, hence the 'data ready' signal should have been made false before reply is made false if the peripheral is not immediately ready for another transfer. The 'Control ready' signal should always be made false before 'reply' is made false, unless it is to terminate a data transfer sequence when it must remain true until the next Status Word Input or Control Word Output. It is then reset before that reply is made false. When software termination of sequence occurs by a 15 5311+N instruction RESET is made true for channel N only.

Sockets A and B
The central processor to A.T.U. peripheral interface is regenerated and connected to SKTA and SKTB. SKTA contains all the direct peripheral signals listed above whilst SKTB only contains:

Output Select
Address 1 and 7–11
Data Out 1 and 2
Power On
Reply
Ready Y
Reset
Mains failure

SKTB is intended for the control of devices connected directly on the store bus (i.e. disc and drum controllers).

Interrupt 'patching' connector
The individual interrupts (generated by either 'ready' signal at the start of a new sequence) are grouped on an additional connector; this enables the allocation of levels and priorities to be 'patched' if necessary, and additional external signals connected where desired. The signals available on the connector and the standard connections are as follows:

One of the select A.T.U. lines are linked to 0v if the A.T.U. is the second, third or fourth A.T.U. respectively.

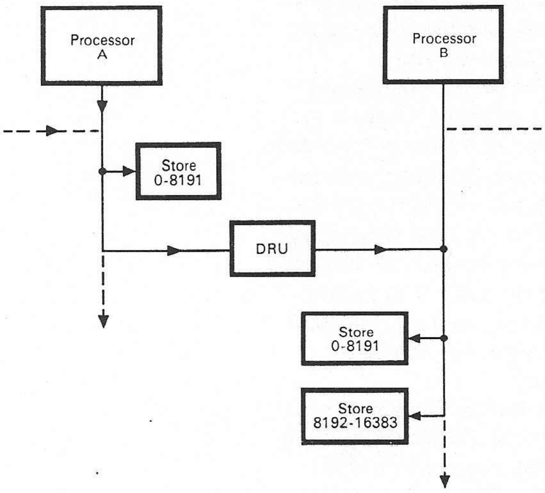
From	To
Mains Failure – Processor	—
Interrupt Channel 1	Interrupt Extension I/P 4
Interrupt Channel 2	Interrupt Extension I/P 5
Interrupt Channel 3	Interrupt Extension I/P 6
Interrupt Channel 4	Interrupt Extension I/P 7
Interrupt Channel 5	Interrupt Extension I/P 8
Interrupt Channel 6	Interrupt Extension I/P 9
Ready Y (skt B)	Interrupt Extension I/P 10
—	Interrupt Extension I/P 11
—	Interrupt Extension I/P 1
—	Interrupt Extension I/P 2
—	Interrupt Extension I/P 3
Interrupt 3 from other units	Interrupt Extension I/P 12
Interrupt Extension Output	Interrupt 3 – to processor
Interrupt 1 from other units	Interrupt 1 – to processor
Interrupt 2 from other units	Interrupt 2 – to processor
Ov	—
—	Select A.T.U. No. 2
—	Select A.T.U. No. 3
—	Select A.T.U. No. 4

If any interrupt extension input is made one, a one will be generated on the interrupt extension output provided that the corresponding bit of the mask register has been set.

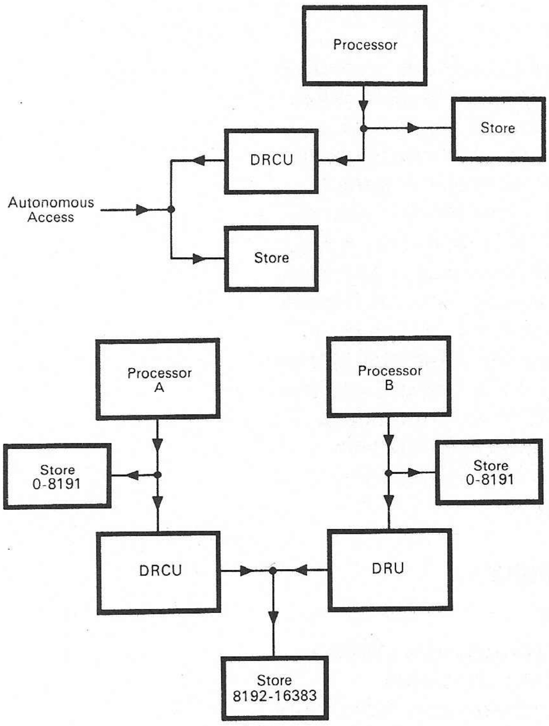
It should be noted that when the A.T.U. channel 'readys' are examined for priority at the end of each store cycle channel 1 still has the greatest priority, no matter what connections are made on the patching connector, the connection only affects the priority of interrupt sources in the 15 1153 instruction.

System Configuration

The block diagram shows the connection of the A.T.U. into a 905 system. It will be seen that a direct interface extension socket is provided to avoid the use of a multiplexer when another A.T.U. or other direct device is attached. This socket is identical to a 900 Direct Interface socket except that the 'interrupt 3' signal is routed to the interrupt patching connector and is normally connected as an external interrupt signal.



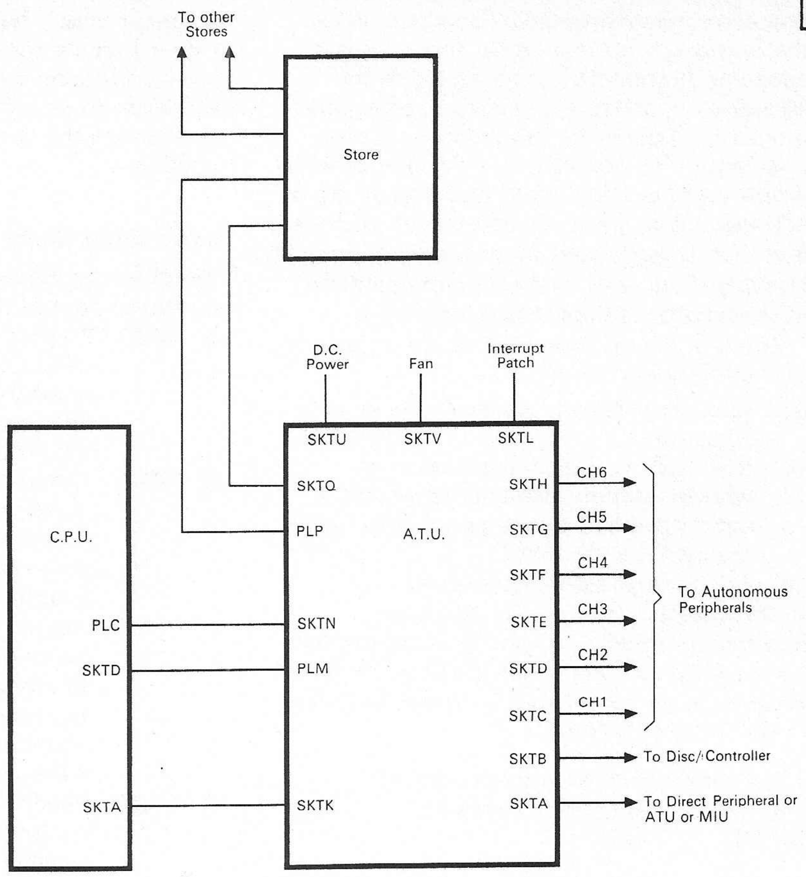
905 Inter-Computer Connections



905 Inter-Computer Connections

Performance

The maximum speed of transfer is 1·2 to 2·2 μsec plus the peripheral response time. On low priority channels these times are increased by the delay caused by higher priority channel operation. For 2 μsec the maximum speed is 2 μsec to 3 μsec. The A.T.U. can be supplied in 2 or 6 channel versions.



Block Diagram-905 System with A.T.U.

DUAL PROGRAM UNIT

Introduction

The Dual Program Unit is intended to allow the computer to be time-shared between one program which is fully checked out, and a second program which is under development, without affecting the integrity of the first program. The unit allows a 'normal' mode of operation, and the operation of the dual program unit makes it impossible for this program to corrupt or hold up the first program. The normal program mode will in practice include an executive routine and one or more fully tested programs, which may be used for on-line control or off-line computing.

The slave mode will normally be used for development of one program, which may be in any stage of development from initial testing to long-term trials. The development program cannot overwrite the store used by 'normal' mode programs, or complete any input-output operations. Any attempt to do so will cause transfer to the executive routines which must take the appropriate action.

The development program may work off-line or on-line, providing that the executive program contains input/output routines for the appropriate peripherals. The developing program will normally arrange input/output by means of standard sub-routines or procedures, which hand over information to and from the executive.

Functional Specification

A one-bit memory within the unit controls the mode of operation. When this memory is set to normal mode all operations of the processor are as specified elsewhere. When the unit is set to slave mode, this causes a constant quantity (L) to be added to the addresses of all store locations used by the processor (but not by autonomous access channels). The constant is a multiple of 4096 words and the effect of adding it to all store addresses is to render locations with addresses less than L completely inaccessible to program Location 0 as used by a program operating in slave mode is thus in fact location L.

The unit reverts to normal mode when any of the following occur:

(a) A location outside the available store is addressed.

(b) Any input or output instruction is obeyed: in this case the instruction is not transmitted to any peripherals but is 'trapped' by the DPU.

(c) An interrupt signal is received.

In the cases of (a) and (b) above an interrupt (normally on level 3) is generated by the DPU: details of the occurrences are retained in an 18-bit status register included in the DPU as follows:

Location outside the available store:

Bits 1–17:	Address of location
Bit 18:	'One'

Input or output instruction

Bits 1–4:	Bits 1 to 4 of instruction address
Bits 5–11:	Bits 5–11 of instruction address, if general input-output instruction, Zero if paper tape instruction.
Bit 14:	'One' if general input instruction.
Bit 15:	'One' if paper tape input instruction.
Bit 16:	'One' if general output instruction.
Bit 17:	'One' if paper tape output instruction.
Bit 18:	'Zero'.

The interrupt generated in these circumstances will normally take place immediately following the instruction which caused it (unless it is a function O instruction following which interrupt cannot occur).

The effects of references outside the available store are as follows:

(a) Extraction of instruction—the instruction 14 0 will be obeyed (shift no places = do nothing).

(b) Extraction of operand—the pseudo-instruction 14 0 will be used as an operand.

(c) Storage of result—no effect on any store location, effects on registers as as normal.

Occurrence of an external interrupt signal is indicated by the DPU status register being clear. When slave mode is in operation the operation of the processor is also altered in respect of block transfer instructions and interrupts after function 0 instructions. Any block transfer instruction obeyed during slave mode has no effect, it is treated as a 14 0 instruction by the processor. An interrupt can occur after a function 0 instruction in slave mode if the succeeding instruction is also a function 0 instruction but not otherwise. At any interrupt before a function 0 instruction the Q register contents are undefined.

Instruction Code

The following input-output instructions will be used to control the DPU.

15 6020 Prepare slave mode. Causes the DPU to switch to slave mode operation when program level 4 next becomes active, also clears the DPU status register.

15 6021 Interrupt on level 3 and cancel slave mode. May be obeyed in slave mode to cause normal mode to be resumed (to allow a slave program to return control to the normal mode on level 4 to cause an interrupt to level 3. It may also be obeyed on level 3 to cancel the effect of a previous 16 6020 instruction (i.e. to 'unprime' slave mode.).

15 1924 Read DPU status. Causes the contents of the DPU status register to be copied into the accumulator. The contents of the register are not altered.

Program Levels

It is implied above that slave mode operation can only occur when program level 4 (base level) is active. When any of levels 1, 2 or 3 become active as a result of interrupts normal mode operation is automatically resumed. When level 4 is active, slave mode operation will occur only if a 15 6020 instruction was obeyed before a higher level was terminated, otherwise normal mode operation continues. When slave mode operation is initiated by level 4 becoming active the S register is then loaded from location L+6 and the B register is held in location L+7. In exit from slave mode the S register is stored in location L+6 and the B register held in location L+7.

DATA ROUTING UNITS

Data Routing Units

In a 905 system as previously described a single 'data bus' links the processor, autonomous access channels and store units. Data routing units provide a means of generating additional data buses within a system and of providing links between these data buses. The units also provide a means of preventing a failure on one data bus from causing the complete failure of a system.

Data Routing Unit

A Data Routing Unit is connected to two data buses and provides a means of access from one to the other. The two buses to which a DRU is connected are referred to as its 'master' and 'slave' buses respectively. It is connected to the master bus as a store unit and to the slave bus as an autonomous access channel. When a store cycle with an address within the range covered by the DRU is initiated on the master bus, the DRU requests access to the store on the slave bus. When this request is accepted, the DRU establishes a two-way connection between the master and slave buses and initiates a store cycle of the required type on the slave bus, thus a store unit attached to the slave bus can be accessed by the processor or other unit attached to the master bus.

The address range to which a DRU responds is normally 8192 words, the addresses which it accepts being identical to those which a store unit connected in its place on the master bus would accept. The slave store unit addressed will normally be the first unit on the slave data bus. Facilities are provided for varying the address range accepted, and the slave unit address generated by a DRU, by means of patch connections. The address range cannot exceed 32768 words.

In the case of access to the slave bus not being possible, the DRU itself performs a pseudo store cycle and gives a failure in indication to the master bus by means of simultaneous 'parity error' and 'lock-out' error' signals. Under these circumstances the pseudo-instruction 8 0 is generated as the 'contents' of the location accessed.

Data Routing Control Unit

A Data Routing Control Unit again provides a means of access from one data bus to another but also provides a means of control of autonomous access to the second data bus. It thus provides a means of generating an independent data bus which is not directly connected to the processor.

The two buses to which a DRCU is connected are again referred to as its 'master' and 'slave' buses. A store cycle on the slave bus can be initiated by any one of four autonomous access channels attached to the slave bus or by the initiation of a store cycle on the master bus, with an address in the range accepted by the DRCU. The DRCU accommodates four 'request' signals from the slave autonomous access channels and generates 'accept' signals in return (in the same way as the autonomous control of the processor does). In the event of simultaneous attempts to use the slave store the DRCU assigns these on a fixed priority basis, thus:

Autonomous Channel 1—has highest priority and is accepted first.

Autonomous Channel 2—is accepted only in the absence of a request from Channel 1.

Autonomous Channel 3—is accepted only in the absence of a request from Channels 1 and 2.

Autonomous Channel 4—is accepted only in the absence of requests from Channels 1, 2 and 3.

In the absence of autonomous channel requests, the DRCU can establish connection between the master and slave and initiate a slave store cycle called for by the master bus. The addressing arrangements and failure detection features are identical to those of a DRU. The bus control and failure detection sections of a DRCU are kept entirely separate so that a failure of one section does not involve failure of the other.

System Configuration

The use of a Data Routing Control Unit to provide an independent store for autonomous input/output is shown in the centre diagram on page 21. The DRCU is used here to allow the processor and peripheral store units to operate simultaneously except when cross reference between them occurs, thus the input/output activity does not reduce the processor throughout. This configuration is specially valuable for peripherals which require repeated access to the same data (e.g. unbuffered displays, line-printers).

The top and bottom diagrams on page 21 show dual processor systems. In the first processor A has access to B's store but not vice-versa: this is sufficient when the requirement is for messages to be passed from one to the other. Where both processors require repeated access to common storage the configuration shown in centre diagram is preferable since reference to the common store area by one processor stand less chance of holding up the other. (It is recommended that very complex configuration of these units should be discussed with Marconi-Elliott engineers at the earliest opportunity.)

Performance

As with any autonomous store access arrangement, the time required for an operation includes a variable quantity to allow for the fact that the store may be at any point of its operating cycle at the instant when a request is made: allowance must also be made for higher priority accesses.

The effective times for store cycles initiated on a master bus and performed on a slave bus are as follows:

Unit	*Operation*	*Time*		*Time*	
		1 µs store		*2 µs store*	
		Min.	Max.	Min.	Max.
DRU	Read-restore	1·8 µs	2·8 µs	3·8 µs	5·8 µs
	Clear-write	2·0 µs	3·0 µs	4·0 µs	6·0 µs
DRCU	Read-restore	1·7 µs	2·7 µs	3·7 µs	5·7 µs
	Clear-write	1·9 µs	2·9 µs	3·9 µs	5·9 µs

The times for an autonomous store access cycle performed on a bus controlled by a DRCU are the same as those for a bus controlled by a processor (see Appendix C).

REAL TIME CLOCK

The real time clock provides a 12 bit binary counting register whose contents are incremented once for each unit of time. The contents of the counting register may be read by the processor, program interrupts may be generated at time intervals corresponding to a change in a selected bit of the register. Interrupt generation and the length of the unit of time may be varied by program action. In order to achieve this the unit contains two further registers which are set by program action as follows:

(a) The unit register (6 bits) which controls the length of the time unit used. The contents of the register are interpreted as a binary number μ; the length of the time units is $(\mu+1)$ X2^{-18} seconds. (i.e. $\mu=0$ gives a time unit of 2^{-18} seconds, 3.8147 μ sec. and $\mu=63$ gives a time unit of 2^{-12} seconds, 244.14 μ sec.)

(b) The rate register (4 bits) controls the number of time intervals which occurs between interrupts. The contents of the register are interpreted as a binary number r, interrupts are then generated every 2^{r-1} units of time unless r=0, 14 or 15, in which case interrupts are suppressed. Thus interrupts can be generated at rates down to 1 per second (r=13, $\mu=63$).

15	193	Place contents of count register in Accumulator bits 1–12.
15	4289	load unit register from Accumulator bits 1–6 and rate register from bits 7–10. Clear count register.
15	4288	Acknowledge interrupt.

The clock has an overall accuracy of ±0.02% on the nominal frequencies; variation in service should not exceed ±0.01%. The clock is used in conjunction with an M.I.U. or A.T.U.

Appendix A: INITIAL INSTRUCTIONS

Locations 8180 to 8191 inclusive are used to contain the initial instructions. These instructions are brought into use when a program is entered and remain in use until a 15 7168 or 15 7177 instruction is obeyed. While the instructions are in use the contents of the locations are fixed and cannot be changed in any way. The locations can be used normally after one of the above instructions has been obeyed. The sequence of the instructions is as follows:

8180	/15	8189	8186	15	2048
8181	0	8180	8187	/5	8180
8182	4	8189	8188	10	1
8183	15	2048	8189	4	1
8184	9	8186	8190	9	8182
8185	8	8183	8191	8	8177

Appendix B: 900 SERIES TELEPRINTER CODE

ISO Code Value	*Value with Parity*	*Telecode Character (General)*	*Binary Pattern*	*Teleprinter Keys Pressed to Transmit*	*Effect when Received*
0	0	blank	00000·000	Run out	no effect
1	129		10000·001	A & control	no effect
2	130		10000·010	B & control	no effect
3	3		00000·011	C & control	no effect
4	132		10000·100	D & control	no effect
5	5		00000·101	E & control	no effect
6	6		00000·110	F & control	no effect
7	135	Bell	10000·111	G & control	Bell
8	136		10001·000	H & control	no effect
9	9	Hor. Tab.	00001·001	Tab. (I & control)	no effect
10	10	Line feed	00001·101	Line feed	Line feed
11	139		10001·011	K & control	no effect
12	12		00001·100	L & control	no effect
13	141	Car. Retn	10001·101	Return	Car. Retn
14	142		10001·110	N & control	no effect
15	15		00001·111	O & control	no effect
16	144		10010·000	P & control	no effect
17	17		00010·001	Q & control	no effect
18	18		00010·010	R & control	no effect
19	147		10010·011	S & control	no effect
20	20	Halt	00010·100	Halt (T & control)	no effect
21	149		10010·101	U & control	no effect
22	150		10010·110	V & control	no effect
23	23		00010·111	W & control	no effect
24	24		00011·000	X & control	no effect
25	153		10011·001	Y & control	no effect
26	154		10011·010	Z & control	no effect
27	27		00011·011	K Shift & Control	no effect
28	156		10011·100	L Shift & Control	no effect
29	29		00011·101	M Shift & Control	no effect
30	30		00011·110	N Shift & Control	no effect
31	159		10011·111	O Shift & Control	no effect
32	160	Space	10100·000	Space bar	Space
33	33	!	00100·001	! (1 & Shift)	!
34	34	"	00100·010	" (2 & shift)	"
35	163	£	10100·011	£ (3 & shift)	½
36	36	$	00100·100	$ (4 & shift)	$
37	165	%	10100·101	% (5 & shift)	%
38	166	&	10100·110	& (6 & shift)	&
39	39	′(acute)	00100·111	′ (7 & shift)	′
40	40	(	00101·000	((8 & shift)	(
41	169	)	10101·001	) (9 & shift)	)
42	170	*	10101·010	* (: & shift)	*
43	43	+	00101·011	+ (; & shift)	+
44	172		10101·100	,	
45	45	-	00101·101	-	-

ISO Code Value	*Value with Parity*	*Telecode Character (General)*	*Binary Pattern*	*Teleprinter*	
				Keys Pressed to Transmit	*Effect when Received*
46	46	.	00101·110	.	.
47	175	/	10101·111	/	/
48	48	0	00110·000	0	0
49	177	1	10110·001	1	1
50	178	2	10110·010	2	2
51	51	3	00110·011	3	3
52	180	4	10110·100	4	4
53	53	5	00110·101	5	5
54	54	6	00110·110	6	6
55	183	7	10110·111	7	7
56	184	8	10111·000	8	8
57	57	9	00111·001	9	9
58	58	:	00111·010	:	:
59	187	;	10111·011	;	;
60	60	<	00111·100	<	<
61	189	=	10111·101	=	=
62	109	>	10111·110	>	>
63	63	?	00111·111	?	$_{10}$
64	192	@	11000·000	@	\
65	65	A	01000·001	A	A
66	66	B	01000·010	B	B
67	195	C	11000·011	C	C
68	68	D	01000·100	D	D
69	197	E	11000·101	E	E
70	198	F	11000·110	F	F
71	71	G	01000·111	G	G
72	72	H	01001·000	H	H
73	201	I	11001·001	I	I
74	202	J	11001·010	J	J
75	75	K	01001·011	K	K
76	204	L	11001·100	L	L
77	77	M	01001·101	M	M
78	78	N	01001·110	N	N
79	207	O	11001·111	O	O
80	80	P	01010·000	P	P
81	209	Q	11010·001	Q	Q
82	210	R	11010·010	R	R
83	83	S	01010·011	S	S
84	212	T	11010·100	T	T
85	85	U	01010·101	U	U
86	86	V	01010·110	V	V
87	215	W	11010·111	W	W
88	216	X	11011·000	X	X
89	89	Y	01011·001	Y	Y
90	90	Z	01011·010	Z	Z
91	219	[	11011·011	[(K & shift)	[
92	92	\	01011·100	\ (L & shift)	£
93	221	]	11011·101	] (M & shift)	]
94	222	↑	11011·110	↑ (N & shift)	↑
95	95	-	01011·111	- (O & shift)	←
96	96	@	01100·000	@	/
97	225	a	11100·001	—	A
98	226	b	11100·010	—	B
99	99	c	01100·011	—	C
100	228	d	11100·100	—	D
101	101	e	01100·101	—	E
102	102	f	01100·110	—	F
103	231	g	11100·111	—	G
104	232	h	11101·000	—	H
105	105	i	01101·001	—	I
106	106	j	01101·010	—	J
107	235	k	11101·011	—	K
108	108	l	01101·100	—	L
109	237	m	11101·101	—	M
110	238	n	11101·110	—	N
111	111	o	01101·111	—	O

				Teleprinter	
ISO Code Value	*Value with Parity*	*Telecode Character (General)*	*Binary Pattern*	*Keys Pressed to Transmit*	*Effect when Received*
112	240	p	11110·000	—	P
113	113	q	01110·001	—	Q
114	114	r	01110·010	—	R
115	243	s	11110·011	—	S
116	116	t	01110·100	—	T
117	245	u	11110·101	—	U
118	246	v	11110·110	—	V
119	119	w	01110·111	—	W
120	120	x	01111·000	—	X
121	249	y	11111·001	—	Y
122	250	z	11111·010	—	Z
123	123		01111·011	—	[
124	252		11111·100	—	no effect
125	125		01111·101	—	no effect
126	126		01111·110	—	no effect
127	255	delete	11111·111	delete	no effect

Some systems use teleprinters to Marconi-Elliott 4100 code which differs from the above as follows.

Value 35 £ is replaced by ½
" 63 ? " 10
" 64 @ " \
" 92 \ " £
" 95 – " ←

Appendix C:
AUTONOMOUS ACCESS FACILITY

1. This allows information to be transferred between the store and peripheral devices without using the processor. Information is extracted from and placed in the store by 'stealing' store cycles, hence data transfers are interleaved with normal computing.

Units using this facility, referred to as autonomous access channels, are connected to the 'store bus' lines which interconnect the processor and store units. Lines carrying signals to the store are thus fed by the processor and autonomous access channels in parallel and feed the store units also in parallel. Similarly, lines carrying signals from the store are fed by the store units in parallel and feed autonomous access channels and the processor in parallel.

Control Logic located in the processor regulates the use of the 'data bus' system. An autonomous access channel requiring to perform a transfer sends a 'request' signal to the control logic. At the end of each store cycle the control logic examines the 'request' signals and sends an 'accept' signal to one autonomous access channel, allowing the channel to perform one complete store cycle.

2. Four 'request' signals from four autonomous access channels are accommodated by the control logic: in the event of simultaneous requests from different channels the control logic accepts these on a fixed priority basis, i.e.

Channel 1 has highest priority and is accepted first.

Channel 2 is accepted only in the absence of a request from channel 1.

Channel 3 is accepted only in the absence of requests from channels 1 and 2.

Channel 4 is accepted only in the absence of requests in other channels.

If no requests are waiting the processor can access the store.

3. Operation Times. The time for an autonomous access operation can be divided into two parts, the response time (from the sending of the 'request' signal until the 'accept' signal is received) and the store operation time. The response time includes the time for the store to complete an operation in progress when the request is received. Total operation times for the transfer of one word into or out of the store on channel 1 (highest priority) are:

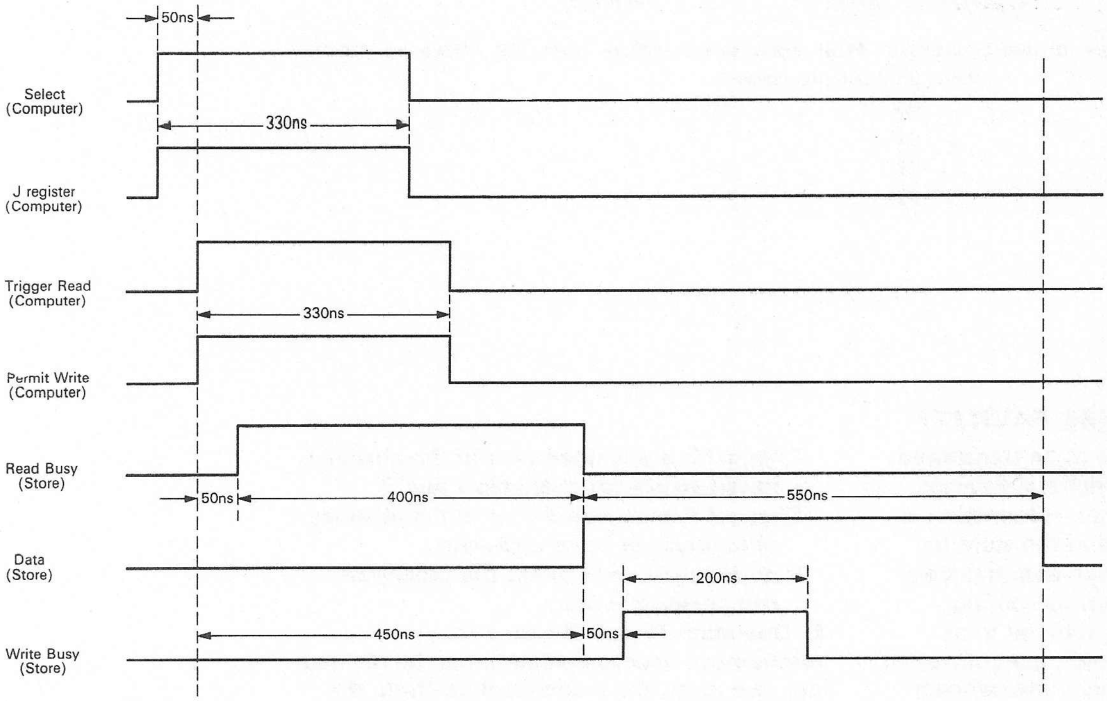
	1·2 µs store	2 µs store
Minimum	1·5 µs	2·5 µs
Maximum	2·7 µs	4·7 µs

For other channels, the response time will be increased when higher priority channels simultaneously make requests. When the maximum possible data transfer rate is required, it is possible for channel 1 to use a number of successive store cycles, hence the maximum rates are:

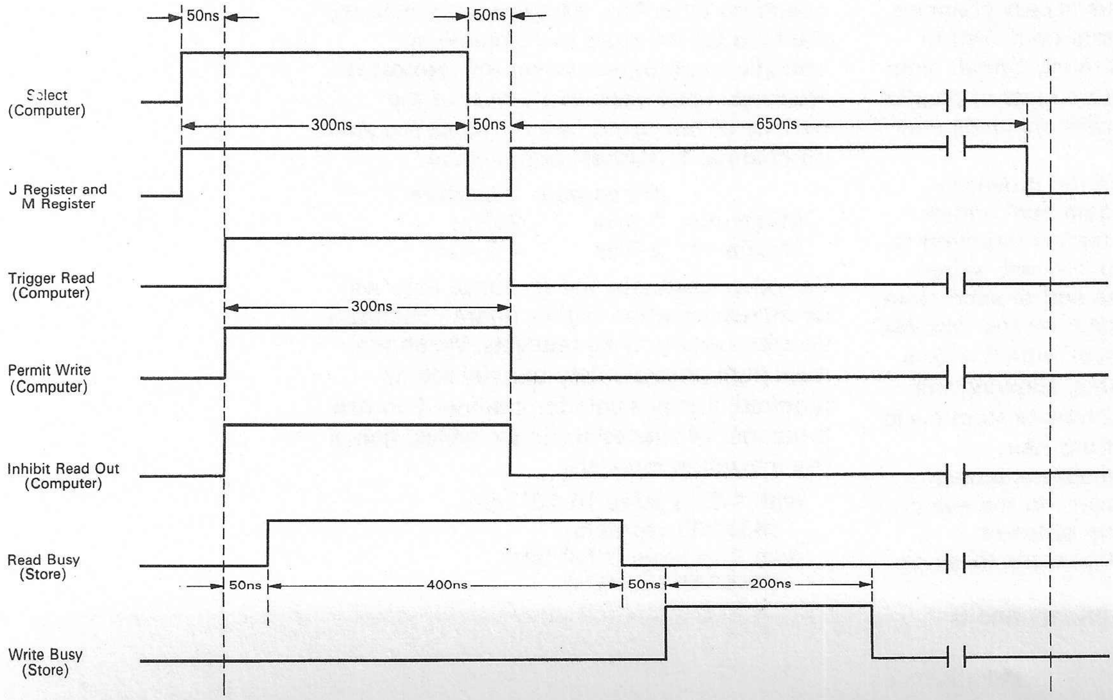
with 1·2 µs store $15{\cdot}10^6$ bit/s (833 333 words/s)
with 2 µs store $8{\cdot}18^6$ bit/s (454 545 words/s)

Appendix D: STORE INTERFACE

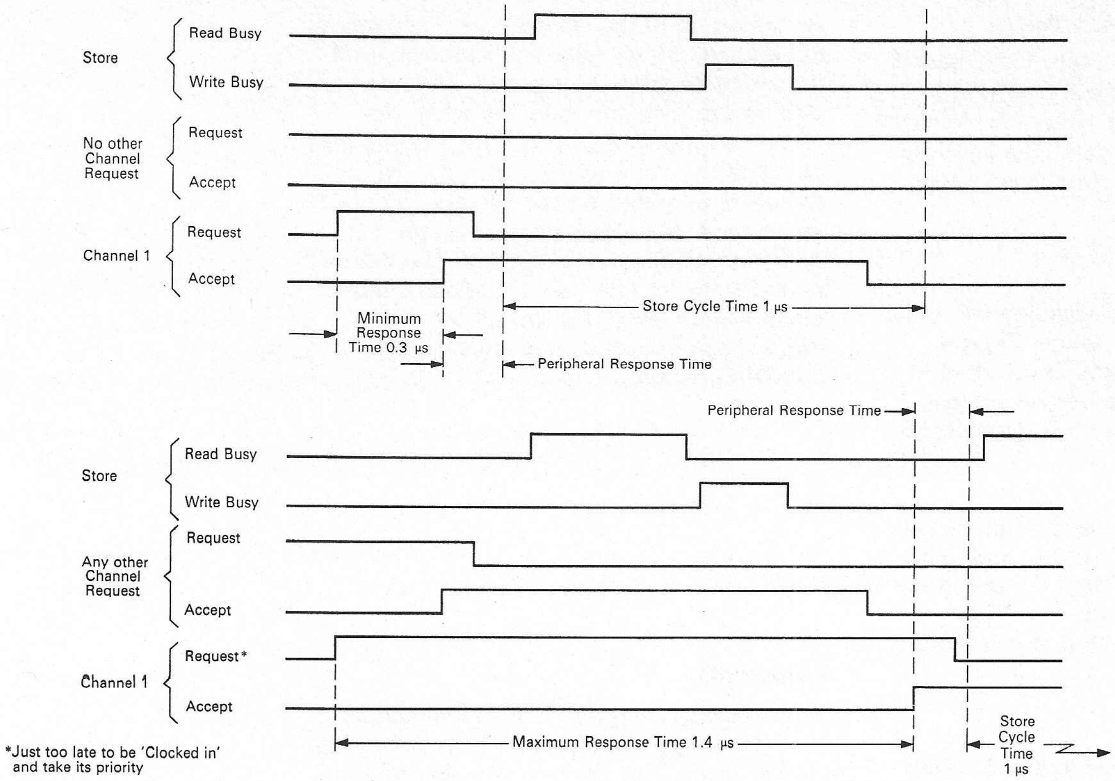
The connectors feed out to a data bus system, which can also be used for data transfers directly to autonomous access channels. Each channel may feed a peripheral capable of corresponding with the store directly: or a less complex peripheral device, via an Autonomous Transfer Unit. In either case, data is transferred without passing through the processor and logic circuitry in the processor regulates the access to store on a priority basis. The processor to store interface therefore contains some signal lines only relevant to the autonomous access channels.



Data Input Timing



Data Output Timing



*Just too late to be 'Clocked in' and take its priority

Autonomous Access Response Timing

Data Transfer

Transfer of data between store and processor will be in a parallel binary mode and will have a word width of 18 bits. The maximum data transfer rate is 833333 words per second.

Data entering the store is duplexed with the store location address, thereby reducing the number of lines involved.

Data Transfer Timing

Data from Store

When an input is required by the processor, it will send a 'Select Store' signal along the store line, and also the address of the store location required. A 'Trigger Read' signal and a 'Permit Write' signal will then be transmitted to the store, and the processor will await a 'Read Busy' signal from the store. The start of data transfer from the store will be indicated by the ending of the 'Read Busy' signal. During the data transfer a 'Write Busy' signal will be sent from the store, and the ending of this signal will occur before the cessation of the data being transferred at the end of the cycle.

Data to Store

When an output is required by the processor it will send a 'Select Store' signal along the store bus, and also the address of the store location required. The processor will then transmit 'Trigger Read', 'Permit Write' and 'Inhibit Read Out' signals to the store, and will await a 'Read Busy' signal from the store.

When the processor receives 'Read Busy', the address information will be removed from the duplexed lines and the data to be transferred substituted. During the data transfer a 'Write Busy' signal will be sent from the store and the ending of this signal will cause the cessation of the data being transferred.

Interface Signals

The functions and directions of the signals on the interconnecting lines at the inferface are given below. The states of the lines carrying binary data are described as ONE or ZERO, and those lines carrying logic or controlling functions, as TRUE or FALSE.

Store Select

From computer, eight lines. A line when set true will allow the appropriate store unit to respond to control signals. It becomes false when the 'Address' lines are set to their zero state. Each line is normally false when the appropriate store is not being accessed.

Address and Data Output

From computer, eighteen lines. Fourteen of the lines are duplexed, carrying both the address and data information. Each duplexed line will be in its correct state for the address bits at the same time as 'Store Select', and will become zero after the start of 'Read Busy' and before the end of 'Trigger Read'. The lines will remain zero for a short duration after transmitting the address. All eighteen lines will then be set to their correct state for the binary word to be transferred, and will remain correct until the end of 'Write Busy'.

Trigger Read and Permit Write

From computer, one line each. Both signals will only become and remain true when 'Store Select' is true, and when the 'Address' lines are in their correct state. The lines are normally false when the store is not being accessed.

Inhibit Read Out

From computer, one line. This line will only become and remain true, when 'Trigger Read' is true and when data is required to be written into store. The line is normally false when the store is not being accessed.

Read Busy

To computer, one line. This line will be set true when 'Trigger Read' is true, and will become false when the 'Data Output' lines are set to their correct state. The line is normally false when the store is not being accessed.

Write Busy

To computer, one line. The line will be set true when 'Read Busy' has become false, and during the time that the 'Data Output' lines are set to their correct state. It will become false before 'Data Input' or 'Data Output' are set to their zero state. The line is normally false when the store is not being accessed.

Data Input

To computer, eighteen lines. The lines will be set to their correct state when 'Read Busy' becomes false, and before 'Write Busy' is set true. The data input information will remain established until the end of the cycle. The lines are normally in the zero state and are only set otherwise when the store is being accessed.

Parity Error

To computer, one line. The line will only be set true when the parity of the data information to be transferred is not correct. In such an event the signal will be set about 150 nanoseconds after the establishment of the data by the store, and will remain true until the end of the cycle.

Store Reset

From computer, one line. The line will be set false when the computer is first switched on, and if in the 'Auto' mode, will become true when the various interlocks clear. On switching on in the 'Manual' or 'Test' mode, the line will be set false continuously until the 'Jump' control is operated. The line will also be set false continuously when the 'Jump' control is operated. The line will also be set false continuously when the 'Reset' control is operated (in the 'Manual' or 'Test' mode) and will only become true on operation of the 'Jump' control. The line will normally be set true but will become false when switching off the computer, or if a line voltage or store temperature fault condition occurs.

Interlock

To computer, one line. The line will be set true when store voltage and temperature are within limits. The line will normally be true, and will only become false when a fault occurs.

Interlock In

From computer, one line. This line will be energised when power is applied to the central processor and will be de-energised when power is removed.

Autonomous Access Channel: Request

To computer, four lines. A line when set to the true state will indicate to the processor that there is an autonomous channel requiring access to store. Towards the end of each store cycle, all 'request' signals will be examined on a priority basis to allow a store access to the data bus system. The 'Request' signal remains true until the appropriate 'Accept' signal is received. The line is normally false.

Autonomous Access Channel: Accept

From computer, four lines. A line, when set true will allow the appropriate autonomous channel unhindered access to store for one complete cycle. The 'Accept' signal will remain true until the end of the cycle, and at all other times when not accessing store, will be false.

Program Level Information

From computer, two lines. The state of these lines, 'E2' and 'E3', will indicate the current level of program, and are provided for a multi-programming facility.

Store Transmitters and Receivers

The central processor contains transmitters and receivers that make direct connection with the signal lines interconnecting the store bus system with the computer.

DATA SUMMARY

Number Representation: Binary fraction in range -1 to $1-2^{-17}$.

Arithmetic: Floating point, double-length fixed point working on fractions, mixed numbers or integers.

Word Length: 18 bits.

Software:

Compilers—ALGOL, FORTRAN or CORAL with blocks of programs written in SIR easily embodied.

Subroutine library—mathematical and test routines.

Diagnostic routines—aids to commissioning and faultfinding.

Speed of Operation: Add, Collate, 2·4 μsecs.

Interrupt: Four levels of interrupt priority allowing access to the computer within 1·2 μsecs.

Interface Signal Levels:

	'0' or False	*'1' or True*
Transmitter	0·4 V	3·2 V
Receiver	1·7 V	2·6 V

Environment: The 905 will operate at temperature within the range 0°C to 40°C (the upper limit may be extended by a suitable cooling system). Humidity limits are 20–90% with no condensation (30–70% is recommended when paper tape is used).

Storage: The units of a 905 system may be stored without detriment at temperature between −10°C and 60°C and humidity up to 95% RH (without paper tape). It is recommended that units be subjected to a functional test at annual intervals. Under these conditions the shelf life is not less than 5 years.

Mains Supply:

The basic 905 system requires an a.c. mains supply as follows:

(i) System with 1.2 μsec store units
Voltage: 230V ± 10%
Frequency 50–60 Hz ± 5 Hz

(ii) Systems with 1.4 μsec or 2 μsec store units
Voltage: 200–250V + 8%–10% selected by tapping in 10V steps
Frequency: 50–60 Hz ± 5 Hz

(iii) Paper tape and teleprinter equipment
Voltage: 230–240V ± 10%
Frequency: 50 Hz ± 1 Hz
Power Consumption
Processor with one store unit of any type: 800VA
Addition for each further store unit: 525VA
Paper tape and teleprinter: 1.2kVA steady. 2kVA surge.

Interference

The system incorporates radio-frequency filters in series with the incoming mains supply. These give suppression of 60 dB over the range 150 kHz to 20 MHz and 40 dB over the range 20 MHz to 150 MHz.

Protection

The incoming mains supply is fused at 10A. The supplies to the various circuits are individually fused and current-limited: high speed over-voltage protection is also fitted.

Failure

In the event of failure of the supply for a period exceeding 10 μs (and on switching off) the computer will revert to the RESET state and the power supply will be switched off in such a way as to retain store contents. When the mains supply is resumed, the computer will start obeying program automatically if the MASTER SWITCH is in the AUTO mode: in the MANUAL or TEST modes it will remain reset until the JUMP control is operated. The register contents will be lost unless use is made of the MAINS INTERRUPT signal.

Dimensions and Weight:

A 905 system consists basically of a series of 19 in. rack-mounting units requiring an overall depth of 57·7 cm (22·75 in.). Dimensions of these units are as follows:

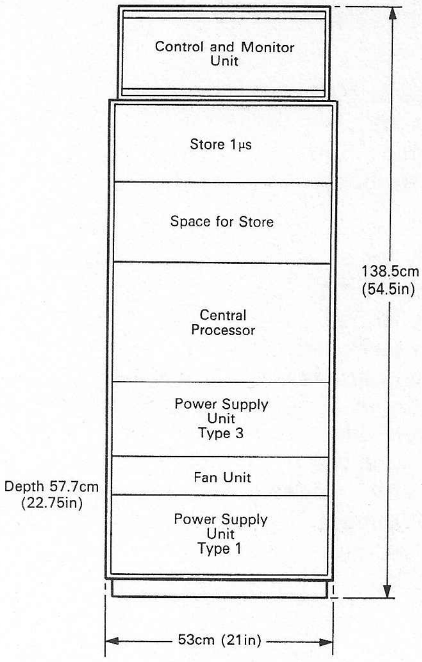
(*a*) *System with 2 μs store*

Unit	*Height*	*Approx. Weight*
Processor	26·6 cm (10·5 in.)	11·4 kg (25 lb)
Store	13·3 cm (5·25 in.)	9·1 kg (20 lb)
Power supply, Type 2	17·7 cm (7 in.)	18·2 kg (40 lb)
Power supply, Type 3	17·7 cm (7 in.)	18·2 kg (40 lb)
Cooling fan	8·8 cm (3·5 in.)	3·2 kg (7 lb)
Control and monitor panel	17·7 cm (7 in.)	4·5 kg (10 lb)
Paper tape control logic and PSU	48·8 cm (19·25 in.)	40 kg (88 lb)
Paper tape control panel	4·4 cm (1·75 in.)	1·6 kg (3·5 lb)

(*b*) *System with 1 μs store*

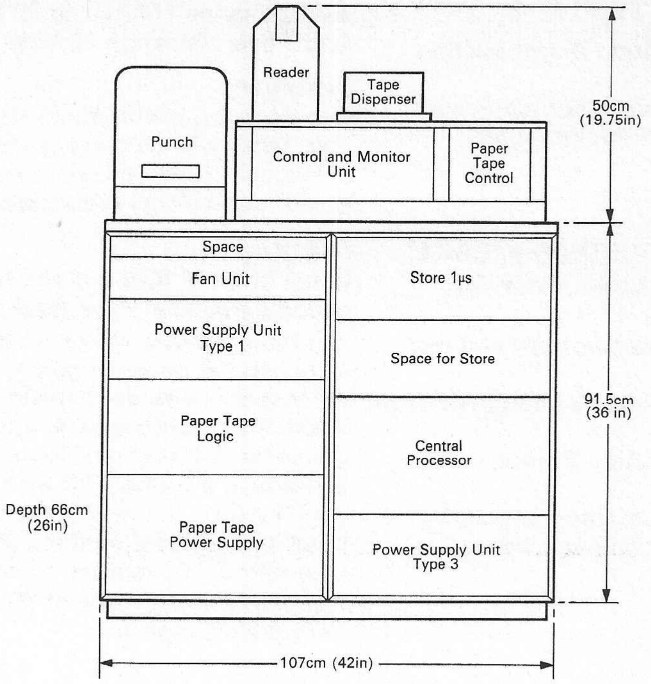
Unit	*Height*	*Approx. Weight*
Processor	26·6 cm (10·5 in.)	11·4 kg (25 lb)
Store	17·7 cm (7 in.)	11·4 kg (25 lb)
Power supply, Type 1	17·7 cm (7 in.)	18·2 kg (40 lb)
Power supply, Type 3	17·7 cm (7 in.)	18·2 kg (40 lb)
Cooling fan	8·8 cm (3·5 in.)	5·2 kg (7 lb)
Control and monitor panel	17·7 cm (7 in.)	4·5 kg (10 lb)
Paper tape control logic and PSU	48·8 cm (19·25 in.)	40 kg (88 lb)
Paper tape control panel	4·4 cm (1·75 in.)	1·6 kg (3·5 lb)

The tape reader is an additional free standing unit 15 cm (6·2 in.) wide, 26 cm (10·5 in.) deep and 25·4 cm (10 in.) high, weighing



Doors removed for Clarity

Dimensions, 905 Standard System, 1 µs Store



Doors removed for Clarity

Dimensions, 905 Desk-Mounted System, 1 µs Store

7·7 kg (17 lb). A simple tape reel box for use with the tape reader is supplied. The teleprinter is supplied complete with stand for floor mounting: it has the following dimensions:

Height: 84 cm (33 in.) (8·4 in. without stand)
Width: 47 cm (18·6 in.)
Depth: 46 cm (18·5 in.)
Weight: 27 kg (60 lb)

The tape punch mechanism is mounted within a sound reducing enclosure with the following dimensions:

Height: 34·9 cm (13·75 in.)
Width: 25·4 cm (10 in.)
Depth: 48·2 cm (19 in.)
Weight: 22·5 kg (50 lb)

A 905 system with 8192 or 16384 words of store will normally be mounted in a desk as shown. Alternatively the systems can be supplied as a series of 48.2 (19 in) rack mounting units. If further store and/or an A.T.U. or M.I.U. is required this will normally be housed in external cabinets.

Height: 145 cm (57 in.)
Width: 53 cm (21 in.)
Depth: 67 cm (26 in.)

The figures quoted are subject to confirmation at the time of ordering.

Marconi-Elliott Computer Systems Limited
A GEC-English Electric Company
Elstree Way, Borehamwood, Hertfordshire
Telegrams and Cables: Elliotauto Borehamwood
Telex: 22777 Answerback: Ellauto Borhwd
Telephone : 01-953 2030

905 Software

The 905 computer system is backed by a comprehensive range of software facilities including compilers, assemblers, operating and executive systems, utility programs, and a library of subroutines.

Complete descriptions, operating instructions and tape copies are provided, together with a regular updating service for all users.

A users' group meets regularly to provide a forum for discussion and exchange of programs.

COMPILERS

High level language programming can be executed on the 905 computer using *ALGOL*, *FORTRAN* or *CORAL*. Versions of these compilers are available to enable programming in these languages on the basic machines with 8K words of store and paper tape facilities. Versions with increased operational facilities, such as "Load and Go", are available for machines with extended core stores or magnetic backing store.

Provision is made in all these compilers for the insertion of machine code and the calling of sub-routines in assembly code (*SIR*). This adds considerably to the power and flexibility of the language, increases its usefulness for on-line programming, and gives the programmer access to the complete 905 library described under Library Facilities.

The compilers are provided with comprehensive diagnostic facilities to assist in the tracing of programming errors.

CONTENTS

Compilers

Assemblers

Library Facilities

Program Preparation Aids

Operating and Executive Systems

ALGOL

Language Facilities

The 905 *ALGOL* is based upon the IFIP subset of *ALGOL 60*, which is particularly suitable for implementation on small computers. The facilities of the language provided by the compiler are:

1) Arithmetic expressions with operators, add, subtract, divide, multiply and exponention. Variables may be real with results in range -9×10^{18} to $+9\times10^{18}$ or integers in range $-131\,072$ to $+131\,072$.
2) Boolean expressions with operators, not, and or, implied, equivalent, less or greater than, and not equal.
3) Designational expressions using labels or subscripted switches (switch lists may use labels only).
4) Compounded statements and blocks.
5) Assignment, go to, conditional, and for statements.
6) Procedure statements with parameters called by value or name. (Call-by-name parameters may only be replaced by actual parameters which are simple variables or constants.)
7) Standard function procedures: abs, exp, ln, sqrt, sin, cos, and arctan, sign, and entier.
8) Standard functions, for print out of intermediate results with real, integer, or boolean arguments.
9) Declaration of arrays of up to 14 dimensions, with standard procedures for lowbound and range determination.
10) Standard procedure for code insertion.
11) Program running control procedures, stop and wait.

In addition there are standard *ALGOL* procedures for reading and writing blocks and files of data onto magnetic tape. The tape formats used are compatible with the equivalent *S/R* assembler and *FORTRAN* programs.

Input and Output

The 905 *ALGOL* introduces two statements, "READ" and "PRINT", and uses very simple syntax.

The elements of a "READ" or "PRINT" list may be arithmetic variables or procedures, whilst a "PRINT" statement may also include arithmetic expressions and strings.

```
e.g "READ" A, B, C [I];
    "PRINT" A, A↑2, B* (C+D), E,
    cos (X/Q) −B [J];
```

The above "READ" and "PRINT" statements would be executed under the control of presumed settings, outputting each number on a separate line with real numbers printed to eight digits, preceded if necessary by a minus sign, and integers to six digits with the leading zeros suppressed and the minus sign, if appropriate, floated i.e. moved along so it precedes the most significant digit.

e.g 8   −9.000000
−136   127.3061
−125372 $-1.36_{10}+12$

Although the presumed settings are adequate for the inexperienced programmer, low program output or program testing, 905 *ALGOL* provides very sophisticated but easily used procedures for controlling input and output format. To specify input from or output to the teleprinter for example it is only necessary to specify either READER (3) or PUNCH (3) in the main program.

For printing several numbers on one line the procedure SAMELINE is used, and for outputting text the characters comprising the message are enclosed in string quotes.

```
e.g "PRINT" PUNCH (3), T, TONS,
    SAMELINE, C, CWT, L, LBS;
```

would produce 16 TONS 4 CWT 2 LBS on the teleprinter.

The following procedures are available to change the presumed setting and the style in which numbers are output.

Digits (N) Prints integers with N digits (1⩽N⩽12)

Freepoint (N) Prints real numbers with N digits (1⩽N⩽8) and a decimal point in the appropriate place.

Scaled (N) Prints real numbers with 1 digit before the decimal point and (N−1) after it and an exponent indicating the power of ten by which the printed number is to be multiplied.

Aligned (M,N) Prints real numbers with M digits before the decimal point and N digits after it (1⩽M+N⩽15)

e.g 'PRINT' X, SAMELINE, SCALED (4), X, ALIGNED (3,4), X, FREEPOINT (4), X;
would produce:

−1.234568 $-1.235_{10}+00$ −1.2346   −1.235
123.4568 $1.235_{10}+02$ 123.4568   123.5
.0012346 $1.235_{10}-03$ 0.0012   .0012

Other characters used for further control of output include:

L. newline
S. space
R. runout
H. halt
B. binary

These characters may appear inside string quotes among text which is itself enclosed within string quotes. If any of these characters is followed by an unsigned integer, the effect is the same as writing the character a specified number of times.

```
e.g "PRINT" L4 CHAPTER N, L2S5;
    "PRINT" L HEIGHT S8 WEIGHT S8
      SPEED;
    "FOR" A: =1 "STEP" 1 "UNTIL" 60
      "DO" "PRINT" B0;
```

The third example has the same effect as "PRINT" "R60".

Strings of characters may be read in as data for subsequent output by using the procedures INSTRING (A,M) or OUTSTRING (A,M), where A is a one-dimensional integer array and M is an integer variable, to which a value is assigned and then incremented automatically by the procedures.

The facilities offered by these input/output procedures give a programmer complete control over any form of desired output.

Error Indications

Translation Errors

905 *ALGOL* provides extremely good error diagnostics and reports which allow for rapid debugging of programs. During the translation phase there are 112 separate error outputs available. These are printed in an easily understandable form with the line in which the error was discovered being displayed. The error will normally be found in this or one of the preceding lines.

```
e.g ERROR No.  28
    LINE No.    6
    2:=6;             ANS:=4*A2;
     ↑
```

If translation is done in the report mode, warning messages are output if identifiers have been declared but not used, or an 'END' is followed by a comment containing a delimiter.

```
e.g *WARNING          *WARNING
    SUM                LINE NO 25
                       "END" X:=1;
```

Also the object program addresses of labels, procedures or an "END" are output in the form:

```
L. LOOP ADR  18
P. CAT ADR   35
E.     ADR   50
```

These are particularly useful if an error occurs at run time for tracing the fault to the point of call.

Run Time Errors

A further 25 separate errors are available at run time taking the form:

```
  ERROR   NO   ADR   RET
           1    36    20
```

With 60% of errors it is possible to continue from where the error occurred. For example, if a negative argument for SQRT (E) is attempted, SQRT (ABS(E)) can be substituted.

Misread or mispunched tapes, two library programs with the same name, a missing library function or a full store are all detected by the loader and a message output.

Operational Modes

Single-pass ALGOL

For a 905 computer with 8K of core store and a paper tape reader and punch.

905 *ALGOL* is, on a basic machine, a single-pass system. On the first pass the programs are translated into an interpretive code in relocatable binary form (RLB) and checked for syntactic errors. A tape can be read in the Report Mode, when the same syntactic checks are carried out as in Translation Mode, but only Errors and Warnings are output and no object code. The use of Report Mode saves time when errors may be expected.

With a standard 250 character per second reader, translation speed is about 270 statements per minute. This is increased to 350 statements with the faster 500 ch/sec reader, using the LG System.

On the second pass, the *ALGOL* Interpreter is first brought into store, followed by the intermediate code tape and any special purpose routines or binary functions required. Machine code procedures can also be added at this point instead of at translation time if so required. The program is then ready for execution.

It is also possible to "dump" a complete image of the store on to paper tape. This is particularly useful for dumping an *ALGOL* program which has been compiled for future loading as a single sum-checked binary tape, or for stopping and dumping the current store state of a long running program.

ALGOL 16K (LG) System

For a 905 computer with at least 16K of core store and a paper tape reader and punch.

With larger areas of core store, *ALGOL* programs can be run "load and go". A minimum of 16K words of store is required and the program is assembled in store as it is translated. This system is designed for convenience in testing small programs and is particularly useful for batch processing.

3500 words of store are available for programs and data without overwriting any part of the system. The translator and loader may be overwritten by data (arrays) leaving 3500 locations for program and 8800 for data. The translator and loader must be re-loaded before running another program.

ALGOL 16K (LP) System

For a 905 computer with at least 16K of core store and a paper tape reader and punch.

ALGOL programs which are too large to be run on the 16K (LG) system may be run using the 16K (LP) system.

Programs are translated to object code by either the basic or 16K (LG) systems and then run using the 16K (LP) system.

There are 8,150 words available for program and 12,200 for program plus arrays and procedures.

FORTRAN

Language Facilities

There are two *FORTRAN* compilers now available for a basic 905 with an 8k store. One corresponds to the level of basic ASA *FORTRAN* and is usable on a basic 905 with 8k store. A full *FORTRAN IV* compiler (ASA standard) is also available for use on larger configurations.

The *905 FORTRAN* allows fixed point and floating point quantities to be mixed freely in any one expression. Integers must lie in the range −131 071 to +131 071 and real numbers in the range -9.10^{18} to $+9.10^{18}$. Control statements include GOTO, IF, DO, CONTINUE, END and STOP and specification statements include DIMENSION, EQUIVALENCE and COMMON. One and two dimensional arrays may be specified and dynamic arrays are allowed in a sub-program. The COMMON statement serves two purposes. Primarily it provides an alternative method of communication between a program and its associated sub-programs to that provided by the use of formal parameters. Secondly, the COMMON statement permits the economic use of storage space allowing the different variables that share the same core store locations each to be referred to by whatever name the programmer finds the most convenient.

There are three types of functions and sub-routines; standard library functions, users FUNCTION and SUBROUTINE sub-programs and additional library sub-programs.

The *library functions* available are ALOG, SIN, COS, EXP, ATAN, ABS, SQRT, all of which are real functions of a single real argument. In addition the function IABS is available which is an integer function of an integer variable.

Function and Sub-Routine Sub-Programs

A SUBROUTINE sub-program has the same form as a FUNCTION sub-program but it returns the results, if any, of its computations to the program or sub-program which called it by altering the values of one or more of its parameters and of variables in COMMON. For FUNCTION sub-programs a value is to be assigned to the function name within the sub-program body. Where an actual parameter to a sub-program is an expression this may include function calls.

e.g B = TMAX (X, (SIN (Y)))

Additional library sub-programs include magnetic tape data handling routines and routines required to operate peripheral devices.

FORTRAN programs are translated into *SIR*, therefore *SIR* code statements may be easily inserted at any point in a *FORTRAN* program and complete sub-programs or parts of sub-programs written in *SIR* may be included. This gives a powerful facility for improving efficiency, handling special types of data and also for driving special purpose peripheral devices.

For certain applications, such as on-line control, when high efficiency of store use and/or running time is required, 905 *FORTRAN* may be used to develop programs and the *SIR* translation produced may then be further developed for greater efficiency.

The efficiency of the *FORTRAN* compiler is about 40%, meaning that it will take 40% of the time to run a program written in *FORTRAN* to run the equivalent program written in *SIR*.

Input and Output

Input and output is paper tape orientated with free format available on input. Input and output statements take the form

```
READ (u,f) K     or    READ (u) K
WRITE (u,f) K    or    WRITE (u) K
```

where

u is an integer constant or variable indicating a device

f is the statement number of a FORMAT statement

K is a list of items to be input or output

'f' may be absent and the statement is then known as an unformatted read/write statement.

If a READ or WRITE statement refers to a FORMAT statement then its effect is determined by the FORMAT statement. FORMAT statements may be continued over several lines and there is, in fact, no limit on the number of continuation lines it is possible to use.

The field descriptors available are F, E, I, H and X. On input, the numeric field descriptors indicate that a number is to be input at this point but the number on the data tape need not be punched in that particular format. Numbers on a data tape are terminated by separators. The field descriptor letters represent the nature of the conversion to be performed between internal and external representations.

Alphanumeric strings on data tapes are simply surrounded by string quotes, 'and'

The Z descriptor is used to cancel an implicit new record. (e.g the newline output at the beginning of a WRITE statement)

Error Indications

Errors detected by the Translator are displayed in the form:

```
E    n+N
<statement>
```

where E is the error number
n is the last statement number
and N is the number of statements since n.

When an error is detected compilation continues in Report Mode. There is a comprehensive list of 49 errors which can be detected at translation time. In addition to these, certain constructions which are not actually *FORTRAN* errors but whose effect in 905 *FORTRAN* is probably not that desired by the programmer are detected by the Translator.

Certain errors in the *FORTRAN* source text will not be detected at translation but will be detected when the object code is assembled. A version of 905 *SIR* within the run-time package is used to assemble the object code. The error messages output at assembly time are *SIR* error messages.

In addition, errors may be detected at run time and comprehensive error messages are output.

Operational Modes

Two-pass FORTRAN

For a 905 computer with 8K of core store and a paper tape reader and punch.

Operation of *FORTRAN* on a basic machine is a two-pass system. On the first pass the *FORTRAN* program is checked for syntactic errors and translated into *SIR* code on paper tape. Complete programs are normally translated as a whole but an individual sub-program may be checked or translated independently.

Typical speed of translation is limited by the punch to about 60 statements per minute.

A tape may be read in Report Mode when the same syntactic checks are carried out as in Translation Mode. Errors and queries are output but no object code is punched. The use of Report Mode saves time when errors may be expected.

There are two methods available for running — Batch Mode and Relocatable Mode. Batch Mode is suitable for programs containing up to about 120 statements. To gain store space larger programs may be further translated into a relocatable binary form and then run. When loading an object code program a store map may be obtained. This lists the absolute addresses of all *SIR* object code identifiers.

When a user has a library of commonly used sub-programs these may be kept as a set of pre-translated relocatable binary tapes. These library tapes can than be added to programs run in either Batch or Relocatable Mode.

The maximum core store available for a *FORTRAN* program plus data on a basic machine is 4500 words including up to 3500 words of program.

FORTRAN 16K (LG) System

For a 905 computer with at least 16K of core store and a paper tape reader and punch.

FORTRAN programs may be translated and run "load and go" using this system. The object is to provide an efficient operating system when running large numbers of small programs containing up to about 120 statements. Larger programs must be run in relocatable mode on the basic system or on the 16K (LP) system. For "load and go" batch operation the maximum space available for program plus data is 2,000 words. Typical translation speed is 250 statements/minute on the 905 with a 250 ch/sec reader, increasing to 350 statements/minute with a 500 ch/sec reader.

To allow the maximum possible size of program to be run, certain parts of the compiler may be overwritten. In this case there are 2000 locations available for program and 11 500 locations available for program plus data.

FORTRAN 16K (LP) System

For a 905 computer with at least 16K of core store and a paper tape reader and punch.

Large *FORTRAN* programs containing more than about 120 statements may be run in a single-pass mode with this system. The object is to run the largest possible *FORTRAN* program on a machine with 16K of core store. There are 7950 words of core store available for program and 12000 words available for program plus data.

Fortran IV

Configuration required:

A 905 computer with a paper tape reader and punch, teleprinter and either 16,384 words of core store, or 8,192 words of core store and random access backing store—a head-per-track disc or a drum with a capacity of at least 64,000 words.

Language

The compiler provides a high-level language facility matching the power and on-line capability of the 905 computer and conforming as closely as possible to the full ASA Standard *FORTRAN IV* Specification. The block data sub-program facility is excluded; mixed type working is allowed.

There is a facility for the free format input of program and data so that for data input it is not essential to know how many spaces or lines separate items.

For use in on-line control and/or data collection, programs written within limited sub-set can be run on an interrupt level. The full language facility may only be used for programs running on base level. *SIR* code may be included at any point.

For a machine with a 16K core store a *FORTRAN* program can be translated to a relocatable binary form in one pass. The compiled program may use any size of core store and each program unit may be up to 8192 words including local data.

Data or program transfer to or from disc (or other devices which deal with binary words rather than 'character' information) are by calls of sub-programs.

CORAL 66

Language Facilities

The language *CORAL 66* has been defined in the Royal Radar Establishment Technical Note No. 732. The facilities provided resemble those of *ALGOL,* but features that are of limited interest in the real time environment and also lead to inefficent implementation are not included. Such features are recursion, call-by-name and dynamic storage allocation.

CORAL 66 has been implemented for the 905 computer, and has demonstrated that average efficiencies of over 70% are achievable, coupled with a considerable saving in program development time. The following language facilities are available in the 905 *CORAL 66* compiler:

1) Arithmetic expressions with operators add, substract, multiply and divide
2) Compound statements and blocks
3) Assignment, go to, conditional and for statements
4) Procedure statements with parameters called by value or location
5) Switch statements
6) Data declarations of single or arrays of items (single or two-dimensional). Items may be integers or scaled fixed point, and may be preset to initialise variables

7) Assembly code insertion and address manipulation
8) Macro generation
9) Character string handling.

Library

The *CORAL 66* library includes the standard mathematical functions such as SIN, COS, ARCTAN, SQRT, and paper tape and teleprinter input/output functions for numbers and character strings.

Operational Modes

A 905 machine with 16K of store and paper tape facilities is required to compile a program. A program can however be compiled to run on a machine with only 8192 words of store. *CORAL 66* is issued as a set of sum-checked binary tapes for input by initial instructions and two passes are required to produce a relocatable binary tape. 400 locations are used by the RLB loader which may be overwritten by data.

The development of large programs is considerably aided by the COMPOOL facility. This enables segments of program to be compiled independently and linked together at load time.

Diagnostics

Rigorous syntax checking is carried out during pass 1 and error messages giving page name, line number, current pair of characters being compiled, current source line contents and fault error code number provide rapid means of fault location.

Some thirty semantic checks are conducted during the second pass and error messages of the same form as above are output.

A store 'map' of the compiled program may be output giving addresses of data and program items.

ASSEMBLERS

The 905 Series Assembler (Symbolic Input Routine *SIR*) enables programs to be written which have a one-to-one correspondence with machine instructions but the programmer need not be concerned with the details of storage allocation. Store addresses can be replaced by names and constants may be included without specifying where they are to be stored. The assembler then performs the task of storage allocation, although the user may retain control over the allocation if he desires.

Blocks of programs written in *SIR* can easily be embodied in *ALGOL, FORTRAN,* and *CORAL* programs, this giving the combination of ease of high-level language programming together with maximum efficiency for critical areas of programs.

An advanced version of the assembler is available to enable 'Macros' to be inserted in a program, and to replace function numerical codes with mnemonics.

SYMBOLIC INPUT ROUTINE (SIR)

Assembler Facilities

Identifiers and Program Blocks

Identifiers are names of up to six characters starting with a letter, invented by the programmer as a substitute for an address. Identifiers are declared by using them as labels preceding an instruction, a constant, or data word.

```
e.g OUTPUT  15      6144
    AREA           -23378
```

Every *SIR* program consists of one or more blocks, each block being divided in a Global Identifier List and a Code body.

Global Identifiers are the links between the different blocks of a program and are listed in the Global Identifier List. They remain in the *SIR* dictionary after an end of program symbol % has been encountered and this permits communication between several programs resident in store together, and between programs independently compiled to relocatable binary form.

Sub-global Identifiers are immediately preceded by " and are removed from the *SIR* dictionary when % is encountered.

Constants

There are four types of constants allowed in *SIR.*

i) Integers and Fractions
ii) Octal Groups
iii) Alphanumeric Groups
iv) Pseudo-instructions

Both integers and fractions are preceded by a + or − sign, negative numbers being held in a 'two's complement' form.

```
e.g +14 stored as
             000  000  000  000  001  110
    −64 stored as
             111  111  111  111  000  000
```

Octal groups are introduced by an & sign so that an 18 bit 900 word can be divided into 6 groups of 3 bits, each being equivalent to a digit from 0 to 7.

```
e.g &312705 is equivalent to
             011  001  010  111  000  101
```

Alphanumeric groups are preceded by a £ sign, followed by up to three alphanumeric characters, which are packed into a location in the six-bit *SIR* internal code. The chief use of alphanumeric groups is for storing characters which are to be punched out at some point in the program. A print routine and conversion table must be included with the program.

Pseudo-instructions are used as constants but are identical in form to ordinary instructions.

Instructions

An instruction comprises three parts—an address, a function and a B-line modifier. A function consists of a decimal integer between 0 and 15 preceded by a / symbol if B-modification is required.

The address part of an instruction can be written in one of four ways, viz:

i) Absolute
ii) Relative

iii) Identified
iv) Literal

An Absolute address is an unsigned integer, not greater than 8191, and refers to the store location with that integer as its address.

There are two types of Relative addresses:
i) Location Relative Address
ii) Block Relative Address

A Location Relative Address is represented by a semicolon followed by a signed integer.

7 ;+3 means 'jump three locations forward if accumulator zero'.
5 ;−1 means 'store in the previous location'.
8 ;+1 means a dynamic stop.

Block Relative addresses consist of an unsigned integer followed by a semi-colon and refer to a location with an address equal to the sum of the integer and the address of the first location in the current block.

An Identified Address consists of an identifier alone or can be followed by a signed integer used to represent an incremented identifier. An identified address may be used before the identifier has been declared.

```
e.g 4      FRED        5      ARRAY+10
```

Literal Addresses are introduced by +, −, =, or £ and are used to write instructions that operate on constants. Instead of labelling a constant, the user may put the constant into the address part of the instruction, and the assembler will automatically allocate storage for that constant. The constant can take the forms described on page 6.

```
e.g 4+10     6  &7777     4   £E5↑
```

A B-Line modification denotes that the contents of the B-register to be added to the address of the instruction, and is used for all forms of indexing including addressing other store modules or handling data arrays.

Directives and other facilities

Other facilities included in 905 *S/R* are:
i) Skips
ii) Patch
iii) Obeyed Instructions
iv) Options
v) Comments

A skip (>) indicates that a number of locations, specified by an integer following the skip, are to be left unaltered, and is used particularly in setting up data arrays.

A patch (↑) directs the assembler to stop placing instructions in consecutive store locations and to place them instead from the location indicated by the patch.

Options are used to alter the way in which the assembler operates and are introduced by asterisk (*) followed by an integer.

e.g *BIT*	*MEANING IF BIT HAS VALUE OF 1*
1	Display labels
2	Load and go
4	Clear the store
8	Punch loader
16	Continue at 32
32	Set dictionary below program
64	Perform checks only

Option settings can be altered at any point within the program.

Comments are included in a program to make the print-up of the program easier to understand, and can be inserted anywhere except in a Global Identifier List.

Any string of characters between (and) is recognised as a comment and is ignored during the assembly.

Error Indications

The *S/R* assembler has 18 different error indications available during assembly and a further 7 during program loading.
Three types of layout are used for assembly error indications:
i) EU, followed by an identifier, which has been detected as unlocated, and an address.
ii) Certain error numbers followed by the bracket count (i.e the number of '['s found since the last START. Assembly is halted but may be restarted.
iii) Error number and bracket count and, on the next line, the line of source text in which the error was detected, with assembly continuing.

```
e.g E 2        16
    PRINT        6        &800000
    E 0        10
               152048
```

At run time errors are diagnosed by reports from individual library programs and by use of the program testing aids described under Program Preparation Aids.

Operational Modes

905 *S/R* is a one-to-one language (i.e one source statement, in general, produces one machine code word) and each source statement comprises either a constant or an instructional word.

The *S/R* assembler is entered into store and the user then has the choice of selecting one of two alternative methods of assembling his program; either "load-and-go", where the programs are assembled directly in the store ready for immediate running, or a single pass system where programs are output on paper tape in relocatable binary (RLB) form.

In the "load-and-go" mode, the assembler occupies about 2500 locations of store, including 900 locations for the binary loader, leaving on a basic (8k) system 5500 locations for program, but the full 8000 words for program plus data by overwriting the assembler and loader may be used.

By outputting the program in relocatable binary form, on subsequent re-entry the complete store is available for program, except for that taken by the binary loader. On a basic (8k) system there are over 7000 locations available for program, which again may be increased to 8000 words for program and data by overwriting the loader.

Typical speeds for "load-and-go" operation are 200 source words per minute on the 903, and 400 source words per minute with the faster 905.

Although it is usually more convenient to assemble programs in "load-and-go" mode, it is occasionally advantageous to assemble programs in "non-load-and-go" for the following reasons:

a) RLB tapes are much smaller than *S/R* tapes and are read in at six times the speed.

b) Larger programs can be entered using "non-load-and-go" assembly because:

   i) In the first pass the program is not stored in the computer. The whole store, apart from the area occupied by the assembler, is available for the dictionary.

   ii) On loading the RLB tapes, dictionary space is not required for local identifiers.

   iii) The loader is substantially shorter than the complete assembler.

   iv) A large program can be assembled in sections so that when errors are discovered only the relevant section need be reassembled.

It is possible to mix RLB and mnemonic tapes using the assembler. This facility permits library subroutines to be stored as RLB tapes and a *S/R* program to use them without itself having to be translated to RLB form.

LIBRARY FACILITIES

The 905 library contains packages for floating point and double length arithmetic, a set of standard mathematical functions, and routines for handling and control of peripherals. These programs use a standard environment provided by *S/R* systems routines, which provides the user with a framework for the development of a library suited to his own use.

Routines are also provided for the handling of data at block and recorded level on magnetic tape files.

MATHEMATICAL ROUTINES

QSQRT

QSQRT calculates the single-length square-root of a single-length or double-length fraction with a maximum error of approximately 7×10^{-6}.

QSQRT uses Newton's method to calculate the square root of a double-length number and occupies 52 locations of store.

The average time is between 250μs and 5·3 milliseconds on the 903, and 30μs and 660μs on the 905. (1μs store)

QLN

Calculates $\frac{1}{16}\log_e x$, where x is the fraction in the accumulator, with a maximum error of $1{\cdot}5\times10^{-5}$. QLN occupies 58 locations and time taken averages between 1·3 and 2·8 milliseconds on the 903 and 0·162 and 0·35 milliseconds on the 905 with 1μs store.

QEXP

Calculates exp $(2^p x)$ where

$-1 \leqslant x < 0$

$p \geqslant 0$ and p is integral, with a maximum error of $1{\cdot}5\times10^{-5}$.

QEXP occupies 55 locations and time taken averages 3·7 milliseconds on the 903 and 0·46 milliseconds on the 905.

QSIN

Calculates $\frac{1}{2}\sin\pi X$ and $\frac{1}{2}\cos\pi X$, where X is the fraction in the accumulator, to a maximum error of $3{\cdot}0\times10^{-5}$. QSIN occupies 74 locations and time taken averages between 1·4 and 1·8 milliseconds on the 903, and between 0·175 and 0·25 milliseconds on the 905.

QATAN

Calculates $T=(1/\ )\tan^{-1}(x/y)$ with both X and Y being between −1 and +1 to a maximum error of $3{\cdot}0\times10^{-5}$. QATAN occupies 128 store locations and the time taken depends on the values of Y and X/Y, but the maximum is approximately 0·4 milliseconds.

FLOATING POINT OPERATIONS

Floating Point Facilities

The interpreter program QF is used to perform operations on floating point numbers and contains routines for operations corresponding to all the machine instructions on fixed point numbers except function 15.

A floating point number may be held in store using either a packed or unpacked format. In the packed format two computer words are used; 27 bits allocated to the mantissa, 7 bits to the exponent, and one to sign. The unpacked format uses three words; 34 bits allocated to the mantissa, 18 bits to the exponent and one bit to sign.

The interpreter also contains facilities for converting integers and fractions to floating point numbers and vice versa.

QF MATH is a set of sub-routines used in conjunction with QF to compute mathematical functions of floating point numbers.

The functions provided are square-root, sine, cosine, arctan, natural logarithm and exponential.

Operational Characteristics

QF occupies some 900 locations and is distributed as a *S/R* mnemonic tape. The maximum error in multiplication is $2^{-34}y$, division error is $2^{-32}y$ and other operations have maximum errors of $2^{-35}y$ where y is the result of an operation. Typical speeds of operation for the 903 and 905 (1µs store) are given in Table 1.

TABLE 1

Execution times, microseconds

Function	*905 (1µs)*
Add	320
Subtract	350
Multiply	350
Divide	660

QFMATH is distributed as a *S/R* mnemonic tape and must be assembled immediately after QF. It occupies some 500 locations. The maximum computational error is 8×10^{-8}. Typical operating times are as shown in Table 2.

TABLE 2

Execution times, microseconds

Function	*905 (1µs)*
Square-root	760
Sine/Cos	200
Arctan	360
Natural log	300
Exponential	160

DOUBLE LENGTH ARITHMETIC

Double Length Facilities

The interpreter QDLA performs arithmetic functions upon double length fixed point fractions in the range $-1{\cdot}0 \leqslant F < 1{\cdot}0$. The majority of the 905 machine code instructions are interpreted, and in addition there are routines for the input and output of numbers in fractional and integer formats.

Mathematical subroutines are provided to calculate as double length fractions, the square root, sin, cos, and arctan of a double length fraction.

Operational Characteristics

QDLA occupies some 820 locations and must be used in conjunction with SSYS1 (*S/R* Systems) which occupies some 200 locations. No errors are introduced by the routines except for multiply where the maximum error is $+2^{-34}$, divide where the maximum error is $+2^{-32}$ and on input and output the error may be $\pm2^{-34}$. Approximate speeds of operation are given in Table 3.

TABLE 3

Execution times, microseconds

Function	*905 (1µs)*
Add	80
Subtract	80
Multiply	130
Divide	490

QDASIN, QDAATAN, and QDASQRT are used in conjunction with QDLA, for double length sin, cos, arctan, and square-root calculations. They are all issued as *S/R* mnemonic tape and occupy 106, 167, and 52 locations respectively. The maximum error for the sin/cos routine is $0{\cdot}5\times10^{-9}$ for arctan $0{\cdot}6 \times10^{-10}$, and the maximum error in square root calculation is $0{\cdot}2\times10^{-9}$. Typical speeds of execution are given in Table 4.

TABLE 4

Execution times, microseconds

Function	*905 (1µs)*
Sin/Cos	6000
Arctan	5200
Square root	2000

MACRO ASSEMBLER (MASIR)

The Assembler will run on any current 900 series machine and the basic version requires an 8k core store, reader, punch and optional teleprinter. On a 905 computer with disc operating system source code may be taken from disc and relocatable binary placed on disc.

MASIR is a development of the 900 series SIR Assembler. It allows a great variety of user defined macros and conditionals and source lines. MASIR generates relocatable binary code, which may be loaded into any module by the linking loader. The code generated can have full machine code efficiency while macros give many of the advantages of a high level language.

Summary of facilities

1. User definition of macros with replacable parameters and nested definitions if required.
2. Conditionally compiled code and macros. This allows dummy peripheral routines or diagnostic information to be assembled or ignored without editing the source program.
3. Macro calls with parameters. A single macro call may generate a large number of machine instructions.
4. Mnemonic names for machine code functions.
5. Flexible loading of program units into any module, and communication between these units.
6. Fortran and Assembly code programs may be linked by loading with the linking loader.

SIR SYSTEMS

SIR Systems Tape 1 (SSYS1)

SSYS1 is a set of *S/R* systems subroutines which define a software interface for:

Character Input and Output
Error Output
and end of program situations.

SSYS1 consists of:

a) QCHIN a routine providing a standard interface for character input from paper tape reader or teleprinter using 8 track code. The user may design versions for use with a choice of telecodes or input devices. It occupies 50 locations.

b) QCHOP is for character output. The standard version is for output to paper tape punch or the teleprinter in 8 track code, but the user may design variations for different telecodes or output devices. The routine occupies approximately 40 locations.

c) QERROR provides a standard interface for error handling. The version of QERROR outputs a one line error message on the teleprinter or tape punch. It occupies some 70 locations and uses QCHOP. The user may develop variations obeying the basic interfaces specification, to output to other devices, alternative layout of error messages etc.

d) QPAUSE is a routine to be used for a temporary halt or break in running of a program, and transfer of control to QSTOP is used for completion of a program.

SIR Systems Tape 2 (SSYS2)

This is a set of *S/R* systems routines for handling of interrupts from standard peripherals. The tapes are not generally distributed, but can be made up for the requirements of a particular installation.

PERIPHERAL ROUTINES

Paper Tape and Teleprinter

QIN1

Input of an integer or mixed number for paper tape reader or teleprinter can be performed by QIN1. Integers must be in the range −131071 to +131071 and are held with absolute accuracy. Mixed numbers are scaled by division of a power of ten using a factor provided by the user and stored as a fraction with a mean error of 4×10^{-6}.

It is distributed as a mnemonic tape for input by the *S/R* assembler. It occupies approximately 220 locations and uses QCHIN and QERROR (approximately 160 locations) of the *S/R* Systems tape 1.

QOUT1

This is used for output of the contents of the accumulator as an integer or a fraction, the format being defined by a parameter word. Fractions are output with a maximum error of approximately $7{\cdot}6\times10^{-6}$.

Approximately 140 locations are used by this routine which is used in conjunction with QCHOP and QERROR (approximately 130 locations) of the *S/R* Systems tape 1.

PROGRAM PREPARATION AIDS

General purpose programs are available for all types of program preparation and testing off line, together with utility programs to produce binary copies of programs for rapid loading.

Program Commissioning and Testing Aids

MONITOR is a dynamic testing aid which gives the facility of a temporary hold-up at any specified point in the program under test while the contents of the accumulator, Q register, and any specified core locations are output to the teleprinter.

A parameter tape is used to define hold-up points and locations to be output. The address of locations whose contents are required for examination may be directly or indirectly defined, and blocks of store locations may be called for monitoring.

Various options of the form and content of the output may be defined by the parameter tape. The output may be in integer, octal or instruction form and the monitoring of the accumulator and the Q register is optional. The parameter list may be cancelled and a new parameter tape input.

MONITOR is distributed as a mnemonic tape for input by *S/R*. It occupies 612 locations.

Static and 'post mortem' checking of programs can be carried out using Q CHECK which enables the contents of any number of specified store locations to be printed in integer, fractional, binary or instruction form.

Q CHECK is distributed as a machine code tape for input by *S/R* or T2 and occupies 249 locations.

Q CHECK IV provides some additional facilities in that the contents of individual locations can be altered by input from the teleprinter. Dynamic stops can be inserted in the program and removed later. A program may be triggered at any store address. Q CHECK IV occupies 500 locations.

Tape editing to producing modified copies of *S/R, ALGOL, FORTRAN* or machine code programs may be performed by the use of EDIT. A correction tape containing a series of commands is stored and the tape to be modified is input. The correction commands are read in succession and operate on the appropriate amounts of the input tape to produce a modified copy.

The editing commands allow insertion and deletion of character strings or blocks of program, in a series of input tapes.

EDIT is distributed as a mnemonic tape for input by *S/R* and occupies 622 consecutive locations, the correction tape being stored above the program.

Program Dumps

Sum checked binary tapes of store contents can be produced by means of T22. Blocks of locations may be output in any order as defined by a data tape. The tape produced is headed by a binary loader and is suitable for input using the processor's built-in initial instructions. The computer words are output as three consecutive characters, each block preceded by a directory. Two check sums are formed by the addition of all the words and directories output and are punched as the final items of the tape.

T22 is distributed as a binary tape to be input by initial instructions and occupies locations 8046 to 8179 inclusive. The SCB tapes produced by T22 may be checked by C4. This program will also compare the contents of the SCB tape with those of the store.

When using C4, errors in the loader or failure of the SCB to sum check are indicated by teleprinter messages. Discrepancies between the contents of the store and the SCB tapes are displayed as three integers giving the address being checked and the contents of the tape and store. C4 is input by initial instructions and occupies locations 8000—8179 inclusive. Production of tapes suitable for input by T2 or *S/R* from stored program can also be achieved by use of QT2OUT. Tapes for input by initial instructions (without sum checks) are produced by QBINOUT. Parameter tapes are used to specify locations to be output. QT2OUT outputs a program from store as a single block of relatively addressed instructions and QBINOUT provides a binary version of the stored program.

Machine Code Input

Programs written in machine code may be read, translated and written into store by means of T2. Programs may be written in blocks, with the absolute value of the first word of the block, the block address, specified in a directory at the head of the program. There is provision for up to 85 block addresses.

An impermissible character, contextual or format errors, directory addresses greater than +7740 and overwriting of T2 by the last block, are detected and indicated. T2 is distributed as a binary tape and occupies locations 7740—8179 inclusive.

Tape Copying

Program tapes can be rapidly copied and simultaneously checked by means of 'COPY TAPE'. Audio indications are given to the operator if errors occur during reading or punching. Long programs can be copied and checked in two separate operations using 'Q COPY'.

RANDOM ACCESS BACKING STORE OPERATING SYSTEM—RADOS

General

A comprehensive operating system to develop and run off-line programs using disc or drum random access backing store is provided by RADOS.

Programs can be stored on the backing store in character form and in relocatable or fixed binary form. Compilers, utilities and fully tested systems are stored in fixed binary. Tested sections of systems and library subroutines are held in relocatable form. A program or batch of programs can be processed automatically using operator commands input by teleprinter or paper tape.

A source code tape is input and stored in character form on the backing store. The operator can then use a set of commands to edit, compile or assemble, load, test or run without operator intervention or further use of paper tape.

Data Filing

Two methods of filing data on the backing store are provided. The data may be arranged in segments which may be addressed randomly or it may be chained together into a number of serial files. In the former case the data is accessed in a manner analogous to that of addressing core store and the Assembler gives the facility of substituting data names for sector addresses. A serial file is referenced by specifying its name, and the file can hold information in word or character form.

Dynamic Program System

Provision is made for dynamic program operation where the systems program or suite of programs is too large to be held in core store. The program is broken into segments held on the backing store, and then called down singly to be run.

As well as running a single large program the dynamic program system may be used to run a number of completely separate jobs, switching between them in some tens of milliseconds on demand.

EXECUTIVE AND CONTROL SYSTEM EX 905

General

EX 905 is modular in concept, providing a number of sections which the system designer may select as appropriate to his task. Assemblers, compilers and device routines are all designed for ease of integration and incorporation in the executive. The executive contains modules for interrupt handling, time allocation, standard peripheral device routines and an executive for the 905 dual program unit. The operating system DISC may be incorporated. A utility program enables the system designer to produce tailored versions of the executive modules fitted to the user's configuration.

Interrupt Handling

The module EX 1 provides the basis for handling the three levels of interrupt available on the 905 computers.

The standard usage of levels is as follows:

Level 1 This is reserved for power failure interrupt. It stores the register contents to allow for restart on power restoration.

Level 2 This is allocated to devices requiring very rapid response time. The systems designer may allocate this normally to one device only. The interrupt routine must be completed within 100µs.

Level 3 All general interrupts are grouped on this level through an interrupt multiplexer.
Control is transferred to one of a set of device routines which must be completed within 300µs.

Level 4 Is used for all routine background work and interrupt programs requiring further processing are queued on this level.

Time Allocation

The allocation of processor time to various demands for work may be either a simple queuing system, EXQ, or a time slot system, EXTIMA.

There are three queues administered by EXQ. Two queues are worked on the end-around principle, first in — first out. Two such queues are provided, one queue always having priority over the other. The third queue is a time event queue. When a process is required at a given time ahead a tag is placed in this queue. The events are arranged in correct time order, by subroutine, so that the closest event is at the head of the queue. Using the above executive a complete real-time system must be designed as a whole, so that no program takes up more than a reasonable amount of time on Level 4. A new program cannot be introduced without calculating its effect on all other real time programs. The time slot allocation system EXTIMA gives greater flexibility and allows independent programs to be introduced into a system and to be run on equal status. Equal slots of level 4 time are allocated to each program. At the end of the time slot the current program is interrupted, the contents of registers are stored away, and replaced by values for the next program. A program may inform the executive that it does not require time until a specified event, and its slot may then be used by another program. Each program runs as though it had exclusive use of the computer but it is not protected against erroneous operation of another program. If common routines are required they must be written in re-entrant form. These time allocation routines may be entered directly from *FORTRAN* programs.

Device-Independent Input/Output Interface

A standard interface is used to communicate with peripheral device routines. All 900 series assembler and compilers use this standard interface thus enabling ready substitution of input and output media.

Dual Program Executive

The dual program executive 'EXDP' enables a slave program to time-share a 905 system with a master on-line program. The slave program may be at any stage of testing, such as compilation, assembly, debugging or simply running.

The slave program will normally be an off-line program but restricted use of on-line peripherals is permitted. EXDP keeps indicators for all peripherals which the slave program may use. Peripherals in use by the master program will not be available to the slave program which will be held up until the relevant peripheral indicator is clear.

The disc operating system may be used to run slave programs. The slave is restricted to an allocated area of the disc but the master program may write into this area to transfer data to the slave.

If the slave program attempts to access illegal store or peripherals an error message is output.

A simplified version of the executive, EXPD1, may be used independently of the other EX 905 routines. This will deal with paper tape and teleprinter peripherals only.

Systems Builder

The modules described above will need fitting to each user's configuration. The utility program 'EXBUILD' provides a means of preparing tailored systems automatically. It accepts a set of parameters consisting of store size, maximum size of buffer areas, peripherals fitted, and code for special device and interrupt routines etc. A relocatable binary form of the required executive will be produced. The systems program may be written in Assembly code or *FORTRAN*, or a mixture of both. Executives may be generated in this way for testing purposes also.

Configurations for use of EX 900

EXI, EXQ and EXBUILD will be available for the 905 with 8192 words or more of store. EXTIMA and EXDP are being designed to operate on a 905 with a minimum of 16K of store and Dual Program Unit.

The operating system is for use on the 905 with disc or drum random access backing store.

Marconi-Elliott Computer Systems Limited
A GEC-English Electric Company

Elstree Way, Borehamwood, Hertfordshire
Telegrams and Cables: Elliotauto Borehamwood
Telex: 22777 Answerback: Ellauto Borhwd
Telephone: 01–953 2030 Ext.

905 Peripherals

A wide range of peripherals is available for use with the 905 computer which operate from a 900 Series Standard Peripheral Interface.

Information may be transferred between a peripheral device and the store or the processor in one of the following three ways:

Single word transfer: One 18-bit word is transferred by a single instruction to or from the accumulator via the Standard Peripheral Interface.

Block transfer: A series of 18-bit words are transferred to or from a series of consecutive store via the Standard Peripheral Interface by a single instruction. This process uses both the A and the Q registers.

Autonomous transfer: A series of 18-bit words are transferred to or from a series of consecutive store locations via the Autonomous Transfer Unit, while the central processor continues with other words.

The teleprinter, paper tape reader and paper tape punch are connected to the processor by a special interface which transfers 8-bit characters to or from peripherals, selected according to a 4-bit address.

CONTENTS

The Marconi-Elliott 900 Standard Peripheral Interface

Transfer of information between the central processor of a 900 Series computer and its peripheral devices is effected across the 900 Standard Peripheral Interface. Any peripheral device designed to match the 900 Standard Peripheral Interface may be connected direct. Peripherals with other interfaces, such as the 4100 interface or the NPL interface, may be connected via the appropriate 900 Interface Matching Unit.

The peripheral interface signal lines operate one peripheral cluster. When more than one peripheral is required a 900 Multiplexer Unit is connected to the interface. Sockets are provided for up to eight peripheral clusters.

The 900 Standard Peripheral Interface transfers 18-bit words in parallel between the accumulator and the peripheral. Each of the 900 Series peripherals is assigned a number within the range 0 to 15 which is known as the 'peripheral class number'. The sixteen classes of peripheral are normally selected according to bits 8 to 11 of the input-output instructions, while bits 1 and 2 are used to indicate the nature of the operation (e.g data transfer or control/status). When the Interface is used in this way, one or more control words are frequently used to specify the operation further. Certain classes of peripherals use all of bits 1 to 7 to indicate the nature of the operation. They may, in addition, require control words. The Interface has three interrupt lines, which are used by the peripheral to interrupt the processor on a priority basis.

Autonomous access facility

There are four autonomous store access channels which are connected to the 'data bus' lines interconnecting store and processor. An autonomous Transfer Unit may be connected to any of these four channels. This provides facilities for up to eight peripherals to transfer information to and from the store, without using valuable processor time. Information is extracted from, and placed in, store by 'stealing' store cycles, thus interleaving data transfers with normal computing. Control logic in the processor regulates the use of the 'data bus' .

905 PAPER TAPE STATION

The 905 Paper Tape Station comprises a paper tape reader, a paper tape punch and a controller, a teleprinter is optional. It provides a means of inputting information and receiving information from the processor and is connected to the processor by a special interface.

Paper tape reader

The paper tape reader is a photoelectric device and is available in 250 or 500 characters-per-second form. Characters are read from an 8-bit buffer register. The tape input instruction causes the contents of the accumulator to be shifted seven places to the left and the contents of the buffer to be transferred to the least significant eight bits of the accumulator. The new bit 8 of the accumulator is zero if, and only if, both the old bit 1 of the accumulator and bit 8 of the paper tape were zero.

Five, seven or eight-track paper tape may be used. These are respectively 0·687 inch, 0·875 inch and 1·0 inch wide. The standard is eight track tape using I.S.O. code. The tape reader sends a signal to the controller when it is ready to input a character.

Paper tape punch

The paper tape punch operates at a maximum of 110 characters per second. The tape output instruction causes the eight least significant bits of the accumulator to be output to a buffer and then punched on tape when the punch is ready. The punch normally uses eight-track paper tape. If five or seven-track tape is used then the bits of the character corresponding to the absent tracks must be zero. The paper tape punch can send a signal to the controller when it is ready to punch a character.

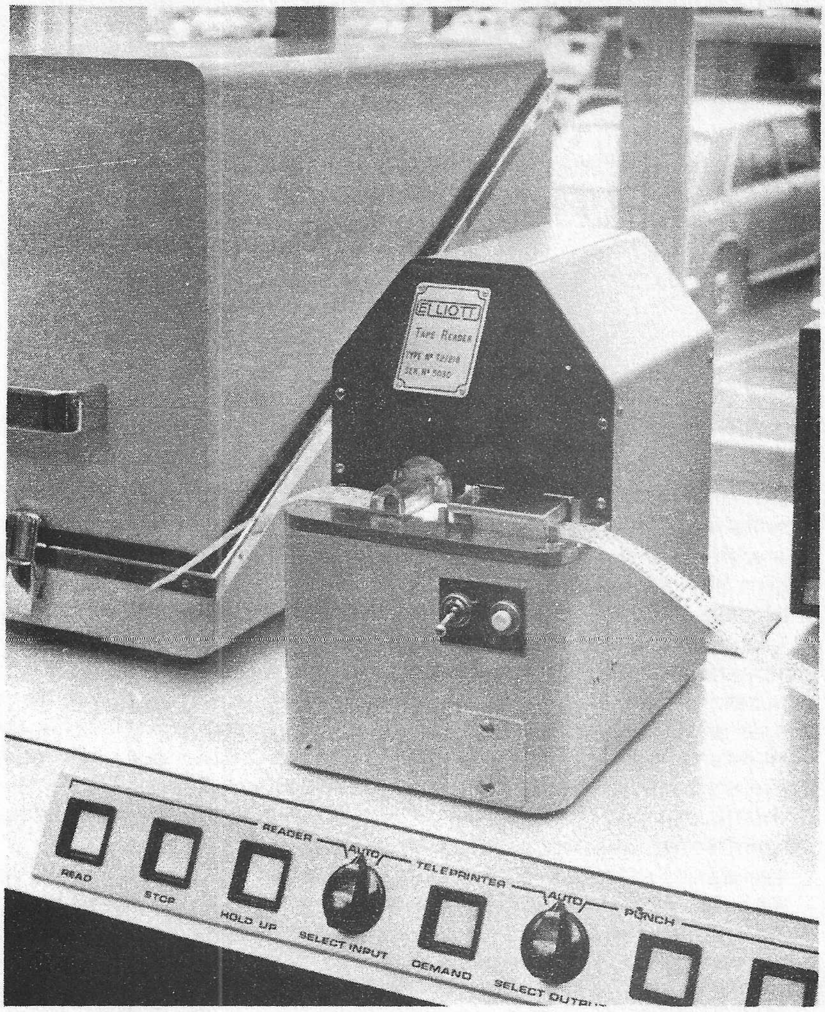
Teleprinter

The teleprinter unit has its own stand and includes an integral paper tape punch and paper tape reader which operate asynchronously at up to 10 c.p.s. It is not recommended that the printer punch be used for outputting large amounts of data.

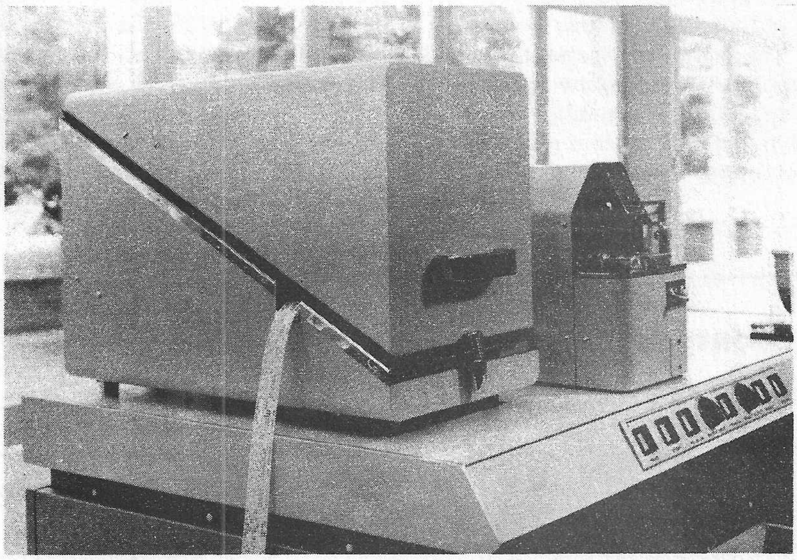
The teleprinter unit enables the operator to control the running of a program by sending information to, and receiving information from, the processor. All information input or output via the teleprinter produces printed copy.

Provision is made for the teleprinter to generate ninety-six codes of which sixty-three produce printed output. There are forty-two character keys, two shift and control keys, and six operation keys. The 7-bit codes are punched on eight-track tape with track 8 as a parity bit. The line spacing of the printed output is normally six to an inch but can be adjusted to three to an inch. The line length is 6·9 inches (sixty-nine characters) and the type pitch is ten characters to the inch.

A LOCAL mode switch is provided to render the teleprinter off-line, i.e the keyboard is connected directly to the teleprinter reader and teleprinter-punch, therefore data input to the teleprinter is not routed to the central processor.



Paper Tape Reader



Paper Tape Punch

Controller

The paper tape station can be operated in 'on-line' or 'off-line' mode. In the 'off-line' mode the paper tape station controller stops the computer until the required device is available.

To facilitate program control a status word indicates the paper tape device channels which are busy.

In the 'on-line' mode an instruction to a busy device is effectively treated as a do-nothing instruction.

The paper tape station controller is switched to the 'on line' mode by a specific instruction. It is switched to 'off-line' mode either by a specific instruction or by a system reset.

Control

Mounted on the control panel are two input/output selection switches. SELECT INPUT: is labelled READER/AUTO/TELEPRINTER and controls the routing of input instructions. If it is in the READER position all input instructions are routed to the reader, and if in the TELEPRINTER position to the teleprinter. In the AUTO position, input instructions are routed as defined by the instructions.

In addition to the above, each item on the paper tape station has its own controls, such as on-off switches.

Packaging

The paper tape reader and paper tape punch are mounted on the 905 desk. The controller, providing logic and power supplies for the equipment, occupies one shelf of a 19-inch rack and may be housed within the 905 desk. The teleprinter is mounted on its own stand. The tape and teleprinter control panel containing the operator's switches and lamps associated with the paper tape station stands on the 905 desk.

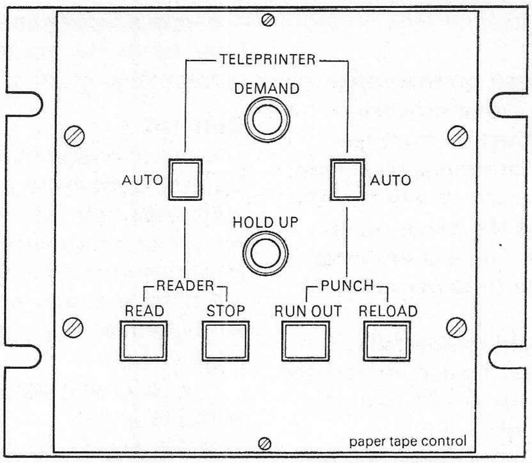
SECOND 905 PAPER TAPE STATION

General

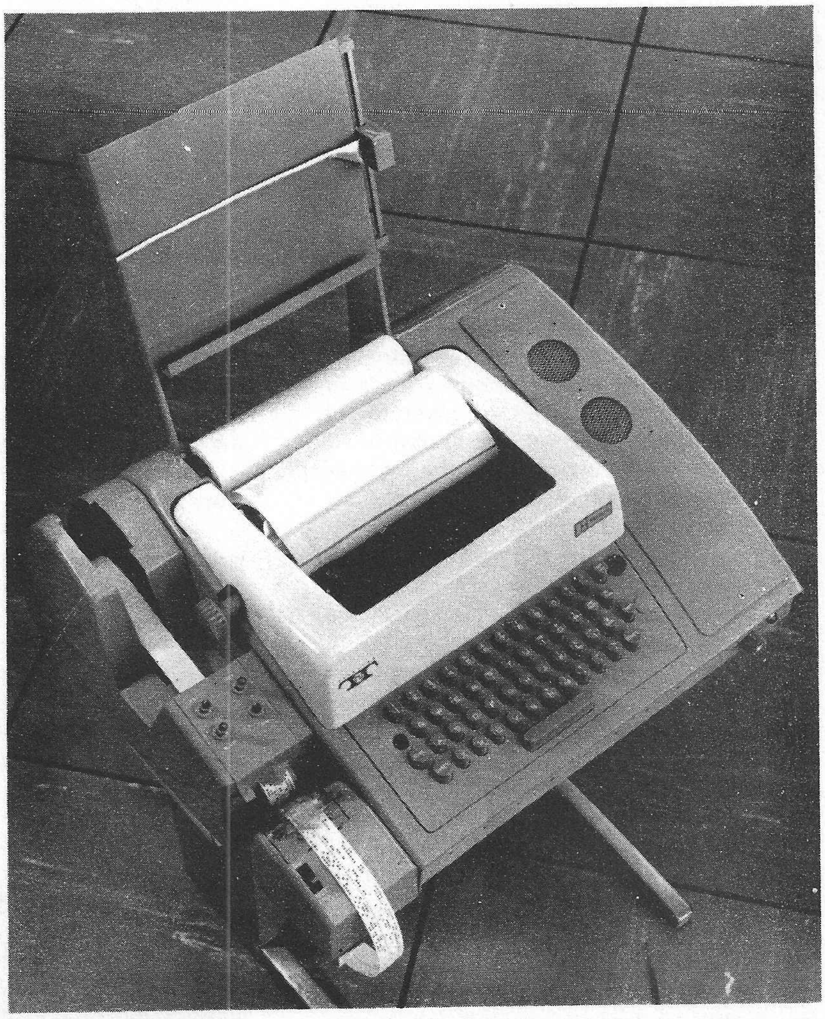
Where additional paper tape input/output facilities are required on the 905 computer, a second paper tape station may be fitted. The second paper tape station consists of a standard 900 Series cabinet containing a second paper tape controller and a second channel interface unit. It may be fitted with one or any combination of the following: a paper tape reader reading at 250 c.p.s or one reading at 500 c.p.s; a punch operating at 110 c.p.s; or a teleprinter.

Operation

The second paper tape and teleprinter station operates in an identical manner to the basic paper tape and teleprinter station, except that special program instructions are used to communicate with it. When a second paper tape station is fitted, there will also be a manual selection facility fitted on the Interface Unit to enable the engineer to override selection of the controller by the program.



Paper tape and teleprinter control panel



Westrex Teleprinter

Packaging

The second paper tape station, with its interface unit and controller occupies its own cabinet, which is connected to the basic paper tape station cabinet by a cable up to 20 feet long. Tape exit from both readers and punches is to the left of the cabinet. Mains power is supplied to each cabinet.

905 LINE PRINTER

General

The 905 line printer is based on the Potter Chain Printer HSP 3502/A and provides a means of outputting information from the computer in printed form at high speed. This line printer differs from other types in that the characters are carried past the paper on a horizontally moving chain, instead of being engraved many times over (one per column) on a rotating drum.

This has two main advantages. Firstly, a very wide character set may be accommodated since the chain can hold up to 192 different characters. A wide range of standard characters is available and this repertoire is constantly growing. It is possible to interchange character sets. Secondly the horizontal chain movement gives extremely good vertical alignment of characters at the expense of some slight worsening of the less critical horizontal alignment.

The printer speed varies with the number of different characters in the character set. If a full 192-character set is specified, it appears once on the chain belt. If a smaller character set is specified, this may be repeated along the chain belt, allowing several lines to be printed during each print cycle. The standard character set size is sixty-four, repeated three times round the chain, giving a printing speed of 315 lines per minute. Printing speeds for other sizes of character set are given below.

The 900 series chain printer system comprises a cabinet containing the mechanism and associated logic, and a cabinet containing the controller. The controller is designed to operate from the standard 900 Series Peripheral Interface.

Operation

The printer controller contains a buffer, which is filled with 8-bit characters transferred from the computer. Printing takes place in two stages with firstly the characters in the odd positions being printed, followed by those in the even positions.

A control word may be output to the printer specifying whether interrupts are to be inhibited or not, and giving paper movement instructions.

If interrupts are permitted, they occur when both printing and paper movement operations are completed. Interrupt level 2 is normally used.

The printer will always operate in Automatic Line Feed mode unless a control word is issued specifying otherwise. In Automatic Line Feed mode one line is advanced after each line has been printed. Alternatively, the printer may set to one of the following modes:

a) *Paper slew:* A specified number of lines is skipped at high speed. A zero line slew can be specified if over printing is desired.

b) *Top of form:* The paper is advanced to the top of the next form.

c) *Channel 1 format:* Channel 1 of the format control tape determines the paper movement (see CONTROL section below).

A status word can be read by the computer from the printer controller, indicating the current state of the printer.

Control

The printer incorporates an Internal Format Control comprising a simple four-channel perforated tape which may be used to control the paper movement. It is used to indicate the positions of the last line on a form, and the top of form. It may also be used in conjunction with channel 1 format instructions to control page layout.

The following control switches are provided with the printer:

TOP OF FORM To position paper for printing the first line.

LINE ADVANCE For stepping the paper a line at a time.

PRINT START To make printer on-line to the computer.

PRINT STOP To make printer logic off-line to the computer.

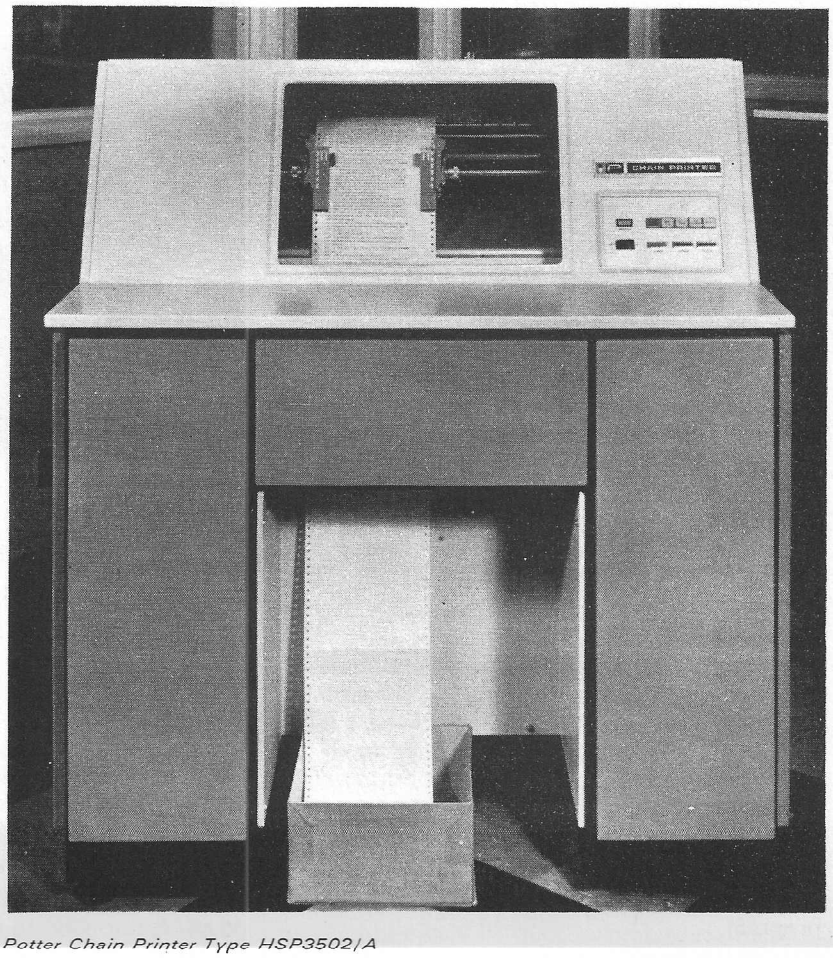
RESET Sets all logic circuits to their initial states.

ON-OFF Switches printer dc power supply.

Lamps are provided to indicate dc power on, ribbon out and paper or carriage out states.

Packaging

The 905 line printer consists of a printer cabinet containing the print mechanism and associated logic, and a controller cabinet. In a standard system the controller is housed in a standard cabinet, where floor space is at a premium.



Potter Chain Printer Type HSP3502/A

Characteristics

Number of characters: 192 maximum, 64 standard.

		Number of characters	Lines/minute
Printing speed:	Standard:	49– 64	315
	Options:	1– 16	800
		17– 24	650
		25– 32	540
		33– 48	400
		65– 96	225
		97–192	120

Column width: 132 columns standard.

Print spacing:	10 columns/inch.
Line spacing:	6 lines/inch.
Paper width:	4·0in to 18·5in.
Number of copies:	Up to 6.
Paper slew speed:	16·5in/second.
Format control:	Continuous 4-channel tape loop, or from computer.
Ribbon:	0·75in ribbon.
Standard code:	900 Series internal (6-bit) character based on the seven-track ISO telecode
Mains supply:	230V, 50Hz.
Dimensions:	Height: 127cm (50in). Depth: 82cm (32in). Width: 115cm (45in).

905 DIGITAL PLOTTER

General

The 905 Digital Plotter allows output data from the computer to be presented in the form of a permanently recorded graph, chart or diagram complete with annotations, where required. There are several models available, differing from each other mainly in respect of step size and plotting width. Data are recorded incrementally, and 18,000 or 36,000 increments can be made per minute.

The Digital Plotter may be connected direct to the peripheral sockets or via a multiplexer.

Operation

In response to computer instructions data are recorded incrementally by the plotter by means of a pen which can move horizontally across a paper plotting surface which itself can move at right angles to the pen. Thus the pen may move to the left or right, and the paper may move forward or backwards.
A single increment on the paper can, by a combination of any of these movements, be in any one of eight directions. A continuous trace can be drawn as a series of correctly directed increments. The pen can be raised from the paper and lowered under computer control.

Control

The plotter is provided with a power on/off switch and a MANUAL/AUTO button.
When the plotter is in MANUAL the pen can be positioned by using a joy stick control. The pen can also be raised or lowered under manual control.

Packaging

The plotter is contained in a compact unit which is mounted on a specially designed mobile stand.

Characteristics

The following models are available:

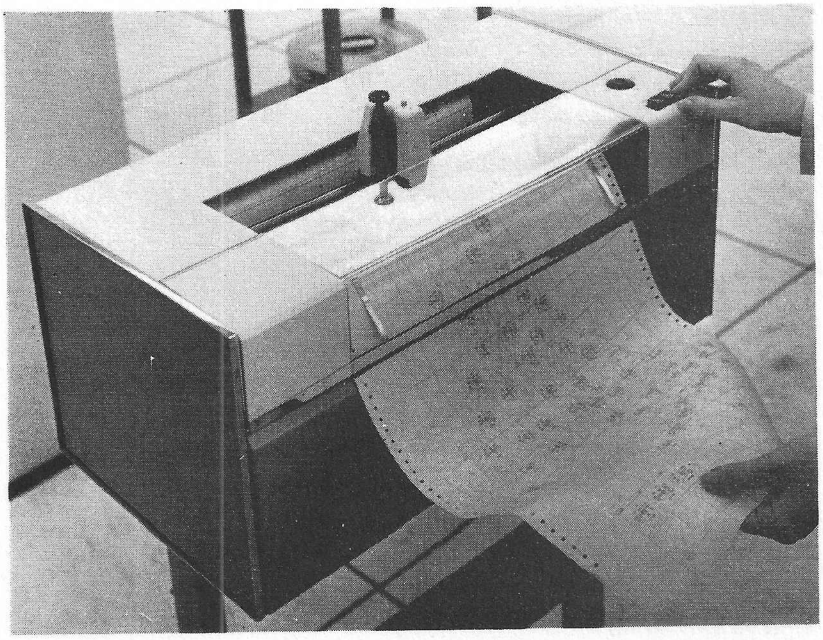
	Chart width	Plotting width	Step size
Model 1	36cm (14·171in)	33cm (13·125in)	0·12cm (0·005in)
Model 2	36cm (14·171in)	33cm (13·125in)	0·025cm (0·01in)
Model 3	36cm (14·171in)	33·3cm (12·125in)	0·01cm (0·004in)
Model 4	77cm (30·5in)	71·8cm (28·25in)	0·012cm (0·005in)
Model 5	77·5cm (3in)	71·8cm (28·25in)	0·01cm (0·004in)

Plotter speed: Models 1, 2 and 3:
Auto 18,000 steps/minute.
Manual 120 or 15,000 steps/minute.
Models 4 and 5:
Auto 36,000 steps/minute.
Manual 240, 9000 or 60,000 steps/minute.

Accuracy: When the correct type of paper is used under constant environmental conditions, the plotter will lose no more than one step in 10^4 reversals.

Mains supply: 230V, 50Hz.

Dimensions: 34cm model
Height 105·4 (41·5in)
Depth 31·8cm (12·5in)
Width 62·3cm (24·5in)
75cm model
Height 114cm (45in)
Depth 48cm (19in)
Width 143cm (56·25in)



34cm Plotter providing meteorological data output

MAGNETIC DISC STORE

General

The 905 Magnetic Disc Store provides a large capacity high-speed, random-access backing store for 905 computers. These stores are based on the Burroughs Model 9370–2 magnetic disc system.

The disc system comprises a controller and one or two 9370–2 dual surface non-replaceable disc units, each with a capacity of 896,000 18-bit words. The disc units are equipped with fixed read/write heads (one head per track), read/write amplifiers and head selection and logic electronics. Data are stored serially on concentric tracks.

Operation

The disc controller is connected directly to the 905 store highway (without the interposition of an Autonomous Transfer Unit), data transfer instructions are loaded into the controller from the Core Store. Transfers take place autonomously between the Disc Store and the Core Store. A connection is also made to the peripheral interface for initiates and interrupt signals.

At the end of an operation the disc issues a 'Ready' signal to which the computer responds either by initiating another transfer or by prohibiting the disc ready until a further transfer is required.

The segments are numbered through consecutively and can be accessed by word addresses. Switching between tracks occurs automatically, without loss of time. A transfer may start on one track and finish on another track, even when the first and last words transferred are on different units.

Packaging

The disc mechanism is housed in a special cabinet, and the control electronics are supplied as standard 19-inch rack mounting.

Characteristics

Instantaneous data transfer rate:
Exceeding 130,000 words per second.

Average access time: 17·5 milliseconds.

Rotation speed, nominal:
1745 revolutions per minute.

Number of disc units:	1	2
Data tracks:	200	400
Capacity in 18-bit words:	896,000	1,792,000
Words per track:	4480	4480
Data segments per track:	70	70
Words per data segment:	64	64
Total data segments:	14,000	28,000

Power supply: 230V, 50Hz.

Dimensions (excluding controller):

Height: 114cm (45in).

Depth: 115cm (45·5in).

Width: 51cm (20in).

SERIES 20 C.R.T DISPLAY SYSTEM

General

The Series 20 C.R.T Display System provides an exceptionally wide and flexible range of display equipment and forms a powerful display satellite for connection to a larger central processor.

The system consists of a range of display modules which centre round a self-contained Display Controller. This may be attached to the computer directly, via a buffer store or via a data link. Modules that may be used to build up a system include three sizes of viewing unit, light pens, buffer stores, keyboards and keyboard controllers and 905 Interface matching units. Matching units are available to provide compatibility with computers from other manufacturers.

Viewing unit modules

Two display sizes are available, 11- and 17-inch rectangular, intended for individual and distant viewing respectively. The cathode ray tubes employ a standard gun with electromagnetic deflection and electrostatic focussing. Either K7 green or 14 amber phosphors may be specified, giving a recommended refreshing rate of 25 and 12·5 times per second respectively. B4 phosphor is provided for light pen sensing. Tabular data are arranged on each viewing unit in any number of lines up to a maximum of sixty-four, with a maximum of sixty-four characters per line.

Display controllers

A single controller can drive up to eight displays which may be at distances of up to 1000 feet away. The controller is connected to the computer directly or via a buffer store. It gives program control over display selection (any combination of eight), screen position selection (any position on a 64×64 grid), picture format (up to sixty-four lines per display and sixty-four characters per line), writing order (tabular, random or mixed) and facilities such as size and brightness of characters, and whether they are to be shown steady or flashing.

Each character or symbol is composed of up to twenty-five equal increments on a grid of 5×5 lines. The character to be displayed is generated by moving the c.r.t. electronic beam at constant speed in any of sixteen directions, from one point in the grid to another. The Mackworth style of print has been chosen as it is universally agreed to be the most acceptable to an operator and is free from any distracting dot or raster effects. Characters may be displayed in one or two sizes and two levels of brightness. Large characters take 20 microseconds to write, and small characters 10 microseconds. Intercharacter positioning time for tabular output is 4 microseconds, and every new position and every flyback require busy periods of 60 microseconds.

Two types of controller are available for the connection of up to eight displays for the display of tabular information. The first provides a 60-character repertoire, and the second a 120-character repertoire, which includes lower-case characters. Both these controllers have a 6-bit discrete component interface, and are connected to the 905 computer via one of the cyclic buffer stores described below. An 18-bit micrologic interface display controller is also available which can be connected directly to the 905 peripheral sockets. One or two displays can be connected via this controller, which provides a repertoire of sixty characters.

Graphic facilities are offered by a special graphics processor, but simple diagrams can be constructed with the standard character repertoire by combining diagram segments which are part of the repertoire.

The Display Controller also provides facilities for the connection of up to eight light pens (two in the case of the 18-bit controller). The controller provides screen position information to the computer when light pen pulses are received, thus allowing the operator to describe a particular part of the display to the computer program by pointing at it.

Series 20 Display – 11-inch version

Buffer stores

An 8192 6-bit character cyclic store is provided for use as a buffer between a central processor and a 6-bit interface display controller. This takes over the work of refreshing the display from the central processor. The store is normally loaded from the central processor and outputs its information in a cyclic manner to the display controller. It also has the facility for allowing direct data transfers from the display controller to the processor.

Keyboards and keyboard controllers

Two standard keyboards are available, one with a 60-character repertoire, and the other with a 120-character repertoire. These are connected to a computer system via a keyboard controller, which can accept inputs from up to eight keyboards, which may be at distances of up to 1000 feet away.

When a key is pressed on any keyboard an interrupt is sent to the computer. The computer then reads from the controller a control word identifying the keyboard in use and a data word giving the key code. The interrupt is not removed until all keyboards which have been pressed have been read on a sequential basis, controlled by a scanner in the keyboard controller. Alternatively the controller can be read at fixed intervals, and the first bit of the control word used to determine if a key has been pressed.

Interface Matching Units can readily be supplied for other manufacturer's computers.

Packaging

The viewing units are available either as free-standing table top units, or as units suitable for mounting in standard 19-inch racks. The store and control modules are all designed for 19-inch mounting and can be house in a standard 900 series cabinet.

Characteristics
Viewing unit

The display format can be up to sixty-four lines, of sixty-four characters on each line, and 11-inch, 17-inch sizes are available. The cathode ray tubes employ a standard gun with electromagnetic deflection and electrostatic focusing and alternative phosphors are available.

Display controller

Two standard units are available, with either sixty or 120 character shapes, the extra sixty in the latter case being selected by shift in and out codes.

The controller operates on digital information in the form of 6-bit codes which define:

the DISPLAY or displays to which the output is addressed,
the POSITION on the screen of each character,
the SIZE and BRIGHTNESS of the characters,
the CHARACTERS required.

Simple mimics and graphs are part of the basic system, so that flow diagrams for instance can be output, amended and automatically recorded.

Characters can be double size, extra bright, flashing or italics, the choice being under software control. Lower case facilities are also available.

Units are self-contained, requiring only mains power, and will drive up to eight viewing units.

Light pen

A light pen can be added to the basic system, enabling light-pen signals to be converted into display and screen position data for use by a computer.

Keyboard

Standard 60-shape or 120-shape keyboards are available, with keys for controlling a cursor on the display screen for entering and recalling data. A single keyboard can be connected directly into the system, or up to eight keyboards can be controlled through a keyboard controller.

Cyclic store

The standard cyclic store unit is designed to supply the display controller. Operation on 6-bit control words, it has store capacity for 8192 characters or control codes in a ferrite memory.

Interface

The interface logic of the cyclic store and display controller modules is designed to accept 6-bit words for both data and control. Standard interfaces are available in micrologic form for the 900 range computers, or in discrete component form for the 4100 Series, while matching units are available to provide compatibility with computers from other manufacturers.

Power requirements

110–120V, 45–65Hz.
220–250V, 45–65Hz.

Mechanical design

All units are of chassis construction and can be supplied as follows:
for standard 19in rack mounting;
for mounting in customers own consoles;
with covers for free standing applications;
ready mounted in standard consoles;
as complete custom-built units for specific installation.

Specification

This equipment is manufactured to the highest commercial standards. The electronics meet Air Registration Board, Military, Naval and CEGB Category 4 specifications, and complete systems are available suitably packaged for such applications.

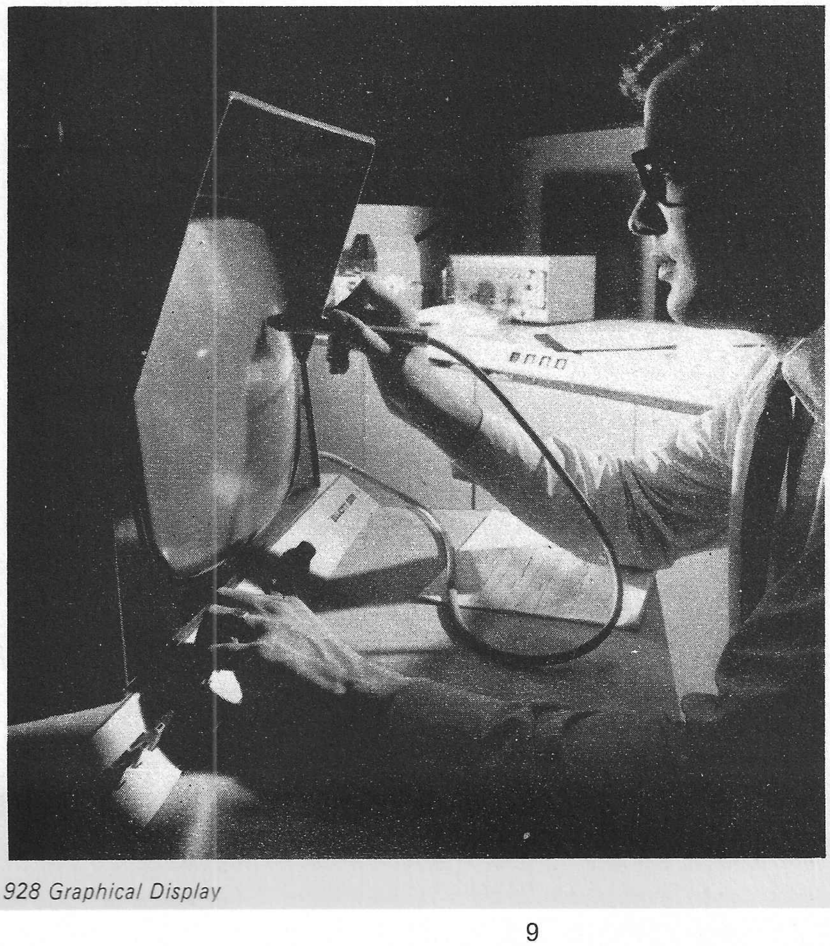
928 GRAPHICAL DISPLAY

The 928 Graphical Display system is a powerful graphical processing system. It operates in association with a 905 computer which provides the computation power necessary for graphic manipulation and for the related calculations. The system includes a graphic console with a light pen, character, vector and arc generators, a graphic control unit, and a keyboard. An extensive graphical programming repertoire complements the hardware. A full range of display capabilities can be performed including circles, enlargement, contraction and rotation about the X, Y or Z axis.

The 928 display has been developed as a satellite to central processors of all makes. Having its own compact computer to perform all the routine tasks concerned with the display manipulation eliminates the problem of surrendering store capacity and time in the parent computer to these duties. All information necessary for solving the problem is stored in the parent computer, and only the specific information needed to display a picture to the user need be transmitted to the 928. The user may modify the displayed image by use of the light pen and when he is satisfied with the revised pattern the 928 can communicate the revision to the parent computer which will up-date its stored information accordingly.

Characteristics

Number of cabinets and size: Two cabinets each 1067mm (42in) wide × 660mm (26in) deep × 940mm (37in) high.



928 Graphical Display

Viewing unit 737mm (29in) wide × 1041mm (41in) deep × 1245mm (49in) high.
Teleprinter 610mm (24in) wide × 610mm (24in) deep × 1041mm (41in) high.

Construction: Logic is monolithic circuits.
Temperature limits: 0°C to 40°C.
Power consumption: 3kVA.
905 store size: 8192 words basic, expandable in 8K or 16K modules up to 128K words.
word length: 18 bit.
cycle time: 1 μs.
928 Cathode Ray Tube size: 17in diagonal.
principle: direct scan.
visible picture area: 10in × 10in.
total picture area: 80in × 80in.
raster size: 1024 points × 1024 points.
phosphor fall-off period: 160 milliseconds.
regeneration rate: 10 times per second.
software: full graphical software support is provided as standard for Algol, Fortran and assembly code.
character generation: 64-character set standard.
128-character set optional.
all characters in two sizes.
vector generation: any direction; components in the range −4096 to +4095.
arc generation: any arc of circle.
speed: visible vectors at 0·75 μs per increment.
characters at 8 to 35 μs.

VIDEODATA 4000

The Marconi-Elliott VIDEODATA 4000 terminal consists of a data entry typewriter keyboard and a cathode ray tube display unit containing integral storage, character generation and data transmission interface. By typing on the keyboard an operator may compose messages for transmission to a remote computer, checking and correcting the data before transmission by means of the built-in text-editing facilities. Having successfully transmitted the message, the terminal will receive computer replies, performing full error correction in the process and display these data on the screen. By means of special control codes, the computer has complete control over the positioning of text on the terminal screen, and may cause data to be presented in page form or rolled up and down the screen a line at a time from any line. Similarly, the screen may be split thus allowing several sets of independent data to be simultaneously serviced.

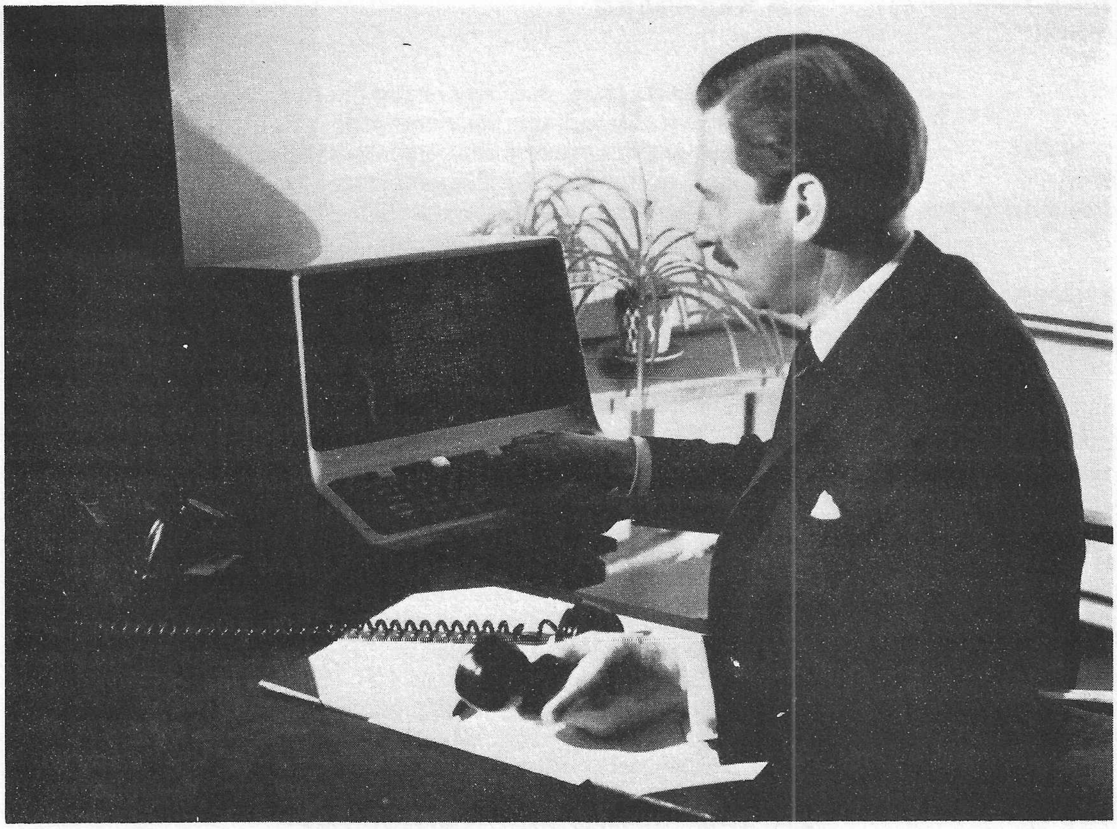
Used in its format mode, the terminal presents tabulated formats containing fixed and variable data fields and the operator may fill in the variable fields using the keyboard. On transmission the terminal transmits only variable fields, thereby effecting considerable economies in line time. By use of the selective retransmission facilities, an operator may be led by programmed steps, through a series of decision tables culminating in a specific task or a block of information of manageable proportions. The provision of remote text-editing and manipulation control permits data file searches to be carried out economically and the flexibility and speed of such sub-routine working makes possible some highly sophisticated man-machine interaction.

Video terminals

The VIDEODATA 4000 range consists of nine basic models offering three choices of character capacity and three methods of data transfer. All models have a full 64-symbol character set and a complete range of cursor movement and text-editing keys. Terminals are equipped with integral storage, character generation, transmission interface and a standard keyboard. Data rate selection and setting-up controls are fitted internally, modem and power connections being made at the rear of the unit. An operator brightness control is provided at the rear right-hand side and a mains on/off switch is mounted on the keyboard. The component modules of the terminal are housed within an attractively styled two-piece case, the top being removable for maintenance access.

Line expander

This unit provides a common connection point when a number of terminals are to share a transmission line or data channel. It has a basic machine capacity of sixteen terminals, each terminal being located at a maximum distance of 2000 cable feet from the modem



Videodata 4000

or computer. Where data traffic conditions permit, additional line expanders may be connected up to a maximum capacity of ninety-six terminals. The unit consists of two basic modules, one comprising chassis, power supplies and modem drive circuits, the other individual drive circuits for each terminal in the configuration. Thus the system may be constructed to service the precise number of machines and has a built-in capability for future expansion. By use of a general poll option, savings in line time may be effected by relieving the remote computer of the task of polling individual terminals.

Data adapters

The VIDEODATA 4000 range provides two versions of data adopter. The asynchronous unit performs character serializing at 600 or 1200 baud and is suitable for use with the GPO Modem No. 1 Model 5 or equivalent. It will connect via a suitable interface unit or satellite computer to the main frame processor multiplexer or selector channel. The corresponding synchronous unit provides transmission and reception at 2400 bits per second and is suitable for use with the GPO modem No. 7 or equivalent.

Hard copy

By use of the auxiliary interface, which is common to all VIDEODATA 4000 terminals, information may be transferred at low speed to a local Teletype or equivalent hard copy device. The transfer takes place via a 7-bit parallel interface in an asynchronous manner on a demand response basis.

Bulk storage

The addition of an optional auxiliary input such as a cassette tape transport to be fitted to the terminal. This will provide for large quantities of input data to be assembled off-line for later data transmission. It may also be used for on-line logging or as a source of fixed format information.

DATA SUMMARY

Display format

		Model No.	
	4020	4050	4090
No. of characters displayed:	288	576	1152
No. of lines of characters:	8	16	16
No. of characters per line:	36	36	72
Display area height:	8·0cm	12·5cm	12·5cm
Display area width:	17·0cm	21·0cm	21·0cm
Character height (max.):	4·3mm	5·3mm	2·6mm
Character width (max.):	3·2mm	4·0mm	2·0mm

Character set

Alpha (upper case):
ABCDEFGHIJKLMNOPQRSTUVWXYZ
Numeric: 1234567890
Control symbols: STX ◁ ETX ▷
TAB START [TAB STOP]
Punctuation: ! " ' ( ) , . : ; ?

Graphic symbols: £ $ % & * + – / = @ ⟨ ⟩
Character code: ISO/ASCII

Transmission options:
Serial asynchronous:
Models X 4021 X4051 X4091.
Data rate 600/1200 baud.
Data structure 10 unit serial start stop.

Serial synchronous:
Models X4022 X4052 X4092.
Data rate 2400/4800 bits/second.
Data structure 8 unit serial synchronous.

Parallel:
Models X4023 X4053 X4093.
Data rate 38,300 bytes/second.
Data structure 8-bit parallel.

Display performance:
Spot diameter 0·30mm.
Display distortion 2% max.
Character brightness 50ft lamberts.
Refresh rate 30 frames/sec.min.
Phosphor P 39 (green).

Power:
Voltage 100–125V a.c or 200–250V a.c.
Frequency 45–65Hz.
Consumption 175 watts approx.

Dimensions:
Depth 69·85cm (27·05in).
Height 33·35cm (13·125in).
Width 40·64cm (16·0in).
Weight 22·67kg (50lb).

Safety: British Standard for Electrical Safety of Office Machines BS 3861.

Environment: Temperature 0–40°C.
Relative humidity up to 90%.

905 KEYBOARD

General

This keyboard system may be attached to the 905 computer for inputting alphanumeric characters and functions to the processor. It is particularly useful with the 928 graphical display. The system includes a controller which operates from the standard 905 Series Peripheral Interface. Up to eight keyboard units may be connected to the controller.

Characteristics

The keyboard has sixty alphanumeric keys and two shift keys. In addition it has twelve function keys in a separate block from the alphanumeric.

Operation

Eack key on any keyboard outputs two 6-bit words to the controller. The first 6-bit word is the control word which identifies the keyboard and defines whether it is a character code or a function code. The other 6-bit word is the data word which contains the 6-bit character code or the function code. Whenever a key is depressed, an interrupt is sent to the computer which then reads both the control word and the data word.

Packaging

The keyboard itself may be placed on any suitable working surface. The logic boards and power supply of the associated control unit occupy 22cm (8·75 inches) high by 35·5cm (14 inches) deep of 48·3cm (19-inch) rack.

Marconi-Elliott Computer Systems Limited
A GEC-English Electric Company

Elstree Way, Borehamwood, Hertfordshire
Telegrams and Cables: Elliotauto Borehamwood
Telex: 22777 Answerback: Ellauto Borhwd
Telephone: 01-953 2030