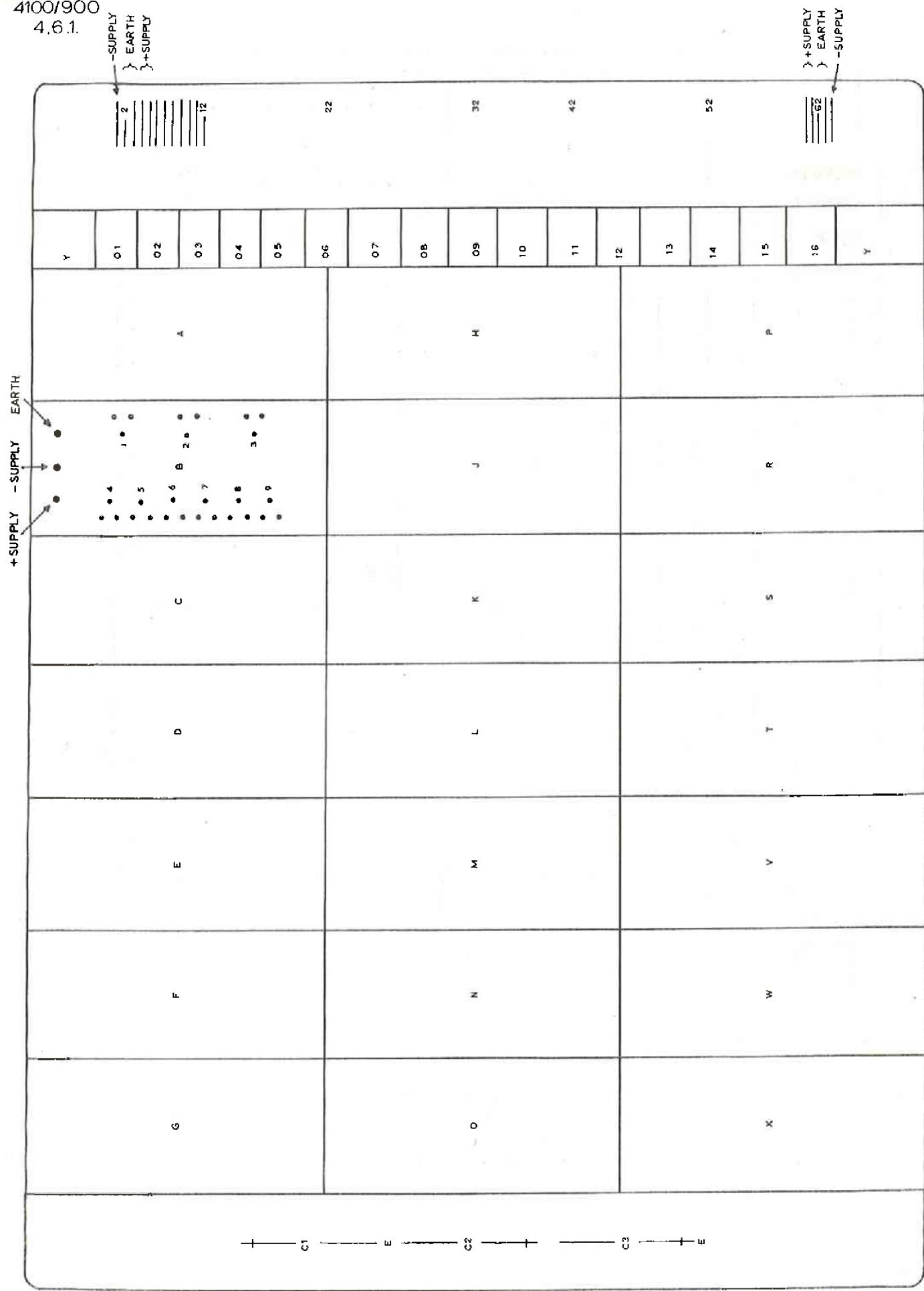


TYPICAL DP BOARD (VIEWED FROM L.S.A. SIDE)

Figure 1 (issue 1)

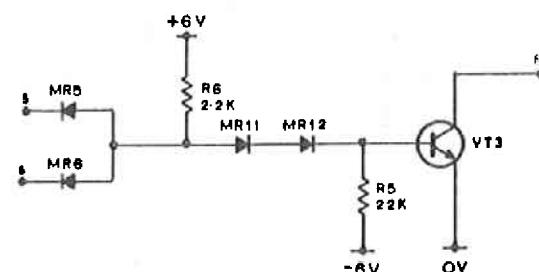
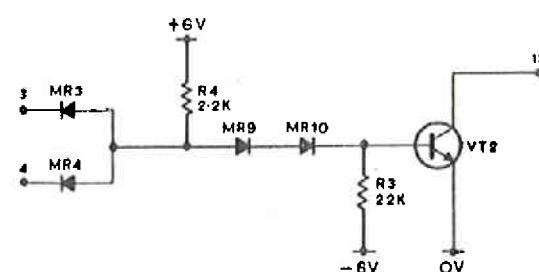
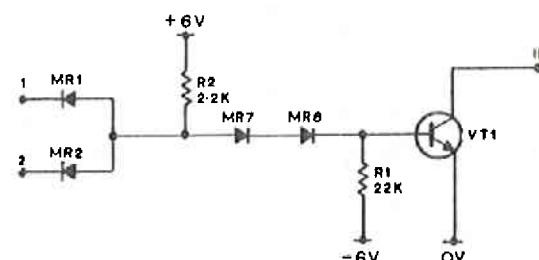
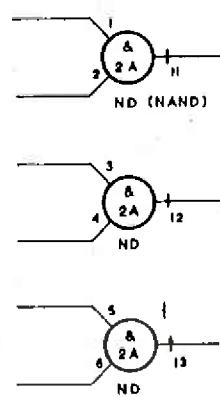
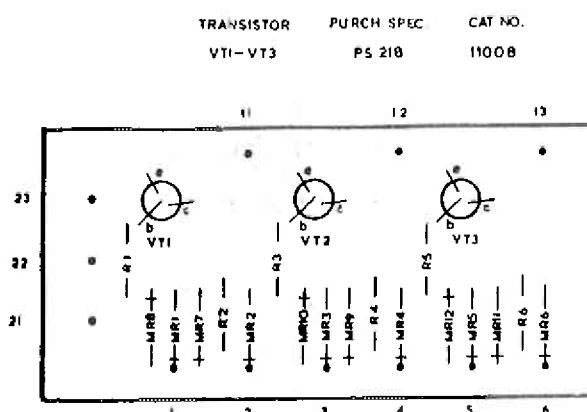
4100/900
4.6.1.



NOTE:
PAO NUMBERS IN L.S.A. AREAS ARE NON-STANDARD

Figure 2 (ISSUE 2)

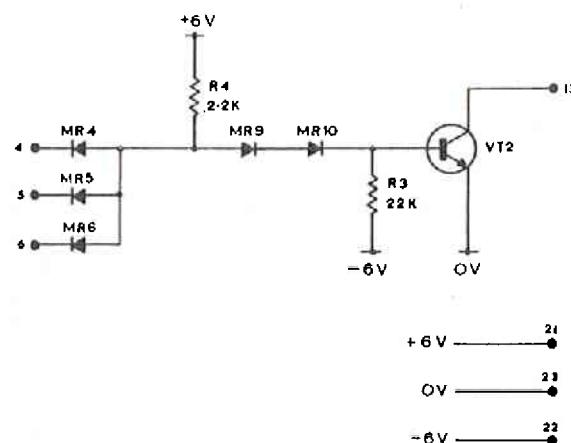
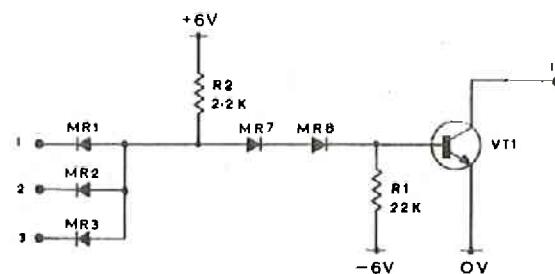
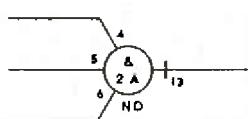
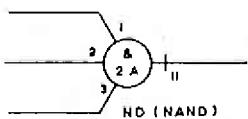
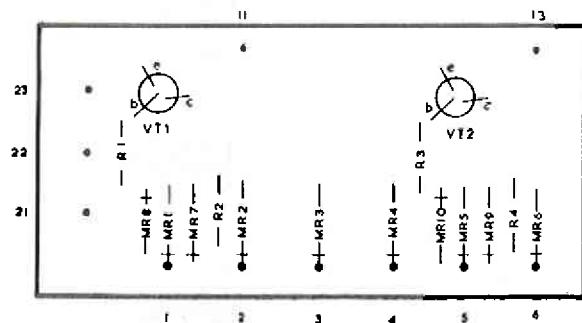
TYPICAL NV BOARD (VIEWED FROM L.S.A. SIDE)



+6V ————— 21
OV ————— 22
-6V ————— 23

| INPUT LOGIC LEVELS | |
|--------------------|--------|
| '1' | = > 8V |
| '0' | = < 1V |

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 VT2 PS 218 11008

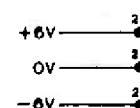
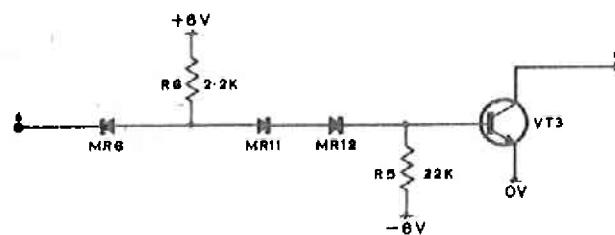
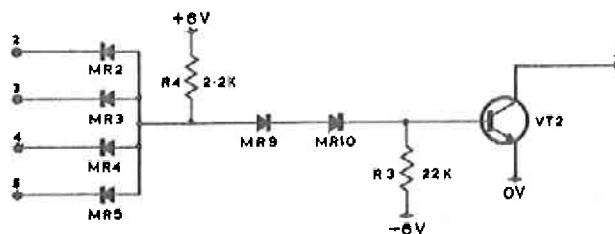
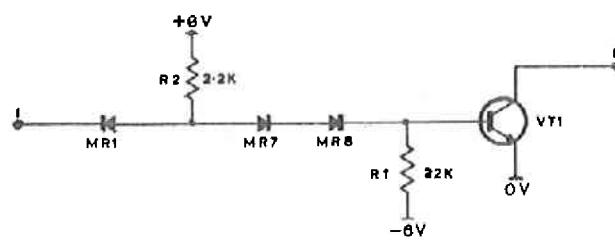
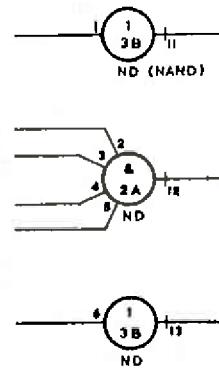
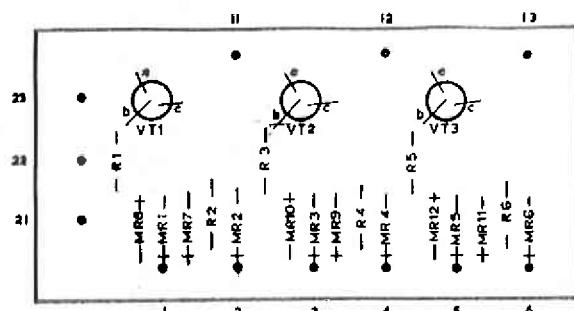


| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = $> 2V$ |
| '0' | = $< 1V$ |

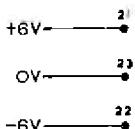
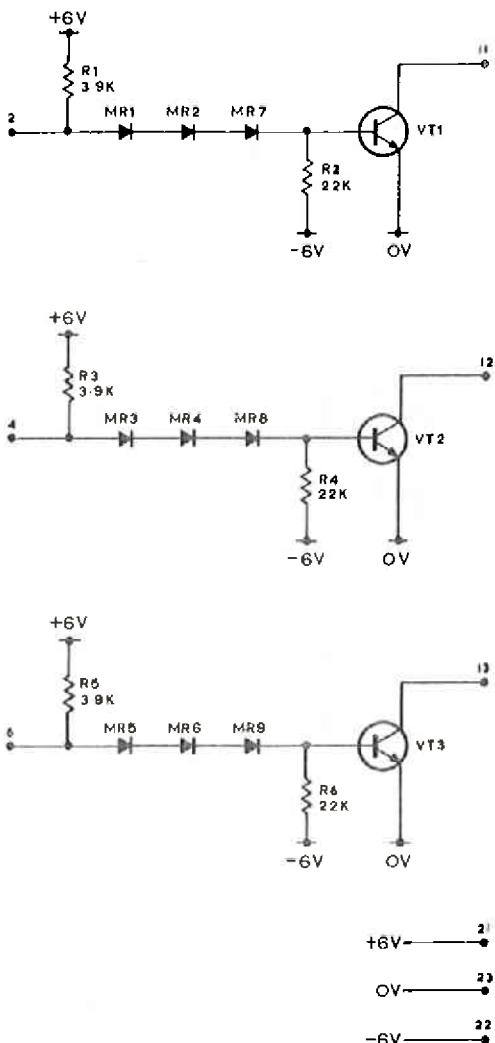
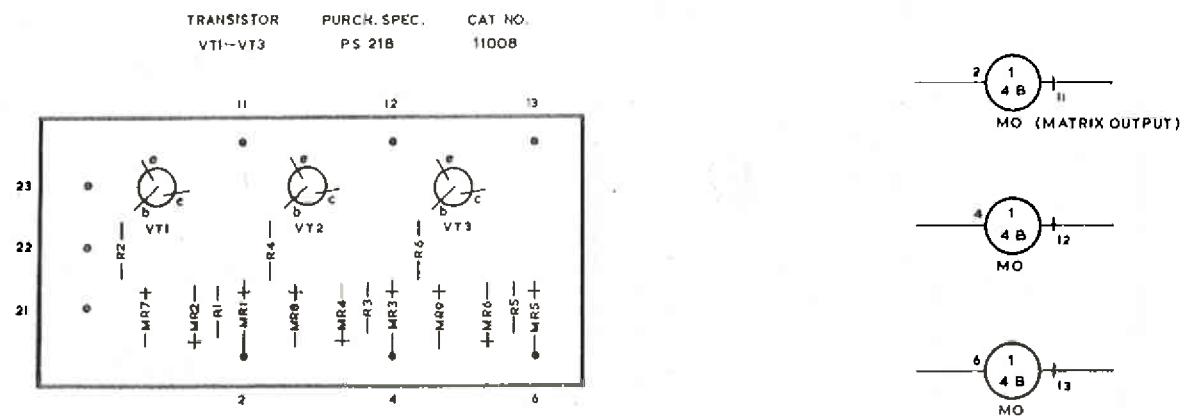
Figure 4 (ISSUE 2)

L.S.A.02

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1-VT3 PS 21B 11008

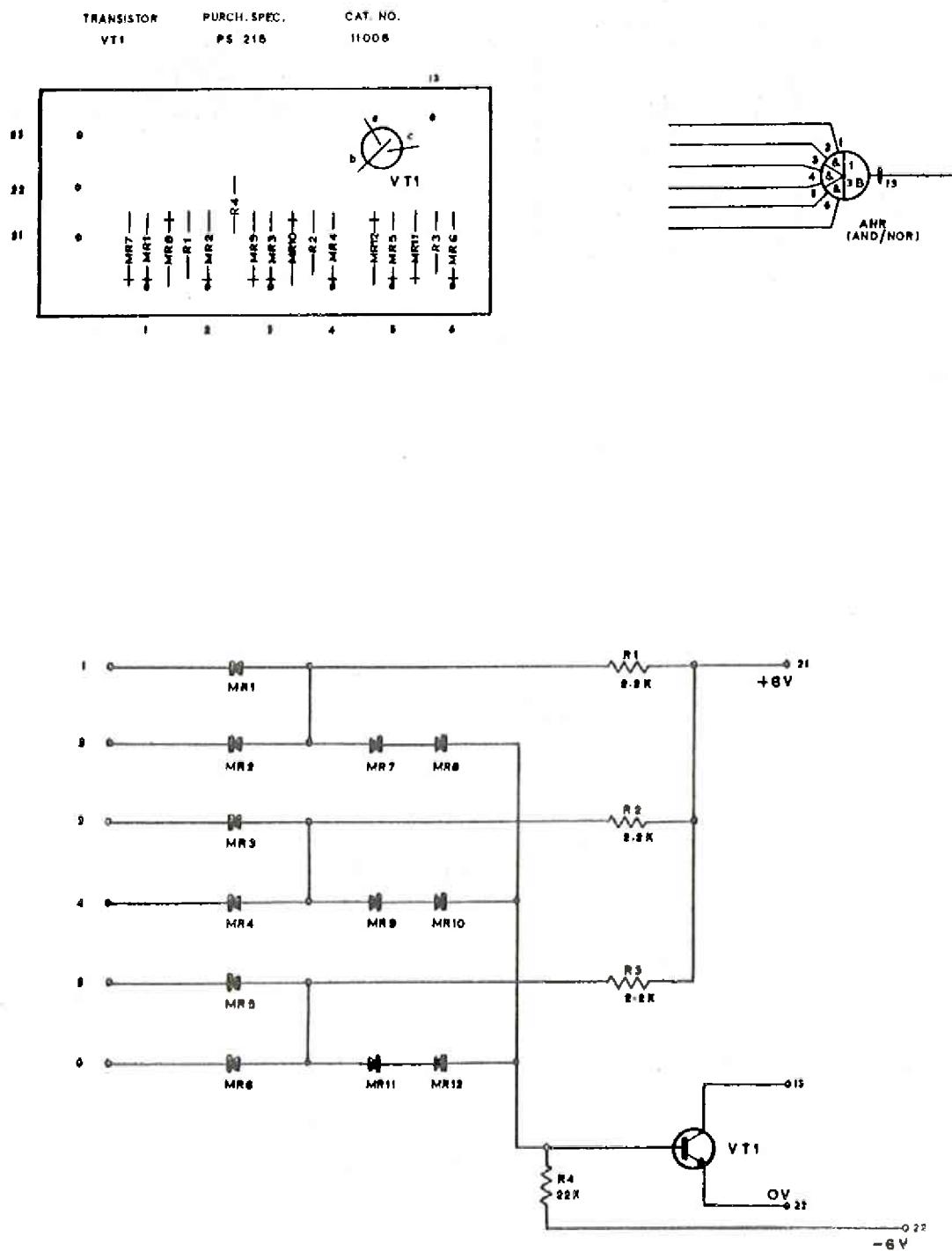


| INPUT LOGIC LEVEL | |
|-------------------|--------------------------|
| '1' | $\Rightarrow 2\text{ V}$ |
| '0' | $< 1\text{ V}$ |

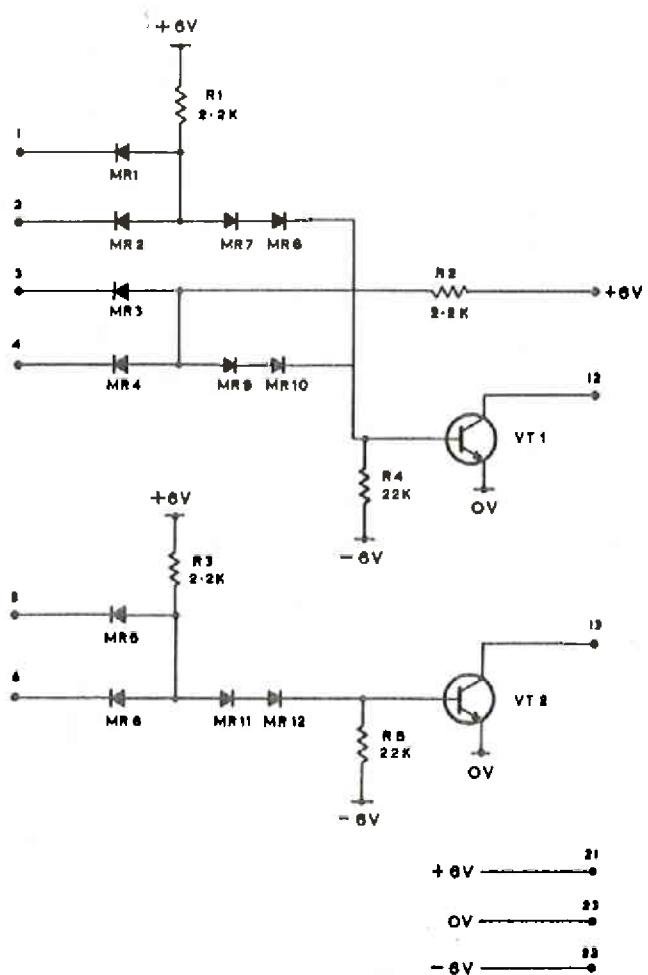
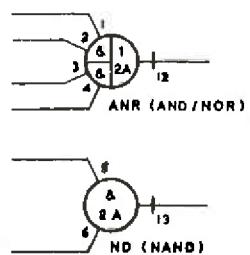
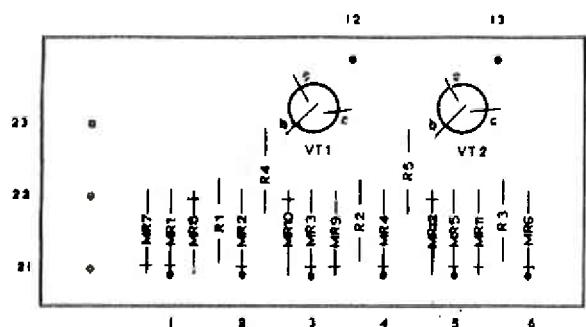


| INPUT LOGIC LEVELS | |
|--------------------|--------|
| 1 | = > 3V |
| 0 | = < 1V |

Figure 6 (ISSUE 2)



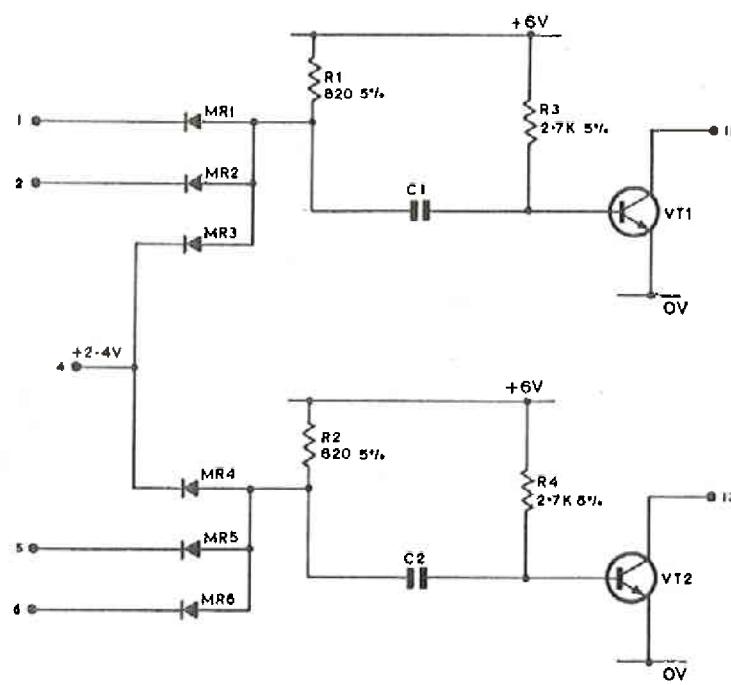
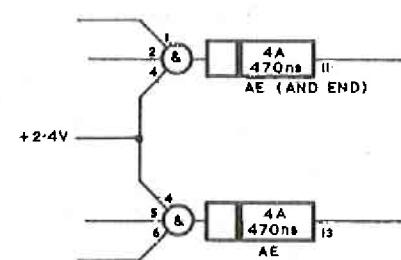
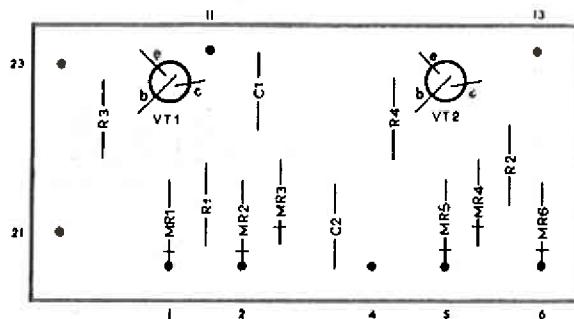
TRANSISTOR PURCH SPEC CAT NO.
VT1, VT2 PS 218 11008



| INPUT LOGIC LEVELS | |
|--------------------|--------|
| '1' | = > 2V |
| '0' | = < 1V |

Figure 8 (ISSUE 2)

TRANSISTOR
VT1, VT2
PURCH. SPEC.
PS 218
CAT. NO.
11008



| LSA No | C1 (pF) | C2 (pF) |
|--------|---------|---------|
| 07 | 100 | 100 |
| 13 | 330 | 330 |
| 137 | 220 | 220 |
| 138 | 470 | 470 |
| 34 | 100 | 330 |

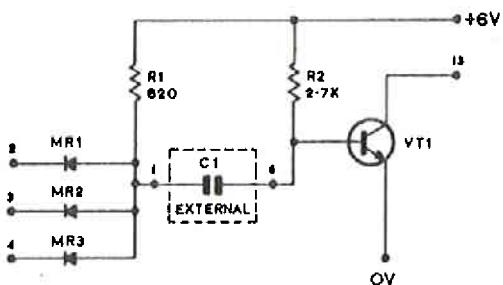
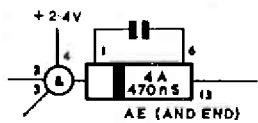
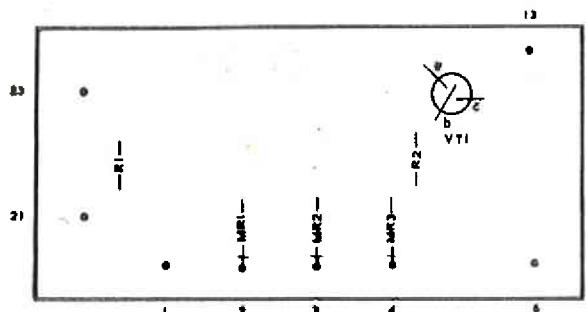
NOTES:

- (1) OUTPUT PULSE POSITIVE
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0'
PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER
THAN C/2 ns (WHERE C = CAPACITANCE IN pF)
- (3) PULSE WIDTH = Cns (WHERE C = CAPACITANCE IN pF)

+6V → 21
OV → 23

| INPUT LOGIC LEVELS | |
|--------------------|-------|
| '1' | = >2V |
| '0' | = <1V |

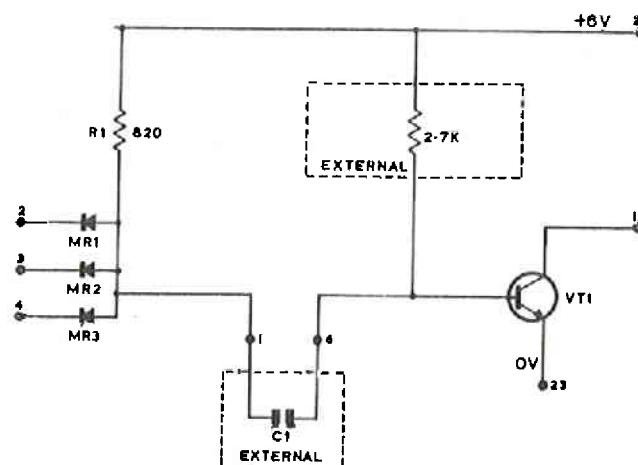
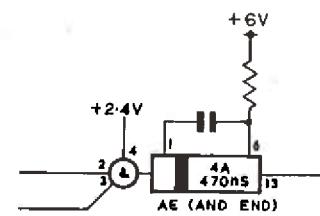
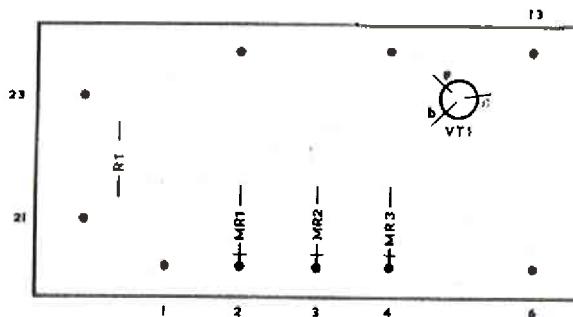
TRANSISTOR
VT1 PURCH. SPEC.
PS 21B CAT. NO.
11008



NOTES

- (1) OUTPUT PULSE POSITIVE.
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL INPUTS HAVE BEEN '1' FOR $> C/2 \text{ nS}$ (WHERE C = CAPACITANCE IN pF).
- (3) PULSE WIDTH = (CnS) (WHERE C = CAPACITANCE IN pF)
C1 WILL BE AN EXTERNAL CAPACITOR.

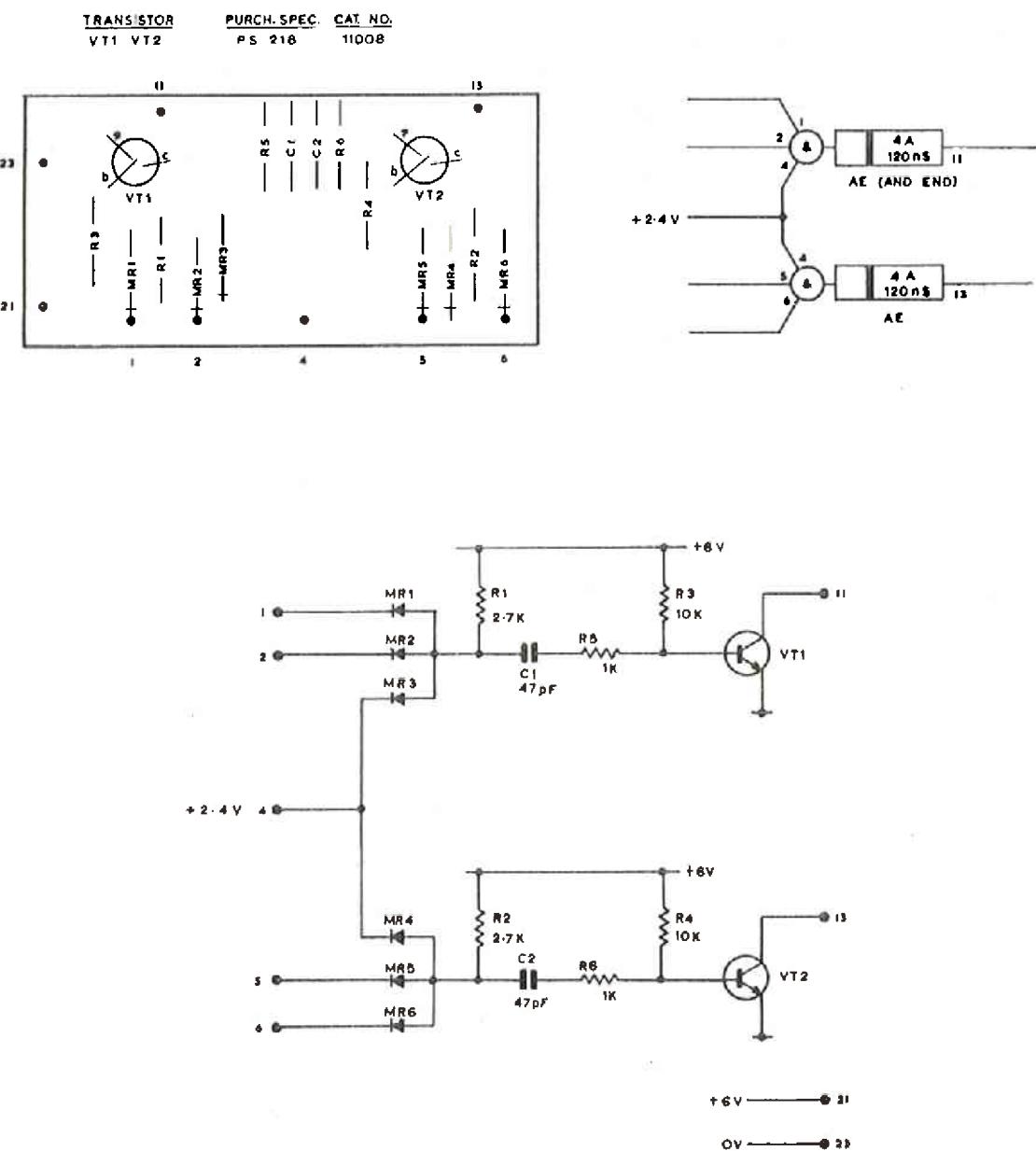
| INPUT LOGIC LEVELS | |
|--------------------|---------------|
| '1' | $> 2\text{V}$ |
| '0' | $< 1\text{V}$ |

TRANSISTOR PURCH. SPEC. CAT. No
VT1 PS 218 H1008

NOTES:

- (1) OUTPUT PULSE POSITIVE.
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR $> 1/2 \mu s$
- (3) PULSE WIDTH $\propto C \cdot t_s$ (WHERE C = CAPACITANCE IN pF)

| INPUT LOGIC LEVELS | |
|--------------------|------------|
| '1' | $\geq 2 V$ |
| '0' | $< 1 V$ |

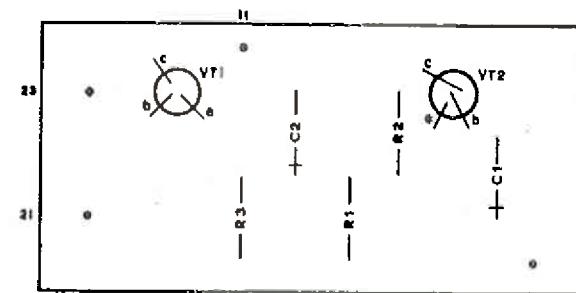
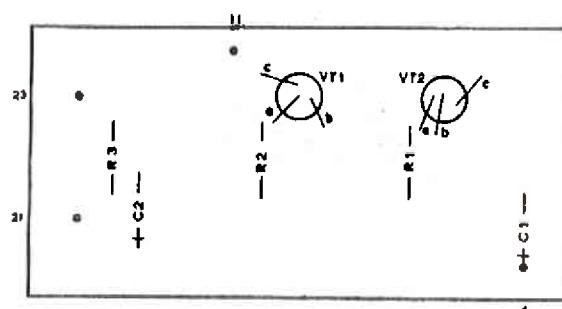


NOTES >

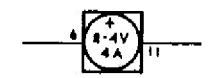
- (1) OUTPUT PULSE POSITIVE
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1' FOR GREATER THAN 80 nS.
- (3) PULSE WIDTH = 120 nS \pm 20%

| INPUT LOGIC LEVELS | |
|--------------------|-----------------|
| '1' | = $> 2\text{V}$ |
| '0' | = $< 1\text{V}$ |

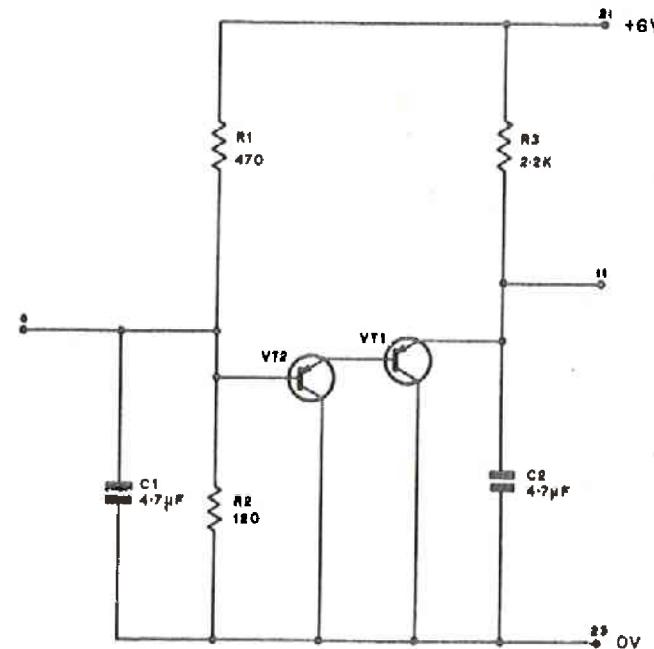
TRANSISTOR
VT₁, VT₂ CAT. NO.
 11740



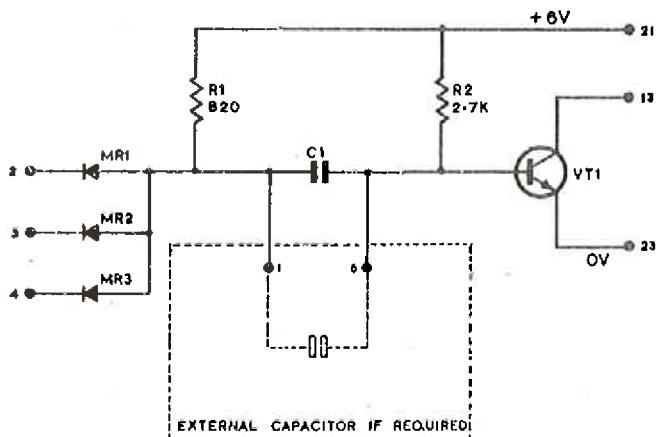
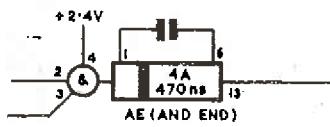
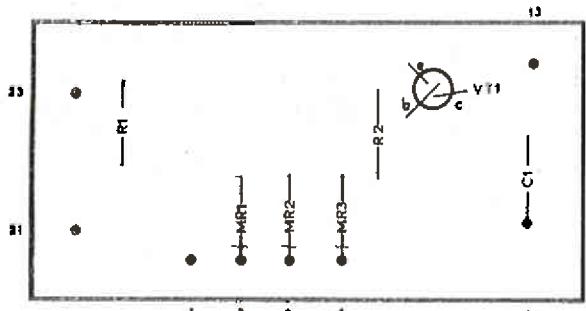
Alternative Layout.



VR (VOLTAGE REFERENCE)



TRANSISTOR
VT1 PURCH. SPEC.
PS 218 CAT. NO.
11008



| LSA NO | C1 | PULSE WIDTH |
|--------|--------|-------------|
| 09 | 470 pF | 470 ns |
| 14 | 680 pF | 680 ns |
| 130 | >22 μF | 220 μs |
| 131 | 2.2 μF | 2.2 ms |

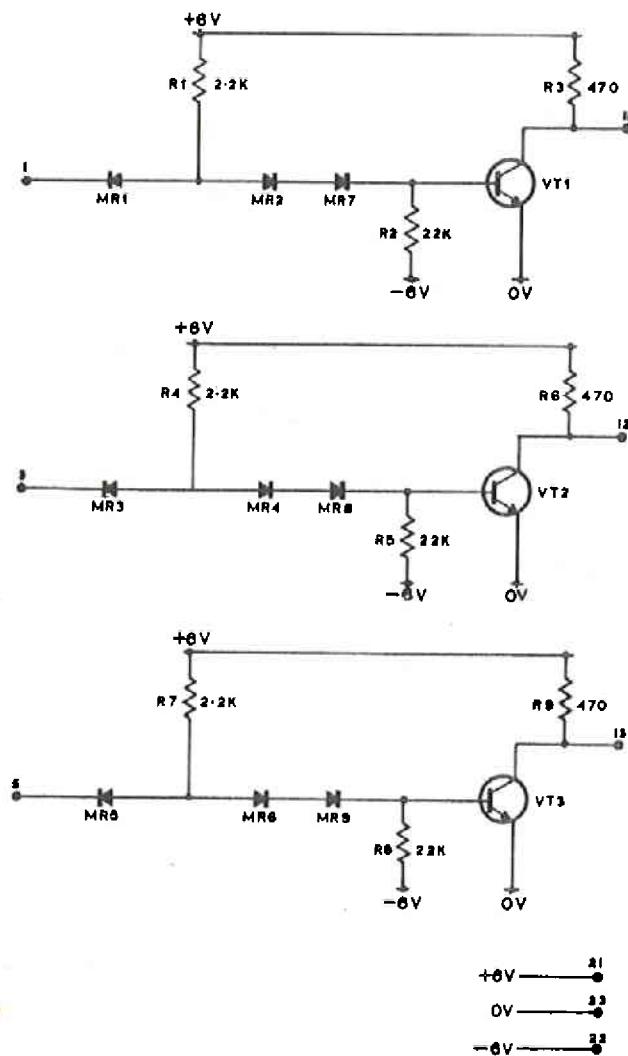
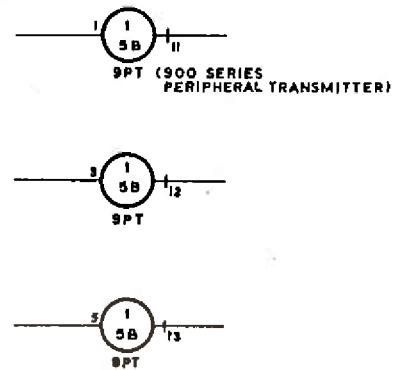
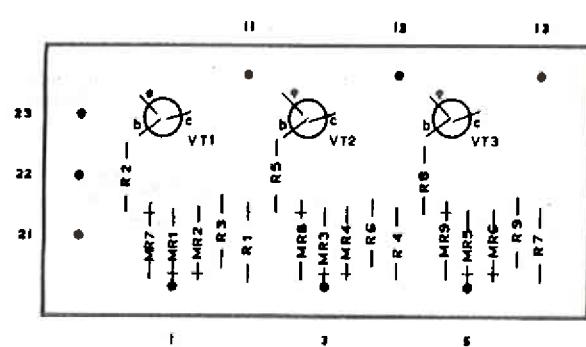
NOTES:

- (1) OUTPUT PULSE POSITIVE
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDING ALL I/P'S HAVE BEEN '1'
FOR $>C/2\pi R$. (WHERE C = CAPACITANCE IN pF)
- (3) PULSE WIDTH = C/R (WHERE C = CAPACITANCE IN pF)
- (4) C1 MAY BE INCREASED BY EXTERNAL CAPACITOR

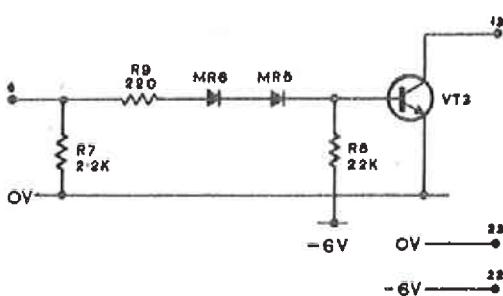
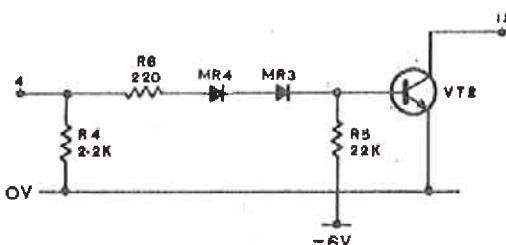
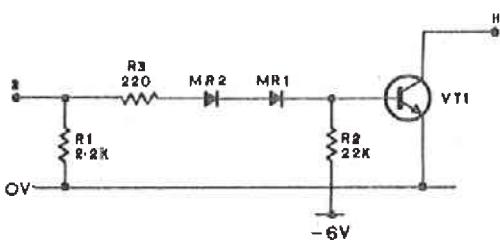
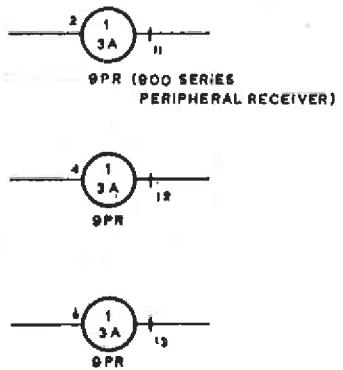
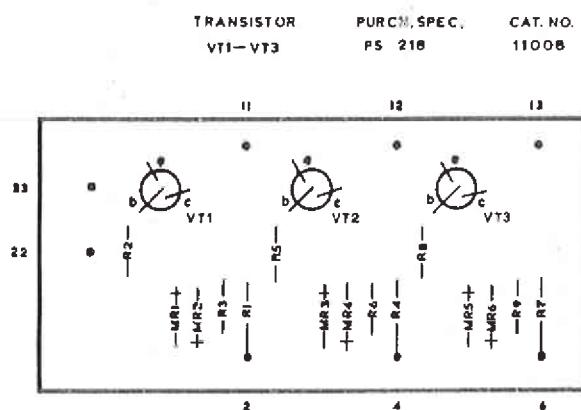
| INPUT LOGIC LEVELS | |
|--------------------|--------|
| '1' | = > 2V |
| '0' | = < 1V |

Figure 14 (ISSUE 2)

L.S.A. 09, 14, 130, 131

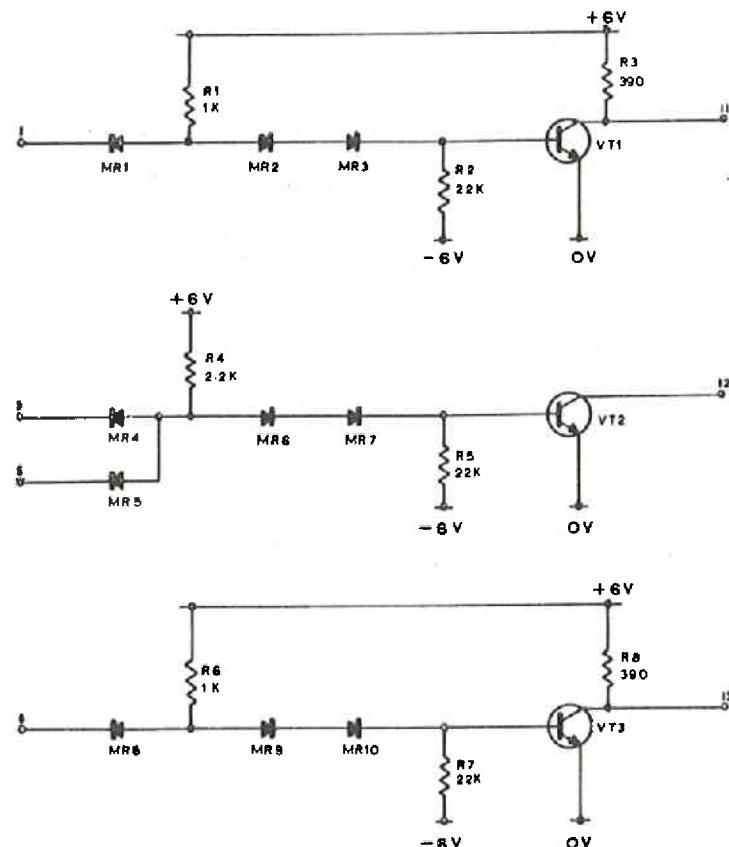
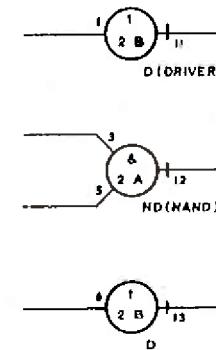
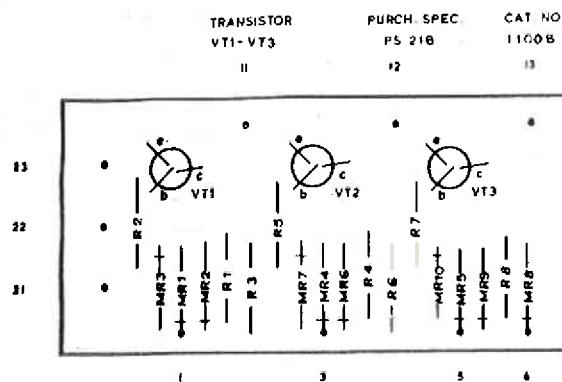
TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 218 11008

| INPUT LOGIC LEVELS | |
|--------------------|----------------|
| '1': | $> 2\text{ V}$ |
| '0': | $< 1\text{ V}$ |



| INPUT LOGIC LEVELS | |
|--------------------|---------|
| '1' | = > 3 V |
| '0' | = < 1 V |

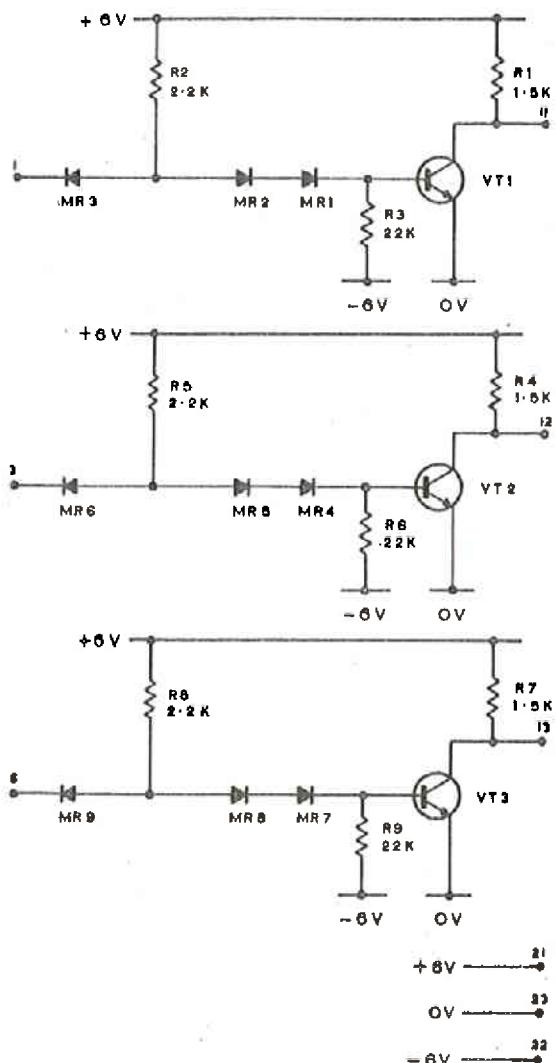
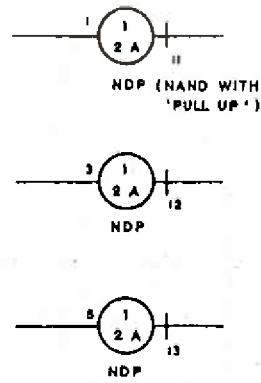
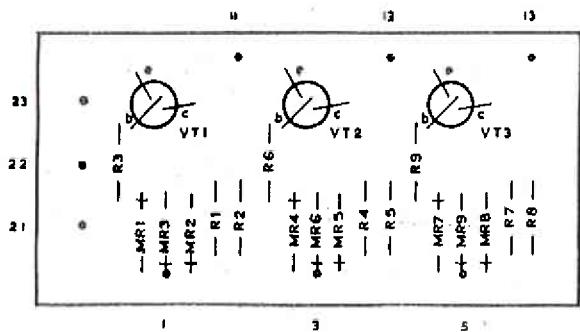
Figure 16 (ISSUE 2.)



+6V ————— 21
OV ————— 23
-6V ————— 22

| INPUT LOGIC LEVELS | |
|--------------------|--------|
| '1' | = > 2V |
| '0' | = < 1V |

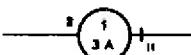
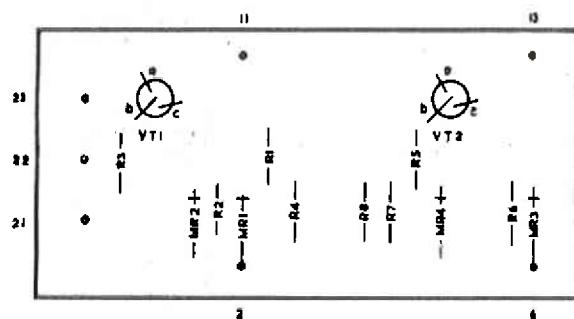
TRANSISTOR PURCH SPEC CAT NO.
VT1- VT3 PS 218 11008



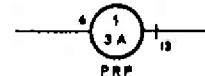
| INPUT LOGIC LEVELS | |
|--------------------|--------|
| '1' | = > 2V |
| '0' | = < 1V |

Figure 18 (ISSUE 2)

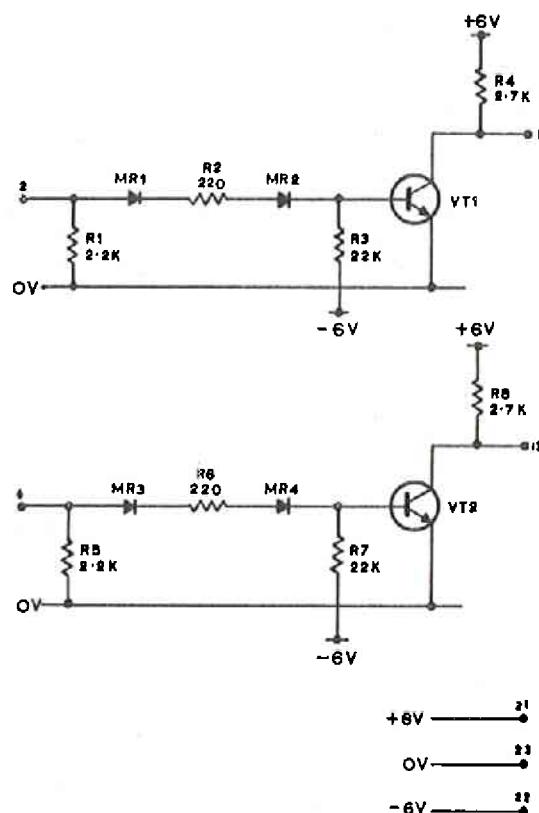
TRANSISTOR
VT1, VT2 PURCH. SPEC.
PS21B CAT. NO.
11008



PRP (PERIPHERAL RECEIVER
WITH PULL UP)



PRP



| INPUT LOGIC LEVELS | |
|--------------------|--------|
| '1' | = > 3V |
| '0' | = < 1V |

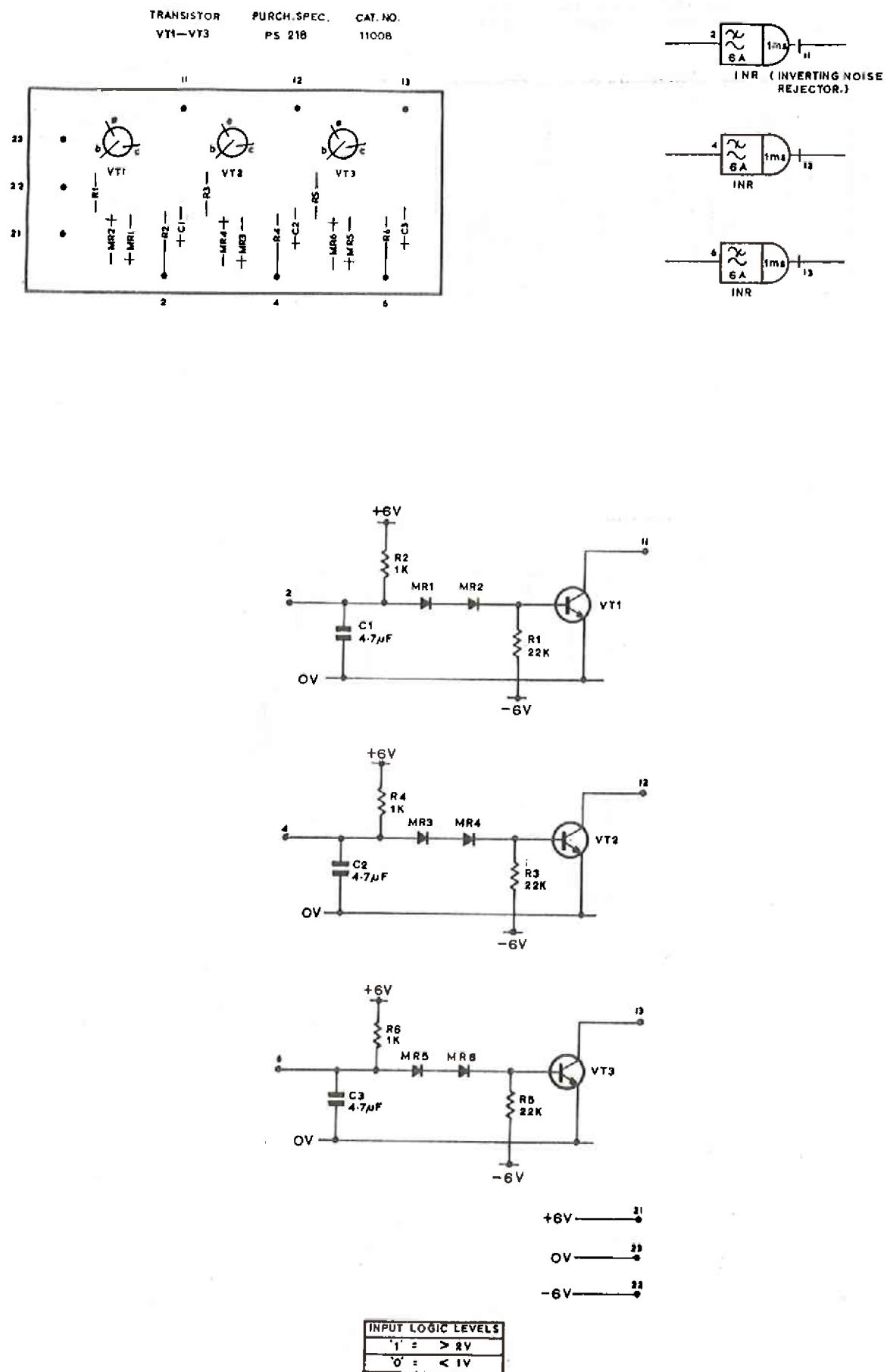
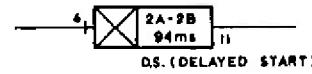
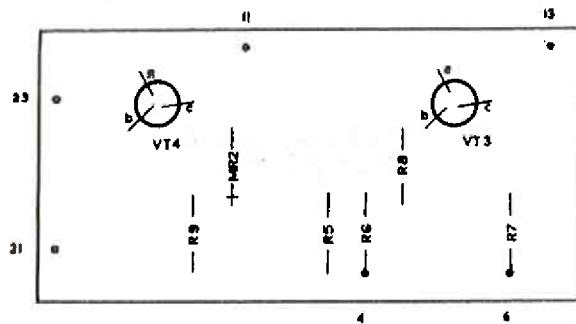
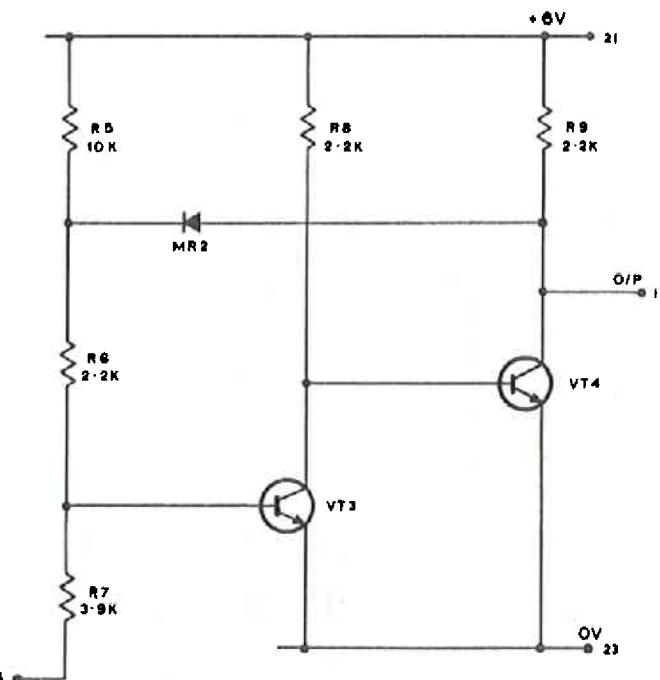


Figure 20 (issue 2.)

TRANSISTOR PURCHASE SPEC. CAT.NO.
VT3 VT4 PS218 11008

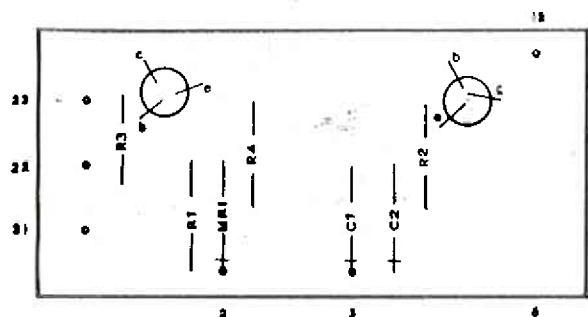


NOTE :-
L.S.A.19 ALWAYS FOLLOWS L.S.A.
20, 21, 24 OR 25. THE SYMBOL
SHOWN IS A COMBINED SYMBOL
FOR THE 2 ELEMENTS.

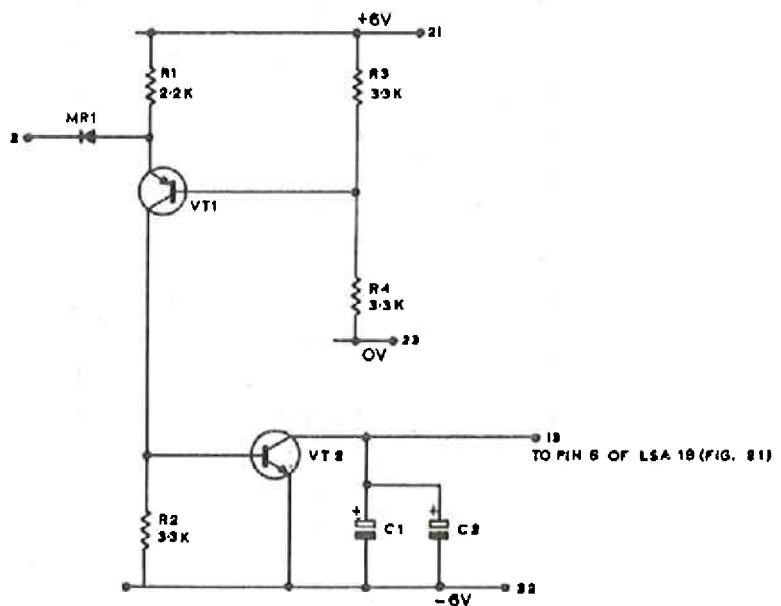


| INPUT THRESHOLD LEVEL |
|------------------------|
| (AT 25°C) = -0.4v ±10% |

| TRANSISTOR | PURCH. SPEC. | CAT. NO. |
|------------|--------------|----------------|
| VT1 VT2 | PS 218 | 14581 11008 |



L.S.A. 19 ALWAYS FOLLOWS
L.S.A. 20 24 OR 25
SEE FIG. 81 FOR COMBINED
SYMBOL.

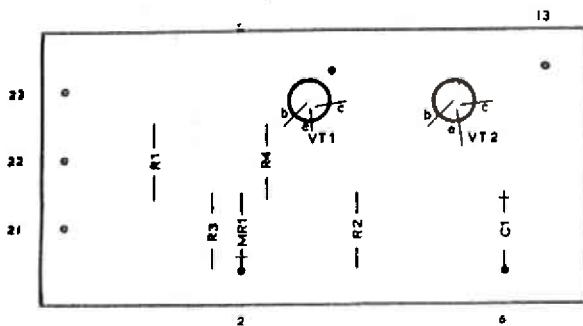


| L.S.A. No. | C1 μ F | C2 μ F | DELAY ms |
|------------|------------|------------|----------|
| 20 | 4.7 | 4.7 | 94 |
| 24 | 2.2 | 1.0 | 32 |
| 25 | 2.2 | 0.47 | 26.7 |

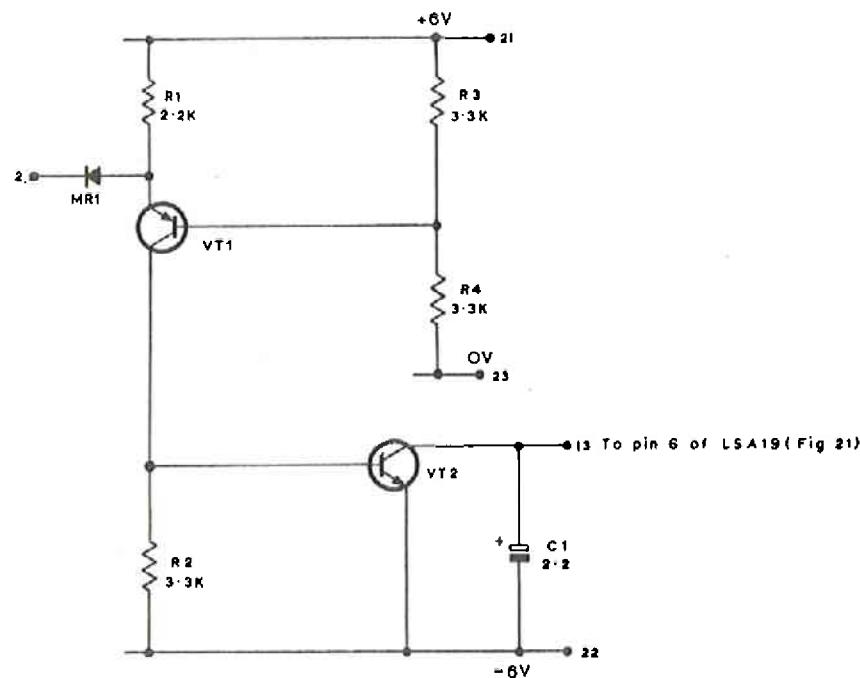
NOTE 1
DELAY Δ 10ms PER μ F (WHERE μ F IS CAPACITANCE OF C1 & C2)

| INPUT LOGIC LEVELS |
|--------------------|
| '1' = > 3V |
| '0' = < 1V |

TRANSISTOR PURCH. SPEC. CAT. NO.
 VT1 — 14581
 VT2 PS 218 11008



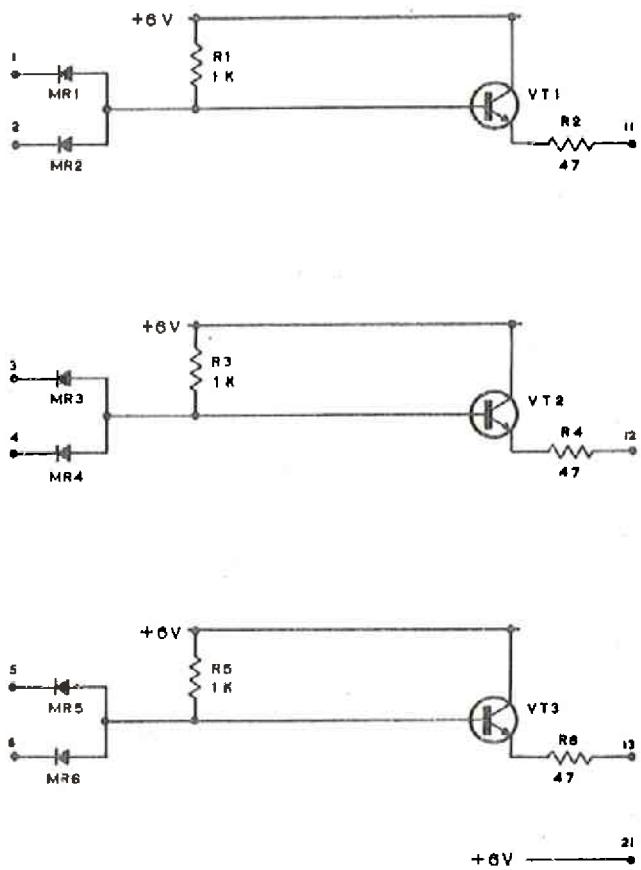
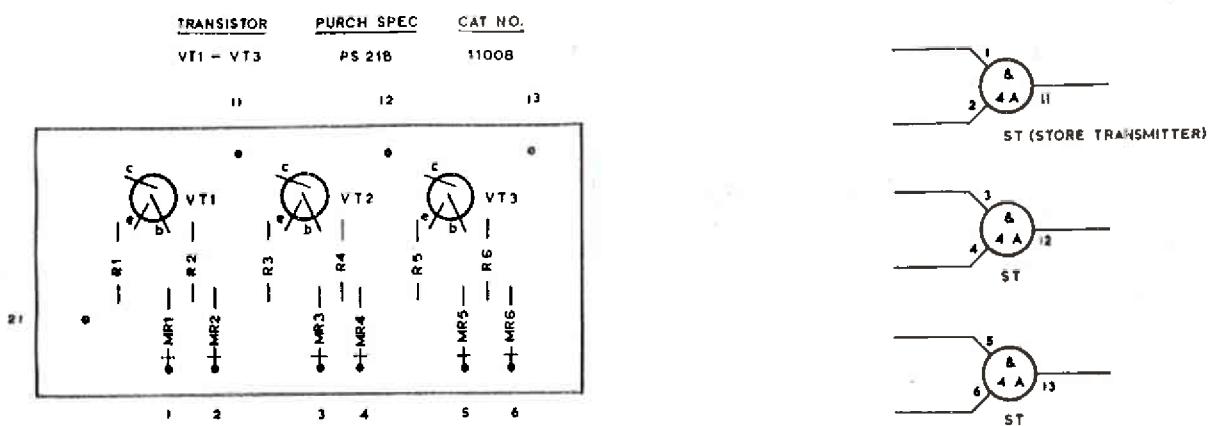
L.S.A.19 ALWAYS FOLLOWS
 L.S.A. 21 SEE FIGURE 21
 FOR COMBINED SYMBOL.



NOTE:

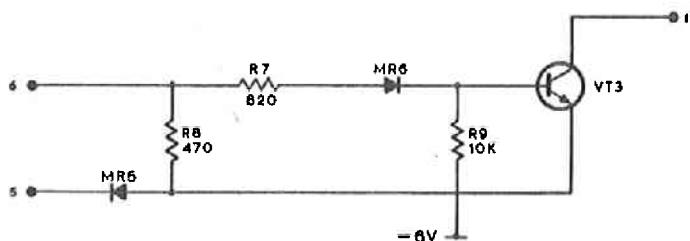
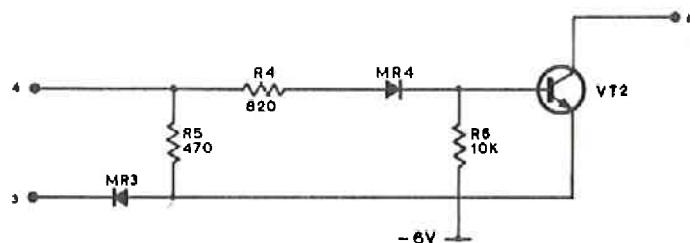
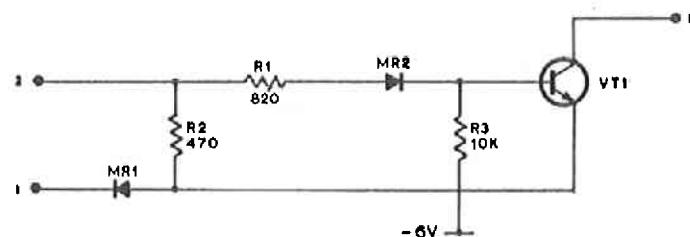
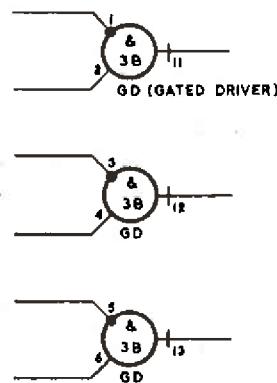
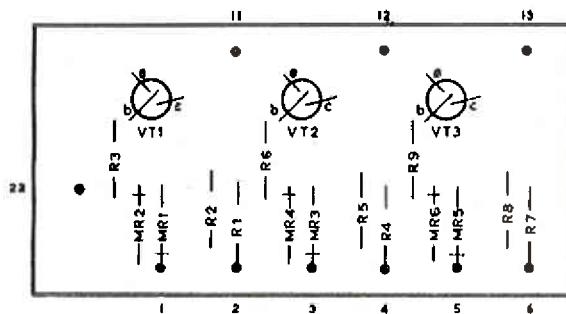
1. DELAY Δ 10ms PER μF
 (WHERE μF IS CAPACITANCE
 OF C1) Δ 22 ms.

| INPUT LOGIC LEVELS |
|--------------------|
| '1' = $> 3V$ |
| '0' = $< 1V$ |



| INPUT LOGIC LEVELS | |
|--------------------|---|
| (1) | O/P FOLLOWS I/P OVER RANGE OV TO 4.7V |
| (2) | WHEN DRIVING A RECEIVER THE LOGIC LEVELS ARE :- |
| | |
| '1' | = > 3V |
| '0' | = < 1V |

TRANSISTOR
VT1 - VT3 PURCH. SPEC.
PS 218 CAT. NO.
11008



-6V —————— 22

| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = $> 3V$ |
| '0' | = $< 1V$ |

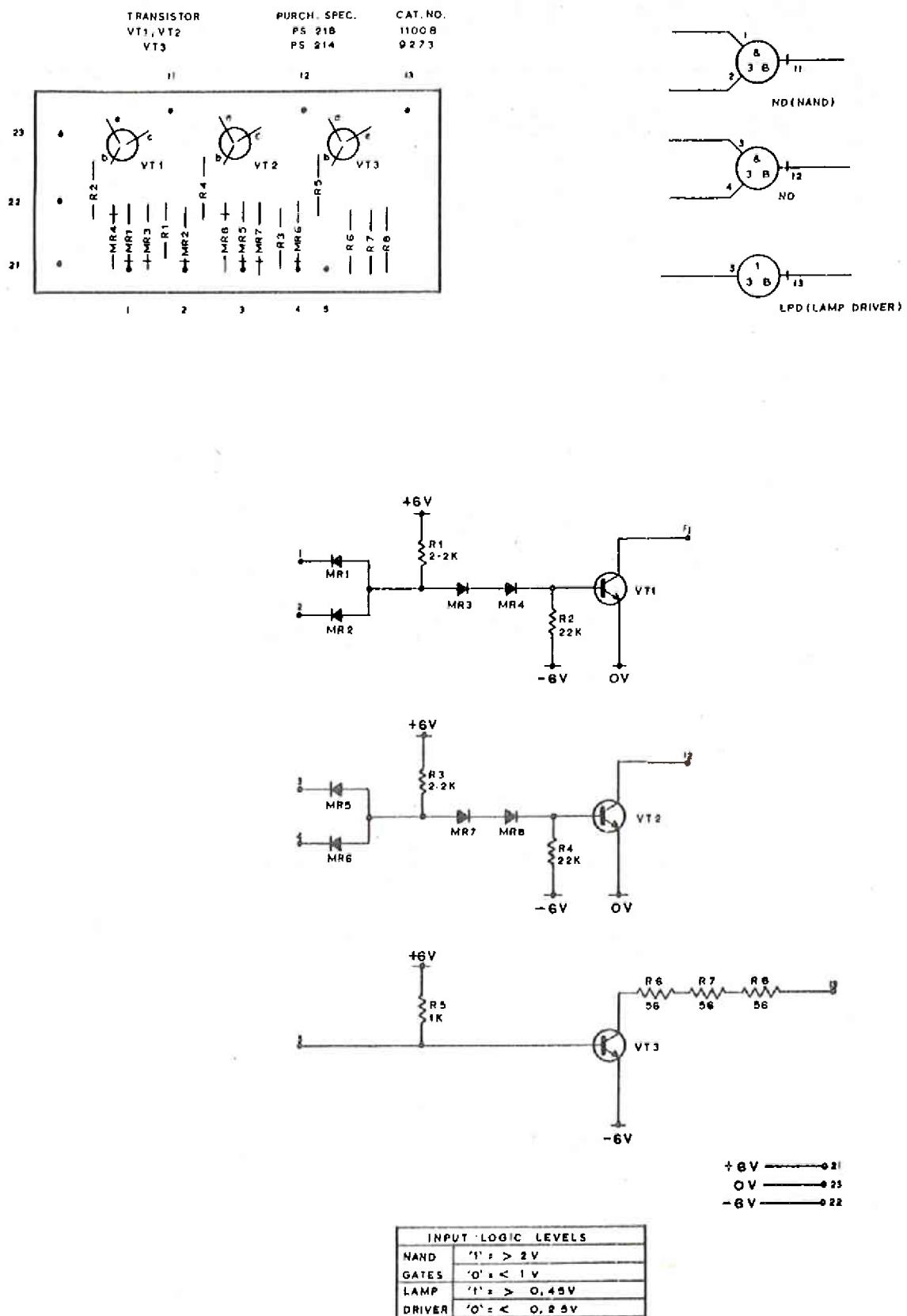
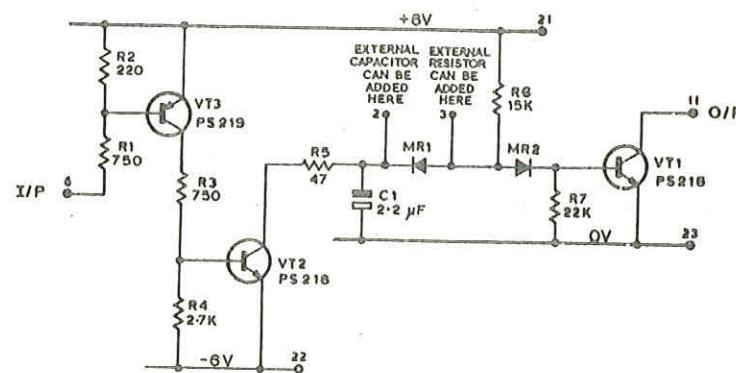
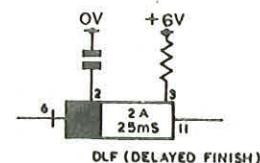
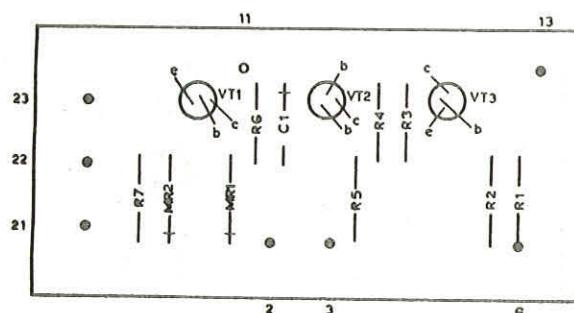


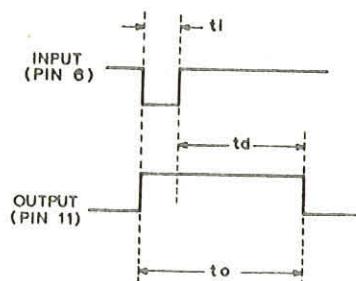
Figure 26 (ISSUE 2)

TRANSISTOR PURCH. SPEC. CAT. No.
 VT1, VT2 PS 218 11008
 VT3 PS 219 11009



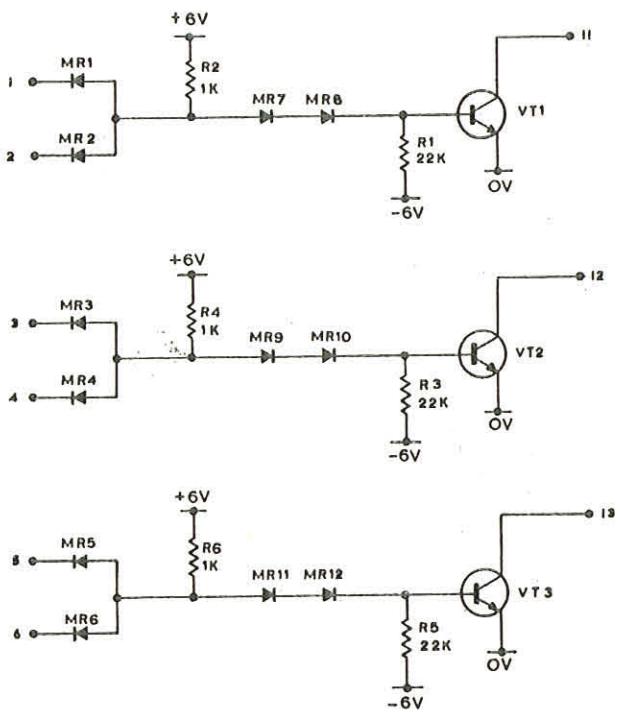
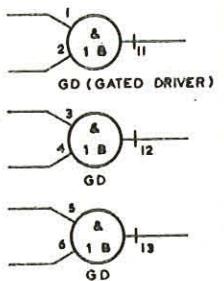
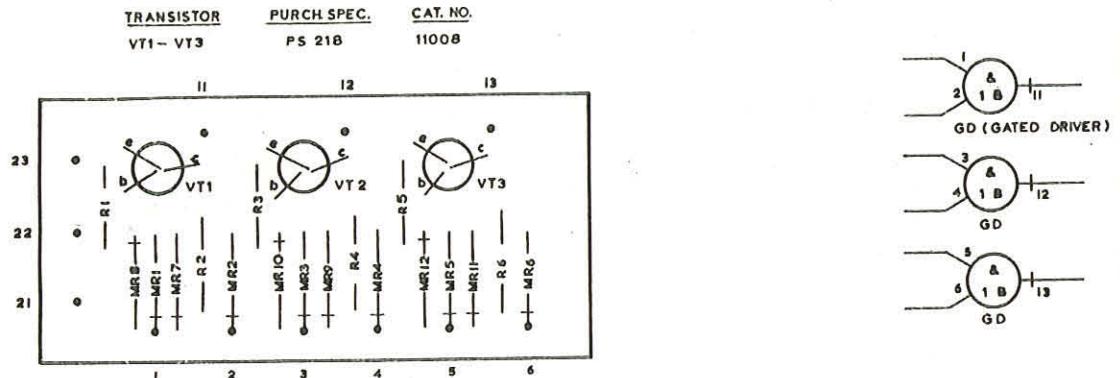
NOTE:

1. SHUNT C1 TO MAKE O/P $> 25\text{ms}$.
2. SHUNT R6 TO MAKE O/P $< 25\text{ms}$.



td NOMINAL = 25ms
 td RANGE = 1m - 5 Secs.
 td TOLERANCE = $\pm 30\%$

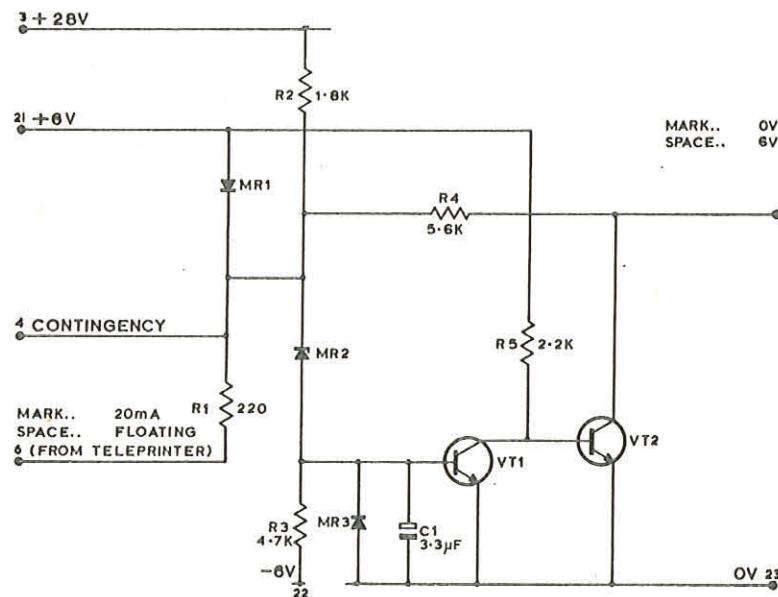
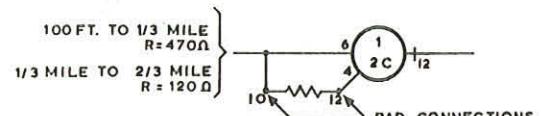
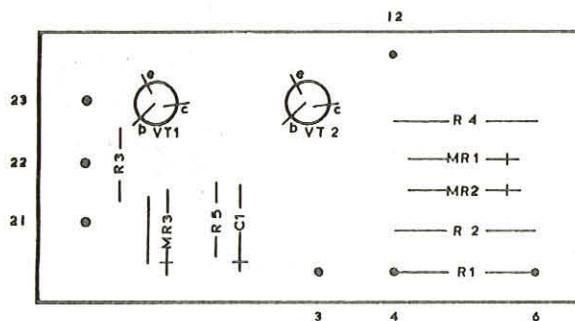
| INPUT LOGIC LEVELS | |
|--------------------|-------------------|
| '1' | = $> 5.4\text{V}$ |
| '0' | = $< 1\text{V}$ |



+ 6V —————— o 21
OV —————— o 23
- 6V —————— o 22

| INPUT LOGIC LEVELS | |
|--------------------|------|
| '1' = | > 2V |
| '0' = | < 1V |

TRANSISTOR PURCH. SPEC. CAT. No.
VT1, VT2 PS 218 1100B



NOTE:

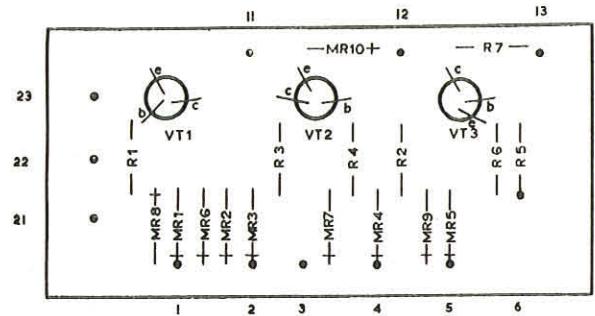
THE ELEMENT IS CONSIDERED TO INVERT BECAUSE THE MARK CURRENT IS TAKEN TO REPRESENT A LOGIC "1" EVEN THOUGH THE POTENTIAL AT PIN 6 FALLS UNDER MARK CONDITIONS.

| INPUT LOGIC LEVELS | |
|--|--|
| 0 = > 5V | |
| 1 = < 0.4V (ASSUMING NO EXTERNAL R AT PIN 4) | |

4100 / 900

4.6.1.

TRANSISTOR PURCH. SPEC. CAT. NO.
 VT1, VT2 PS21B 11008
 VT3 PS219 11009



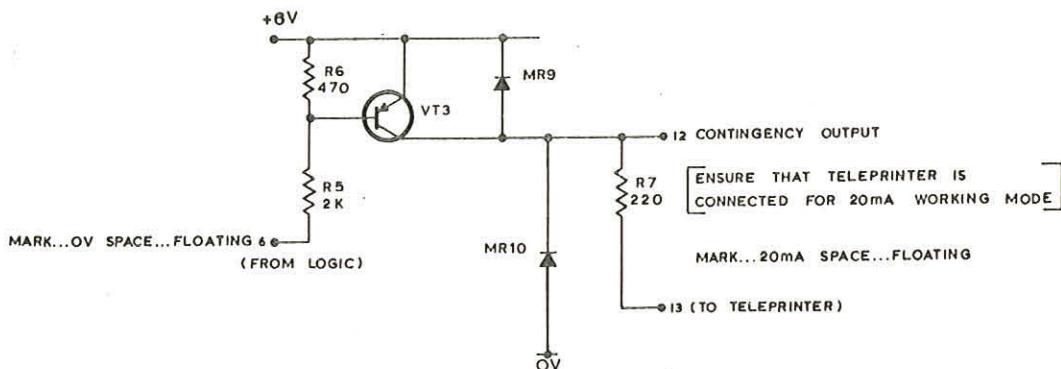
CABLES UP TO 100FT ————— 6 1 2 A 13 —————
 TPD(TELEPRINTER DRIVER)

100FT TO $\frac{1}{3}$ MILE
 $R = 470\Omega$
 $\frac{1}{3}$ MILE TO $\frac{2}{3}$ MILE
 $R = 120\Omega$

$\frac{2}{3}$ MILE - 1 MILE ————— 6 1 2 A 13 —————

AND-OR
 4 & 1
 5 & 2A II

AOR (AND OR)



TELEPRINTER DRIVER

| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = $> 4V$ |
| '0' | = $< 1V$ |

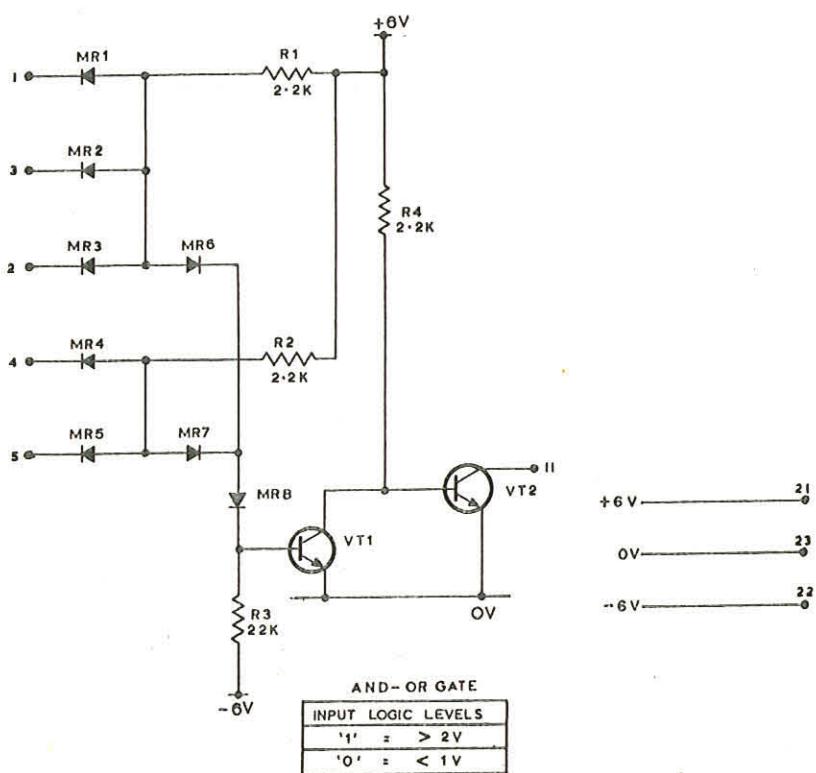
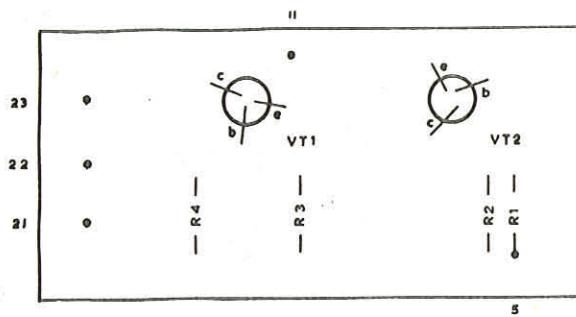
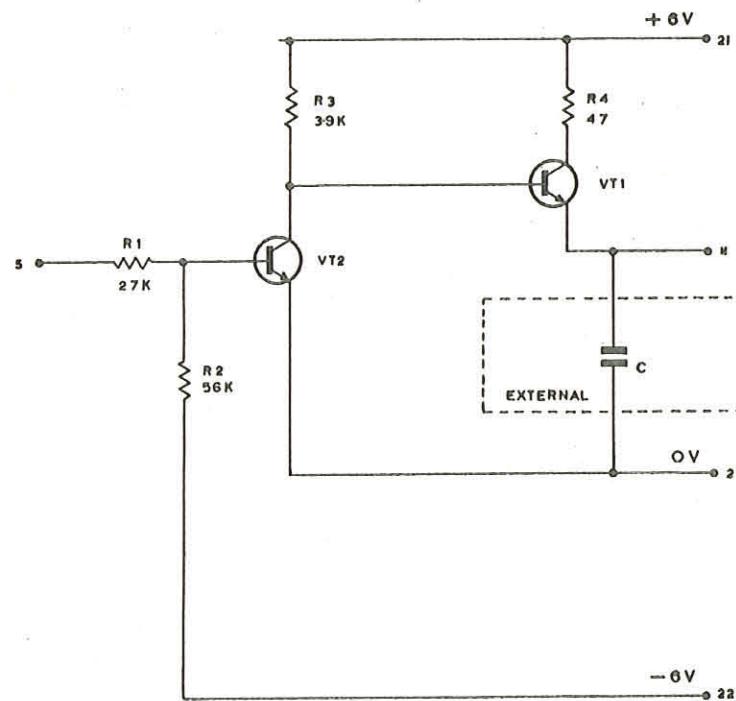


Figure 30 (ISSUE 2)

| | | |
|------------------------|----------------------|-----------------|
| TRANSISTOR VT1, VT2 | PURCH SPEC PS 212 | CAT NO. 8843 |
|------------------------|----------------------|-----------------|



SEE FIGURE 32 FOR SYMBOL

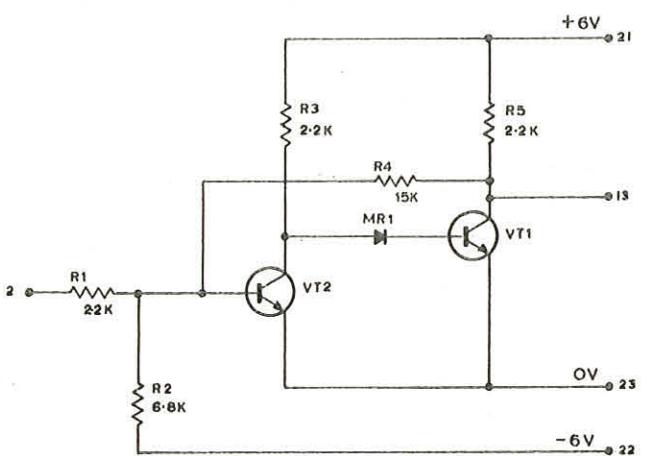
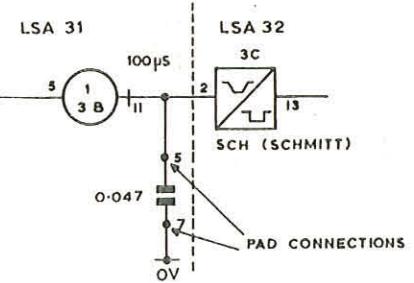
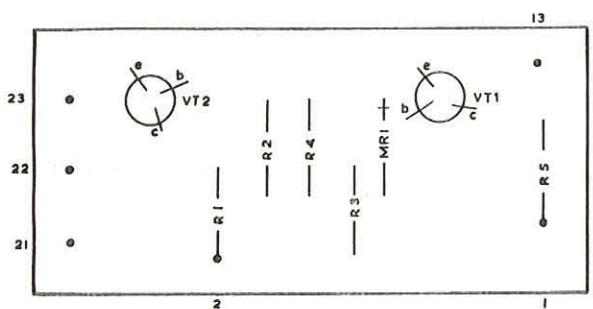


NOTES:

(1) INPUT VOLTAGE LEVELS ARE '1' = +12V ±3V; '0' = OV ±3V

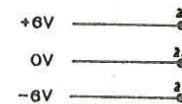
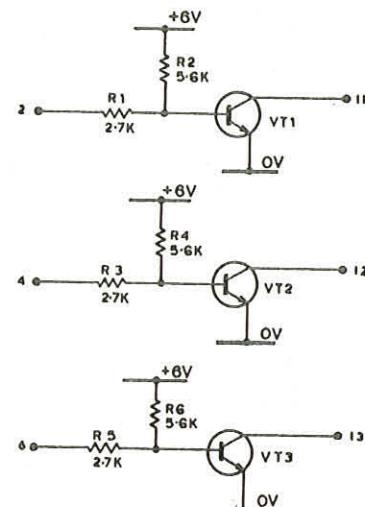
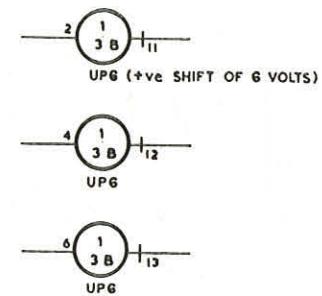
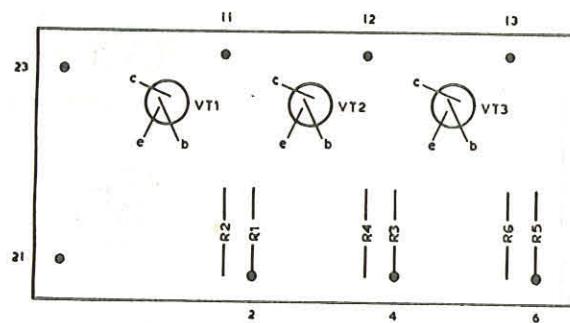
(2) C IS CONNECTED EXTERNALLY WHEN USED IN CONJUNCTION WITH
A RESISTOR ON LSA 32

(3) C = 0.047 μF FOR A DELAY OF 100 μS.

TRANSISTOR
VT1, VT2PURCH. SPEC.
PS 212CAT. NO.
8843

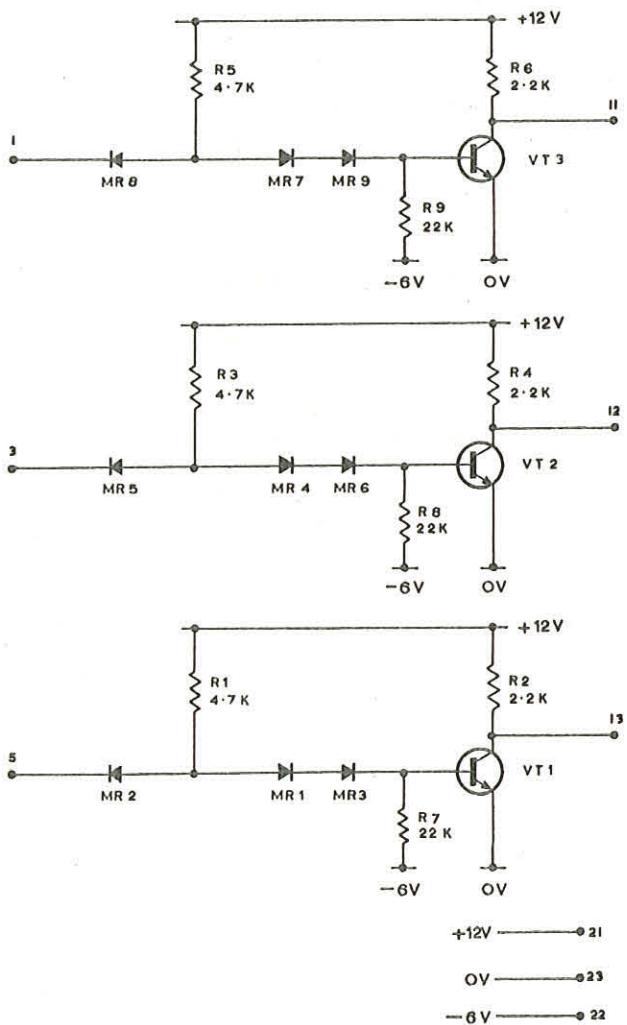
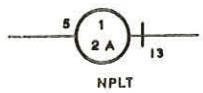
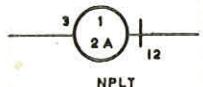
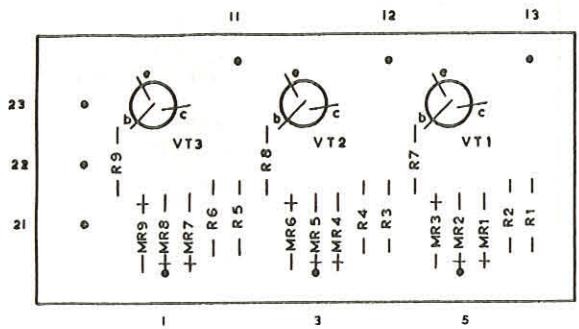
| THRESHOLD VOLTAGE AT PIN 2 | OUTPUT WAVEFORM PIN 13 |
|-------------------------------|---------------------------|
| RISING VOLTAGE $+3.1V$ | |
| FALLING VOLTAGE $+2.4V$ | |

TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 218 11008

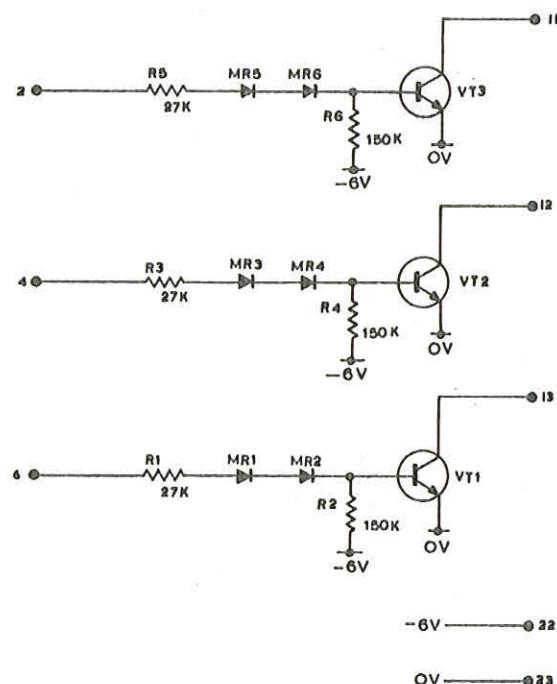
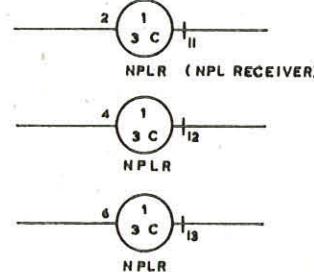
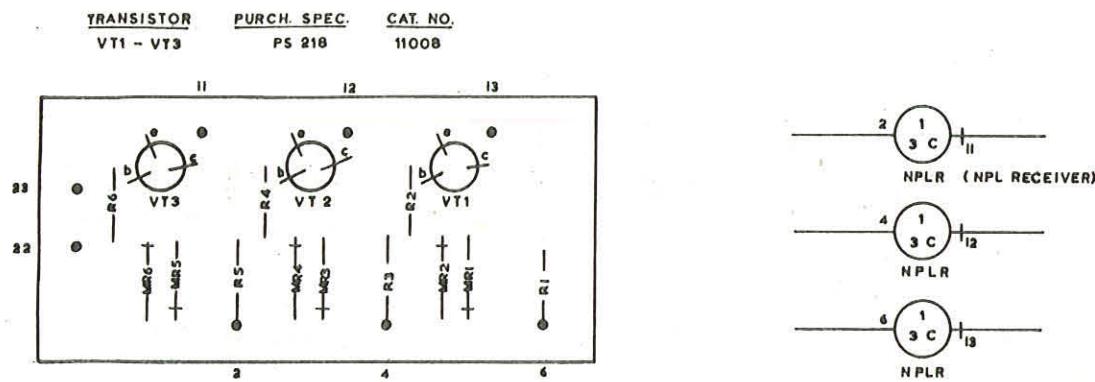


| INPUT LOGIC LEVELS | |
|--------------------|-----------|
| '1' | = > -1.2V |
| '0' | = < -3V |

| TRANSISTOR | PURCH. SPEC. | CAT. NO. |
|------------|--------------|----------|
| VT1 - VT3 | PS 218 | 11008 |



| INPUT LOGIC LEVELS | |
|--------------------|-------|
| '1' | = > 2 |
| '0' | = < 1 |

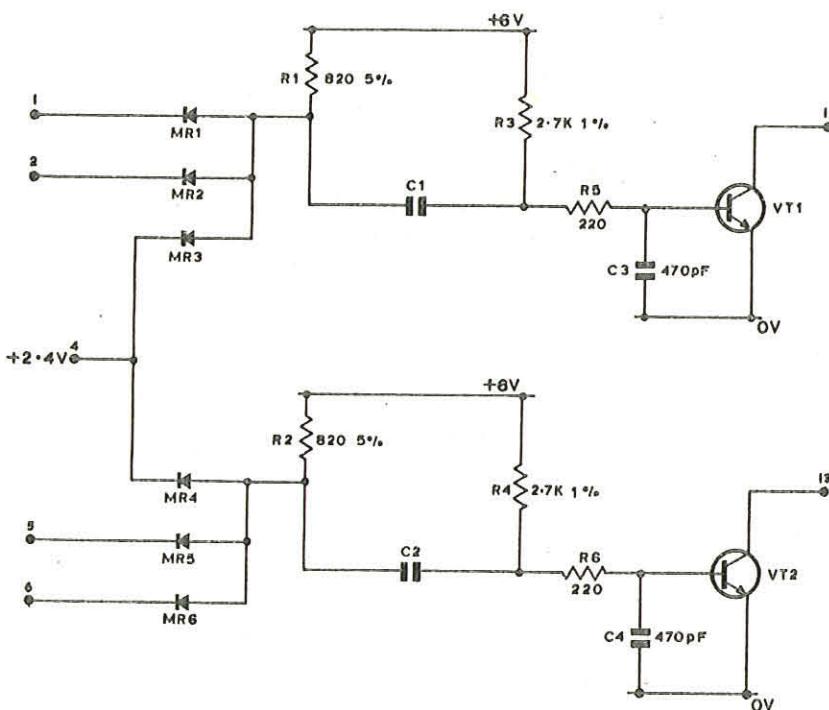
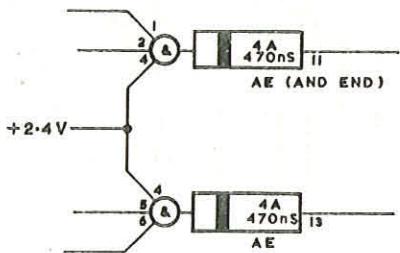
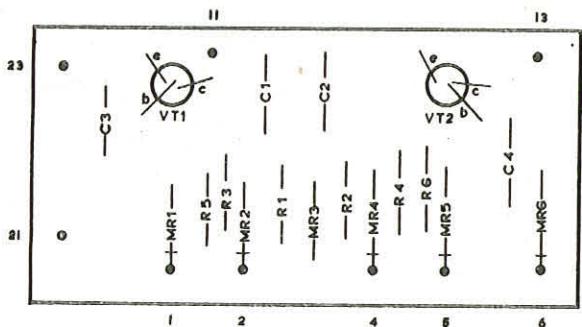


-6V —————— ② 22

OV —————— ② 23

| INPUT LOGIC LEVELS | |
|--------------------|-------|
| "1" | = > 2 |
| '0' | = < 1 |

TRANSISTOR
VT1, VT2 PURCH. SPEC.
 PS 21B CAT. No.
 11008



| PULSE WIDTH = $C_n S$ (WHERE C = CAPACITANCE IN pF.) | | |
|--|---------------|---------------|
| | UPPER ELEMENT | LOWER ELEMENT |
| L.S.A. | C1 | C2 |
| 37 | 680pF | 680pF |
| 39 | 100pF | 100pF |
| 40 | 330pF | 330pF |
| 41 | 220pF | 220pF |
| 42 | 470pF | 470pF |

NOTES:

- (1) OUTPUT PULSE POSITIVE.
- (2) PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR GREATER THAN $C/2$ ns. (WHERE C = CAPACITANCE IN pF.)

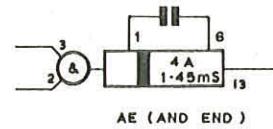
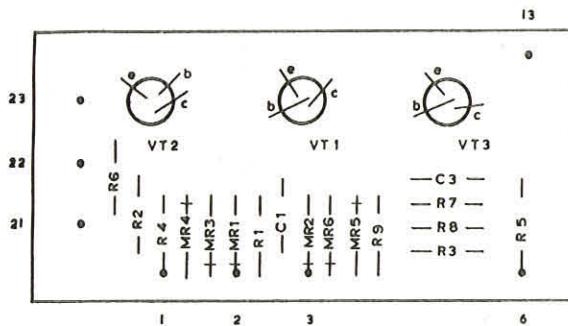
+6V —— ②1
OV —— ②3

| INPUT LOGIC LEVELS |
|--------------------|
| '1' = > 2.4V |
| '0' = < 1V |

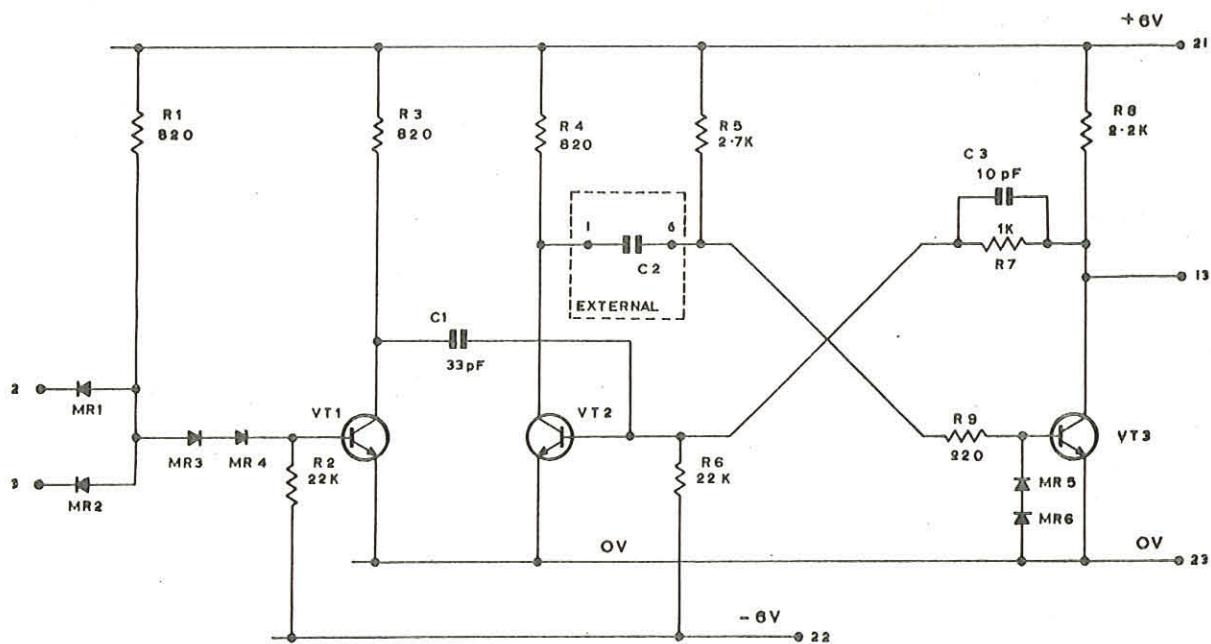
Figure 36 (ISSUE 2)

L.S.A. 37, 39, 40, 41, 42.

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1~VT3 PS 218 1100B



AE (AND END)



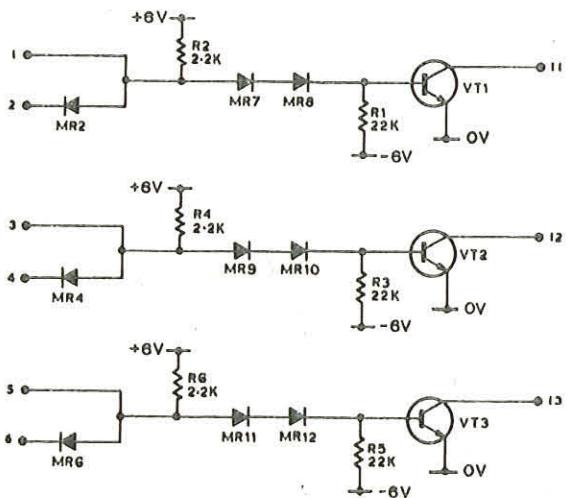
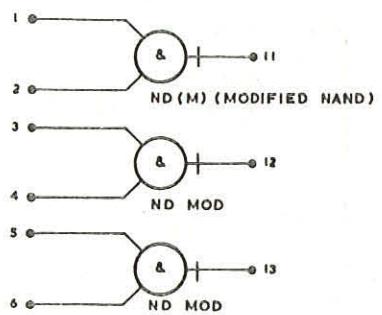
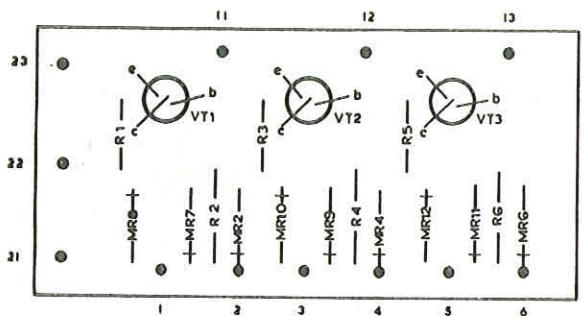
NOTES:

- (1) C2 IS EXTERNAL AND SETS PULSE WIDTH
- (2) OUTPUT PULSE POSITIVE
- (3) PULSE TRIGGERED BY ANY INPUT REVERTING TO A '0' PROVIDED OTHER INPUT IS A '1'
- (4) PULSE WIDTH $T = 1.36 \times C_2 \text{ nS}$ $\pm 36\%$
(WHERE C2 IS IN pF)

| INPUT LOGIC LEVELS | |
|--------------------|--|
| '1' = > 2 | |
| '0' = < 1 | |

4100/900
4.6.1.

TRANSISTOR
VT1-VT3 PURCH. SPEC.
 PS 218 CAT. No.
 11008

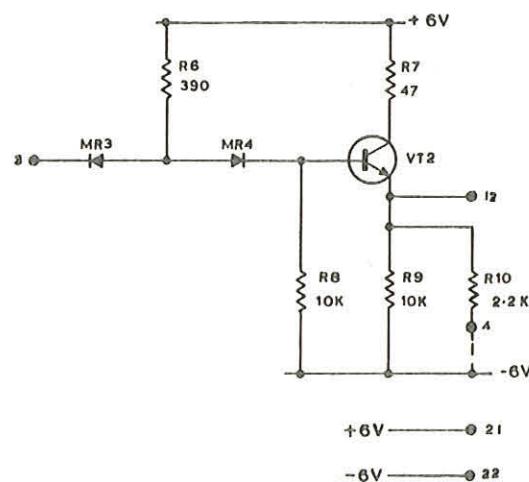
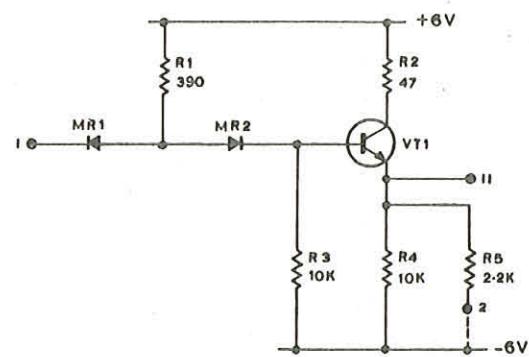
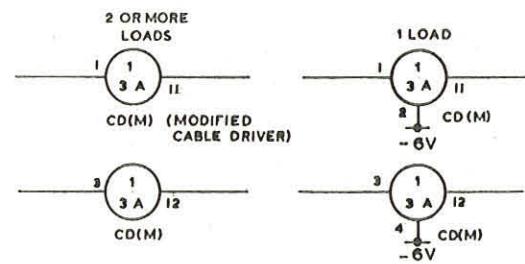
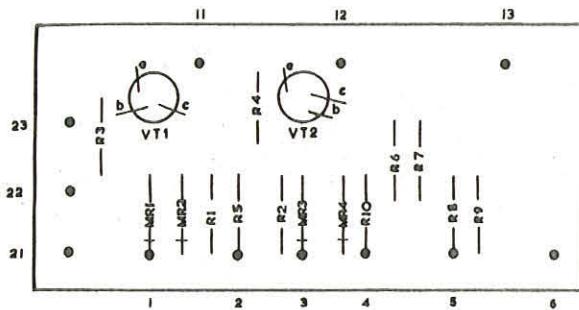


+6V —————— 0 21
0V —————— 0 22
-6V —————— 0 23

| INPUT LOGIC LEVEL | |
|-------------------|--------|
| '1' | = > 2V |
| '0' | = < 1V |

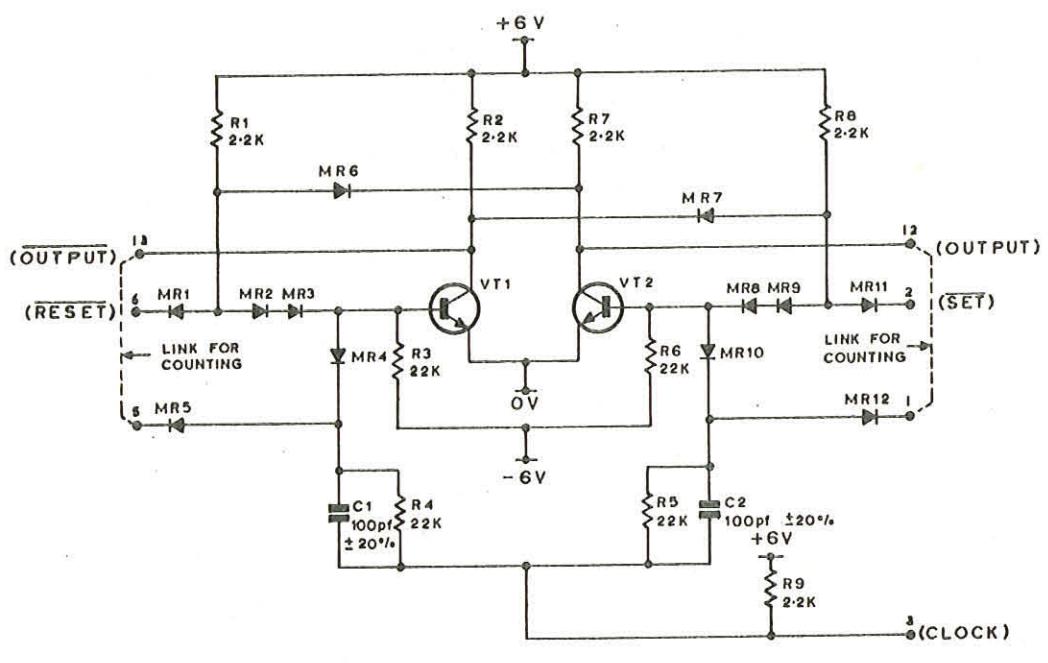
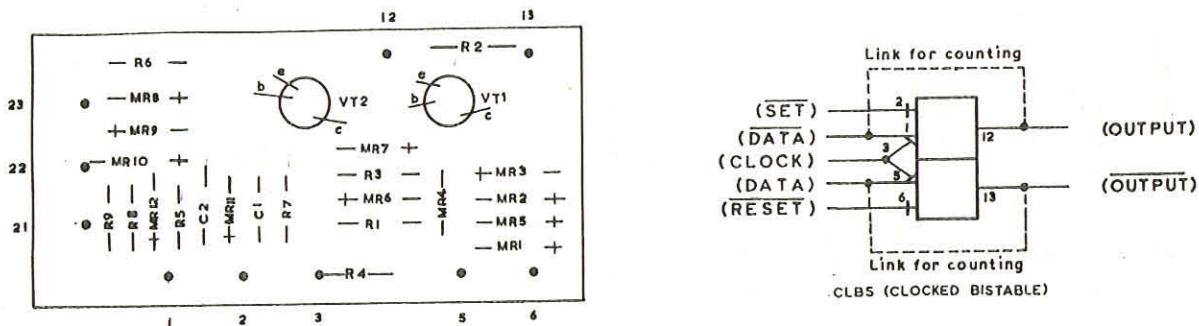
Figure 38 (ISSUE 2)

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1 VT2 PS 216 11008



| INPUT LOGIC LEVELS | |
|--------------------|------|
| '1' = | > 2V |
| '0' = | < 1V |

TRANSISTOR PURCH. SPEC. CAT. NO.
VT1, VT2 PS21B 1100B

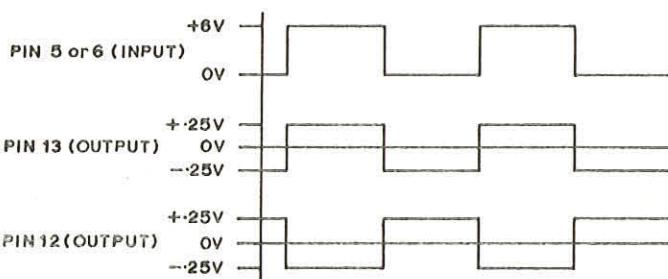
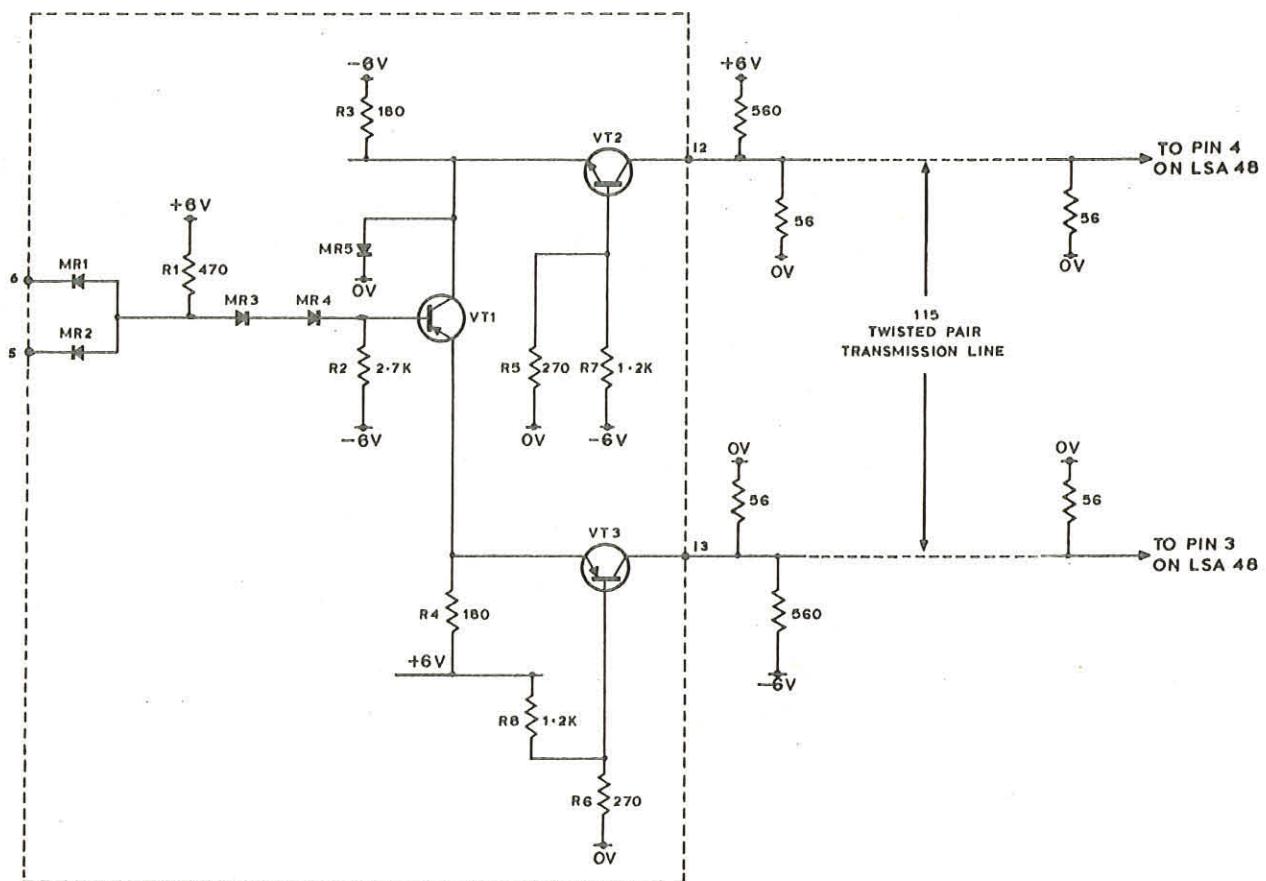
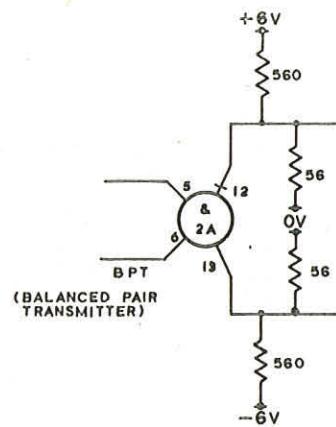
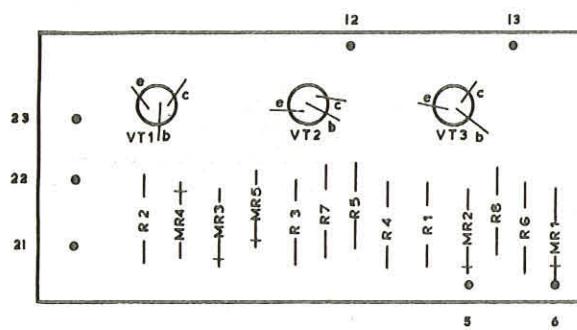


+6V —————— 21
OV —————— 23
-6V —————— 22

| INPUT LOGIC LEVELS | |
|--------------------|---------|
| '1' | = > 2 V |
| '0' | = < 1 V |

Figure 40 (ISSUE 2)

TRANSISTOR PURCH. SPEC. CAT. No.
 VT1, VT3. PS 216. 9725.
 VT2. PS 212. 8843.



+6V ————— 021
 0V ————— 023
 -6V ————— 022

NOTE:

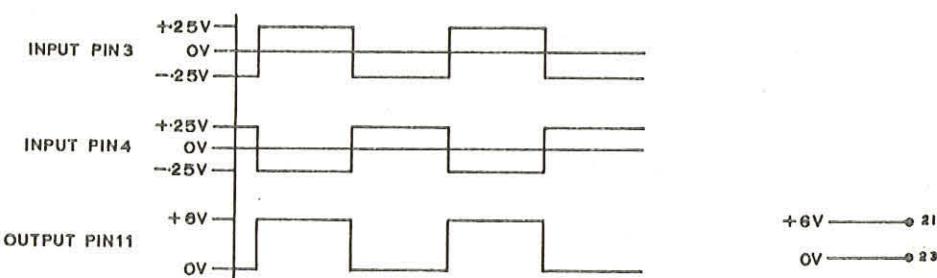
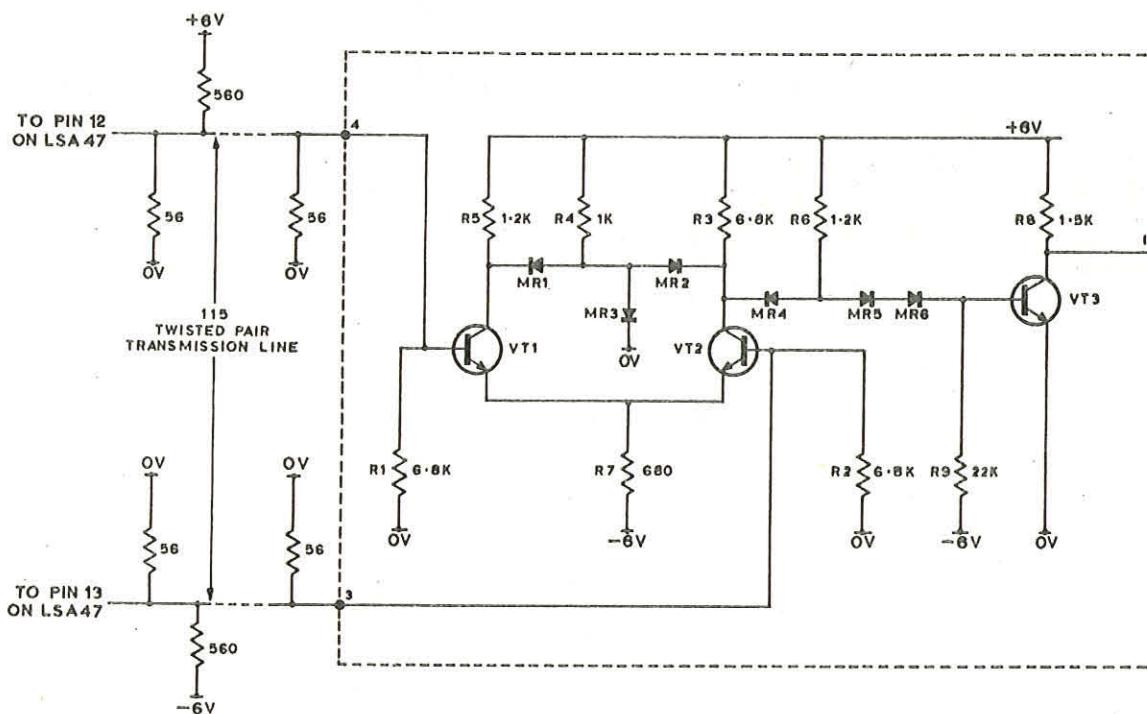
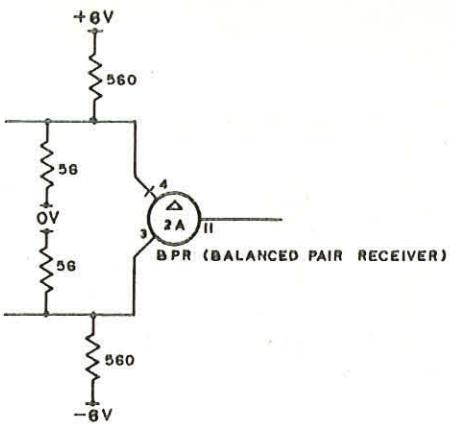
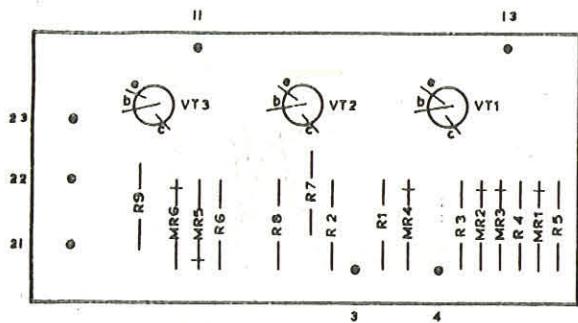
THE OUTPUT WAVEFORMS ABOVE ARE THOSE OBTAINED WITH TERMINATION AND BIASING AS USED ON THE CDC INTERFACE.
 THE 56Ω TERMINATING RESISTORS MUST BE ON EACH END OF THE TRANSMISSION LINE.
 THE 560Ω BIASING RESISTORS MAY BE AT EITHER END OF THE LINE, BUT NOT AT BOTH.

| INPUT LOGIC LEVELS | |
|--------------------|--|
| '1' = > 2V | |
| '0' = < 1V | |

4100/900.

4.6.1.

| | | |
|-----------------------------------|--------------|----------|
| TRANSISTOR | PURCH. SPEC. | CAT. No. |
| VT ₁ , VT ₂ | PS 212 | 6843 |
| VT ₃ | PS 218 | 11008 |



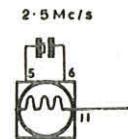
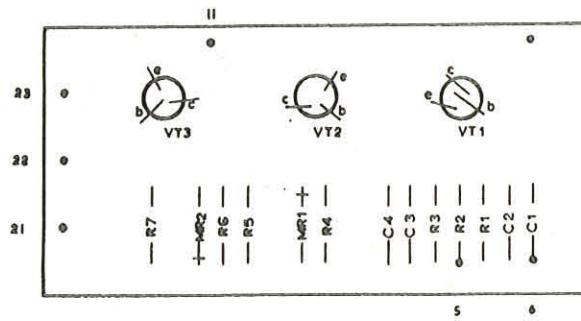
NOTE:
THE INPUT WAVEFORMS ABOVE ARE THOSE
OBTAINED WITH TERMINATION AND BIASING
AS USED ON THE CDC INTERFACE.
THE 56Ω TERMINATING RESISTORS MUST BE
ON EACH END OF THE THE TRANSMISSION LINE.
THE 56Ω BIASING RESISTORS MAY BE AT
EITHER END OF THE LINE, BUT NOT AT BOTH.

| INPUT LOGIC LEVELS | |
|----------------------|--|
| '1'=PIN 4 > PIN 3 BY | |
| 0.4V MIN. 0.6V MAX. | |
| '0'=PIN 3 > PIN 4 BY | |
| 0.4V MIN. 0.6V MAX. | |

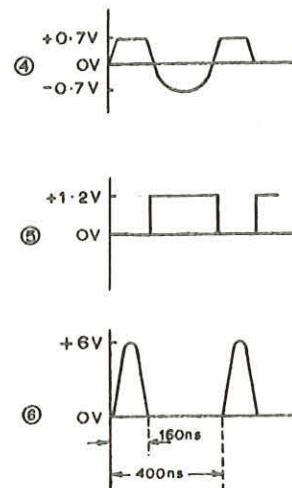
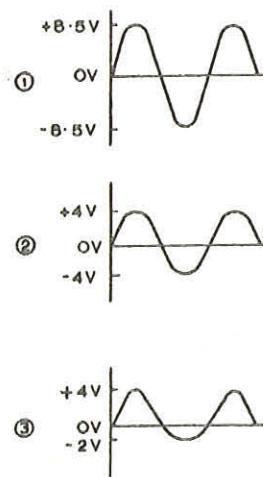
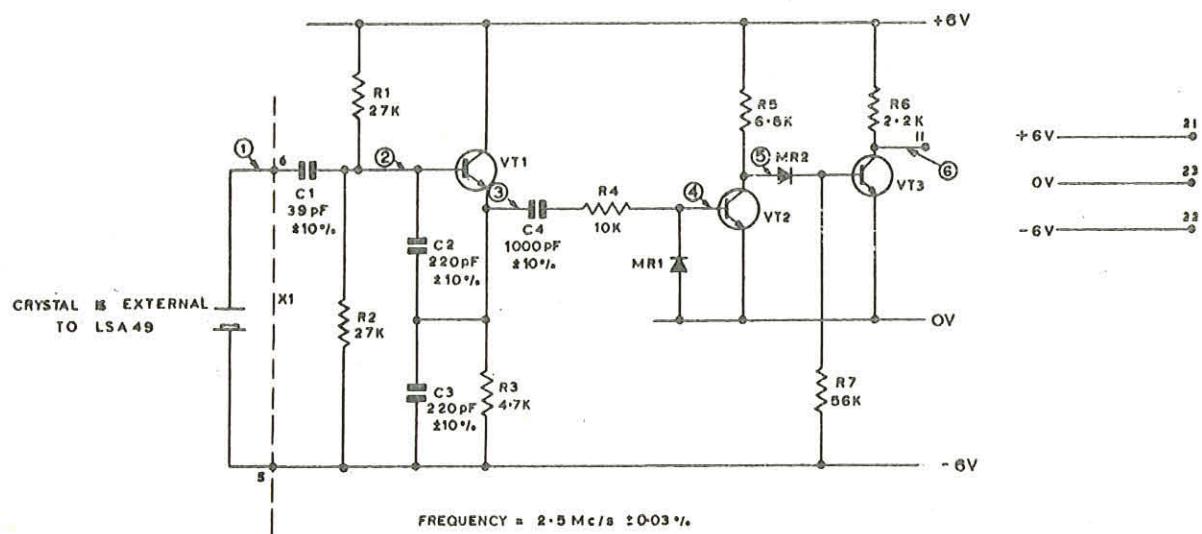
Figure 42. (ISSUE 2)

L.S.A.48.

| | | |
|------------|--------------|----------|
| TRANSISTOR | PURCH. SPEC. | CAT. NO. |
| VT1 | — | 13053 |
| VT2 VT3 | PS 218 | 11008 |

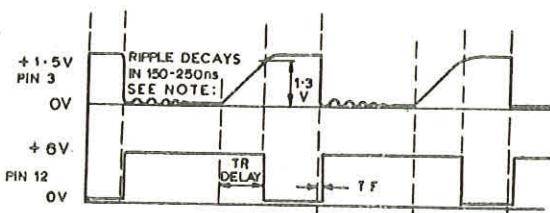
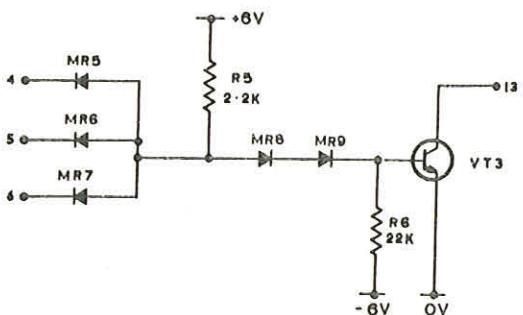
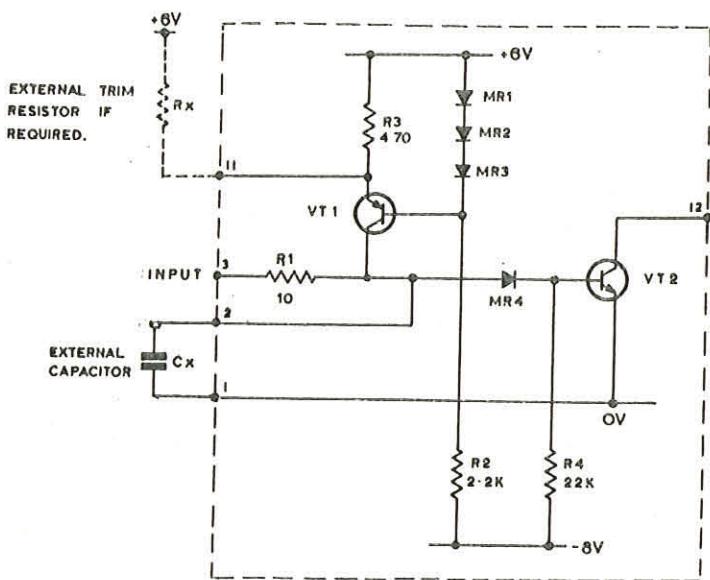
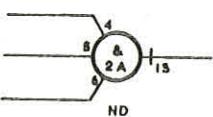
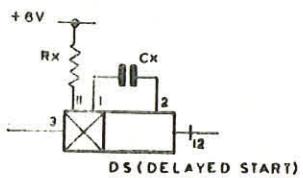
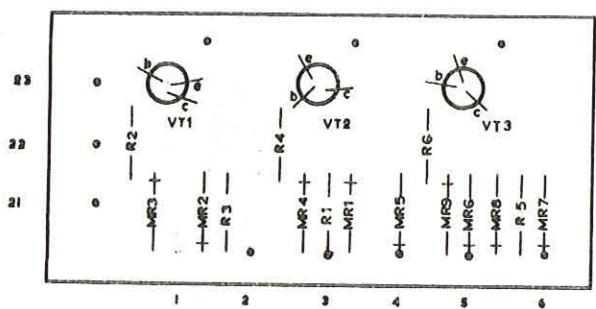


CO (CRYSTAL OSCILLATOR)



4.6.1.

TRANSISTOR PURCH. SPEC. CAT. NO.
 VT1 PS 219 11009
 VT2, VT3 PS 210 11008



+ 6V ————— ②1
 OV ————— ②3
 - 6V ————— ②2

ADD:
 $TR = 35 + 0.44 C_x \text{ ns}$
 (where C_x is in pF)
 $TF = 30 + 0.05 TR \text{ ns}$
 (where TR is in ns)

NOTE:

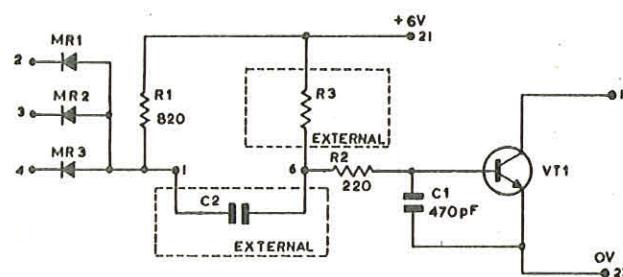
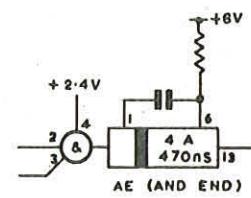
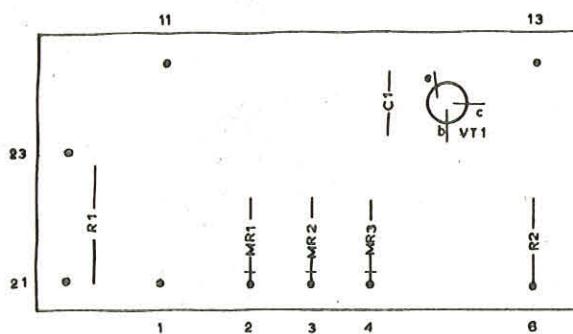
- Assuming connection to driving source is not more than 6ins long.

| INPUT LOGIC LEVELS | |
|--------------------|---------------------|
| DELAY ELEMENT | '1': > 0.25V AT 3mA |
| HAND GATE | '0': OPEN CIRCUIT |
| NAND | '1': > 2V |
| GATE | '0': < 1V |

| Value | Tol. | Voltage | Cat. No. | Nominal Delay |
|----------------|----------|---------|----------|-----------------------------|
| 220 pf | \pm 5% | 400V | 9313 | 132 \pm 32, 9 ns. |
| 330 pf | \pm 5% | 400V | 8479 | 180 \pm 45, 1 ns. |
| 470 pf | \pm 5% | 400V | 7916 | 242 \pm 60, 4 ns. |
| 680 pf | \pm 5% | 400V | 8480 | 334 \pm 83, 6 ns. |
| 1000 pf | \pm 5% | 400V | 7917 | 475 \pm 119 ns. |
| 1500 pf | \pm 5% | 400V | 7924 | 695 \pm 174 ns. |
| 2200 pf | \pm 5% | 400V | 7918 | 1, 00 \pm 0, 251 μ s. |
| 3300 pf | \pm 5% | 400V | 7919 | 1, 49 \pm 0, 372 μ s. |
| 4700 pf | \pm 5% | 125V | 7920 | 2, 10 \pm 0, 526 μ s. |
| 6800 pf | \pm 5% | 125V | 7921 | 3, 03 \pm 0, 757 μ s. |
| 0. 01 μ F | \pm 5% | 400V | 7922 | 4, 44 \pm 1, 11 μ s. |
| 0. 015 μ F | \pm 5% | 125V | 7504 | 6, 63 \pm 1, 66 μ s. |
| 0. 022 μ F | \pm 5% | 125V | 7475 | 9, 72 \pm 2, 43 μ s. |
| 0. 033 μ F | \pm 5% | 125V | 7720 | 14, 6 \pm 3, 64 μ s. |
| 0. 047 μ F | \pm 5% | 125V | 7044 | 20, 7 \pm 5, 18 μ s. |
| 0. 068 μ F | \pm 5% | 125V | 8481 | 30, 0 \pm 7, 49 μ s. |
| 0. 1 μ F | \pm 5% | 20V | 9136 | 44, 0 \pm 11, 0 μ s. |
| 0. 15 μ F | \pm 5% | 20V | 9915 | 66, 0 \pm 16, 5 μ s. |
| 0. 22 μ F | \pm 5% | 20V | 11043 | 96, 8 \pm 24, 2 μ s. |
| 0. 33 μ F | \pm 5% | 15V | 9369 | 145 \pm 36, 3 μ s. |
| 0. 47 μ F | \pm 5% | 15V | NR | 207 \pm 51, 7 μ s. |
| 0. 68 μ F | \pm 5% | 15V | 9430 | 299 \pm 74, 8 μ s. |
| 1. 0 μ F | \pm 5% | 15V | 9386 | 440 \pm 110 μ s. |
| 1. 5 μ F | NR | 15V | ---- | 660 \pm 165 μ s. |
| 2. 2 μ F | NR | 15V | ---- | 968 \pm 242 μ s. |
| 3. 3 μ F | \pm 5% | 15V | 9431 | 1, 45 \pm 0, 363 ms. |
| 4. 7 μ F | \pm 5% | 15V | 9398 | 2, 07 \pm 0, 517 ms. |
| 6. 8 μ F | \pm 5% | 15V | 9387 | 2, 99 \pm 0, 748 ms. |
| 10. 0 μ F | \pm 5% | 15V | 9309 | 4, 40 \pm 1, 10 ms. |
| 15. 0 μ F | \pm 5% | 15V | NR | 6, 60 \pm 1, 65 ms. |
| 22. 0 μ F | \pm 5% | 15V | 9385 | 9, 68 \pm 2, 42 ms. |
| 33. 0 μ F | \pm 5% | 15V | 11044 | 14, 5 \pm 3, 63 ms. |
| 47. 0 μ F | \pm 5% | 15V | 11042 | 20, 7 \pm 5, 17 ms. |
| 68. 0 μ F | \pm 5% | 15V | 9308 | 29, 9 \pm 7, 48 ms. |
| 100. 0 μ F | \pm 5% | 10V | 9151 | 44, 0 \pm 11, 0 ms. |

| % Reduction of delay | 0. 99 | 1. 4 | 2, 1 | 3. 0 | 4. 5 | 5. 4 | 6. 5 | 7. 7 | 9. 1 | 12 | 18 |
|----------------------|-------|------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------|
| Resistor | 47K | 33K | 22K | 15K | 10K | 8. 2K | 6. 8K | 5. 6K | 4. 7K | 3. 3K | 2. 2K |
| % Reduction of delay | 24 | 32 | 36 | 41 | 46 | 50 | 59 | 68 | 76 | 82 | |
| Resistor | 1. 5K | 1 | 820 Ω | 680 Ω | 560 Ω | 470 Ω | 330 Ω | 220 Ω | 150 Ω | 100 Ω | |

TRANSISTOR PURCH. SPEC. CAT NO.
VT1 PS 21B 11008



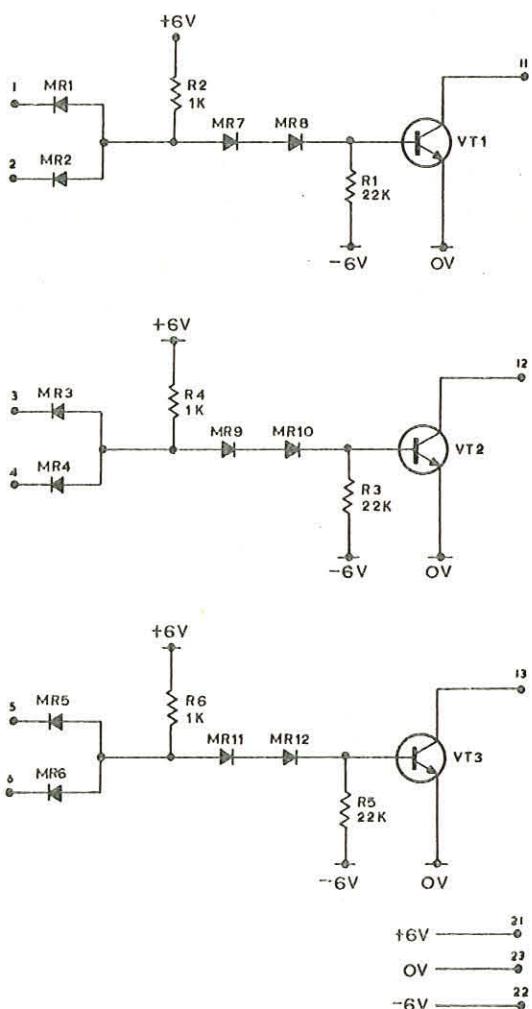
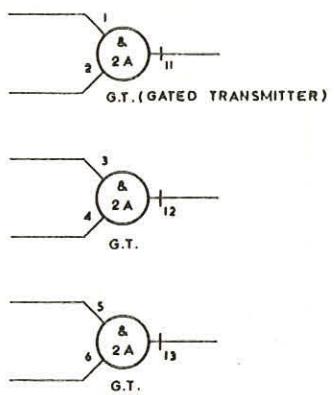
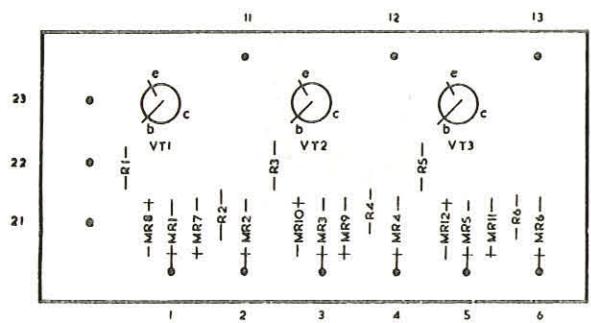
NOTES

1. OUTPUT PULSE POSITIVE.
2. PULSE TRIGGERED BY ANY INPUT REVERTING TO '0' PROVIDED ALL I/P'S HAVE BEEN '1' FOR $\geq \frac{C}{2} \text{ ns}$.
(WHERE C = CAPACITANCE IN pF)
3. R3 AND C2 ARE EXTERNAL.
4. IF R3 = 2.7 K THEN THE PULSE WIDTH = C ns (WHERE C IS CAPACITANCE OF C2 IN pF). INCREASING VALUE OF R3 INCREASE PULSE WIDTH IN PROPORTION.

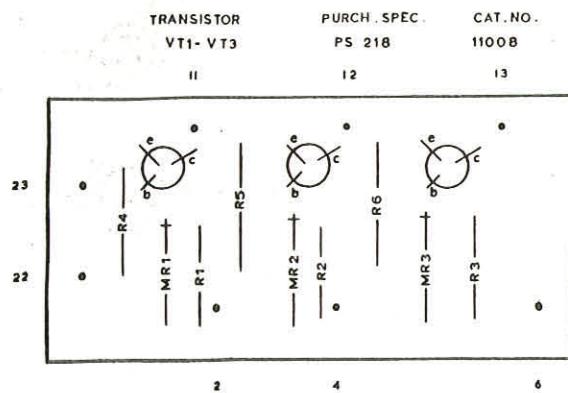
| INPUT LOGIC LEVELS | |
|--------------------|------|
| '1' = | > 2V |
| '0' = | < 1V |

4.6.1.

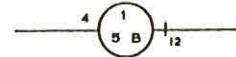
TRANSISTOR PURCH. SPEC. CAT. NO.
VT1~VT3 — 7573



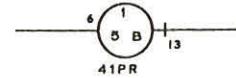
| INPUT LOGIC LEVELS | |
|--------------------|------------------|
| '1' | = $> 2\text{ V}$ |
| '0' | = $< 1\text{ V}$ |



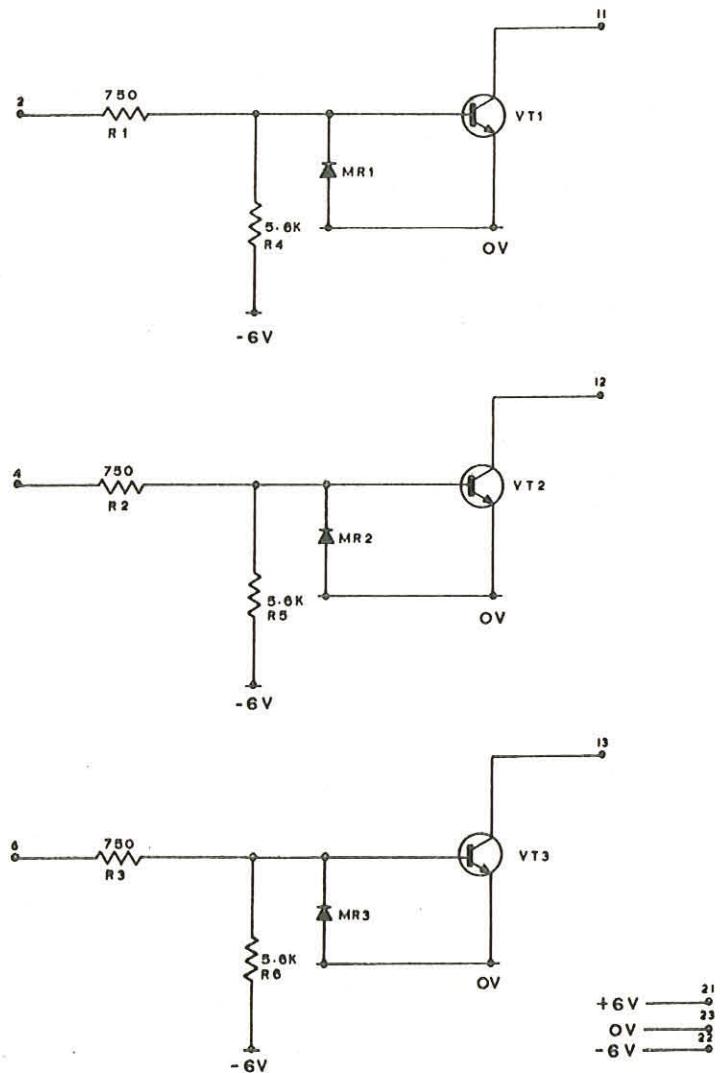
41PR (4100 PERIPHERAL RECEIVER)



41PR



41PR

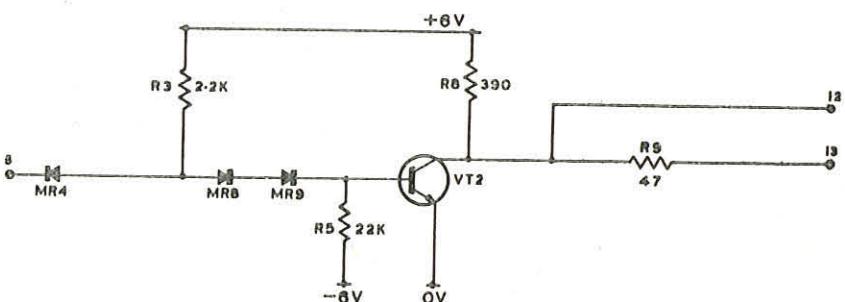
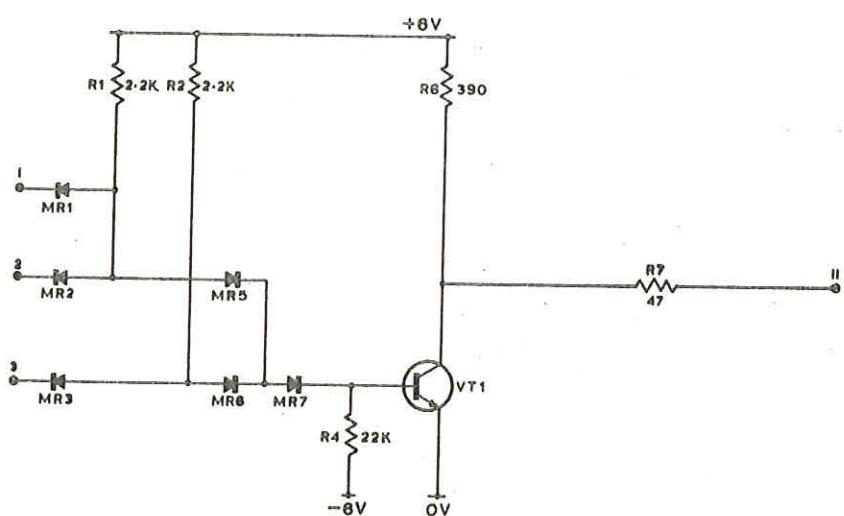
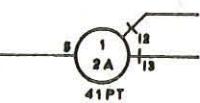
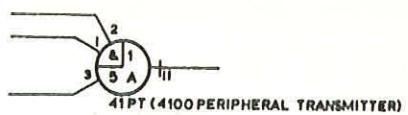
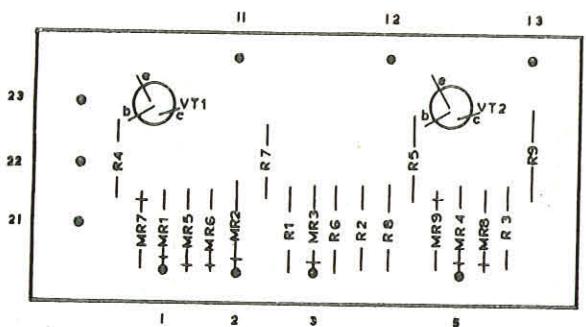


| INPUT LOGIC LEVELS | |
|--------------------|---------|
| '1' | = > 3 V |
| '0' | = < 1 V |

4100 / 900

4.6.1.

TRANSISTOR. PURCH. SPEC. CAT. No.
VT1, VT2. PS 216 11008

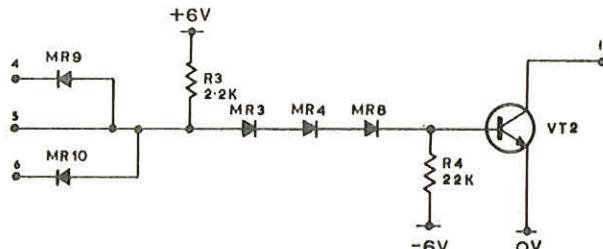
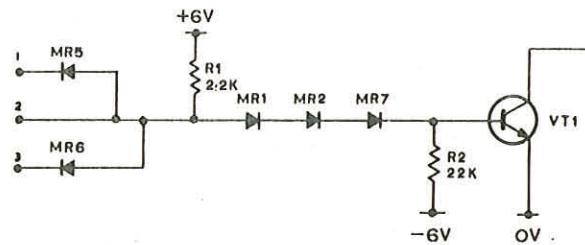
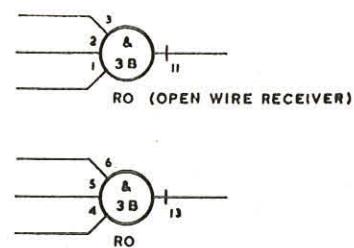
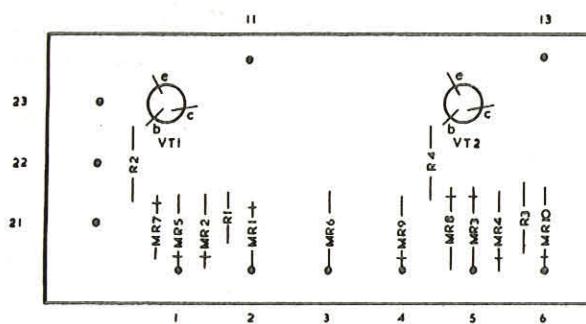


+6V —— o 21
OV —— o 22
-6V —— o 23

| INPUT LOGIC LEVELS | |
|--------------------|----------|
| ↑ | = $> 2V$ |
| ○ | = $< 1V$ |

Figure 48 (ISSUE 2)

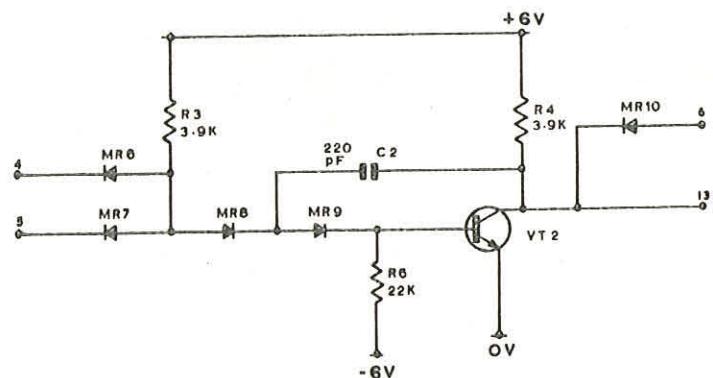
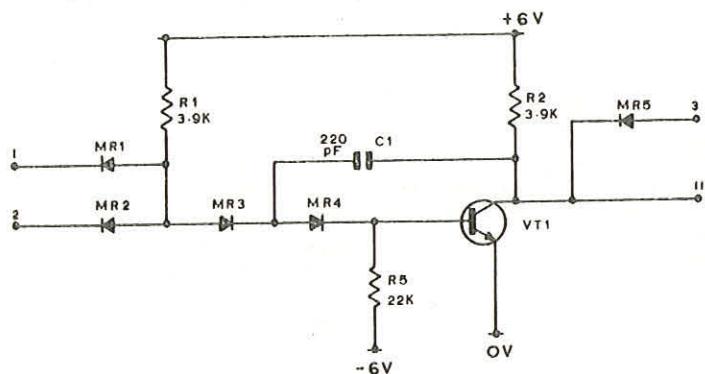
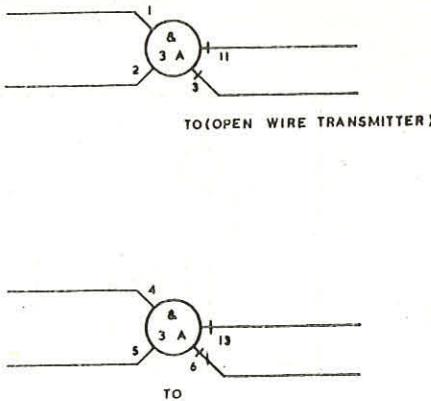
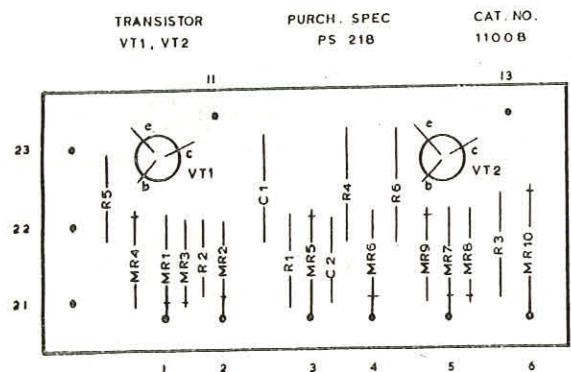
TRANSISTOR PURCH. SPEC CAT. NO.
VT1, VT2 PS 218 11008



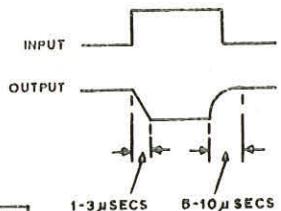
+6V —————— 21
OV —————— 23
-6V —————— 22

NOTE
INPUTS 1,2 AND 4,6, USED WHEN RECEIVING
FROM BUS INPUTS 2 AND 5 OTHERWISE

| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = > 2.5V |
| '0' | = < 1.5V |

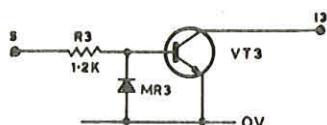
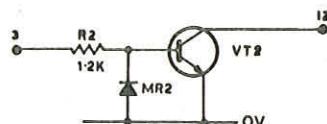
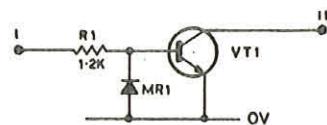
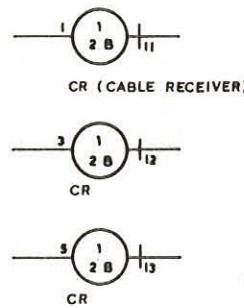
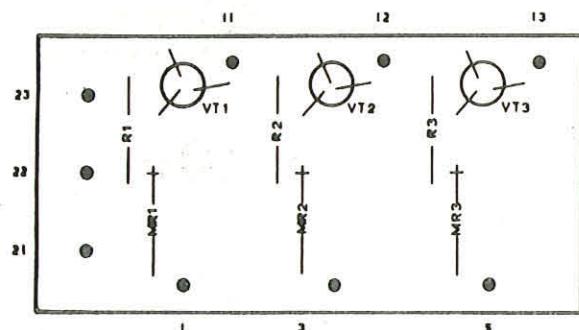


| INPUT LOGIC LEVELS | |
|--------------------|---------|
| '1' | = > 2 V |
| '0' | = < 1 V |



NOTE:-
OUTPUTS 3&6 USED WHEN DRIVING
ON TO BUS. OUTPUTS 11&13 USED OTHERWISE.

TRANSISTOR PURCH. SPEC. CAT. No.
VT1-VT3 PS 218 11008



OV —————— 23

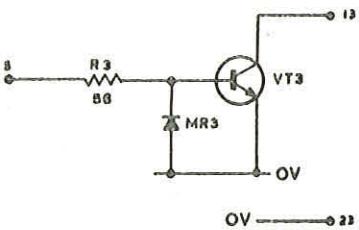
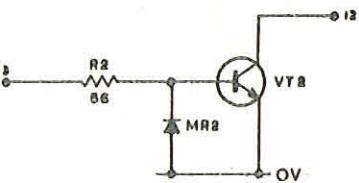
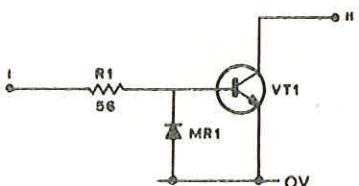
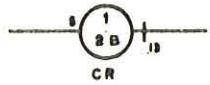
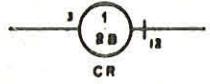
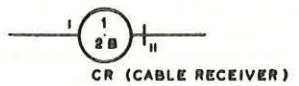
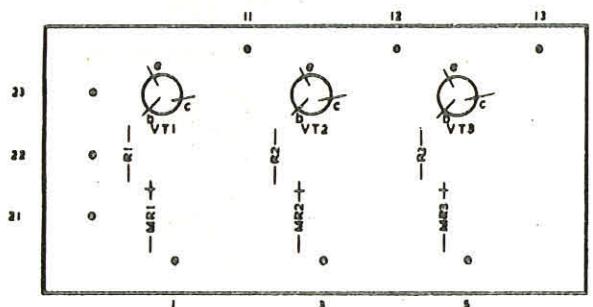
NOTE:-

USED IN CONJUNCTION WITH A SINGLE FAST
CABLE DRIVER LSA.12G FEEDING BUS
OF RECEIVERS.

| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = > 2V |
| '0' | = < 1.5V |

4.6.1.

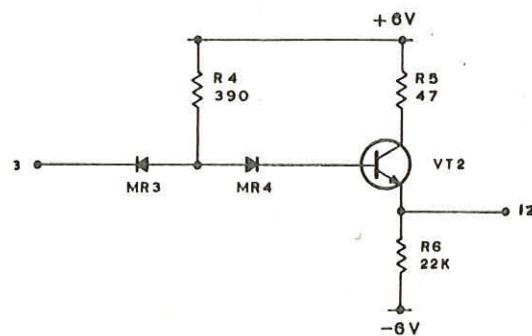
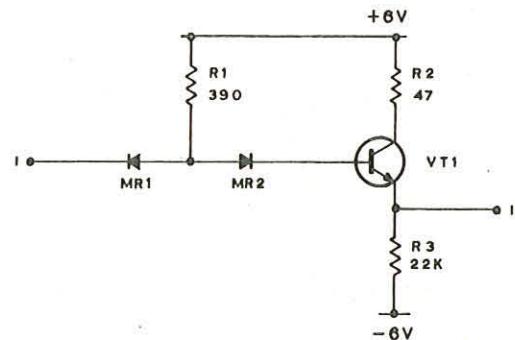
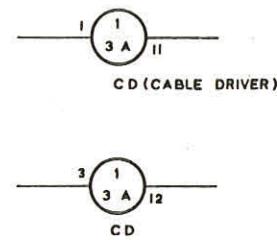
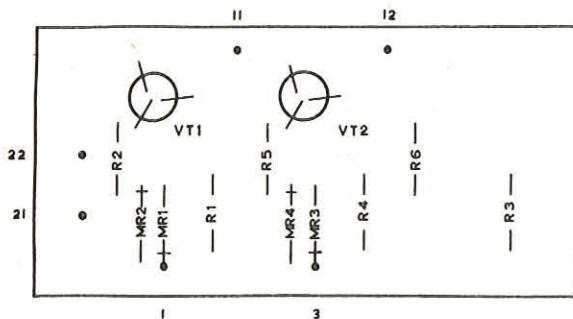
TRANSISTOR PURCH. SPEC. CAT NO.
VT1—VT3 PS 218 1100B



NOTE:
USED IN CONJUNCTION WITH A BUS OFF CABLE
DRIVERS L.S.A. 126 FEEDING A SINGLE RECEIVER.

| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = > 2V |
| '0' | = < 1.5V |

TRANSISTOR PURCH. SPEC CAT. NO.
VT1, VT2 PS 218 11008

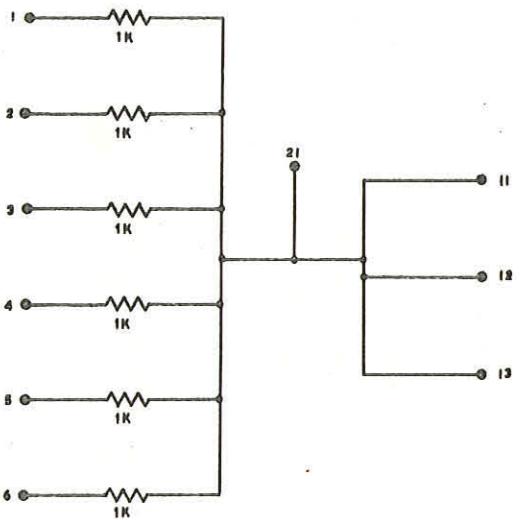
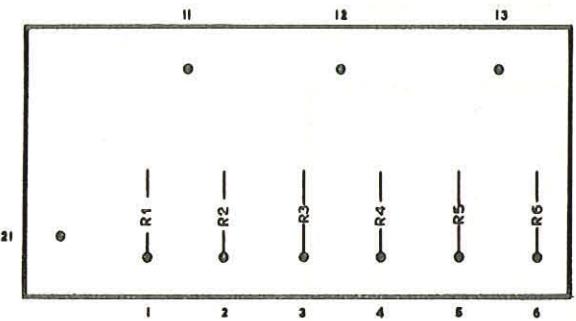


+6V —————— 21
-6V —————— 22

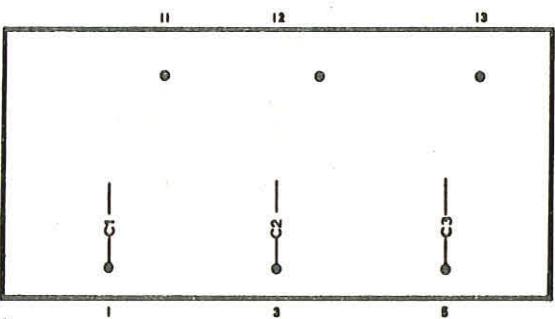
| INPUT LOGIC LEVELS | |
|--------------------|----------|
| '1' | = > 3.5V |
| '0' | = < 1V |

4100/900

4.1.6.



L.S.A. 132



1 ○ — [] — ○ II
470pF

3 ○ — [] — ○ 12
.0012

5 ○ — [] — ○ 13
750pF

L.S.A. 133

Figure 54 (ISSUE 2)

L.S.A.132 & L.S.A.133

TRANSISTOR CAT. No.
VT1—VT3 11740

