

# ELLIOTT

9000

VOLUME 4: ENGINEERING MAINTENANCE

PART 6: LOGIC ELEMENTS

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ERRATA

Figure 25 (Issue 2) - LSA 23.

The mnemonic should be,

"GR (GATED RECEIVER)" and not,  
\* "GD (GATED DRIVER)".

## Chapter 1: INTRODUCTION

### 1.1 General

This section describes the series of logic sub-assembly (LSA) elements used in the 4100 and 900 systems.

The LSA elements are mounted on small boards, each of which can hold from one to three basic logic elements. Up to 21 of these LSA boards are mounted on one of several types of 'mother' board, which is then plugged into the logic shelf.

It is not intended that a LSA should be repaired. If one becomes faulty in any way, the complete LSA should be replaced. Catalogue numbers are given in Appendix 1.

### 1.2 Logic Levels

In the description of the LSA elements it is assumed that a positive logic convention is being used, i. e. that the more positive signal level is logic '1' (=true) and the more negative level is logic '0' (=false). In general the logic levels are 0v (false) and +6v (true). In practice, however, a true signal is often one which is sufficiently positive (e. g. more than +2v) to switch on a transistor, and a false signal is often one which is sufficiently negative (e. g. less than +1v) to switch off a transistor.

The input logic levels for each LSA are given on its circuit diagram. The output logic levels are not quoted as they can usually be deduced from the circuit diagram, and will often vary according to the load placed on the circuit.

### 1.3 Pin Numbers

The pin numbers for the individual LSA boards are not printed on the boards themselves, but are found on the 'mother' board. Most LSA's

have their pins numbered according to a standard system, and it is this pin numbering which is used in all the circuit diagrams in this section. Some LSA's might be encountered, however, which have non-standard pin numbering. The conversion between the two numbering systems is as follows:-

STANDARD PIN NUMBERS		NON-STANDARD PIN NUMBERS
1	-	4
2	-	5
3	-	6
4	-	7
5	-	8
6	-	9
11	-	1
12	-	2
13	-	3

#### 1.4 LSA 'Mother' Boards

LSA boards are mounted on special 'mother' boards. Each 'mother' board is divided up into a number of areas, each of which can accommodate one LSA board. There are also smaller areas on the board for mounting any additional components that may be necessary.

The electrical connections between the LSA boards and the edge connector on the 'mother' board are made by means of printed circuit tracks (for the power supplies) and wire links (for logic signals). The 'mother' boards also usually contain power supply decoupling capacitors.

In one type of 'mother' board, known as a DP board (Figure 1), there are 14 areas in which LSA boards can be mounted, and 34 smaller 'G' areas for additional components. In another type, known as a NV board (Figure 2), there are 21 areas for LSA boards, and 16 small 'Y' areas for additional components.

The various types of 'mother' board used in the 903 central processor are not shown in this section but are fully described in Section 4.1.2 of the 900 Manual.

### 1.5 Logic Symbols and Mnemonics

The symbols and mnemonics shown on the figures are those given in the approved Company document known as "Logic Drawing Standards".

The symbols show (by way of example) how positional information will be given if a grid reference is employed to indicate the position of a LSA on its 'mother' board (such as the "DP" series of logic boards). For example, the "2A" shown in the symbol for the LSA 01 might indicate the position of the three Nand gates on the DP board shown in Figure 1. Each individual Nand gate would then be identified by the numbering of its input and output pins.

Components, external to an LSA, are drawn outside the symbol but connected to the appropriate pins.

## Chapter 2: LSA ELEMENTS

### 2. 1 LSA 01, 02 and 03 Standard Nand Gates (Figures 3, 4 and 5)

LSA 01, 02 and 03 contain standard Nand type logic elements. LSA 01 has three 2-input elements, LSA 02 has two 3-input elements and LSA 03 has a single 4-input element plus two single input inverters. As all the elements function in a similar manner only the first element of LSA 01 will be described.

If the two inputs at pins 1 and 2 are true, diodes MR1 and MR2 are reverse-biased, current flows through the resistor-diode network R2, MR7, MR8 and R1, transistor VT1 is switched on and the output at pin 11 goes false.

If any input goes false, subsequent to both inputs being true, the appropriate input diode is forward biased, VT1 is biased off (base approximately -0.75v) and the output goes true.

### 2. 2 LSA 04 Control Matrix Waveform Amplifiers (Figure 6)

LSA 04 contains three high noise-threshold matrix amplifiers. Each amplifier is used to buffer the output of a matrix diode. The circuit is similar to the standard Nand element except that the input resistance is increased to limit the current through the matrix diode, and an extra diode is inserted in the base circuit to match the output of the matrix line which is +0.9v at logic 0.

### 2. 3 LSA 05 and 06 And/Nor Gates (Figures 7 and 8)

LSA 05 contains a triple 2-input And/Nor gate. LSA 06 contains a dual 2-input And/Nor gate and a standard 2-input Nand gate. The And/Nor gates on both LSA elements are similar, and so only LSA 05 will be described.

When input pins 1 and 2, or 3 and 4, or 5 and 6 are true, the output transistor is biased on and the output is false. If input 1 or 2 is false, together with inputs 3 or 4 and 5 or 6, the transistor is cut-off (base approximately -0.75v) and the output is true.

#### 2.4 LSA 07, 09, 13, 14, 34, 129, 130, 131, 134, 135, 137 and 138 Pulse Generators (Figures 9, 10, 11, 12 and 14)

These pulse generators all have similar circuits, but their pulse widths differ as each has a different time-constant capacitor. As they are similar, except for capacitor value and the option of adding extra capacitors, only LSA 07 will be described.

LSA 07 contains two 3-input pulse generators with one input of each element biased with a 2.4v reference voltage. When all inputs are true the output transistor is conducting and the output is false. If any input or if both inputs go false, subsequent to all inputs being true for greater than  $\frac{C}{2}$  nanoseconds ( $C$  = capacitor value in pF), the common input point (junction of R1, C1, MR1 and MR2) will fall to approximately +1v. This sudden change of voltage will be transmitted through C1 to the base of the transistor, switching it off and making the output true. The capacitor immediately begins to charge, and when the base voltage rises to approximately +0.7v the transistor is switched on and the output becomes false.

Except for LSA 135, the duration of the true output pulse in nanoseconds is equal to  $C$  in picofarads. If the false input returns to true before the normal pulse duration has expired, the output pulse is prematurely terminated.

All capacitor values and pulse widths are given on the appropriate figures.

LSA 135 contains two 3-input pulse generators and the circuit is similar to LSA 07 except for the addition of R5 and different values of R1 and R3. Resistor R5 is provided to prevent output pulses due to noise.

## 2.5 LSA 08 Voltage Reference (Figure 13)

LSA 08 provides a +2.4v reference voltage for the LSA pulse generators. The circuit is an emitter follower with transistor VT2 biased on by resistors R1 and R2. When VT2 is conducting its emitter voltage biases transistor VT1 so that VT1's emitter is at +2.4v. Capacitor C1 is inserted to provide a time constant (R2, C1) sufficiently long to prevent a change of output voltage should there be a sudden surge on the +6v supply. Capacitor C2 acts as a smoothing or de-coupling capacitor.

An external circuit is sometimes connected to pin 6 in order to permit some variation of the reference voltage. This is normally done only to apply test margins to the pulse generators.

## 2.6 LSA 11 Cable Transmitters (Figure 15)

LSA 11 contains three 1-input inverting transmitters. These transmitters are used with cables up to 20 ft. in length, and each always drives one LSA 12 cable receiver element.

Each element is basically a standard one-input inverter (i. e. LSA 03) with R3/R6/R9 added to provide voltage drive. The output is at approximately +4.9v when VT1 is cut off, and at approximately +0.3v when VT1 is conducting.

## 2.7 LSA 12 Cable Receivers (Figure 16)

LSA 12 contains three 1-input inverting receivers. These receivers are always driven by LSA 11 cable transmitter elements.

## 2.8 LSA 15 Nand Gate and Inverting Drivers (Figure 17)

LSA 15 contains one 2-input Nand gate (identical to a LSA 01 element), and two inverting drivers.

## 2.9 LSA 16 F-Minilog Drivers (Figure 18)

This LSA contains three 1-input drivers. Except for the value of the collector load resistor the circuit is identical to the cable transmitter LSA 11.

## 2.10 LSA 17 Paper Tape Receiver (Figure 19)

LSA 17 contains two 1-input receivers. The circuit is similar to the cable receiver LSA 12 except that a collector load resistor has been added.

## 2.11 LSA 18 Noise Rejecting Inverters (Figure 20)

LSA 18 contains three 1-input noise rejecting inverters. They are normally used in the output circuit of key-type switches to reduce the effects of contact bounce.

If a momentary '1' is applied to the input it has insufficient time to charge up C1 to the level necessary to switch on the transistor. The time constant of C1 R2 is 1 mS. When the input goes to '0' C1 is virtually short circuited and the transistor is switched off with little delay.

Occasionally, however, this circuit has been used solely to obtain a delay of approximately 1 mS in a positive-going waveform.

## 2.12 LSA 19, 20, 21, 24 and 25 Delayed Start Elements (Figures 21, 22 and 23)

A delayed start element is always made up of two elements in

series. The first element can be LSA 20, 21, 24 or 25, depending on the time delay required, and the second element is always LSA 19. The time delay is 10 mS per  $\mu$ F of capacitance in the first element.

The logic rules for the complete element are as follows.

When the input goes to '1' the output goes to '0' with no delay. When the input goes to '0' the output goes to '1' after a delay. Thus, when a negative-going pulse is applied to the input, a positive going output pulse is obtained with its leading edge delayed.

LSA's 20, 24 and 25 are identical except for the values of C1 and C2. LSA 21 is identical to LSA 24 except that C2 is omitted. The delays introduced by these elements are shown in the appropriate figures.

The complete circuit operates in the following manner. The input going to a '1' switches on VT1, which in turn switches on VT2. VT2 switching on rapidly discharges C1 (or C1 and C2 in parallel), and thus causes VT3 to be switched off, and VT4 to be switched on, so making the output a '0'. When the input goes to '0' VT1 and VT2 are switched off and C1 charges up via R5, R6 and R7. When the junction of R6 and R7 reaches a sufficiently positive voltage VT3 is switched on, and VT4 is switched off, thus making the output a '1'.

#### 2.13 LSA 22 Two-Input Transmitters (Figure 24)

LSA 22 contains three 2-input non-inverting transmitters. These transmitters always drive LSA 23 gated receivers.

#### 2.14 LSA 23 Gated Receivers (Figure 25)

This LSA contains three receivers. Each receiver has one signal input (pins 2, 4 and 6) and one inhibit input (pins 1, 3 and 5). When the inhibit input is true the output is permanently true; when the inhibit input is false, the output is the inverse of the signal input.

## 2.15 LSA 26 Nand Gate and Lamp Driver (Figure 26)

LSA 26 contains two 2-input Nand gates (identical to LSA 01 gates), and a 28v, 40 mA lamp driver.

## 2.16 LSA 27 Regenerable Monostable (Figure 27)

The logic rules for this element are as follows. When the input goes to '0' the output goes to '1' with no delay; when the input goes to '1' the output goes to '0' after a delay. Thus, if a negative-going pulse is applied to the input, a positive-going output pulse is obtained with the trailing edge delayed (see timing diagram in Figure 27).

The duration  $t_o$  of the output pulse is  $t_i$  (duration of input pulse) plus  $t_d$  (delay time). With no external components fitted  $t_d$  is 25 mS  $\pm$  30%.  $t_d$  can be increased up to a maximum of 5 seconds by shunting C1 with an external capacitor, and can be decreased to a minimum of 1 mS by shunting R6 with an external resistor.

The circuit operates as follows. When the input goes to '0' VT3 is switched on, which in turn switches on VT2. VT2 switching on causes C1 to rapidly charge. When C1 is charged its top plate is at approximately -5v, so reverse biasing MR2 and cutting off VT1, and thus making the output a '1'. When the input goes to '1' VT3 is switched off, so in turn switching off VT2. When VT2 switches off C1 begins to charge in the opposite direction via MR1 and R6. When the capacitor has charged up sufficiently VT1 is turned on and the output falls to a '0'.

The output pulse is "regenerable" in that a second negative-going pulse, occurring during  $t_d$ , will cause the delay to be timed from the trailing edge of the second pulse. The output pulse is thus prolonged, and may be prolonged indefinitely by a succession of input pulses of sufficiently high periodicity. It ends  $t_d$  milliseconds after the trailing edge of the last input pulse.

### 2.17 LSA 28 Gated Drivers (Figure 28)

This LSA contains three 2-input Nand elements. Except for R2/R4/R6, the reduced value of which provides a larger fan-out, the circuits are identical to those of LSA 01 elements.

### 2.18 LSA 29 Teleprinter Receiver (Figure 29)

This LSA contains one teleprinter receiver which converts the 20 mA working current signal from a Type 33 Teleprinter to a logic signal.

If the cable feeding the receiver is between 100 ft. and one third of a mile in length, input pin 6 is connected to pin 4 by a  $470\Omega$  resistor via pads 10 and 12. If the cable is between one third of a mile and two thirds of a mile the  $470\Omega$  resistor is replaced by a  $120\Omega$  resistor. If the cable is between two thirds of a mile and a mile in length input pin 6 is shorted directly to pin 4.

A mark (20 mA) input at pin 6 switches VT1 off, and VT2 on, and so makes the output a '0'. A space (floating) input allows VT1 to switch on, so causing VT2 to switch off and making the output a '1'.

### 2.19 LSA 30 Teleprinter Line Driver and And/Or Gate (Figure 30)

LSA 30 contains one inverting teleprinter line driver and one And/Or gate.

If the cable being driven by the driver is between 100 ft. and a third of a mile long, output pin 13 is connected to pin 12 by a  $470\Omega$  resistor via pads 8 and 6. If the cable is between one third of a mile and two thirds of a mile the  $470\Omega$  resistor is replaced by a  $120\Omega$  resistor. If the cable is between two thirds of a mile and a mile in length output pin 13 is shorted directly to pin 12.

A mark (0v) input at pin 6 switches VT3 on and its collector current of approximately 20 mA is the line signal. A space (floating) input at pin 6 switches VT3 off, and terminates the output current.

The And/Or circuit consists of a 3-input And gate and a 2-input And gate feeding a 2-input Or gate, with the resulting output being doubly inverted by VT1 and VT2.

#### 2.20 LSA 31 and 32 NPL Interface Delay and Schmitt Trigger (Figures 31 and 32)

LSA 31 is an inverting delay circuit, and LSA 32 is a Schmitt trigger. LSA 31 is used in conjunction with LSA 32 as shown in Figure 32. The smoothing effect of the delay circuit together with the fairly high threshold voltage of the Schmitt trigger ensures that the trigger is not switched by noise on the interface lines.

When used in conjunction with LSA 32, and with a 0.047  $\mu$ F external capacitor, the delay element introduces a 100  $\mu$ s delay between a positive-going edge at pin 5 and the resulting negative-going edge at pin 11. The delay between the negative-going edge at pin 5 and the resulting positive-going edge at pin 11 is less than 10  $\mu$ s.

The Schmitt trigger circuit, LSA 32 performs the usual function of converting slowly changing waveforms into pulses with fast edges. When the input is rising positively the threshold is +3.1v, and at this point VT2 switches on and VT1 switches off, so making the output true. When the input is falling negatively the threshold is +2.4v, and at this point VT2 switches off and VT1 switches on, so making the output false.

#### 2.21 LSA 33 Level Shifter (Figure 33)

LSA 33 contains three 1-input level shifters. Each element converts input levels of 0v and -6v to 0v and +6v respectively. The level shifters thus invert signals passing through them, and at the same time raise the logic levels by 6v.

## 2.22 LSA 35 and 36 NPL Transmitters and Receivers (Figures 34 and 35)

LSA 35 contains three 1-input inverting transmitters, and LSA 36 contains three 1-input inverting receivers.

## 2.23 LSA 37, 39, 40, 41 and 42 Pulse Generators (Figure 36)

Each of these LSA's contains two 3-input pulse generators. Except for the value of the time constant capacitor all these LSA's are identical.

The circuits are similar to those of LSA 07 etc. except that a noise rejecting circuit R5/R6, C3/C4 has been added.

As in LSA 07 etc. the circuit is triggered by any one input going false subsequent to all inputs being true for greater than  $C/2$  nanoseconds, where  $C$  is the value of  $C_1$  (or  $C_2$ ) in picofarads. The duration of the true output pulse in nanoseconds is always equal to  $C_1$  (or  $C_2$ ) in picofarads. The various capacitor values are given in Figure 36.

## 2.24 LSA 38 Single Pulse Generator (Figure 37)

LSA 38 contains a single pulse generator. The circuit is triggered by a negative-going edge at either input, provided that the other input is not already negative. The output pulse is positive-going and is of  $1.36 \times C_2 \text{ nS} \pm 36\%$  duration, where  $C_2$  (the external capacitor) is in picofarads.

The circuit consists of a Nand gate followed by a conventional monostable multivibrator. Under quiescent conditions VT3 is conducting and VT2 is cut off, so that the output is false. When either input goes negative VT1 is cut off and its collector goes positive. This positive-going transition is transmitted via  $C_1$  to the base of VT2, and causes this transistor to switch on and VT3 to switch off in the usual way. The output

thus goes true. The junction of C2 and R5 now rises positively as C2 charges up via VT2 and R5, and when the junction becomes sufficiently positive VT3 is switched on and VT2 is switched off, thus making the output false again.

#### 2.25 LSA 43 Voltage Rail Sensing

This is a very specialised LSA element and will not normally be met with in 4100/900 equipment.

#### 2.26 LSA 44 Nand Gate (Figure 38)

This LSA contains three 2-input Nand gates. Each element is identical to a LSA 01 except that diodes MR1/3/5 are replaced by direct links. These gates are always driven by LSA 23 gated receivers. The output from the gated receiver is connected to the direct input (pin 1/3/5), while the controlling signal is connected to the diode input (pin 2/4/6).

#### 2.27 LSA 45 Modified Fast Cable Driver (Figure 39)

This is a modified fast cable driver (LSA 126). When only one load is being driven the emitter resistor R4/R9 is shunted by R5/R10 (by connecting pin 2/4 to -6V). When more than one load is being driven pin 2/4 is left open circuit and the emitter resistor is not shunted.

#### 2.28 LSA 46 Counter Bistable (Figure 40)

This LSA contains one bistable circuit. The unmodified circuit forms a shift register type of element, but by connecting together pins 13 and 5, and 12 and 1, however, a binary counter element is formed.

The bistable is set by a negative-going edge applied to pin 3 when pin 1 is already negative, and is reset by a negative-going edge at pin 3 when pin 5 is already negative. The bistable can also be set or reset by negative levels applied to pins 2 or 6 respectively.

The circuit is that of a conventional bistable multivibrator with steering circuits. Depending on the inputs at pins 5 and 1 the negative-going triggering edge is applied to the base of either VT1 or VT2. If pin 5 is negative the edge is steered to VT1, but if pin 1 is negative, the edge is steered to VT2. The negative-going edge begins to switch off the transistor to which it is applied (provided it is not already off) and so initiates the rapid switching of the bistable to the opposite state. Positive-going edges at the clock input have no effect.

When the circuit is connected as a counter element the steering voltages at pins 1 and 5 are always such that the triggering edge is steered to the transistor which is conducting. The result is that the bistable changes state every time a triggering edge is received.

When the circuit is used in a shift register the output of each element are connected to the steering inputs of the following element. The way in which any element switches when a trigger pulse is applied is therefore determined by the state of the previous element.

#### 2.29 LSA 47 Balanced Pair Transmitter (Figure 41)

This LSA contains one  $115\Omega$  balanced pair transmitter which converts logic signals of +6v and 0v to push-pull signals of +0.25v and -0.25v.

Provided that one input is true, a signal applied to the other input will produce equal antiphase signals at the two outputs. The output at pin 12 is in antiphase with the input, while that at pin 13 is in phase with the input.

Signals at pins 5 and 6 are applied via the And gate to the phase-splitter stage VT1. The equal antiphase outputs from VT1 are applied to the common-base stages VT2 and VT3 respectively which drive the two wires of the transmission line.

### 2. 30 LSA 48 Balanced Pair Receiver (Figure 42)

This contains one  $115\Omega$  balanced pair receiver which converts push-pull signals of +0. 25v and -0. 25v to logic signals of +6v and 0v.

When input pin 3 is at +0. 25v and input pin 4 is at -0. 25v the output is true. When any other input conditions prevail the output is false.

The input signals at pins 3 and 4 are applied to the differential amplifier formed by VT1 and VT2, and the output of VT2 is amplified and inverted by VT3. Only when VT2 base is at +0. 25v and VT1 base at -0. 25v is VT2 conducting hard enough to cut off VT3, and so make the output true.

### 2. 31 LSA 49 Crystal Oscillator (Figure 43)

LSA 49 contains a crystal oscillator and driver. The crystal controlled Colpitts oscillator, VT1, has a frequency of  $2.5 \text{ Mc/s}^+ 0.03\%$ . The output of VT1 is amplified and inverted by VT2 and VT3 to produce positive-going pulses of 6v amplitude and 160 nS duration with a repetition rate of 400 nS. The crystal is mounted externally.

### 2. 32 LSA 50 Delay Element and Nand Gate (Figure 44)

This LSA contains a delay element and a 3-input Nand element. The Nand gate is identical to a LSA 02.

The logic rules for the delay element are as follows: When the input goes to '1' the output goes to '0' after a pre-set delay of time TR. When the input goes to '0' the output goes to '1' after a much shorter delay TF. Thus, when a positive-going pulse is applied to the input, a negative-going output pulse is obtained with its leading edge delayed. The formulae for calculating TR and TF are given in Figure 44.

The delay circuit is always fed from a collector without a "pull-up" resistor. The circuit operation is as follows. When the transistor in the previous stage is switched off the input at pin 3 rises positively from 0v as CX is charged up via VT1 and R3. When, after time TR, the voltage at pin 3 reaches +1.3v, VT2 switches on and the output falls to 0v. When the input at pin 3 falls to 0v, CX discharges rapidly through the  $10\Omega$  resistor R1, VT2 is switched off and the output goes to a '1' with little delay. Resistor R1 ensures that the surge of discharge current from CX does not exceed the collector current rating of the previous transistor.

#### 2.33 LSA 51 Variable Pulse Delay (Figure 45)

LSA 51 contains one variable pulse delay element. The circuit is similar to that of LSA 129 except that both the resistor and the capacitor of the timing circuit are external, and a noise rejection circuit R2,C1 has been added.

#### 2.34 LSA 54 Transmitters (Figure 46)

This LSA contains three 2-input transmitters. Each element is identical to an LSA 01 element except that R2/R4/R6 has been changed to 1K, and a different transistor has been used which allows a larger swing (from 0v to +15v) at the output.

#### 2.35 LSA 120 4100 Standard Interface Receivers (Figure 47)

This LSA contains three 1-input inverting receivers. The diode in the base circuit protects the base-emitter junction from high reverse voltages.

#### 2.36 LSA 121 4100 Standard Interface Transmitters (Figure 48)

LSA 121 contains two elements, a 3-input And /Or gate followed by an inverting transmitter, and a 1-input inverting transmitter.

If input pins 1 and 2, or 3 are true, transistor VT1 is biased on and the output is false. If pins 1 or 2, and 3 are false, VT1 is switched off and the output is true. R7 is for matching purposes.

The second element is a standard Nand gate with a  $390\Omega$  'pull up' resistor. Pin 12 may be used to enable another Nand gate or inverter to drive the same interface line via the common  $47\Omega$  matching resistor.

#### 2.37 LSA 122 Open Wire Receivers (Figure 49)

This contains two 3-input inverting receivers. Inputs 1, 3, 4 and 6 are used for receiving information from bus lines. Inputs 2 and 5 are used for other lines. (See also LSA 123).

#### 2.38 LSA 123 Open Wire Transmitters (Figure 50)

This LSA contains two 2-input Nand gate transmitters. The outputs at pins 3 and 6 are gated with other paralleled outputs (to feed a common line) and are transmitted to the inputs on pins 2 and 5 on LSA 122. Alternatively, the outputs at pins 11 and 13 may be used to drive a 'bus' which supplies a number of LSA 122 elements (pins 1, 3, 4 and 6). C1 and C2 are used to slow down the edges of the output waveforms.

#### 2.39 LSA 124 and 125 Fast Cable Receiver Slave and Master (Figures 51 and 52)

Both of these LSA's contains three 1-input inverting receivers. The only difference between LSA 124 and 125 is in the value of base resistor, which is 1.2K in LSA 124 and  $56\Omega$  in LSA 125. (See the notes on Figures 50 and 51).

2. 40 LSA 126 Fast Cable Transmitters (Figure 53)

This contains two 1-input non-inverting transmitters. Each element consists of an emitter-follower stage having an output impedance of  $50\Omega$ .

2. 41 LSA 132 and 133 Miscellaneous Components (Figure 54)

The components on these LSA's are used with pulse generator LSA 134 to vary the width of its output pulse.

2. 42 LSA 136 Level Shifters (Figure 55)

This LSA contains three 1-input level shifters. Each element converts input levels of 0v and -10v to 0v and +6v respectively.

Appendix 1: LSA CATALOGUE NUMBERS

LSA No.	Cat.No.	LSA No.	Cat.No.	LSA No.	Cat.No.
01	10864	30	10893	120	10894
02	10865	31	11251	121	10895
03	10866	32	11252	122	10896
04	10867	33	11177	123	10897
05	10868	34	(MCD Drg. No. 322B7582)	124	10898
06	10869	35	11253	125	10899
07	10870	36	11254	126	10900
08	10871	37	11760	127	-
09	10872	38	11761	128	-
10	-	39	11762	129	10903
11	10874	40	11763	130	10904
12	10875	41	11764	131	10905
13	10876	42	11765	132	10906
14	10877	43	(MCD Drg. No. 322B7736)	133	10907
15	10878	44	(MCD Drg. No. 322B7897)	134	10908
16	10879	45	11949	135	10909
17	10880	46	14329	136	10910
18	10881	47	14330	137	10911
19	10882	48	14331	138	10912
20	10883	49	14332		
21	10884	50	14333		
22	10885	51	(CPG Drg. No. B23288)		
23	10886				
24	10887				
25	10888				
26	10889				
27	10890				
28	10891				
29	10892				