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ANDREW K. DAVIS

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US Citizen
Secret Security Clearance

Professional Summary

I am an FPGA Engineer with 5 years of VHDL industry experience, and I am looking for opportunities to accelerate my technical proficiency and career growth. I have been both an individual contributor since 2019, and I have led a small team of firmware engineers since the beginning of 2024. My work has been primarily Zynq Ultrascale+ family of devices, with a focus on DAC/ADC RF Data Converter and 10G Ethernet IP.

Skills

- Languages: Python, TCL, VHDL (CocoTB Simulation, Hardware Integration)
- Standards: AXI4-Stream, AXI4-Lite, MORA, Ethernet II, UART, I2C, SPI
- Software: LaTeX, Git, Perforce, MS Visio, Linux
- Hardware: Zynq US+ RFSoC (XCZU28DR:ZCU111, XCZU43DR, XCZU47DR), Zynq US+ MPSoC (XCZU9EG:ZCU101, XCZU7EV:ZCU106, XCK26:Kria K26), Artix US+ ()
- Functional: Mentorship, Tasking, Sprint Standups

Education

Clarkson University *Potsdam, NY* May 2019
Bachelor of Science in Computer Engineering | 3.520 GPA

Undergraduate Research: *3D Fingerprint Scanning and Modeling*
Created a prototype to scan and produce 3D renders of users fingerprints. Helped to develop an algorithm in C++ to project and unwrap the 3D renders into fingerprint rolls. Presented the prototype and research at the IARPA N2N Challenge 2017 in Laurel, Maryland.

Work Experience

SRC Inc *Syracuse, NY* October 2023 – Present
Acting Lead Firmware Engineer

- Interview team member for the Firmware Engineering department; performed over 20 interviews, evaluating technical skill and a candidate's overall fit for the company and department.
- Act in a lead role to oversee a team of 2-3 engineers; lead daily standups and assign bi-weekly Sprint tasking.
- Act as the responsible individual for Functional Overview architecture and documentation.
- Oversee Detailed Design architecture and documentation, coding and simulation, and hardware integration.
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SRC Inc *Syracuse, NY* June 2019 – Present
Firmware Engineer

- Created SVD to Latex Python command line tool. Automatically generated Latex based off the CMSIS SVD specification. Tool was used to generate memory-mapped documentation for AXI4-Lite register, FIFO, and RAM memory style regions.
- Detailed Design, Code and Simulation for a CORDIC Processing IP. Designed using a CORDIC Rotation processor that could accept pipelined requests. (what FPGA?)
- Detailed Design, Code and Simulation for a DAC8771 (single channel, 16bit) AXI4-Lite to SPI interface. Also used Python script to configure and set output voltages via SPI, through AXI4-Lite commands issues through Zynq US+ PS. Verification performed with Oscilloscope. (what FPGA?)
- Detailed Design, Code and Simulation for an electrical Resolver (azimuth/elevation/speed) feedback loop. (what FPGA?)
- Detailed Design, Code and Simulation for an I/O Recoder IP. Could detect edge detections on GPIO and would record and store time deltas between transitions. Stored in BRAM and could be later played back for debugging efforts. (what FPGA?)
- Updated existing RFDC block design to use all 7 DACs across 2 Tiles. Integrated IFGEN