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ANDREW K. DAVIS

US Citizen
Secret Security Clearance

Professional Summary

I am a VHDL FPGA Engineer with 5 years of industry experience. I have been both an individual contributor, and I have lead a small team of firmware engineers since the beginning of 2024. My work has been primarily Zynq Ultrascale+ family of devices, with a focus on DAC/ADC RF Data Converter and 10GbE Ethernet IP.

Skills

- Languages: Python, TCL, VHDL (CocoTB Simulation, Hardware Integration)
- Standards: AXI4-Stream, AXI4-Lite, MORA, Ethernet II, UART, I2C, SPI
- Software: LaTeX, Git, Perforce, MS Visio, Linux
- Hardware: Zynq US+ RFSoC (XCZU28DR:ZCU111, XCZU43DR, XCZU47DR), Zynq US+ MPSoC (XCZU9EG:ZCU101, XCZU7EV:ZCU106, XCK26:Kria K26), Artix US+ ()
- Functional: Mentorship, Tasking, Sprint Standups

Education

Clarkson University *Potsdam, NY*   May 2019
Bachelor of Science in Computer Engineering | 3.520 GPA
   Undergraduate Research: *3D Fingerprint Scanning and Modeling*
   Created a prototype to scan and produce 3D renders of users fingerprints. Helped to develop an algorithm in C++
   to project and unwrap the 3D renders into fingerprint rolls. Presented the prototype and research at the IARPA
   N2N Challenge 2017 in Laurel, Maryland.

Work Experience

SRC Inc *Syracuse, NY*   October 2023 – Present
Acting Lead Firmware Engineer
- Interview team member for the Firmware Engineering department; performed over 20 interviews, evaluating technical skill and a candidate's overall fit for the company and department.
- Act in a lead role to oversee a team of 2-3 engineers; lead daily standups and assign bi-weekly Sprint tasking.
- Act as the responsible individual for Functional Overview architecture and documentation.
- Oversee Detailed Design architecture and documentation, coding and simulation, and hardware integration.
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SRC Inc *Syracuse, NY*   June 2019 – Present
Firmware Engineer
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