andrewdavis
andrewkdavis.com
andrewkdavis97

ANDREW K. DAVIS

andrewkdavis@protonmail.com
115 Solar Street, Apartment 407
Syracuse, NY 13204
(315) 630-8565

US Citizen with Security Clearance

Professional Summary

I am an FPGA Engineer with 5 years of VHDL industry experience. I am looking for opportunities to accelerate my technical proficiency and growth. I have been both an individual contributor since June 2019, and I have been a team lead since October 2023. My work has been primarily with Zynq Ultrascale+ family of devices.

Education

Clarkson University *Potsdam, NY* August 2015 – May 2019

GPA 3.520, Bachelor of Science in Computer Engineering

Undergraduate Research *3D Fingerprint Scanning and Modeling*

Created a prototype to photograph fingers and output 3D renders. Helped develop an algorithm in C++ to unwrap the 3D renders into nail-to-nail fingerprint rolls. Presented at the 2017 IARPA N2N Challenge in Laurel, Maryland.

Work Experience

SRC Inc *Syracuse, NY* June 2019 – Present

- As team lead: oversee a team of 2-3 engineers; lead daily standups; assign bi-weekly tasking.
- As individual contributor: architecture and documentation; coding and simulation; hardware integration.
- As interview team-member: performed over 20 interviews, where I evaluate technical skill; and evaluate culture fit.

RF Front End *MPSoC, XCAU15P, Team Lead* October 2023 – Present

- Lead a team of 3 engineers to design, simulate, and implement firmware targetting the FPGA.
- FPGA design for Artix Ultrascale+ RF Front End card. Matched hardware requirements to FPGA IO planning and clock management.
- Designed firmware that queues RF Control MORA messages and communicates with off-card hardware (filter shift registers, amplifiers, attentuators).
- Implemented manual clock routing for external clock source and performed post route timing analysis.

SDR *RFSoC, XCZU43DR, Lead* May 2023 – September 2023

- FPGA design for Zynq Ultrascale+ AMS WB3XR2 Dual RFSoC. Matched hardware requirements to FPGA IO planning.
- Designed high level AXI4L memory map between RFSOC0 and RFSoC1. Documented the allocation of 4.25GB of user space addressable by each RFSoCs programmable logic.
- Performed initial bringup of card using TCL build scripts and Petalinux image using third party IP and Zynq US+ block design.

DAC Stimulator *RFSoC, ZCU111, Individual Contributor* December 2020 – May 2022

- Integrated 10GbE with SFP PHY/MAC. An external PDW generator sent ethernet packets containing transmit-scheduled pulse descriptor words. Designed message parsing logic on top of the extracted UDP data to extract the fields needed for transmit on the ZCU111 DACS.
- Designed AXI4-Lite controlled I/Q scaling. Scale factors were multiplied onto I/Q from full scale (1) down to zero. Polar inputs converted to complex I/Q and fed into complex multipliers against a single I/Q data stream from the transmit scheduler.

Motor Control *MPSoC, ZCU106, Individual Contributor* December 2019 – November 2020

- Motor control with DAC8771 (single channel, 16bit DAC). AXI4-Lite to SPI interface. Wrote to DAC registers via SPI from Zynq US+ PS interfaced through Python. Verification with Oscilloscope.

SVD to LaTeX *Python, Individual Contributor* June 2019 – November 2019

- Created SVD to LaTeX tool in Python, based off of CMSIS SVD specification. This tool generates memory-mapped documentation for AXI4-Lite regions: register, FIFO, and RAM memory styles.

Skills

- **Hardware**: Zynq US+ RFSoC/MPSoC, Zynq7000, Artix US+
- **Software**: VSCode, Git, JIRA, Perforce, Confluence, MS Visio, LaTeX, Linux, Windows
- **Languages**: VHDL, TCL, Python (VUnit/CocoTB simulation, and integration scripting)
- **Functional**: Mentor, Strong Communicator, Team Player, Self Motivator, Book Reader