CPE 151/EEE 234
Digital IC Design

Project No. 2

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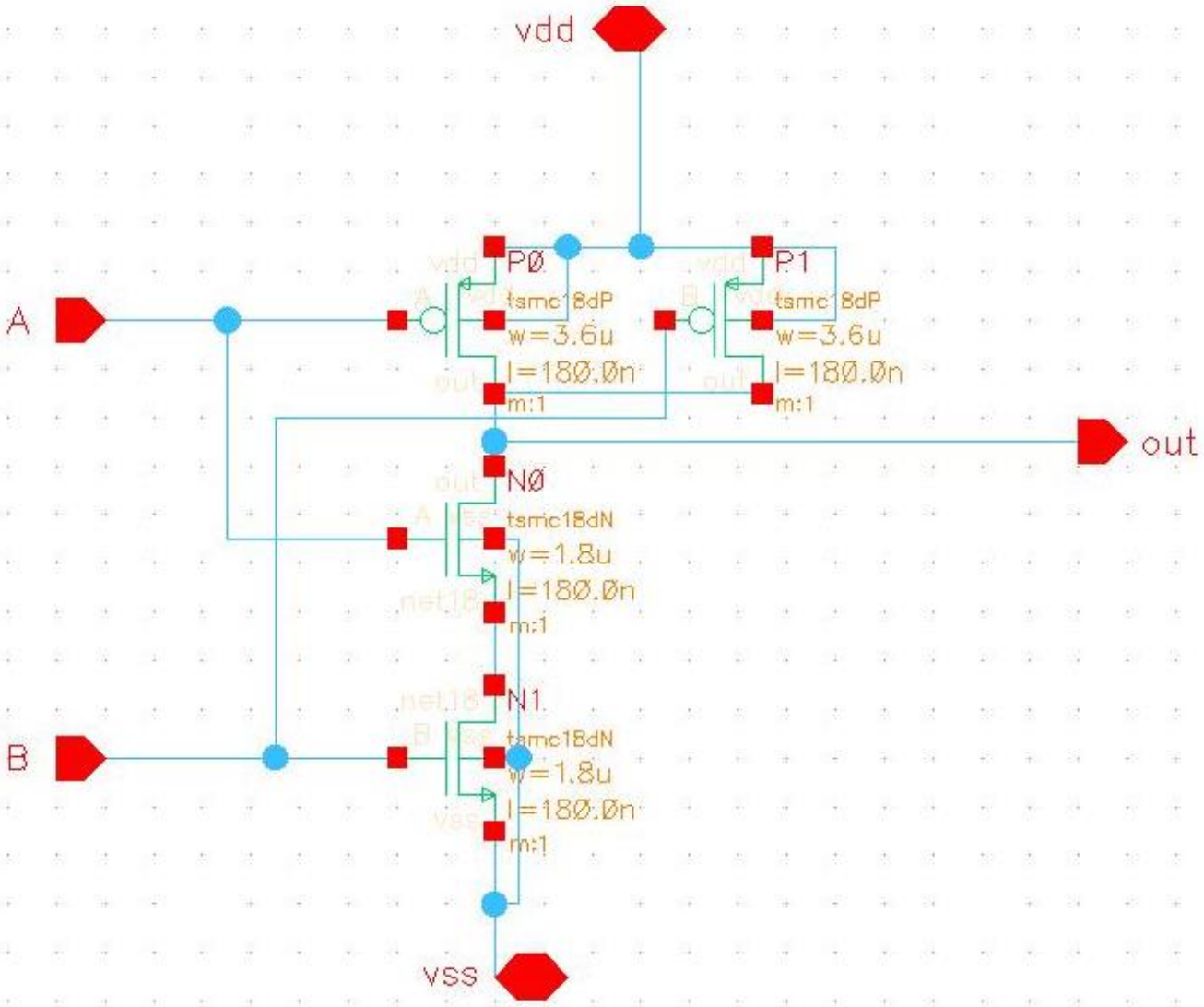
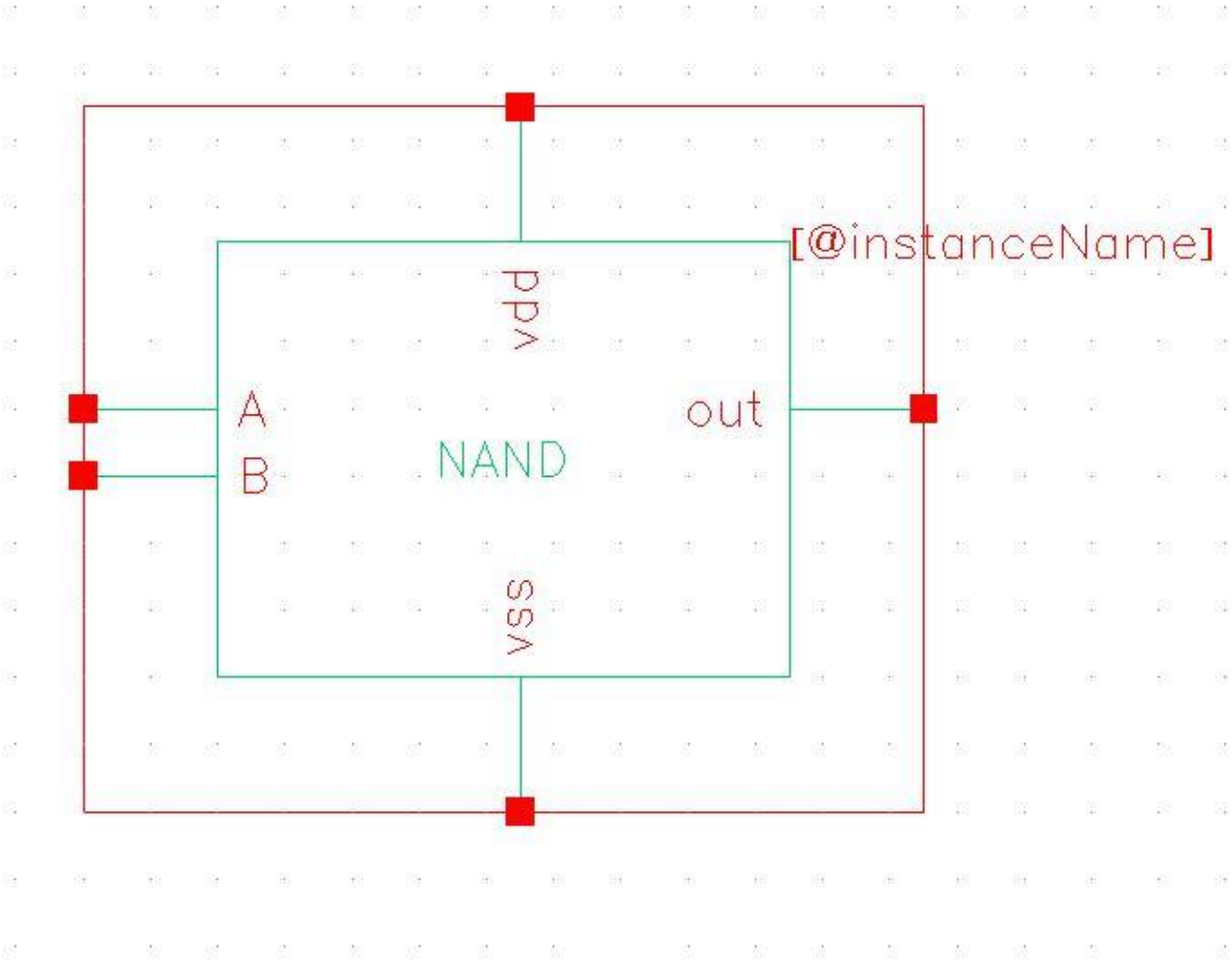
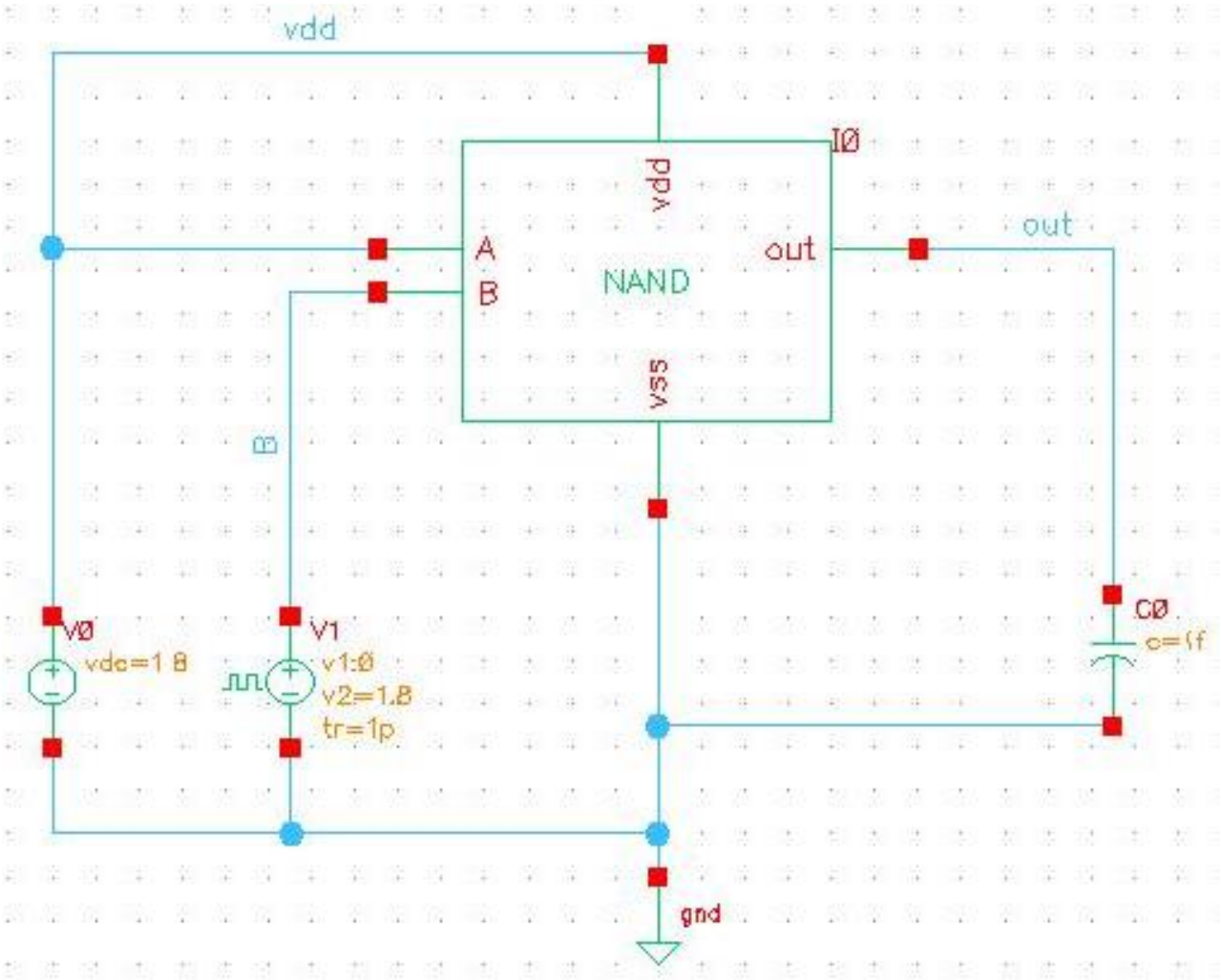
2-Input NAND Schematic



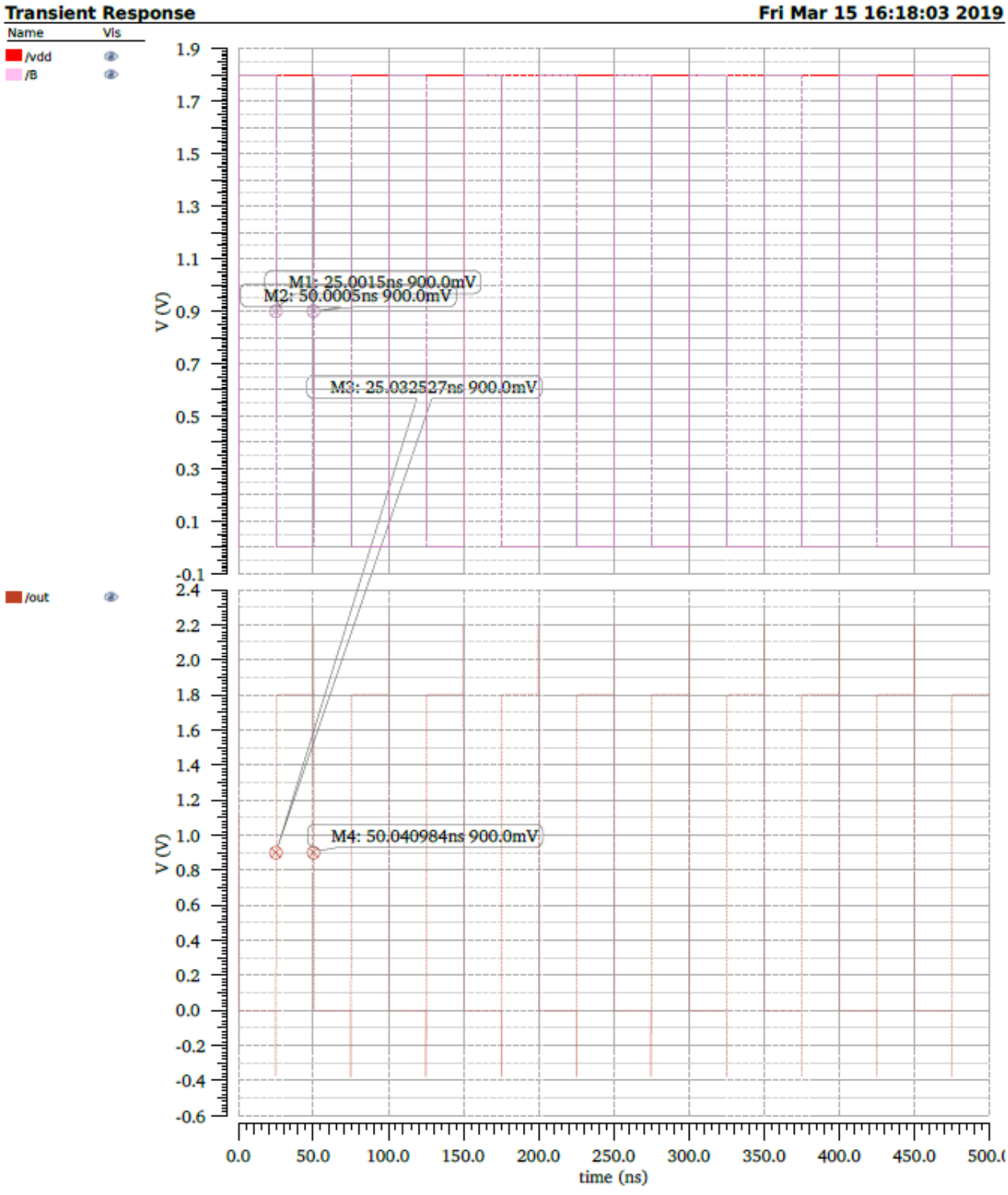
2-Input NAND Symbol



2-Input NAND Testbench

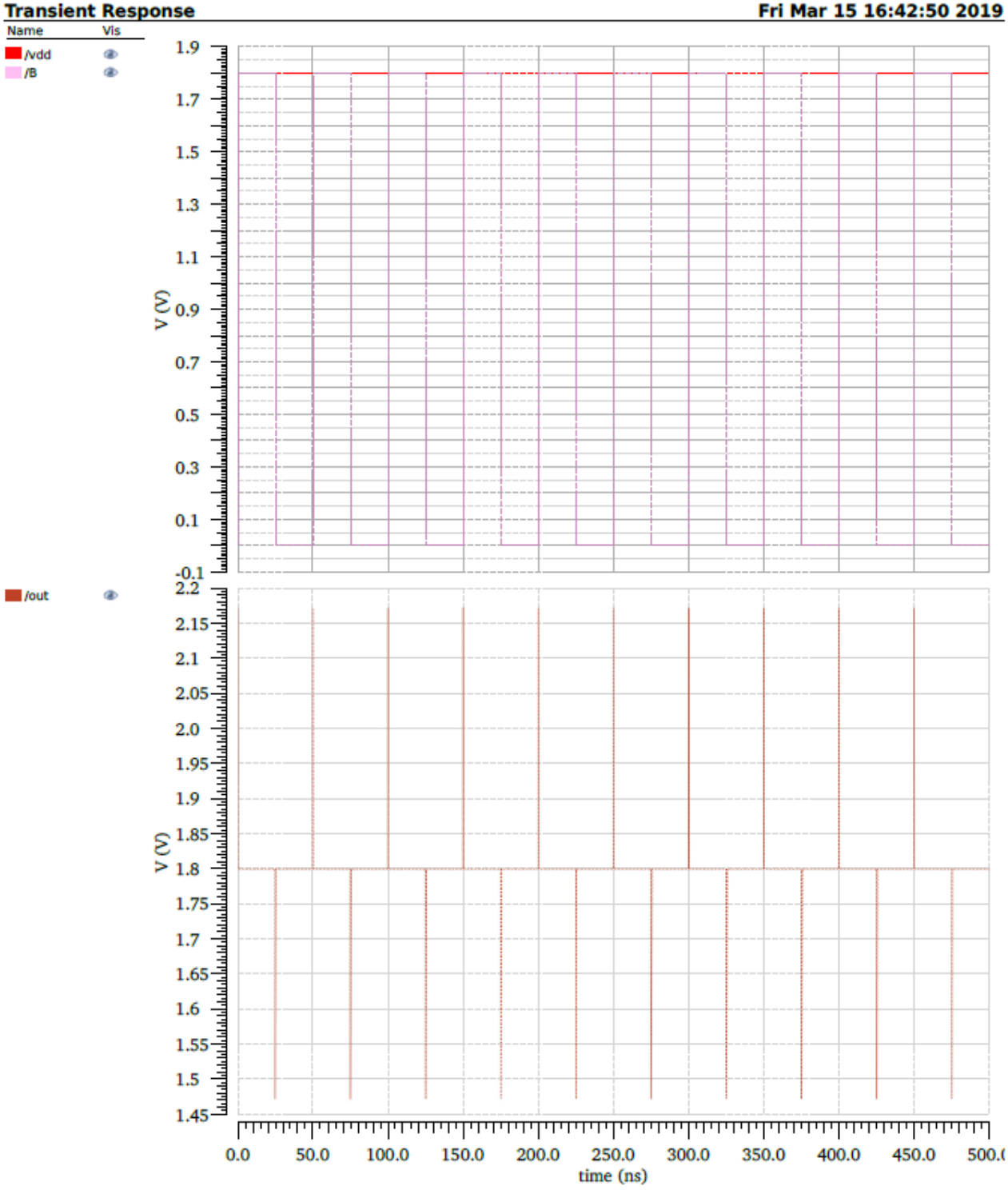


Testbench Waveforms

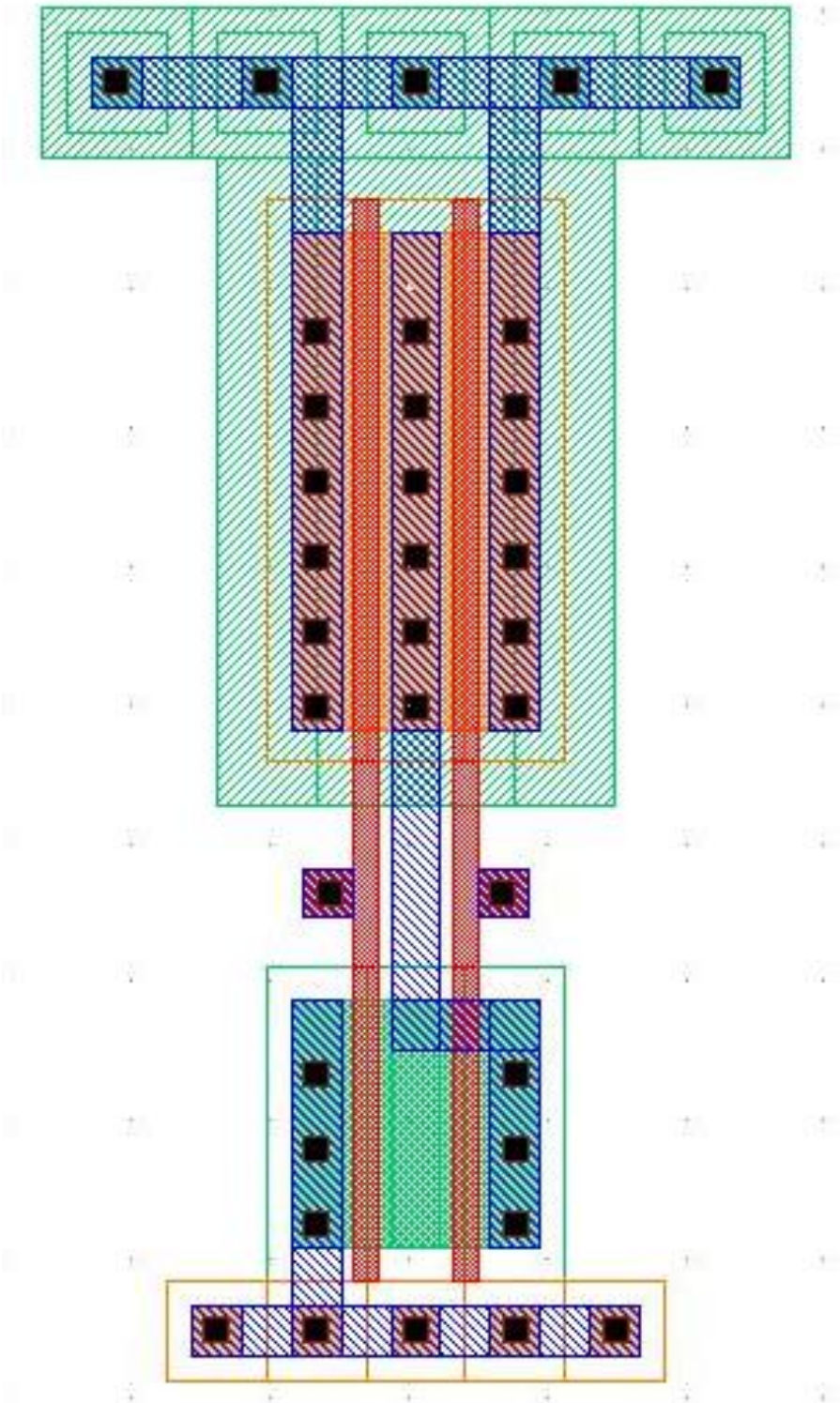


(A second one with the A input tied to ground instead of vdd)

Transient Response **Fri Mar 15 16:42:50 2019**



2-Input NAND Layout

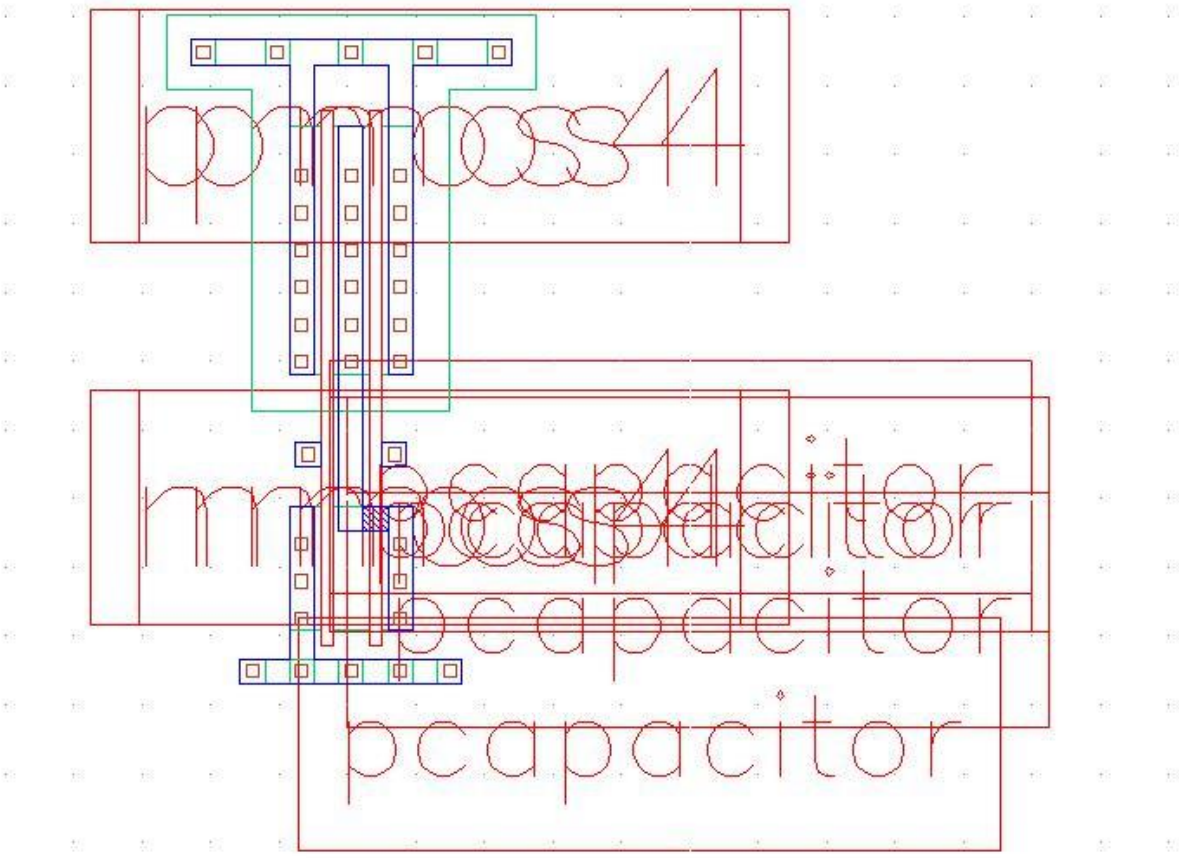


2-Input NAND DRC and LVS

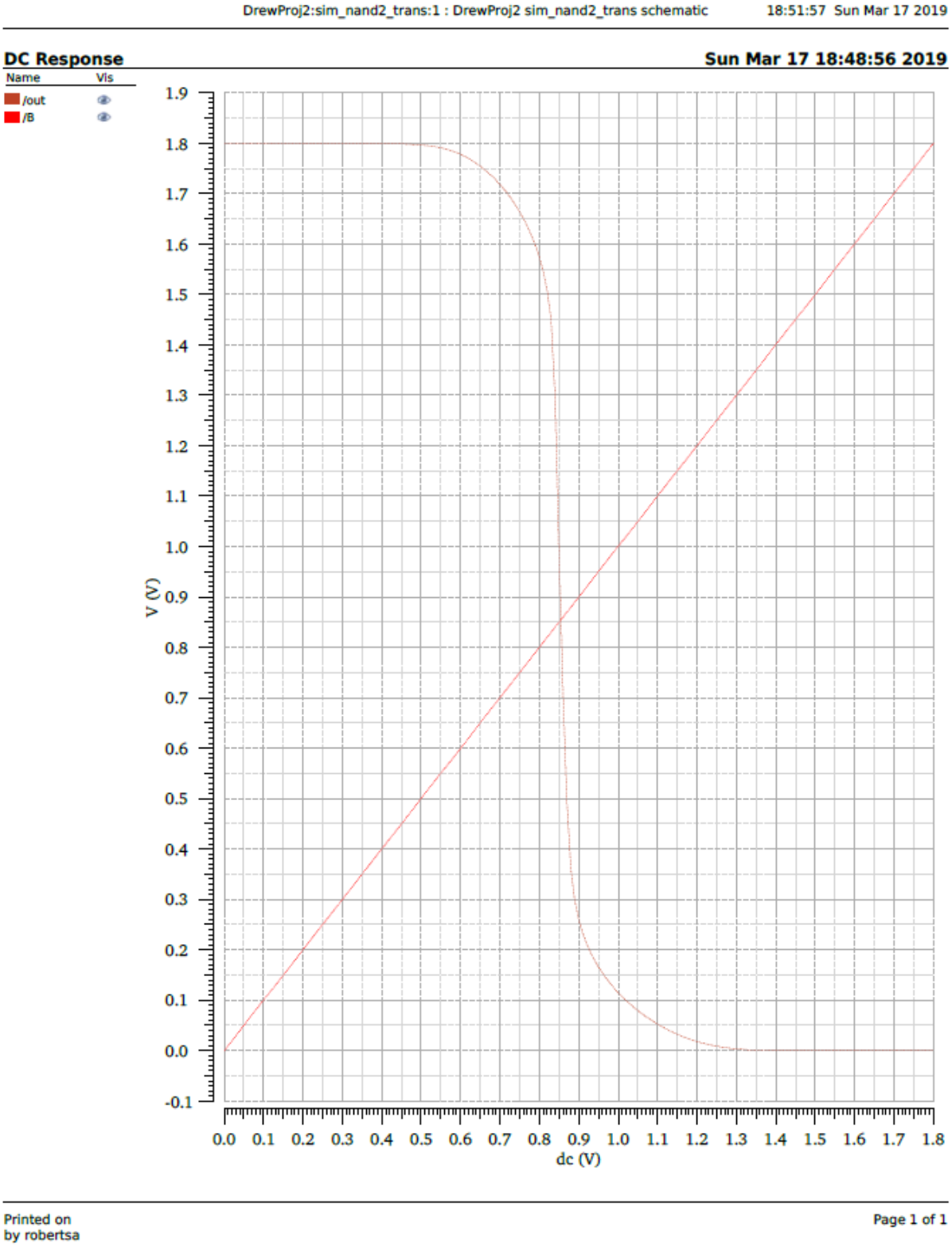
```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Sun Mar 17 19:00:34 2019
    completed ....Sun Mar 17 19:00:34 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "nand2_Layout layout"   *********
   Total errors found: 0
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS
-dir /gaia/class/student/robertsa/cadenceV/LVS -l -s -t
/gaia/class/student/robertsa/cadenceV/LVS/layout
/gaia/class/student/robertsa/cadenceV/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for
/gaia/class/student/robertsa/cadenceV/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for
/gaia/class/student/robertsa/cadenceV/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N4        N1        A
    N3        N5        B
    N5        N4        out
    N1        N2        vdd
    N2        N0        vss

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                               terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from
/gaia/class/student/robertsa/cadenceV/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from
/gaia/class/student/robertsa/cadenceV/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

2-Input NAND Extracted Parasitic Layout



Post Layout Response



Conclusion Table

Description	Rise Time	Fall Time	Delay
2 input NAND	.031027ns	.040484ns	.0357555