CPE 151/EEE 234
Digital IC Design

Project No. 1

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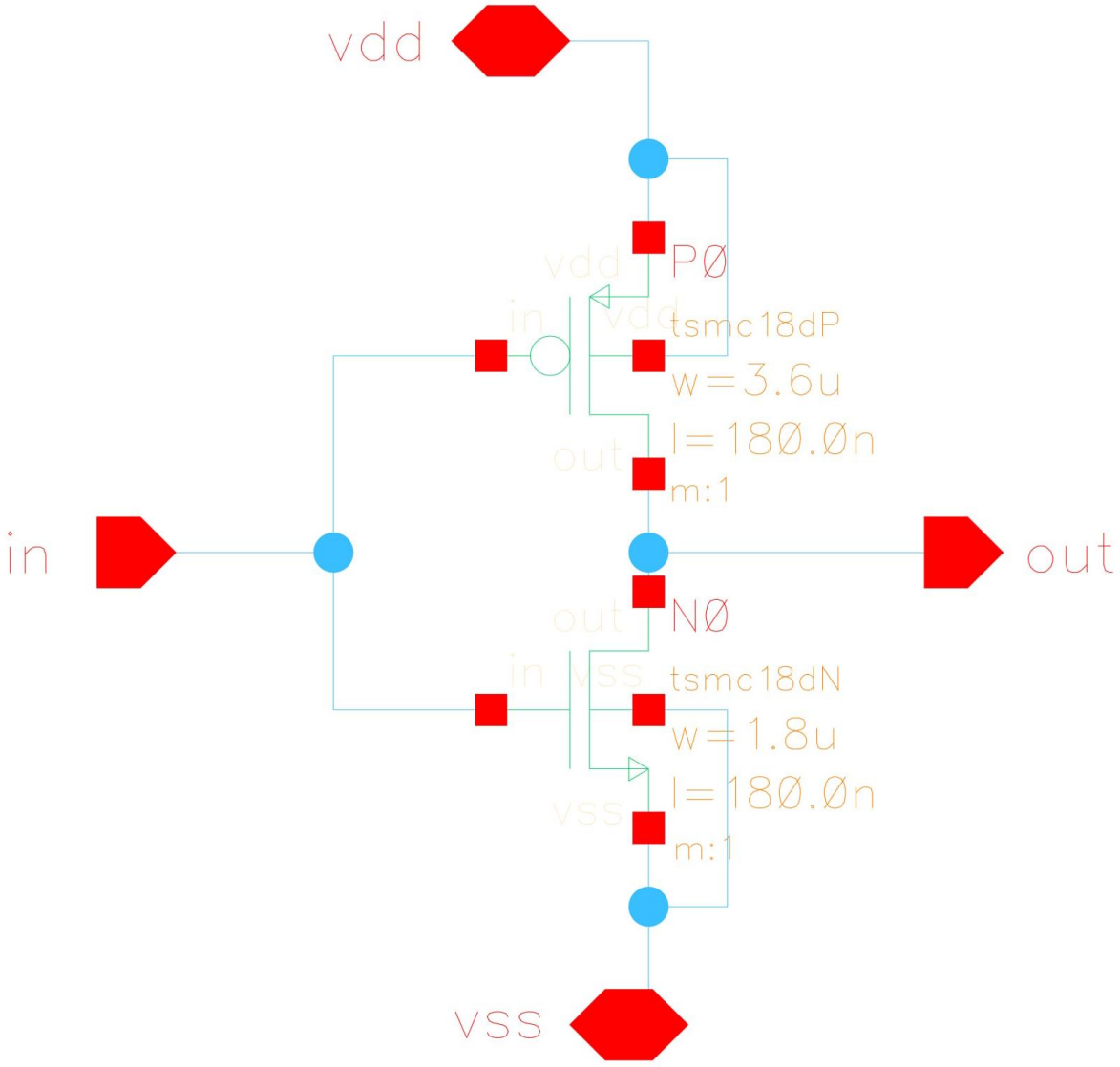
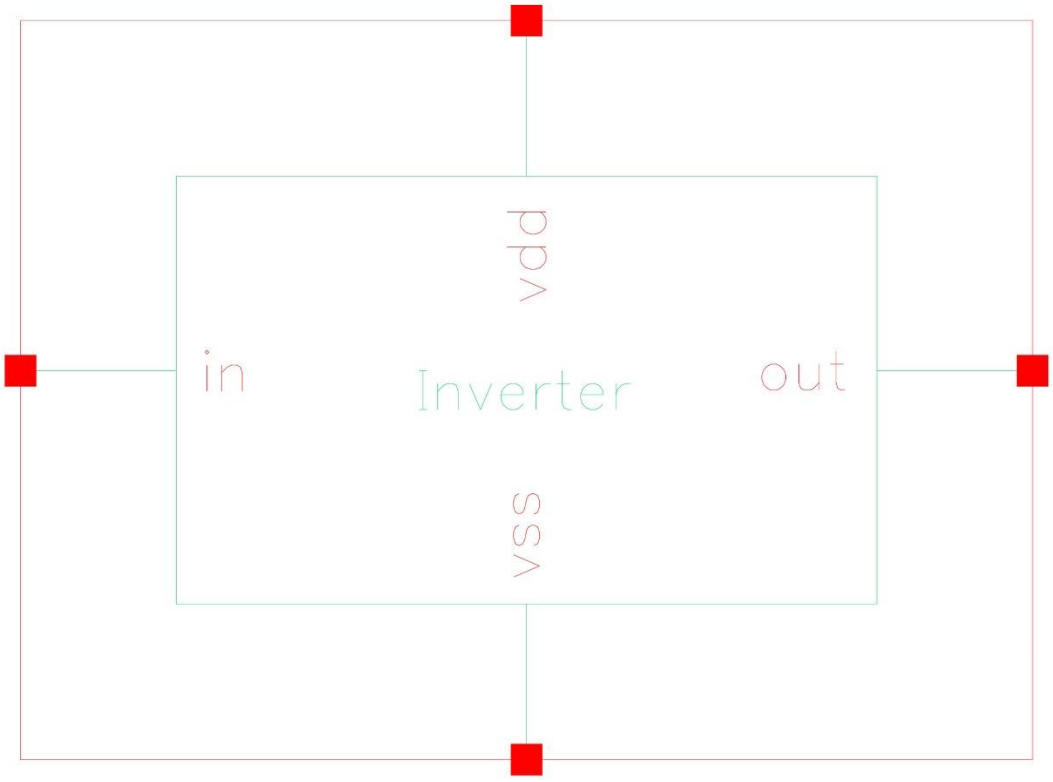
Contents

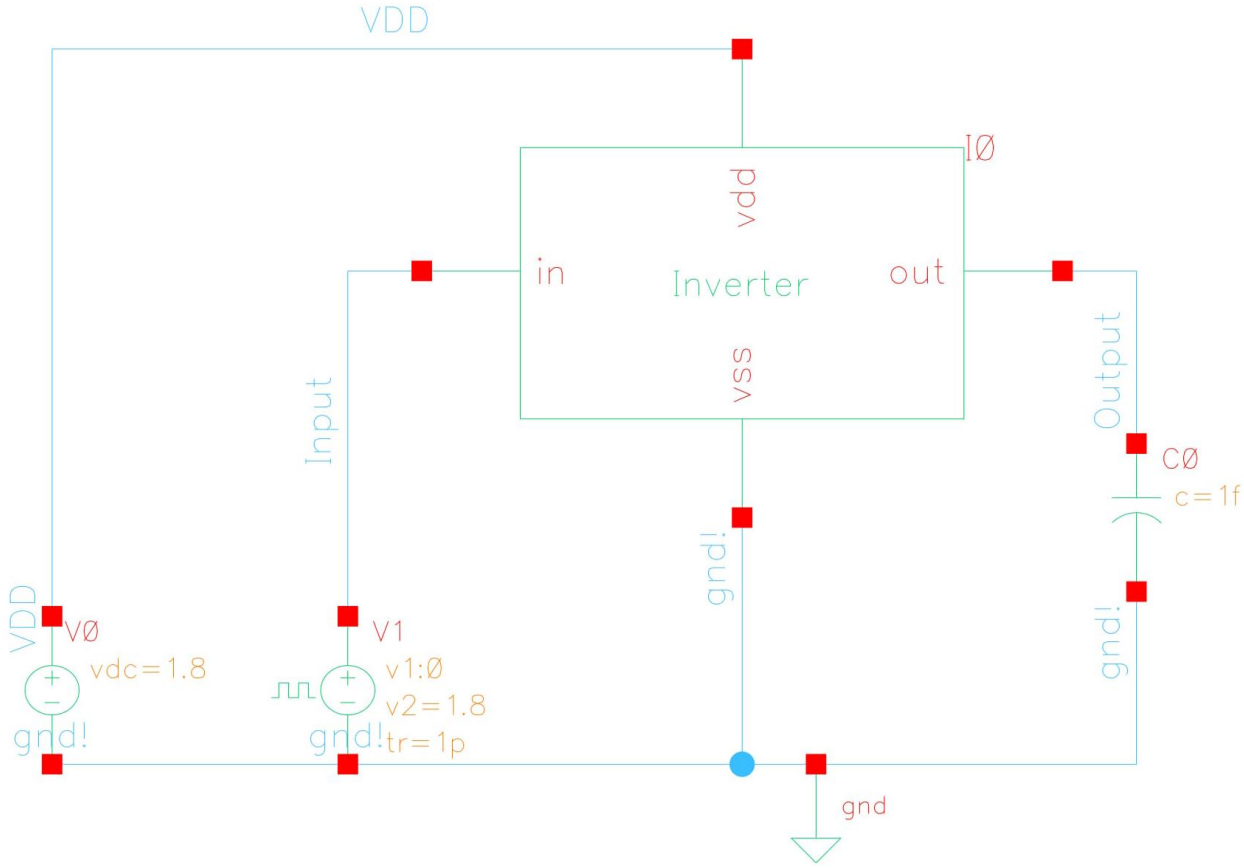
Inverter Schematic



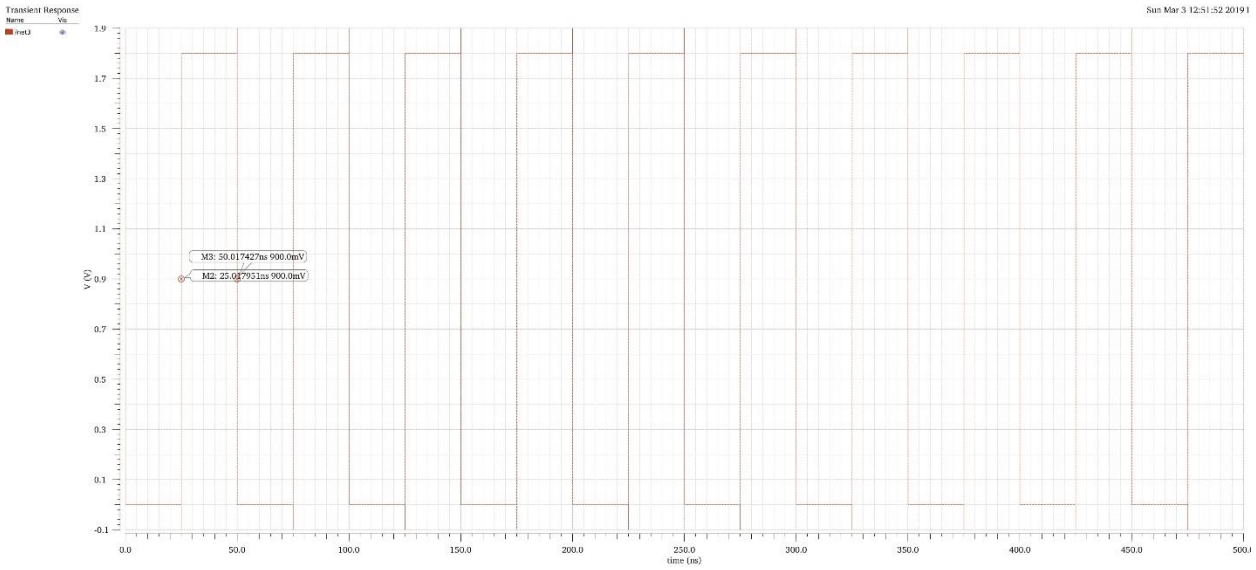
Inverter Symbol

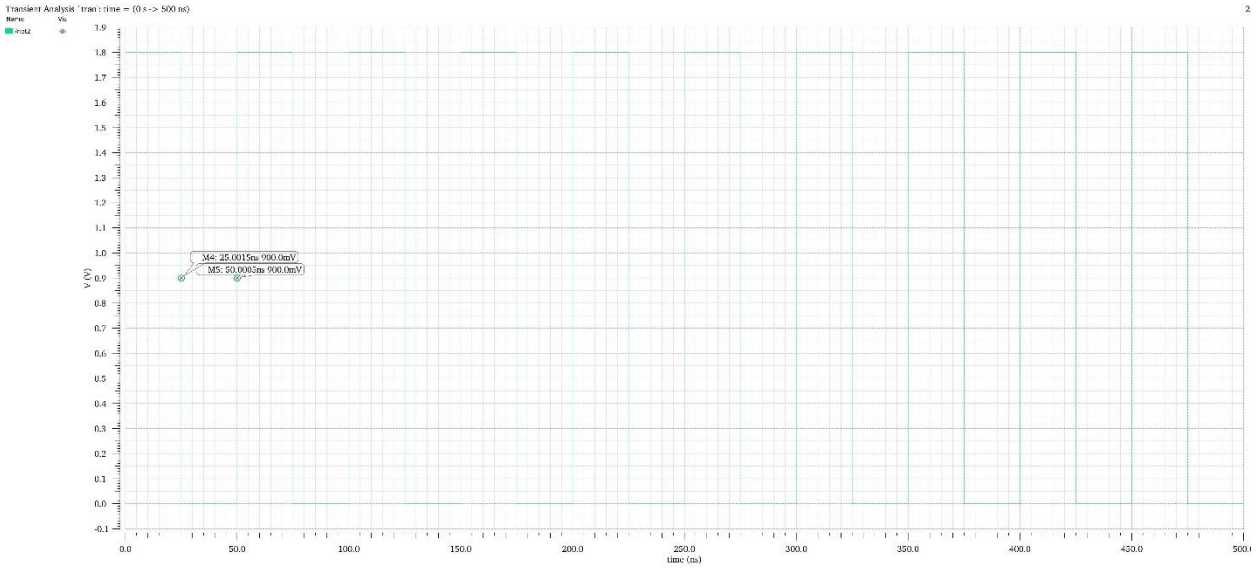


Inverter Testbench

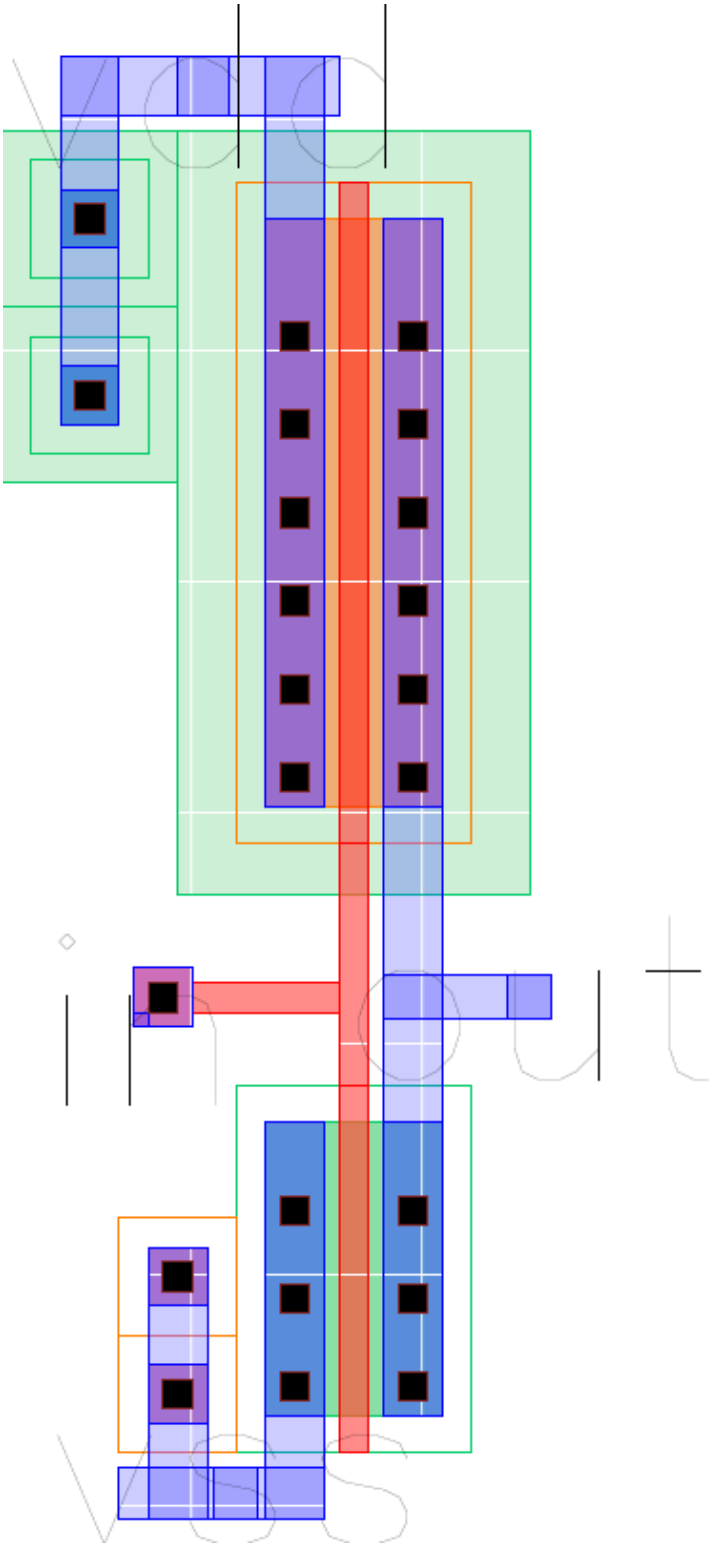


TestBench waveforms





Inverter layout

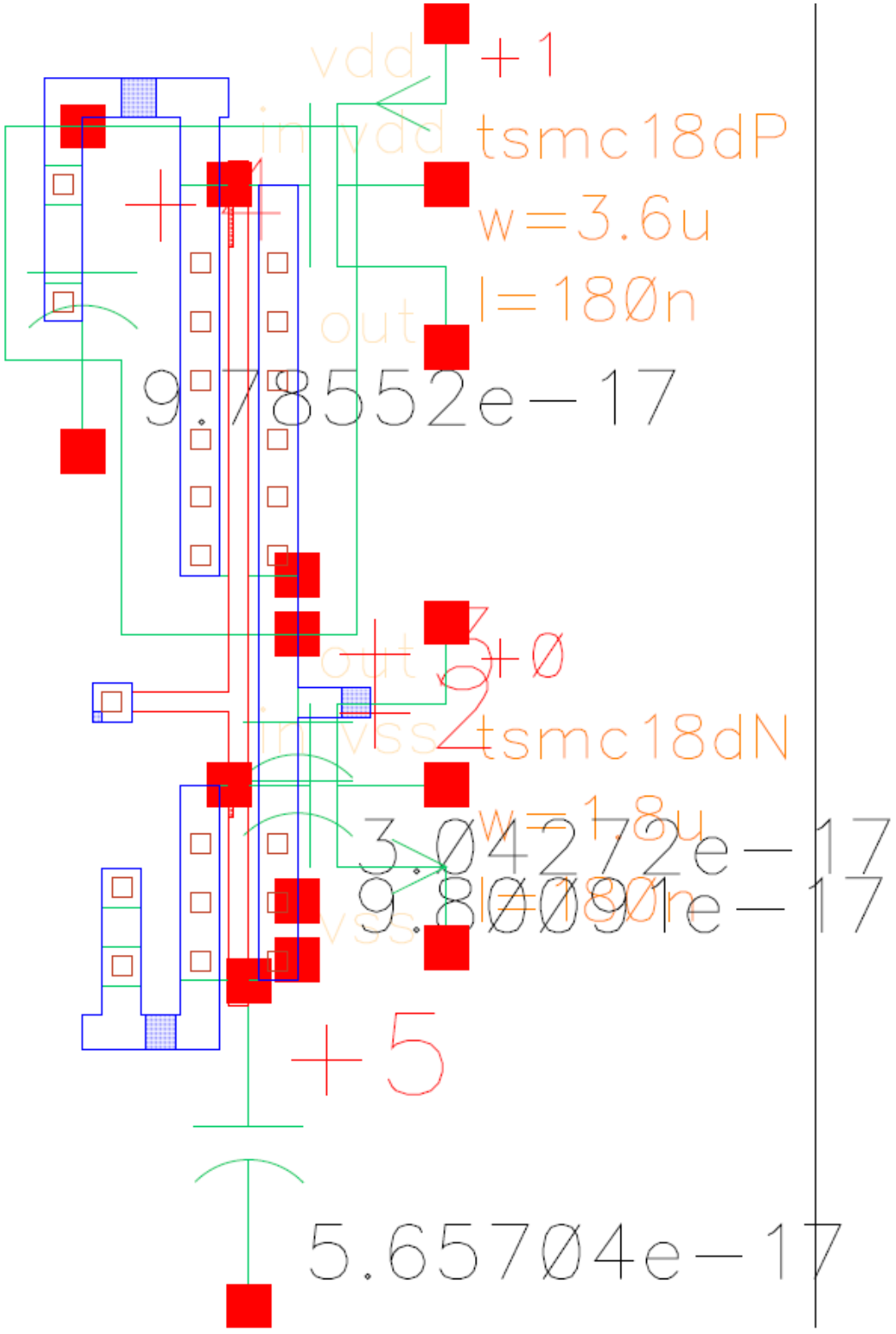


Inverter DRC and LVS

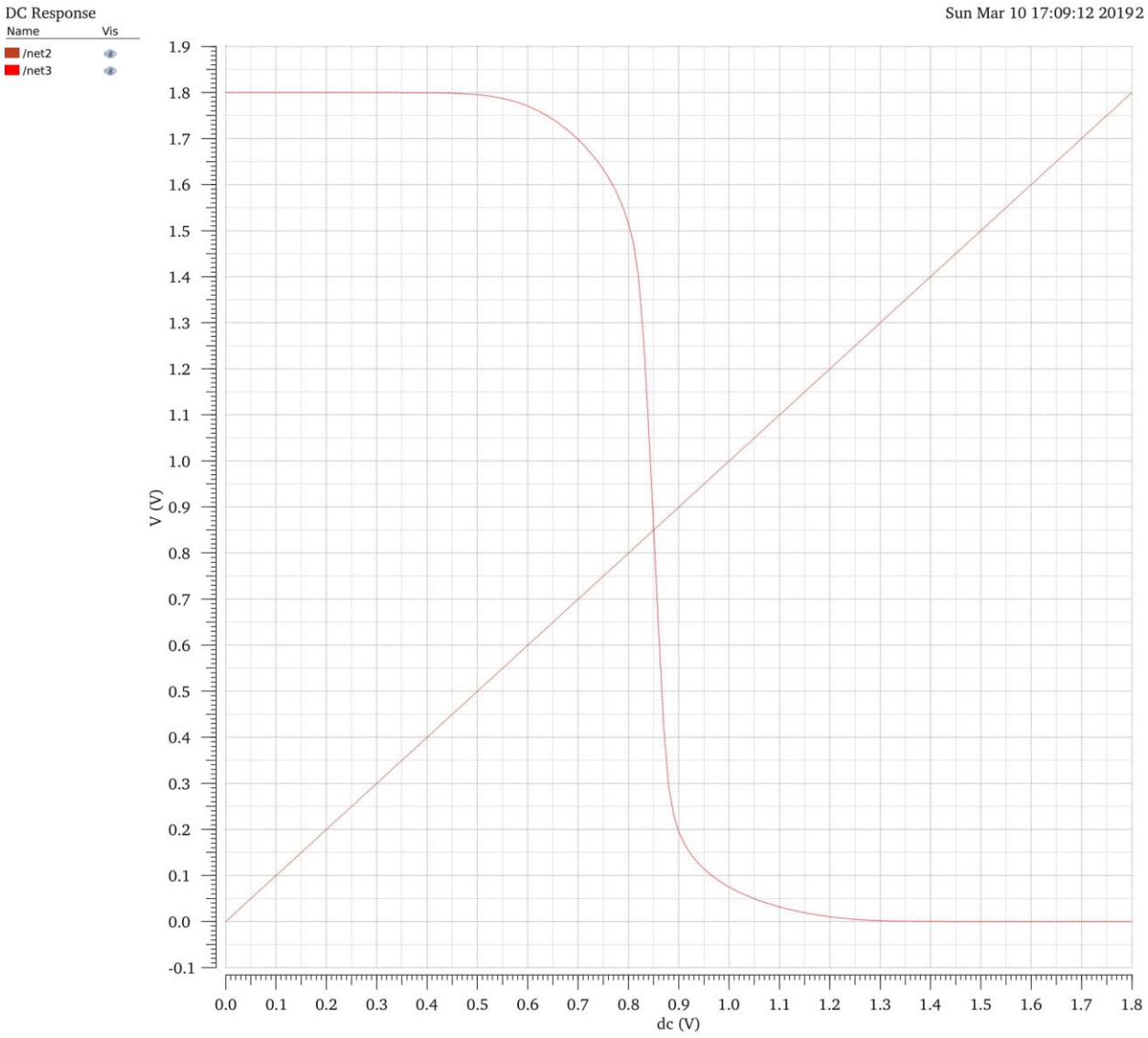
```
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Sun Mar 10 17:33:14 2019
    completed ....Sun Mar 10 17:33:14 2019
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell
"Inverter_Layout2 layout"   *********
   Total errors found: 0
```

```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line:
/software/cadence/installs/IC617/tools.lnx86/dfII/bin/64bit/LVS
-dir /gaia/class/student/robertsa/cadenceV/LVS -l -s -t
/gaia/class/student/robertsa/cadenceV/LVS/layout
/gaia/class/student/robertsa/cadenceV/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for
/gaia/class/student/robertsa/cadenceV/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for
/gaia/class/student/robertsa/cadenceV/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N3        N0        in
    N2        N3        out
    N0        N2        vdd
    N1        N1        vss

Devices in the netlist but not in the rules:
        pmos nmos

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 4       4
        total                  4       4

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  4       4


Probe files from
/gaia/class/student/robertsa/cadenceV/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from
/gaia/class/student/robertsa/cadenceV/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Inverter Extracted Parasitic Layout



Post Layout Response



Conclusion Table

Description	Rise Time	Fall Time	Delay
Inverter	.016451ns	.016927ns	.016689ns