# EEE 108L MICRO-ELECTRONICS 1 LAB 4

**Lab Session: Tuesday 3PM - 5:40PM**

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# PRE-LAB CALCULATIONS

STEP 1.

$$Gain = \frac{R2}{R1} + 1$$

The spec to meet this time is a gain between 30V/V and 45V/V inclusive. Selecting R2 as 36K Ohms and R1 as 1K ohms yields a gain of 37K ohms

(Please see figure 1 in appendix A for complete calculations, also note R2 as 37K ohms is an error. The correct value is used immediately below the boxed value in figure 1)

STEP 2.

$$(R1 = Xc) => (1K = \frac{1}{2\pi FC}) => (F = 15.915Hz)$$

(Please see figure 1 in appendix A for complete calculations)

STEP 3.

Vout should be 5V under these circumstances. Deduced entirely from ideal op amp assumptions.

(Please see figure 1 in appendix A for complete calculations)

STEP 4.

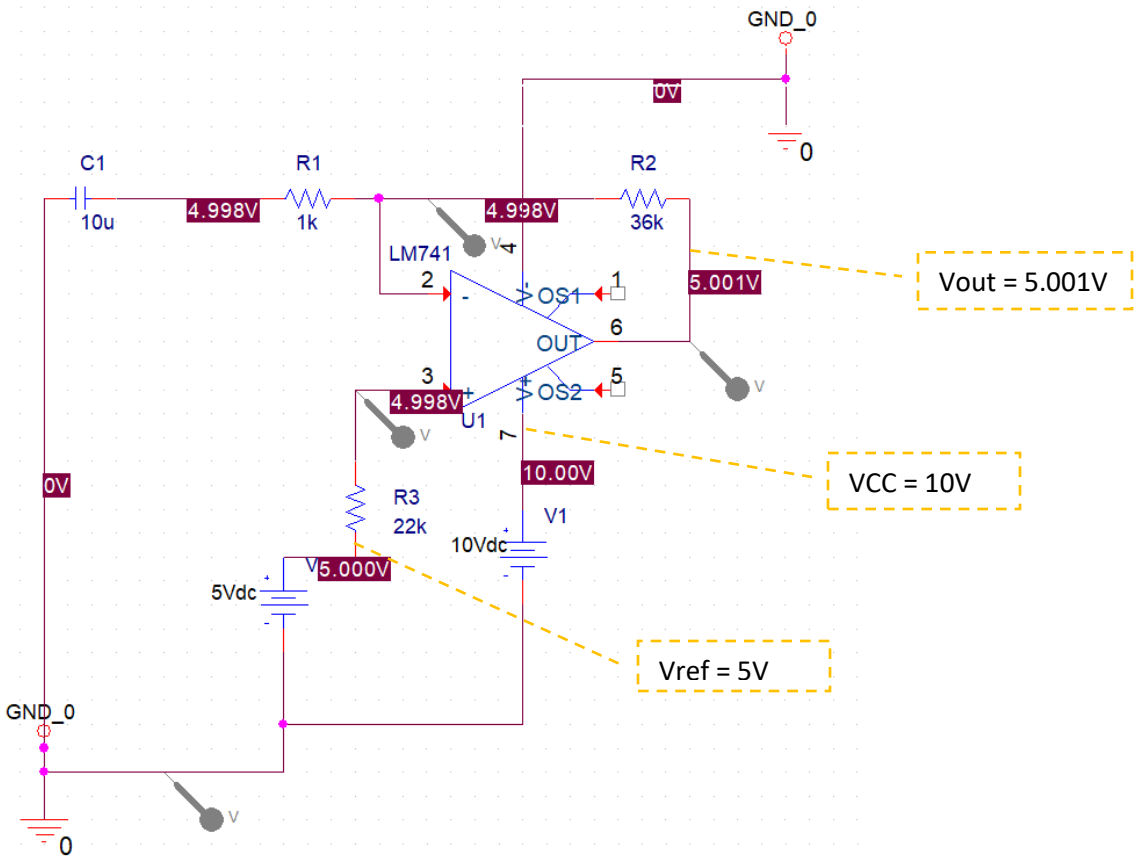
Lowest: 22K Ohms

Highest: 32K Ohms

(Please see figure 1 in appendix A for complete calculations)

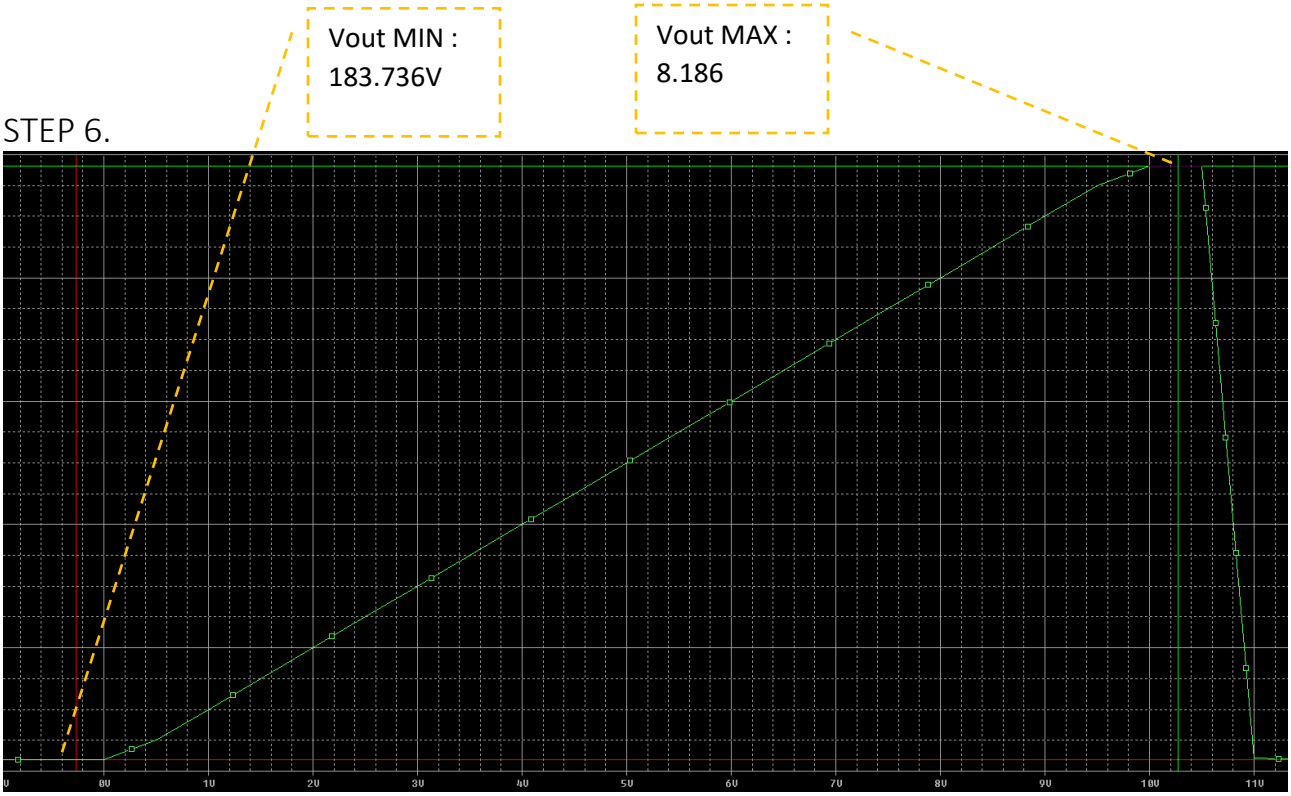
# SPICE SIMULATION

STEP 5.



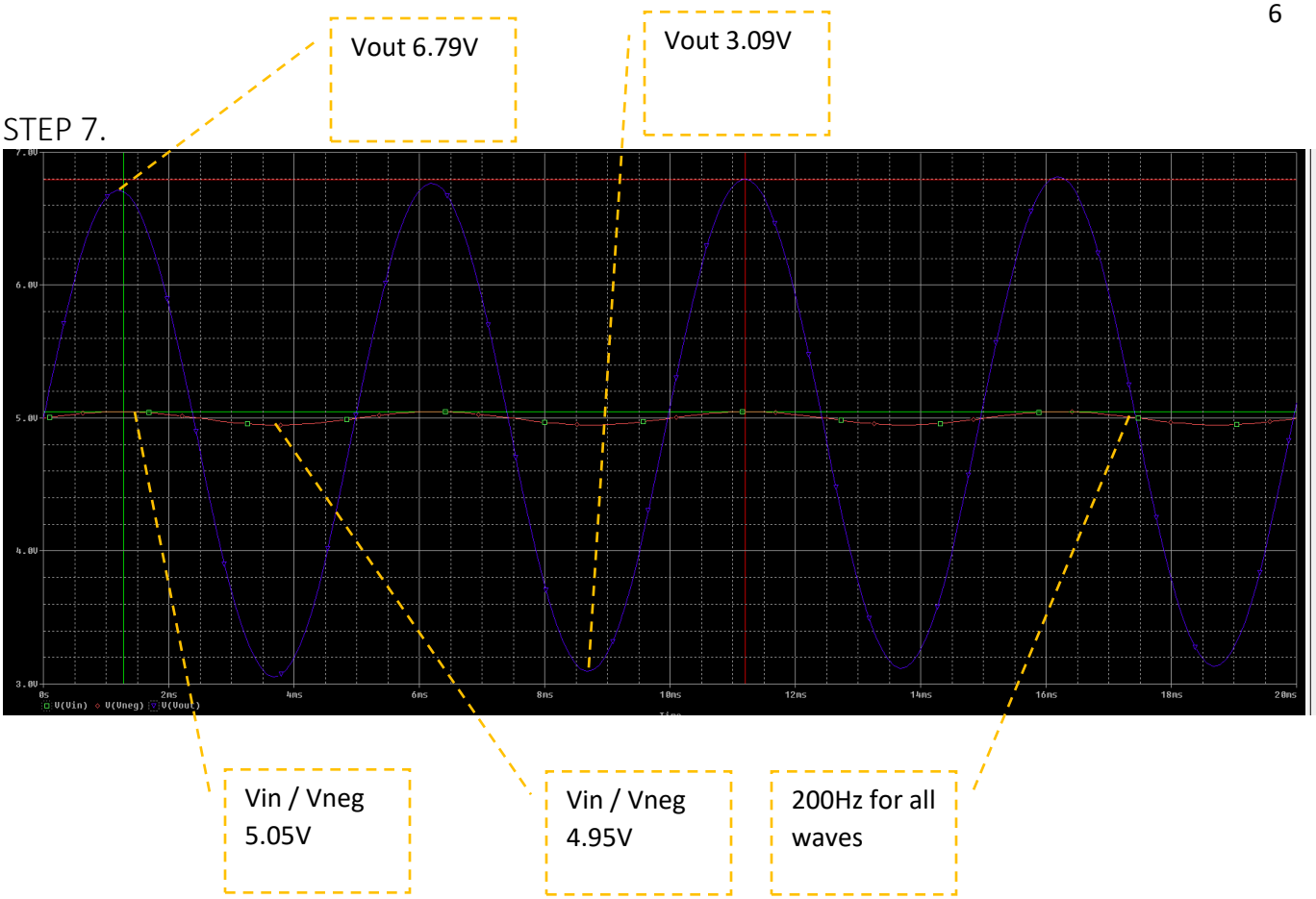

The SPICE simulation results do indeed match up with my theoretical calculations. This is still strange to look at but makes a lot more sense once realizing the C1 R1 branch is basically null and void from the lone DC signal.

STEP 6.




In the lab instructions we are told to sweep from 0V to 10V however it was very difficult to see what was happening that way. We decided to extend the sweep 2V in each direction and this is the result. We were able to clearly see the outputs simulated minimum and maximum values.

STEP 7.




The pole frequency for C2 as calculated came to 723.43mHz, this is much smaller than the pole calculated for C1 so that is the frequency that was chosen as a baseline. 10 times the C1 pole frequency of 15.915Hz is 159.15Hz. To be safe, we used a frequency of 200Hz for the AC signal at Vin.

(Refer to figure 2 for the complete calculation)

STEP 8.

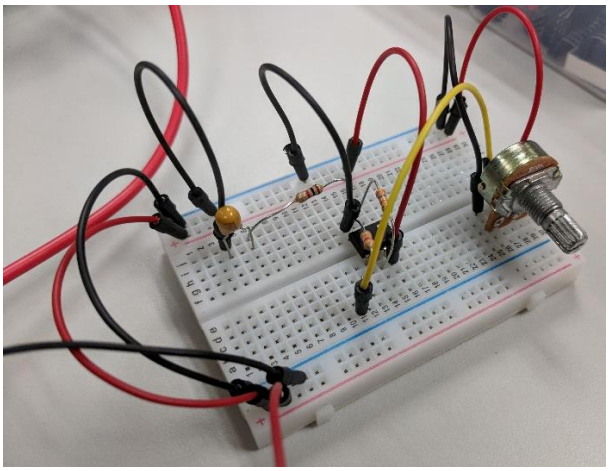


Figure 1 as constructed. Actual resistor values as follows:

R1 = 985 Ohms, R2 = 34.1K Ohms, RB = 21.4K Ohms

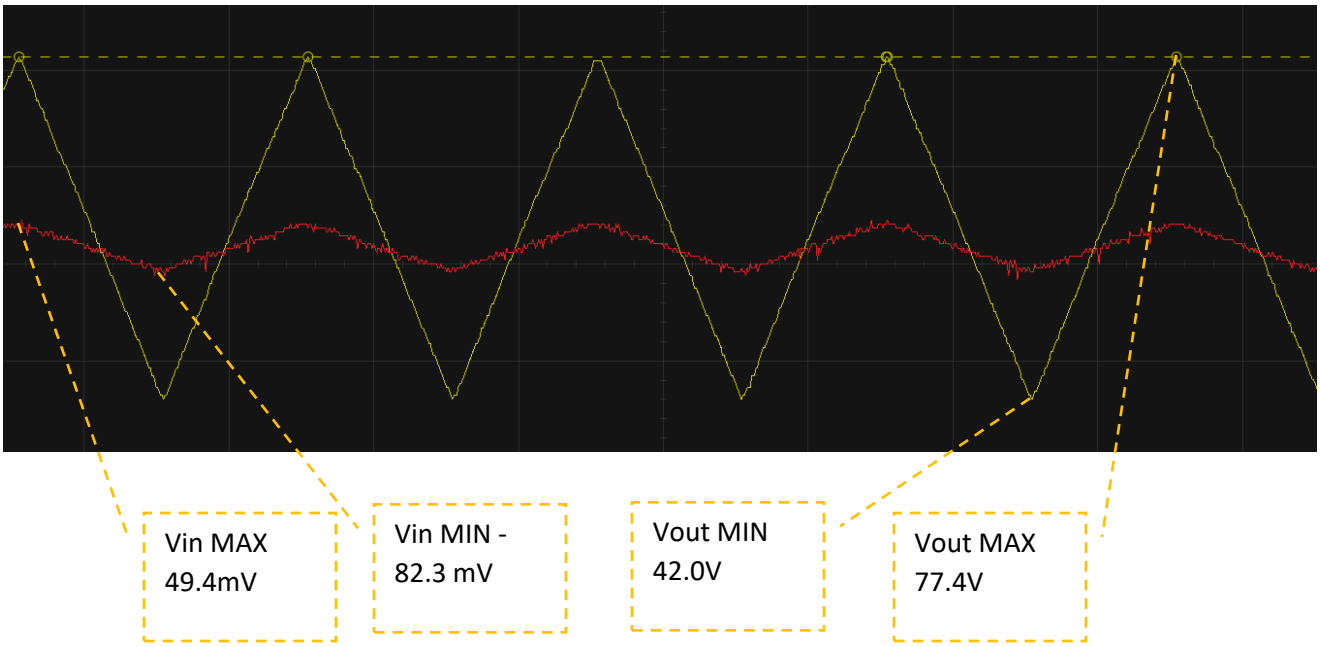
# EXPERIMENT

STEP 9.

| Vref | Vin | Vout |
|---|---|---|
| 1.6mV | 1.65mV | 1.94V |
| 833mV | 831mV | 1.94V |
| 2.09V | 2.09V | 2.09V |
| 4.89V | 4.89V | 4.90V |
| 9.37V | 9.35V | 9.37V |
| 9.999V | 9.913V | 9.42V |

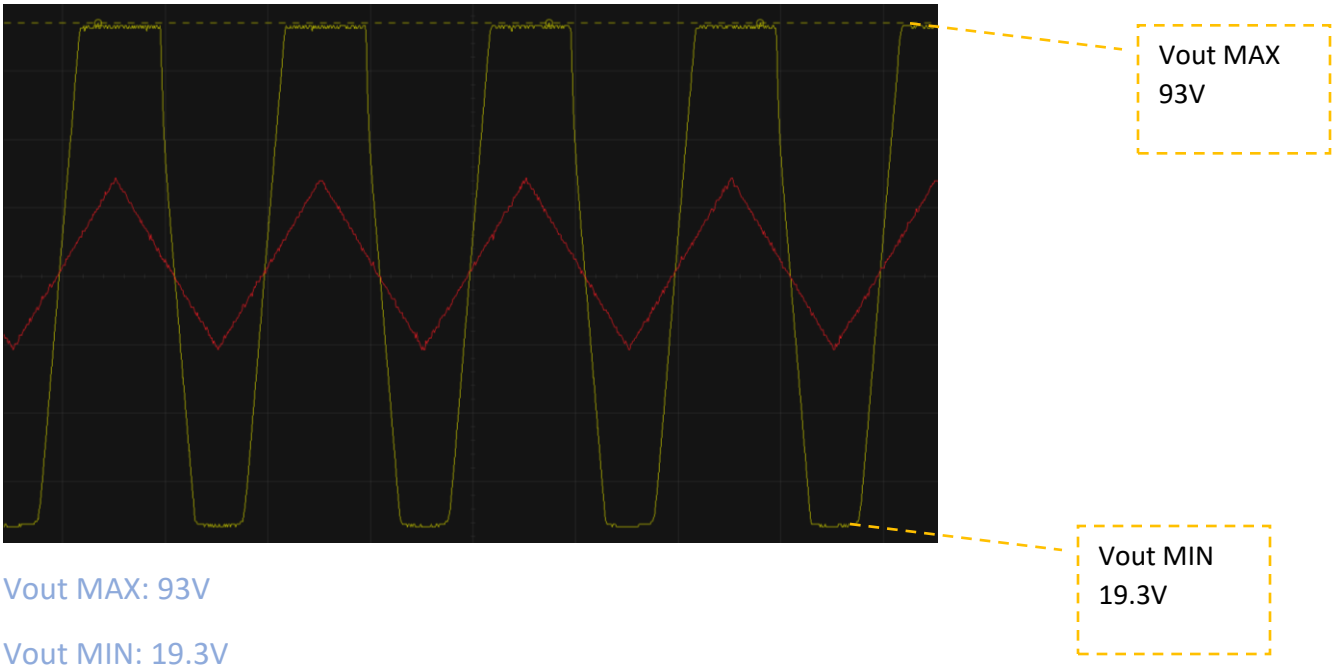
The minimum value for Vout is 1.94V and the maximum is 9.42V. It appears that Vin is roughly equal to Vref at all values V until passing the maximum for Vout. As a range this would be 0V – 9.42V

STEP 10.




As previously calculated, the frequency to operate at for both capacitors to appear to be shorts is about 160Hz. The outputs peak here was 77.4V and the valley was 42.0V. 77.4-42 = 35.4P-P. 35.4/2 = 17.7 Amplitude. DC offset is 17.7 + 42 = 59.7V

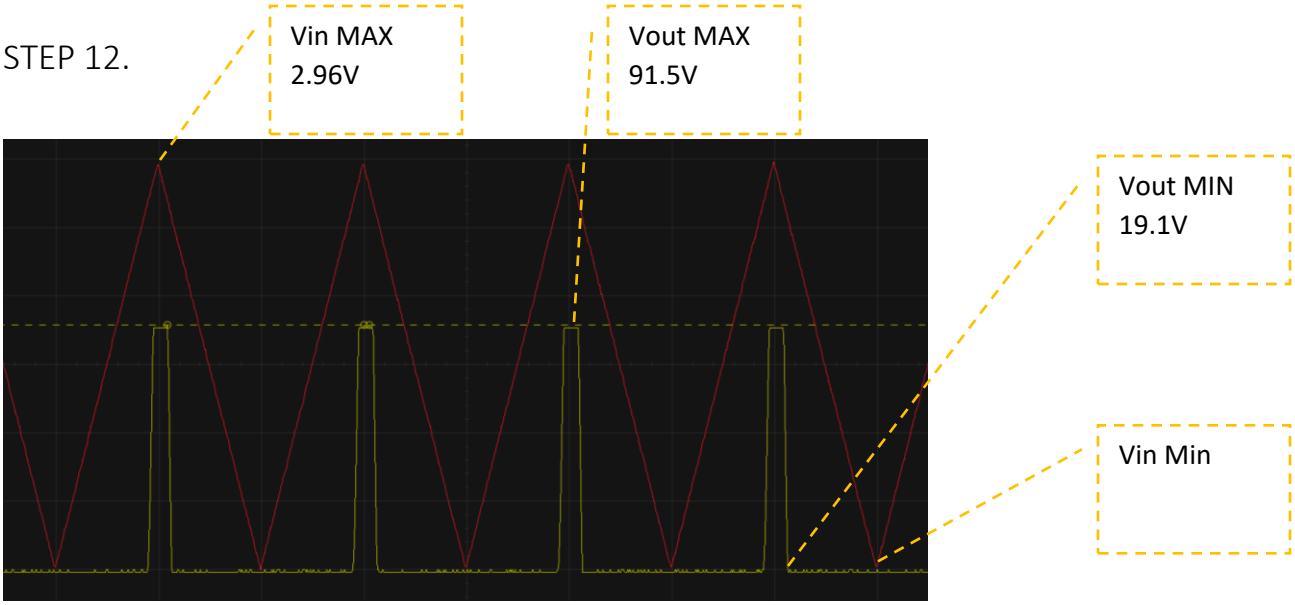
STEP 11.




Vout MAX: 93V

Vout MIN: 19.3V

STEP 12.




I suspect we interpreted the instructions incorrectly for this step. We calculated the value needed for Vout to be 6V offset and applied it to Vref but must have thought to statement about clipping was for the input. Our output here is clearly clipping and clipping heavily at that.

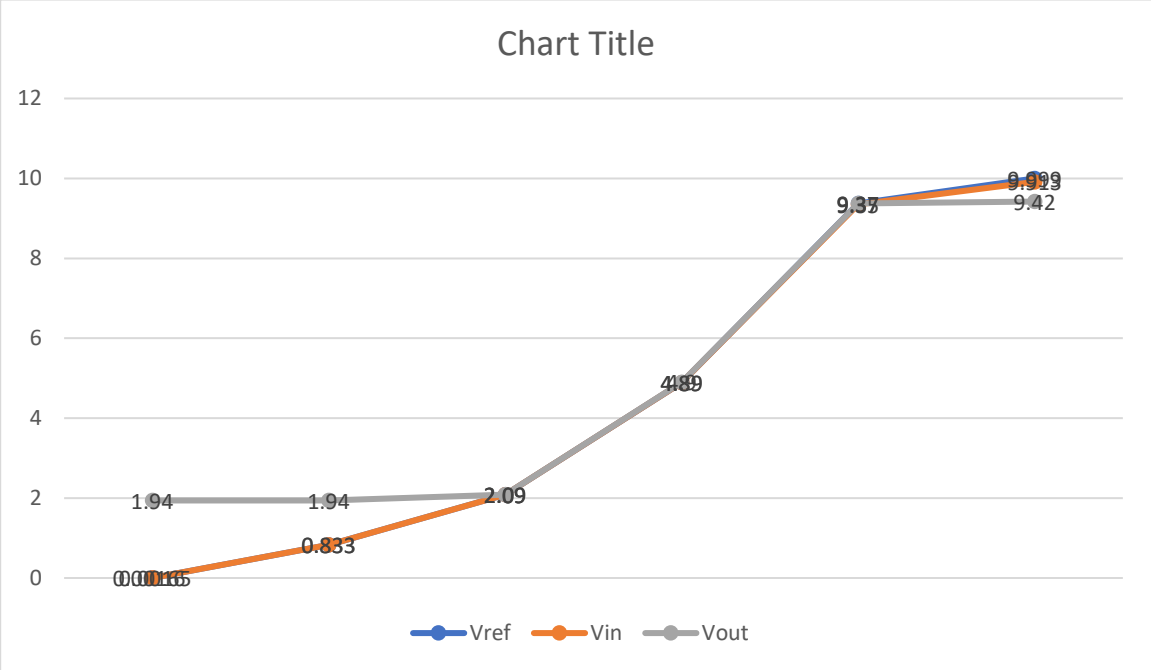
STEP 13.


Our Vout signal disappeared as soon as we attempted to bias for 5V DC offset. Re-building the circuit did nothing. Initially we received what looked to be a flat DC response but it only lasted a short period of time.

# CONCLUSIONS

**Item 1.**

From the data table in Step 9, make a graph with VIN on the horizontal axis and VOUT on the vertical axis. Indicate actual data points on the graph. Put the graph on a separate sheet of paper or use a computer-based graphing program (label the graph "Item 1"). On the graph, indicate the upper and lower output clipping levels.




**Item 2.**

Re-state your data from Step 10 regarding the DC bias voltage at the input and the DC bias voltage at the output. What is their relationship? Why?

Vref was supposed 6V DC, and were seeing 59.7V as the offset for Vout. That amounts to a ratio of 1 : 9.95. This is strange to me as I would have assumed the DC offset at the input would be multiplied by the gain to get the DC offset at the output but this is not consistent.

**Item 3.**

Show calculations (From the measured part values) for fp1 and fp2 for the circuit of Step 10.

(Figure 1 in Appendix A shows the calculation for Fp1, and Figure 2 shows the calculation for Fp2)

**Item 4.**

The bias condition found in Step 12 is called maximum symmetrical clipping. Explain this term and why the clipping is called symmetrical.

Maximum symmetrical swing occurs when the bias point is half of VCC, this allows the greatest amplitude swing in Vout if the input signal is not too large to cause clipping. If the input is too great, then the output will still be symmetrical about the VCC half way point but will clip on both sides.

**Item 5.**

In Step 13 were you able to bias the output voltage at +5 V? Check a data sheet to see if the value of VREF required to make VOUT = +5 V falls within the input common-mode voltage range of the operational amplifier used in this experiment (the LM741CN).

(Courtesy of http://www.ti.com/lit/ds/symlink/lm741.pdf )

**6.7 Electrical Characteristics, LM741C(1)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Input offset voltage | | $R_S \le 10\ k\Omega$ | $T_A = 25°C$ | | 2 | 6 | mV |
| | | | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | 7.5 | mV |
| Input offset voltage adjustment range | | $T_A = 25°C$, $V_S = \pm 20\ V$ | | | ±15 | | mV |
| Input offset current | | $T_A = 25°C$ | | | 20 | 200 | nA |
| | | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | | 300 | |
| Input bias current | | $T_A = 25°C$ | | | 80 | 500 | nA |
| | | $T_{AMIN} \le T_A \le T_{AMAX}$ | | | | 0.8 | µA |
| Input resistance | | $T_A = 25°C$, $V_S = \pm 20\ V$ | | 0.3 | 2 | | MΩ |
| Input voltage range | | $T_A = 25°C$ | | ±12 | ±13 | | V |
| Large signal voltage gain | | $V_S = \pm 15\ V$, $V_O = \pm 10\ V$, $R_L \ge 2\ k\Omega$ | $T_A = 25°C$ | 20 | 200 | | V/mV |
| | | | $T_{AMIN} \le T_A \le T_{AMAX}$ | 15 | | | |
| Output voltage swing | | $V_S = \pm 15\ V$ | $R_L \ge 10\ k\Omega$ | ±12 | ±14 | | V |
| | | | $R_L \ge 2\ k\Omega$ | ±10 | ±13 | | |
| Output short circuit current | | $T_A = 25°C$ | | | 25 | | mA |
| Common-mode rejection ratio | | $R_S \le 10\ k\Omega$, $V_{CM} = \pm 12\ V$, $T_{AMIN} \le T_A \le T_{AMAX}$ | | 70 | 90 | | dB |
| Supply voltage rejection ratio | | $V_S = \pm 20\ V$ to $V_S = \pm 5\ V$, $R_S \le 10\ \Omega$, $T_{AMIN} \le T_A \le T_{AMAX}$ | | 77 | 96 | | dB |
| Transient response | Rise time | $T_A = 25°C$, Unity Gain | | | 0.3 | | µs |
| | Overshoot | | | | 5% | | |
| Slew rate | | $T_A = 25°C$, Unity Gain | | | 0.5 | | V/µs |
| Supply current | | $T_A = 25°C$ | | | 1.7 | 2.8 | mA |
| Power consumption | | $V_S = \pm 15\ V$, $T_A = 25°C$ | | | 50 | 85 | mW |

(1) Unless otherwise specified, these specifications apply for $V_S = \pm 15\ V$, $-55°C \le T_A \le +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \le T_A \le +70°C$.

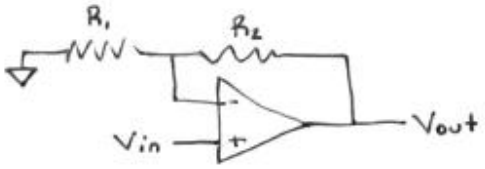
We needed a DC offset of about 140mV to have a 6V DC offset at V out. We were unable to achieve this. Looking at this spec sheet it appears to be within range, I am now puzzled even more by why our output disappeared.

# APPENDIX A

Figure 1.

## Lab 4 Pre-Lab

1) Under the short assumption for C, cleared op circuit:




10k pot in kit

Non-inverting amp gain = $1 + \frac{R_2}{R_1}$

if we choose $R_2 = 37k$ & $R_1 = 1k$

gain = $1 + \frac{36k}{1k} = 36 + 1 = 37 \frac{V}{V}$

± 10% vals: $gain_+ = 1 + 44 = 45 \frac{V}{V}$ $gain_- = 1 + 29.\overline{45} = 30.\overline{45}$

2) $R_1 = 1k$, $X_c = \frac{1}{\omega C} = \frac{1}{2\pi f C}$

$1k = \frac{1}{2\pi f \cdot 10\mu} \Rightarrow \left[1000(2\pi \cdot 10\mu)\right]^{-1} = f$

$f = 15.915\ Hz$

4) Wiper centered: $R_P + R_B = 10k + 22k = 32k$

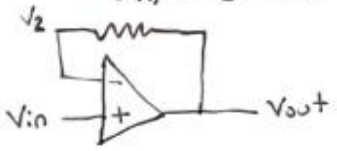
Wiper nearly full left: $\approx R_B = 22k$

3) Capacitors block DC current $i = C \cdot \frac{dV}{dt}$, $\left(\frac{dV}{dt} = 0\right)$

$i = C \cdot 0$, $i = 0$

$R_1$ is in series with C so $i_{R_1} = i_C = 0$

New circuit




@ $R_B$, $i = 0$, so $V_{REF} = V_{in}$, $V_{in} = 5V$. If $V_{in} = 5V$ then $V_2 = 5V$. $i$ @ $R_2 = 0$ now so $V_{out} = V_2$

$V_{out} = 5V$

Figure 2.

Step 7)

$$f_{p2} = \frac{1}{2\pi C_{in} R_B}$$

$$723.43\,mHz = \frac{1}{2\pi \cdot 10\mu \cdot 22K}$$

the greater is $f_{p_1} = 15.915\,Hz$

$10 \cdot f_{p_1} = 159.15\,Hz$

Step 8)

$R_1 \cong 985\Omega$
$R_2 \cong 34.1K\Omega$
$R_B \cong 21.4K\Omega$

$A_v = 35.619$

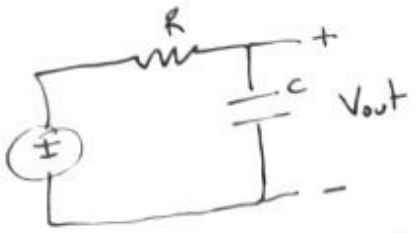
for $35.619 \frac{mV}{mV} \cdot X$

$168.448\,mV$

Step 10
$= 6V_{DC}$

Step 9)

| $V_{REF}$ | $V_{in}$ | $V_{out}$ | ($V_{cc} = 10V$) |
|---|---|---|---|
| 4.89V | 4.89V | 4.90 | |
| 9.999V | 9.913V | 9.42V | |
| 1.6mV | 1.65mV | 1.94V | |
| 833mV | 831mV | 1.94V | |
| 2.09V | 2.09V | 2.09V | |
| 9.37V | 9.35V | 9.37V | |




$Z_R = R$

$Z_c = \frac{1}{sC}$

$V_{out} = V_{in}\left(\frac{\frac{1}{sC}}{\frac{1}{sC} + R}\right)$

$A_v = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + sCR}$

$\frac{1}{1 + j\omega CR}$

$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1^2 + (\omega CR)^2}}$

$\sqrt{2} = \sqrt{1^2 + (\omega CR)^2}$

$2 = 1 + (\omega CR)^2$

$1 = (\omega CR)^2$

mag $\frac{1}{\sqrt{1^2 + (\omega CR)^2}}$

$f = \omega = 2\pi f$

step 13
$V_{out\,DC} = 35.619 \cdot X$
$140.374\,mV = X$