# EEE 108L MICRO-ELECTRONICS 1 LAB 5

Lab Session: Tuesday 3PM - 5:40PM

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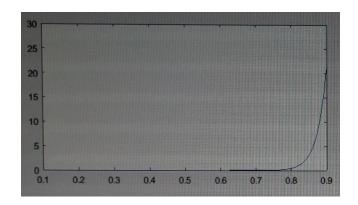
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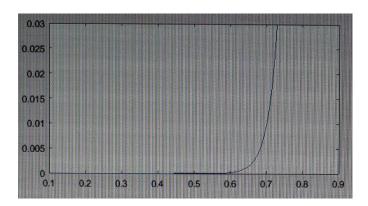
## PRE-LAB CALCULATIONS

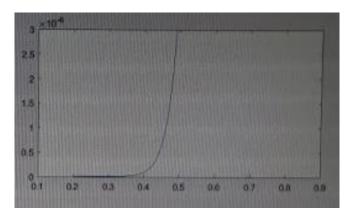
STEP 1.

Doping	Majority Carrier	Minority Carrier
$ND = 1 \times 10^{15} \text{ cm}$ -3	~= ND	Pn ~= 225 x 10^3 cm-3
NA = 1 x 10^17 cm-3	~= NA	Nn ~= 2.25 x 10^3 cm-3

Built in potential of PN diode built from above doping levels: 697.3223 mV







(Please see figure 1 in appendix A for complete calculations)

STEP 2.

$$Vx = \frac{\frac{Vd1 + Vd2}{R} + \frac{Vbias}{Rbias}}{\frac{2}{R} + \frac{1}{Rbias}}$$

$$Id1 = \frac{\frac{Vbias}{Rbias} + \frac{Vd2}{R} - Vd1(\frac{1}{R} - \frac{1}{Rbias} - \frac{2}{R})}{2 + \frac{R}{Rbias}}$$

$$Id2 = \frac{\frac{Vbias}{Rbias} + \frac{Vd1}{R} - Vd2(\frac{1}{R} - \frac{1}{Rbias} - \frac{2}{R})}{2 + \frac{R}{Rbias}}$$

(Please see figure 2 in appendix A for complete calculations)

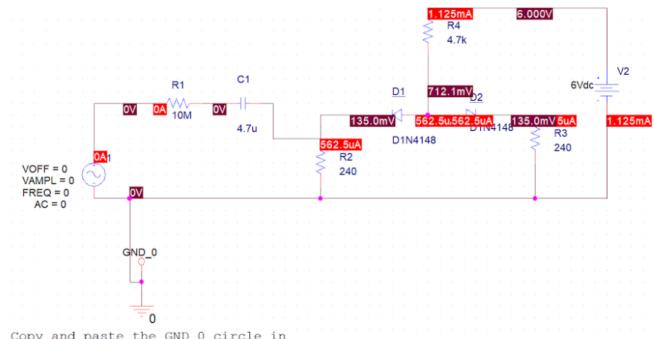
STEP 3.

$$\frac{Vout}{Vin} = \frac{1}{1 + \frac{Rd1 + Rd2}{R}} = \frac{R}{R + Rd1 + Rd2} = \frac{R}{R + 2Rd}$$

(Please see figure 3 in appendix A for complete calculations)

## SPICE SIMULATION

### STEP 4.

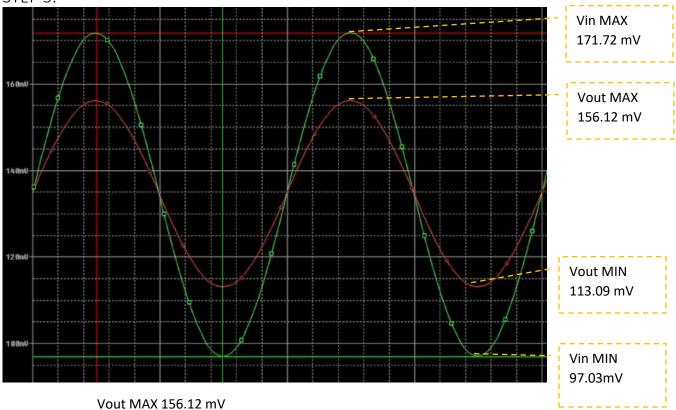


Copy and paste the GND\_0 circle in order to connect the Analog GND to the appropriate wires in your circuit.

$$Id1 = \frac{\frac{Vbias}{Rbias} + \frac{Vd2}{R} - Vd1\left(\frac{1}{R} - \frac{1}{Rbias} - \frac{2}{R}\right)}{2 + \frac{R}{Rbias}} = \frac{\frac{6}{4700} + \frac{.7}{240} - .7\left(\frac{1}{240} - \frac{1}{4700} - \frac{2}{240}\right)}{2 + \frac{240}{4700}}$$

 $= 549.79\ micro\ Amps$ 





$$\frac{5 + ep 5}{\sqrt{50} - e^{-5}} = \frac{240}{240 + 28d}$$

$$240 (.576)^{-1} = 240 + 28d$$

$$240 (.576)^{-1} - 240 = 8d$$

$$2$$

$$88.33 = Rd$$

$$\frac{(.026)}{562.5m}$$

$$\frac{(.026)}{(.026)}$$

$$\frac{(.026)}{562.5m}$$

$$\frac{(.026)}{(.026)}$$

$$\frac{(.$$

## STEP 6.

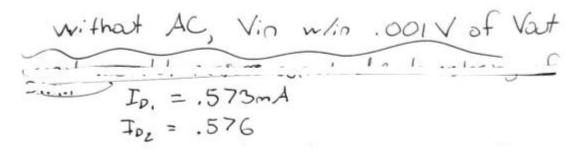
Step 6

Voias	10stp-p	Vin P-P	gain
2	20.72 m	78.66 m	.2634
4	35.17m	76.08m	.4623
8	47.81m	73.58m	.6498
10	51.32m	73.19	.7012
16	57.121,	72.15~	.7917
40	64.05	70.97m	.9025
(00)	67.24	70.45m	,9544

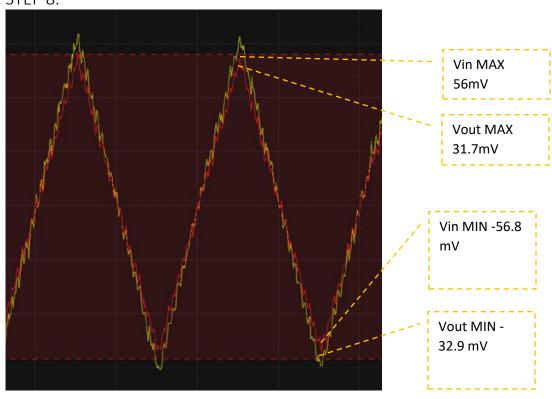
As Vbias increases, the gain approaches a unity asymptote. The Vbias signal is shared between Vin and Vout equally, as the Vbias signal becomes large, the small signal input becomes less relevant in comparison.

## **EXPERIMENT PART 1**

STEP 7.



STEP 8.



Vin MAX 171.72 mV Vin MIN 97.03mV

Vout MAX 156.12 mV Vin MIN 113.09 mV

us vbias 1, output is shifted up

us vbias 1, " "down ubtil

bian is too love. Fx Vbin) =. SV killed output

us vbian 1, gain approaches 1

STEP 9.

$$\frac{\sqrt{\text{out}_{P-P}}}{\sqrt{\text{in p-P}}} = \frac{R}{R + Rd 1 + Rd 2}$$

$$\frac{70mV}{12mV} = .625 = \frac{240.15}{240.15 + 2Rd}$$

$$(240.15)(.625)' = 240.15 + 2Rd$$

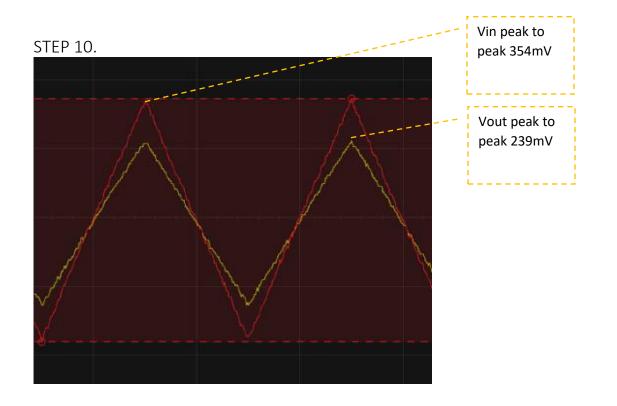
$$(240.15)(.625)' - 240.15 = Rd$$

$$2$$

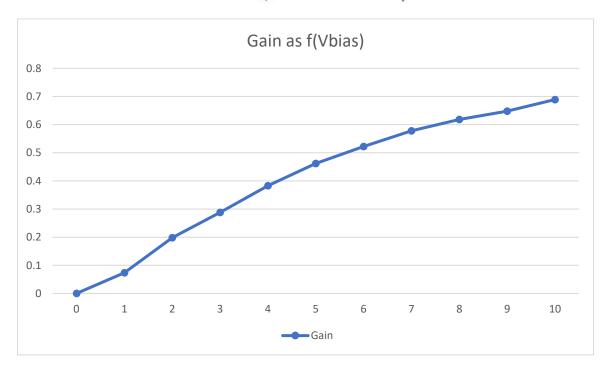
$$Rd = 72.045$$

$$72.045 = \frac{n(.026)}{.574m}$$

$$n = 1.591$$

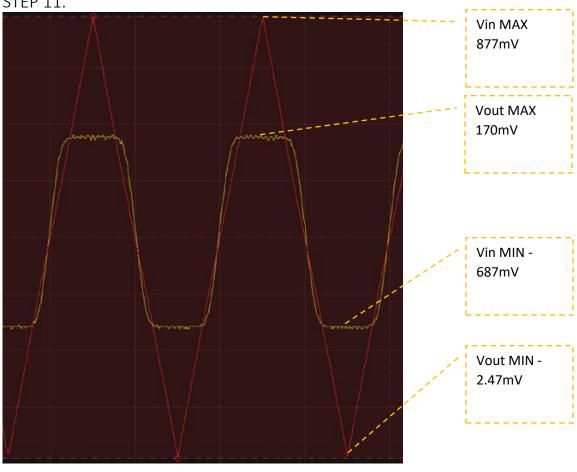


v bias	vout p-p	Nhp-1	gw -
0	0	~ 407mV	0
1	26.8 mV	~391mV	.0137
2	74 mV	~374mV	108
3	WYMV	~37 tmV	.288
4	Homv	-364 mV	. 383
5	169m1	~ 366mV	1,442
6	189 mV	~562mv	.5 12
7	208 m	-360 Mr	. 678
8	220mV	~356 mV	.618
9	228mV	-358mV	.648
10	241mV	~350 mV	.689



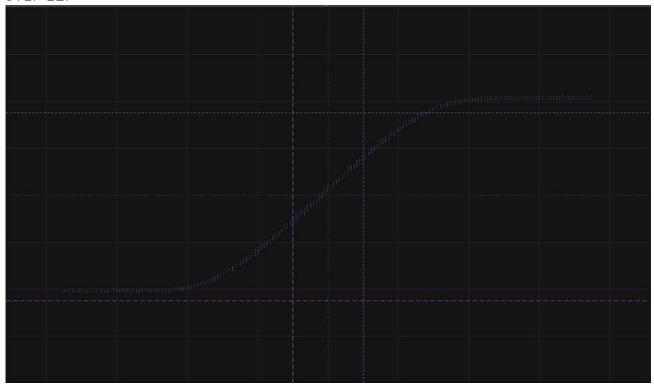
## **EXPERIMENT PART 2**



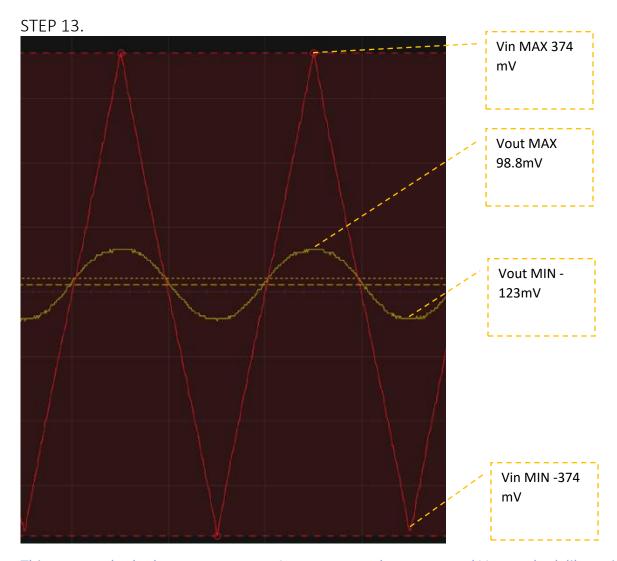


vbias	pos die	reg dip
4	165mV	-12.3 mV
3	115,00	-10 mV
5	214 mV	-10 mV
6	263mV	-10. mV
7	BILMY	-10 mV
8	350mv	-10mV
0)		1

STEP 12.



This initially seemed to be a sweep of the gain as a function of Vbias since there is a plateau on the left and it approaches a value on the right with a linearity region in between but the left side of this graph does not begin at zero on the vertical scale nor does it approach 1 on the right.



This step made the least sense to me, I was unsure why we wanted Vout to look like a sine wave but there were a couple ways to do it. We chose Vbias as 5V then cleaned it up a bit further by changing the volts per division for the output.

## **CONCLUSIONS**

#### Item 1.

Students are told that the standard voltage approximation of a 0.7V drop across a forward biased diode is acceptable. Based on the three plots in Step 1, does it look like the standard voltage approximation holds true for all current ranges?

Discuss this issue; Why is  $V_D = 0.7V$  acceptable for general use?

At first glance, the plots make it appear this approximation is not acceptable. Looking closely at them as a whole, with the scale of current in mind, it's a different story. Vd as .7V is acceptable for general use because it offers a happy medium between ease of use and accuracy. The ideal model is inaccurate but very easy to use and the exponential model is very accurate but hard to use for hand analysis.

#### Item 2.

Re-state your expression from Step 2. What relationship between the small-signal resistance of the diode and the resistance *R* is indicated when a small-signal gain near unity is observed?

What relationship between the small-signal resistance of the diode and the resistance *R* is indicated when a small-signal gain near zero is observed?

$$Id1 = \frac{\frac{Vbias}{Rbias} + \frac{Vd2}{R} - Vd1(\frac{1}{R} - \frac{1}{Rbias} - \frac{2}{R})}{2 + \frac{R}{Rbias}}$$

$$Vx = \frac{\frac{Vd1 + Vd2}{R} + \frac{Vbias}{Rbias}}{\frac{2}{R} + \frac{1}{Rbias}}$$

#### Item 3.

Use the large-signal model to explain the data from Step 11. That is, explain the relationship between  $V_{BLAS}$  and the clipping levels.

$$V_D = nV_T \ln \left( \frac{I_D}{I_S} \right)$$

Vbias serves to increase the forward bias current over the diodes, so as it increases so does the current. Is, Vt, and n are constants for an individual diode so the forward current is all that will determine the voltage across the diode. By transitivity, this means the greater Vbias then the greater Vd.

#### Item 4.

The large-signal model described in conclusion item 3 can explain the observed clipping levels, but can it be used to calculate the small-signal gain?

Why or why not?

The large signal model does not linearize it's elements, so it cannot be used to calculate the small signal gain.

#### Item 5.

Can the small-signal model be used to calculate the output clipping levels?

Why or why not?

The small signal model alone will not produce any asymptotes and thus will not show any clipping levels.

#### Item 6.

The large-signal model  $I_D = I_S \exp\left(\frac{V_D}{nV_T}\right)$  was not used to calculate the diode bias

currents.

Could it be used for that purpose?

If so, why wasn't it used to calculate bias currents?

It could be used for this purpose for diodes in forward bias, yes. It requires knowledge of the saturation current, n, and the voltage drop across the diode. Our calculated values of n changed depending on our Vbias setting so we would have had to calculate a new n for every occasion we would use this.

## APPENDIX A

Figure 1.

For silicon, intensic carrier concentration (ni) is:

$$n_i \approx \frac{1.5 \cdot 10^{10}}{cm^5}$$

Step 1)

Port 1. No  $\approx N_0 = \frac{1 \cdot 10^{15}}{cm^5}$ 
 $P_0 \approx \frac{(7:)^2}{N_0} = \frac{(1.5 \cdot 10^{10}/cm^3)^2}{(1 \cdot 10^{15}/cm^3)}$ 

Port 2. Po  $\approx N_A = \frac{1 \cdot 10^{17}}{cm^5}$ 

No  $\approx \frac{(0:)^2}{N_A} = \frac{(1.5 \cdot 10^{10}/cm^3)^2}{(1 \cdot 10^{17}/cm^3)}$ 

Port 3  $V_0 = V_T \ln \left( \frac{N_A N_D}{(0:)^2} \right)$ 

Vo =  $(26mV) \ln \left( \frac{10^{17}}{cm^3} \cdot \frac{10^{15}}{cm^5} \right)$ 
 $V_0 = (26mV) \ln \left( 444.44 \pm 9 \right)$ 
 $V_0 = (26mV) \left( 26.8201 \right)$ 
 $V_0 = (26mV) \left( 26.8201 \right)$ 
 $V_0 = (26mV) \left( 26.8201 \right)$ 

Figure 2.

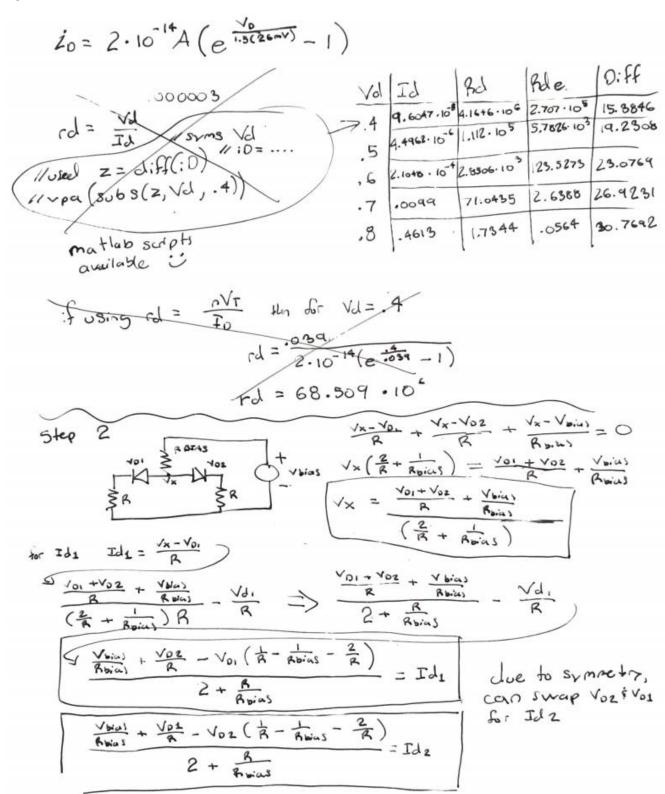


Figure 3.

