EEE 108L MICRO-ELECTRONICS 1
LAB 8

Lab Session: Tuesday 3PM - 5:40PM

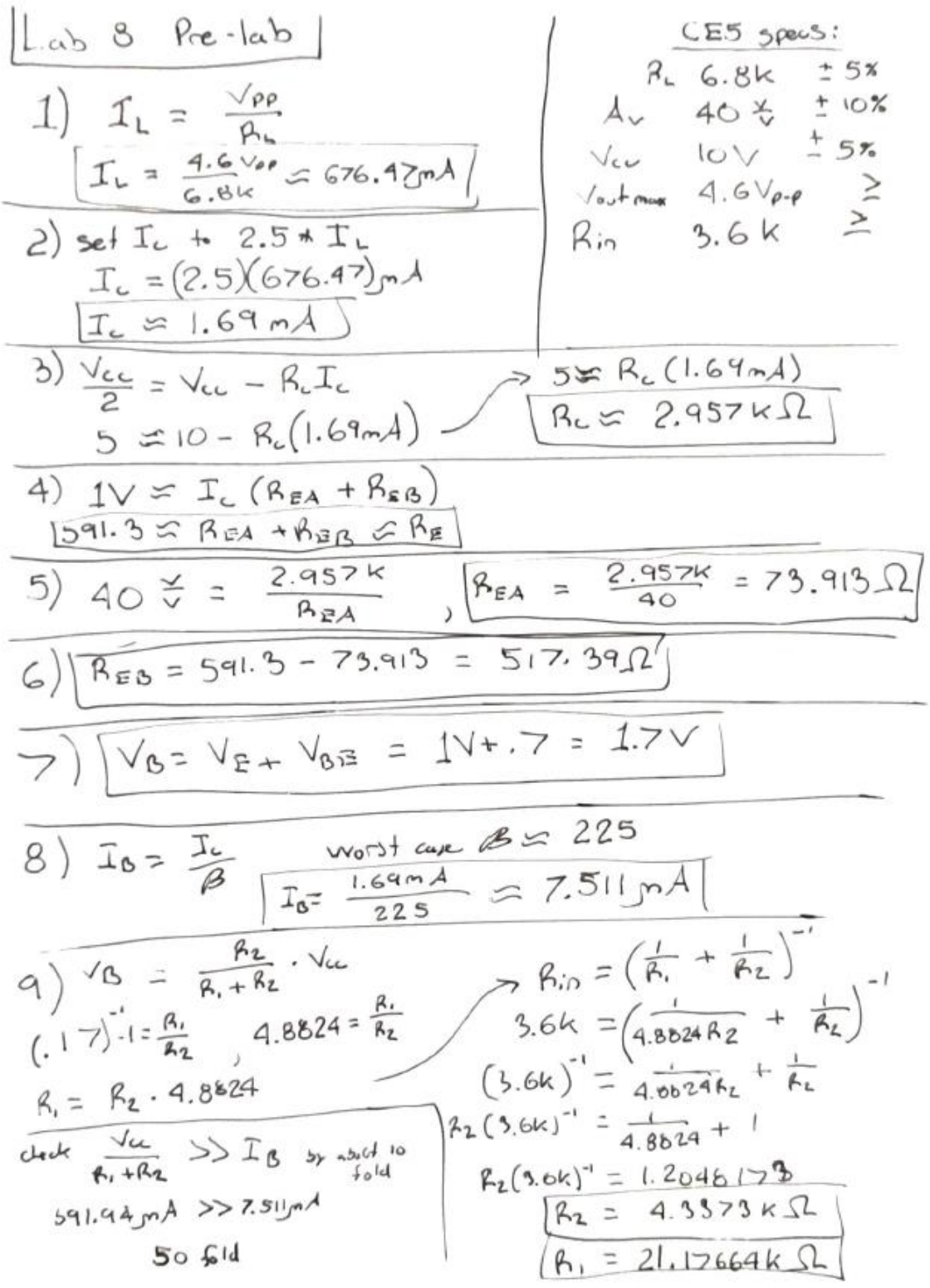
Student Name: Andrew Robertson

TABLE OF CONTENTS

PRE-LAB CALCULATIONS

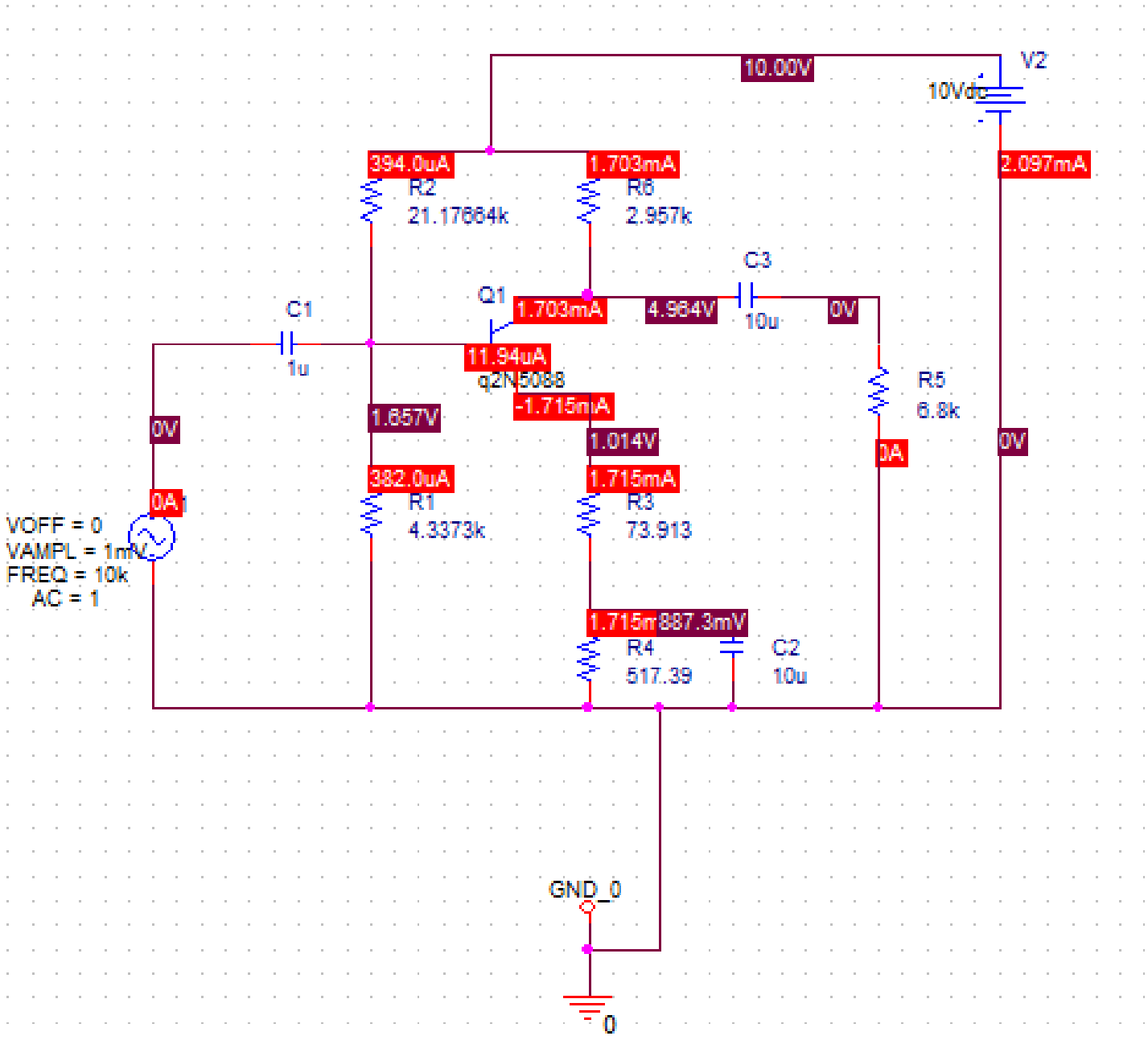
STEP 1.

(Using the steps outlined in Appendix A, Figure 1)

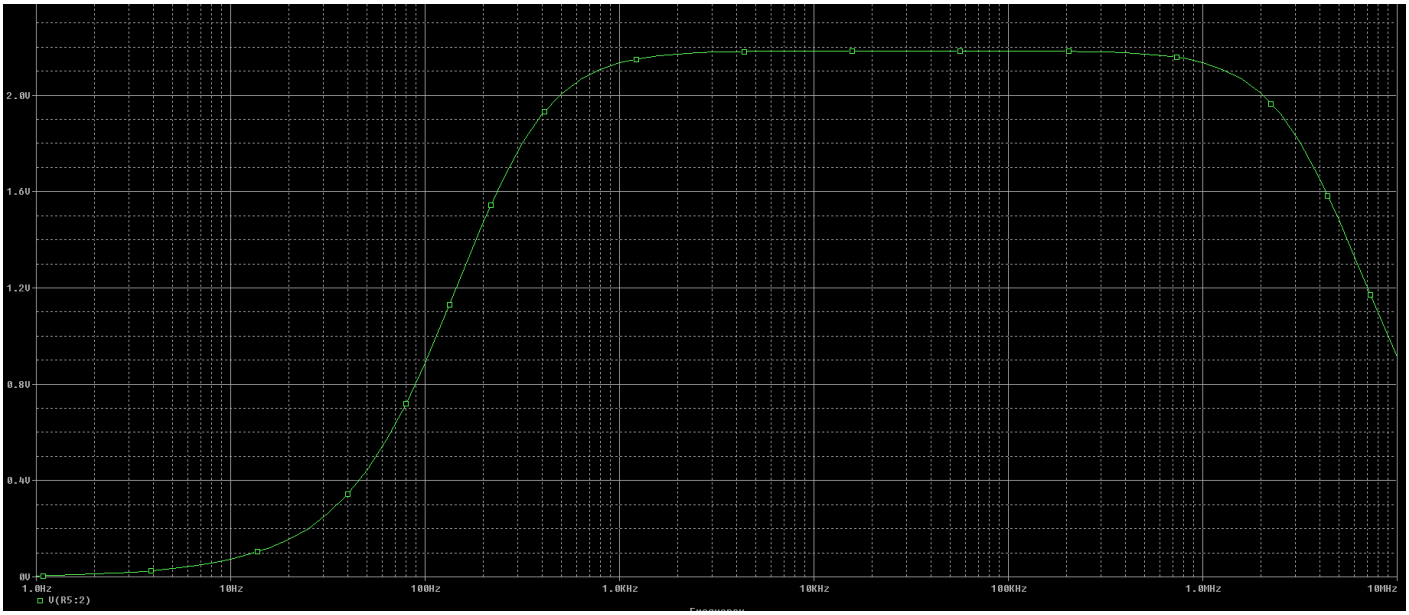


SPICE SIMULATION

STEP 2.



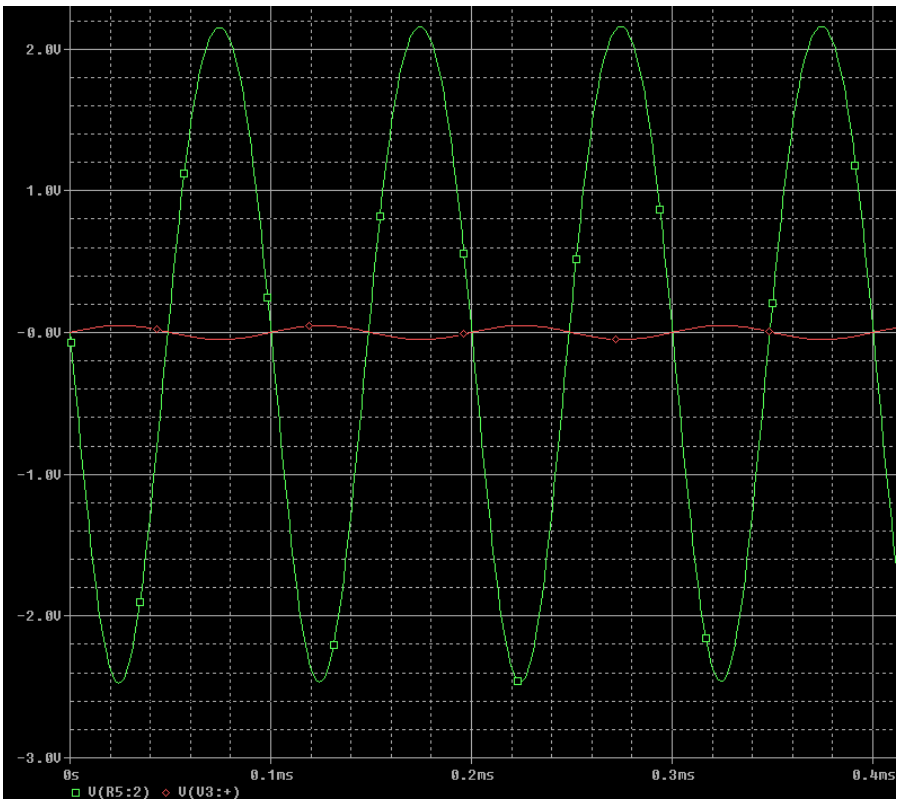
STEP 3.



In the mid band we're seeing 2.19 Volts out when there is 50 millivolts coming in. $\frac{2.19V}{50mV} \cong 43.8\frac{V}{V}$

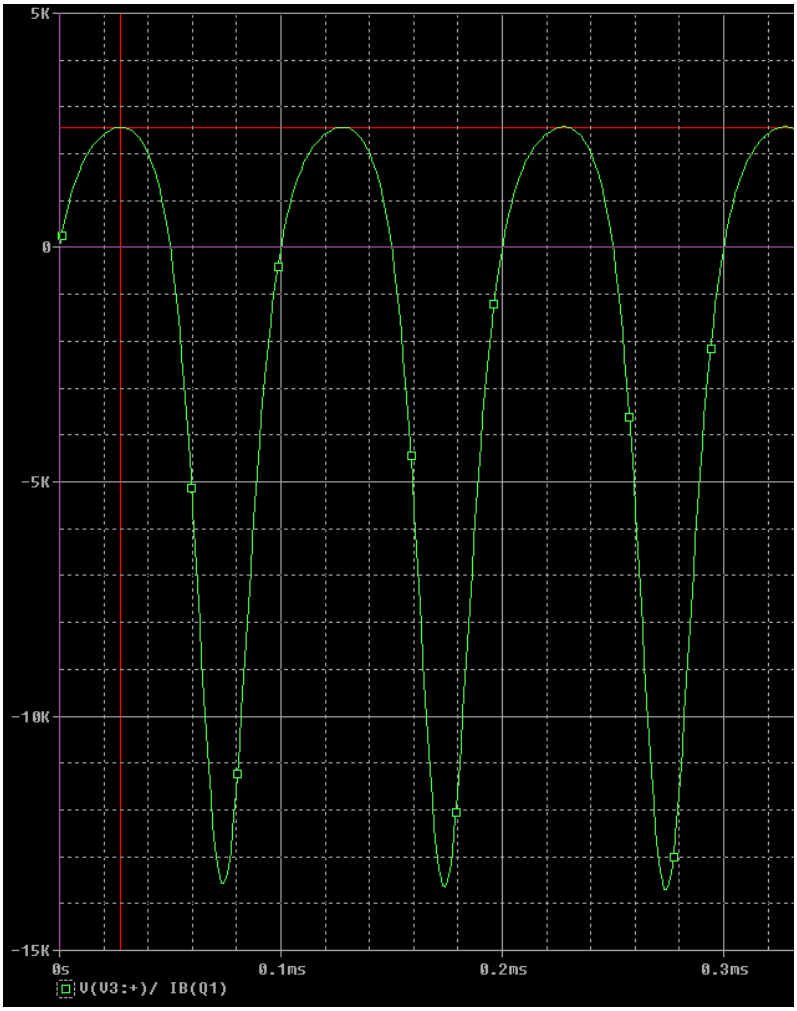
-3Db point @ roughly 250Hz

STEP 4.



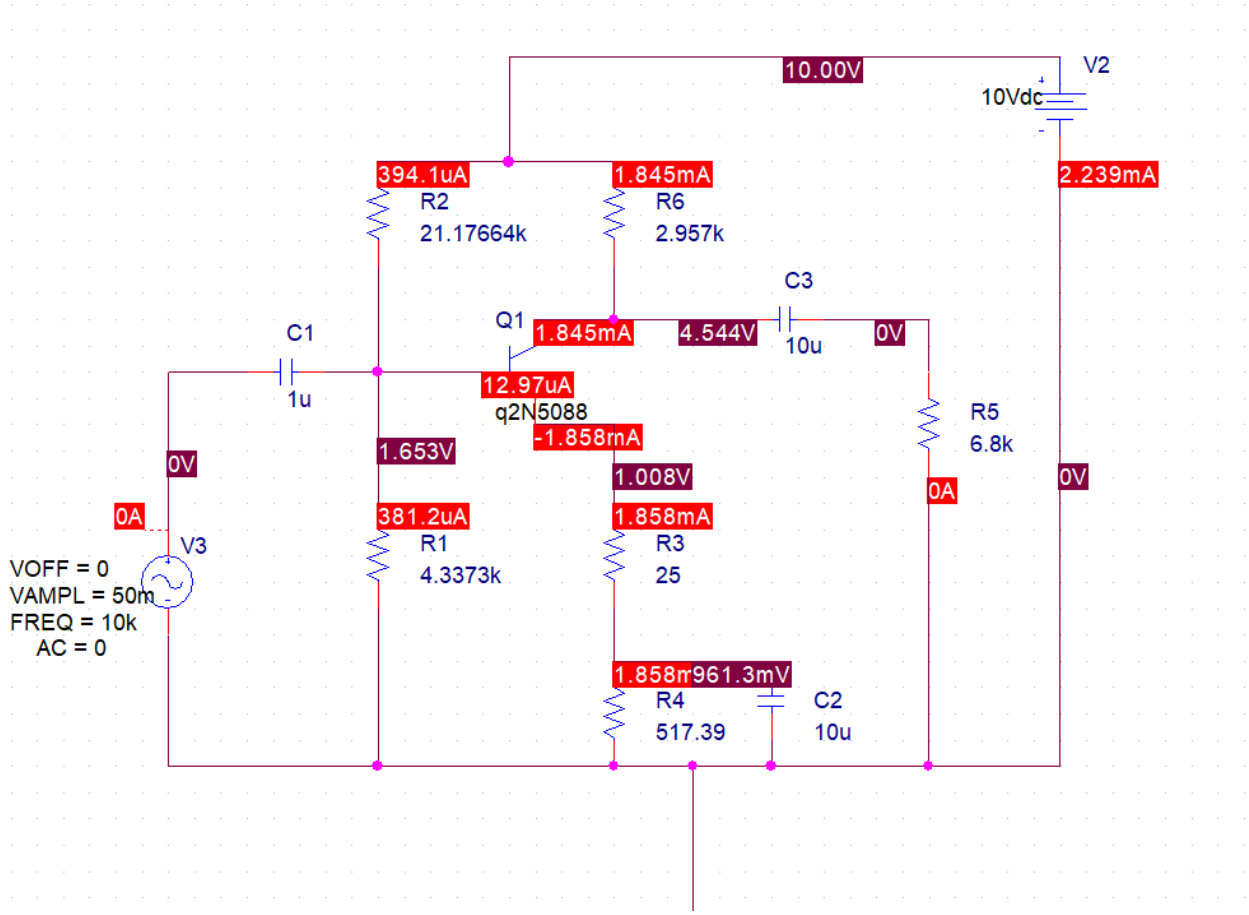
This is again at 50mV p-p in.

STEP 5.



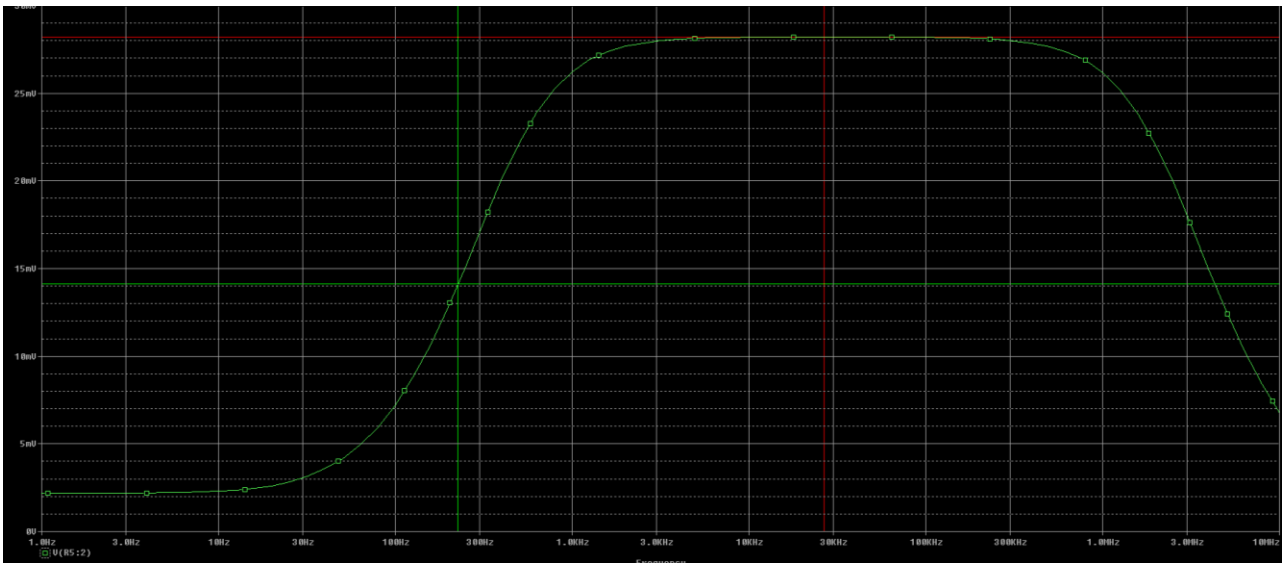
I could not understand what the appendix was asking of us so Instead I used two traces and the division function to check for maximum input resistance. Vb / Ib. This seemed like a good idea but the value was roughly 2.6k instead of the parallel combination of resistors connected to the base, which was 3.6k so the idea is flawed.

STEP 6.

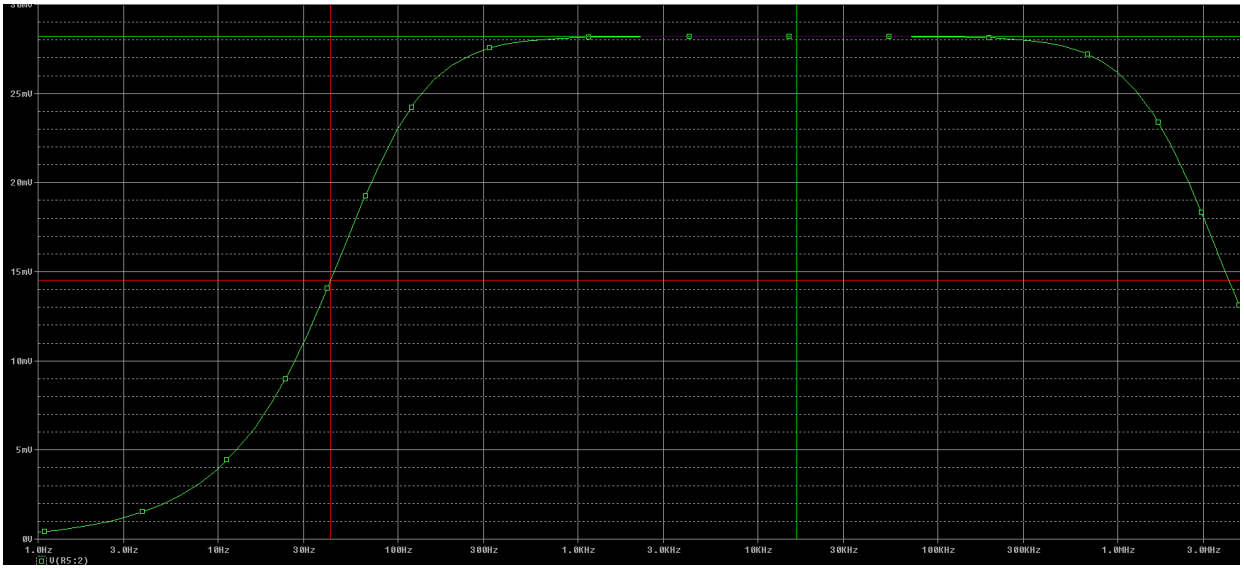


Changing R3 to about a third of the original value allowed us to exceed specs (in simulation). Note that Vc is now roughly 4.5V instead of 5V.

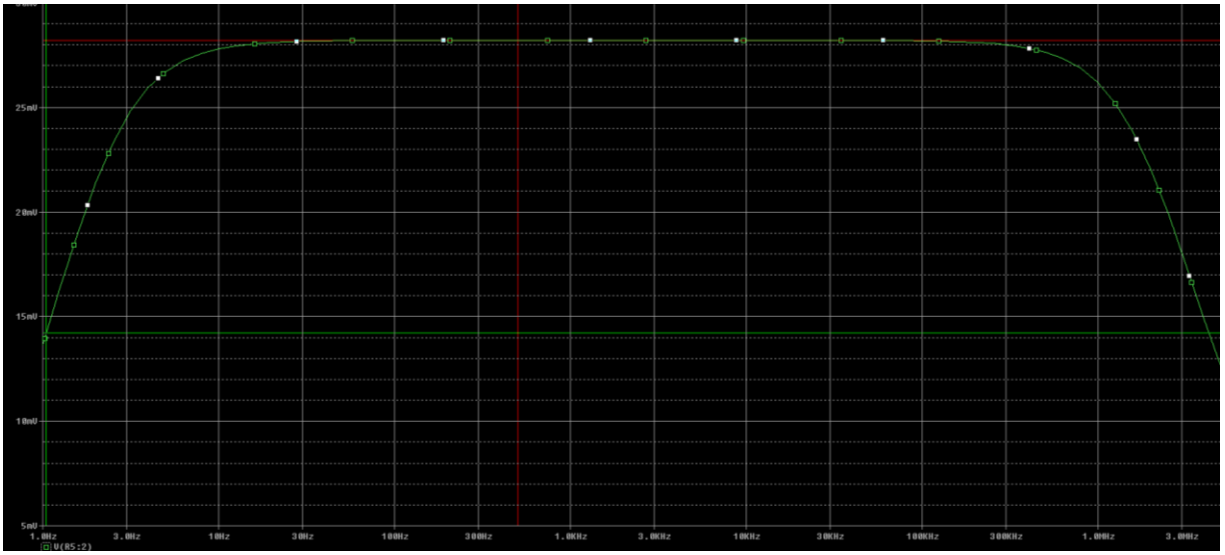
STEP 7.



(Cursor is further left than it should be. Initially forgot half power point is -3db is .707 times the max)
CE -3db point at 350Hz



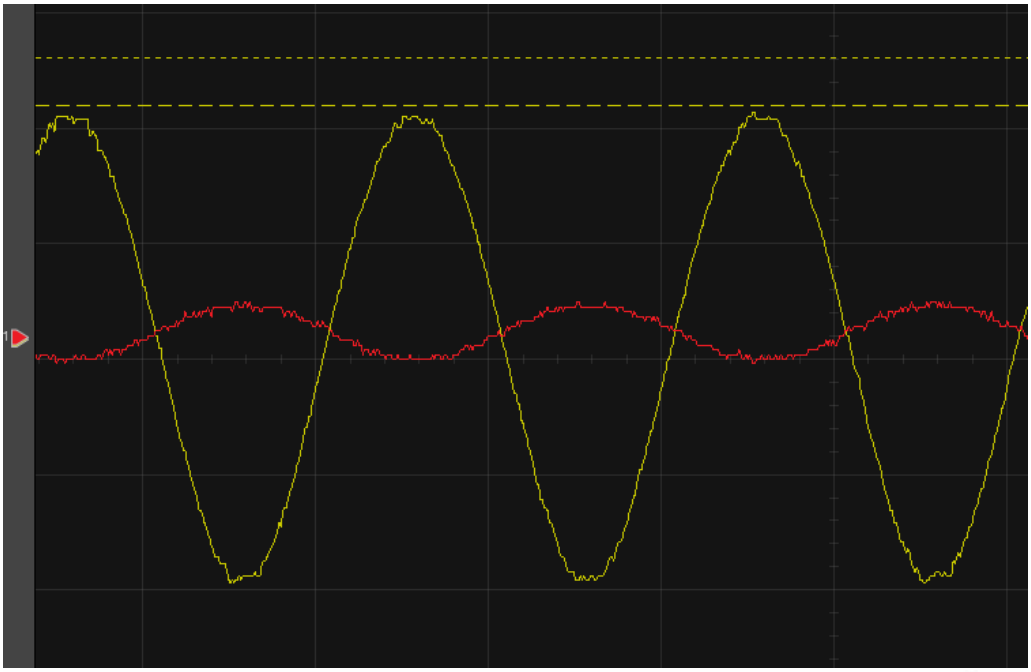
Cursor is further left than it should be. Initially forgot half power point is -3db is .707 times the max)
CIN -3db point at 50Hz



Cursor is further left than it should be. Initially forgot half power point is -3db is .707 times the max)
COUT -3db point at 1.3Hz

EXPERIMENT

STEP 8.



Step 8) $I_c = \frac{V_{RC}}{R_c} = \frac{4.997V}{2.98k} = 3.355mA$

$V_c = 5.1895$

$V_B = 1.5V$

$V_E = 870.66mV$

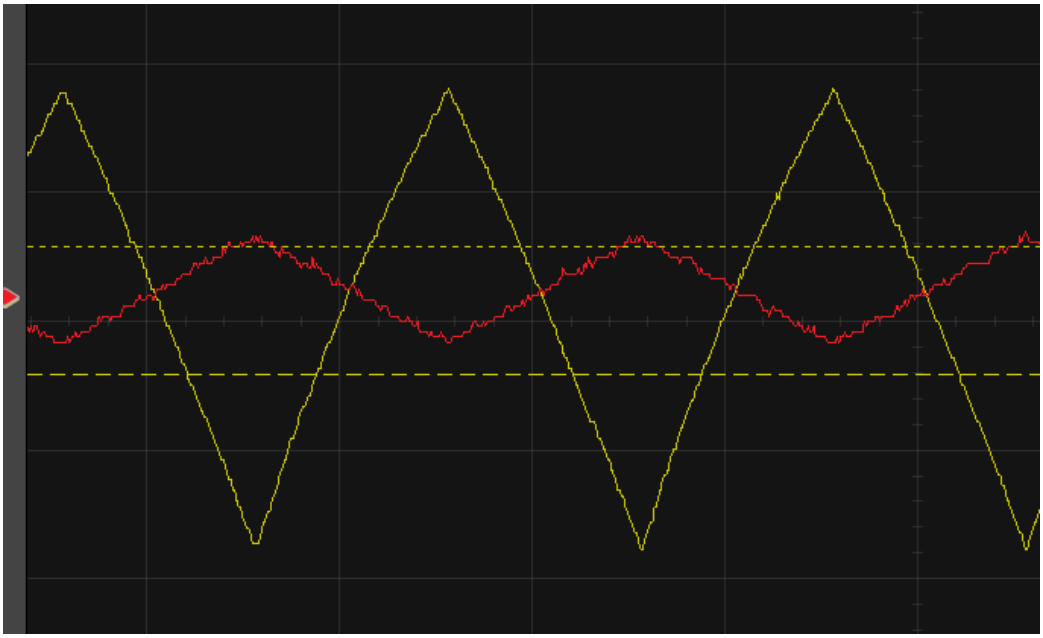
This is reasonably close given the deviation from the original design.

STEP 9.

Using a frequency of 10k (found during SPICE simulation), the snapshot in step 8 has the following characteristics:

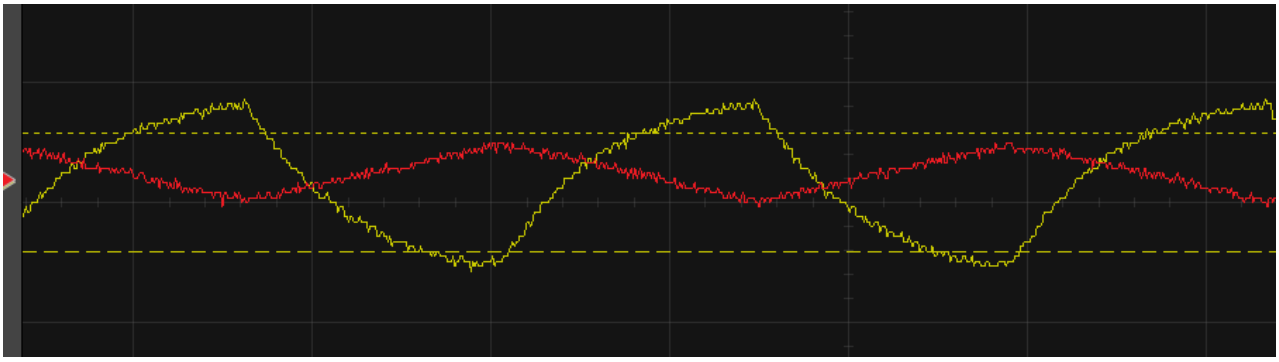
$$\frac{2.04V}{53.5mV} \cong 38.13\frac{V}{V}$$

STEP 10.



Was a slight bit unsure what the instructions meant to look for here as well. At first I thought clipping was the goal but after playing around with the input amplitude some slew rate becomes visible and that seems more like what was asked. Here, it started to become apparent around 90mV.

STEP 11.

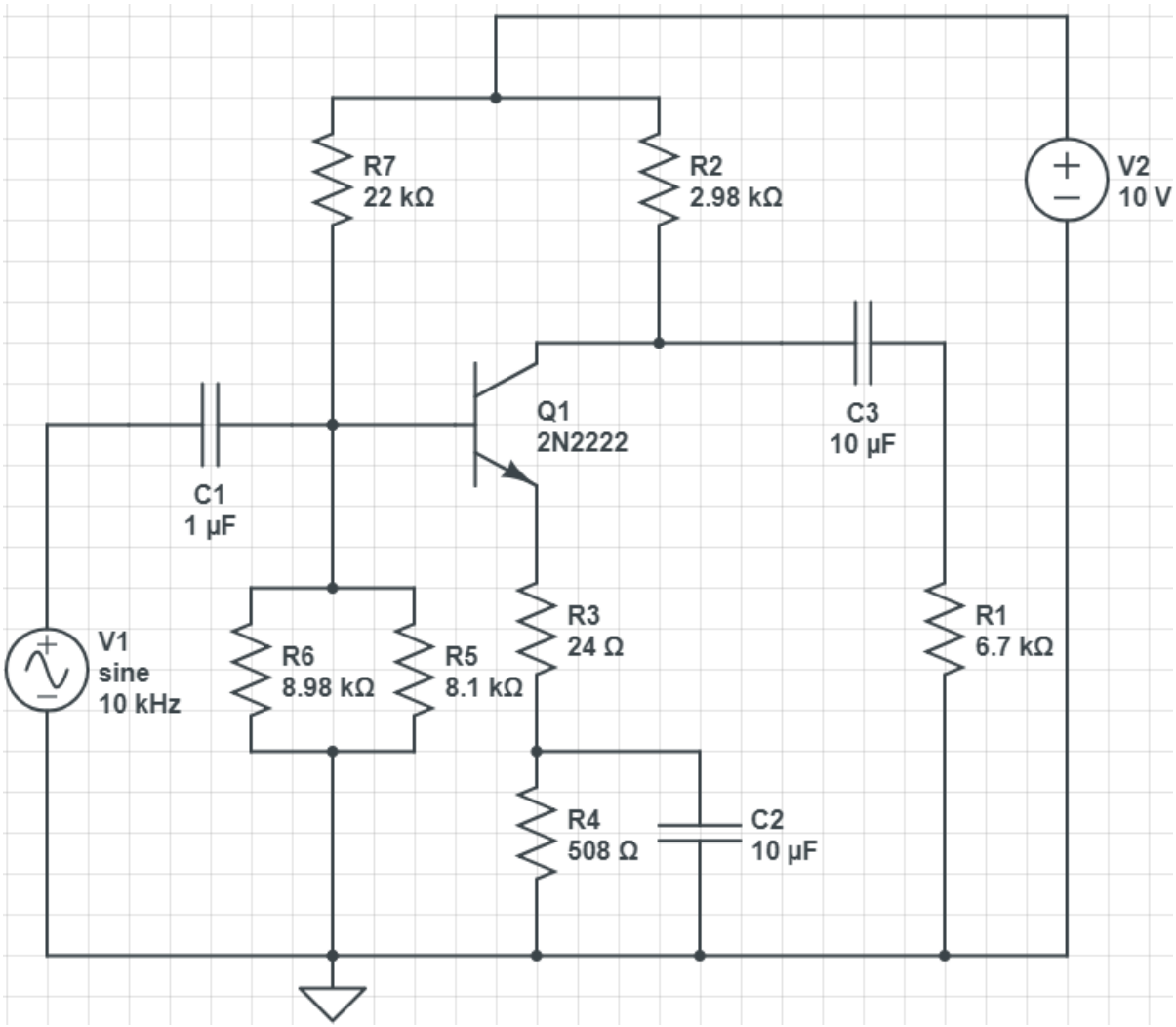


(In our design, both 10 micro Farad capacitors were polarized) The lower -3db frequency we found was at 700Hz, about twice that of CE.

CONCLUSIONS

Item 1.

Item 1. Present your final design in the form of a schematic diagram with all part values labeled. State the specifications for gain and output voltage swing, along with the given specifications. State the collector current and the value of V_{BB}.



Gain: **38.13 V/V**
Out swing: **4.6V**
Ic: **3.355mA**
VBB (V1): **50mV**

Set CE5	Load Resistance	R_L	6.8k	Ω	±5%
	Voltage gain	v_o/v_s	40	V/V	±10%
	Power supply voltage	V_{CC}	10	V	±5%
	Minimum swing capability	$v_{out\,max}$	4.6	V_{pp}	≥ spec.
	Input Resistance	R_{in}	3.6k	Ω	≥ spec.

APPENDIX A

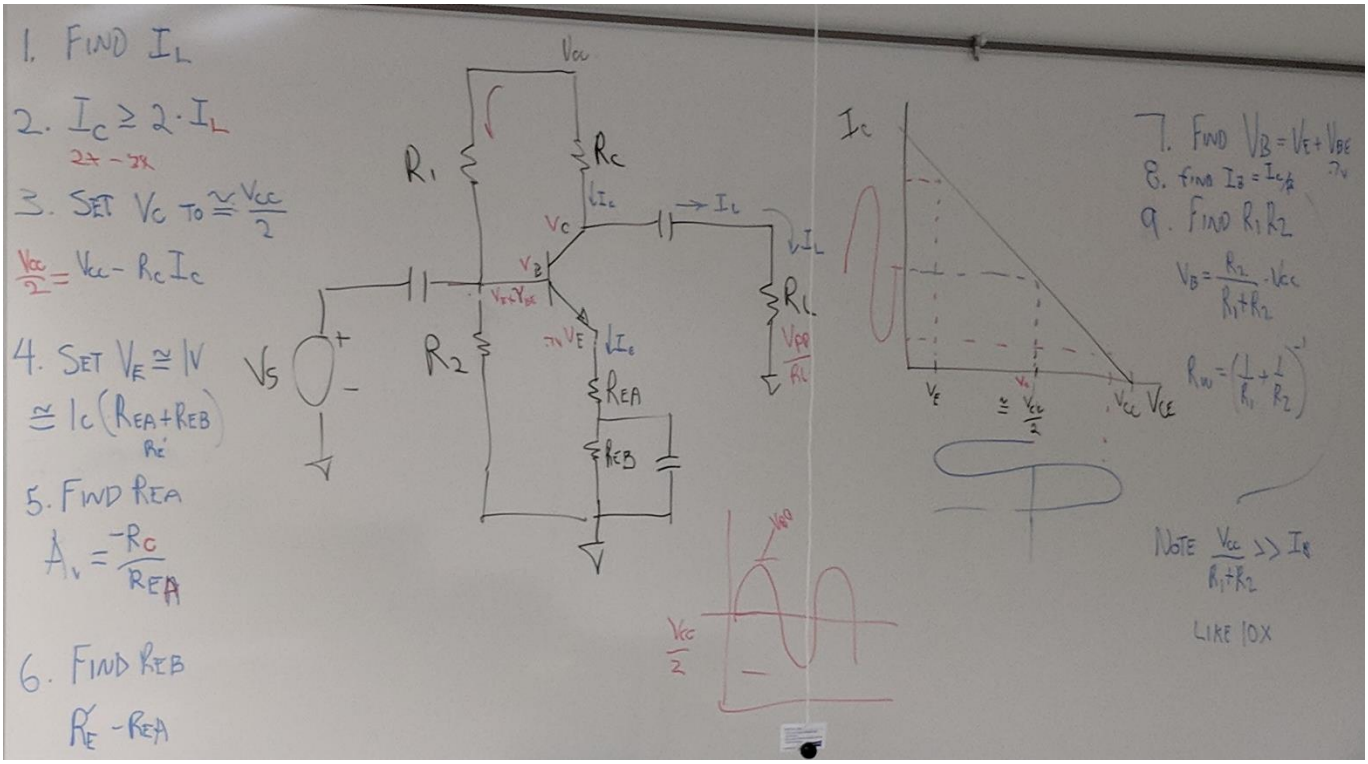


FIGURE 1