EEE 108L MICRO-ELECTRONICS 1 LAB 7

Lab Session: Tuesday 3PM - 5:40PM

Student Name: Andrew Robertson

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PRE-LAB CALCULATIONS

STEP 1.

$$i_{c} = \frac{3}{(3+1)}i_{c}$$
 $i_{c} = \frac{3}{(3+1)}i_{c}$
 $i_{c} = \frac{3}{(3+1)}$

STEP 2.

$$1.2733 = I_{B} \cdot 22k + .7v + (I_{B} \cdot 225)1k$$

 $.5733 = I_{B}(22k + 225k)$
 $I_{B} = 2.32_{m}A$

$$I_c = 225 I_B = .522 mA$$

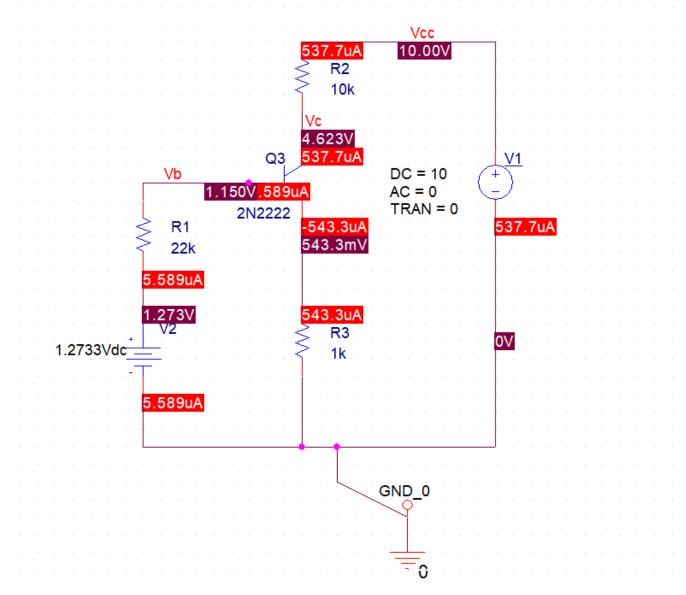
 $\frac{.522 mA}{.5 mA} = 1.044 = 4.4\%$

STEP 3.

STEP 4.

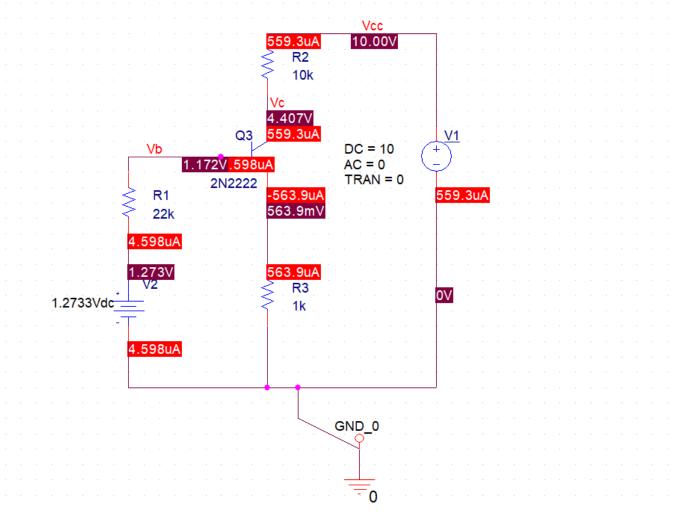
SPICE SIMULATION

STEP 5.



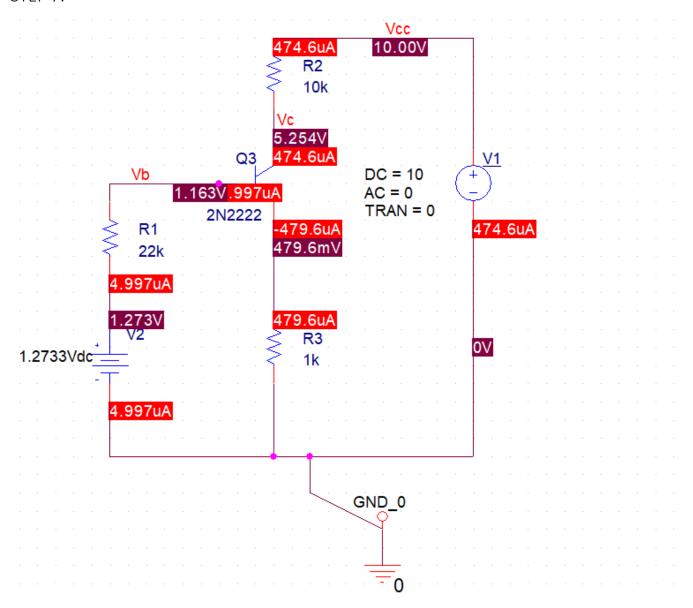
VBB	VB	VE	VC	IC	IB	β
1.2733V	1.15V	.5433V	4.623V	537.7 micro	.589 micro	150

STEP 6.



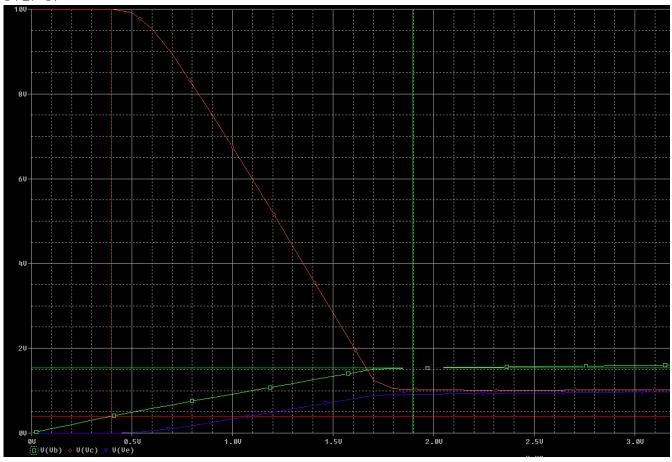
VBB	VB	VE	VC	IC	IB	β
1.2733V	1.172V	.5639V	4.407V	559.3 micro	.598 micro	225

STEP 7.

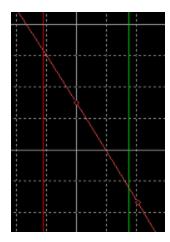


VBB	VB	VE	VC	IC	IB	β
1.2733V	1.163V	.4796V	5.254V	474.6 micro	.997 micro	150

STEP 8.



Note, the green cursor should be slightly more left here, at a point where Vb(green) and Vc(red) cross. There is no defined point where Vb is less than Vc so cutoff is technically not occurring however left of the red cursor the behavior is most certainly not the same as the forward active region and so it acts this way, forward active will be up to the (adjusted) green cursor, and saturation past that.



Using a small section of the forward active region, we can calculate $\frac{\Delta V_{c}}{\Delta V_{B}}$

$$\frac{7.5862 - 5.3846}{827.294 - 1.0689} \cong -9.1124$$

EXPERIMENT

STEP 9.

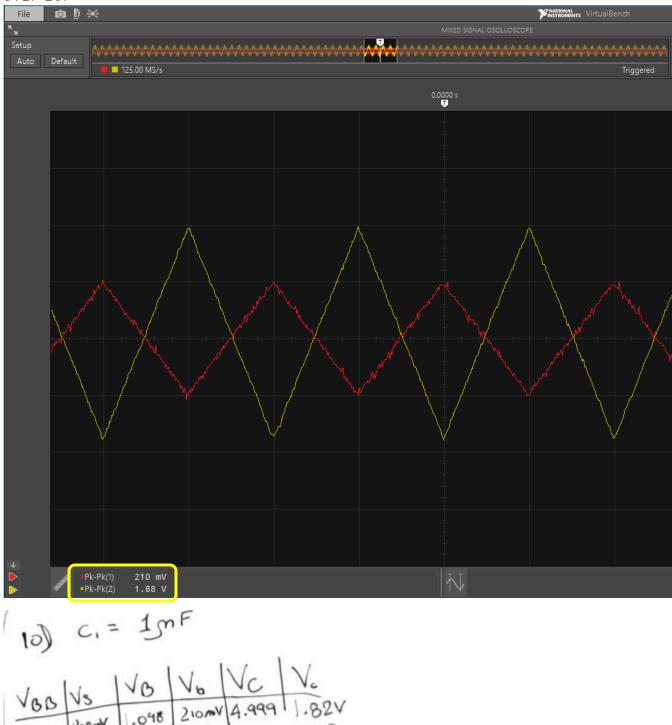
a) VBB Ic Vc VB	Ic = Vu-Vc Rc	Rc= 9.95K
1 ,2600 6.319 ,9586	15 10 15k	
1.5 .305 . 1.992 1.415	$5ml = \frac{10-x}{4.95k}$ $4.975 = 10-x$ $x = \sqrt{c} = 5.0$	
2 .9086 .9692 1.549	975 = 10 -	25
2.5 ,40% ,9642 1.580	4, 10= 5,0	
3.0 .907 .9780 1.408	×	
3.5 .905 .9946 1.635		
4.0 ,903 1.012 1.461		
6.0 1 1.038 1.757		
VB 12 15.02 5.025 1.1		
VOP IL VC VB 1.27 1.6040 3.99 1.205		2002

Calculating for $\frac{\Delta V_{\scriptscriptstyle C}}{\Delta V_{\scriptscriptstyle B}}$

$$\frac{5.023 - 3.99}{1.1 - 1.205} \cong -9.838$$

This is a similar value to the previous step.

STEP 10.



Small signal gain Vcp-p / Vbp-p : $\frac{1.88}{.210}\cong 8.95238$

This is again near the value in step 8

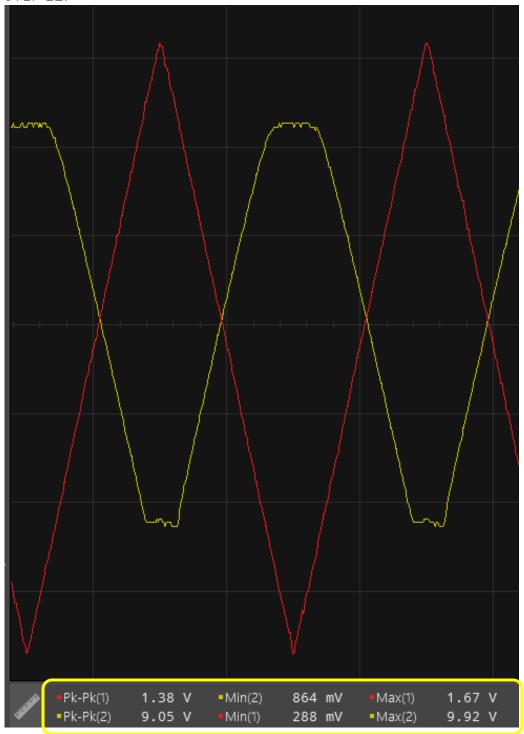
STEP 11.



The blue line indicates the DC bias, about 5v at the collector

Pk-Pk(1)	210 mV	Min(2)	4.05 V	Max(1)	1.20 V
Pk-Pk(2)	1.88 V	Min(1)	994 mV	Max(2)	5.93 V

STEP 12.



STEP 13.

$$R_{2}R_{1} = \frac{\lambda_{2}R_{1}}{R_{2}+R_{1}}$$

$$190.641 \cdot 10^{3} = R_{1}$$

$$22K = \frac{R_{1}R_{2}}{R_{1}+R_{2}}$$

$$(22K)(R_{1}+R_{2}) = R_{1}R_{2}$$

$$(22K)(190.641K+R_{2}) = (190.641K)(R_{2})$$

$$190.641K+R_{2} = 8.66551 \cdot R_{2}$$

$$190.641K = 8.66551 \cdot R_{2} - R_{2}$$

$$190.641K = (8.66551 \cdot R_{2} - R_{2})$$

$$190.641K = (8.66551 - 1)R_{2}$$

(Ran out of time to introduce these resistors to our circuit and test it)

CONCLUSIONS

Item 1.

Considering the collector current of the transistor, comment on the agreement between the preliminary calculations of Step 1 and the SPICE simulations of Step 5. Describe how you arrived at the required value of V_{BB} in Step 1, including the equations used and the assumptions made. What did SPICE do differently? (Hint: what values of V_{BE} and β did SPICE use?)

Seen in figures 2 and 3 of Appendix A, the model used a VBE (VJS) of .7. Beta was originally 150. Given these values we could first plug in our target current to Ic and Ie, using the given assumption of equivalence. We then use beta to find Ib. Knowing VBE we could then calculate Vb then finally VBB by adding the voltage drop of Rb to Vb.

Item 2.

Consider the effect of increasing the value of β in the hand calculations and in the SPICE model (Steps 2 and 6). Was the effect on the collector current comparable? Comment on the sensitivity of the collector current to the value of β . How does this issue impact the design process, given that the β of manufactured transistors varies significantly?

I'd say the results were comparable. Since the initial value of Ic wasn't exactly .5 mA as used in the prelab we'll need to compare percentages. The calculated change was 4.4% when beta was bumped by 50%. The simulated change is $\frac{559.3}{537.7} = 104.01\%$ so 4.01% change. Seems this will mainly just affect the extremes of the gain, the clipping points since Vc is changed

Item 3.

Consider the effect of increasing the temperature in both the preliminary calculations and in the SPICE model (Steps 3 and 7). Were the changes similar? Comment on the sensitivity of the collector current to the temperature. How does this issue impact the design process, given that the temperature of operation varies significantly?

This has a similar affect as Item 2 observed bu in the opposite direction. Higher temperatures mean a greater resistance overall, and lower current reflected this. I believe the circuits should be engineered with these factors in mind. Built to meet spec in the worst of reasonable conditions.

Item 4.

From the measured data of Step 9, calculate the beta of the transistor used.

$$\frac{1}{2c} = \left(\frac{B}{B+1}\right) \frac{1}{2c} = \sum_{z=1}^{2} \frac{1}{2c} \left(\frac{B}{B+1}\right) \left(\frac{1}{2c} + \frac{1}{2b}\right)$$

$$\frac{1}{2c} = \left(\frac{1}{2c} + \frac{1}{2b}\right)$$

Item 5.

In Steps 9 and 10, V_{BB} was set to the same value (such that $I_{C} = 0.5 \text{mA}$). In Step 9 the DC collector voltage was measured. In Step 10 the average value of the collector voltage was measured with an AC signal present. What conclusions can be drawn about the addition of a small signal to a biased circuit?

The small signal had virtually no affect on the circuit. VB and VC seemed unaffected.

Item 6.

Compare the small-signal gain $\frac{v_c}{v_b}$ measured in Step 10 to the slope of the

transfer characteristic $\frac{\Delta V_C}{\Delta V_B}$ measured in Step 9. Explain their relationship.

How does the expression for the small-signal gain of a common-emitter amplifier with degeneration resemble the result of Step 4?

The small signal and large signal gain in the forward active region are very close. I believe this is because of the idea behind the small signal idea. Anything nonlinear in a small enough slice can be treated as linear.

Item 7.

Relate the shape of the clipped output waveform of Step 12 to the plot of $V_{\rm c}$ generated in Step 8. How should the bias voltage at the collector be chosen for maximum symmetrical swing?

The top clipping point was roughly VCC and the bottom clipping point about one diode drop above OV. It seems a good point for the collector voltage VC would be about half of VCC.

APPENDIX A

FIGURE 1

Lab 7 Pre 1

1)

$$i_{c} = \frac{3}{(a+1)}i_{c}$$
 $i_{c} = \frac{3}{(a+1)}i_{c}$
 $i_{c} = \frac{3$

FIGURE 2

**** BJT MODEL PARAMETERS

```
X Q3.model4
       NPN
LEVEL
       1
  IS 166.780000E-15
  EG
      1.11
  BF
  NF
      1.074
 VAF
       78
 IKF
       . 5
       3.920000E-12
 ISE
       1.776
  NE
  BR 2.394
  NR
       1.074
 VAR 500
  NC
       1
 ISS
      0
       .676
  RB
        .676
 RBM
        .1
  RE
  RC
        .654
 CJE
      22.250000E-12
 VJE
       1.333
        .522
 MJE
       8.370000E-12
 CJC
 VJC
       1.333
 MJC
        .518
XCJC
        .5
 CJS
        0
       .7
.5
 VJS
 MJS
  TF 454.400000E-12
 XTF
      13.24
      4.83
 VTF
       .2163
 ITF
  TR 117.500000E-09
 XTB
      2.34
  KF
       0
  AF
       1
       2.42
  CN
   D
        .87
```

FIGURE 3

**** BJT MODEL PARAMETERS

```
X Q3.model4
       NPN
LEVEL
     1
  IS 166.780000E-15
  EG 1.11
  BF 150
  NF 1.074
 VAF
      78
 IKF
       . 5
 ISE
       3.920000E-12
  NE
       1.776
  BR
       2.394
  NR
       1.074
 VAR 500
  NC
      1
 ISS
       0
       .676
  RB
       .676
.1
.654
 RBM
  RE
  RC
       22.250000E-12
 CJE
      1.333
 VJE
        .522
 MJE
       8.370000E-12
 CJC
       1.333
 VJC
 MJC
       .518
 XCJC
        . 5
       0
 CJS
       .7
 VJS
        .5
 MJS
  TF 454.400000E-12
 XTF
     13.24
      4.83
 VTF
 ITF
       .2163
  TR 117.500000E-09
 XTB
      2.34
  KF
       0
       1
  ΑF
       2.42
  CN
   D
       .87
```