Lab 2: *Advanced synthesis*

- Copy “LAB1” directory to a one named as “LAB2”, and then go inside “LAB2”:
    - cp -r LAB1 LAB2
    - cd LAB2

Lab 2a: *Clock Gating*

- Now, add the “gate clock” option to your first compile:
    - compile_ultra -gate_clock
- Check the typical reports (add the clock gating ones) and compare with previous stage.

Lab 2b: *Optimize registers*

- Check the number of flip flops in your design (“size_of_collection” and “all_registers”).
- Now, run “optimize_registers” over your design and check again the number of registers:
    - optimize_registers
- Check the typical reports again and compare with previous stage.

Lab 2c: *Incremental and optimize_netlist -area*

- Run an “incremental compile” to do incremental synthesis over the design:
    - compile_ultra -incremental -gate_clock
- Check the typical reports again and compare with previous stage.
- Then, apply the command to optimize the area of your netlist:
    - optimize_netlist -area
- Check the typical reports again and compare with previous stage.

Lab 2d: *Change names*

- Apply the “change_names” command before writing your final design.
    - change_names -rule verilog

Lab 2e: *16bit and define the final clock period*

- Change your bus size to 16 and the clock period to 45 [ns].
- Rerun the flow just created, review the reports, save your design and now you are ready for next part of the course (Place and Route using IC Compiler).