	Saturday 3/9/19	Sunday 3/10/19	Monday 3/11/19	Tuesday 3/12/19	Wednesday 3/13/19
8:30	Registro	Asado	Event Registration	-	-
9:00			Fundamentals of CMOS II (Ronald Valenzuela)	Design Compiler I (Esteban Viveros)	IC Compiler I (Agustin Martinez)
9:30					
10:00					
10:30					
11:00			Coffee break	Coffee break	Coffee break
11:30	Introduction to Digital Design Flow (Ronald Valenzuela)		Simulation of Digital Circuits with VCS (Ronald Valenzuela)	Design Compiler II (Esteban Viveros)	IC Compiler II (Agustin Martinez)
12:00					
12:30					
13:00	Lunch Break		Lunch Break	Lunch Break	Lunch Break
13:30					
14:00					
14:30	Verilog for Synthesis (Ronald Valenzuela)		Lab 1: Verilog (Ronald Valenzuela)	Lab 3: Synthesis with Design Compiler (Esteban Viveros)	Lab 5: Place & Route with IC Compiler (Agustin Martinez)
15:00					
15:30					
16:00	Coffee break		Coffee break	Coffee break	Coffee break
16:30	Fundamentals of CMOS I (Ronald Valenzuela)		Lab 2: Verilog (Ronald Valenzuela)	Lab 4: Synthesis with Design Compiler (Esteban Viveros)	Lab 6: Place & Route with IC Compiler (Agustin Martinez)
17:00					
17:30					
18:00			Continue Lab	Continue Lab	Continue Lab
18:30					
19:00					
19:30					