LAB 0*: Familiarize with DC shell.*

- Copy the lab directory to you home directory and go to the new directory:

    % cp -r <carpeta_de_referencia>/FE/LAB0 <carpeta_de_destino>
    % cd <carpeta_de_destino>

- You can see the Verilog file here:

    % gedit ./rtl/fulladder.v

- Load the synthesis tools and then open a “dc_shell” and source the DC script:

    % dc_shell
        source -echo -verbose ./scripts/dc.tcl

- Try out the command line help to check available commands:

        help report*
        help get*

- Check the documentation of some commands:

        man report_timing
        man report_qor
        man compile_ultra

- Try out some of the commands mentioned during the course or demo sessions:

        get_designs
        get_libs
        report_lib <lib_name>
        get_attribute <lib_name> time_unit_name
        get_ports
        all_inputs
        all_outputs
        get_cells
        report_cell <cell_name>
        report_cell [get_cells –hier *C2*]

- Save a report into an ASCII file:

        report_cell [get_cells –hier *C2*] > reports/report_cells.rpt

- Open the GUI (called “Design Vision”) and review the design:

        start_gui

- In the window “Logical Hierarchy” you can see the “fulladder” design. Right-Click gives you some options. Select “Schematic View” and with double-click over the showed symbol you can see the inside of the design.

- Close the GUI window and then exit from the “dc_shell”:

        exit

- Check the report created during the session:

    % gedit ./reports/report_cells.rpt

TIP: “shell” commands can be executed from the “dc_shell” doing “sh <command>”.