Fundamentals of CMOS Design I

Ronald Valenzuela - ronaldv@synopsys.com
Corporate Application Engineer at Synopsys

Outline

Motivation

Transistors

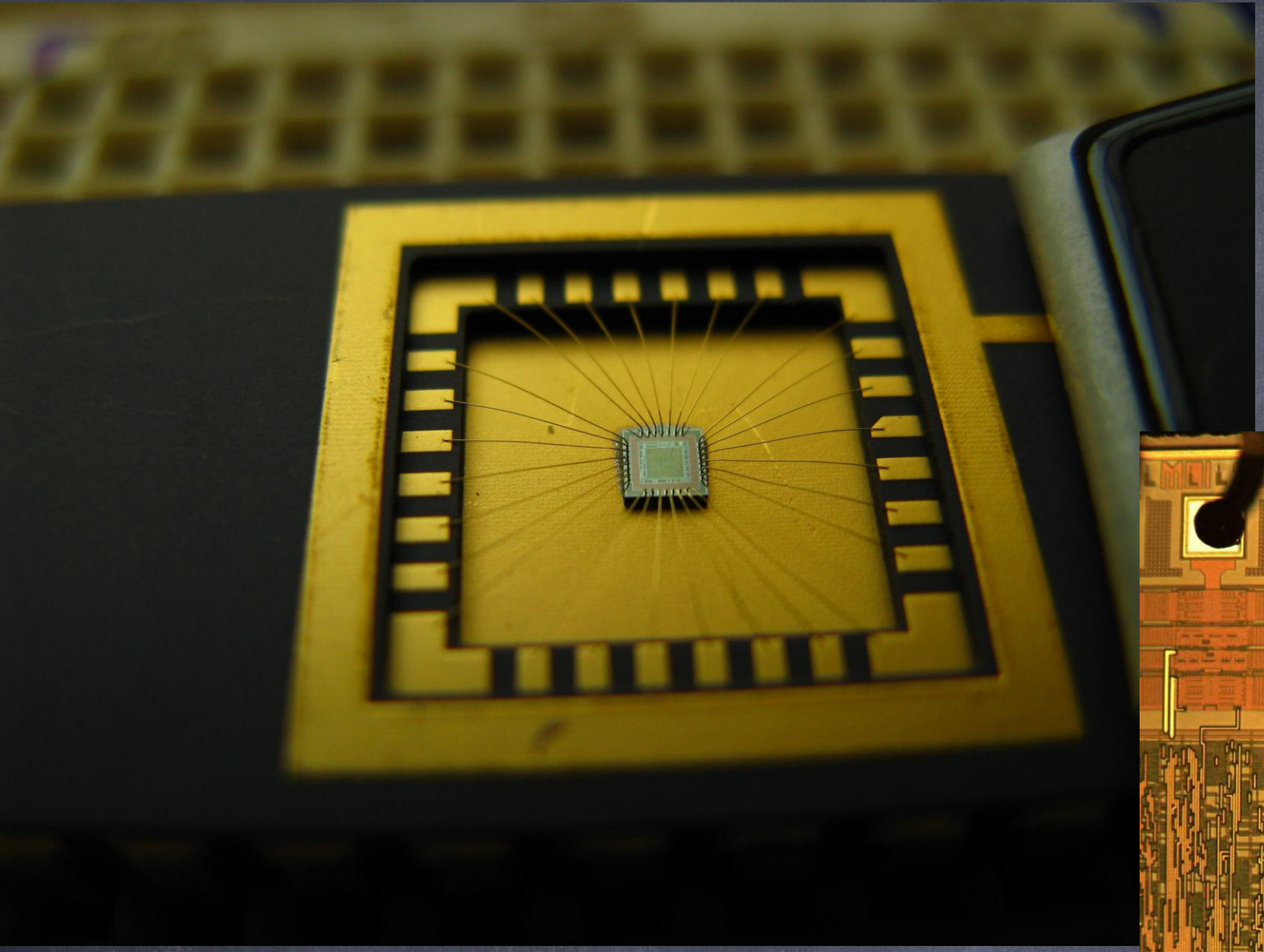
Digital Circuits

Motivation

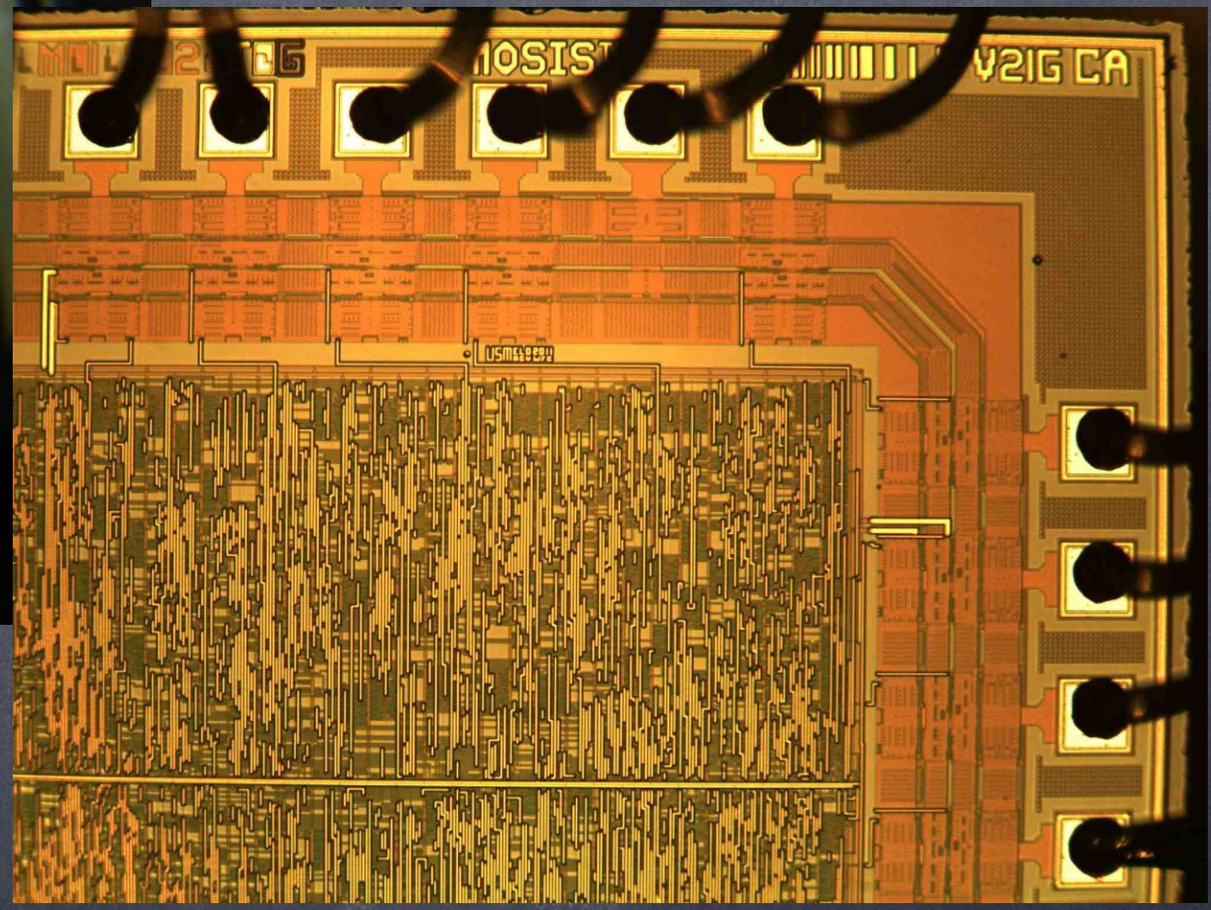
Challenge - Why VLSI?

- No other technology can do so much at so low cost and using such few energy.
  - Easier to move electrons than things. Check a mechanic counter part below.
  - And of course… because we CAN and is FUN!!

(http://www.computerhistory.org/babbage/overview/)

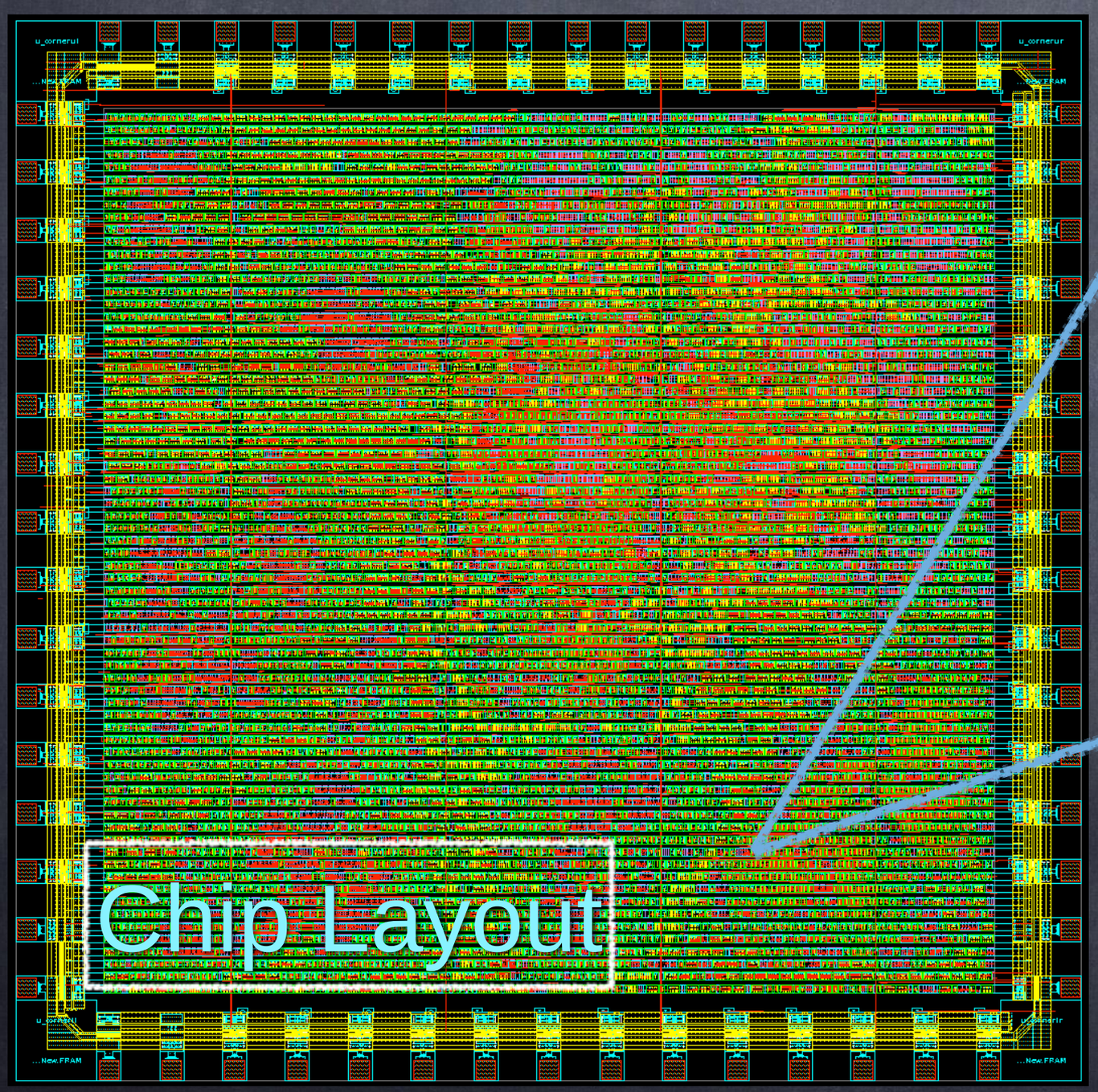


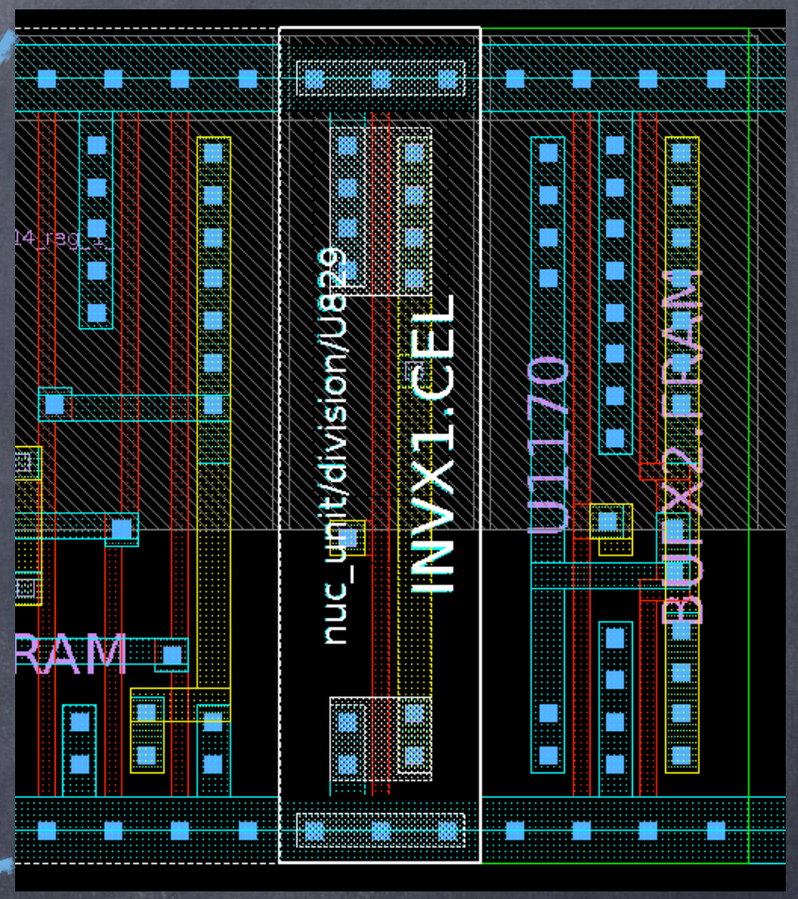
*Courtesy of UTSFM



A Chip designed in Chile!
(Fabricated for free through MOSIS)

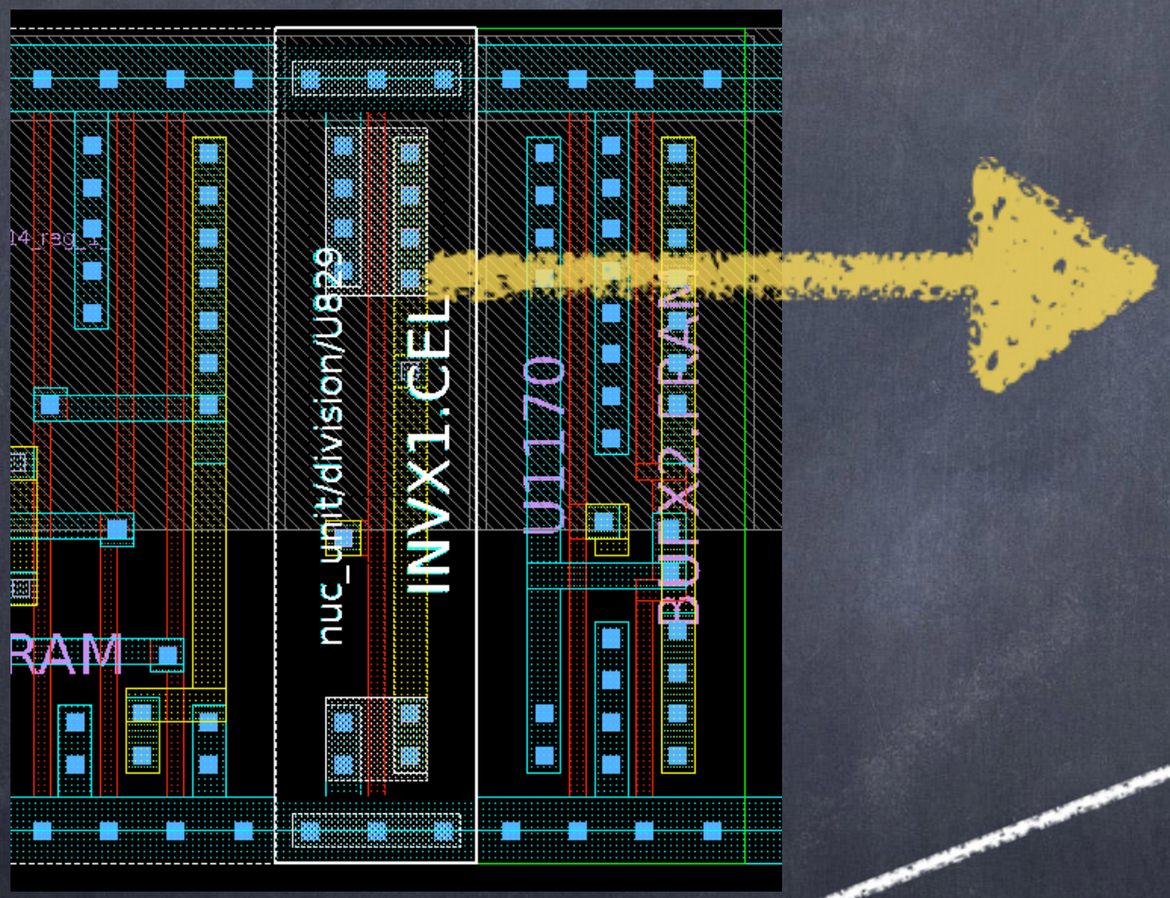
But how to get there? Let's look inside!

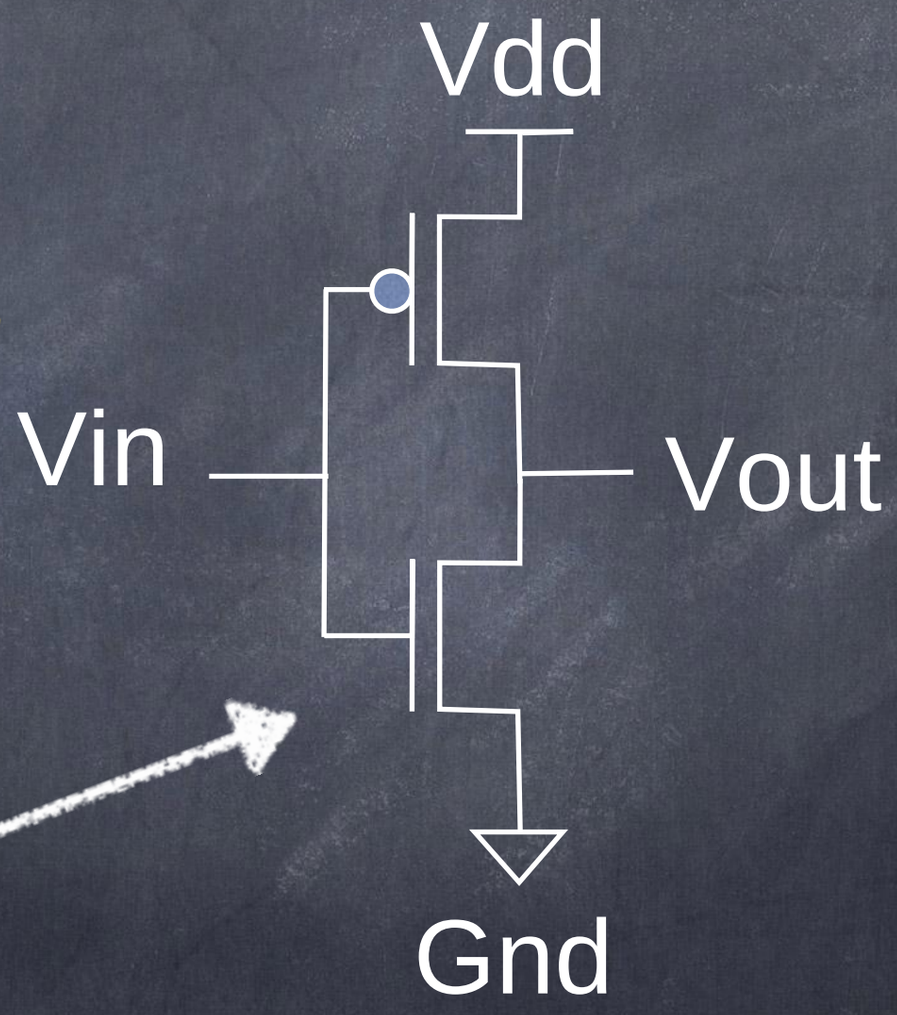




Zoom x1000

Rectangles that will be used to engrave circuits through lithography



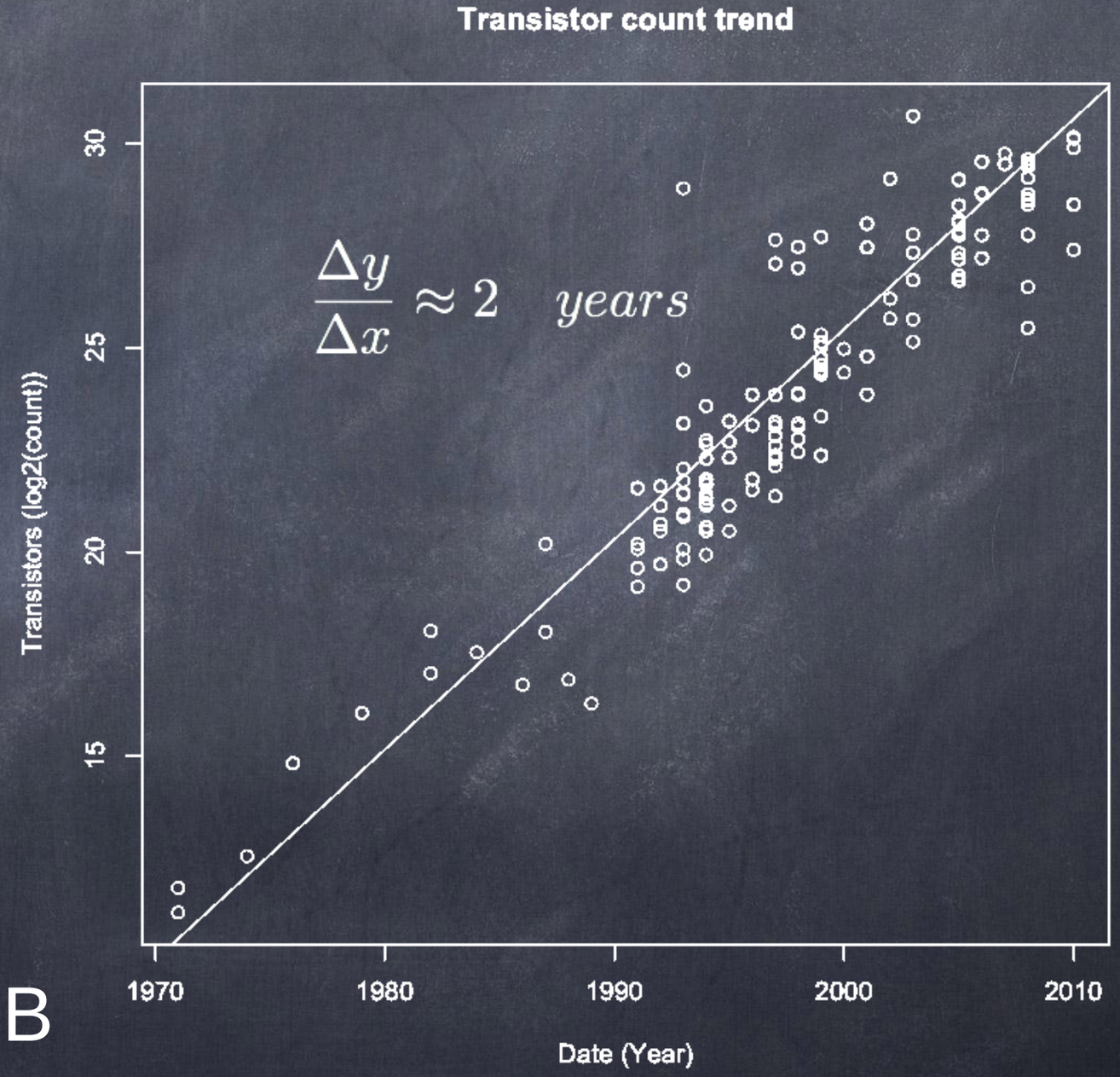


At the bottom what we have are TRANSITORS

Moore

”Cramming more components onto integrated circuits”,
Electronics Magazine, Aprils 19th, 1965

- Much smaller
- More transistors
- More features
- Much Cheaper
- More data?
  - ITRS
  - Stanford CPUDB



Scaling - Dennard

- Moore’s article was about promoting a new technology. On the other side Robert Dennard (IBM) relates parameter scaling on a transistor with its features.

- V scales -> V/a
- L scales -> L/a
- C scales -> C/a

Feature	Factor
More Transistors	a^2
Faster, delay	1/a
Less energy	1/a^2

“Design of Ion-Implanted MOSFET’s with Very Small Physical Dimensions”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-9, no. 5, pp. 256–268, October 1974.

Some difficulties

- Complexity
  - Verification
- Power
  - Heat
  - Supply
- Noise
  - Signal integrity, coupling
- Process Variation, Robustness,Reliability
  - Fabricate 1B transistors/chip and most chances are that some have defects
  - Soft errors, timing errors, defects,variations
- Non recurring engineering costs (NRE)
  - Design time,CAD tools
  - Mask costs(tooling needed to create IC)
  - NRE fabrication charges (fabs are VERY expensive)

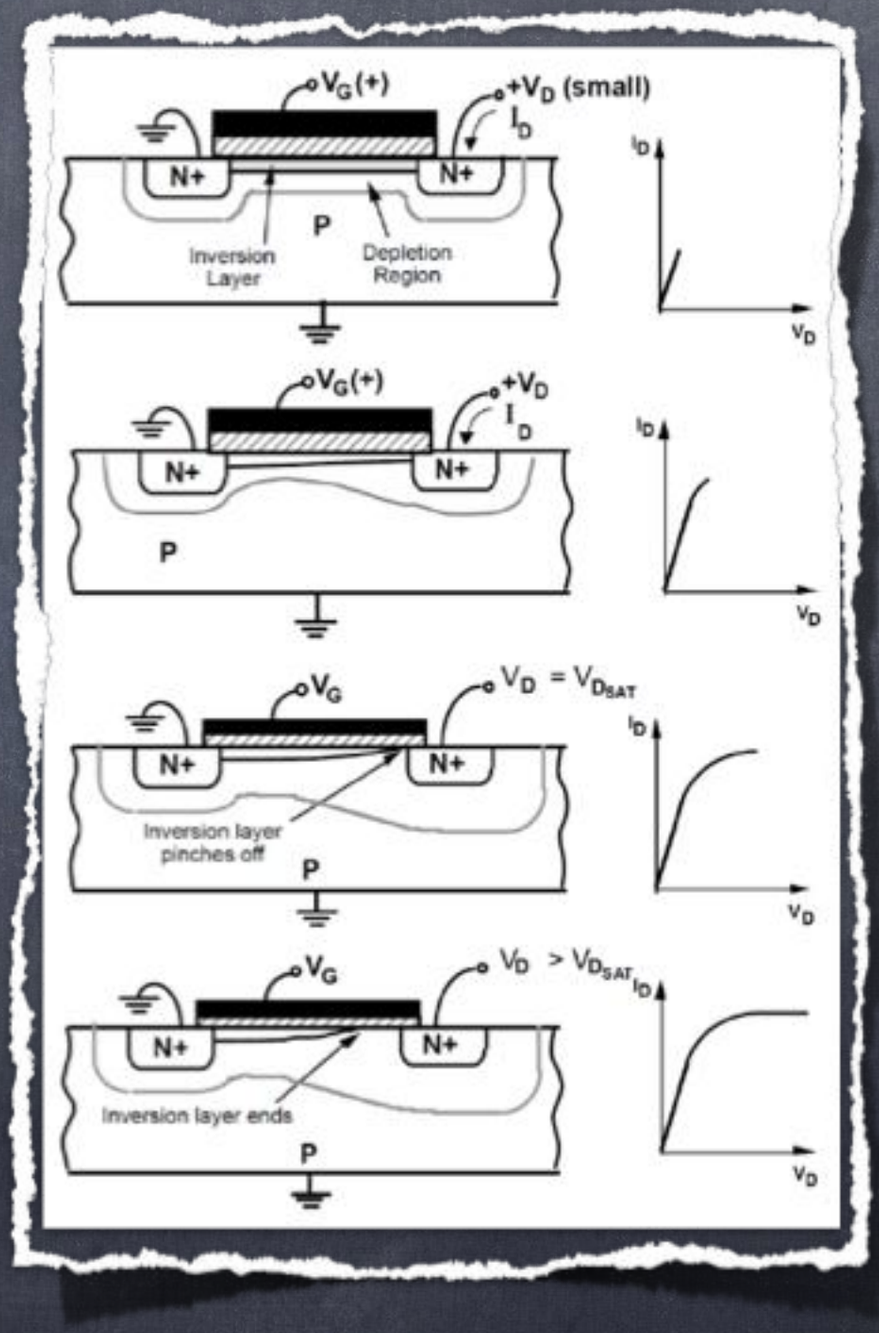
OK… motivated already?

Transistors

Transistor is a **MONSTER**

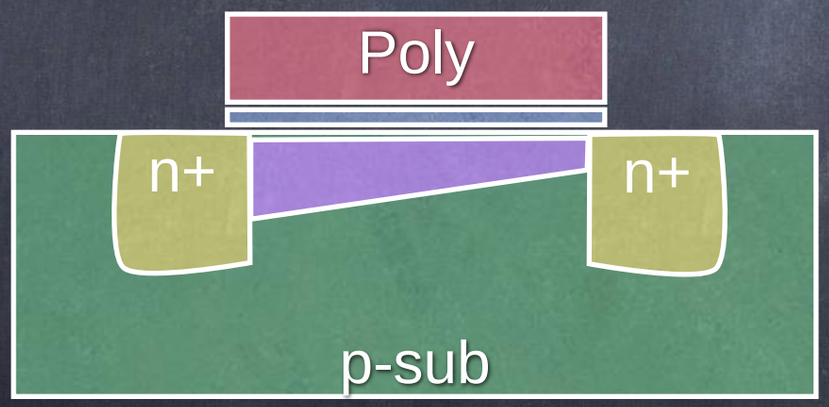
A non-linear monster in fact

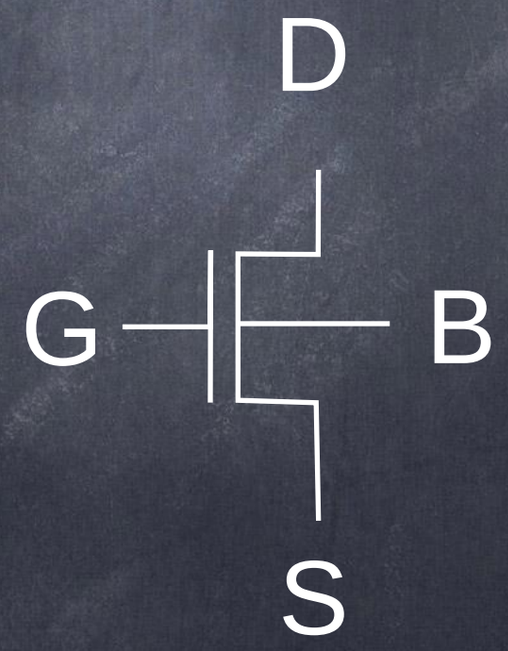
* From Prof. James Harris Notes (Stanford)



Transistor

- MOSFET
  - Controlled by 4 voltages: Vg, Vd, Vs, Vb.
  - Also by Vt, threshold voltage (set during fabrication)





Highly non linear models, must be abstracted to handle billion transistor designs.

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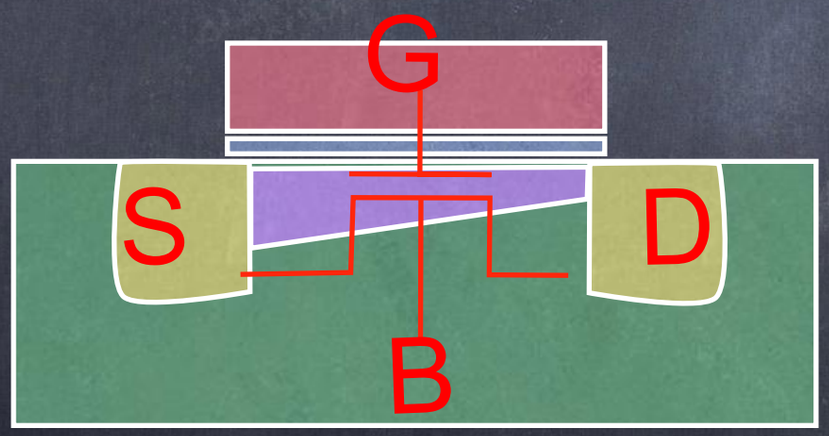
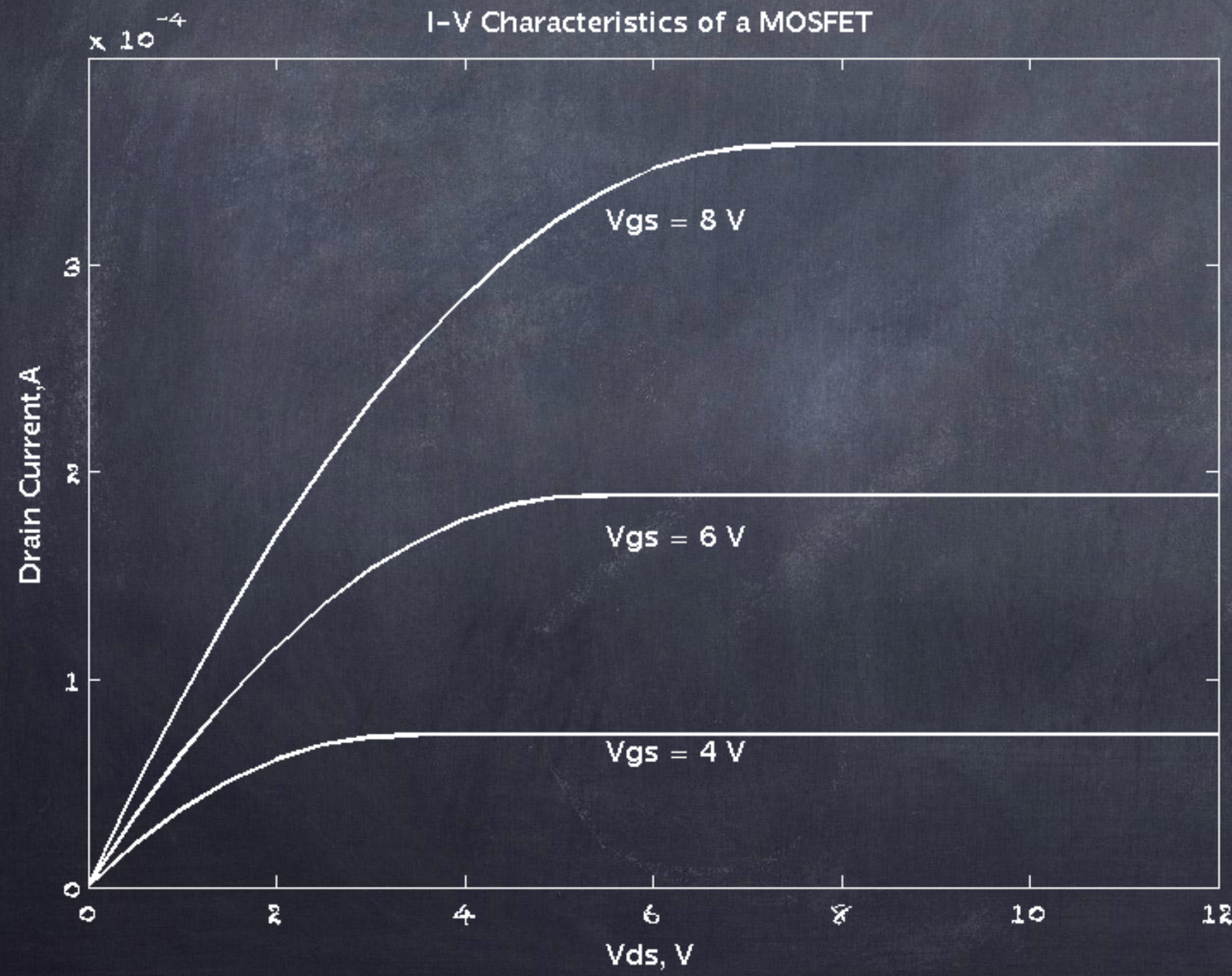


Highly non linear models, must be abstracted to handle billion transistor designs.

Transistor

- Often characterized by its current to voltage curve.



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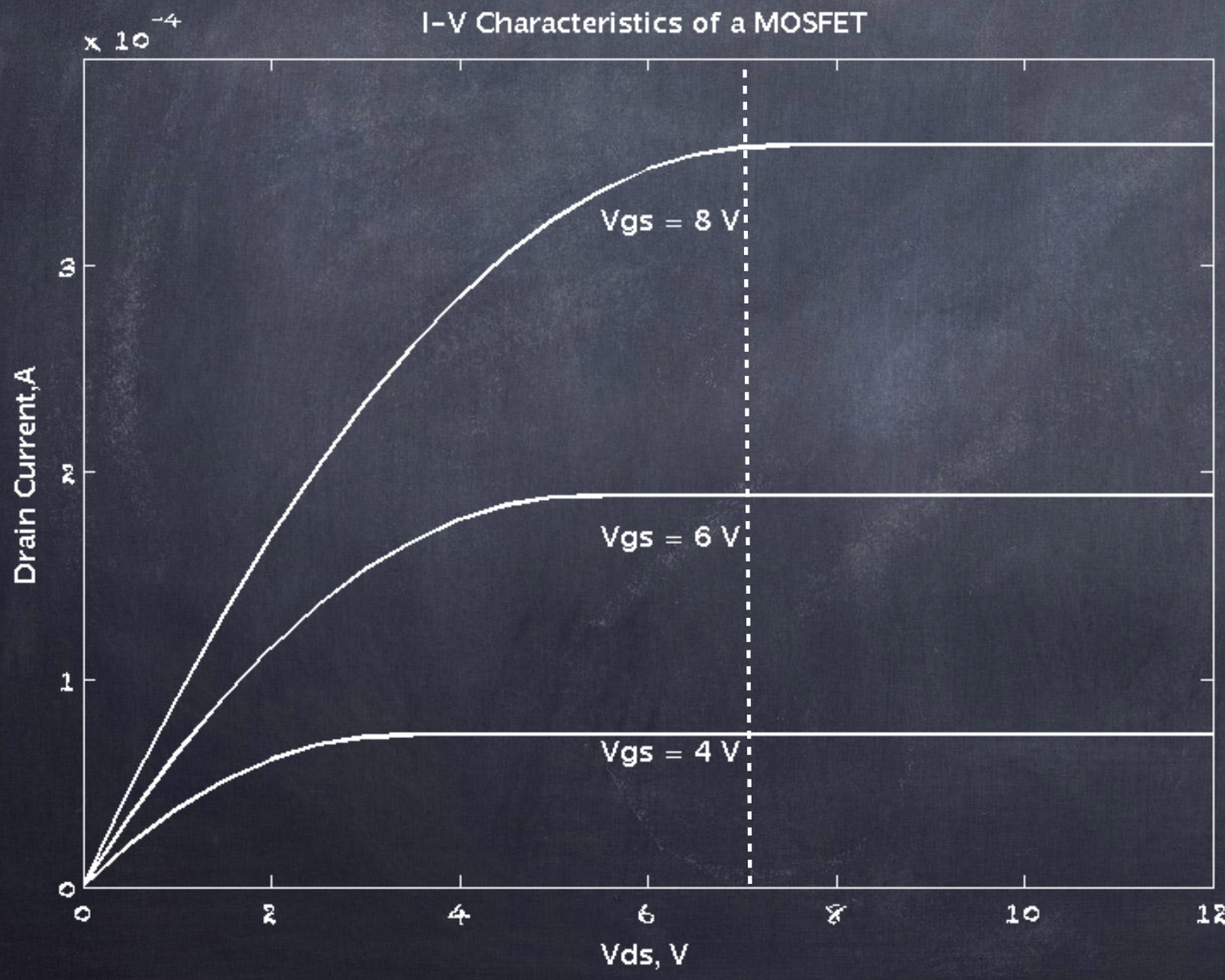


3 Operating zones

Ids= 0

Cutoff: Vgs < Vt

Ids = uCox*W/L*(Vov-Vds/2)*Vds

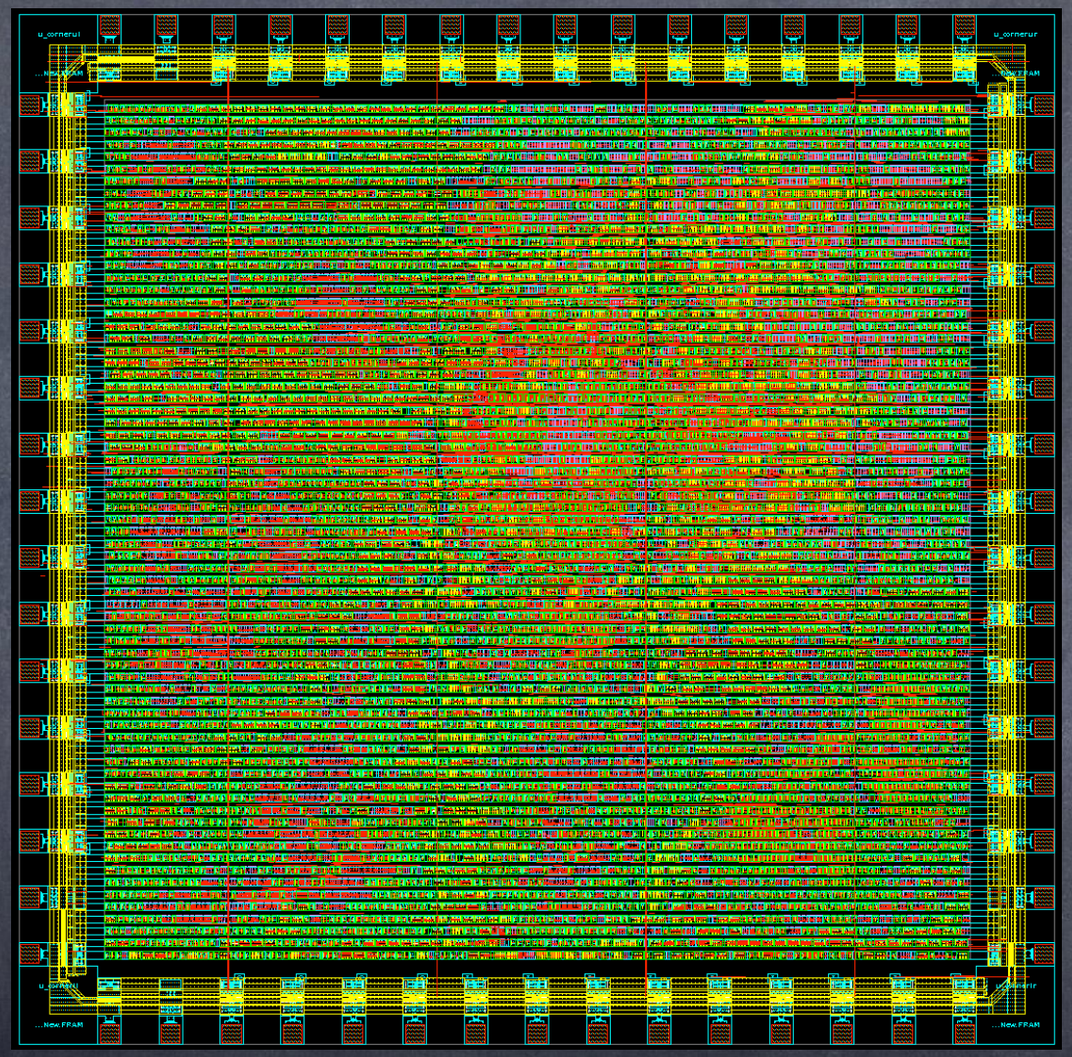
Linear: Vgs - Vt > Vds

Ids = 1/2*uCox*W/L*(Vov)^2

Saturation: Vgs - Vt < Vds

*Vov = Vgs - Vt

Transistors

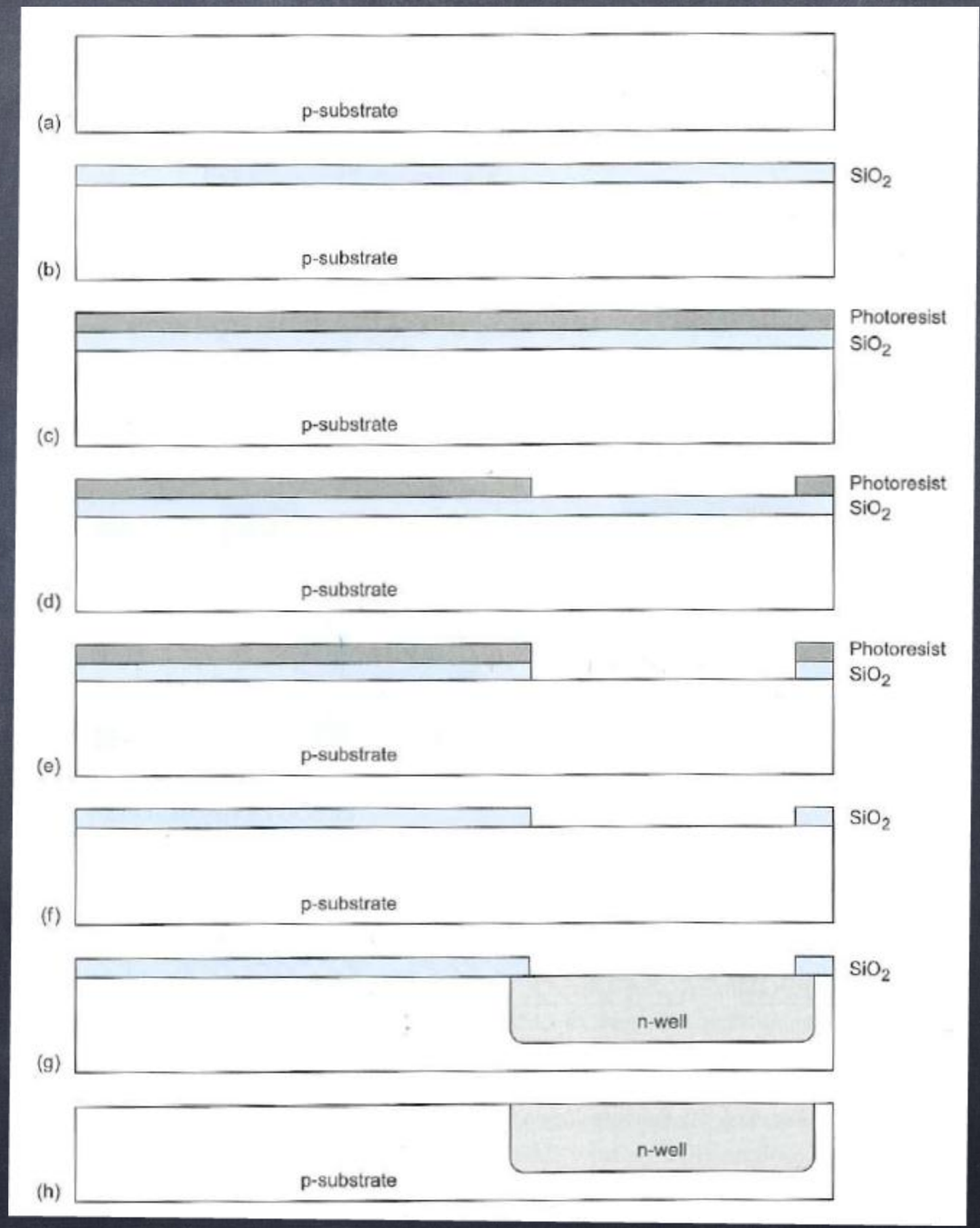


We Need SIMPLER models to handle Billion Transistor Design (More on this later)

Yeah sure, but where can I get one?

You print, they build

The picture shows how an n-type well is created over a p-type silicon wafer.



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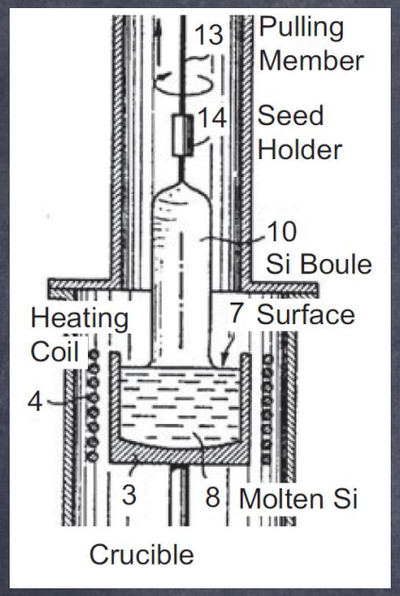
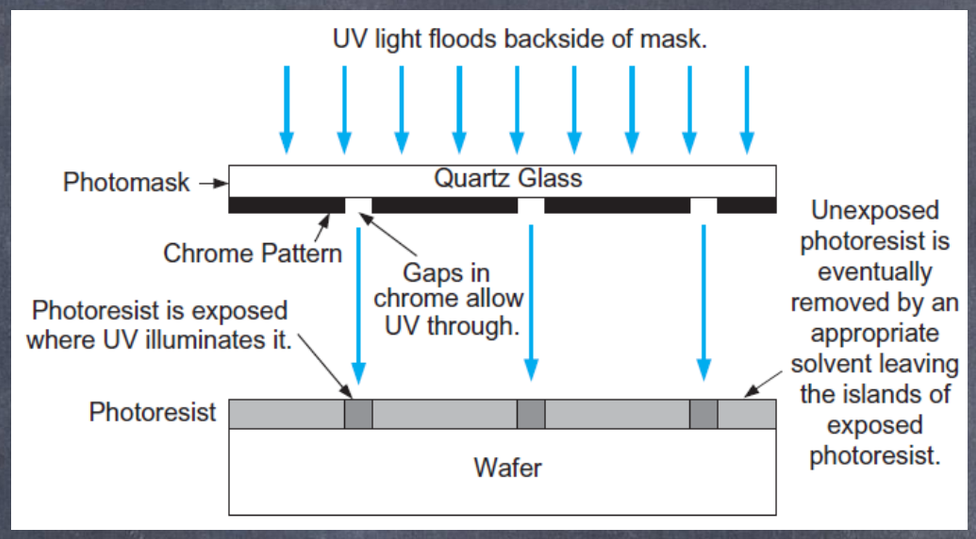
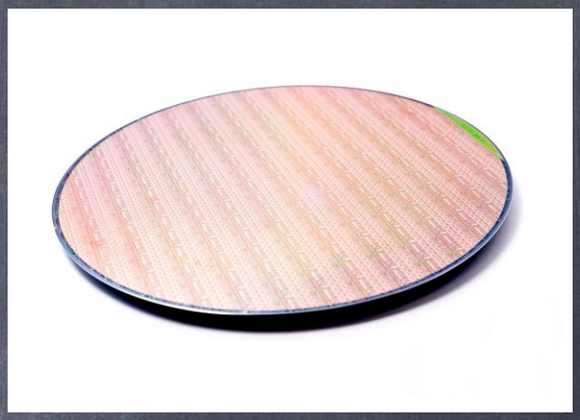
Circuits are printed in Wafers



Raw Wafer (ie: 100 P-type Si Wafer)



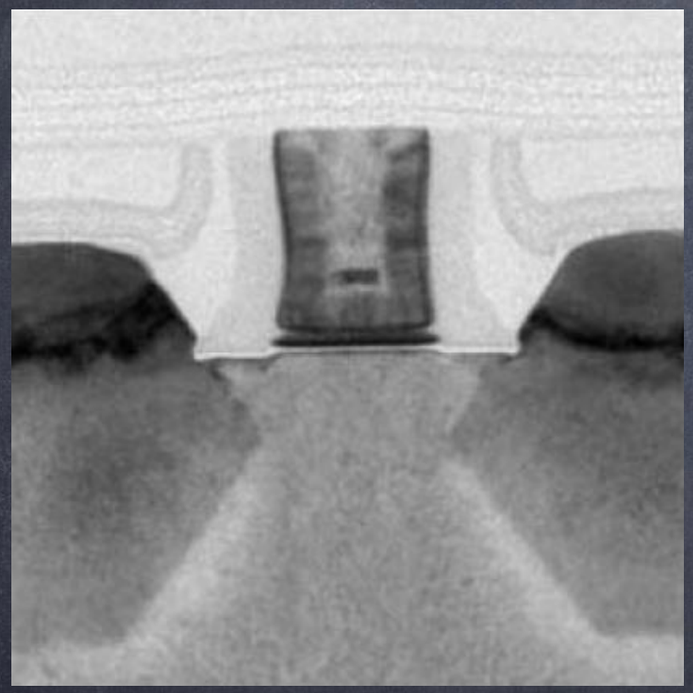
Photolitography



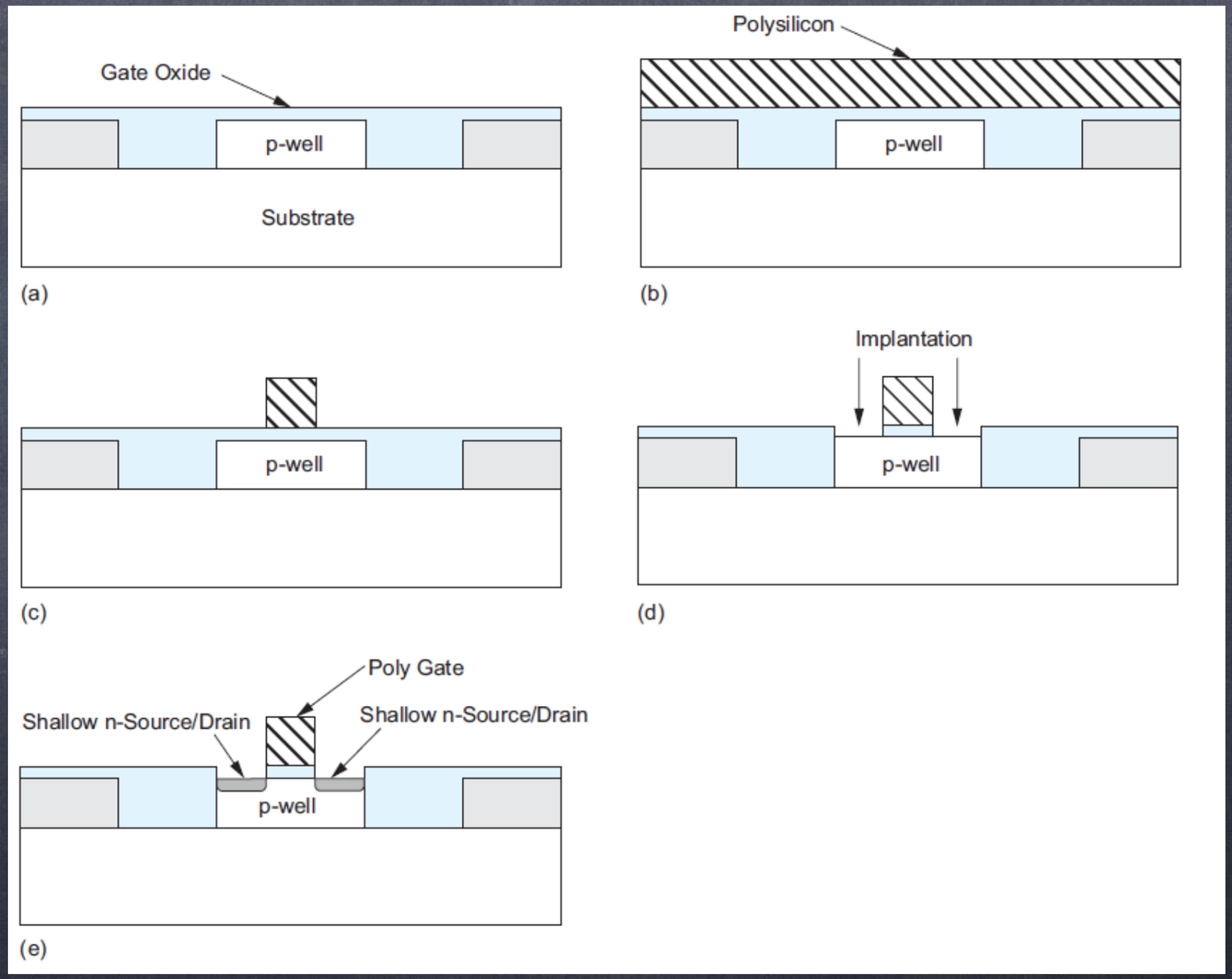
Wafer

Process

Quick look at fabrication



The Monster



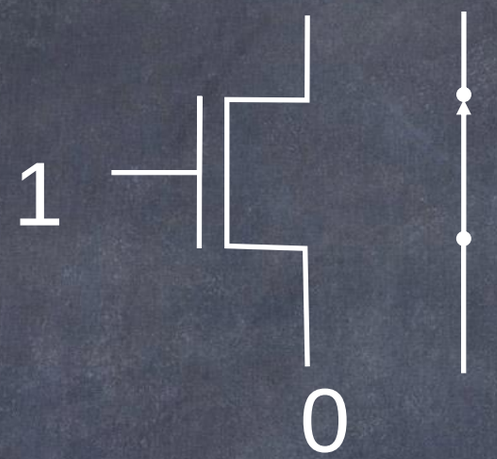
**Weste, Harris - CMOS VLSI Design 4th Edition*

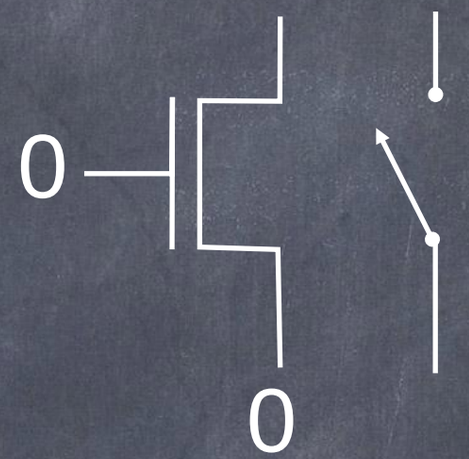
Digital Circuits

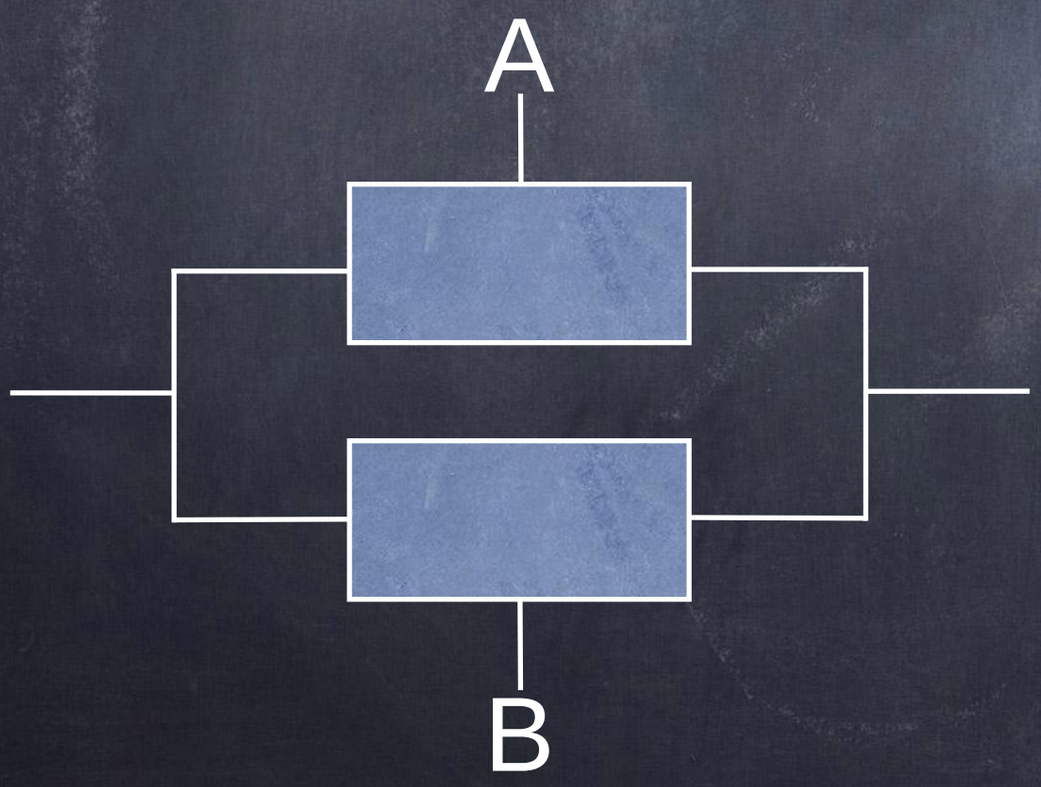
Digital Circuits

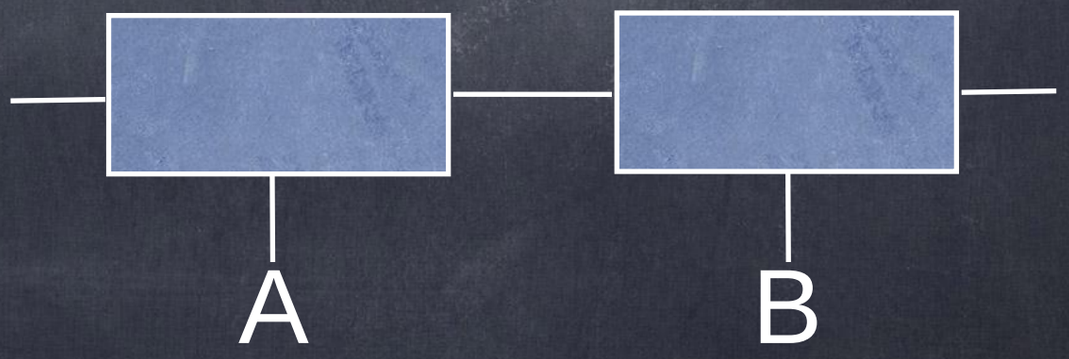
- Good CMOS gates are:
  - Uni-directional
  - Rail to rail
  - Noise attenuated
  - Defined by binary equations
  - Low dynamic power dissipation

Switch Networks

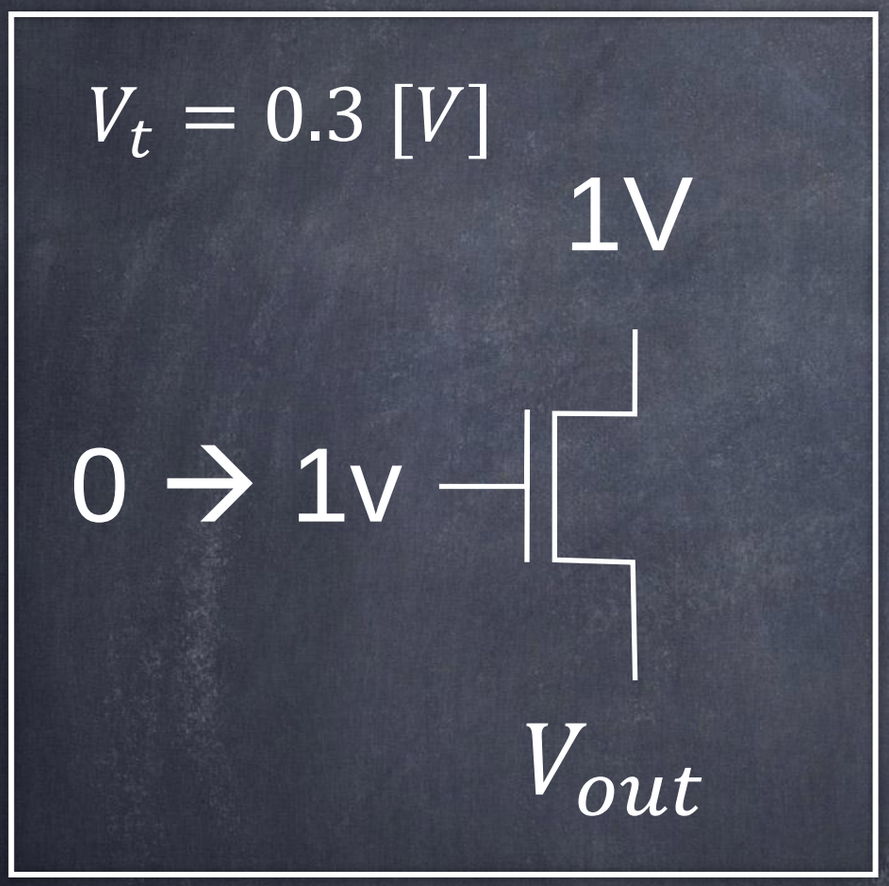








NMOS as Pass transistor



Conduction condition:
$V_g - V_s > V_t$

At $t = 0^-$

$V_{out} = 0\ [V]$
$V_g = 0\ [V]$
$V_g - V_s = 0 - 0 = 0 < V_t = 0.3\ [V]$

⇒ No conduction

At $t = 0^+$

$V_{out} = 0\ [V]$
$V_g = 1\ [V]$
$V_g - V_s = 1 - 0 = 1 > V_t = 0.3\ [V]$

⇒ Transistor conducts (V_{out} rises)

Conduction stops at
$V_g - V_s = V_t \Leftrightarrow V_s = V_g - V_t = 1 - 0.3 = 0.7\ [V]$

PMOS as Pass transistor

$V_t = -0.3\ [V]$

Conduction condition:
$V_g - V_s < V_t$

At $t = 0^-$

$V_{out} = 1\ [V]$
$V_g = 1\ [V]$
$V_g - V_s = 1 - 1 = 0 > V_t = -0.3\ [V]$

⇒ No conduction

At $t = 0^+$

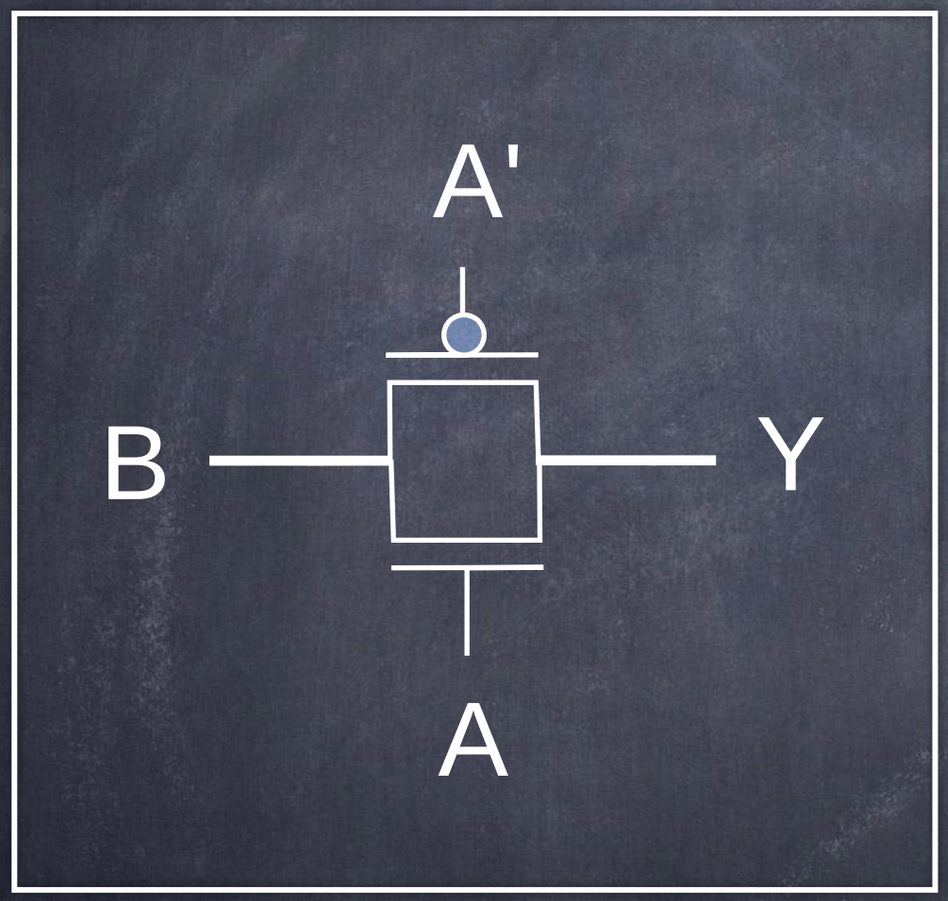
$V_{out} = 1\ [V]$
$V_g = 0\ [V]$
$V_g - V_s = 0 - 1 = -1 < V_t = -0.3\ [V]$

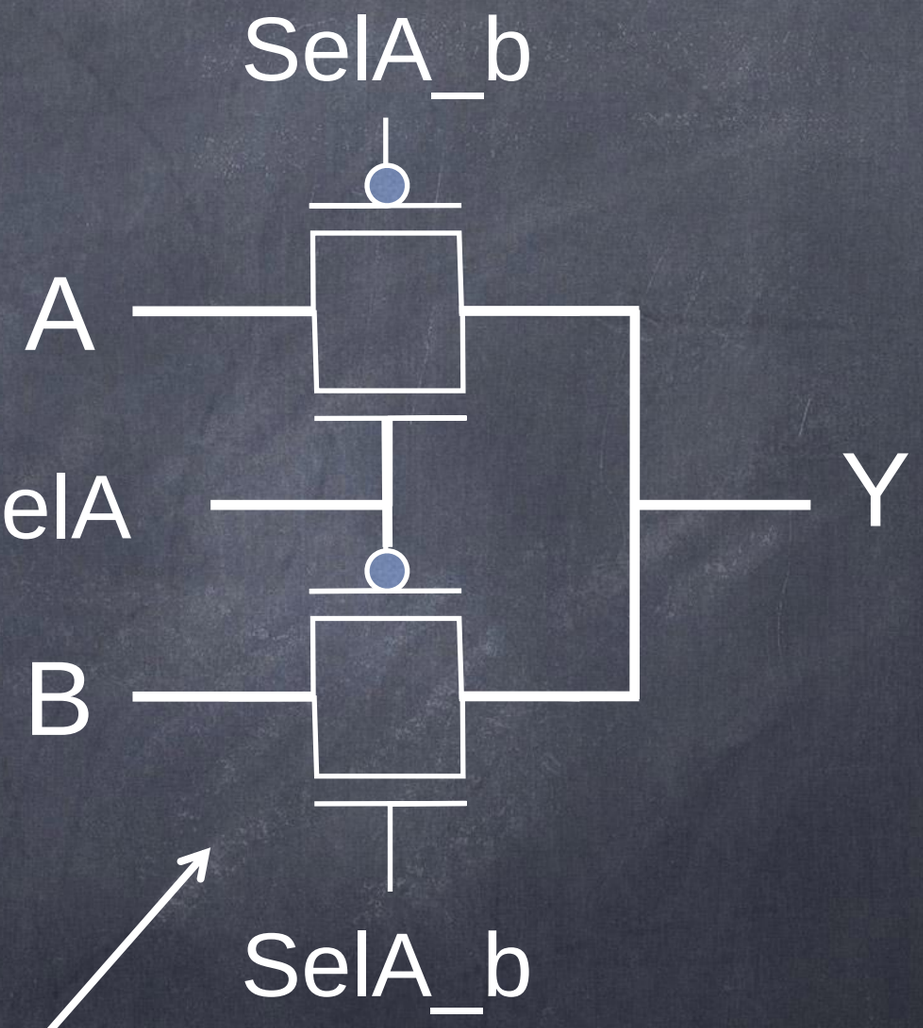
⇒ Transistor conducts (V_{out} decreases)

Conduction stops at

$V_g - V_s = V_t \Leftrightarrow V_s = V_g - V_t = 0 - (-0.3)$
$= 0.3\ [V]$

Pass Gate

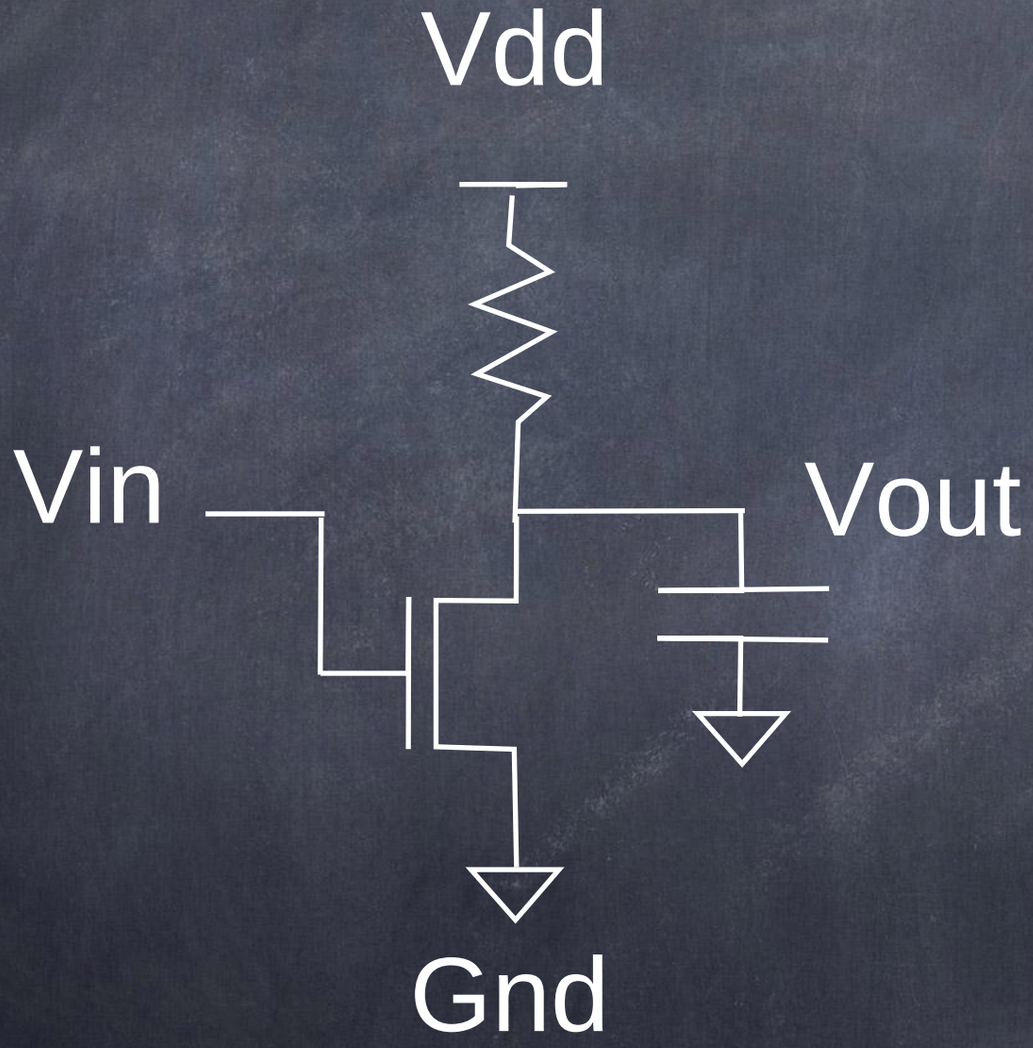




Is this a good digital circuit?

- Still it could be handy

NMOS logic



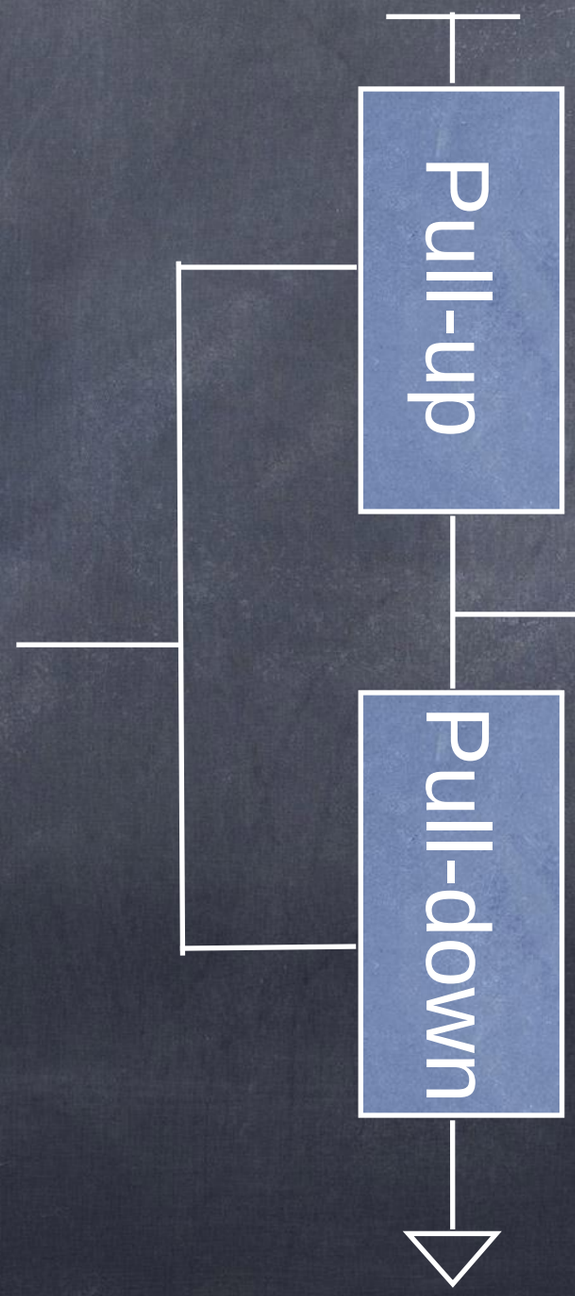
What is the value of Vout when Vin = Vdd ?

When current will stop flowing?

Which states disipate energy?

CMOS Gates
Pull-up / Pull-down networks

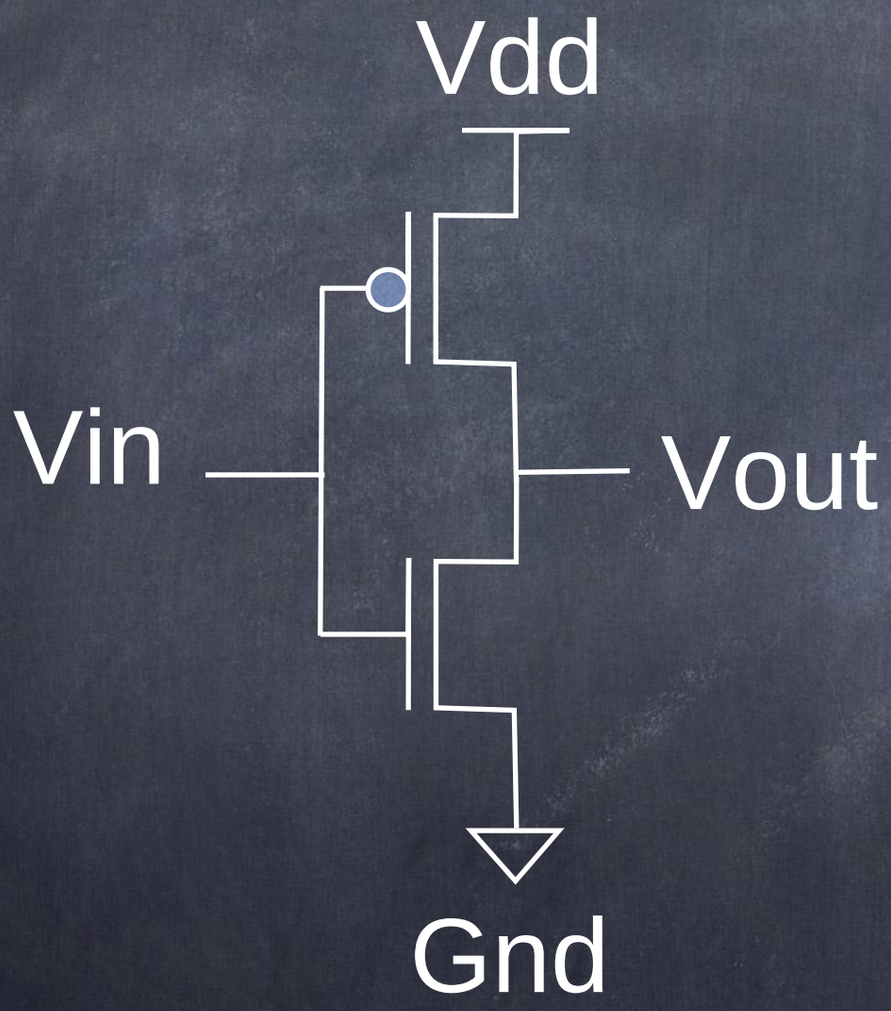
- CMOS: Complementary MOS
- No floating wires, outputs connects to either Vdd or Gnd.
- Vdd & Gnd are never shorted together.

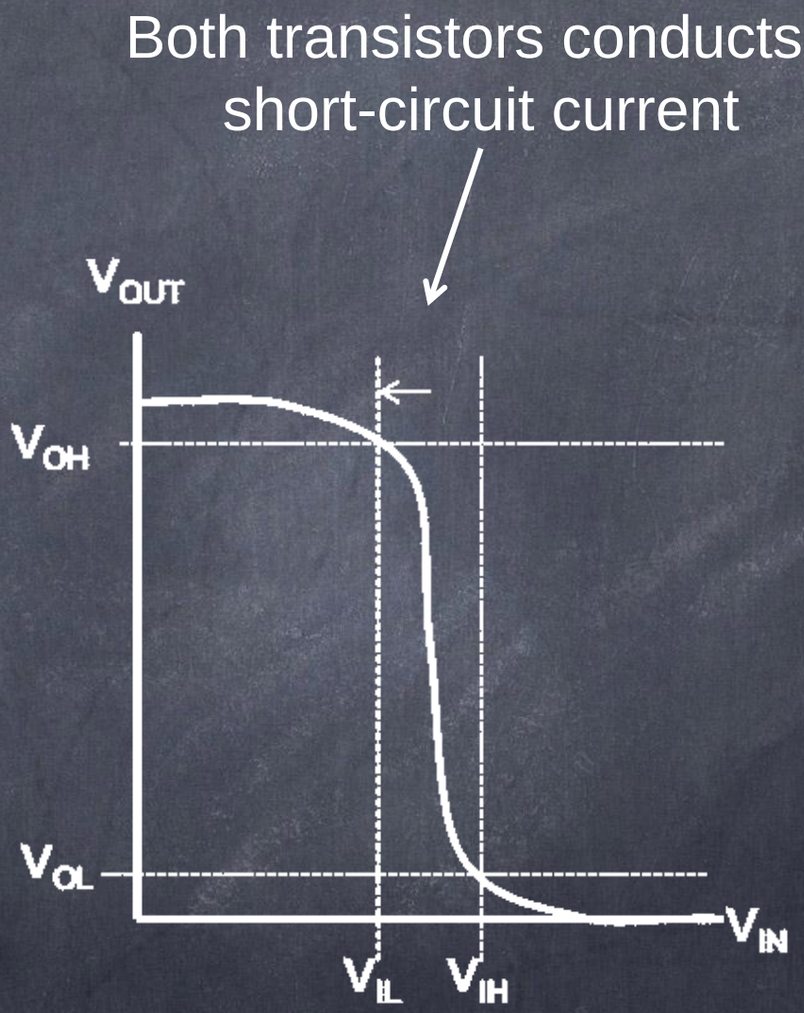


pMOS

nMOS

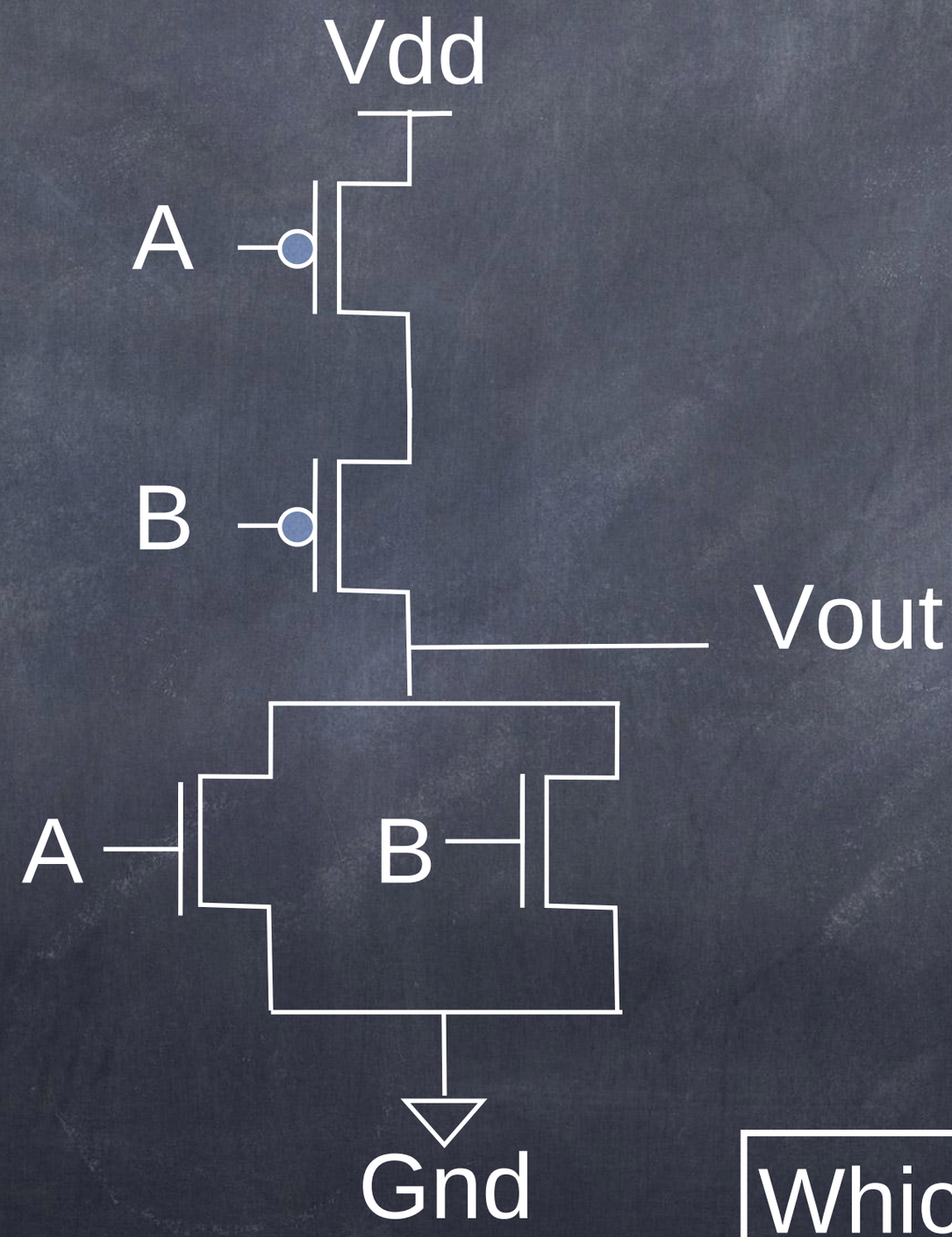
The Inverter





Identify regions? Which MOS, Which region?

More Gates



Which gate is this?

More Gates

NOR gate:

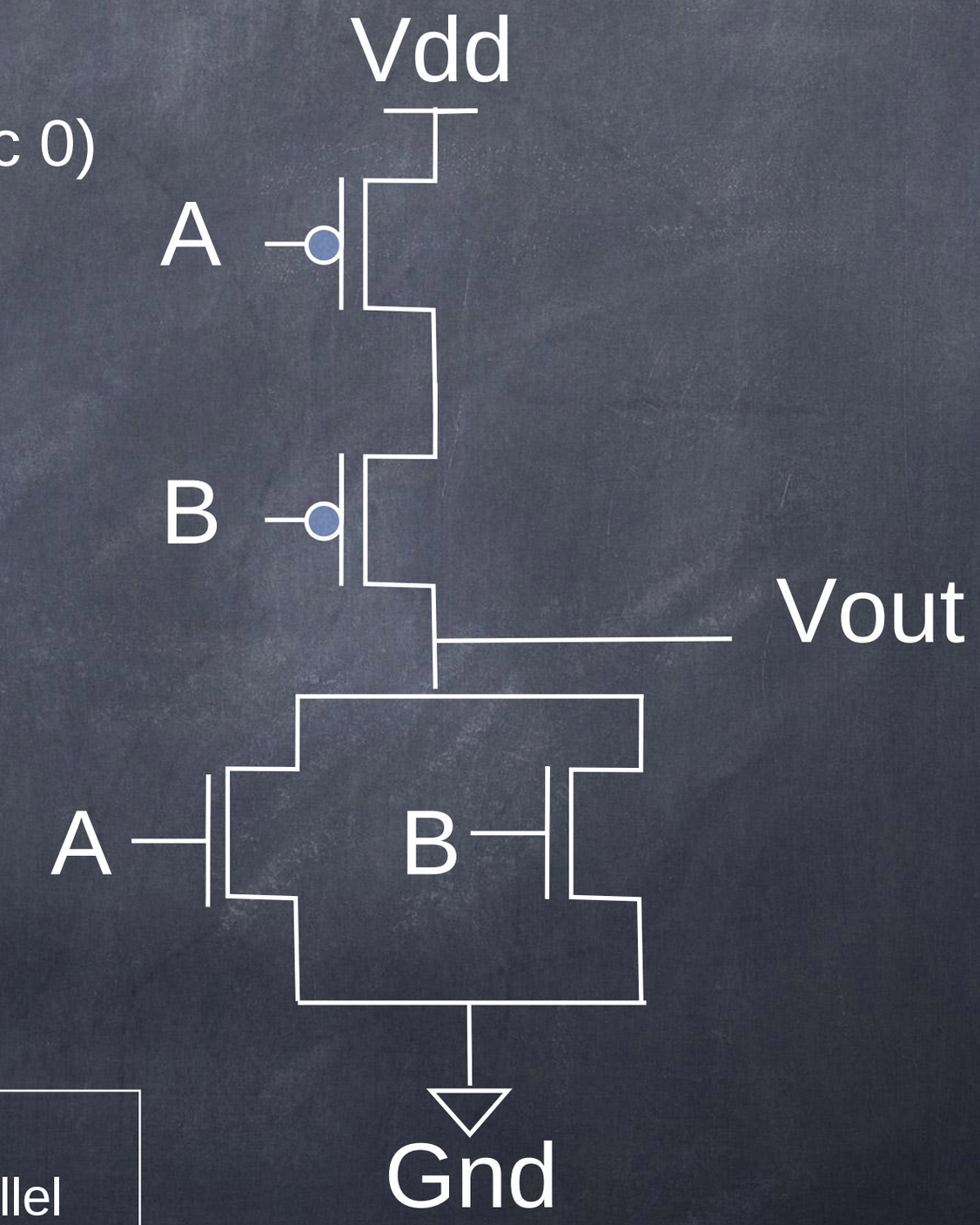
- OR branch discharges to ground (logic 0)
- Dual branch charges to Vdd (logic 1)

Dual:

- The complementary branch can be obtained from De Morgan's law

$$(A+B)' = A'*B'$$

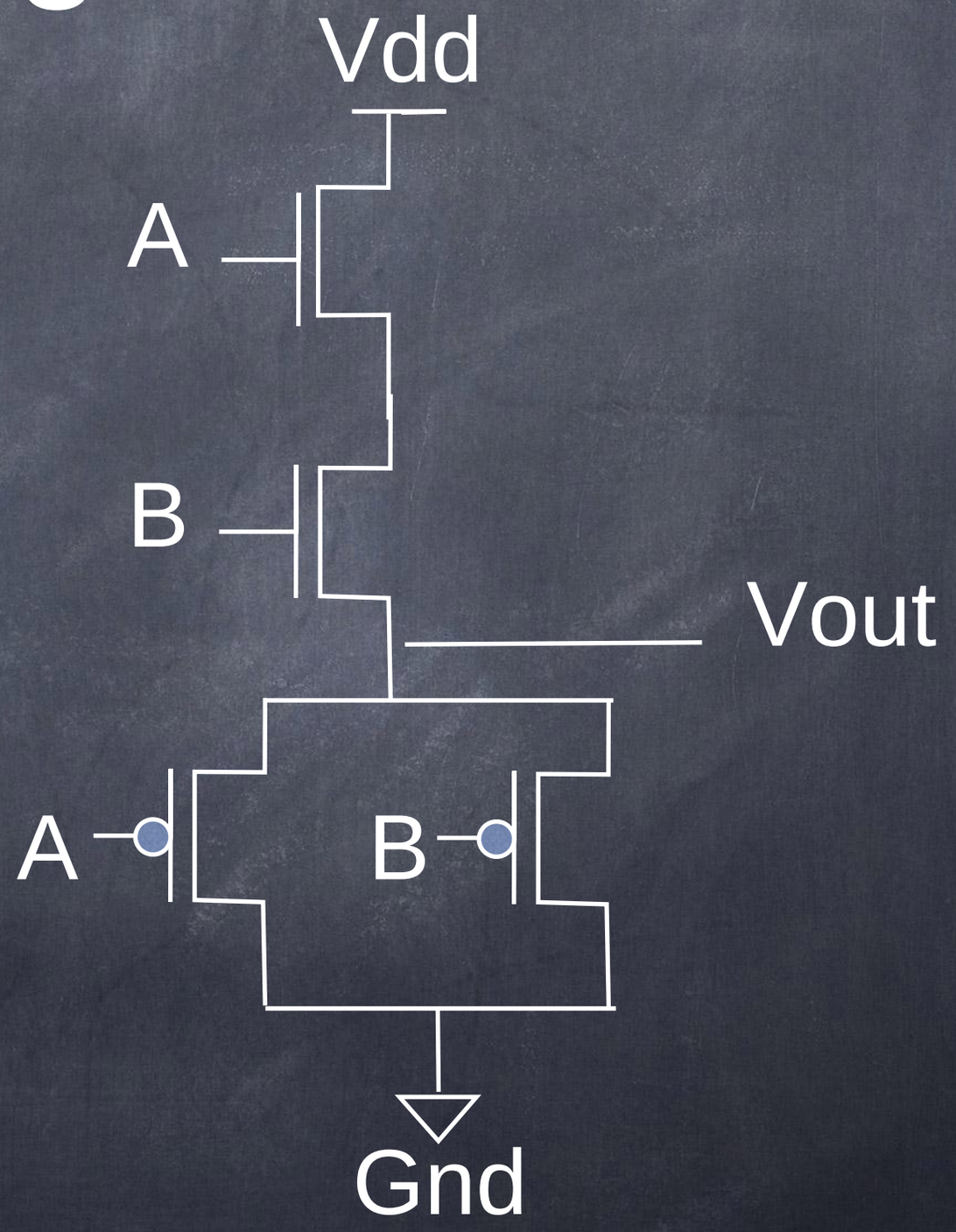
$$(A*B)' = A'+B'$$



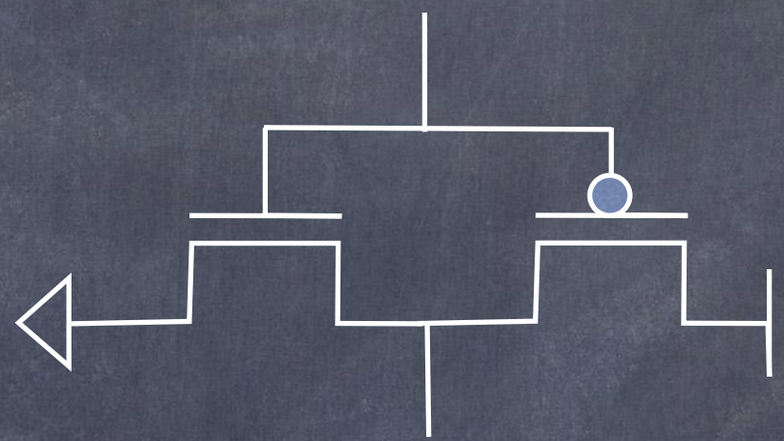
Note that:
OR operations are implemented by switches in parallel
AND operations are implemented by switches in series

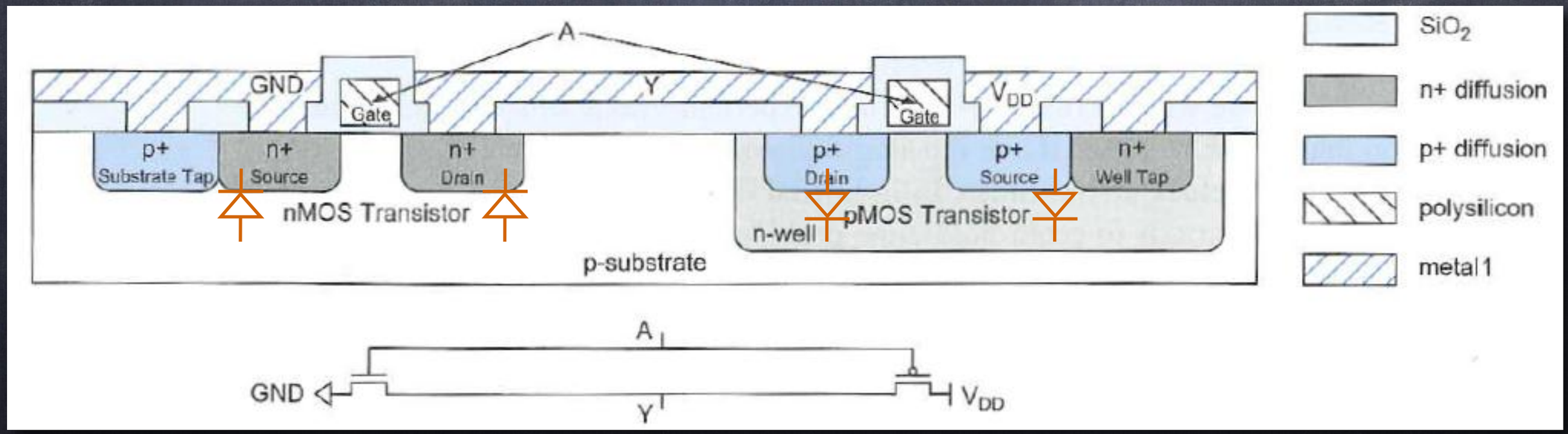
Direct Logic?

- What is the problem with this gate?



Gate Layout





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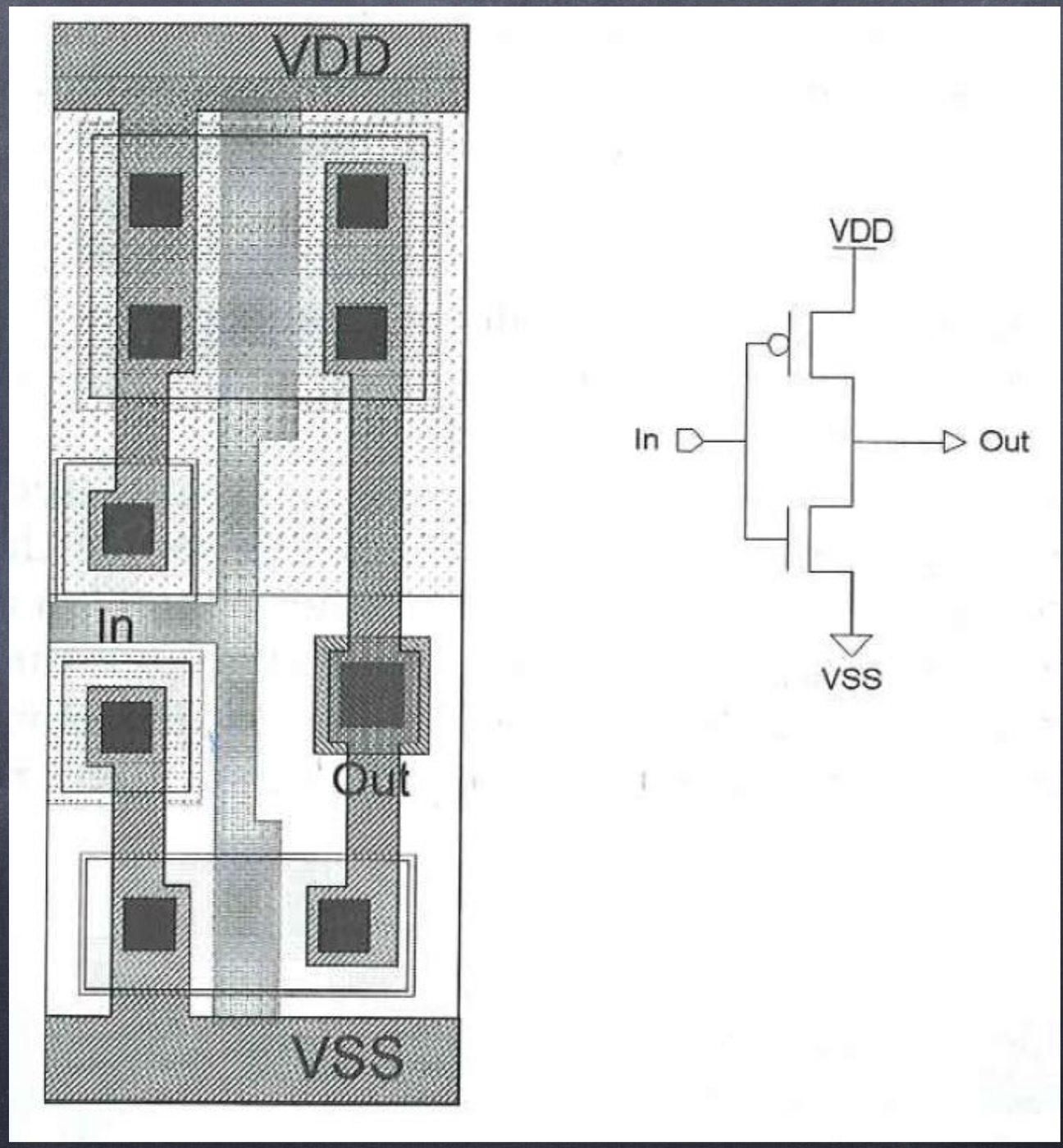
Standard Cell

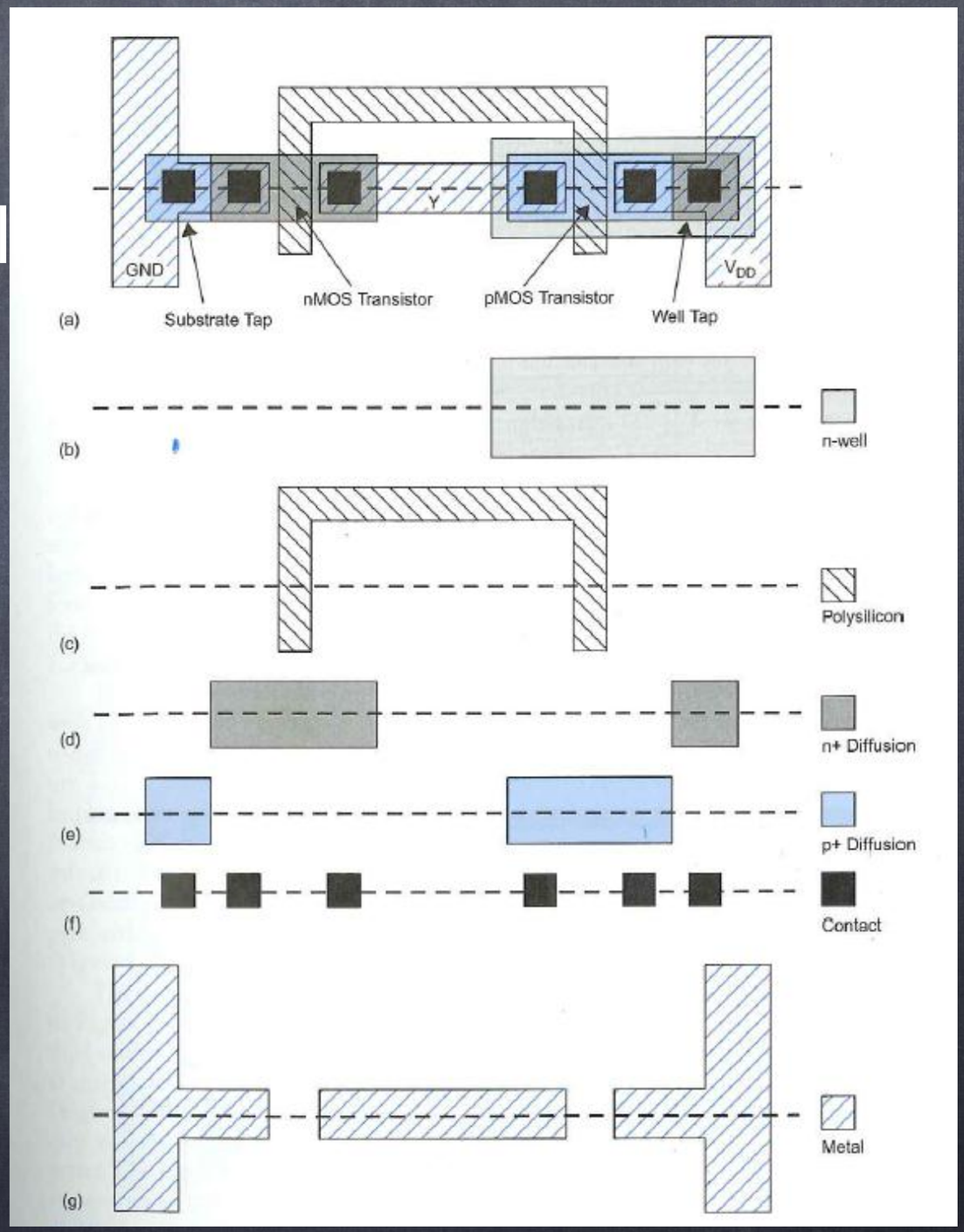
- A contained circuit that can be handled by tools.
- It has a standard height which ease placement on the chip area
- Associated with model that characterizes its physical and logical properties.



Gate Layout (Standard Cell)

- We need to comunicate a design intent without handling all fabrication details.
- Draw layers, simple forms that contain the information required to build our circuits.
- Foundry provides Design Rules (DRC) to guarantee that whats delivered is feasible to build.

http://www.mosis.com/files/scmos/scmos.pdf



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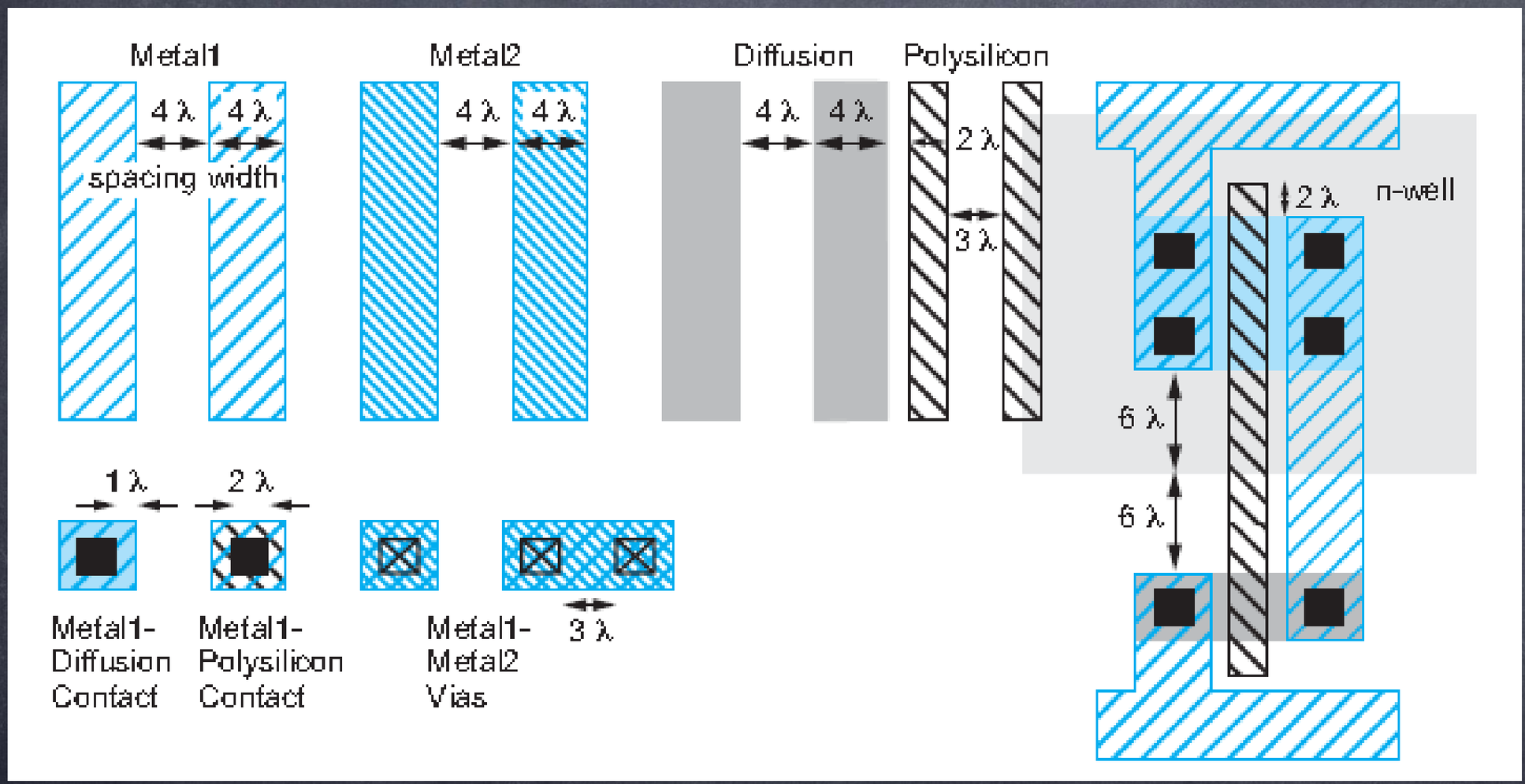
Rules



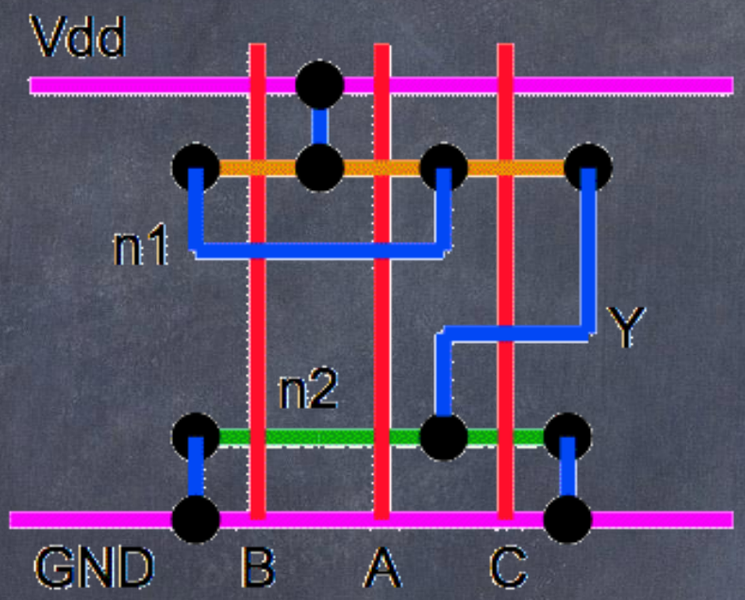
Rules for MOSIS process

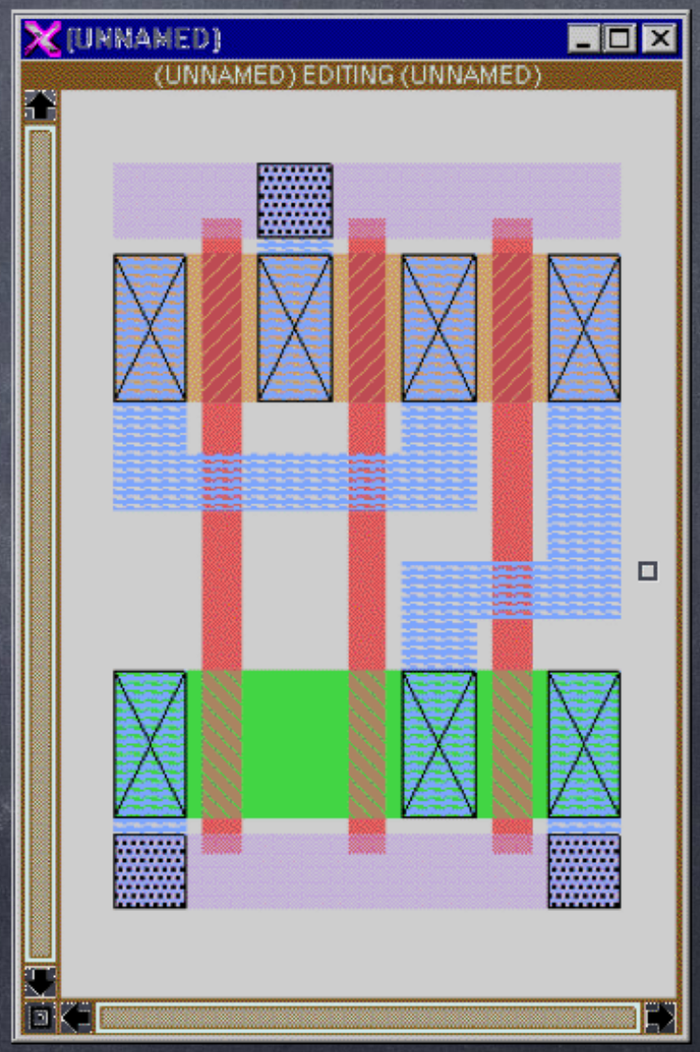
Note that they are based on a single parameter

λ represents half of the minimum transistor channel length

(or in other words, half of minimum polysilicon wire width)

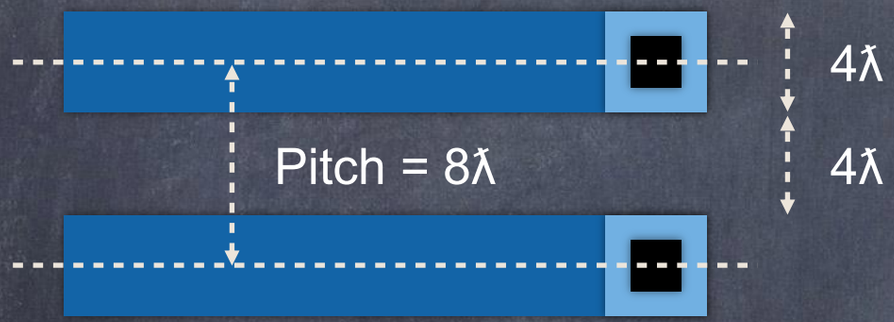
Stick Diagrams (MacGyver's clip)

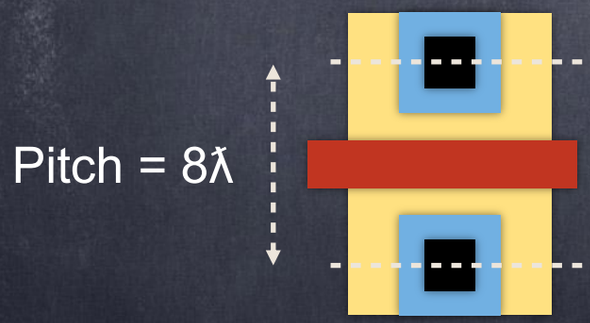


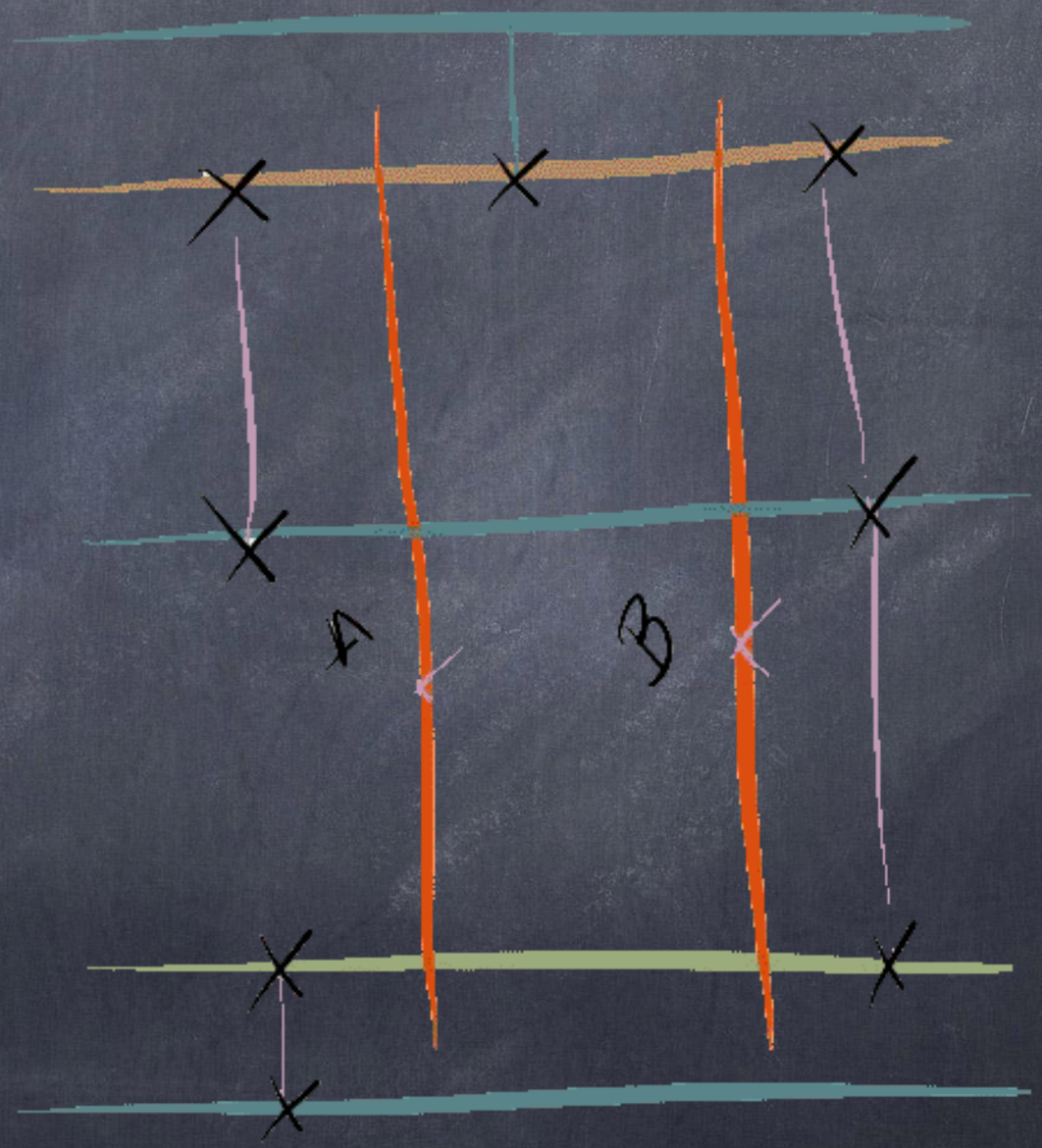


- Abstract version of layout
- Workout topology without the details

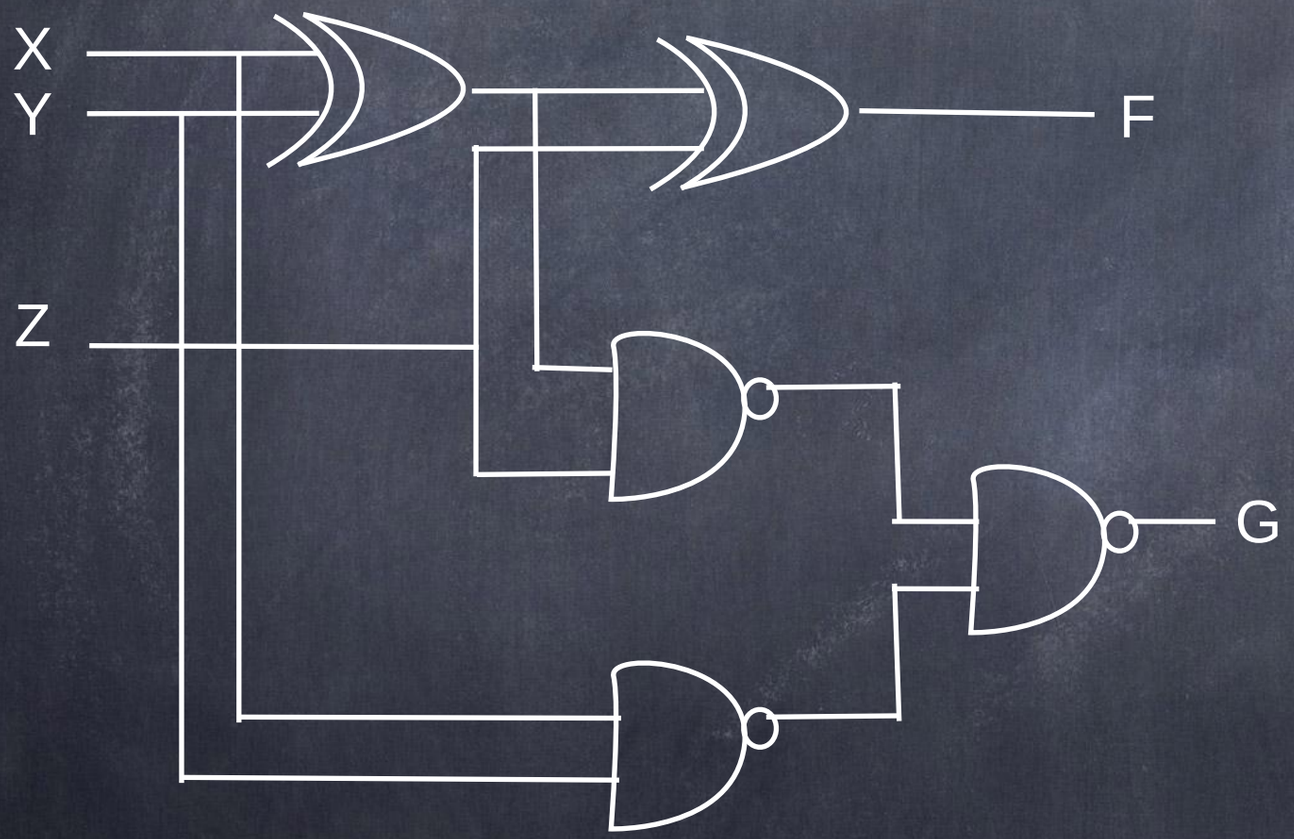
Quick area estimation

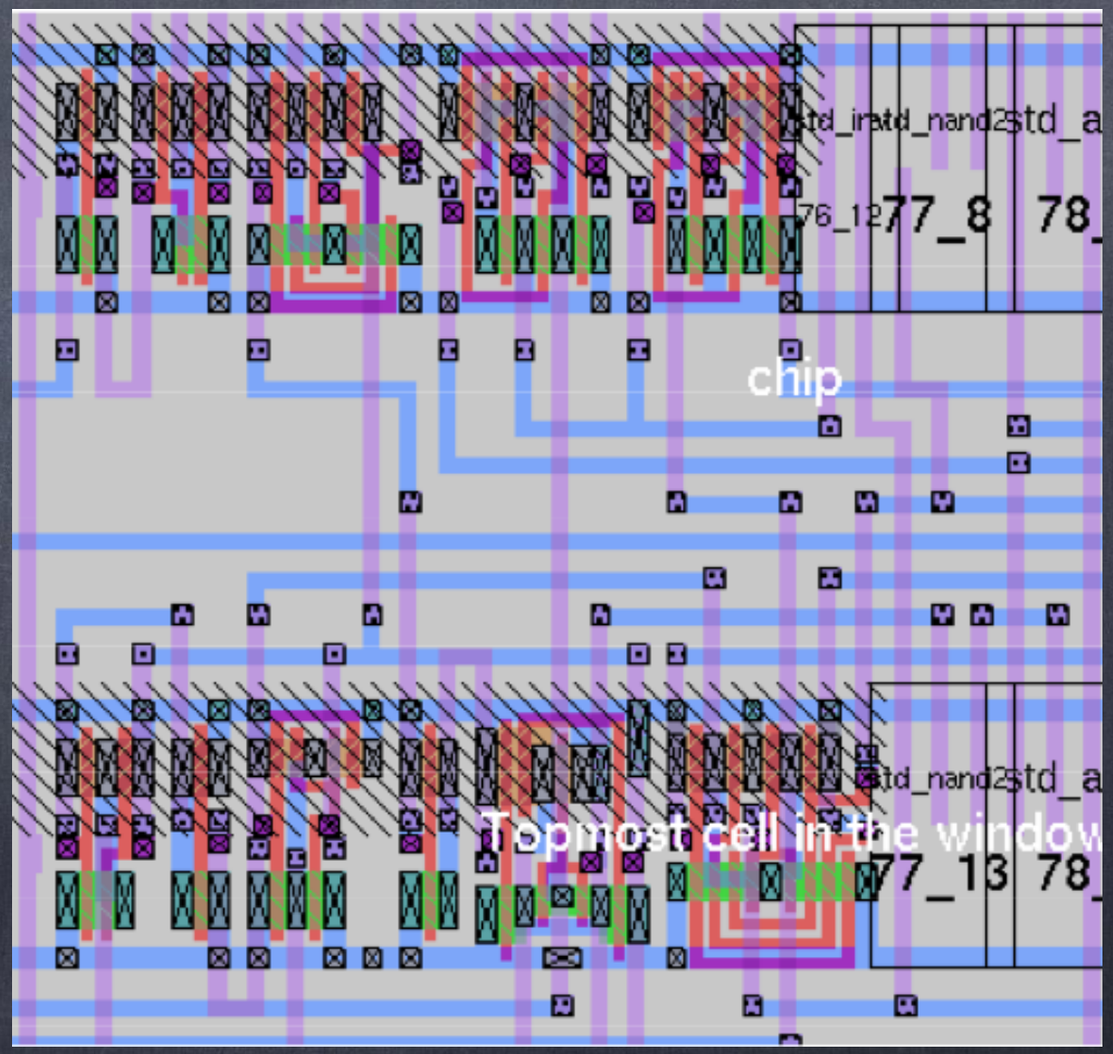






Place & Route



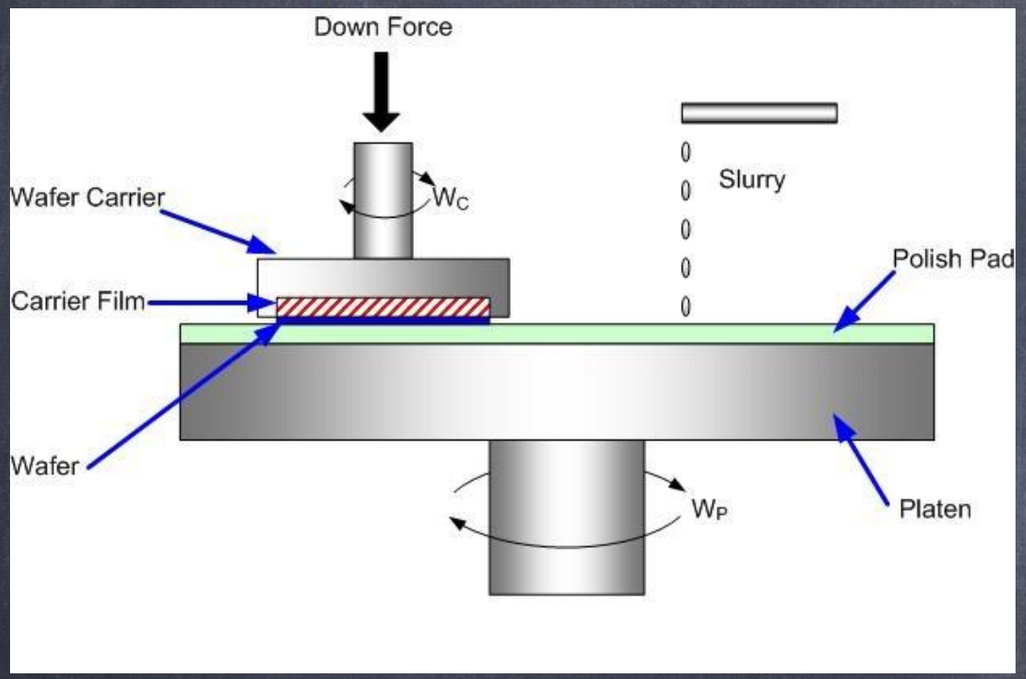


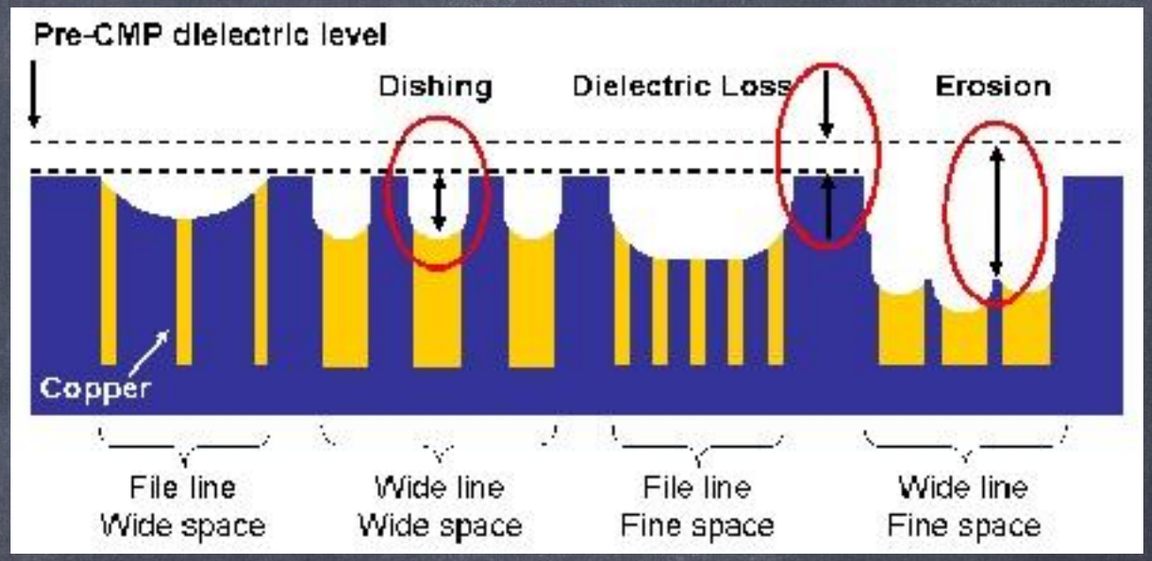
More subtleties of Manufacture

- Metal density
- Metal Slotting
- Antenna Rules
- Optical proximity correction (<180nm)
- Phase shifting masks
- Double Patterning (<45nm)

Metal Density

Chemical Mechannical Polishing



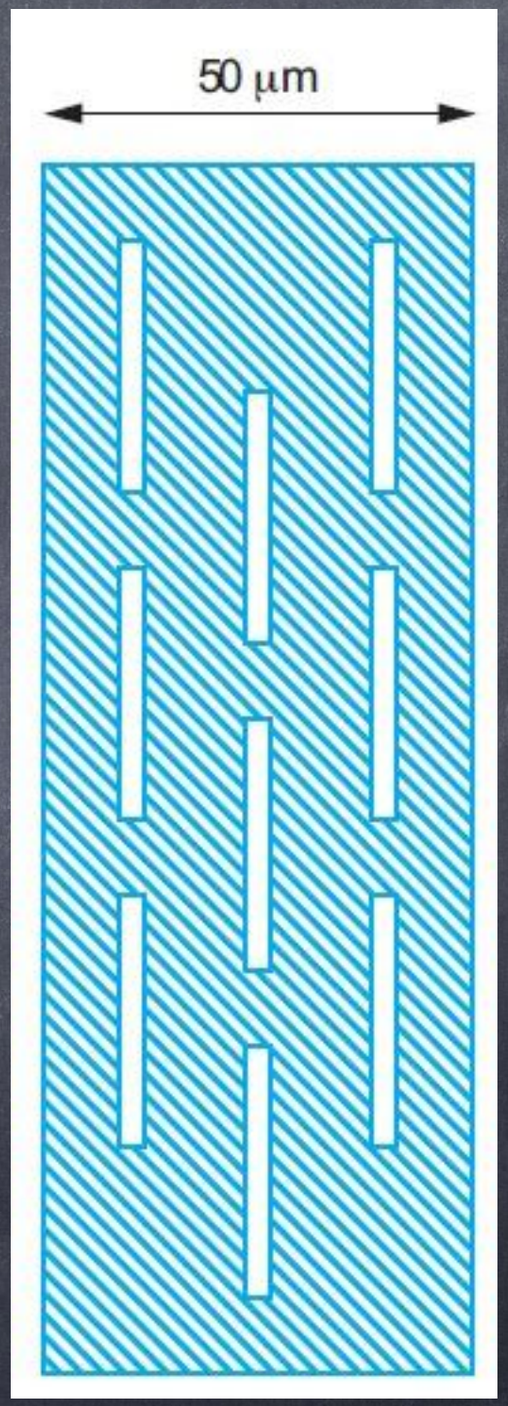


Copper is more sensitive to polishing

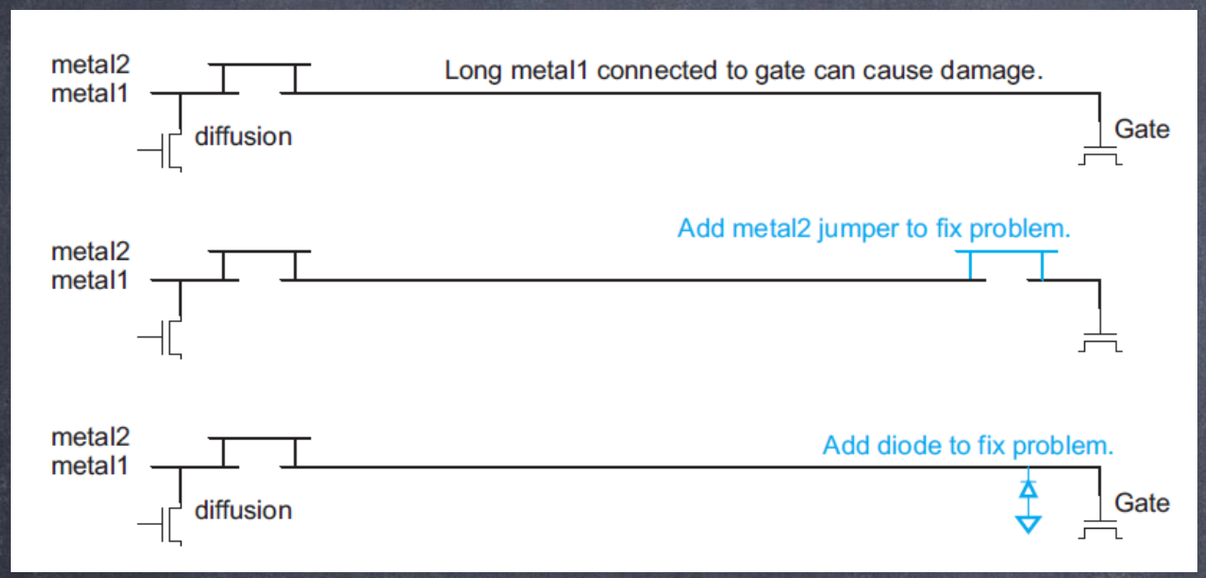
This can also be an issue during Etching.
Bottom line: each layer has a density target (max & min)

Metal Slotting

In some process, slots should be introduced for wide wires in order to relief stress and reduce risk of electromigration



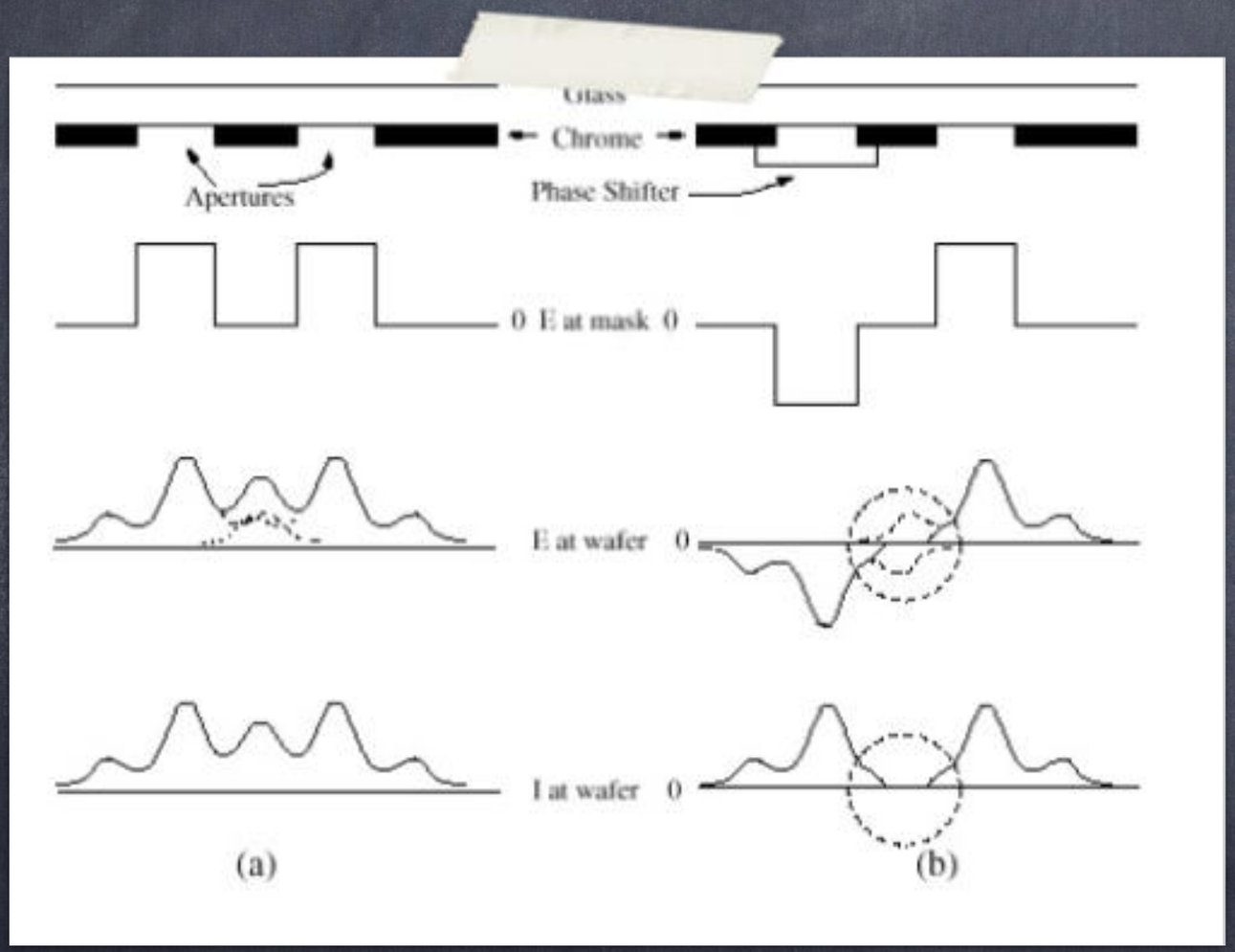
Process-Induced Damage Antenna Rules



Target = Area Metal / Area Gate

Wire is charged during etching and can gather enough voltage to damage transistor gate

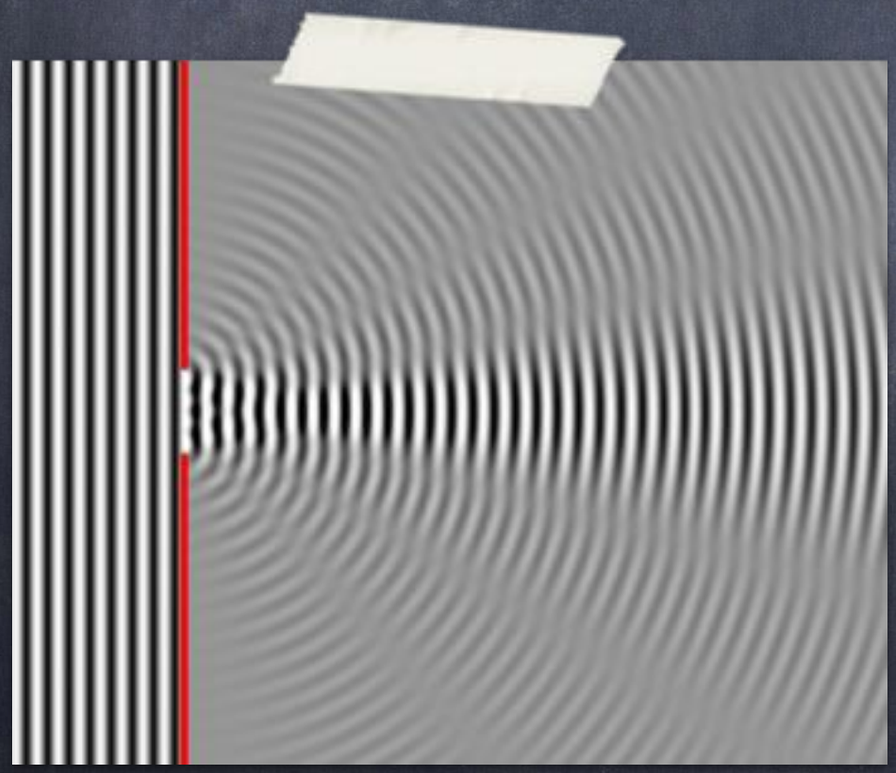
Phase Shifting Masks (PSM)

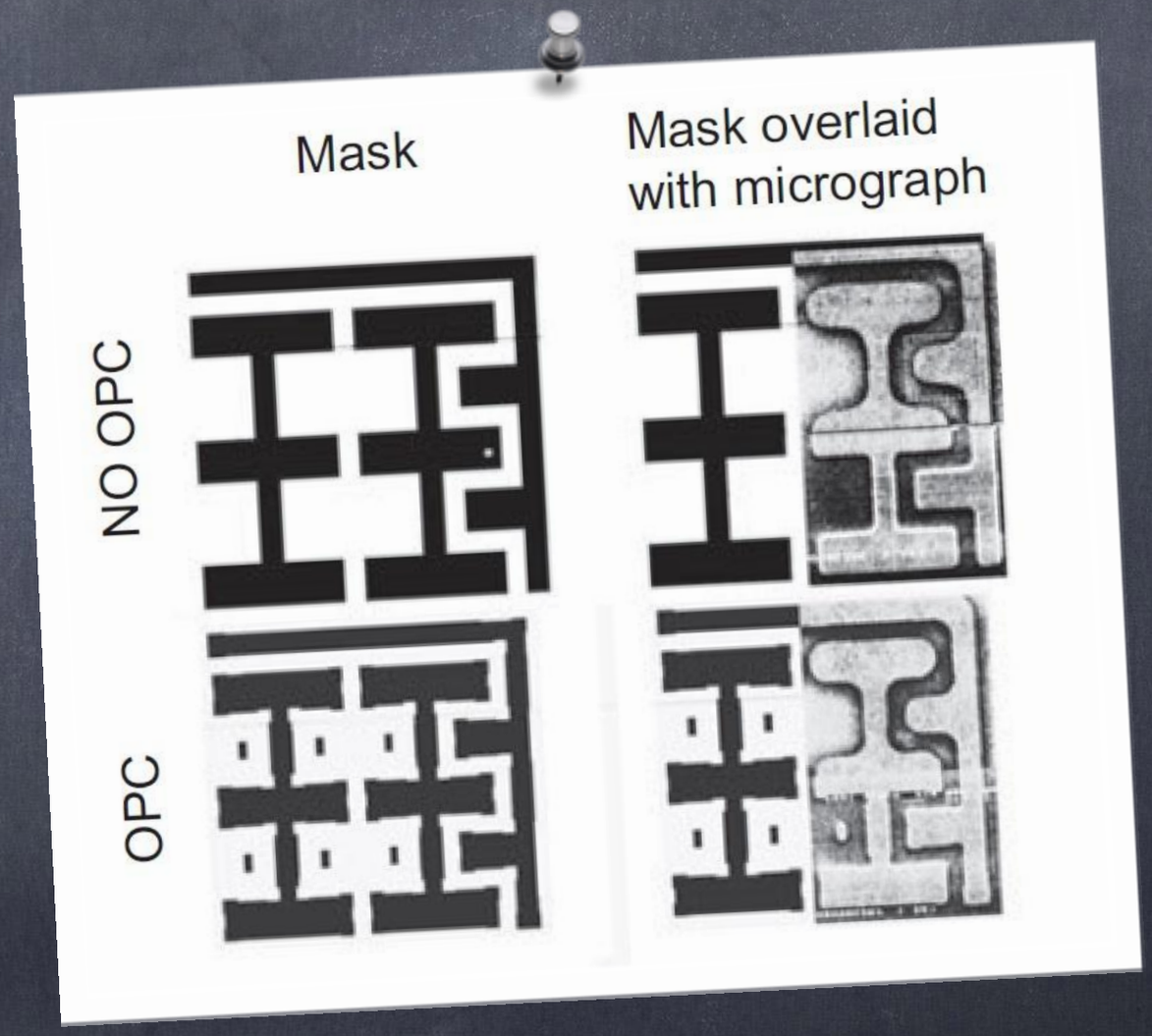


Adjacent Transparent parts are made with opposite phase so that the intersections can be substracted, thus increasing resolution.

Optical Proximity Correction (OPC)

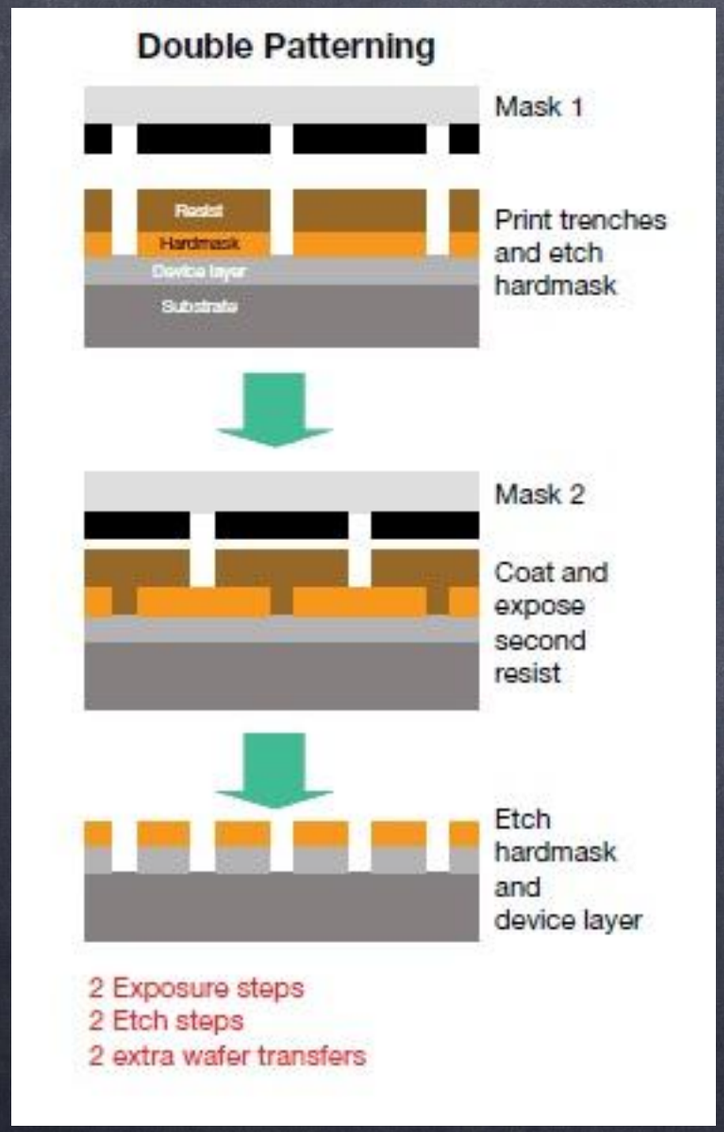
Non-Uniform exposure* is compensated in the mask





*Center receive more light than edge due to diffraction

Double Patterning



Use two precisely aligned mask and two exposure steps to reduce pitch

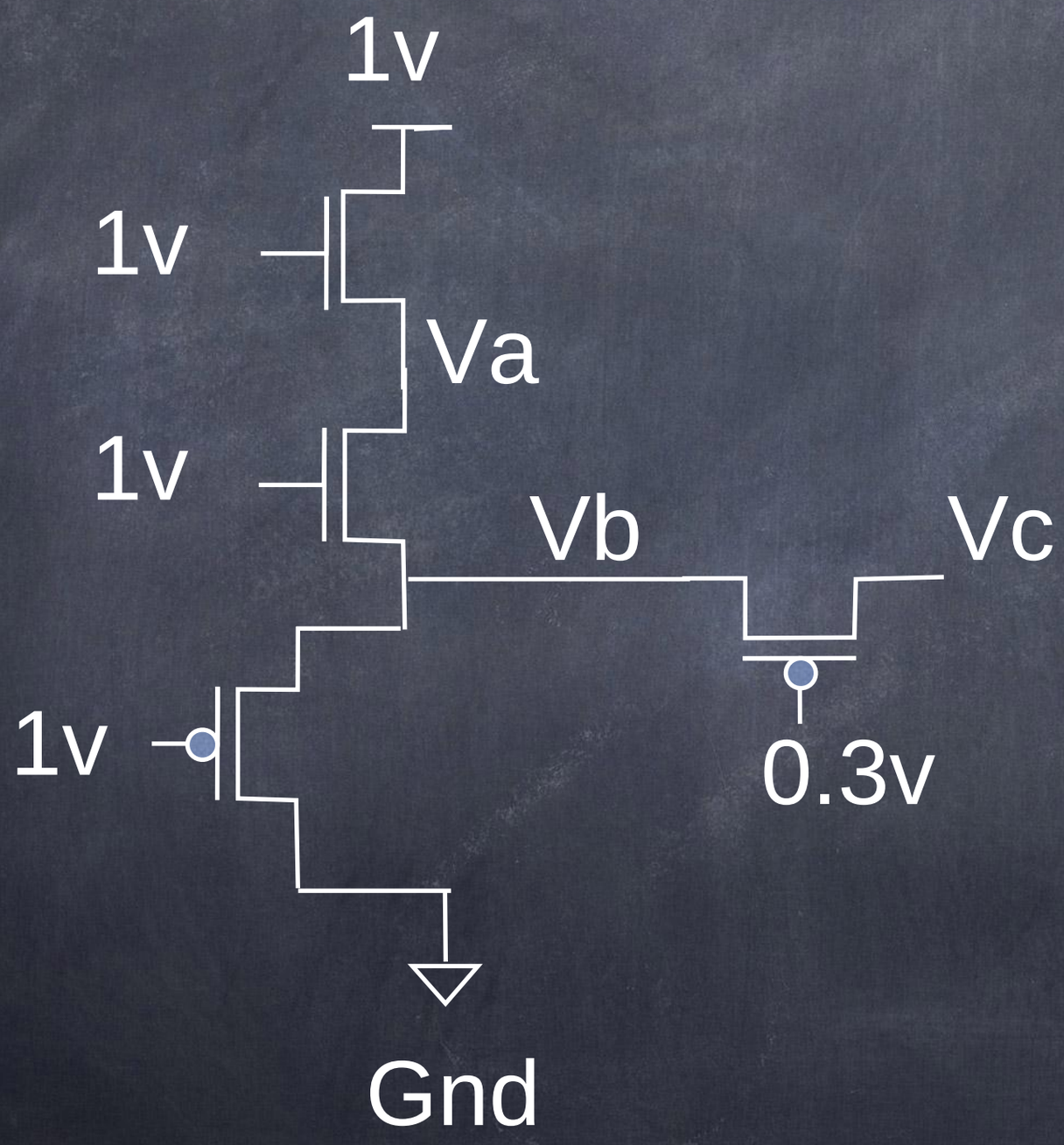
*Future Fab Intl. Issue 28. Michael Lercel, IBM

Quiz for Understanding

Draw the circuits for the functions below

- A+B
- (A*(B+C))’
- A xor B

Calculate Node Voltages

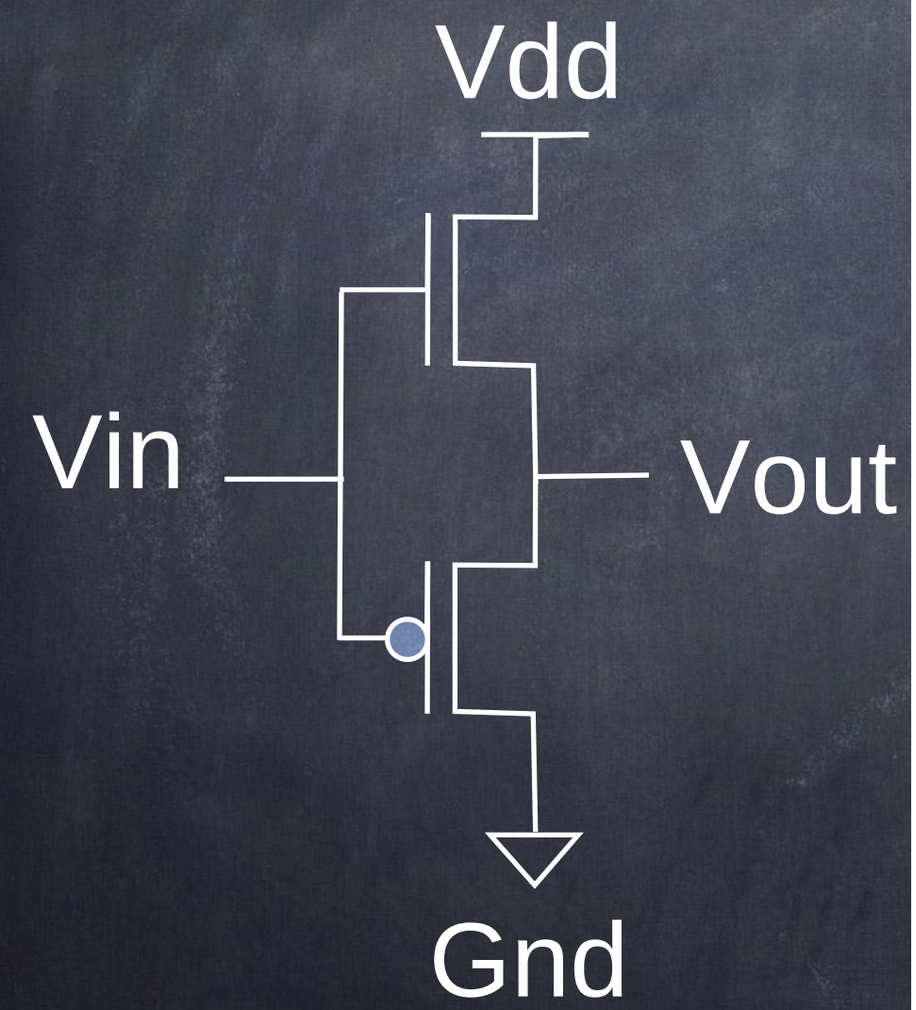


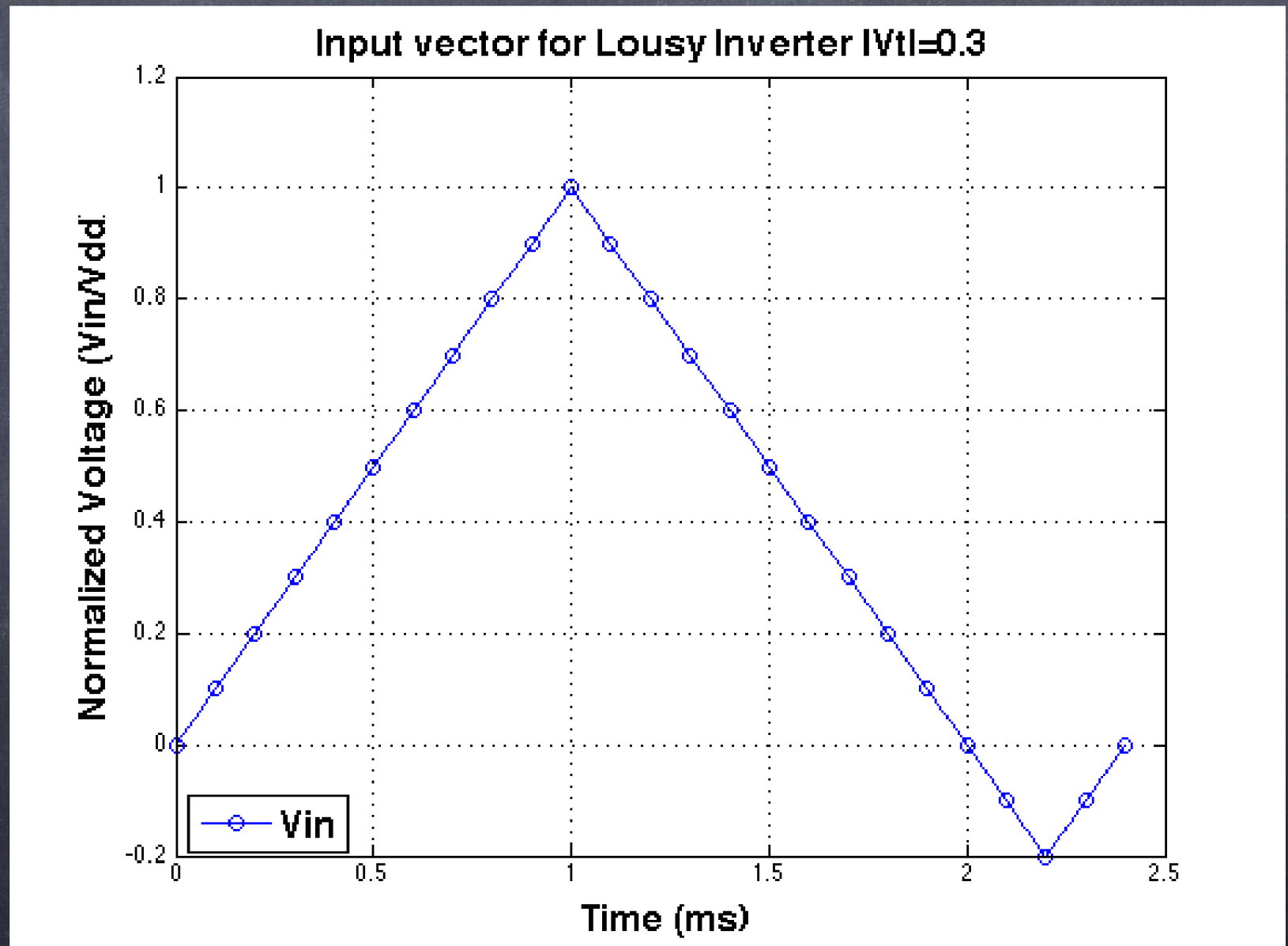
Assume that at t = 0, all nodes are at 0 [V]

|Vt| = 0.3

Node	Voltage
Va	
Vb	
Vc	

Plot the output response for the given input





Summary

- Silicon technology enables cheap and efficient computation
- Good CMOS gates are:
  - Uni-directional
  - Rail to rail
  - Noise attenuated
  - Defined by binary equations
  - Low dynamic power dissipation
- Standard Cells
  - Allows tools to handle circuits, synthesis / place & route

References

- *Weste, Harris - CMOS VLSI Design 4th Edition*
- *Rabaey, Digital Integrated Circuits*
- *Moore65, “Cramming more components onto integrated circuits”*
- *Dennard74, “Design of Ion-Implanted MOSFET’s with Very Small Pl*