SYNOPSYS®
Silicon to Software™

IC Design

An Introduction

Material based on Synopsys University Courseware and Synopsys CES

Developed by Vazgen Melikyan

Agenda

Introduction

IC types and design flows

IC Manufacturing Process

Digital design flow by Synopsys tools

New challenges to IC design flow

Introduction

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Implementation of Chips

- Semiconductor industry is about $410B.
- Electronic Design Automation (EDA), i.e. the industry of creating automated design tools of semiconductor chips and IP is about $ 7B.
- Semiconductor chips are used in:
  - Computers
  - Cellular phones
  - Gaming systems
  - DVD players, TVs
  - Watches
  - Cars
  - Medical devices
  - Pacemakers and coffee pots
  - Space stations
  - Greeting cards
  - . . .

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History and Evolution of the IC Industry

Semiconductor Industry Association (SIA) Roadmap

Date	1999	2005	2016
Technology (nm)	180	65	7
Minimum mask count	22/24	25	29/30
Wafer diameter (mm)	200	400	450
Memory samples (bits)	1G	8G	1T
Transistors /cm^2	6.2Ø	180M	390M
Maximum number of metal layers	6-7	9	13
Clock frequency (MHz)	1250	3200	10000
IC sizes (mm^2)	400	760	2240
Power supply (V)	1.5-1.6	0.8-1.2	0.37-0.42
Maximum power (W)	90	150	183
Number of pins	700	1957	3350

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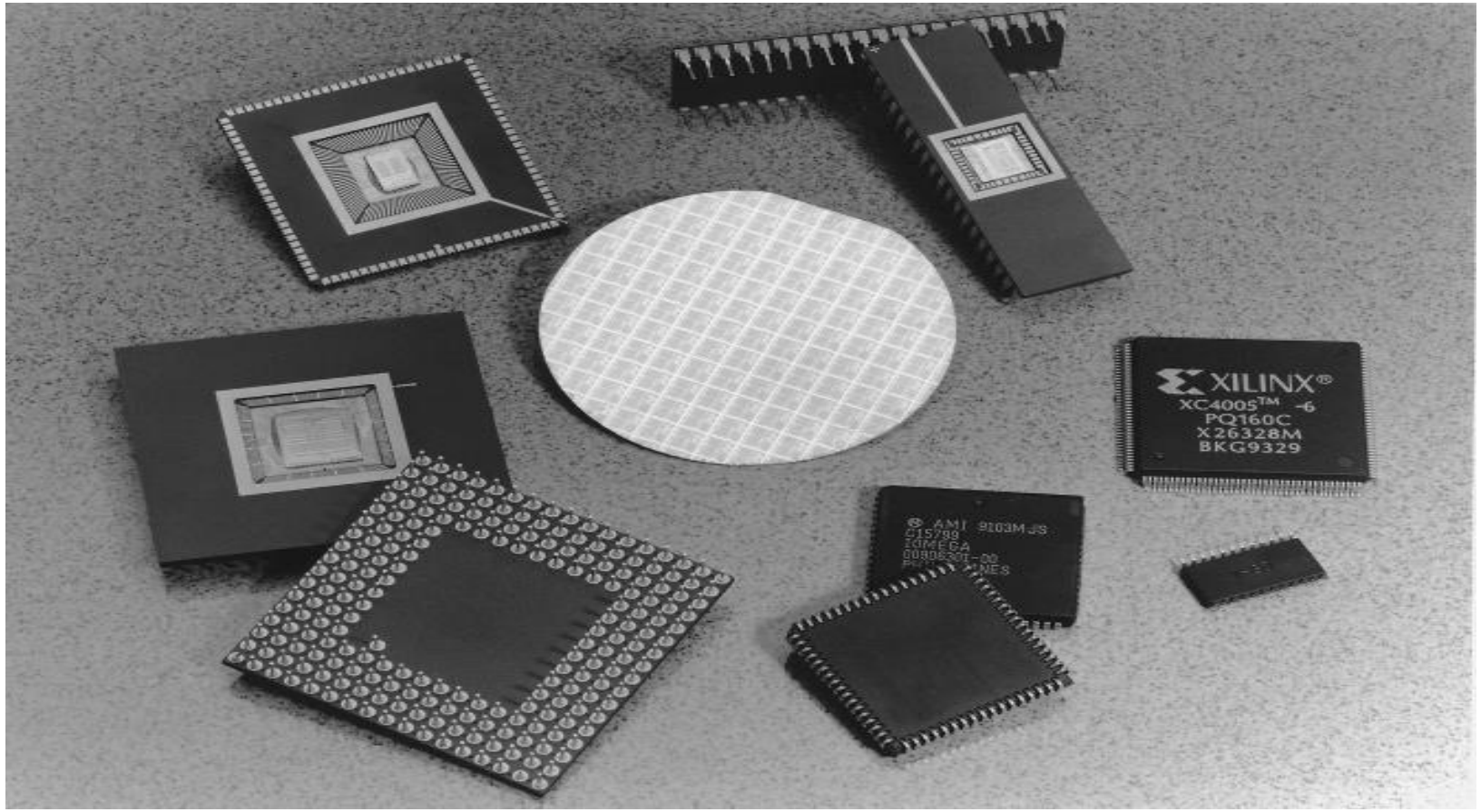
History and Evolution of the IC Industry

Other Source

Date	2004	2007	2010	2013	2016	2019
Technology (nm)	90	65	45	32	7	5
Clock frequency (MHz)	4171	9285	15079	22980	39683	53207
Chip area (mm^2)	280	280	280	280	280	280
Supply voltage (V)	1.2	1.1	1.0	0.9	0.8	0.7
Maximum power (W)	158	189	218	251	288	300
Average chip current (A)	132	172	218	279	360	429

Chip Packages



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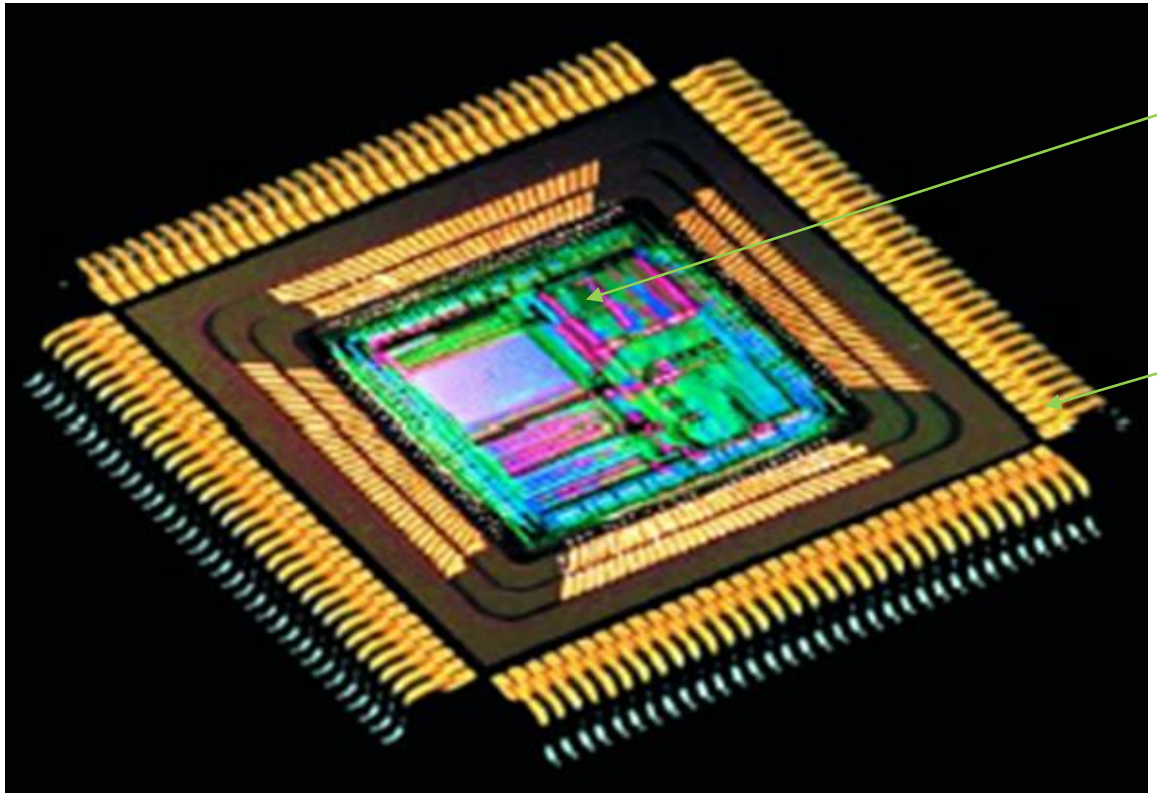
Die and package



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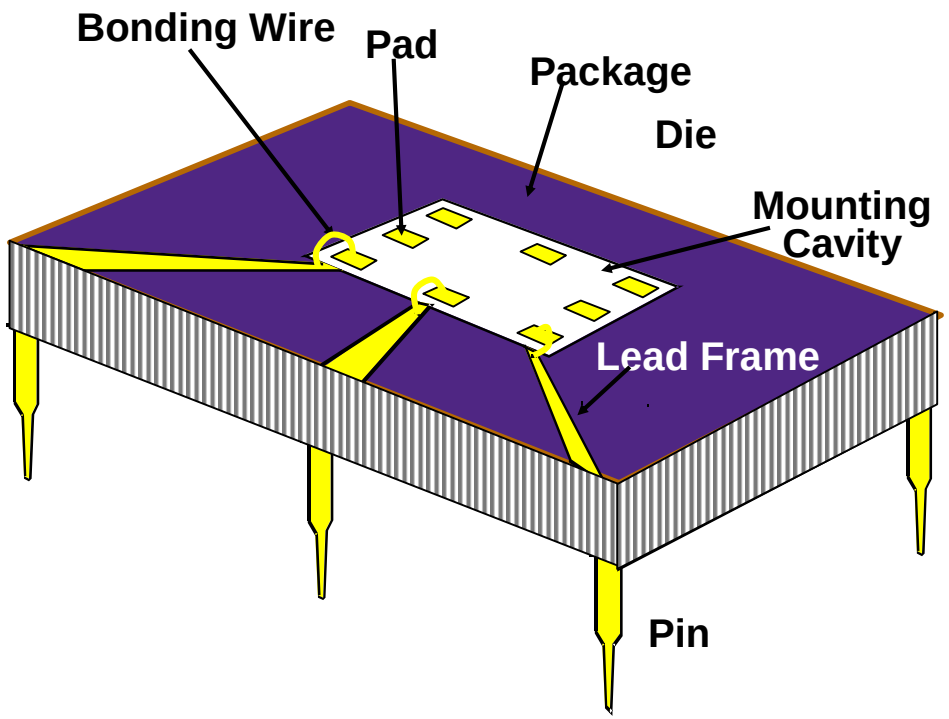
IC Packaging

- Bonding wires connect the package to the chip.
  - They are relatively large ~950μm in 45nm technology, with pitch 40μm
- Pads are arranged in a frame around the chip.
  - Pads are relatively large ~20μm in 45nm technology, with pitch 15μm



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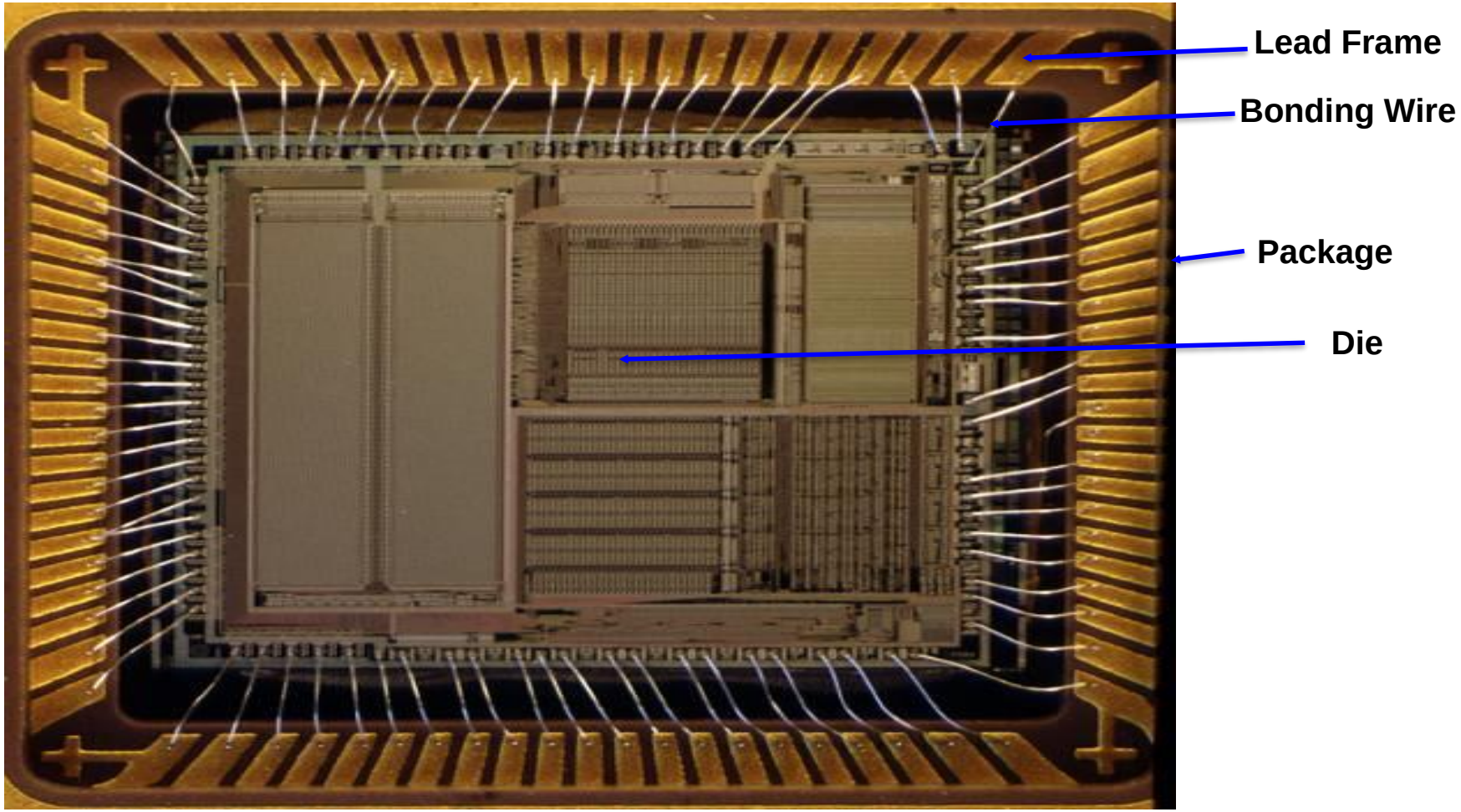
Top View of a Real IC



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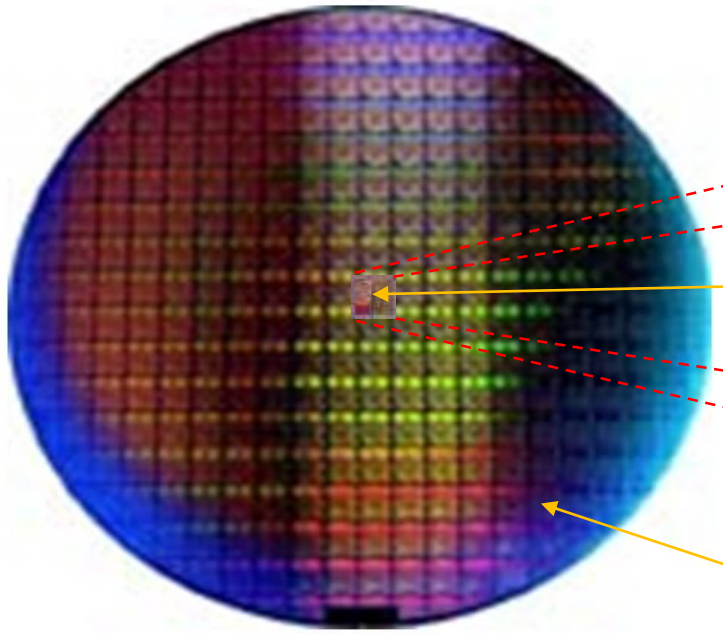
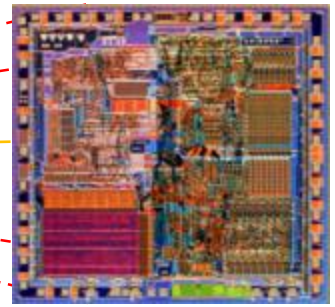
Wafer and Die

- CMOS ICs are fabricated on circular slices of silicon called wafers.
- Wafer contains various identical dies.

Side view of a Wafer



Die



Top view of a die

Wafer

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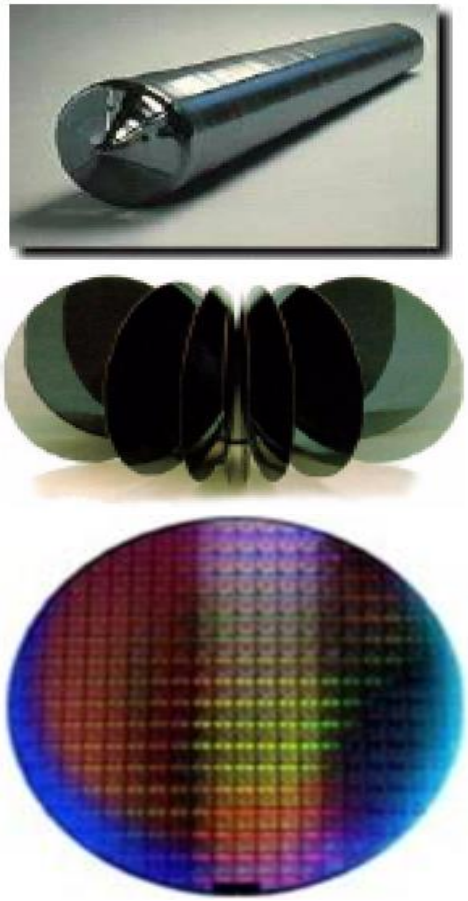
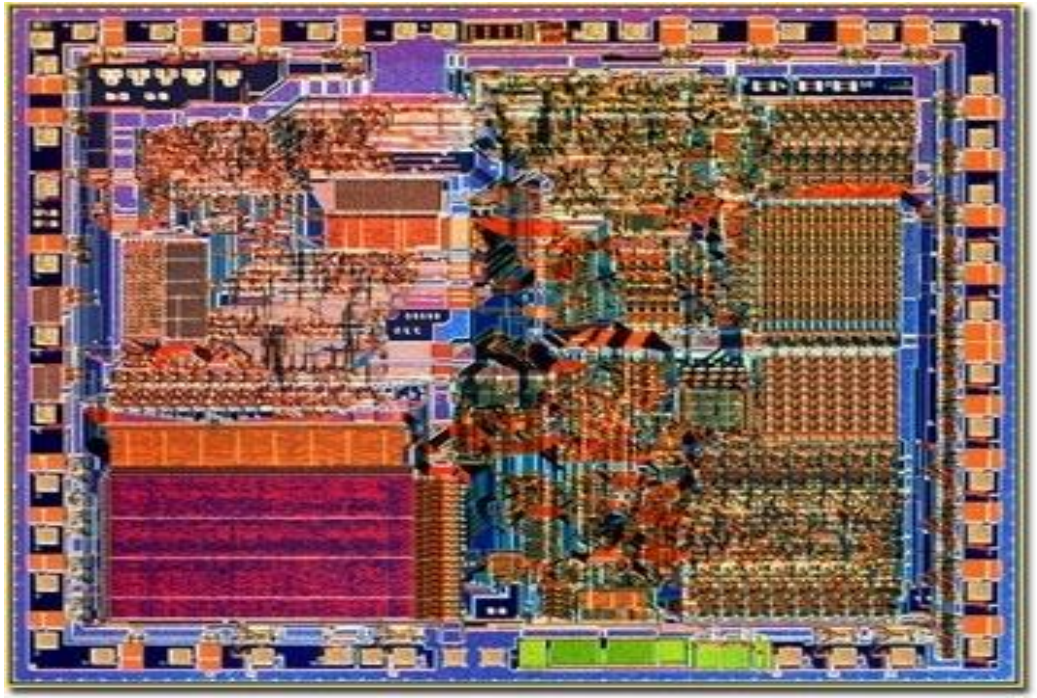
Wafer and Die (2)

- Thickness 275um – 925um
- Diameter up to 450mm
- Wafer is cut from metal-cast of single crystal silicon.



IC Definition

- Integrated circuits (IC) is a complex set of electronic components and their interconnections etched on a chip.



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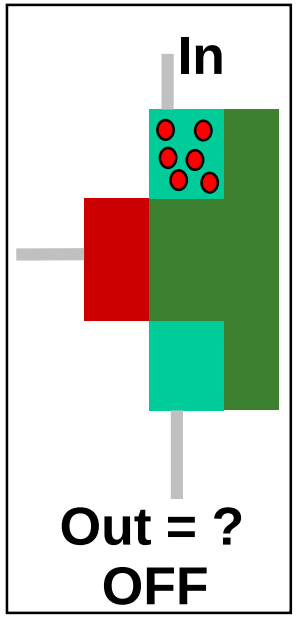
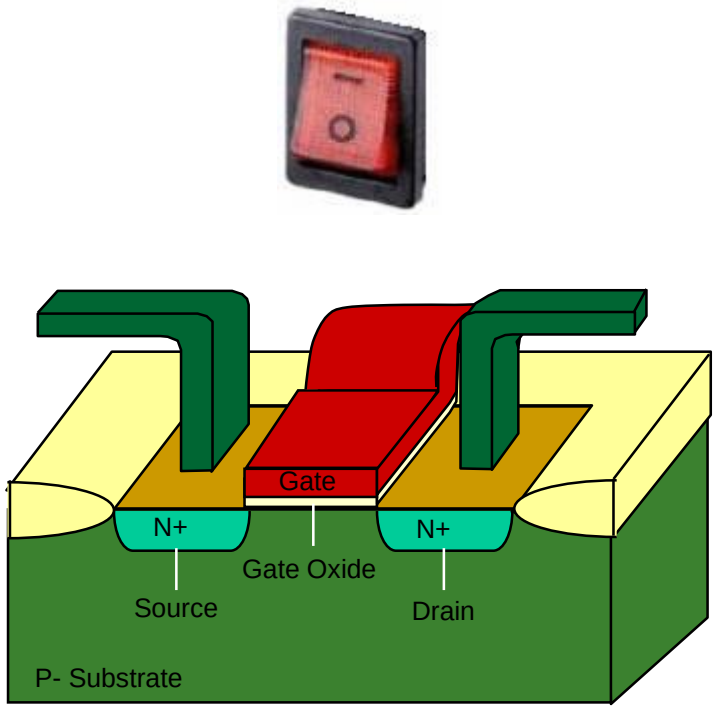
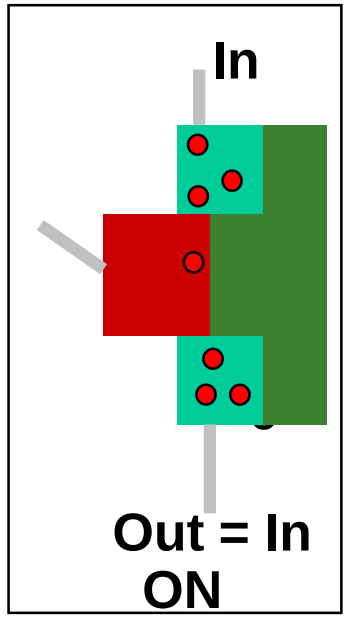
Basic Element of IC – The Transistor

CMOS Transistor is a switch







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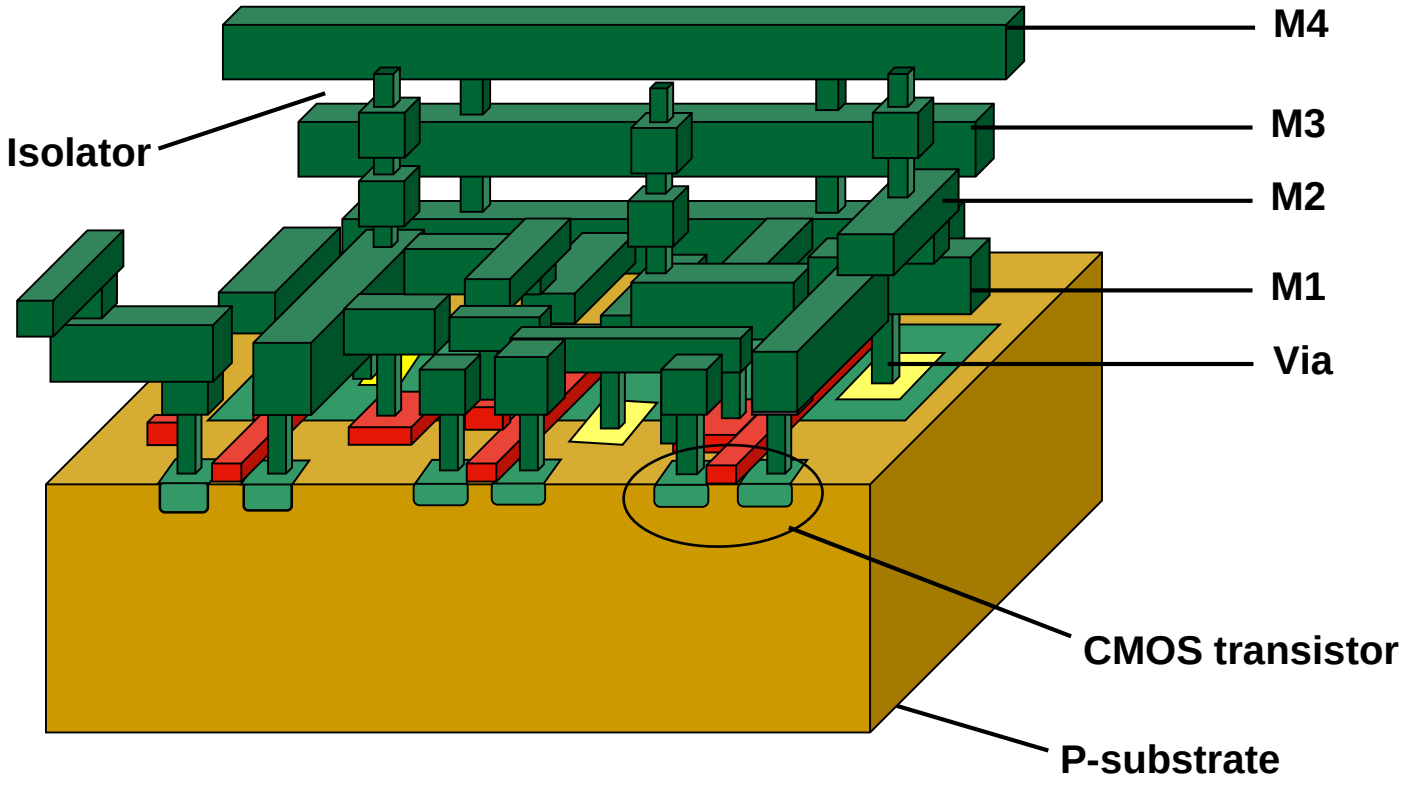
IC is a Multi Layer Structure



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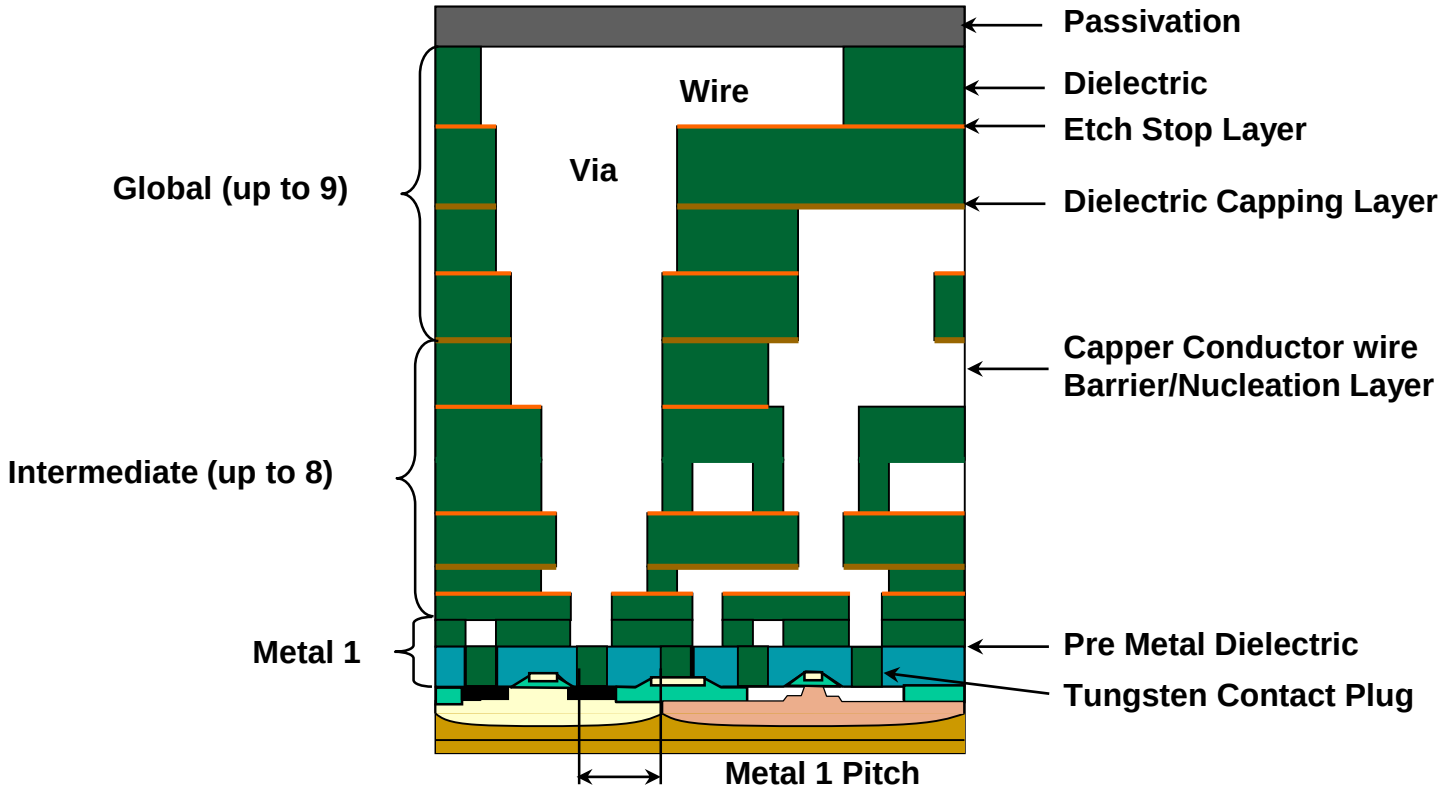
IC is a Multi Layer Structure (2)



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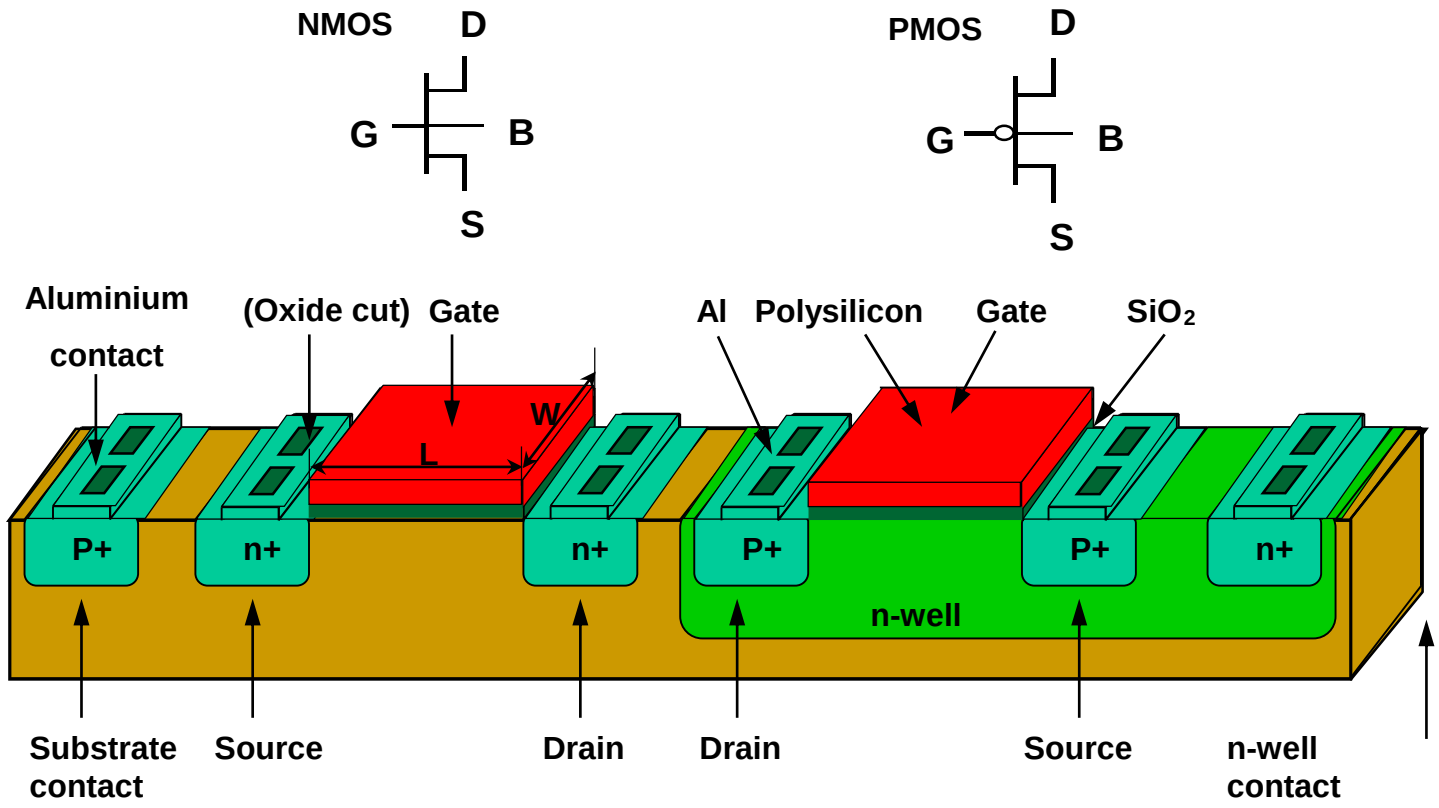
NMOS and PMOS Transistor Structures



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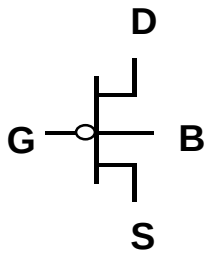
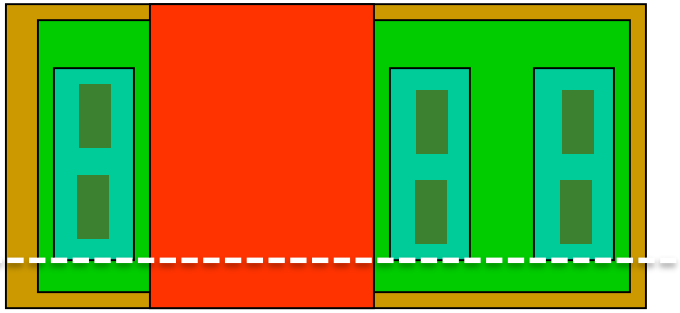
Concepts of the Circuit and Layout

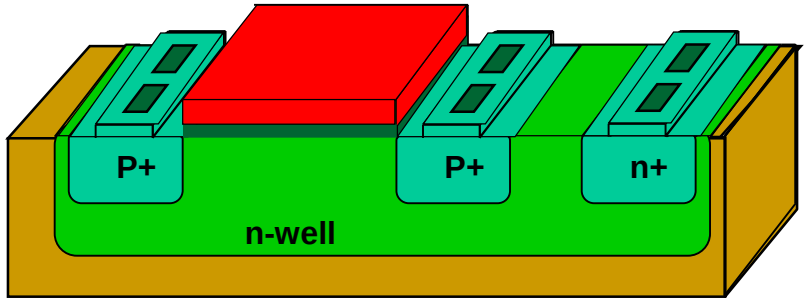
Circuit



Layout



Resulting structure in manufactured IC



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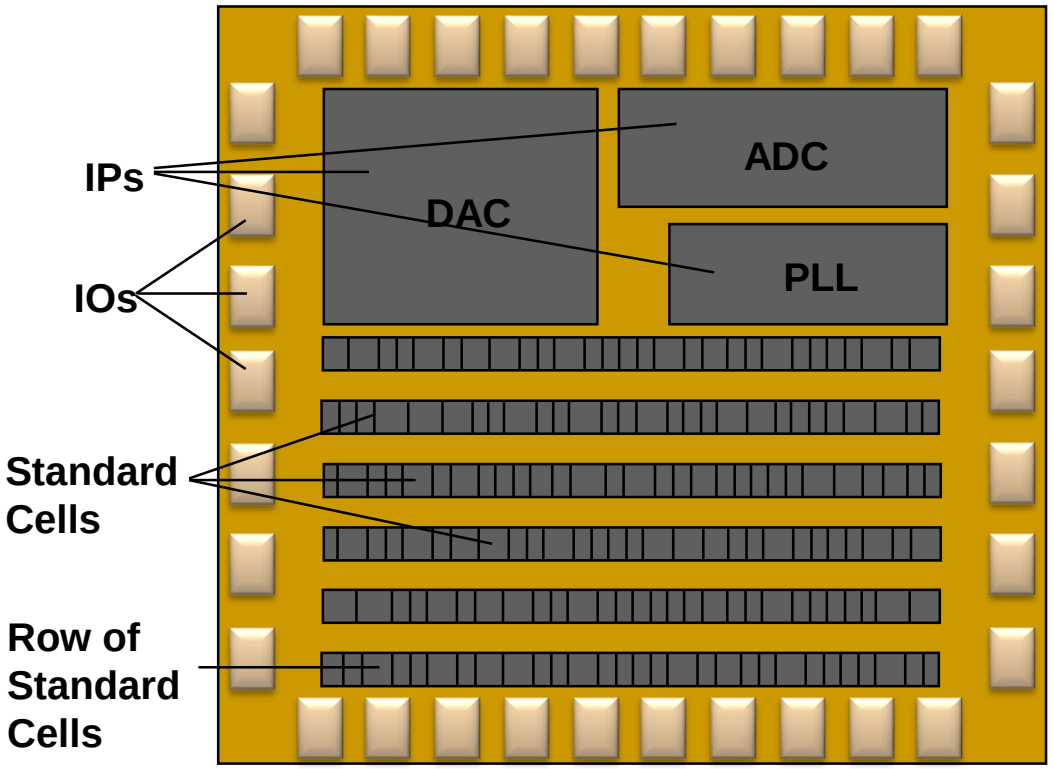
IC Component Types



- Intellectual Property (IP) represents large blocks performing completed functions (DAC, ADC, PLL, etc)
- Standard Cells represent digital nodes performing simplest functions.

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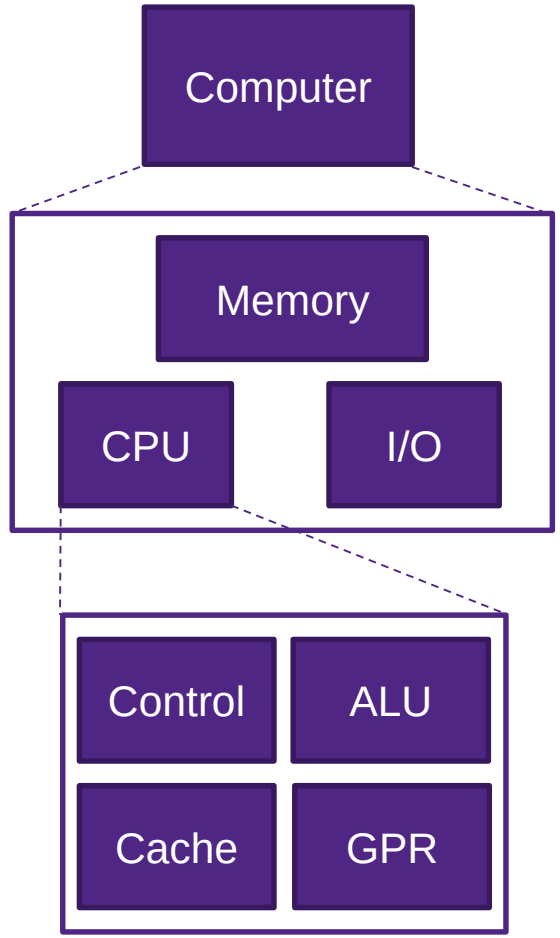
IC Design Problems

- IC Characteristics
  - Area
  - Speed
  - Power dissipation
  - Design time
  - Testability
- It is impossible to design an integrated circuit at once while having required characteristics
- The complexity is simply too high

Complexity Management: Abstraction

- Abstraction is the definition of object at some level of detail hiding away the more detailed implementation
  - Simplifies the design process
  - Enables design at various levels of abstraction
- Abstraction example
  - Black box abstraction
  - Black box is a device, system or object which can be viewed solely in terms of its input, output and transfer characteristics without any knowledge of its internals



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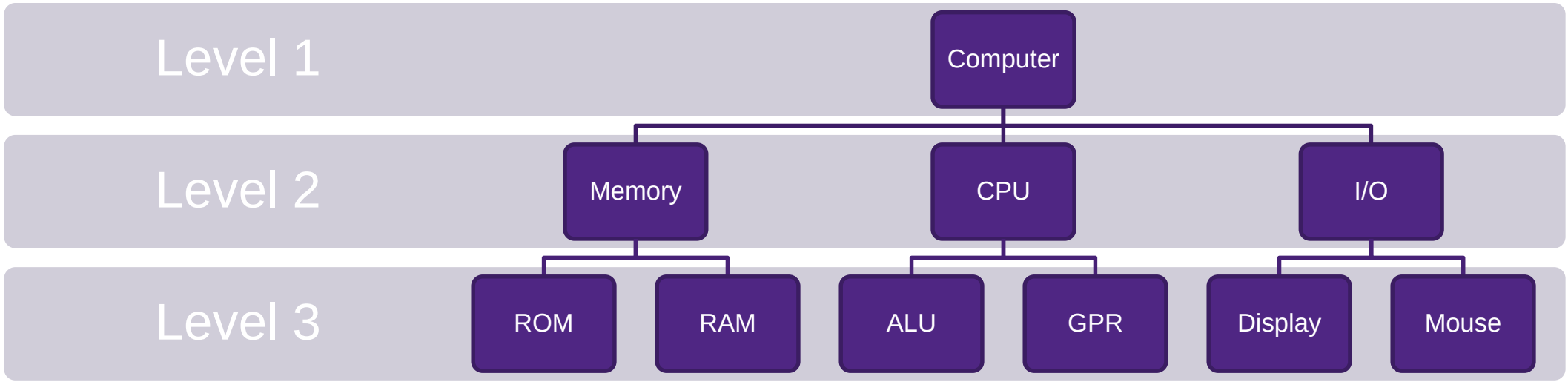
Complexity Management: Hierarchy

- Hierarchy is the structure of a design at different levels
  - Each part is itself composed of interacting subparts at a lower level of abstraction.
- This decomposition continues until the basic building blocks (e.g. transistors) of an IC are reached.



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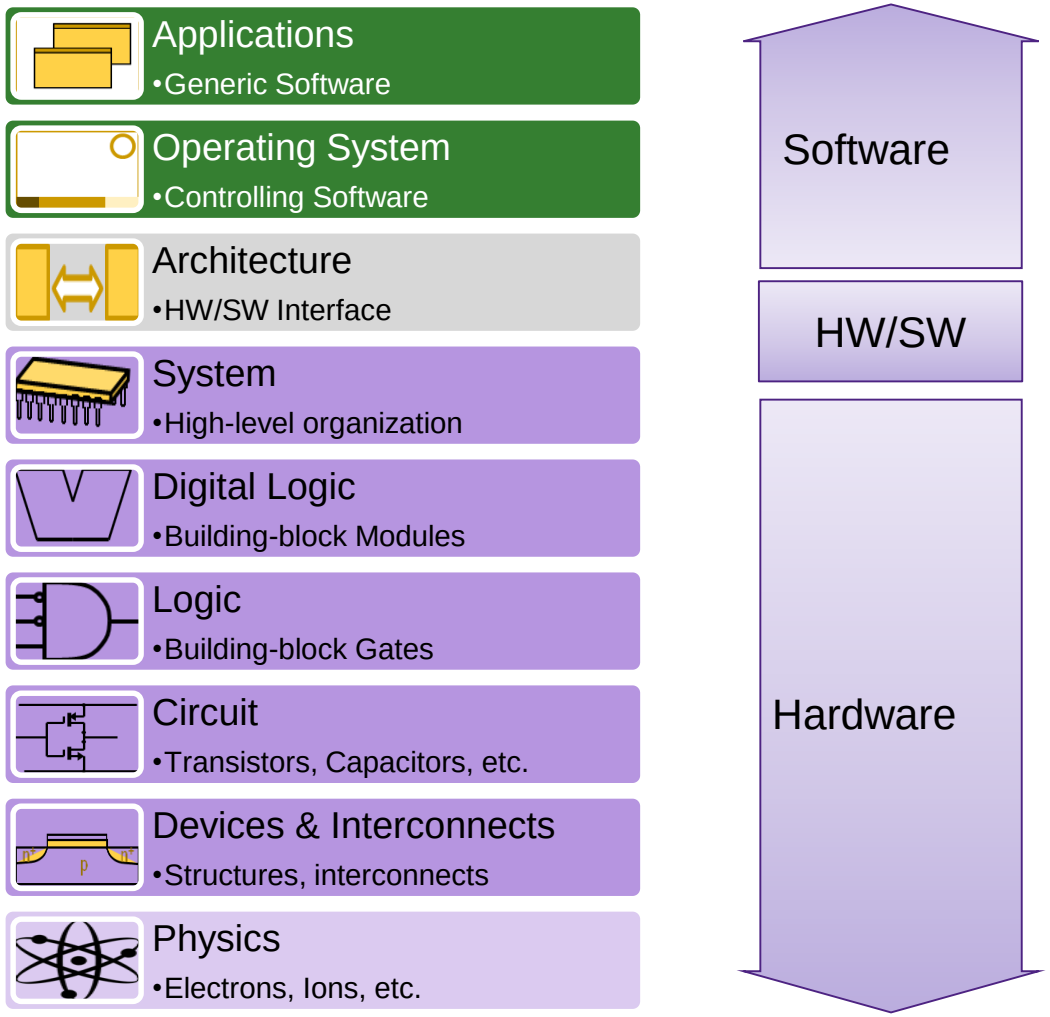
Design Abstraction Levels



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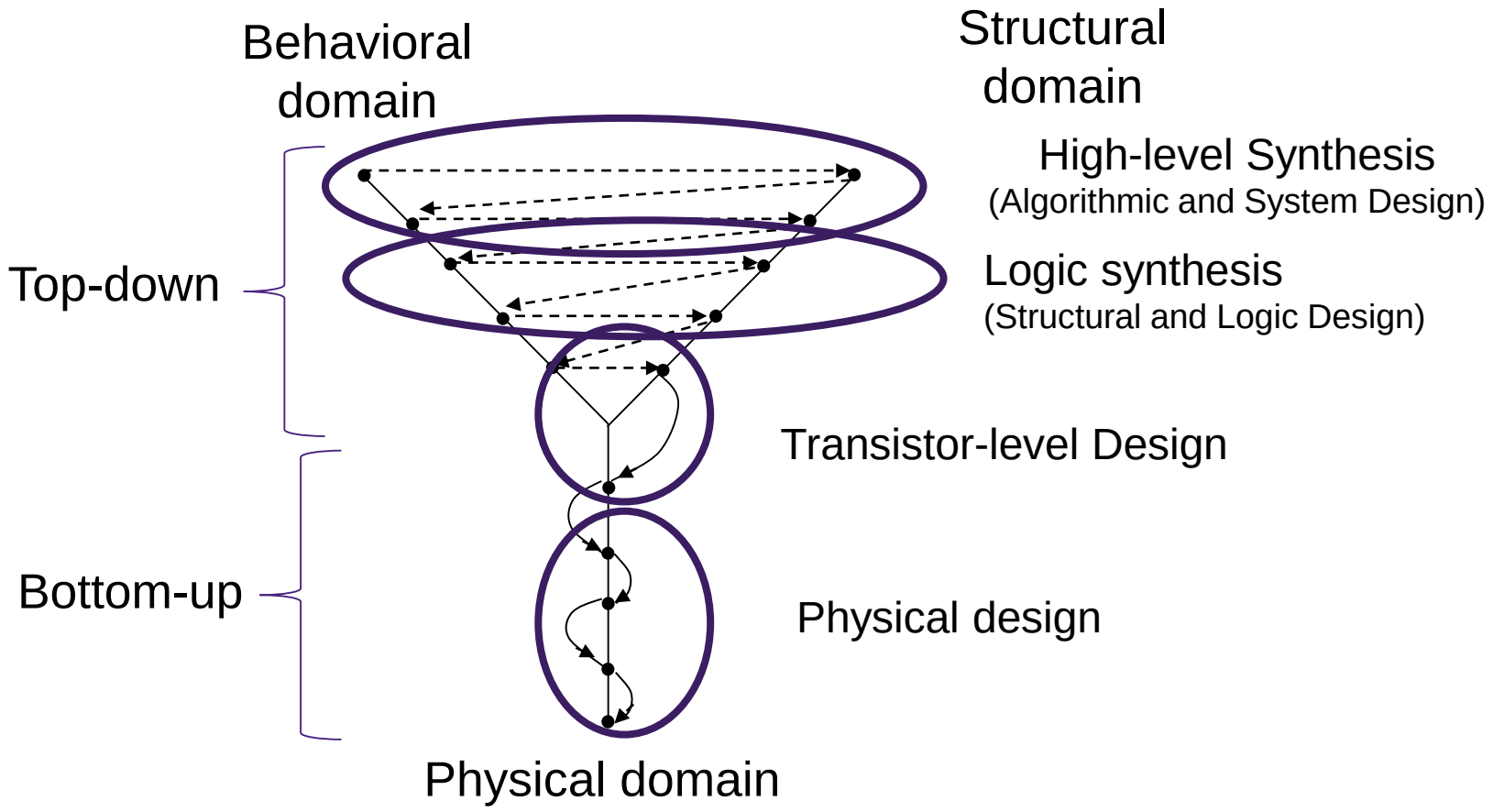
Top-down and Bottom-up Design Methodology



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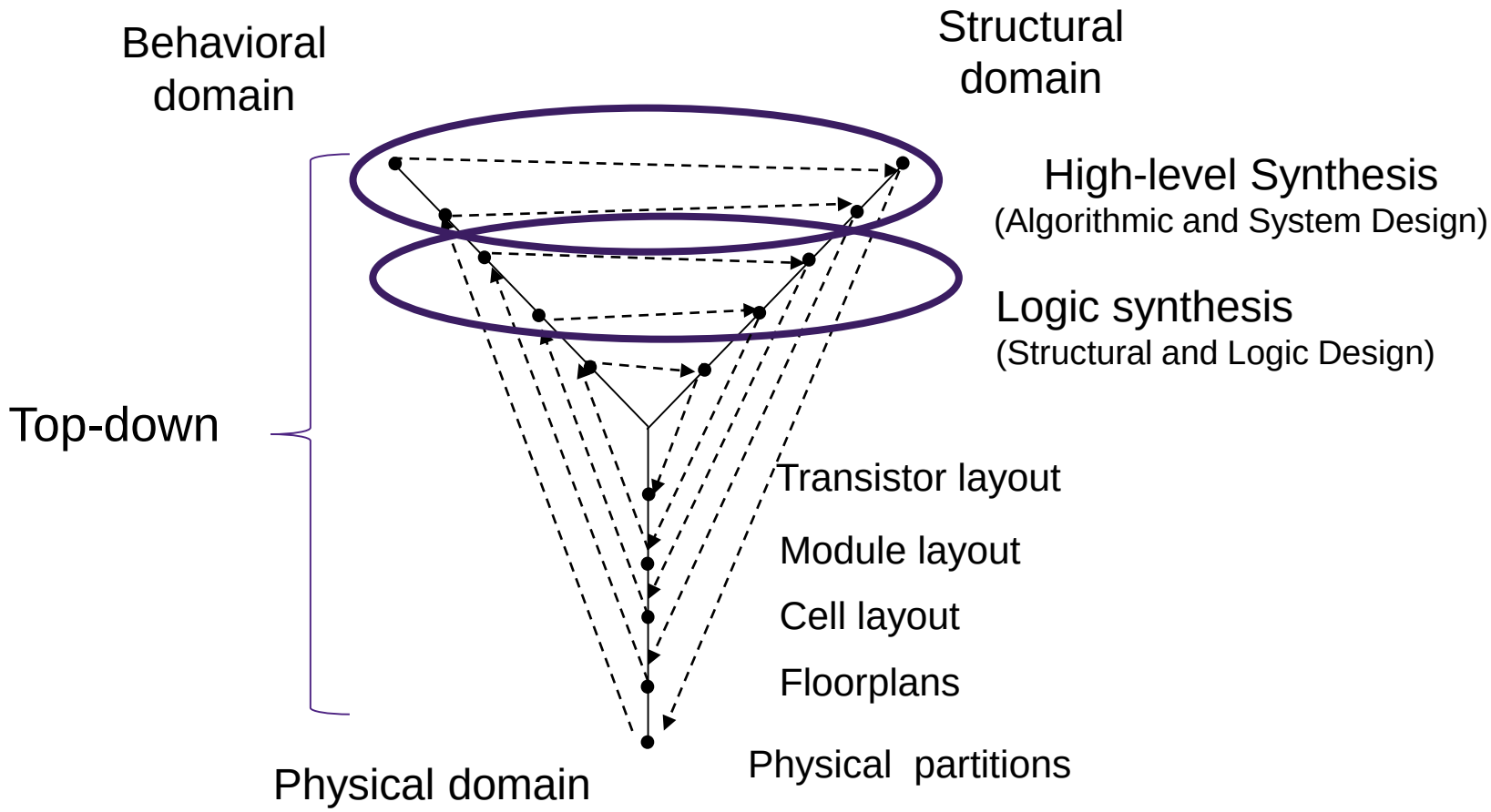
Only Top-down Design Methodology



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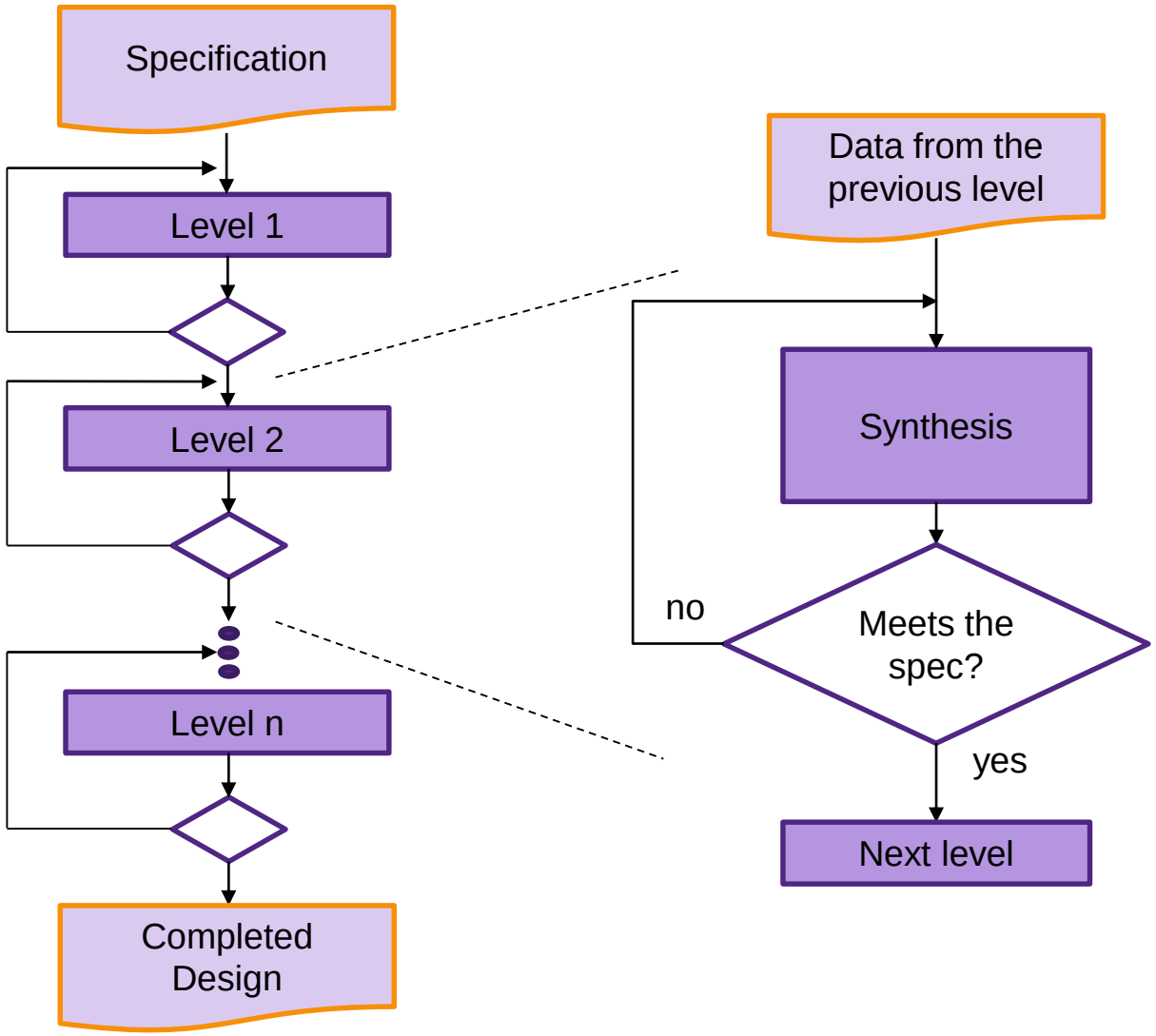
The Concept of Design Flow



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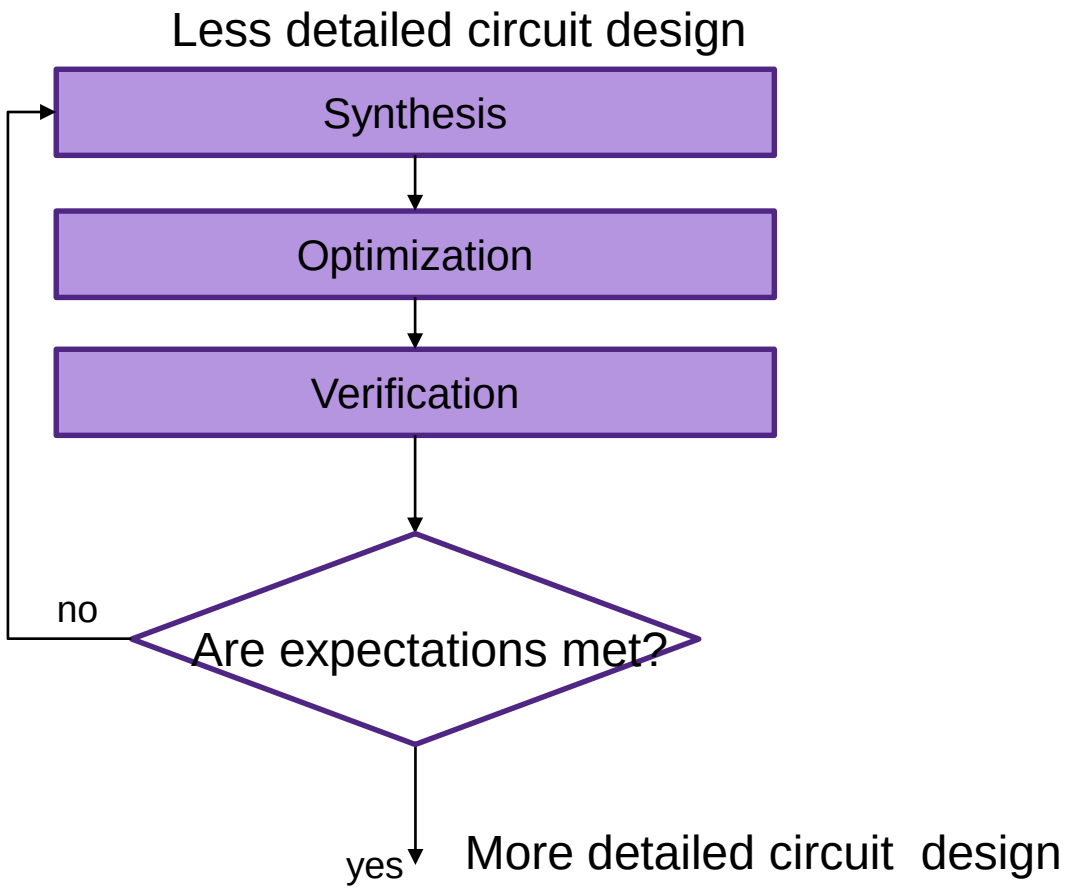
Problems Solved in One Design Level



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IC Types and Design Flows

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Design Goals

- Cost
  - Non-Recurring Engineering (NRE) cost
    - One-time cost spent on research and design of IC after which recurring manufacturing can be started
  - Manufacturing cost
- Quality
  - Design performance/area/power tradeoff
- Time-to-Market
  - Design and manufacturing time

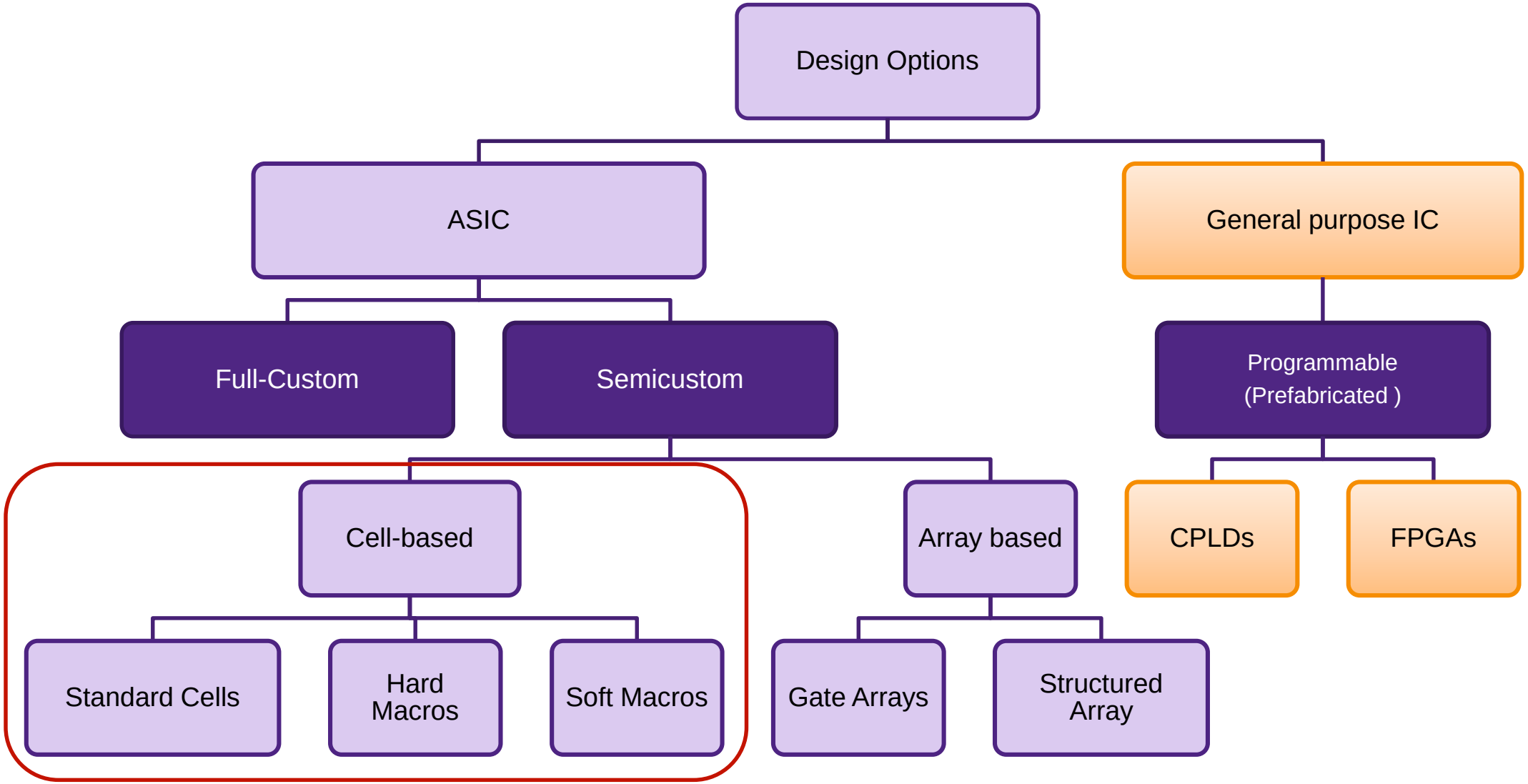
Design Manufacturing Options

- Full-Custom
  - All design and manufacturing process cycles are circuit specific
- Semicustom
  - Some design and manufacturing cycles is predefined
- Programmable
  - Functionality achieved by configuring (programming) already fabricated general purpose IC

	Full-Custom	Semi-Custom	Prog.
Cost (design/manufacturing)	High	Small	Low
Quality (performance/area/power)	Best	Low	Low
Time-to-Market (time-to-market)	Long	Short	Short
Production Volume (use cases)	Large	Medium	Small

Full-Custom and Semicustom fabrication is used for Application Specific ICs (ASIC), i.e. manufactured for specific purpose

Design Options



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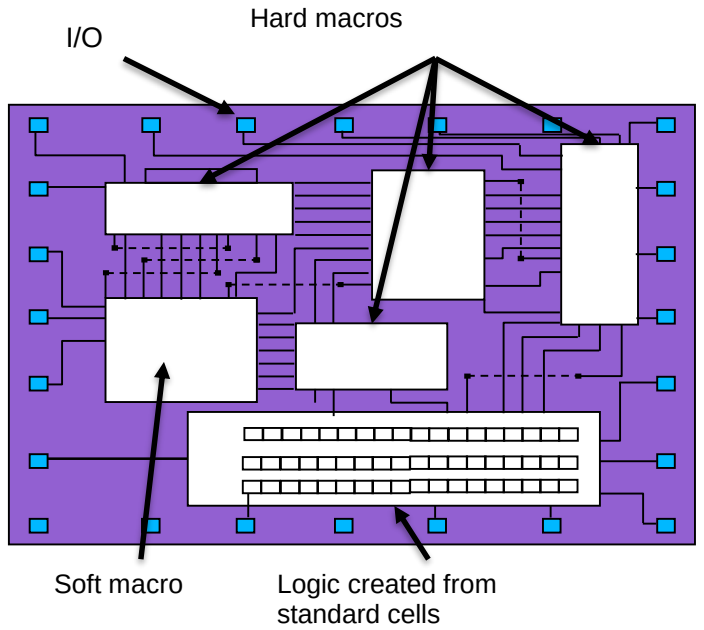
Cell-based design

- Design is compiled using ready blocks:
  - Technology-dependent fixed size physical designs
    - Digital standard cells
      - Small cells performing simple logic used to build larger designs (Boolean primitives: and, or, xor; flip-flops; adders, etc.)
    - Hard macros (Hard IP)
      - Ready physical design (analog cells, I/O cells, etc.)
  - Technology-independent behavioral descriptions, synthesizable to physical design using standard cells and if necessary hard-IPs
    - Soft macros (Soft IP),
      - synthesizable register transfer level descriptions of complex functions (processor cores, arithmetic units, etc.).
    - System-level macros (SLMs)
      - High level behavioral descriptions (DSP logic, digital filters, etc.)



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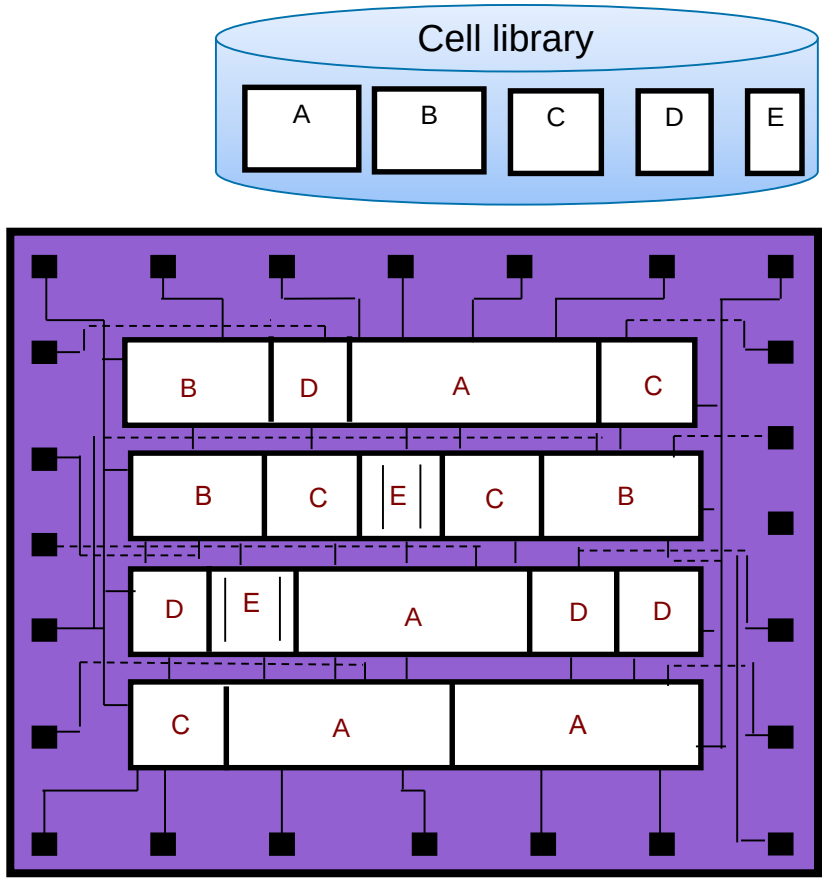
Cell-based design: Standard Cells

- Design done at behavioral level
- Behavioral description automatically translated to logic circuit and layout by EDA tools
- Standard cells are used to build logic
- Use:
  - Large digital designs (arithmetic units, processors)



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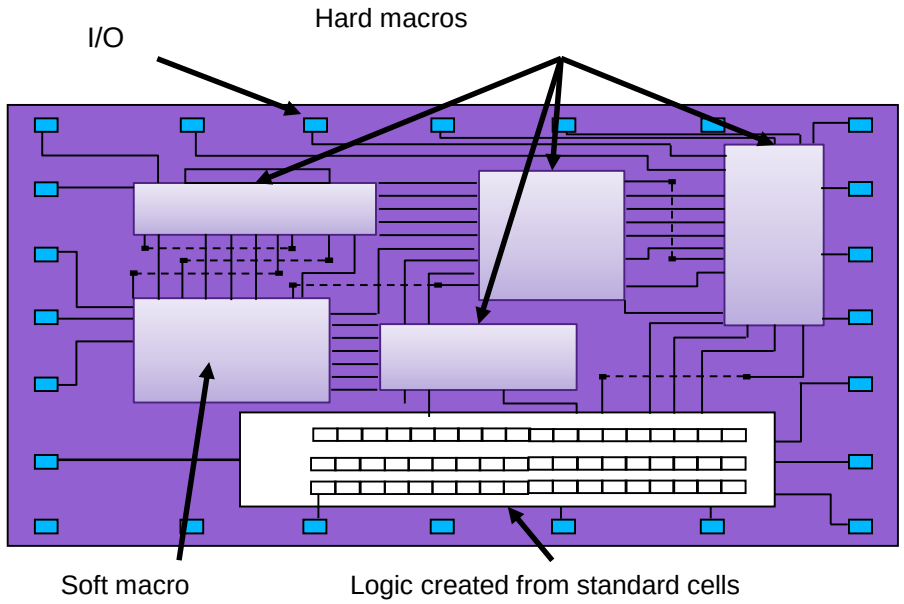
Cell-based design: Macro Cells

- Design is created of ready macro cells
  - Hard macros
  - Soft macros (first synthesized for specific technology)
- Use:
  - Functionality that cannot be synthesized using only standard cells (analog functions, cache cells, I/Os, etc.)



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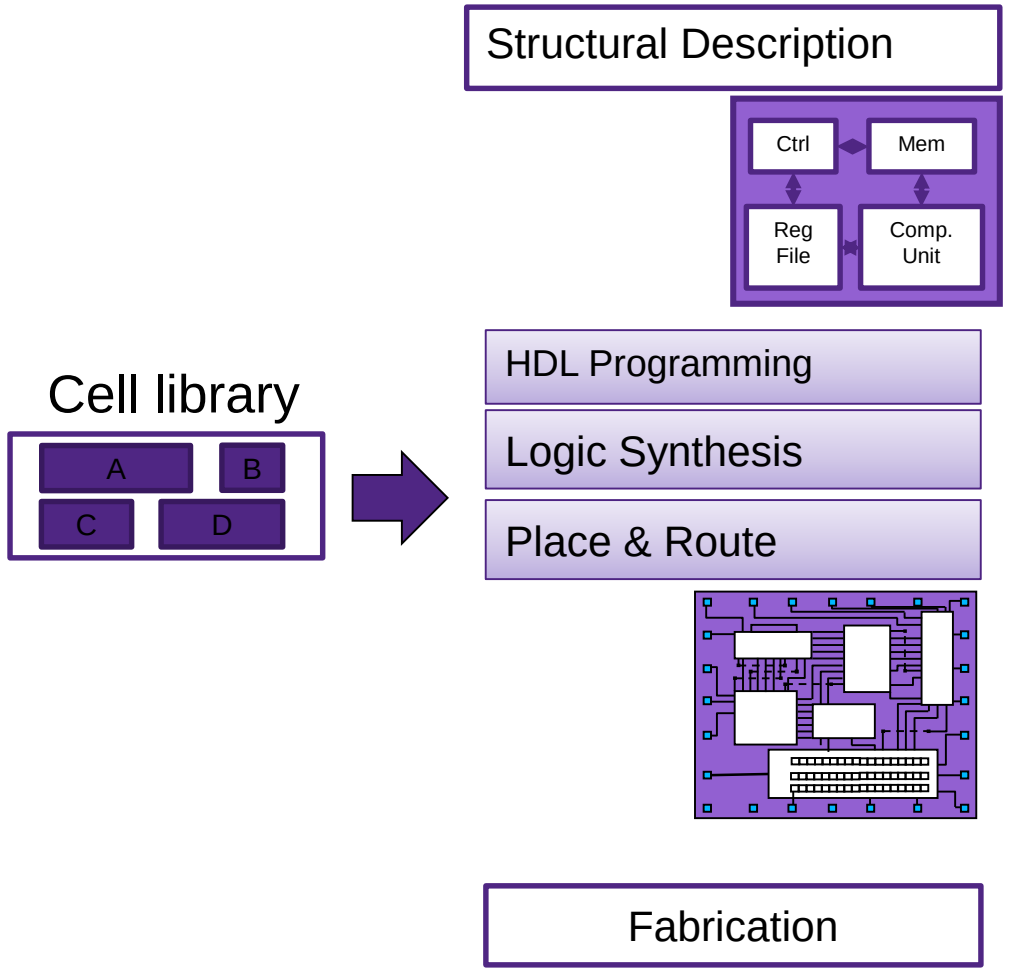
Semi Custom: Cell Based Design Cycle

- Standard cells and another components are predesigned



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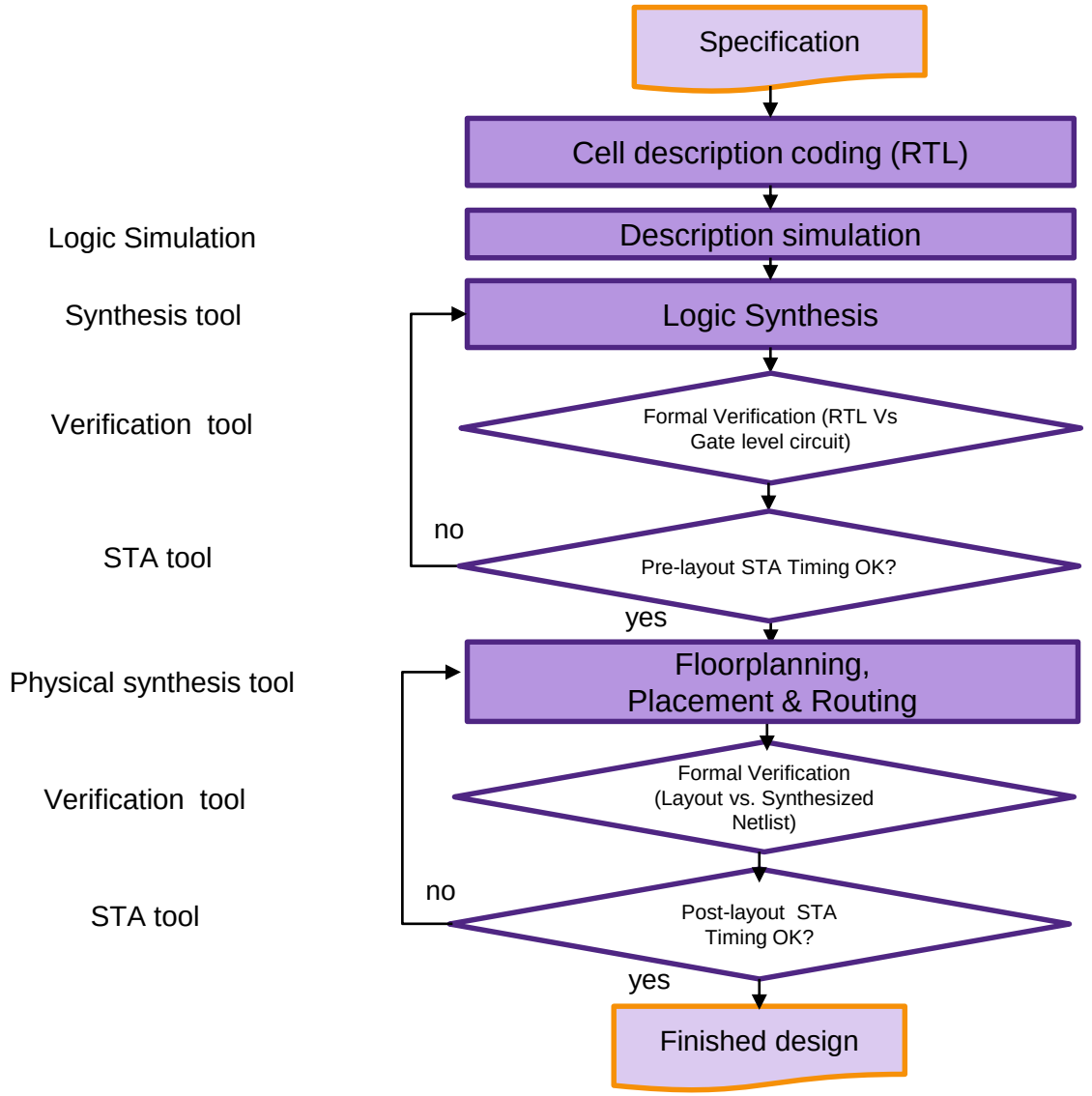
Digital IC Design Flow



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IC Manufacturing Process

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Largest IC Foundries

TSMC (Taiwan Semiconductor Manufacturing Company)

Global Foundries

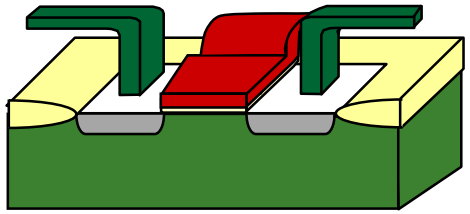
UMC (United Microelectronics Corporation)

SMIC (Semiconductor Manufacturing International Corporation)

SAMSUNG

Evolution of Technological Process

Technological processes are defined by the minimum length (L) of CMOS transistor channel



- 90nm technology – L_{min}=90nm
- 45nm technology – L_{min}=45nm
- 22nm technology – L_{min}=22nm

- TSMC 90nm G Logic 1.0V/3.3V
- SMIC 90nm LL Logic 1.2V/3.3V
- SMIC 130nm LV Logic 1.0V/3.3V
- Samsung 90nm LP Logic 1.2V/3.3V
- UMC 90nm LL Logic 1.2V/2.5

G – generic

LL – low leakage

LV – low voltage

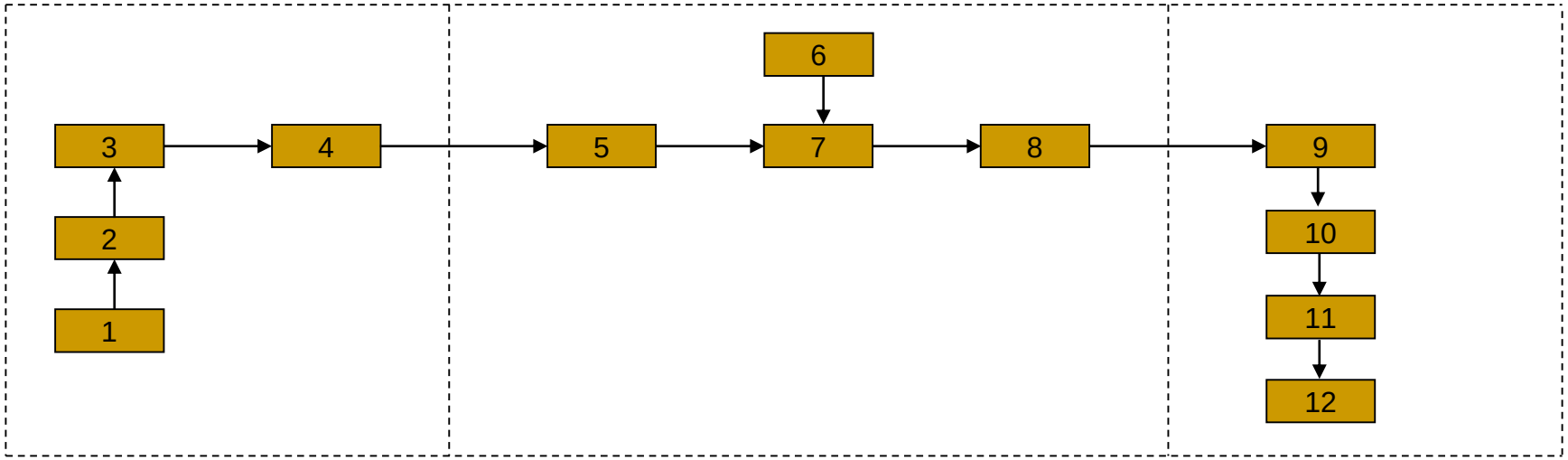
LP – low power

Lithography

- Silicon Technology ≡ Lithography Technology
  - Lithography is a basic method of IC fabrication process.
  - Process is used to transfer patterns from masks to each layer of the IC on the surface of a wafer by employing a photosensitive, chemically resistant layer (photoresist).
  - Masks are created using the layout information provided by the designer.
  - The lithographic process is repeated on each physical layer, but the process sequence is always the same.

Photolithography Steps

- Lithography sequence steps:
  - Designer – Drawing the layer patterns
  - Silicon Foundry – Mask generation, printing, the wafer process



1-wafer
2-surface preparation
3-photoresist application
4-soft baking (100….120ºC)
5-aligment and exposition
6-photomasks
7-development
8-chemical treatment
9-hard baking
10-selective etching
11-photoresist away
12-pattem control

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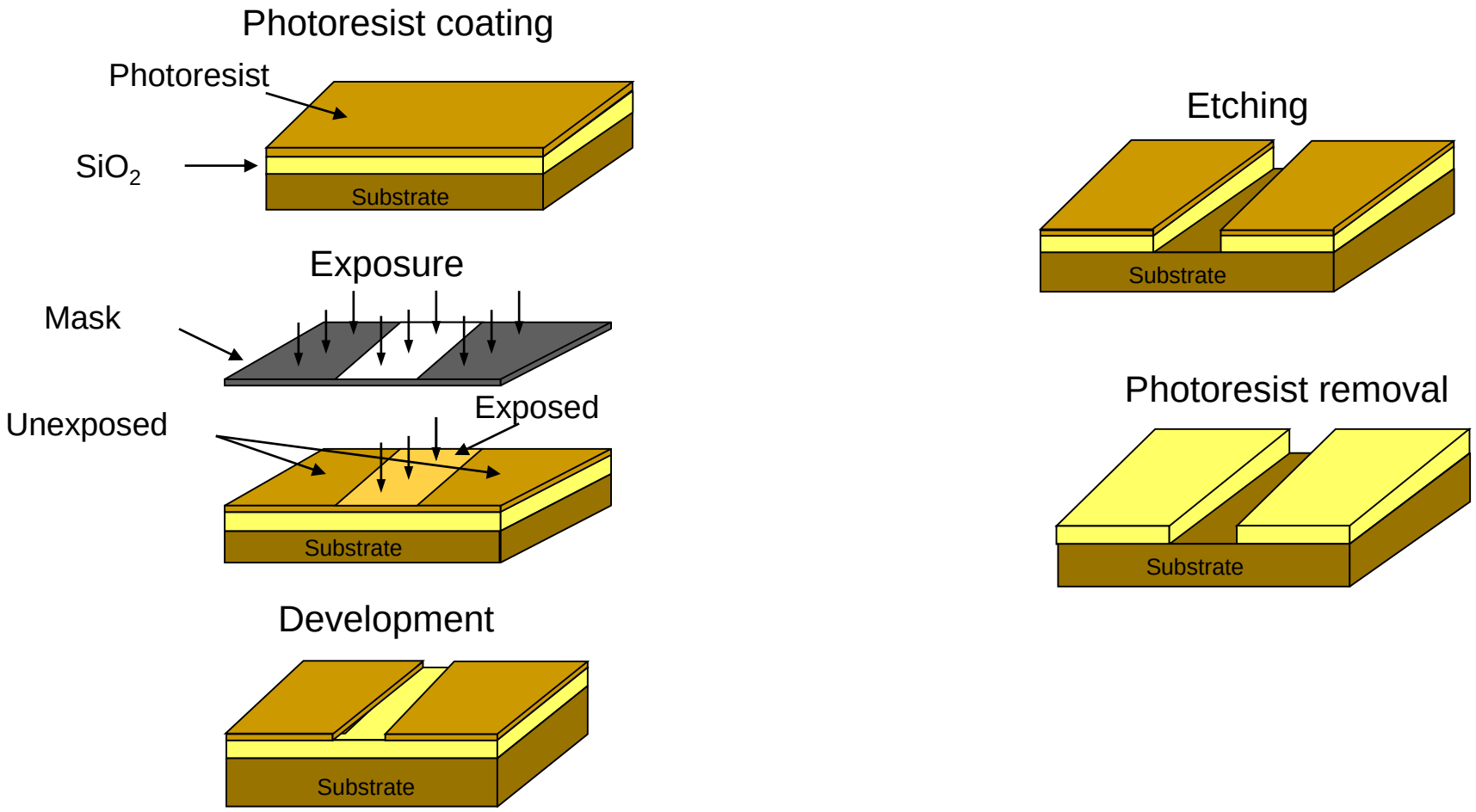
Photolitography Steps



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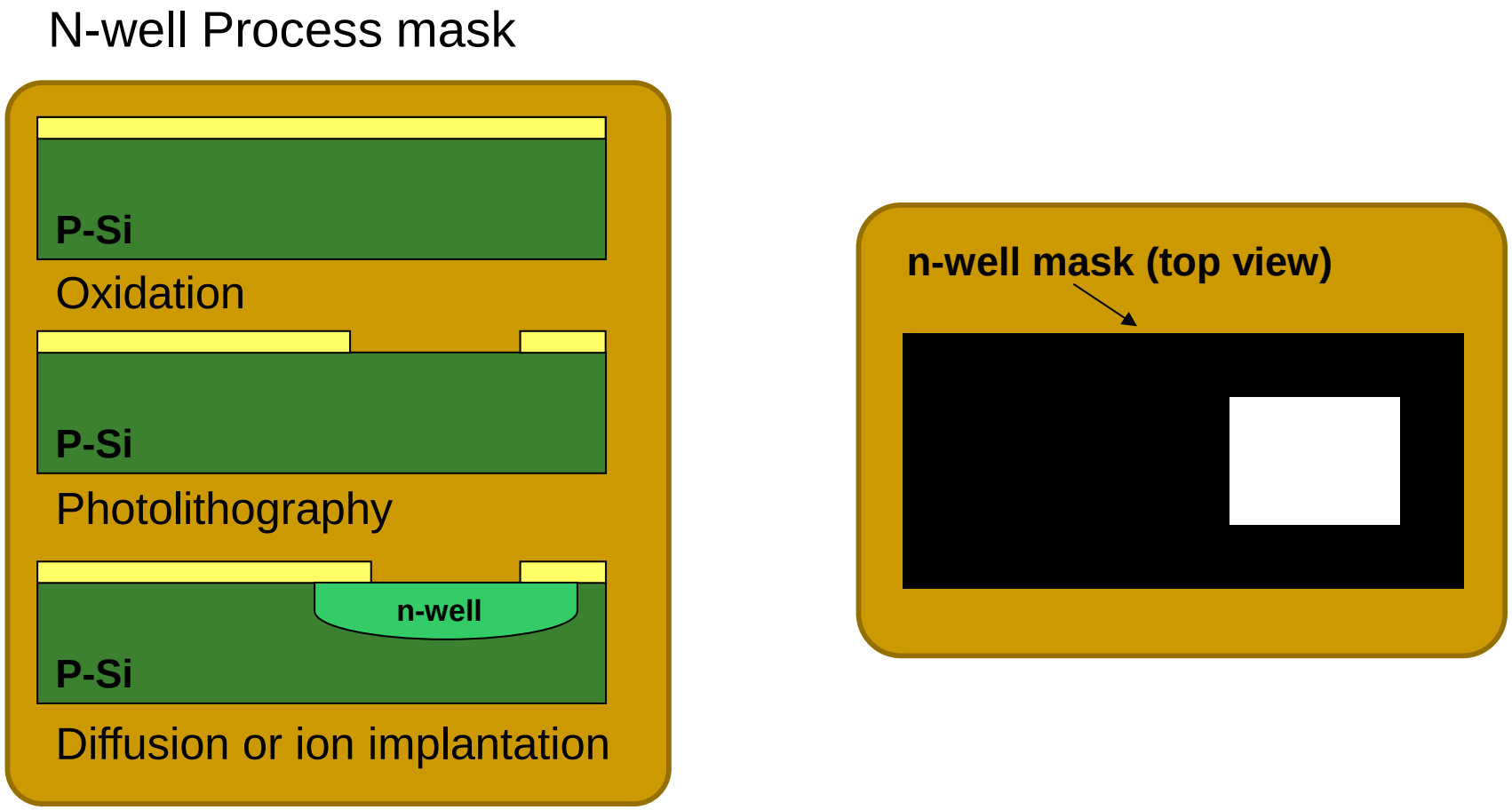
Mask Example (1)



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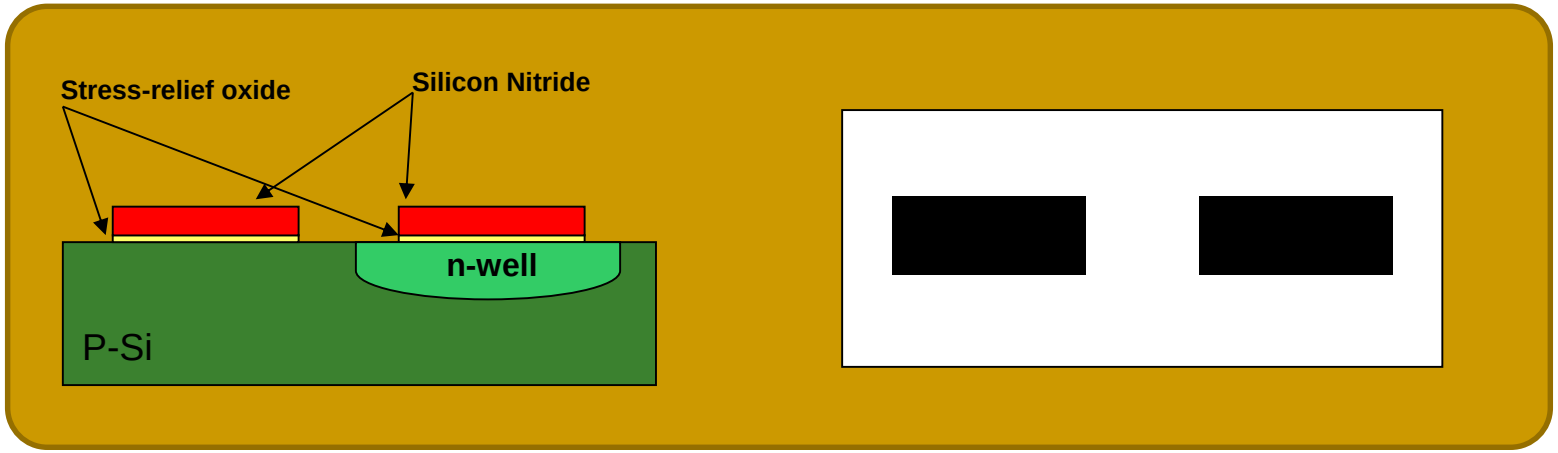
CMOS Fabrication Sequence (2)

- Active area definition
  - active area is a planar section of the surface
  - defines transistors regions
  - defines the n+ and p+ regions
  - defines the gate region



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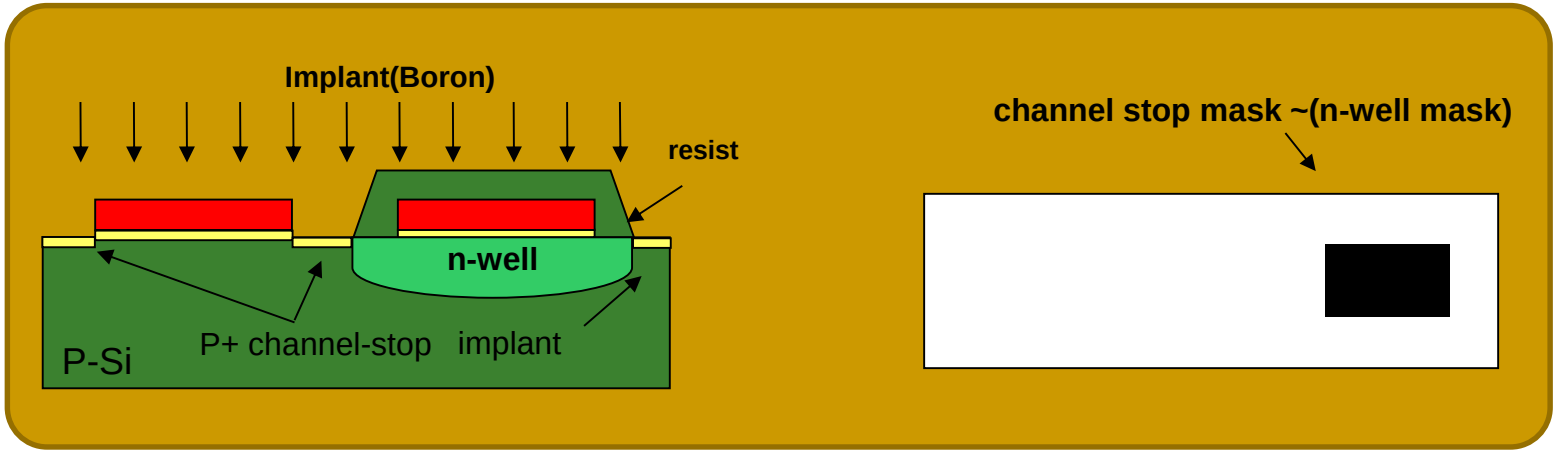
CMOS Fabrication Sequence (3)

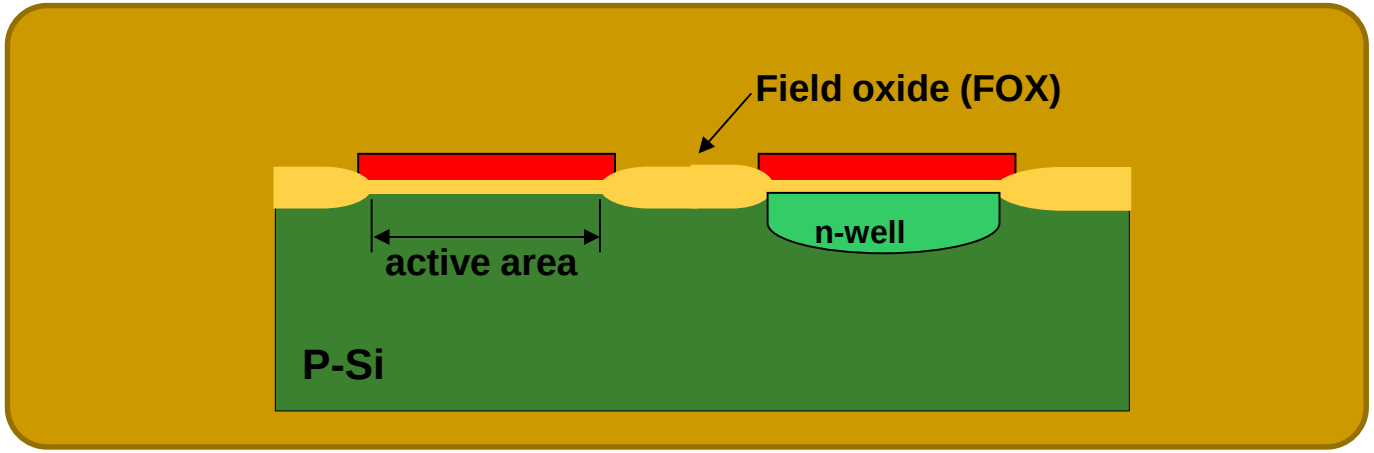
Channel-stop implant



Ion implantation

CMOS Fabrication Sequence (4)

LOCOS (Local oxidation of silicon)



Field oxide formation

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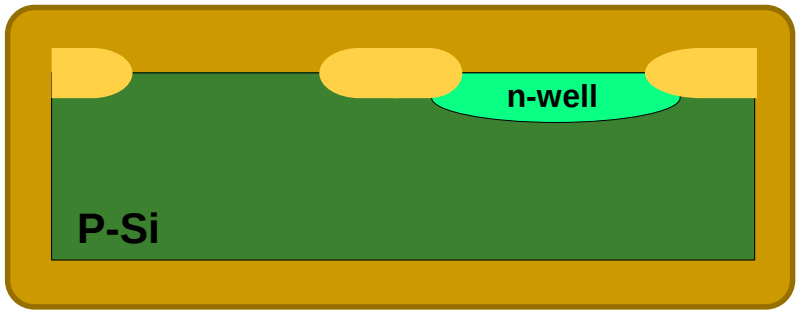
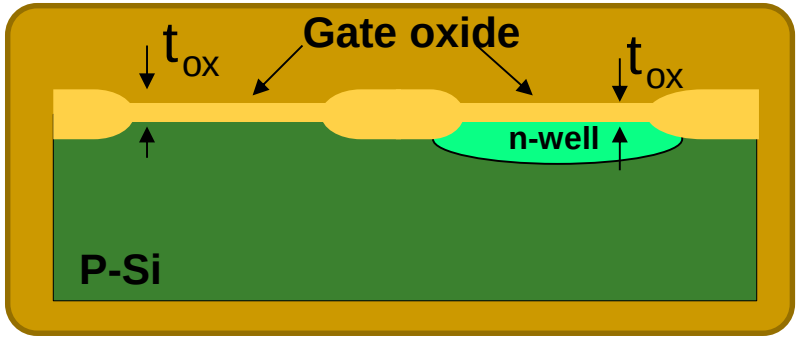
CMOS Fabrication Sequence (5)

Thin Gate Oxide Growth



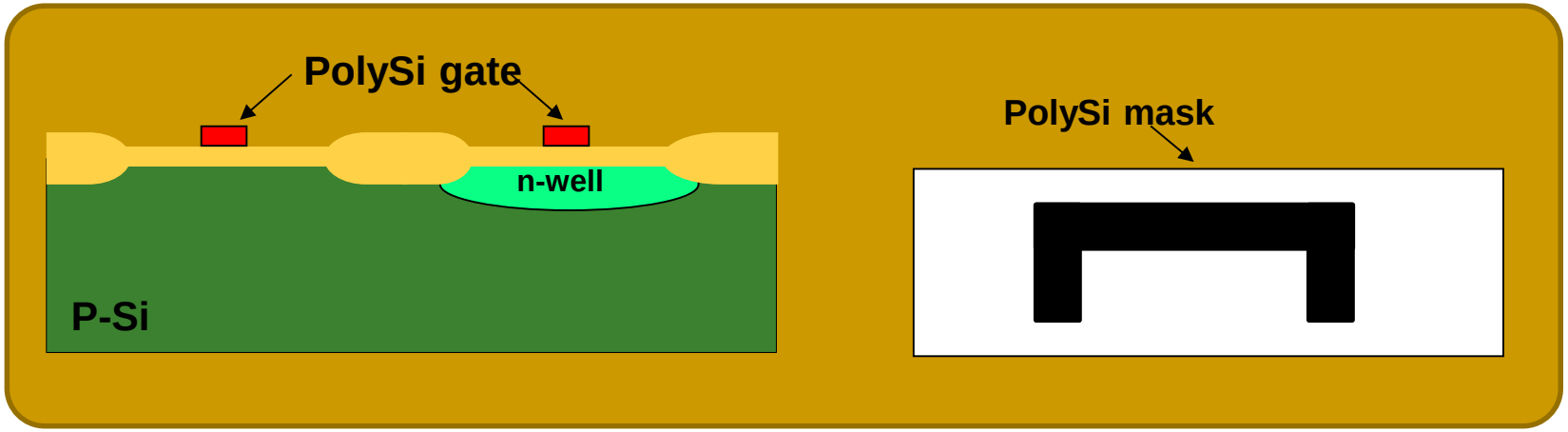
- The nitride and stress-relief oxide is removed.
- The threshold voltage is adjusted by ion implantation.



- Gate oxide growth, tox =50…2nm
- Thermal oxidation

CMOS Fabrication Sequence (6)

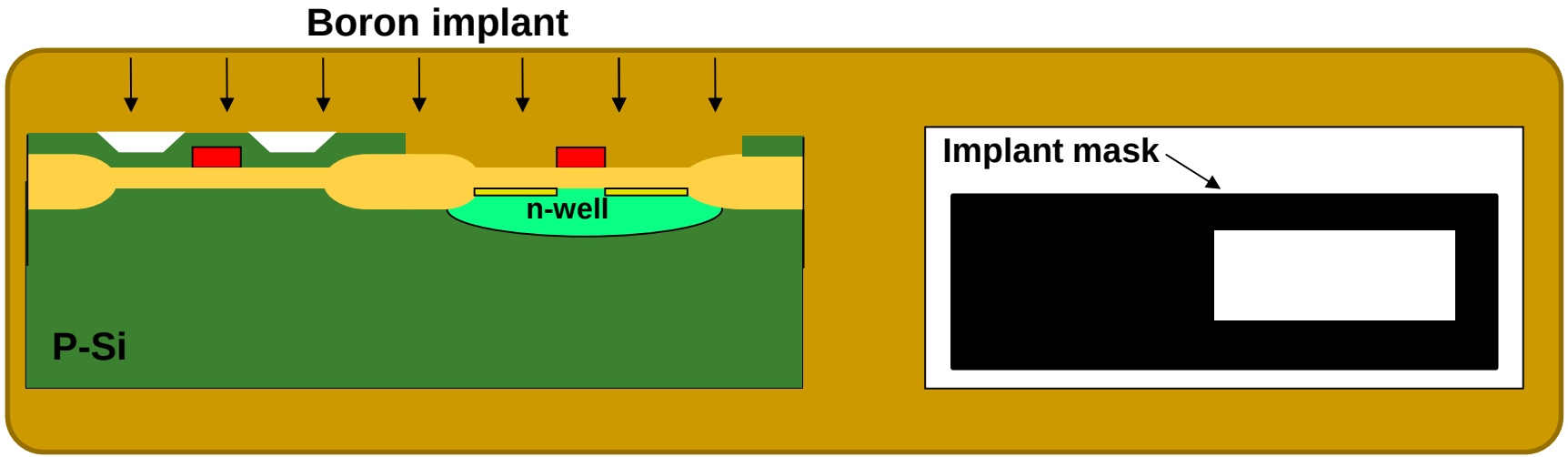
Polysilicon deposition and photolithography



All the gates are formed and doped (n+) by CVD technique in the single step.

CMOS Fabrication Sequence (7)

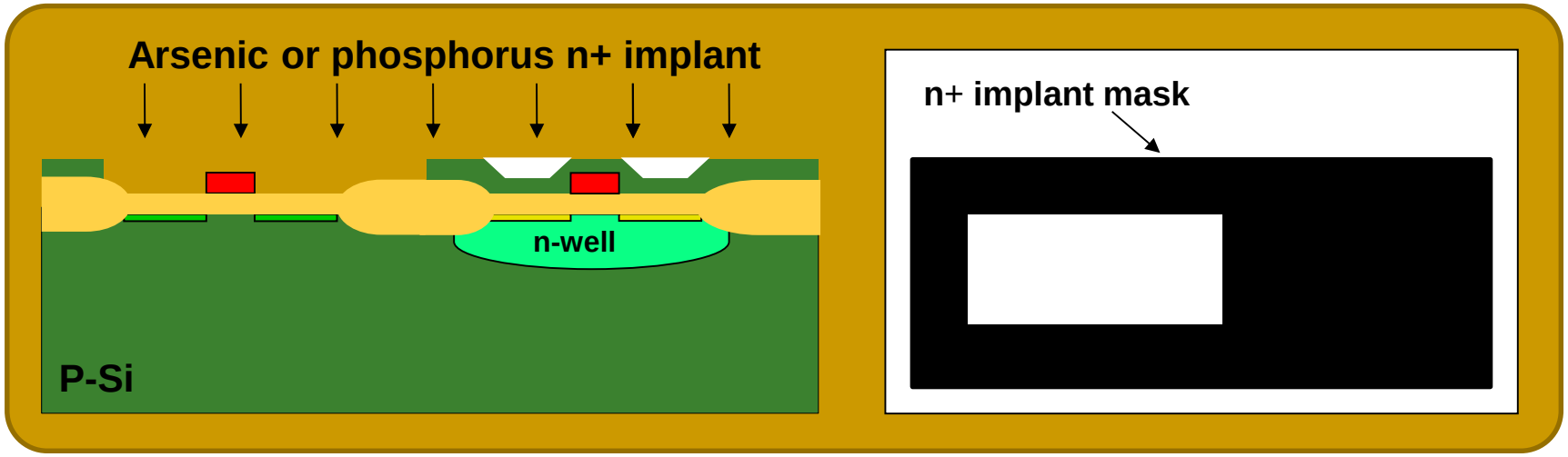
P-MOS Formation



Photolithography and boron ion implantation – Self aligned process

CMOS Fabrication Sequence (8)

N-MOS Formation

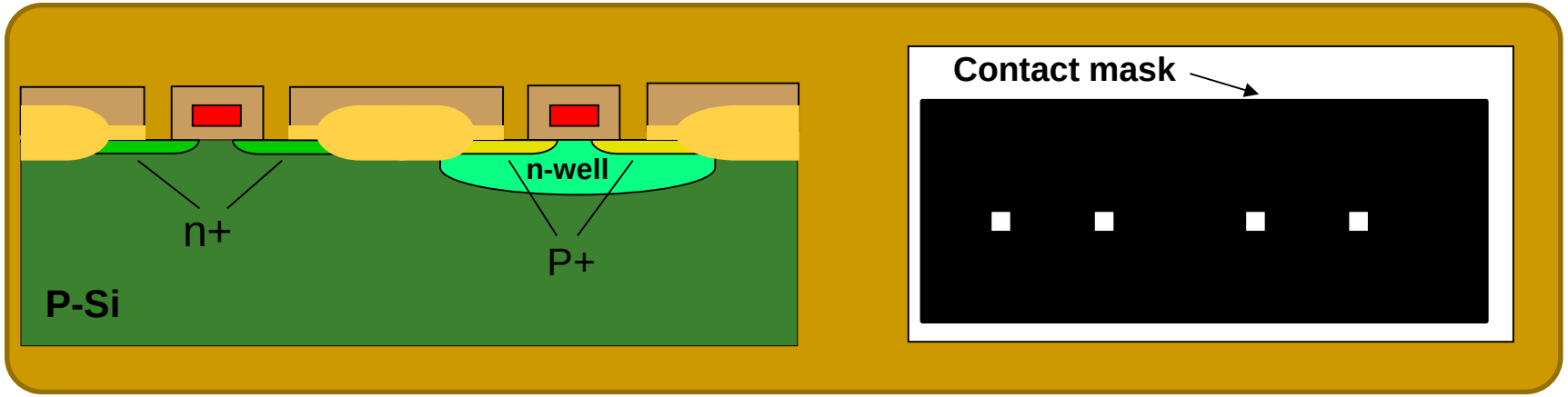


Photolithography and ion implantation – Self aligned process (n+ doped gate)

Thermal annealing cycle is performed.

CMOS Fabrication Sequence (9)

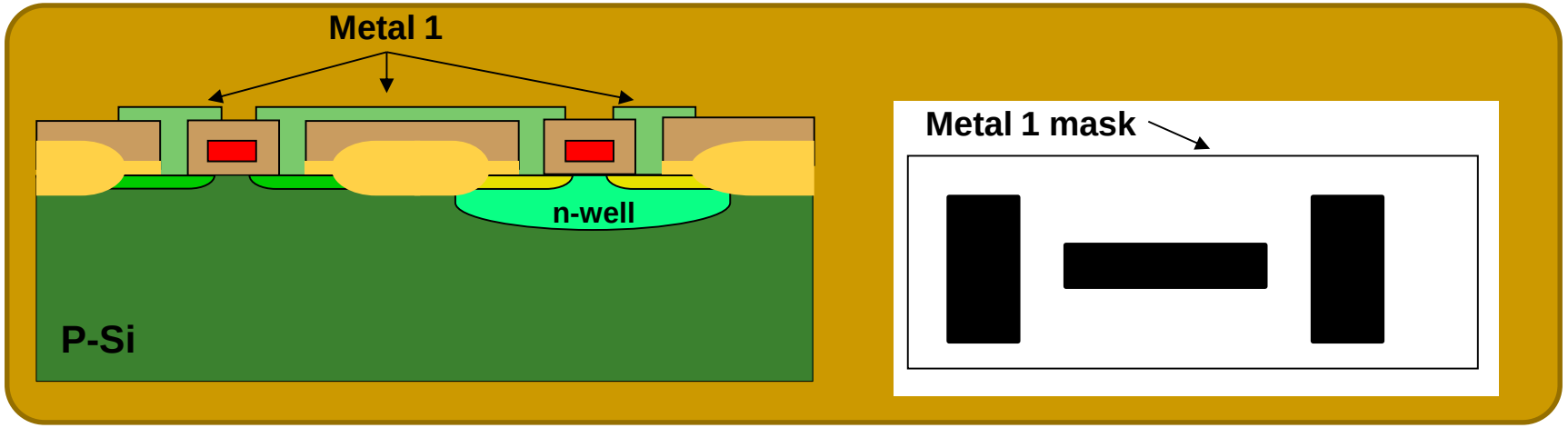
Contact cut formation



- Oxide deposition by low temperature CVD process.
- Photolithography and SiO2 etching.

CMOS Fabrication Sequence (10)

Contact formation



- Metal (Al or Cu) deposition and photolithography.
- Contacts and interconnects are formed.
- In just the same way the other metal layers are formed.
- After surface glass passivation and pad opening, the chips pass to the next step according to general IC fabrication flow.

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Digital Design Flow by Synopsys Tools

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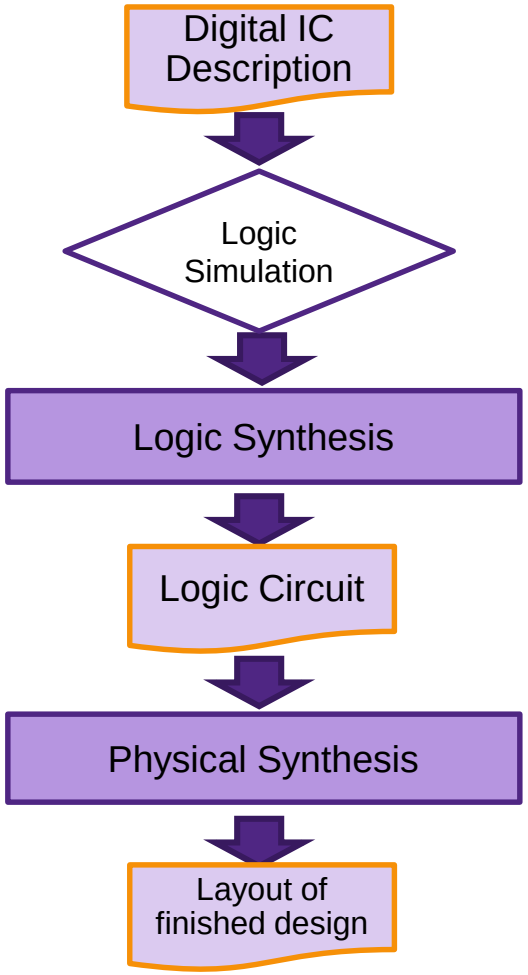
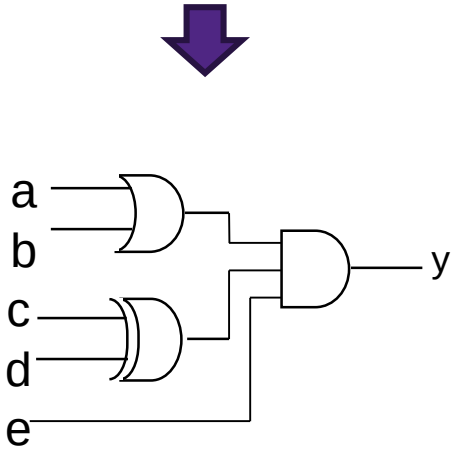
Basic Steps of Digital Design Flow

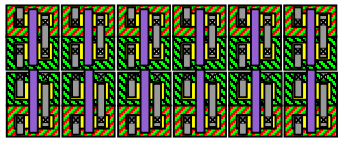
- Circuit design
  - –Based on specification, synthesize the netlist
- Physical design
  - –Based on the netlist, synthesize layout
- Verification
  - –Perform pre-layout and post-layout verification of IC performance

Basic Steps of Digital Design



y=(a+b)&(c⊕d)&e





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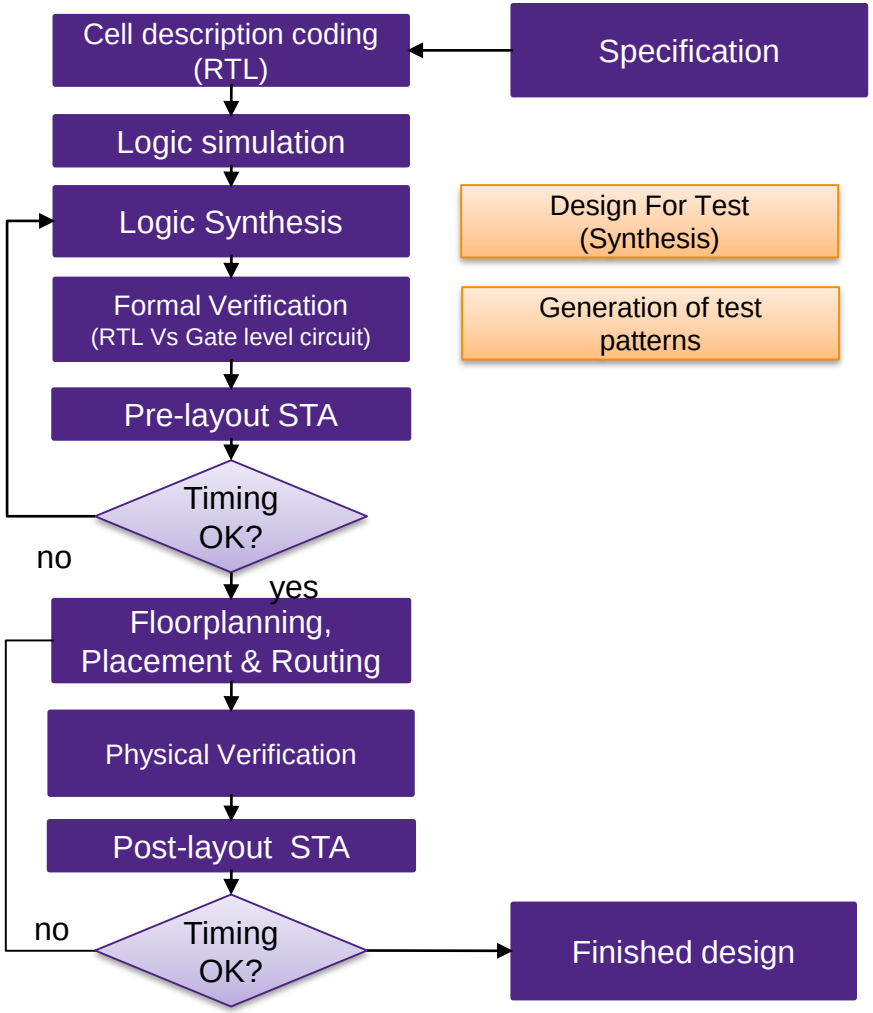
Digital Design Flow



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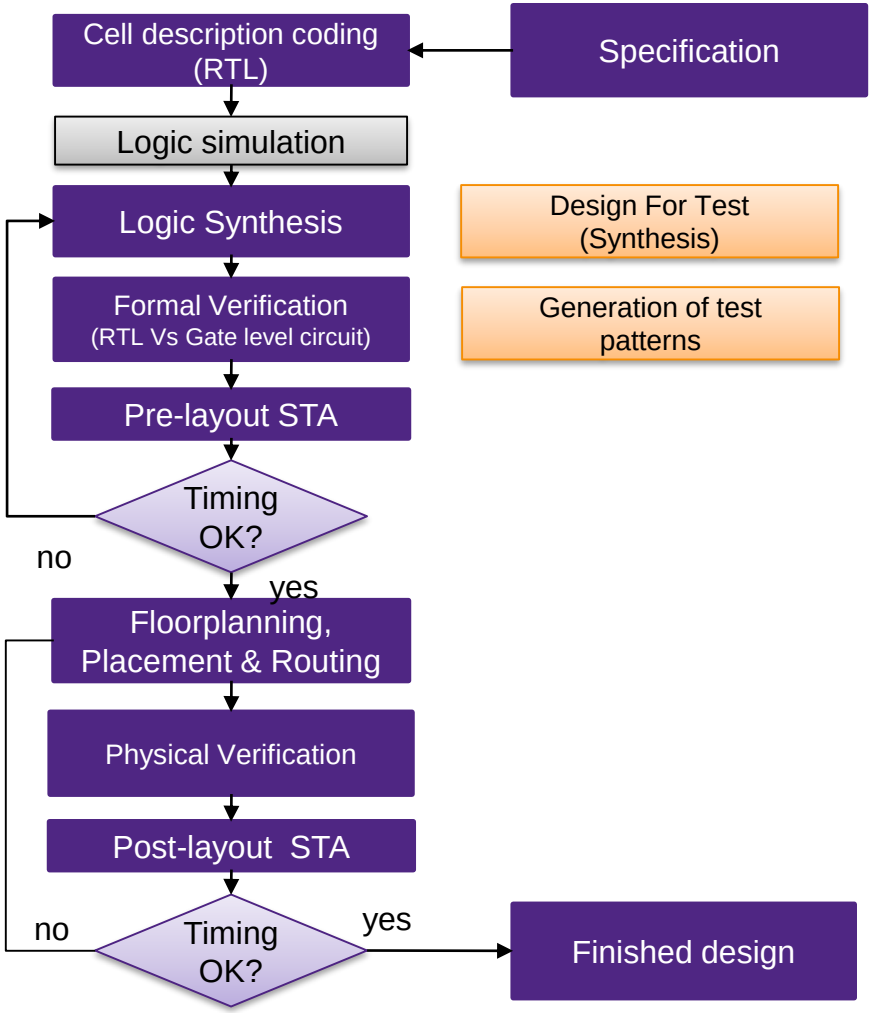
Digital IC Specification

- Description of Digital IC functionality
- With the help of Verilog or VHDL in the specification
- An example of specification line:
  - if incoming_call AND line_is_available then RING;
- The specifications of contemporary Digital IC can contain millions of lines, can be created by a collective of numerous participants within a few months

Verilog Description Example *(8-bit counter)*

```
module counter(out, reset, clock);

output   [7:0] out;
input    clock, reset;
reg  [7:0] out;

always @(posedge clock or posedge resetn)

    if (resetn)
        out  = 0;
    else
        out = out + 1;

endmodule
```


Digital Design Flow



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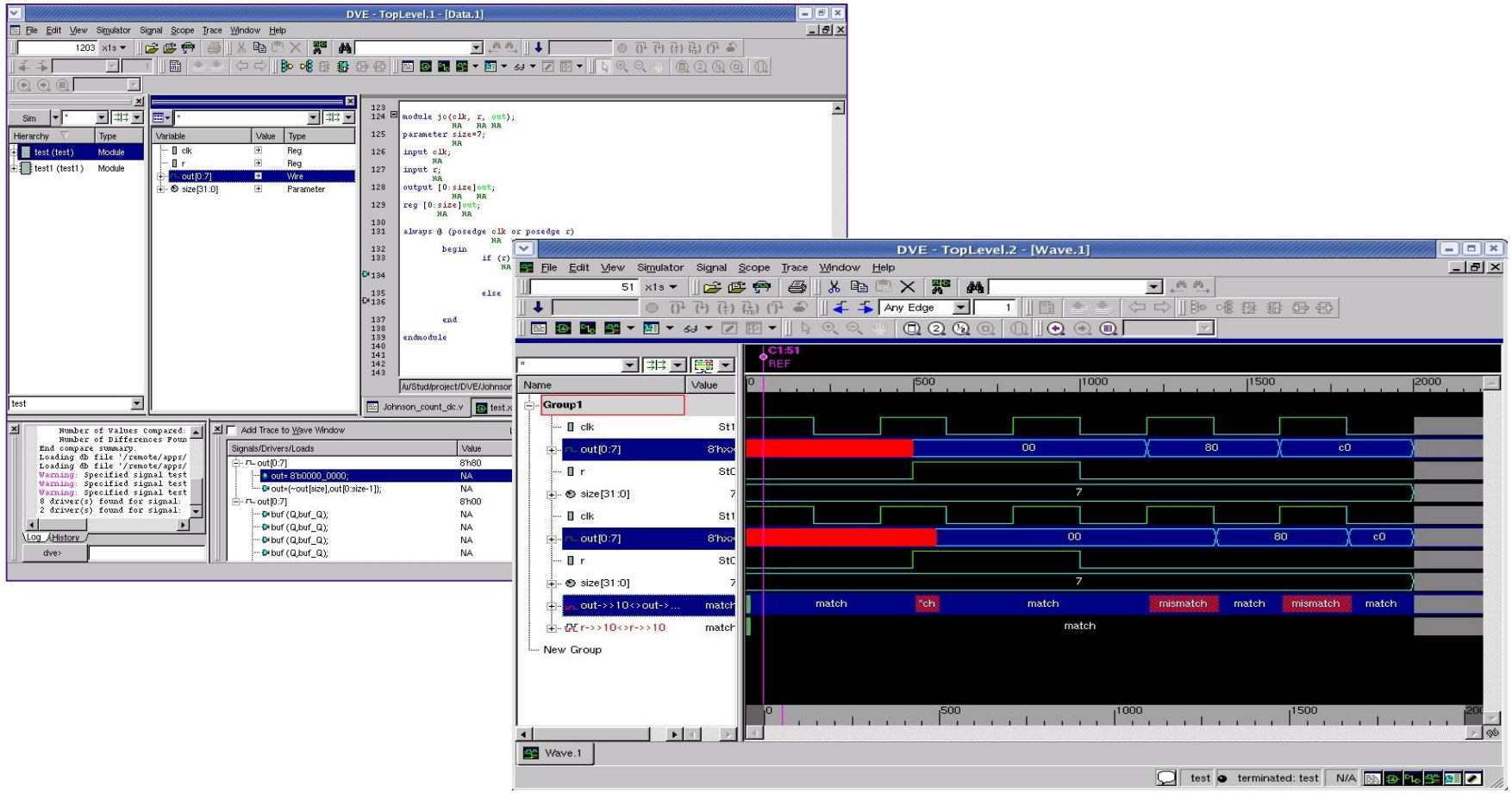
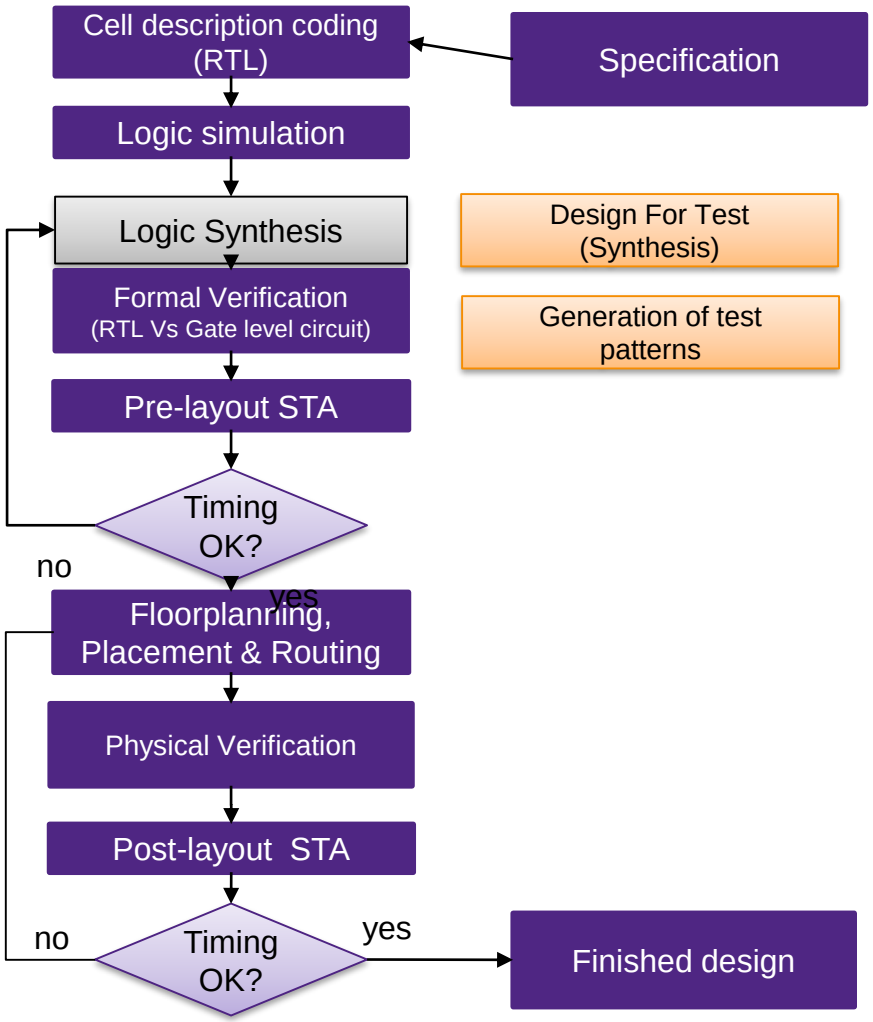
Logic Simulation



Digital Design Flow



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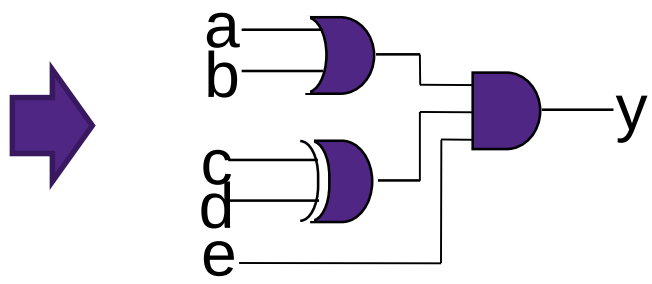
Logic Synthesis

- Synthesis
  - The process which converts an abstract form of desired circuit behavior into a design implementation in terms of logic gates
- Optimization
  - Changing design to achieve design goal (required by specification)

Concept of Automated Design

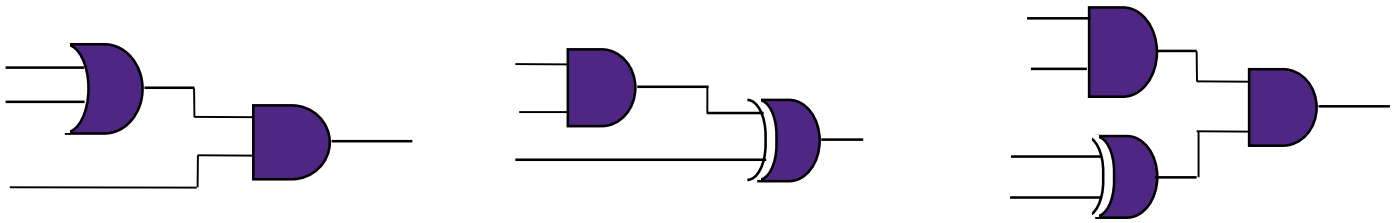
Any digital function can be easily converted to a logic circuit. Synthesis tool uses this to automatically synthesize circuit from functional description.

Y=(a+b)&(c⊕d)&e

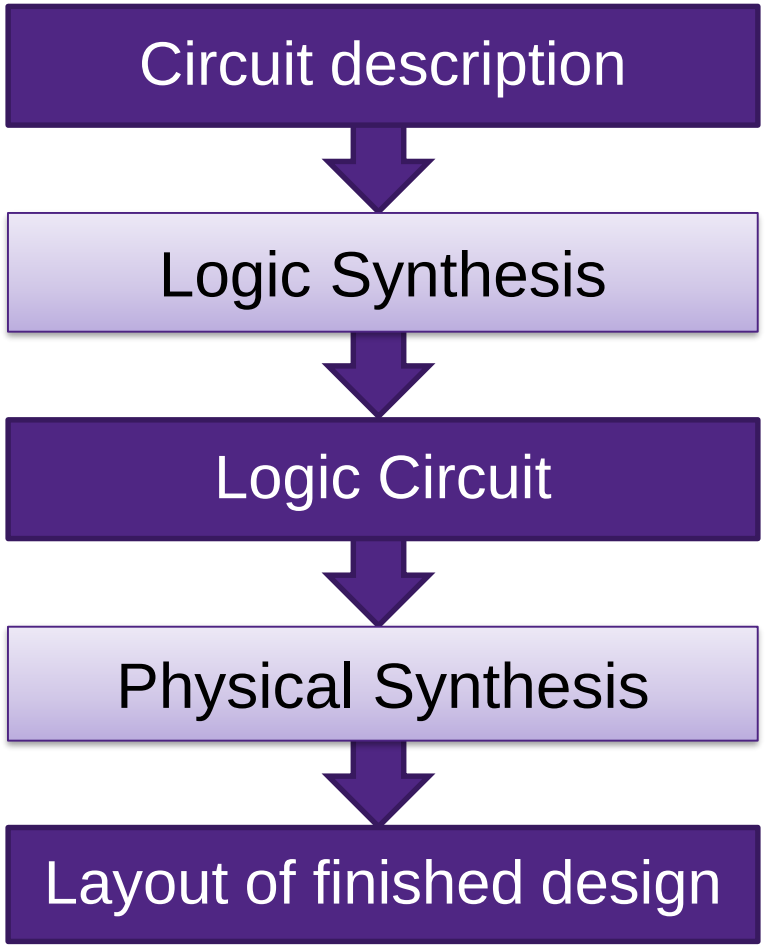


Concept of Automated Design (2)

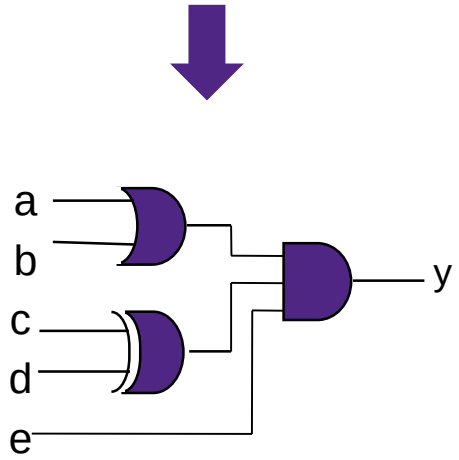
- If primitive (standard) cells are previously designed, large number of various digital circuits can be built using these parts

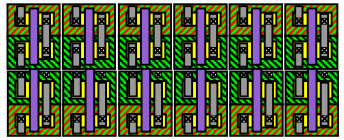


Basic Steps of Synthesis



y=(a+b)&(c⊕d)&e





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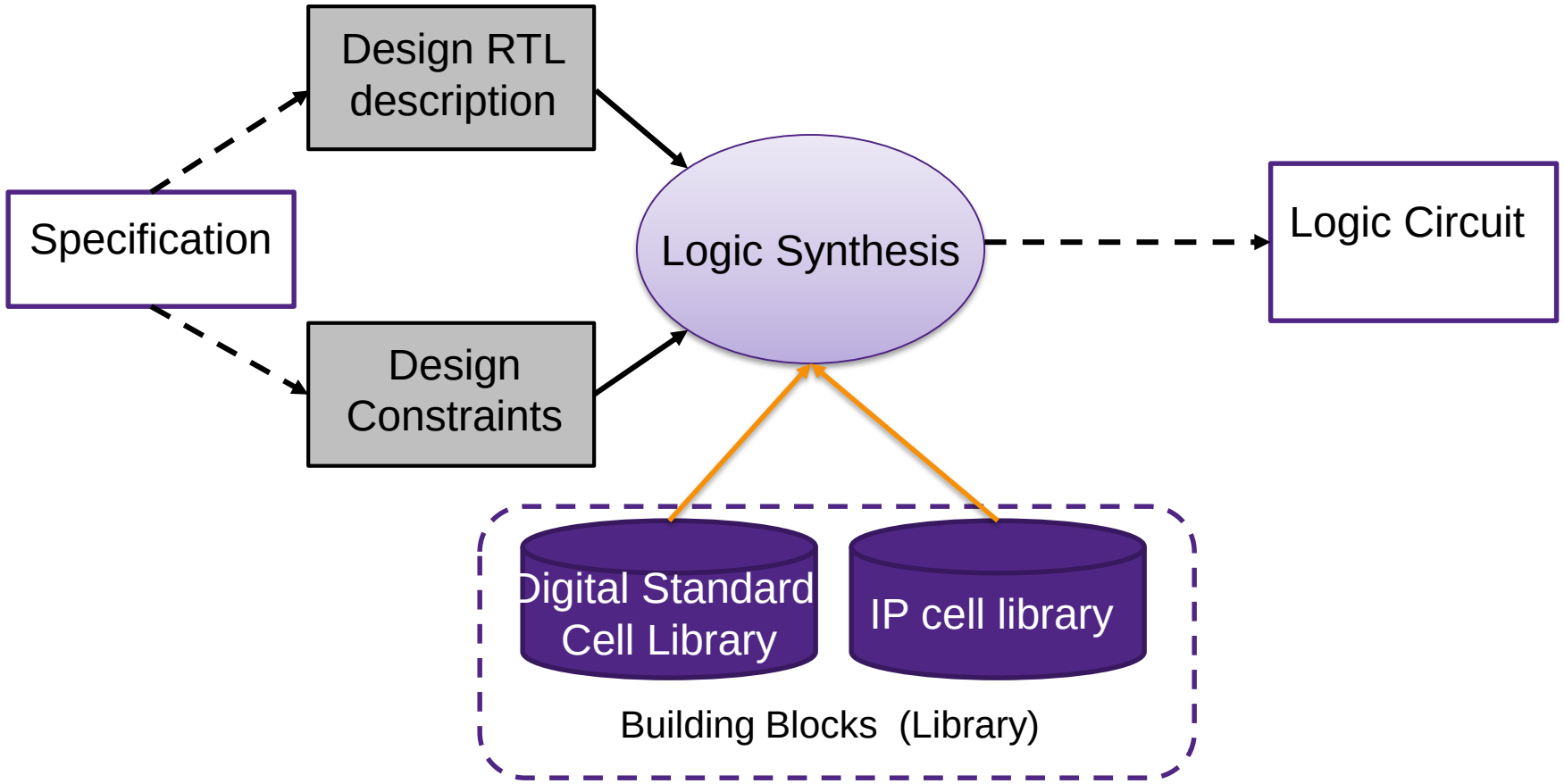
Logic Synthesis



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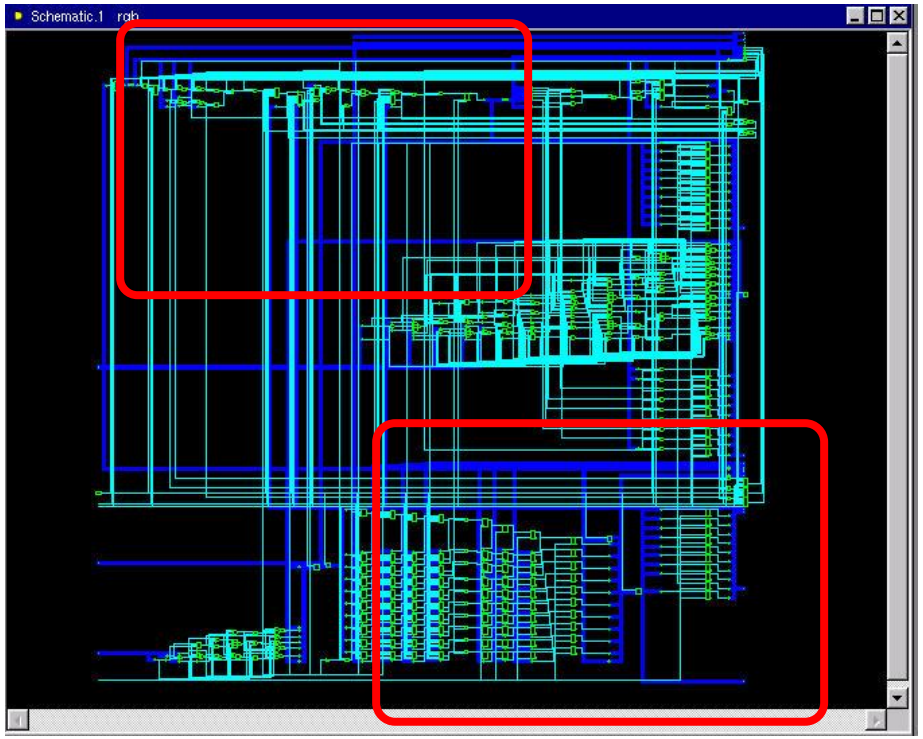
Logic Circuit

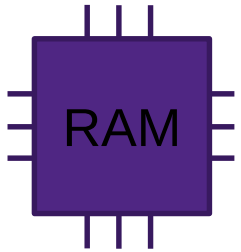
Digital standard cells



Intellectual property (IP) block

Final logic circuit consists of digital standard cells and Intellectual Property (IP) blocks.

Digital Standard Cell Library and IP cell library should be given as input to synthesis to be used as building blocks.



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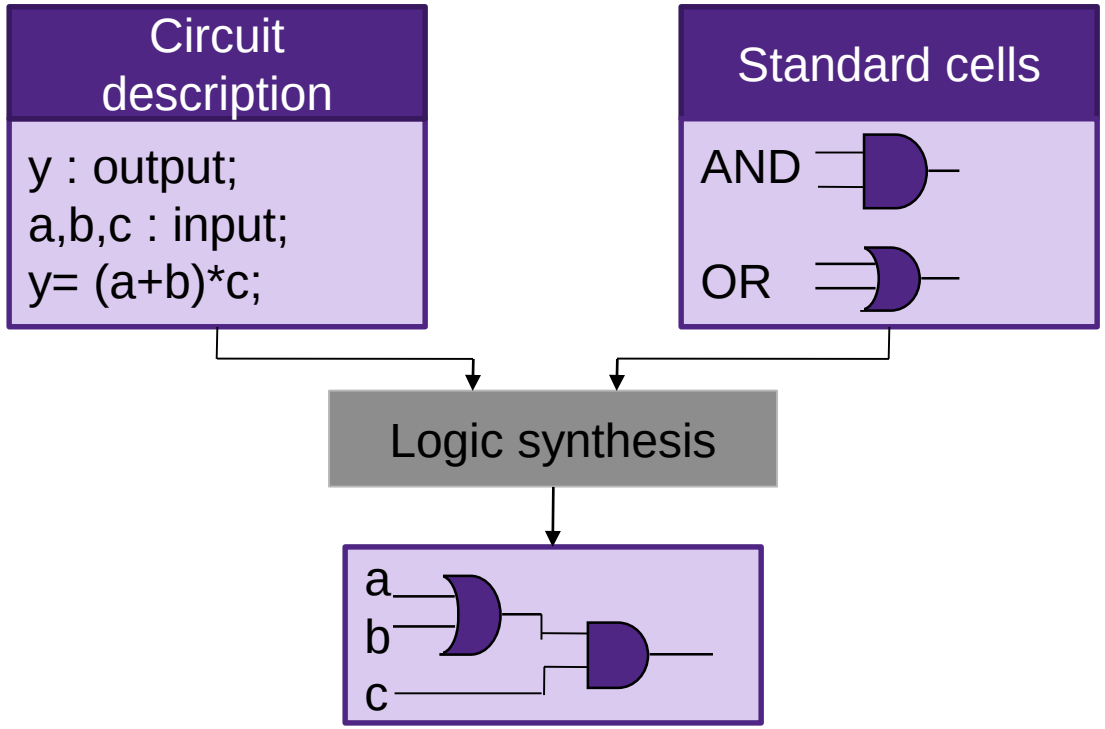
Logic Synthesis

Logic synthesis is the process which produces logic circuit from circuit description



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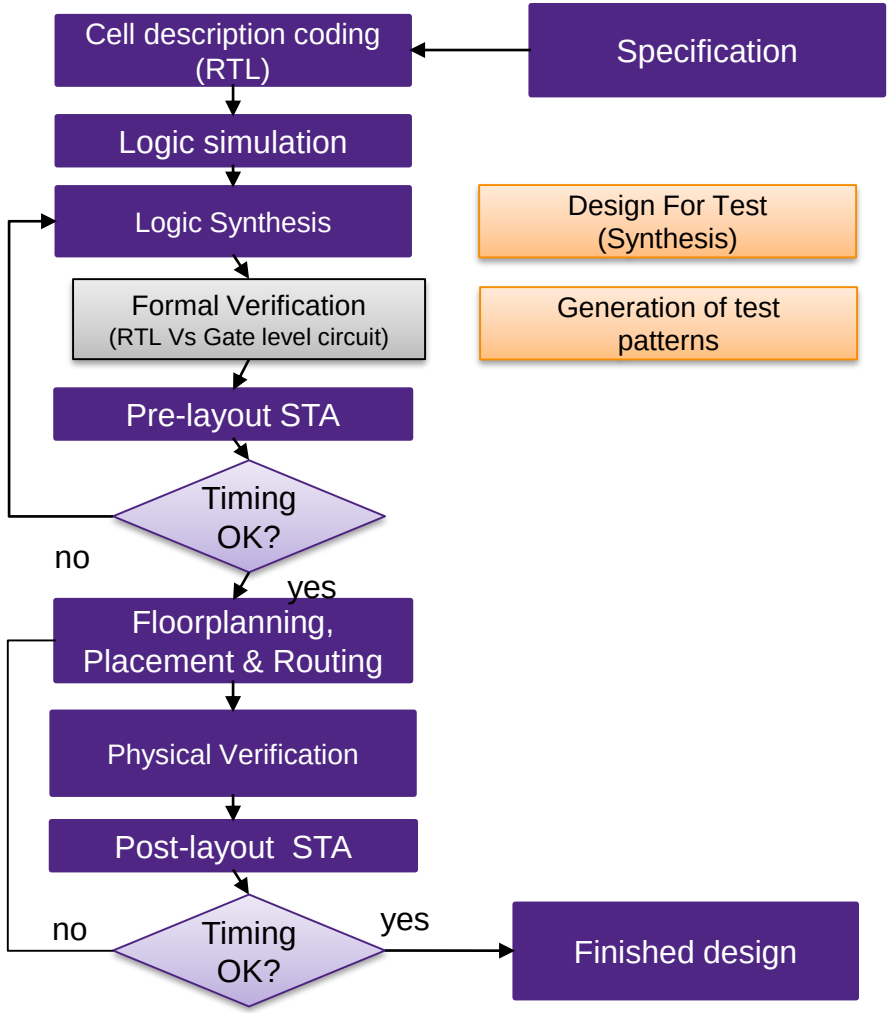
Digital Design Flow



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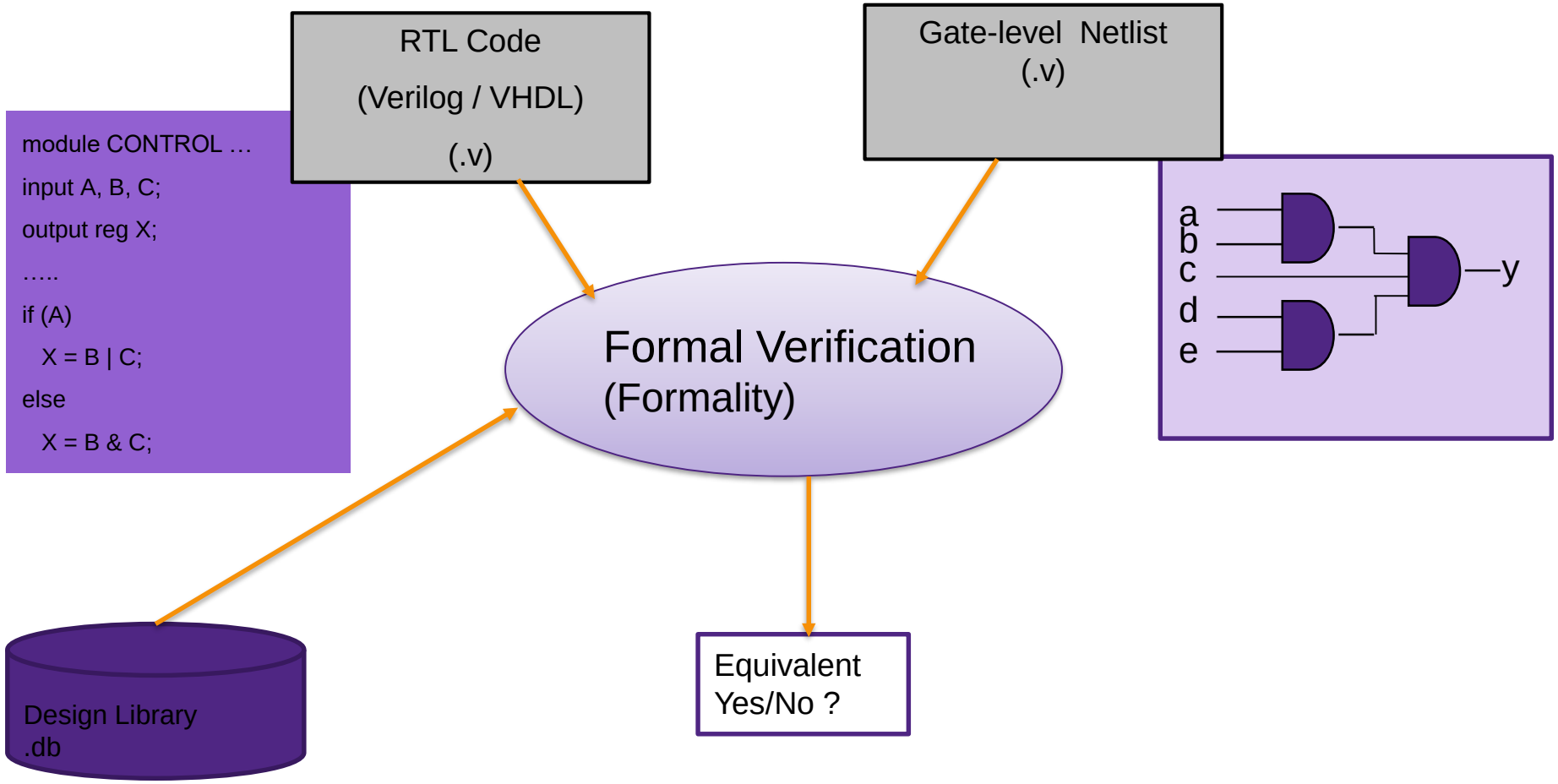
Formal Verification



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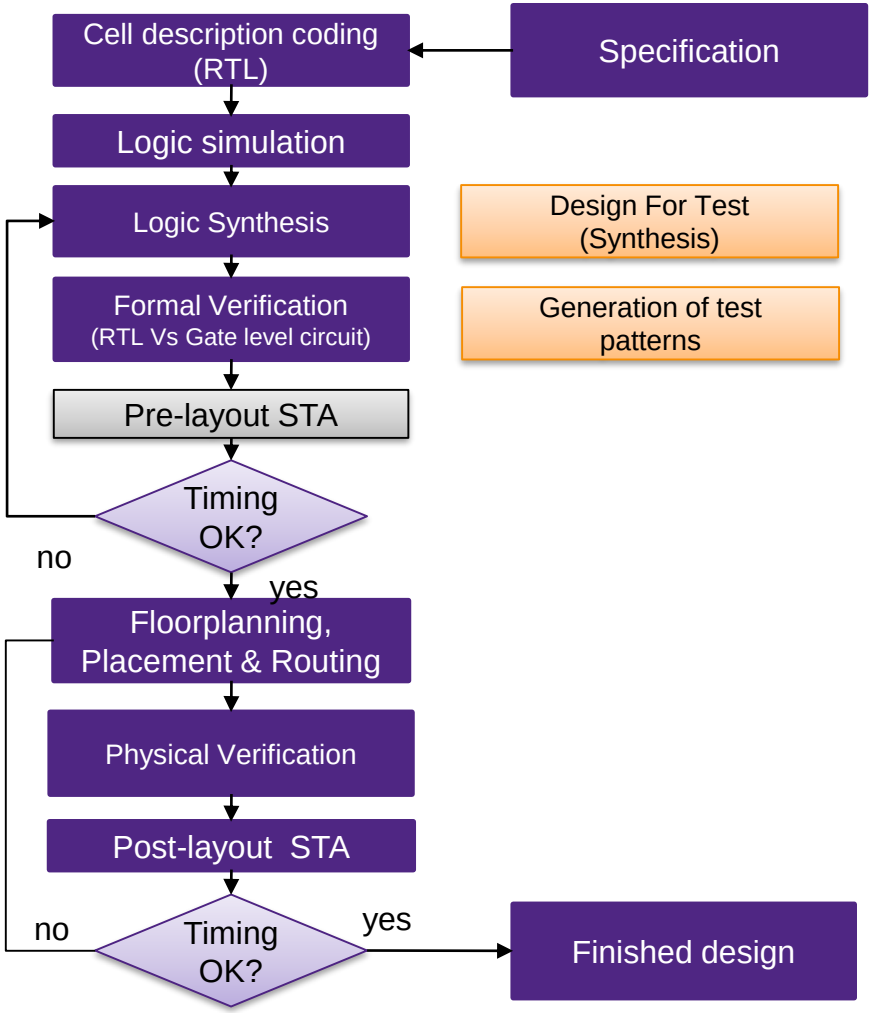
Formal Verification (2)

- Checks whether two designs are functionally equivalent or not
- Its purpose is to detect unexpected differences that may have been introduced into a design during development

Digital Design Flow



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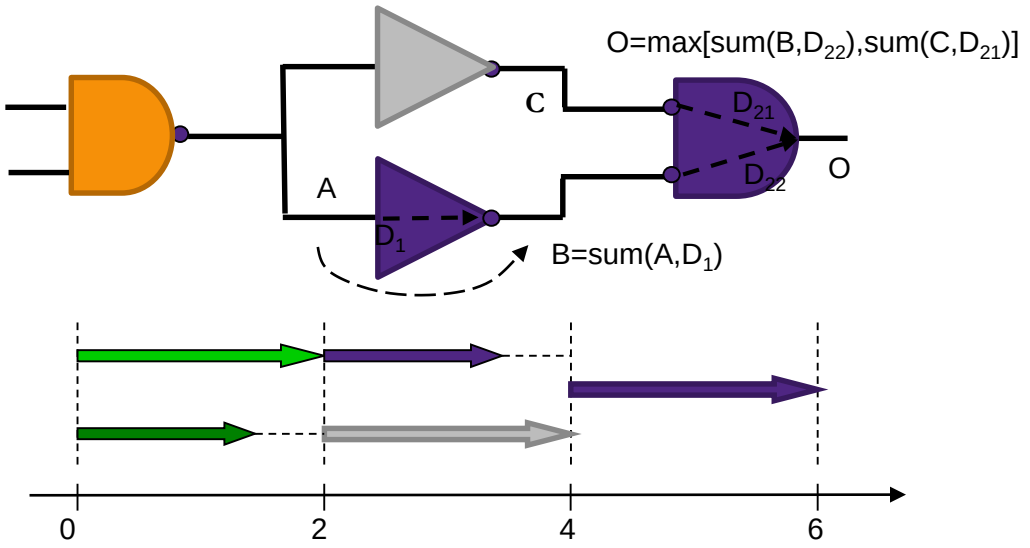
Static Timing Analysis (STA)

The arrival time at the input is propagated through the gates at each level till it reaches the output



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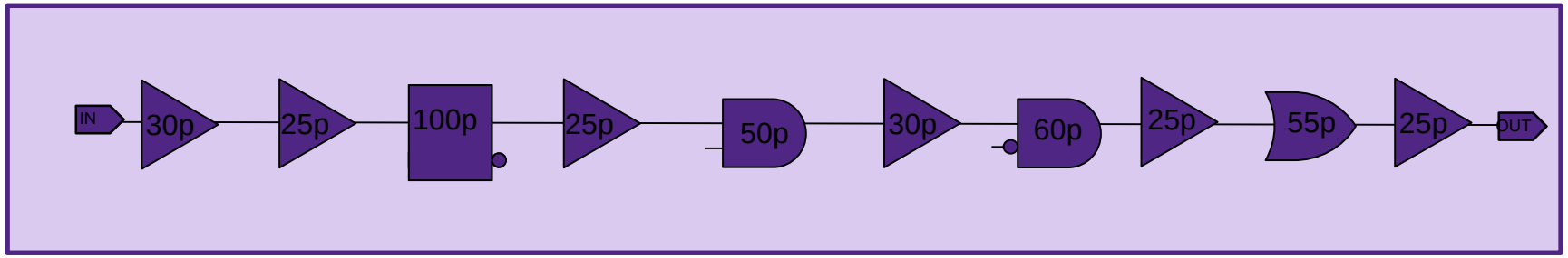
Example

- Static Timing Analysis (STA) is a method of computing the expected timing of a digital circuit without requiring simulation



Delay=30p+25p+100p+25p+50p+30p+60p+25p+55p+25p=425p

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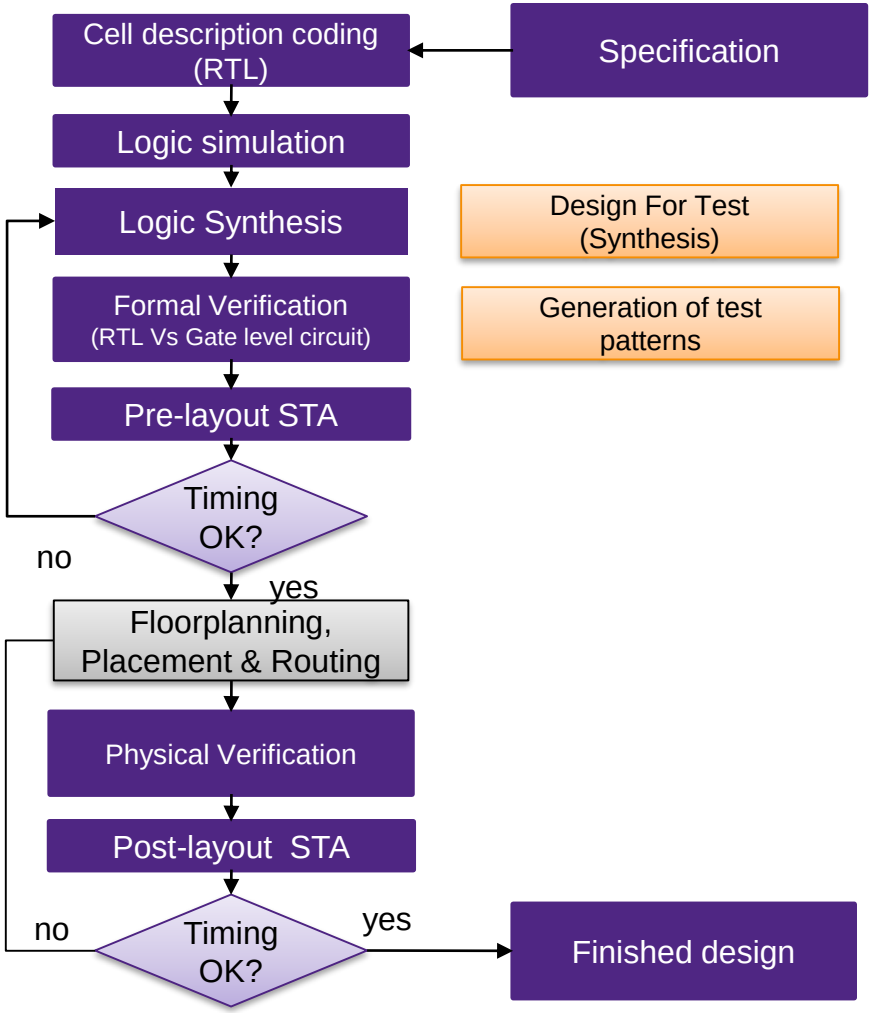
Digital Design Flow



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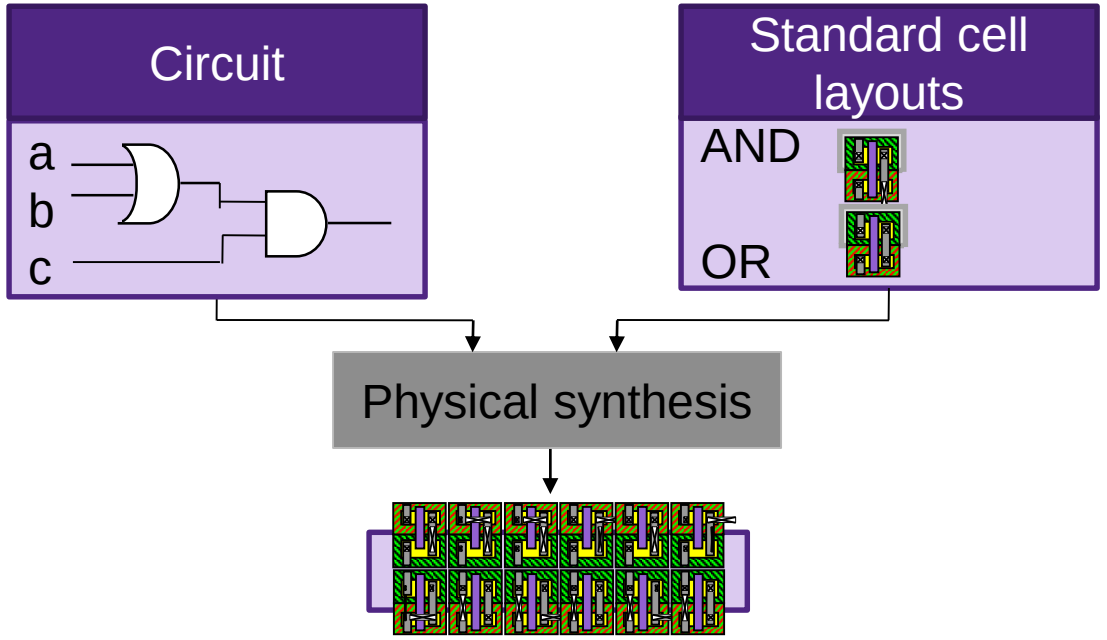
Physical Synthesis

Physical synthesis is the process that produces layout of logic circuit.



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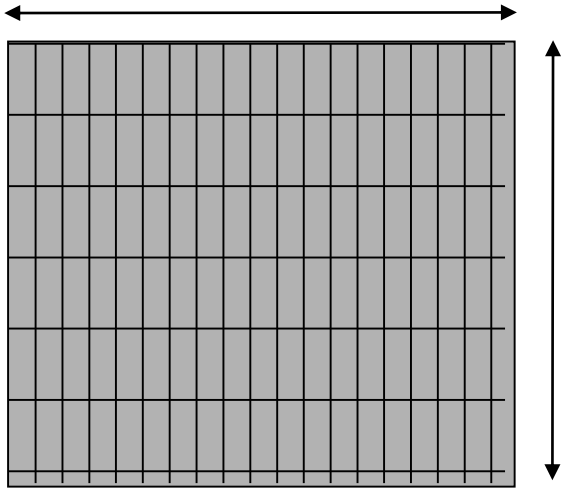
Physical Synthesis Steps

- Floorplanning
- Placement
- Routing

Floorplanning

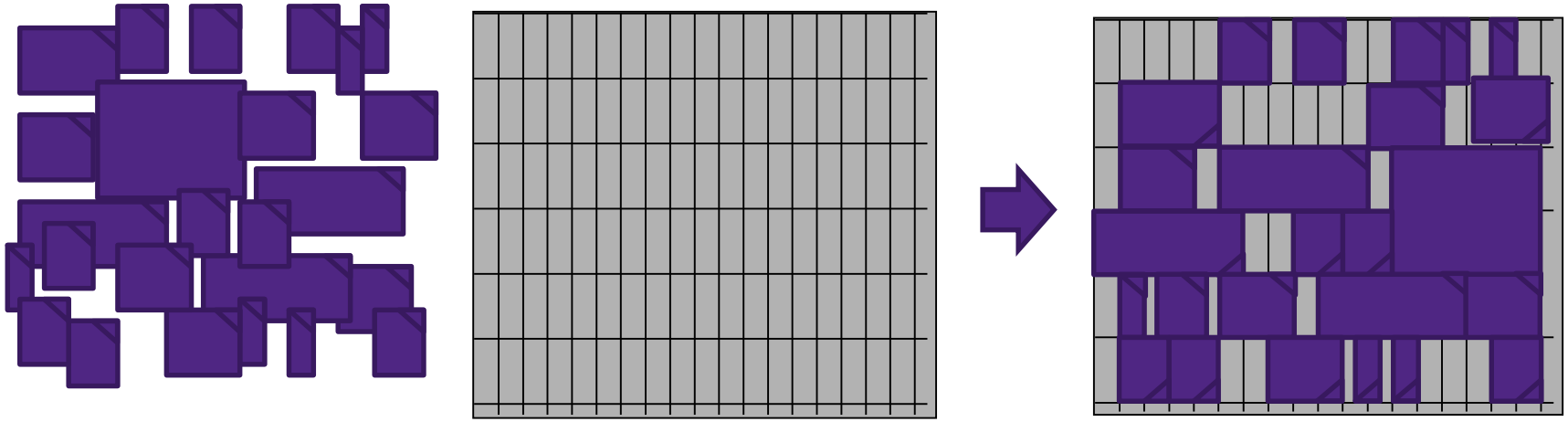
During the floorplanning step the overall cell is defined, including: cell size, supply network, etc.



Floorplan

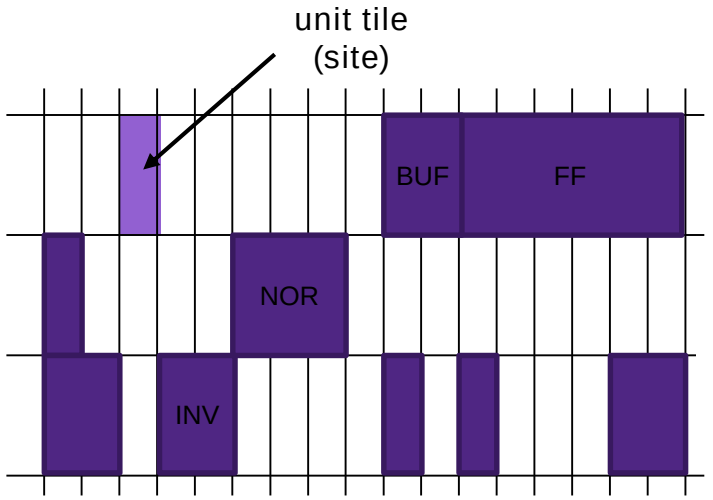
Placement

- Placement – exact placement of modules (modules can be standard cells, IPs).
- The goal is to minimize the total area and interconnect length



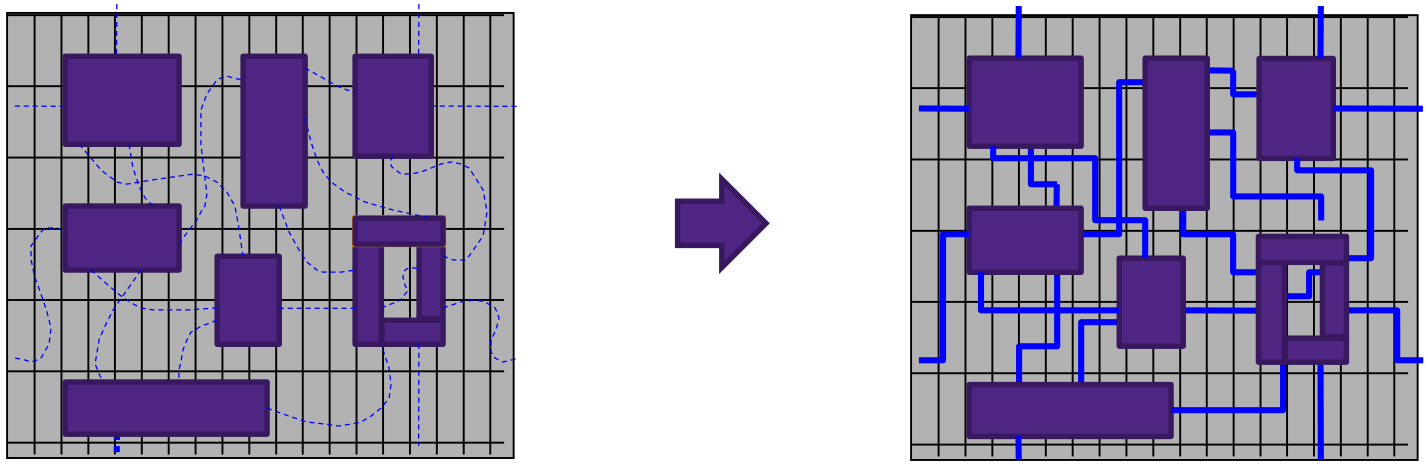
Unit Tile

- Placement uses grid in which cells are placed
- Floorplaning uses ‘unit tile’ cell to build this grid
  - Unit tile is defined by a library developer
  - All the cells in the library are designed to be multiple to unit tile



Routing

- Routing connects placed cells according to schematic
- The goal is minimal impact of interconnects on circuit operation



Placed design

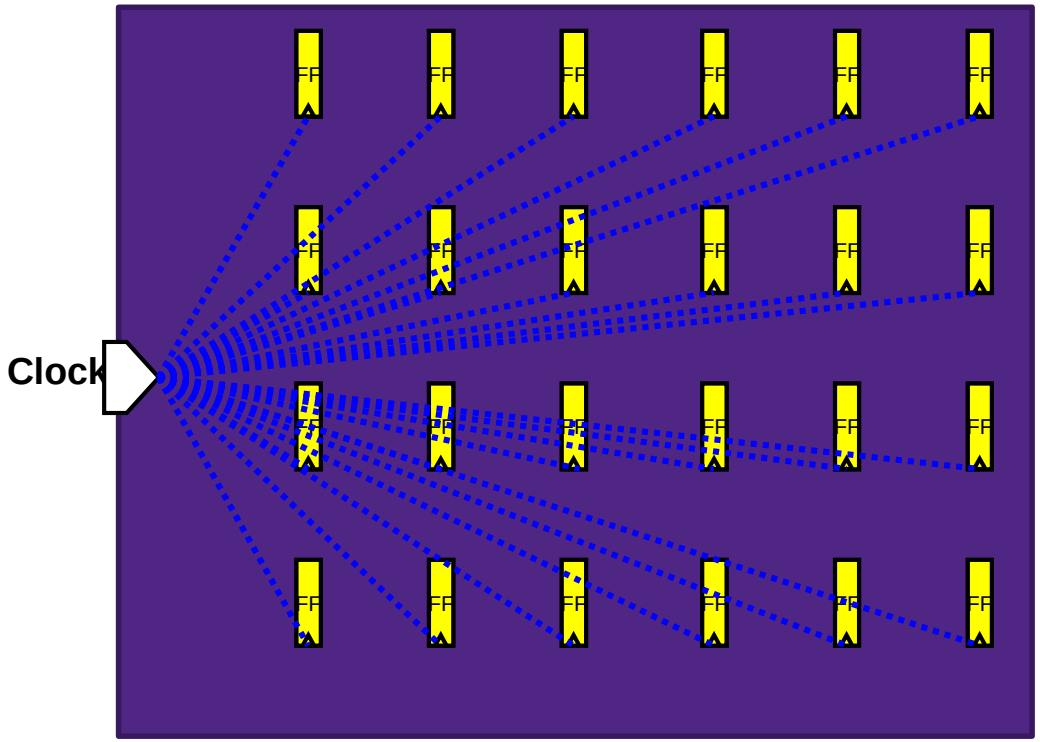
Routed design

Circuit Optimization During Physical Synthesis

- Physical synthesis not only places and routes the cells of a circuit but also optimizes the cell as required by the designer
- Optimizations
  - Area
  - Interconnect length
  - Power density
  - Clock distribution
  - etc.

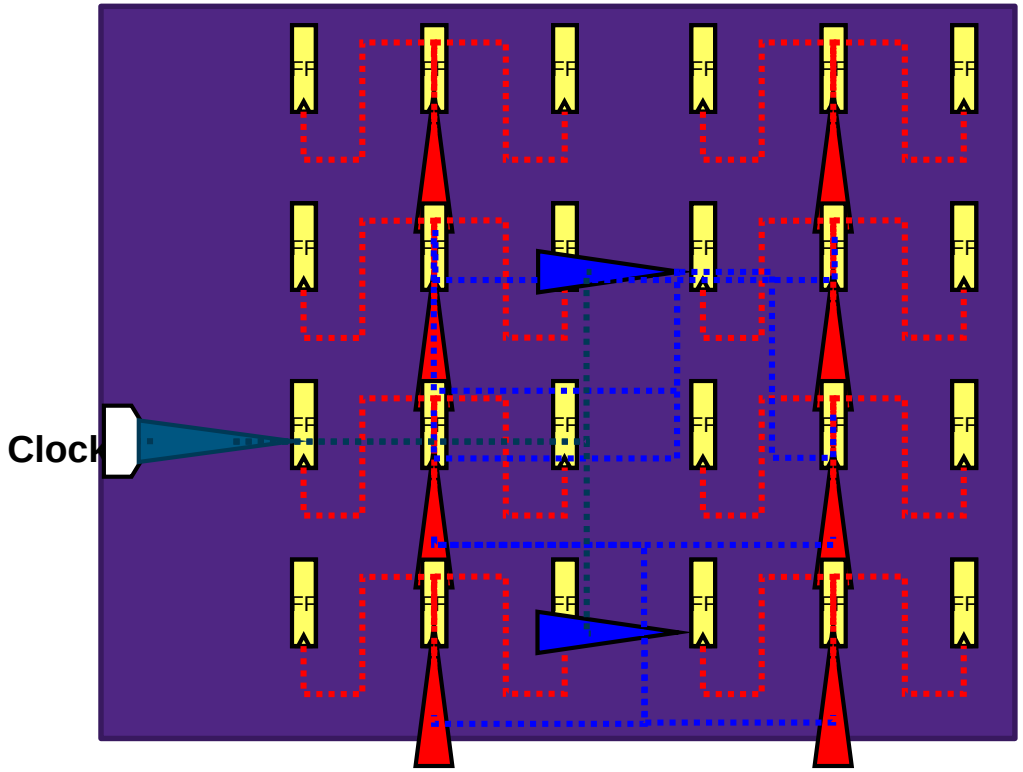
Physical Synthesis Circuit Optimization Example: Clock Delay Problems

- All clock pins are driven by a single clock source



Physical Synthesis Circuit Optimization Example: Clock Tree Synthesis

- A buffer tree is built to balance the loads and minimize the delays



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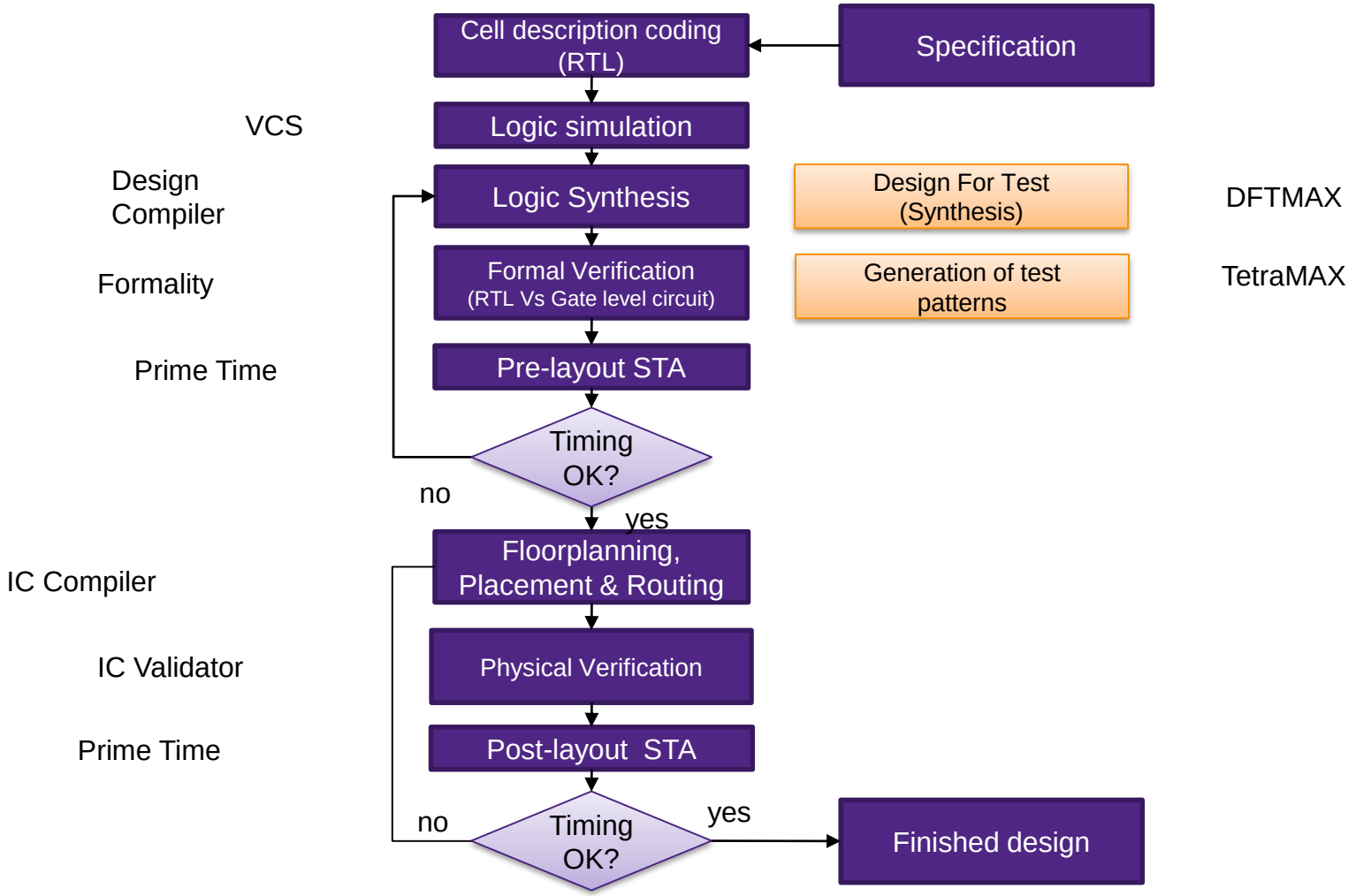
Digital Design Toolchain



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New Challenges to IC Design Flow

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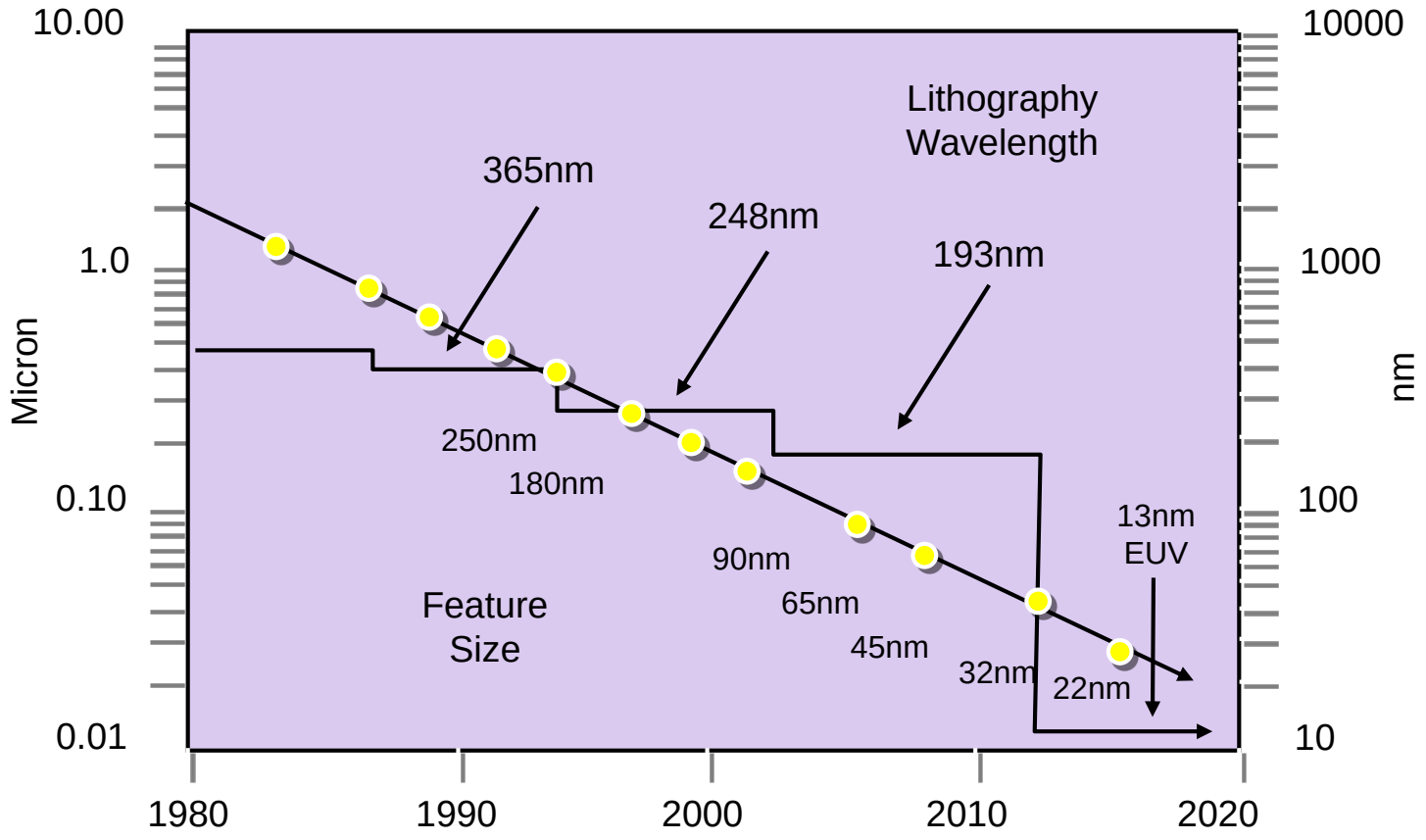
Litography Trends



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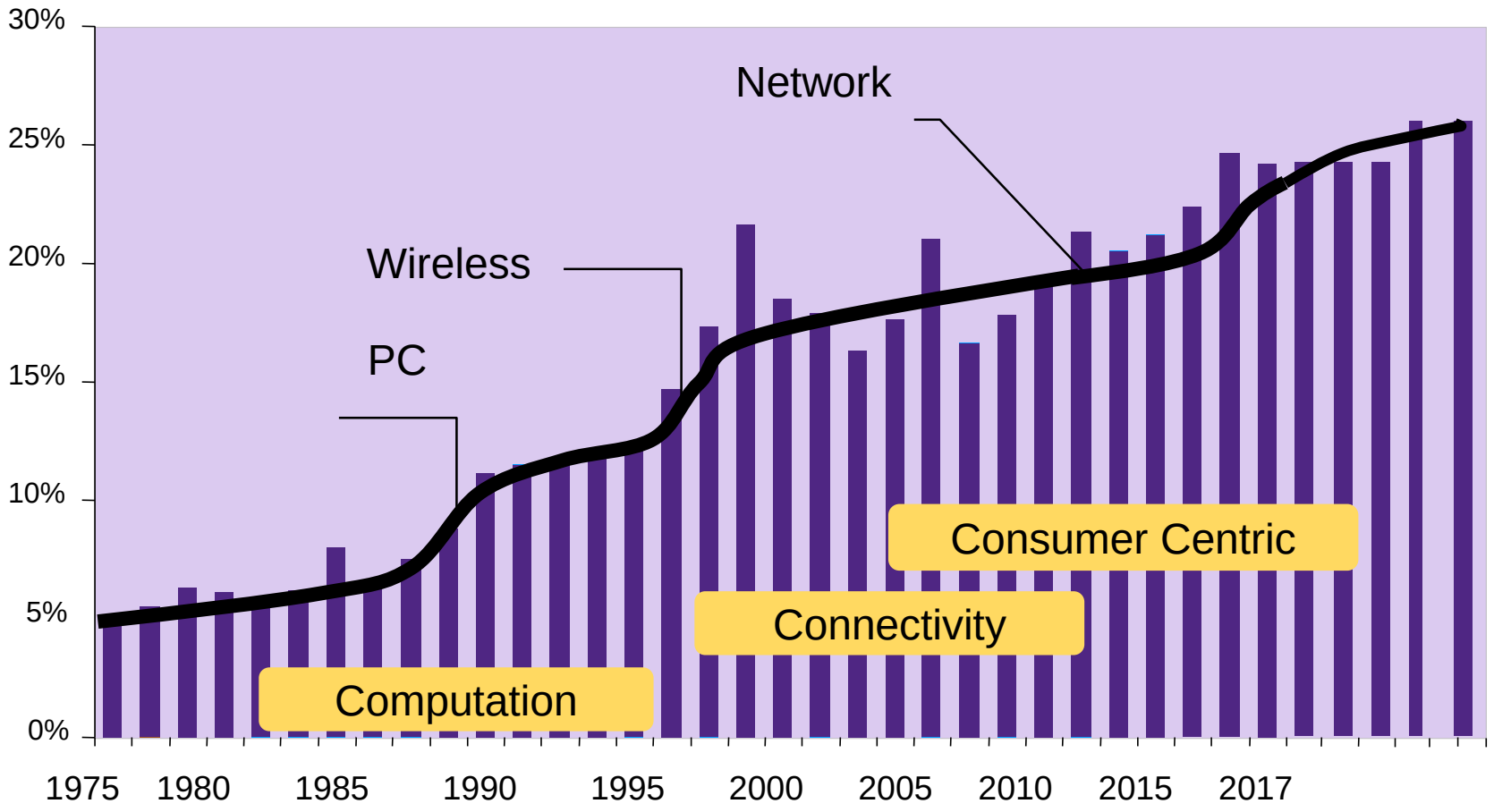
The Cost of Chip Content in Electronic Systems



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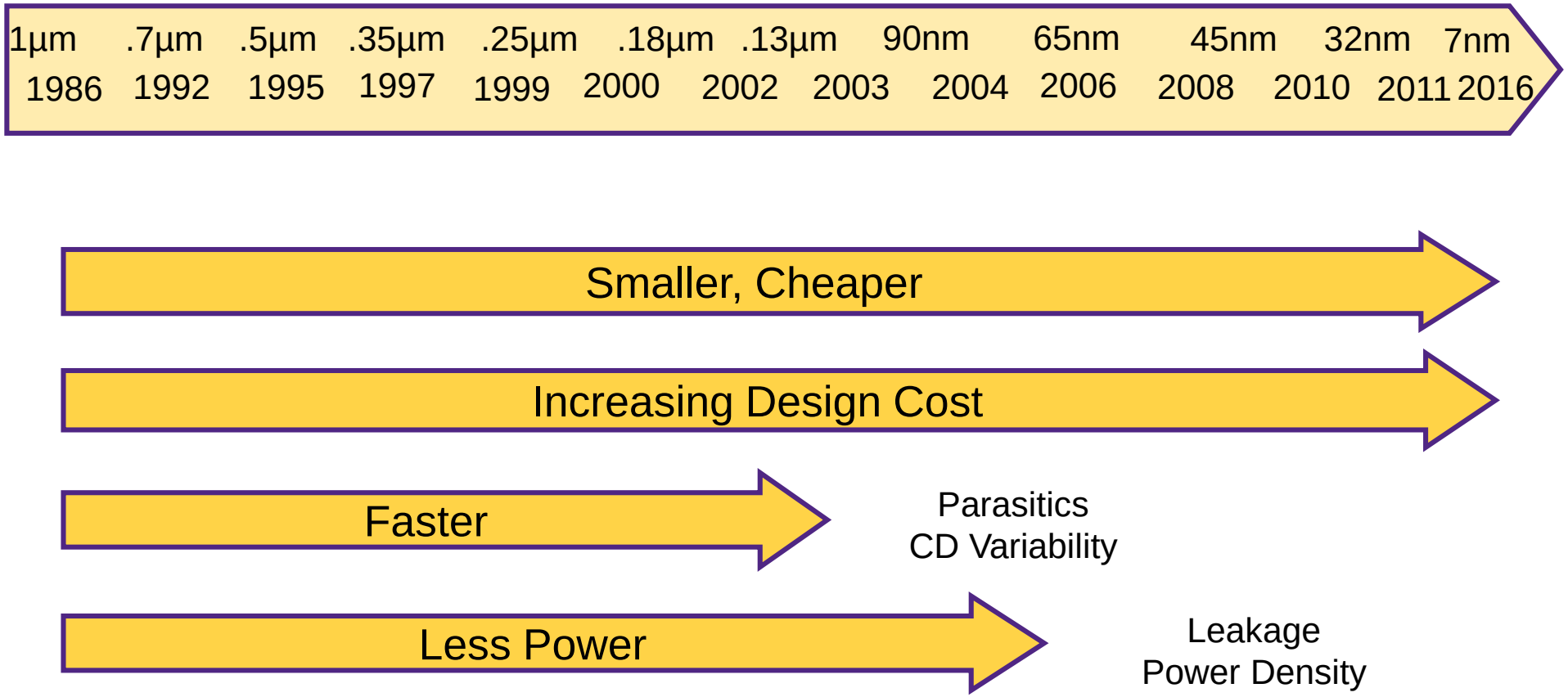
Technology Roadmap



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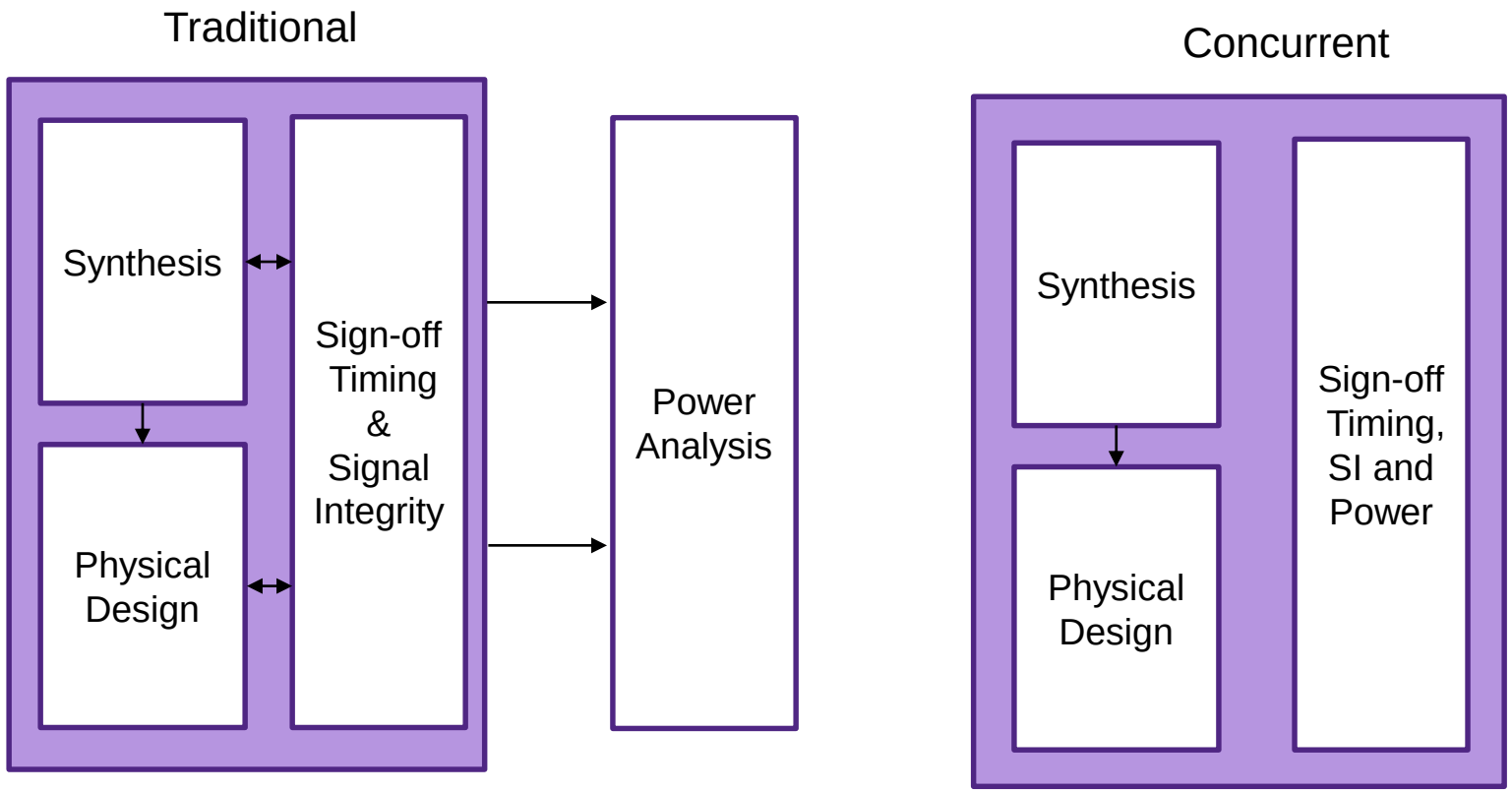
Concurrent Design Methodology



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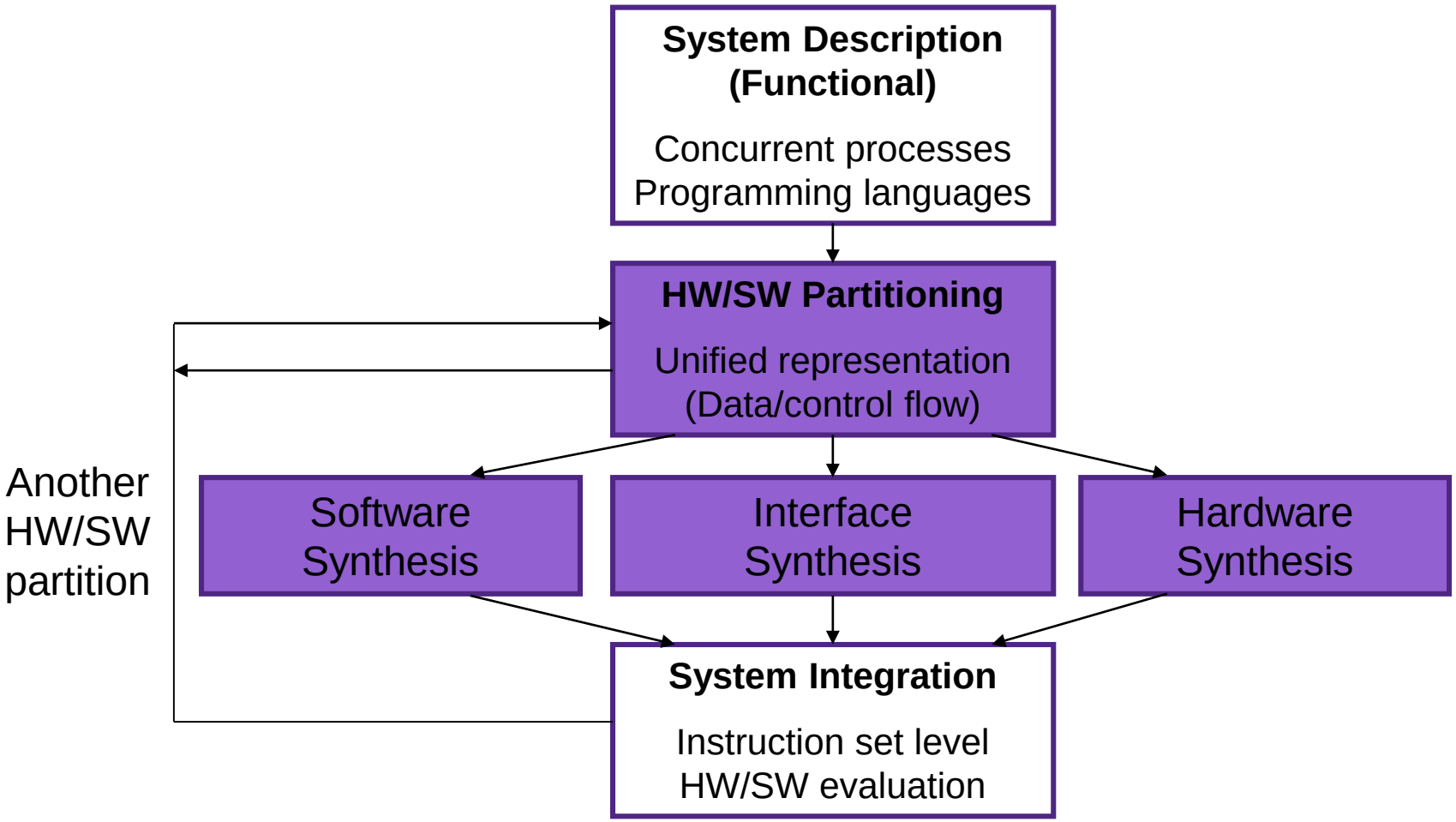
HW/SW Co-Design Flow



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