Lab 1: *Synthesis and results evaluation*

- Copy the lab directory to you home directory and go to the new directory:
    - cp -r <carpeta_de_referencia>/FE/LAB1 <carpeta_de_destino>
    - cd <carpeta_de_destino>

- Complete the DC script at ./scripts/dc.tcl with these values:

User-defined variable	**Directory/File Names/Values**
SEARCH PATH	. ./rtl ./libs
TARGET LIBRARY FILES	nldm_op_cond_typ.db
LINK LIBRARY FILES	* $target_library
RTL FILES	regbank.v muxed_regbank.v control.v alu.v top.v
ELABORATE PARAMETERS	WIDTH = 8

- The recommended flow is:
    - Logic library setup
    - RTL reading
    - Constrains setup
    - Pre-compile reports
    - Compile
    - Post-compile reports
    - Save design

- Create a csh file ("run.csh") to run Design Compiler with your script:
    - dc_shell -f ./scripts/dc.tcl | tee -i ./logs/dc.log

- You always can add a "return" command to stop the "dc.tcl" to have the "dc_shell" in interactive mode. In this case, add a return after RTL reading.

- The script will stop due to the "return" command. Start the GUI ("start_gui") and review your design.

- Remember you can analyze datapath extraction using:
    - analyze_datapath_extraction

- After this, please continue editing your “dc.tcl”. The next step is setup the following constrains:

Constraint	Value
Clock period	30
Clock Setup uncertainty	10%
Clock transition	20%
Clock Source latency	5%
Clock Network latency	-
Input delay*	40%
Output delay	50%
Output load	1
Input Min transition	1%
Input Max transition	10%

*** Do not add input delay to clock ports (use “remove_from_collection”).**

- Generate the pre-compile reports (clock, timing, constraints, power, etc). Save them using the “>” character (use spaces before and after). For example:
    - report_clock > ./reports/report_clock_precompile.rpt
- Synthetize (“compile_ultra”) your design using the “no autoungroup” option.
- Review your implemented design.
- Generate the post-compile reports like qor, timing, area, power, etc.
- Now, change your clock period (20) and see the differences in the reports (qor, timing, area, power).
- Take notes of the relevant numbers.
- Save the current compiled design using the two formats (DDC and Verilog+SDC).
- Exit DC