

SC70, 5ns, Low-Power, Single-Supply, Precision TTL Comparators

ABSOLUTE MAXIMUM RATINGS

Power Supply (V_{CC} to GND)-0.3V to +6V
 Analog Input (IN+ or IN-) to GND.....-0.3V to ($V_{CC} + 0.3V$)
 Input Current (IN+ or IN-) $\pm 30mA$
 LE to GND-0.3V to ($V_{CC} + 0.3V$)
 Continuous Output Current..... $\pm 40mA$
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 6-Pin SC70 (derate 3.1mW/ $^\circ C$ above $+70^\circ C$).....245mW
 6-Pin SOT23 (derate 8.7mW/ $^\circ C$ above $+70^\circ C$).....696mW
 8-Pin μ MAX (derate 4.5mW/ $^\circ C$ above $+70^\circ C$).....362mW

8-Pin SO (derate 5.9mW/ $^\circ C$ above $+70^\circ C$).....471mW
 Operating Temperature Range-40 $^\circ C$ to +85 $^\circ C$
 Junction Temperature+150 $^\circ C$
 Storage Temperature Range-65 $^\circ C$ to +150 $^\circ C$
 Lead Temperature (soldering, 10s)+300 $^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (MAX9010/MAX9011)

($V_{CC} = 5V$, $V_{LE} = 0$ (MAX9011 only), $V_{CM} = 0$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from V_{OS} tests	4.5		5.5	V
Power-Supply Current (Note 2)	I_{CC}			0.90	2.1	mA
Input Offset Voltage (Note 3)	V_{OS}	$T_A = +25^\circ C$		± 1	± 5	mV
		$T_A = T_{MIN}$ to T_{MAX}			± 7	
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$			± 2		$\mu V/^\circ C$
Input Bias Current	I_B			± 0.5	± 2	μA
Input Offset Current	I_{OS}			± 40	± 200	nA
Differential Input Resistance (Note 4)	$R_{IN(DIFF)}$	$V_{IN(DIFF)} = \pm 10mV$		250		k Ω
Common-Mode Input Resistance (Note 4)	$R_{IN(CM)}$	$-0.2V \leq V_{CM} \leq (V_{CC} - 1.9V)$		1		M Ω
Common-Mode Input Voltage Range (Note 4)	V_{CM}	Inferred from V_{OS} tests	-0.2	$V_{CC} - 1.9$		V
Common-Mode Rejection Ratio	CMRR	$-0.2V \leq V_{CM} \leq (V_{CC} - 1.9V)$		95		dB
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 4.5V$ to $5.5V$		82		dB
Small-Signal Voltage Gain	A_V	$1V \leq V_{OUT} \leq 2V$		3000		V/V
Output Low Voltage	V_{OL}	$V_{IN} \geq 100mV$		$I_{SINK} = 0$	0.3	V
				$I_{SINK} = 4mA$	0.5	
Output High Voltage	V_{OH}	$V_{IN} \geq 100mV$, $V_{CC} = 4.5V$		$I_{SOURCE} = 0$	2.7	V
				$I_{SOURCE} = 4mA$	2.4	
Output Short-Circuit Current	I_{OUT}	Sinking		20		mA
		Sourcing		30		
Latch Enable Pin High Input Voltage	V_{IH}	MAX9011 only	2			V
Latch Enable Pin Low Input Voltage	V_{IL}	MAX9011 only			0.8	V
Latch Enable Pin Bias Current	I_{IH} , I_{IL}	MAX9011 only, $V_{LE} = 0$ and $V_{LE} = 5V$			± 25	μA

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MAX9010-MAX9013

ELECTRICAL CHARACTERISTICS (MAX9010/MAX9011) (continued)

($V_{CC} = 5V$, $V_{LE} = 0$ (MAX9011 only), $V_{CM} = 0$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Latch Setup Time (Note 8)	t_{SU}	MAX9011 only	2	0		ns
Latch Hold Time (Note 8)	t_H	MAX9011 only	2	0.5		ns
Latch Propagation Delay (Note 8)	t_{LPD}	MAX9011 only		5		ns
Input Noise-Voltage Density	e_n	$f = 100kHz$		6		nV/\sqrt{Hz}
Propagation Delay (Note 6)	t_{PD+}, t_{PD-}	$C_{LOAD} = 5pF$, $T_A = +25^\circ C$		5	8	ns
		$V_{OVERDRIVE} = 100mV$				
		$V_{OVERDRIVE} = 5mV$		5.5	9	
		$C_{LOAD} = 5pF$, $T_A = T_{MIN}$ to T_{MAX}			9	
		$V_{OVERDRIVE} = 5mV$			10	
Output Rise Time	t_R	$0.5V \leq V_{OUT} \leq 2.5V$		3		ns
Output Fall Time	t_F	$2.5V \geq V_{OUT} \geq 0.5V$		2		ns
Input Capacitance	C_{IN}	MAX9010EXT		0.8		pF
		MAX9011EUT		1.2		
Power-Up Time	t_{ON}			1		μs

ELECTRICAL CHARACTERISTICS (MAX9012/MAX9013)

($V_{CC} = 5V$, $V_{LE} = 0$ (MAX9013 only), $V_{CM} = 0$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test	4.5		5.5	V
Power-Supply Current (Note 2)	I_{CC}	MAX9012		2.4	4.2	mA
		MAX9013		1.3	2.3	
Input Offset Voltage (Note 5)	V_{OS}	$T_A = +25^\circ C$		± 0.7	± 3	mV
		$T_A = T_{MIN}$ to T_{MAX}			± 5.5	
Input Offset-Voltage Drift	$\Delta V_{OS}/\Delta T$			± 2		$\mu V/^\circ C$
Input Bias Current	I_B			± 0.5	± 2	μA
Input Offset Current	I_{OS}			± 40	± 200	nA
Differential Input Resistance (Note 4)	$R_{IN(DIFF)}$	$V_{IN(DIFF)} = \pm 10mV$		250		$k\Omega$
Common-Mode Input Resistance (Note 4)	$R_{IN(CM)}$	$-0.2V \leq V_{CM} \leq (V_{CC} - 1.9V)$		1		$M\Omega$
Common-Mode Input Voltage Range (Note 4)	V_{CM}	Inferred from CMRR test	-0.2	$V_{CC} - 1.9$		V
Common-Mode Rejection Ratio	CMRR	$-0.2V \leq V_{CM} \leq (V_{CC} - 1.9V)$	75	95		dB
Power-Supply Rejection Ratio	PSRR	$V_{CC} = 4.5V$ to $5.5V$	63	82		dB

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ELECTRICAL CHARACTERISTICS (MAX9012/MAX9013) (continued)

($V_{CC} = 5V$, $V_{LE} = 0$ (MAX9013 only), $V_{CM} = 0$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal Voltage Gain	A_V	$1V \leq V_{OUT} \leq 2V$		1000	3000		V/V
Output Low Voltage	V_{OL}	$V_{IN} \geq 100mV$	$I_{SINK} = 0$		0.3	0.5	V
			$I_{SINK} = 4mA$		0.5	0.6	
Output High Voltage	V_{OH}	$V_{IN} \geq 100mV$, $V_{CC} = 4.5V$	$I_{SOURCE} = 0$	2.7	3.3		V
			$I_{SOURCE} = 4mA$	2.4	2.9		
Output Short-Circuit Current	I_{OUT}	Sinking			20		mA
		Sourcing			30		
Latch Enable Pin High Input Voltage	V_{IH}	MAX9013 only		2			V
Latch Enable Pin Low Input Voltage	V_{IL}	MAX9013 only				0.8	V
Latch Enable Pin Bias Current	I_{IH} , I_{IL}	MAX9013 only $V_{LE} = 0$ and $V_{LE} = 5V$				± 25	μA
Input Noise-Voltage Density	e_n	$f = 100kHz$			6		nV/\sqrt{Hz}
Propagation Delay (Note 6)	t_{PD+} , t_{PD-}	$C_{LOAD} = 5pF$, $T_A = +25^\circ C$	$V_{OVERDRIVE} = 100mV$		5	8	ns
			$V_{OVERDRIVE} = 5mV$		5.5	9	
		$C_{LOAD} = 5pF$, $T_A = T_{MIN}$ to T_{MAX}	$V_{OVERDRIVE} = 100mV$			9	
			$V_{OVERDRIVE} = 5mV$			10	
Differential Propagation Delay (Notes 6, 7)	$\Delta t_{PD\pm}$	$V_{IN} = 100mV$ step, $C_{LOAD} = 5pF$, $V_{OD} = 5mV$			2	3	ns
Channel-to-Channel Propagation Delay (Note 6)	$\Delta t_{PD(ch-ch)}$	MAX9012 only, $V_{IN} = 100mV$ step, $C_{LOAD} = 5pF$, $V_{OD} = 5mV$			500		ps
Output Rise Time	t_R	$0.5V \leq V_{OUT} \leq 2.5V$			3		ns
Output Fall Time	t_F	$2.5V \geq V_{OUT} \geq 0.5V$			2		ns
Latch Setup Time (Note 8)	t_{SU}	MAX9013 only		2	0		ns
Latch Hold Time (Note 8)	t_H	MAX9013 only		2	0.5		ns
Latch Propagation Delay (Note 8)	t_{LPD}	MAX9013 only			5		ns
Input Capacitance	C_{IN}	MAX9012EUA/MAX9013EUA			1.5		pF
		MAX9012ESA/MAX9013ESA			2		
Power-Up Time	t_{ON}				1		μs

Note 1: All specifications are 100% tested at $T_A = +25^\circ C$; temperature limits are guaranteed by design.

Note 2: Quiescent Power-Supply Current is slightly higher with the comparator output at V_{OL} . This parameter is specified with the worst-case condition of $V_{OUT} = V_{OL}$ for the MAX9010/MAX9011 and both outputs at V_{OL} for the MAX9012. For the MAX9013, which has complementary outputs, the power-supply current is specified with either $OUT = V_{OL}$, $\overline{OUT} = V_{OH}$ or $OUT = V_{OH}$, $\overline{OUT} = V_{OL}$ (power-supply current is equal in either case).

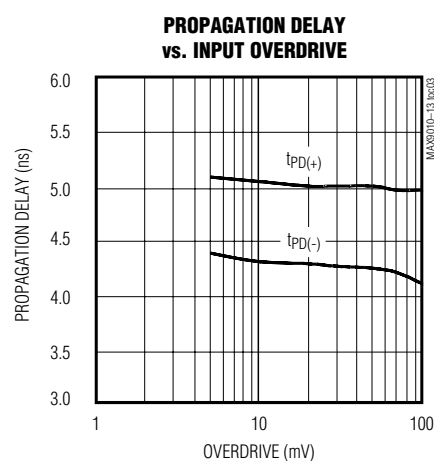
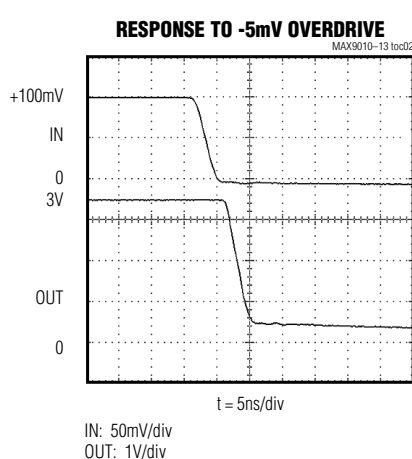
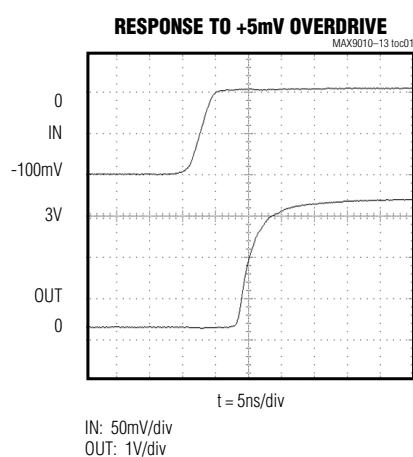
Note 3: Input Offset Voltage is tested and specified with the Input Common-Mode Voltage set to either extreme of the Input Common-Mode Voltage Range ($-0.2V$ to $(V_{CC} - 1.9V)$) and with the Power-Supply Voltage set to either extreme of the Power-Supply Voltage Range ($4.5V$ to $5.5V$).

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- Note 4:** Although Common-Mode Input Voltage Range is restricted to $-0.2V \leq V_{CM} \leq (V_{CC} - 1.9V)$, either or both inputs can go to either absolute maximum voltage limit, i.e., from $-0.3V$ to $(V_{CC} + 0.3V)$, without damage. The comparator will make a correct (and fast) logic decision provided that at least one of the two inputs is within the specified common-mode range. If both inputs are outside the common-mode range, the comparator output state is indeterminate.
- Note 5:** For the MAX9012, Input Offset Voltage is defined as the input voltage(s) required to make the OUT output voltage(s) remain stable at 1.4V. For the MAX9013, it is defined as the average of two input offset voltages, measured by forcing first the OUT output, then the \overline{OUT} output to 1.4V.
- Note 6:** Propagation delay for these high-speed comparators is guaranteed by design because it cannot be accurately measured with low levels of input overdrive voltage using automatic test equipment in production. Note that for low overdrive conditions, V_{OS} is added to the overdrive.
- Note 7:** Differential Propagation Delay, measured either on a single output of the MAX9012/MAX9013 (or between OUT and \overline{OUT} outputs on the MAX9013) is defined as: $\Delta t_{PD(\pm)} = |t_{PD(+)} - t_{PD(-)}|$.
- Note 8:** Latch times are guaranteed by design. Latch setup time (t_{SU}) is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time (t_H) is the interval after the latch is asserted in which the input signal must remain stable. Latch propagation delay (t_{LPD}) is the delay time for the output to respond when the latch enable pin is deasserted (see Figure 1).

Typical Operating Characteristics

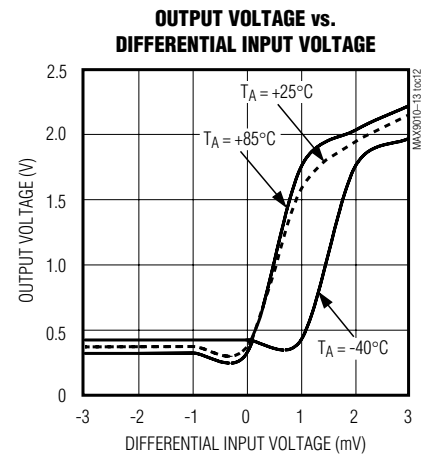
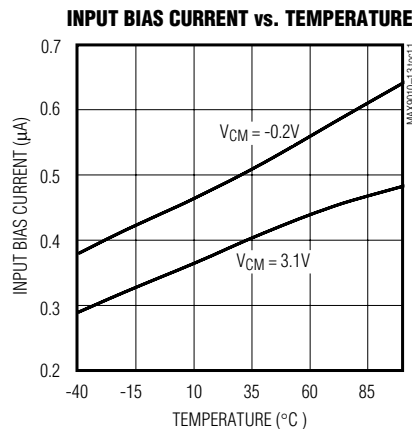
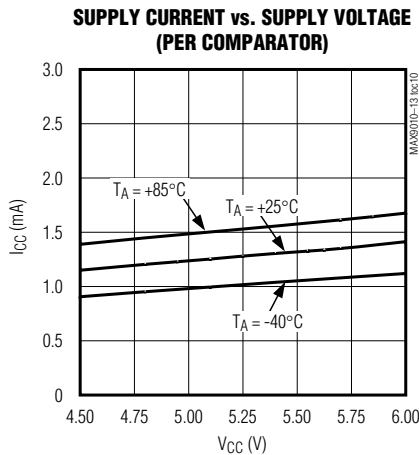
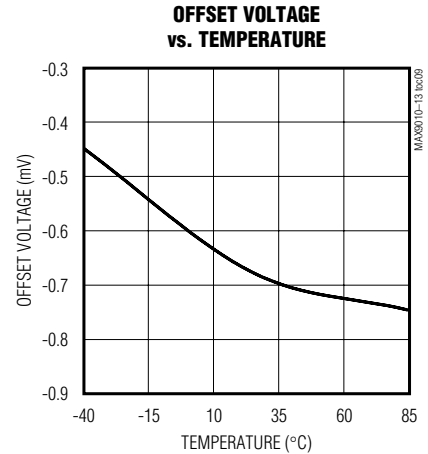
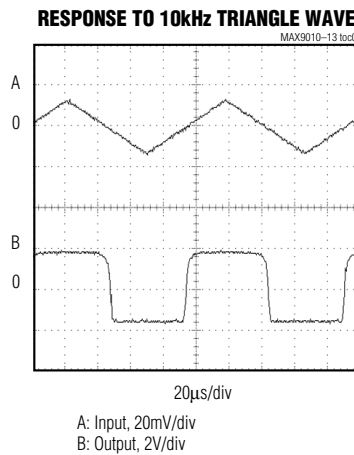
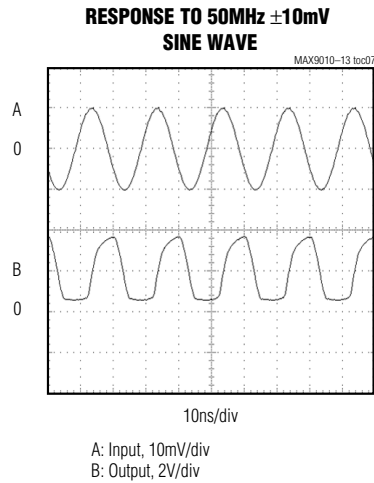
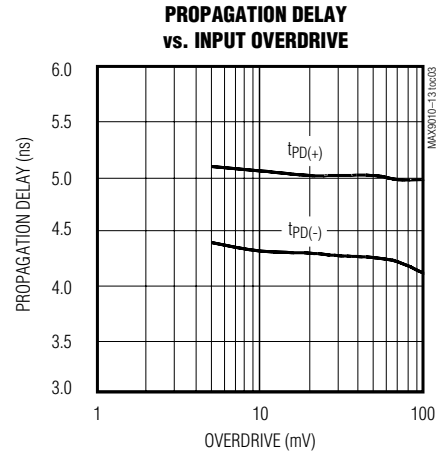
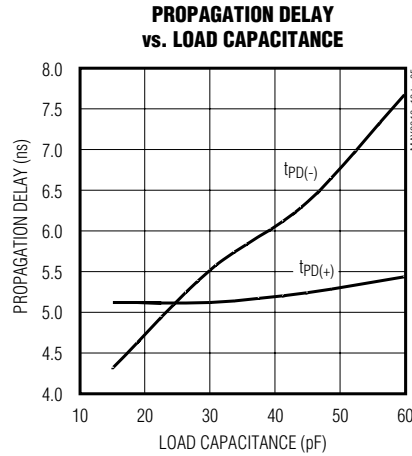
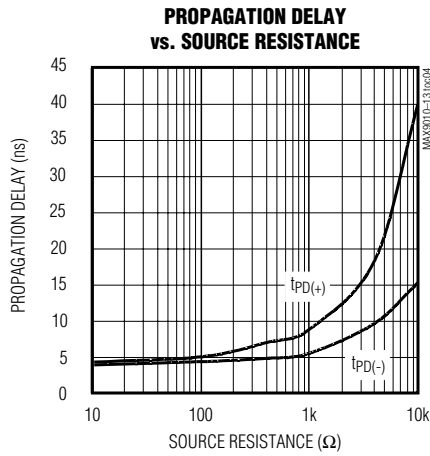
($V_{CC} = 5V$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $C_L = 15pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

PIN				NAME	FUNCTION
MAX9010	MAX9011	MAX9012	MAX9013		
1	1	—	7	OUT	Comparator Output. OUT is high when IN+ is more positive than IN-.
2	2	5	6	GND	Ground
3	3	—	2	IN+	Noninverting Input
4	4	—	3	IN-	Inverting Input
5, 6	6	8	1	V _{CC}	Positive Power-Supply Voltage. Pins 5 and 6 of the MAX9010 must BOTH be connected to the power-supply rail. Bypass with a 0.1μF capacitor.
—	5	—	5	LE	Latch Enable Input
—	—	1	—	INA+	Noninverting Input, Channel A
—	—	2	—	INA-	Inverting Input, Channel A
—	—	3	—	INB+	Noninverting Input, Channel B
—	—	4	—	INB-	Inverting Input, Channel B
—	—	6	—	OUTB	Comparator Output, Channel B
—	—	7	—	OUTA	Comparator Output, Channel A
—	—	—	4	N.C.	No Connection. Not internally connected. Connect to GND for best results.
—	—	—	8	$\overline{\text{OUT}}$	Comparator Complementary Output

Detailed Description

These high-speed comparators have a unique design that prevents oscillation when the comparator is in its linear region, so no minimum input slew rate is required. Many high-speed comparators oscillate in their linear region. One common way to overcome this oscillation is to add hysteresis, but it results in a loss of resolution and bandwidth.

Latch Function

The MAX9011/MAX9013 provide a TTL-compatible latch function that holds the comparator output state (Figure 1). With LE driven to a TTL low or grounded, the latch is transparent and the output state is determined by the input differential voltage. When LE is driven to a TTL high, the existing output state is latched, and the input differential voltage has no further effect on the output state.

Input Amplifier

A comparator can be thought of as having two sections: an input amplifier and a logic interface. The input amplifiers of these devices are fully differential, with input offset voltages typically 0.7mV at +25°C. Input common-mode range extends from 200mV below ground to 1.9V below the positive power-supply rail. The

total common-mode range is 3.3V when operating from a 5V supply. The amplifiers have no built-in hysteresis. For highest accuracy, do not add hysteresis. Figure 2 shows how hysteresis degrades resolution.

Input Voltage Range

Although the common-mode input voltage range is restricted to -0.2V to (V_{CC} - 1.9V), either or both inputs can go to either absolute maximum voltage limit, i.e., from -0.3V to (V_{CC} + 0.3V), without damage. The comparator will make a correct (and fast) logic decision provided that at least one of the two inputs is within the specified common-mode range. If both inputs are outside the common-mode range, the comparator output state is indeterminate.

Resolution

A comparator's ability to resolve a small-signal difference, its resolution, is affected by various factors. As with most amplifiers and comparators, the most significant factors are the input offset voltage (V_{OS}) and the common-mode and power-supply rejection ratios (CMRR, PSRR). If source impedance is high, input offset current can be significant. If source impedance is unbalanced, the input bias current can introduce another error. For high-speed comparators, an addi-

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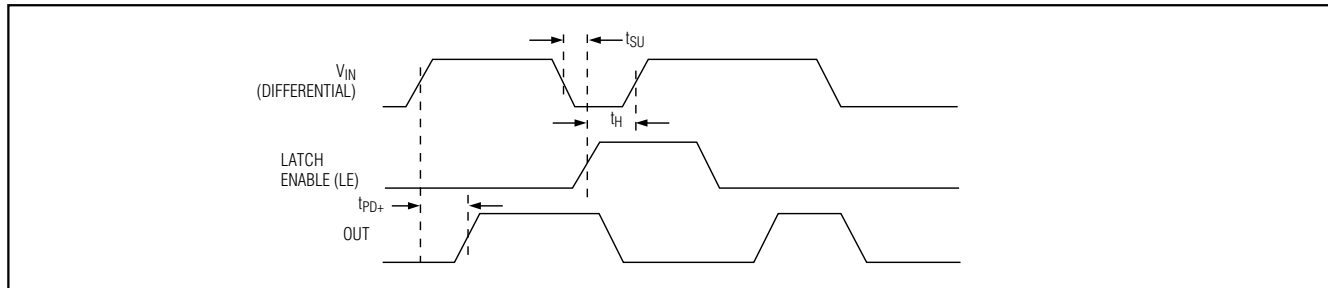


Figure 1. Timing Diagram

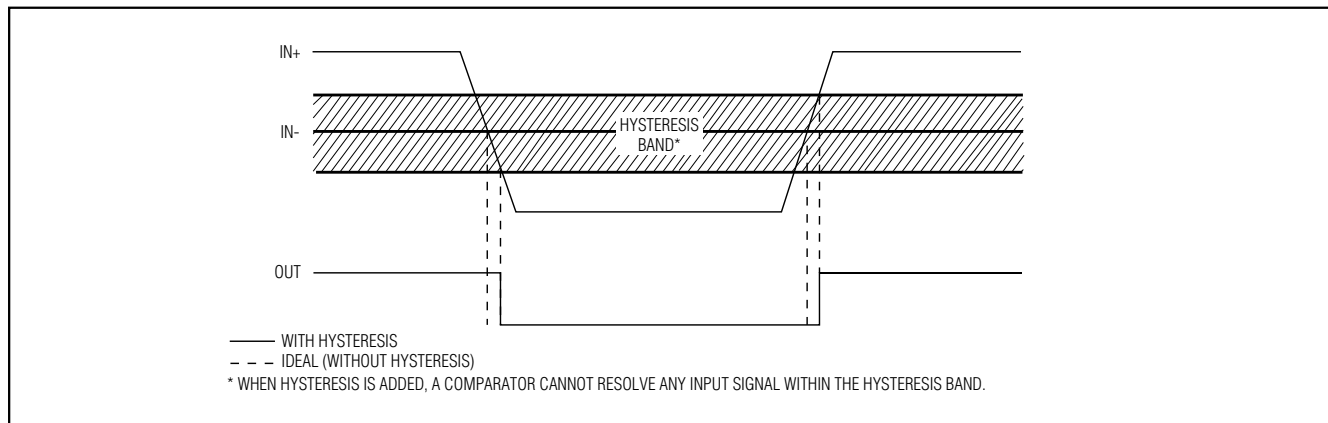


Figure 2. Effect of Hysteresis on Input Resolution

tional factor in resolution is the comparator's stability in its linear region. Many high-speed comparators are useless in their linear region because they oscillate. This makes the differential input voltage region around zero unusable. Hysteresis helps to cure the problem but reduces resolution (Figure 2). The devices do not oscillate in the linear region and require no hysteresis, which greatly enhances their resolution.

Applications Information

Power Supplies, Bypassing, and Board Layout

These products operate over a supply voltage range of 4.5V to 5.5V. Bypass V_{CC} to GND with a 0.1 μ F surface-mount ceramic capacitor. Mount the ceramic capacitor as close as possible to the supply pin to minimize lead inductance.

As with all high-speed components, careful attention to board layout is essential for best performance. Use a PC board with an unbroken ground plane. Pay close attention to the bandwidth of bypass components and place them as close as possible to the device.

Minimize the trace length and area at the comparator inputs. If the source impedance is high, take the utmost care in minimizing its susceptibility to pickup of unwanted signals.

Input Slew Rate

Most high-speed comparators have a minimum input slew-rate requirement. If the input signal does not transverse the region of instability within a propagation delay of the comparator, the output can oscillate. This makes many high-speed comparators unsuitable for processing either slow-moving signals or fast-moving signals with low overdrive. The design of these devices eliminates the minimum input slew-rate requirement. They are excellent for circuits from DC up to 200MHz, even with very low overdrive, where small signals need to be resolved.

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Selector Guide

PART	COMPARATORS	LATCH	COMPLEMENTARY OUTPUTS
MAX9010	1	No	No
MAX9011	1	Yes	No
MAX9012	2	No	No
MAX9013	1	Yes	Yes

Chip Information

MAX9010 TRANSISTOR COUNT: 106

MAX9011 TRANSISTOR COUNT: 137

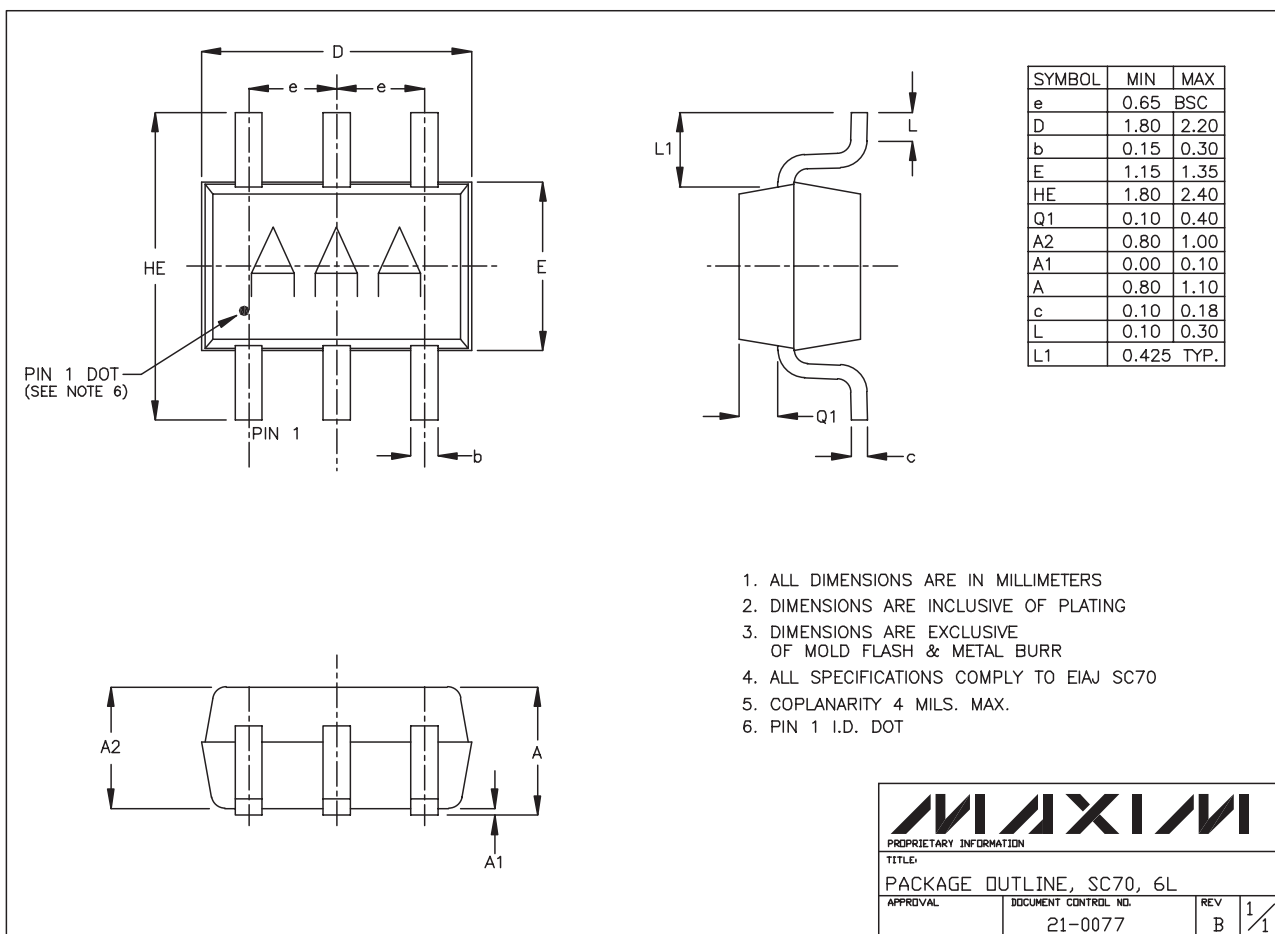
MAX9012 TRANSISTOR COUNT: 212

MAX9013 TRANSISTOR COUNT: 145

PROCESS: Bipolar

Package Information

MAX9010-MAX9013

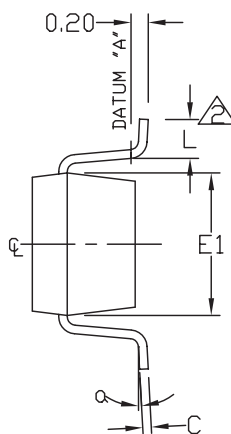
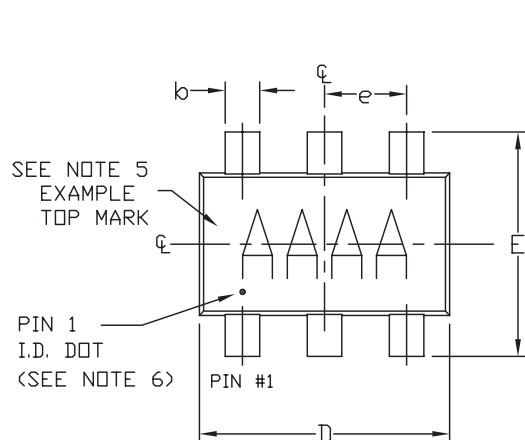


SC70, 6LEPS

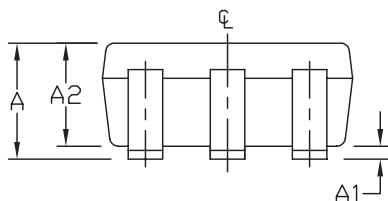
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Package Information (continued)

6LSOTEP5



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM Ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

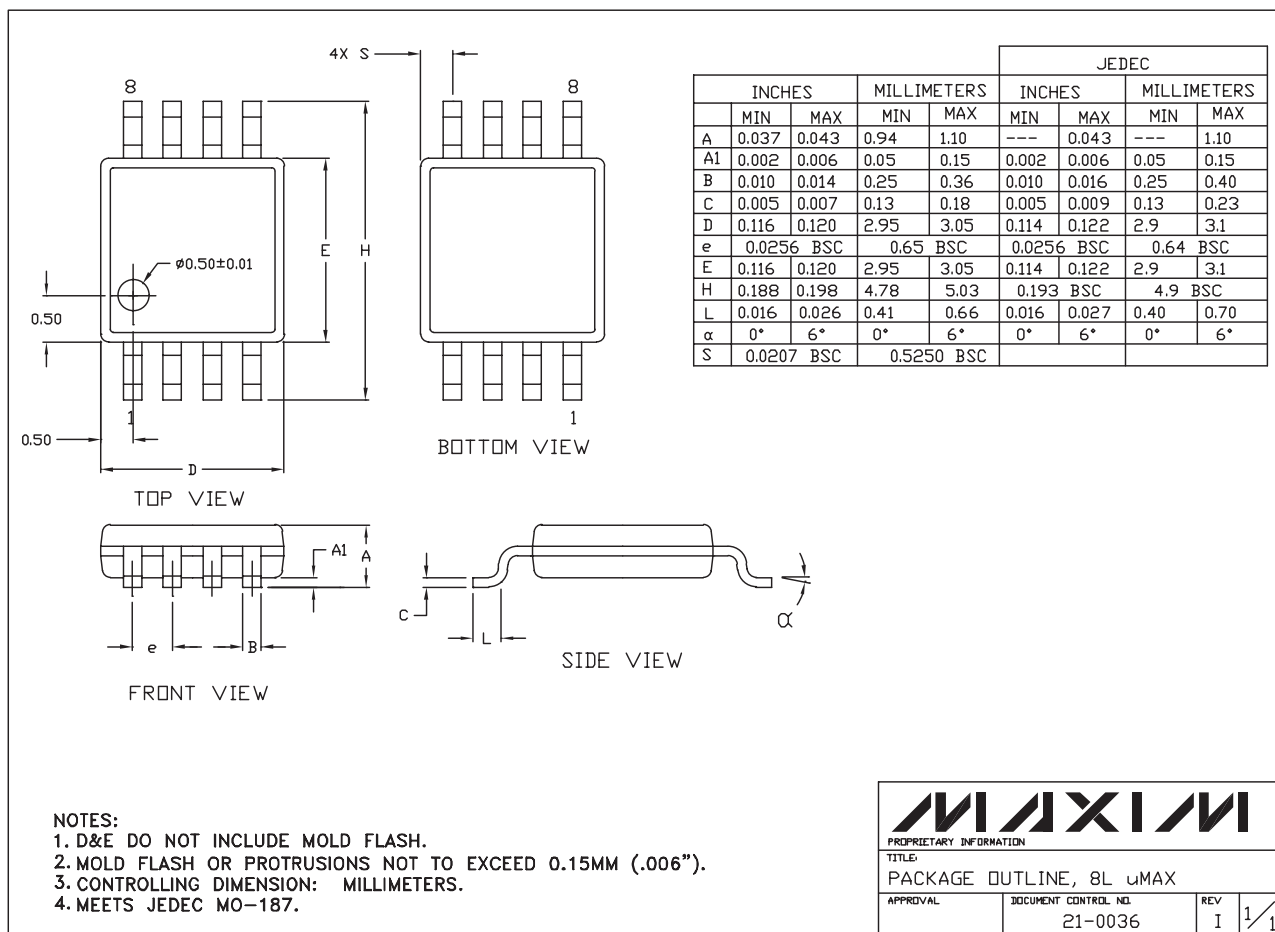
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Package Information (continued)

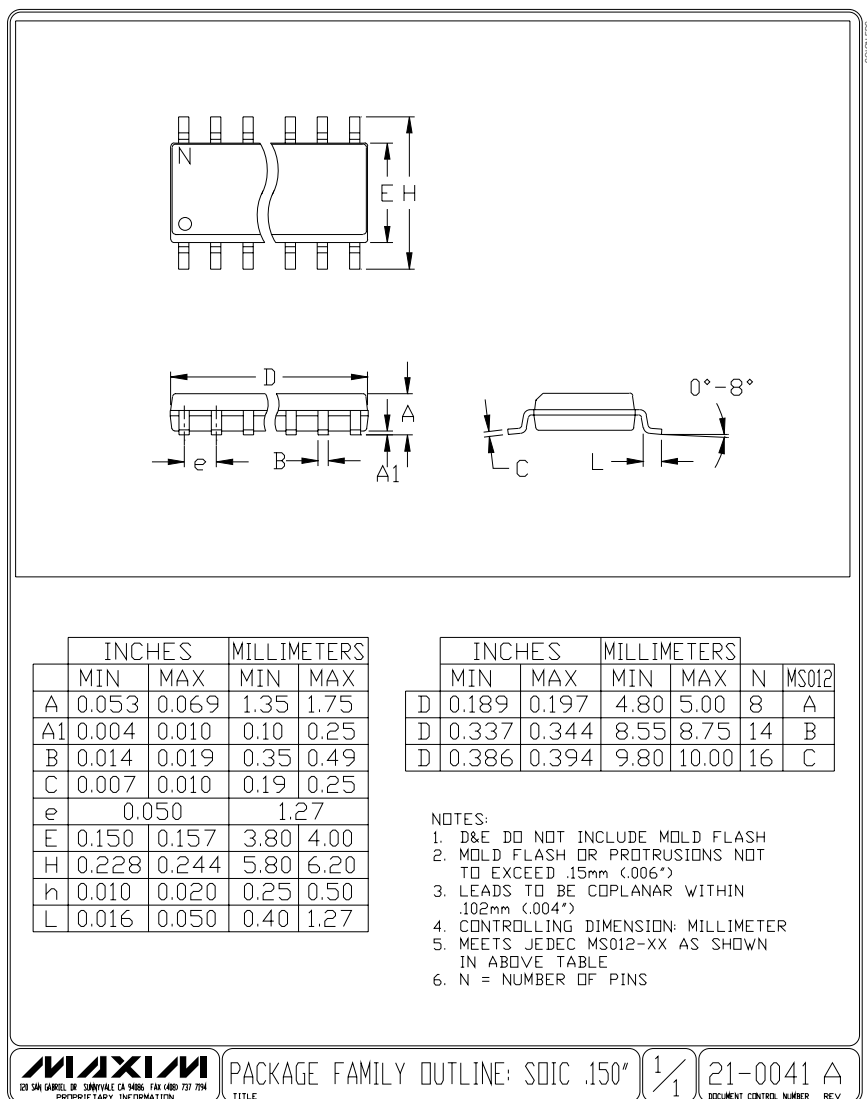
MAX9010-MAX9013

8LUMAXD.EPS



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Package Information (continued)



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