

# 74LVC574A

Octal D-type flip-flop with 5 V tolerant inputs/outputs;  
positive edge-trigger; 3-state

Rev. 6 — 30 August 2021

Product data sheet

## 1. General description

The 74LVC574A is an 8-bit positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable ( $\overline{OE}$ ) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

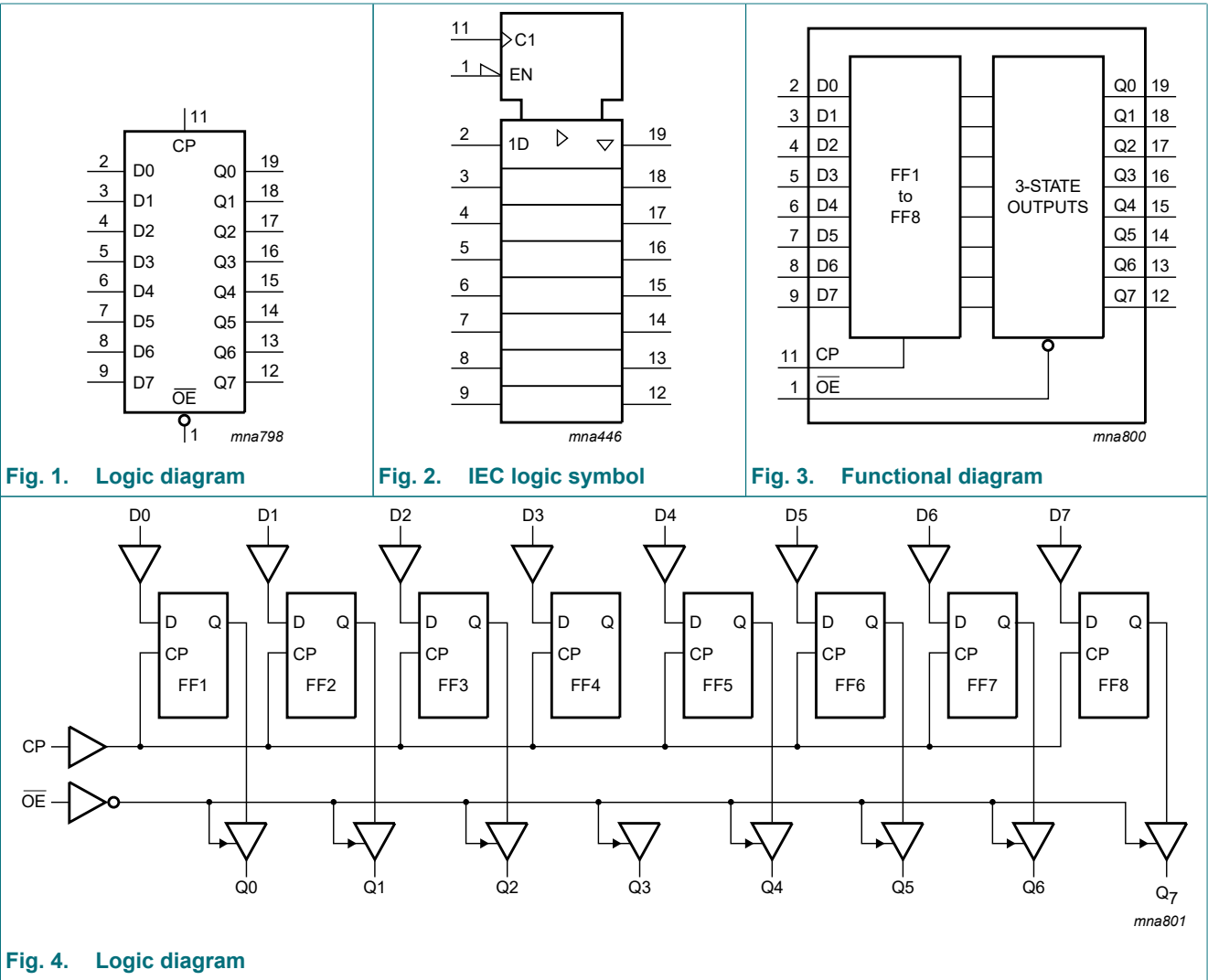
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- High-impedance when  $V_{CC} = 0$  V
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Flow-through pin-out architecture
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7A (1.65 V to 1.95 V)
  - JESD8-5A (2.3 V to 2.7 V)
  - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC574AD	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC574APW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC574ABQ	-40 °C to +125 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



5. Pinning information

5.1. Pinning

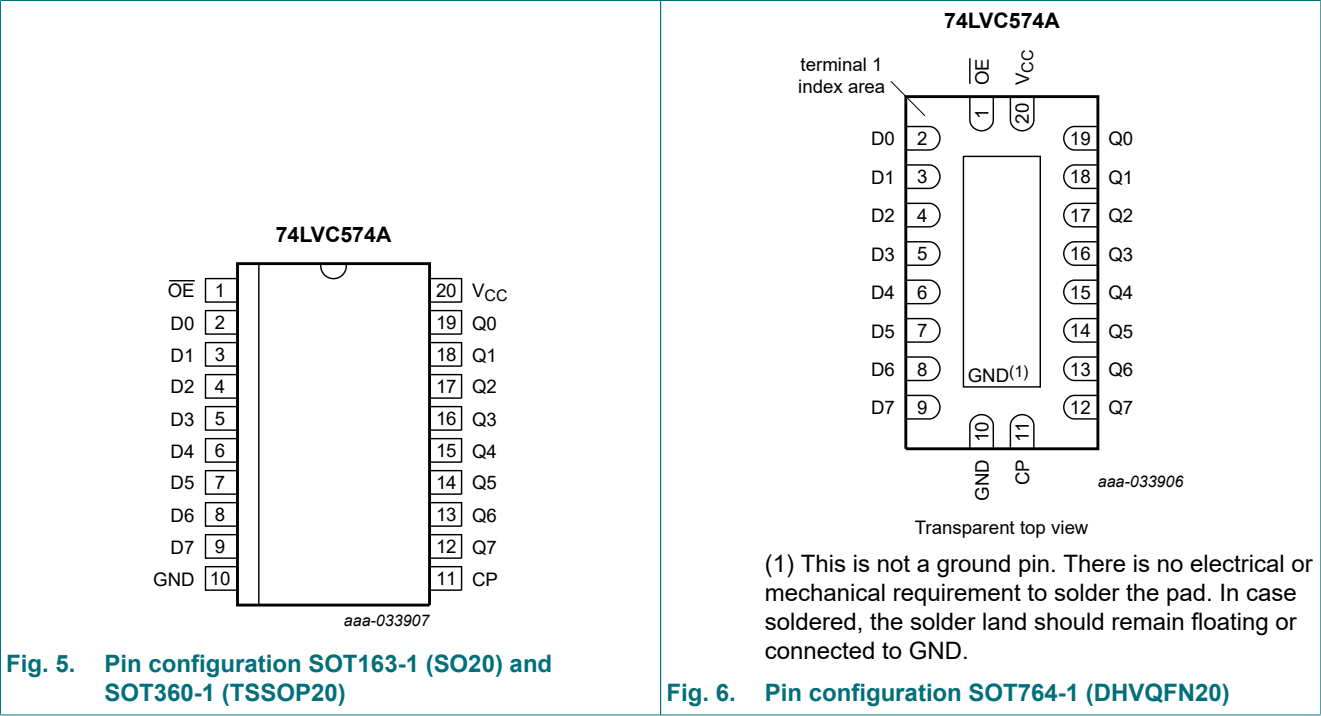


Fig. 5. Pin configuration SOT163-1 (SO20) and SOT360-1 (TSSOP20)

Fig. 6. Pin configuration SOT764-1 (DHVQFN20)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	output enable input (active LOW)
CP	11	clock input (LOW to HIGH; edge triggered)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
GND	10	ground (0 V)
VCC	20	supply voltage

## 6. Functional description

**Table 3. Functional table**

*H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition;*

*L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition;*

*↑ = LOW to HIGH clock transition;*

*Z = high-impedance OFF-state*

Operating modes	Input			Internal flip-flop	Output Qn
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$	-50	-	mA
$V_I$	input voltage	[1]	-0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
$V_O$	output voltage	output HIGH or LOW state [2]	-0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0\text{ V to }V_{CC}$	-	±50	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C to }+125\text{ °C}$ [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT163-1 (SO20) package:  $P_{tot}$  derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package:  $P_{tot}$  derates linearly with 10.0 mW/K above 100 °C.

For SOT764-1 (DHVQFN20) package:  $P_{tot}$  derates linearly with 12.9 mW/K above 111 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V <sub>I</sub>	input voltage		0	-	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35V <sub>CC</sub>	-	0.35V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.2	-	-	V <sub>CC</sub> - 0.3	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	2.4	-	-	2.25	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 5.5 V or GND	-	0.1	±10	-	±20	μA
I <sub>OFF</sub>	power-off leakage supply	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	0.1	±10	-	±20	μA

## Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
$I_{CC}$	supply current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$	-	0.1	10	-	40	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V}$ to $3.6 \text{ V}$ ; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$	-	5	500	-	5000	$\mu\text{A}$
$C_I$	input capacitance	$V_{CC} = 0 \text{ V}$ to $3.6 \text{ V}$ ; $V_I = \text{GND}$ to $V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  (unless stated otherwise) and  $T_{amb} = 25 \text{ °C}$ .

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_{pd}$	propagation delay	CP to Qn; see Fig. 7 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	17.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	4.6	6.4	13.1	4.6	15.1	ns
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	2.6	3.9	7.9	2.6	9.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.7	8.0	1.5	10.0	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1.5	3.5	7.0	1.5	9.0	ns
$t_{en}$	enable time	$\overline{OE}$ to Qn; see Fig. 9 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	19.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	1.5	7.0	17.1	1.5	19.8	ns
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	1.5	4.0	9.4	1.5	10.9	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	4.1	8.5	1.5	11.0	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1.5	3.2	7.5	1.5	9.5	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see Fig. 9 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	9.0	-	-	-	ns
		$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	2.5	4.1	10.1	2.5	11.6	ns
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	1.0	2.3	5.7	1.0	6.6	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.1	6.5	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	1.5	2.9	6.0	1.5	7.5	ns
$t_W$	pulse width	clock HIGH or LOW; see Fig. 7						
		$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	5.0	-	-	5.0	-	ns
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.3	-	-	3.3	-	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	3.3	1.7	-	3.3	-	ns
$t_{su}$	set-up time	Dn to CP; see Fig. 8						
		$V_{CC} = 1.65 \text{ V}$ to $1.95 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.3 \text{ V}$ to $2.7 \text{ V}$	2.5	-	-	2.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.0	-	-	2.0	-	ns
		$V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$	2.0	0.3	-	2.0	-	ns

## Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
$t_h$	hold time	Dn to CP; see Fig. 8						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.0	-	-	2.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	-	1.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	+1.5	-0.2	-	+1.5	-	ns
$f_{\max}$	maximum frequency	see Fig. 7						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	100	-	-	80	-	MHz
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	125	-	-	100	-	MHz
		$V_{CC} = 2.7 \text{ V}$	150	-	-	120	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	150	200	-	120	-	MHz
$t_{sk(0)}$	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [3]	-	-	1.0	-	1.5	ns
$C_{PD}$	power dissipation capacitance	per flip-flop; $V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	11.2	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	13.2	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	14.9	-	-	-	pF

[1] Typical values are measured at  $T_{\text{amb}} = 25 \text{ °C}$  and  $V_{CC} = 1.2 \text{ V}, 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}$  and  $3.3 \text{ V}$  respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

$t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

$t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz;

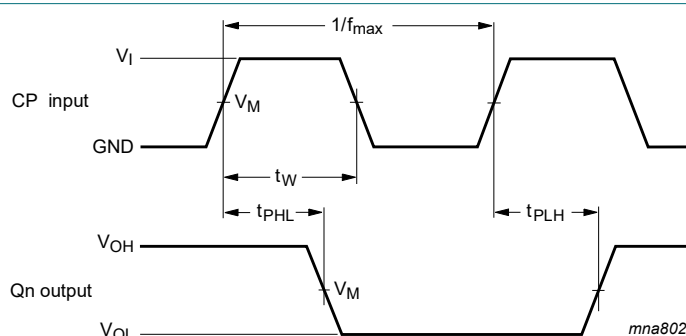
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volt;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

## 10.1. Waveforms and test circuit

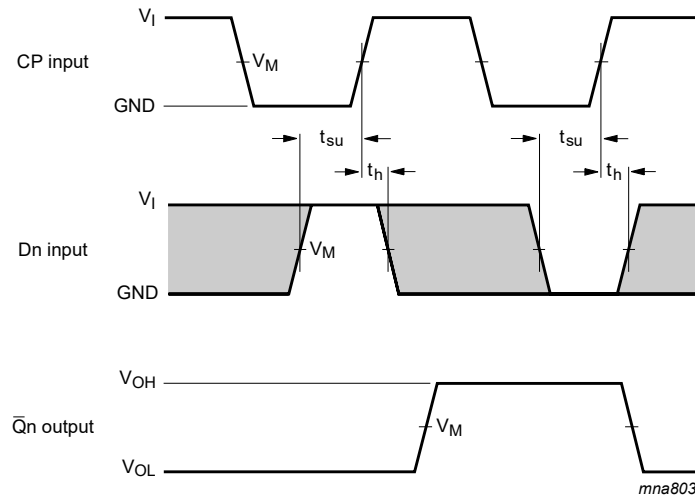


Measurement points are given in Table 8.

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 7.** Clock (CP) to output (Qn) propagation delays, the clock pulse width, output transition times, and the maximum frequency

## Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

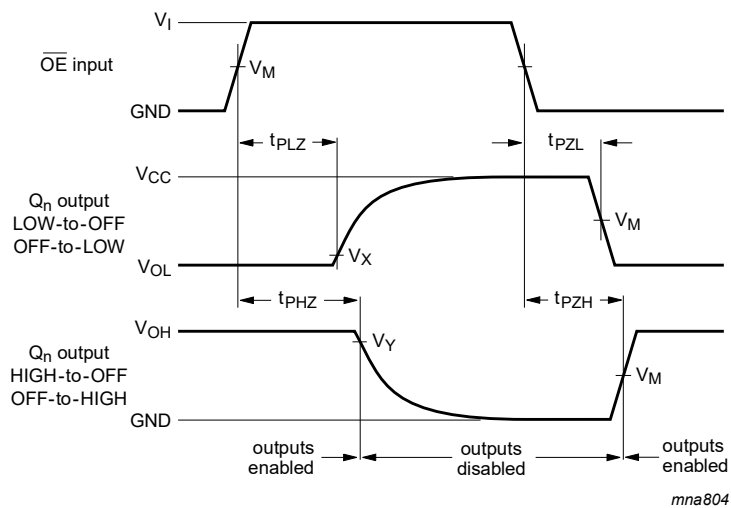


Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 8. Data set-up and hold times for the Dn input to the CP input**



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 9. 3-state enable and disable times**

**Table 8. Measurement points**

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

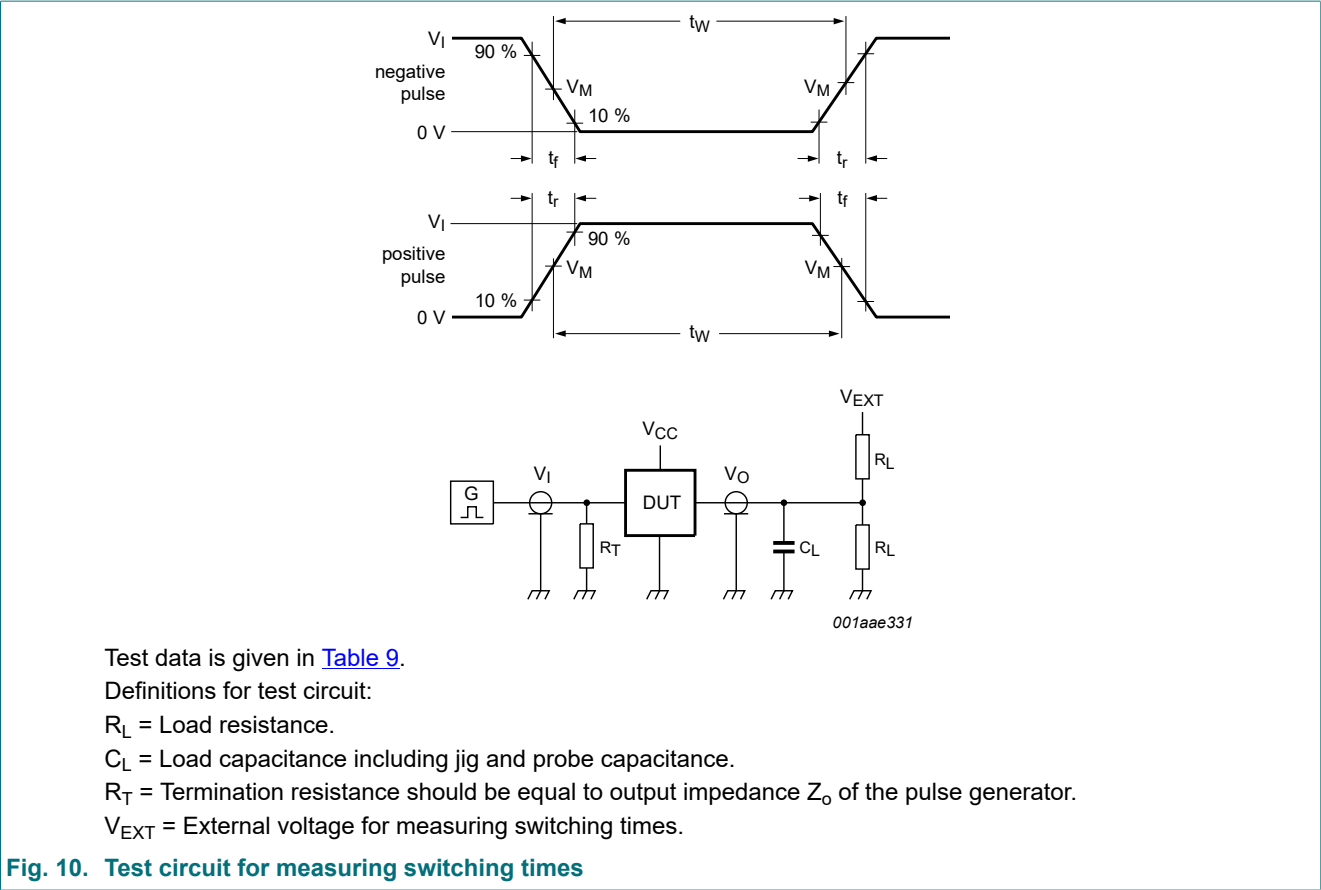


Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

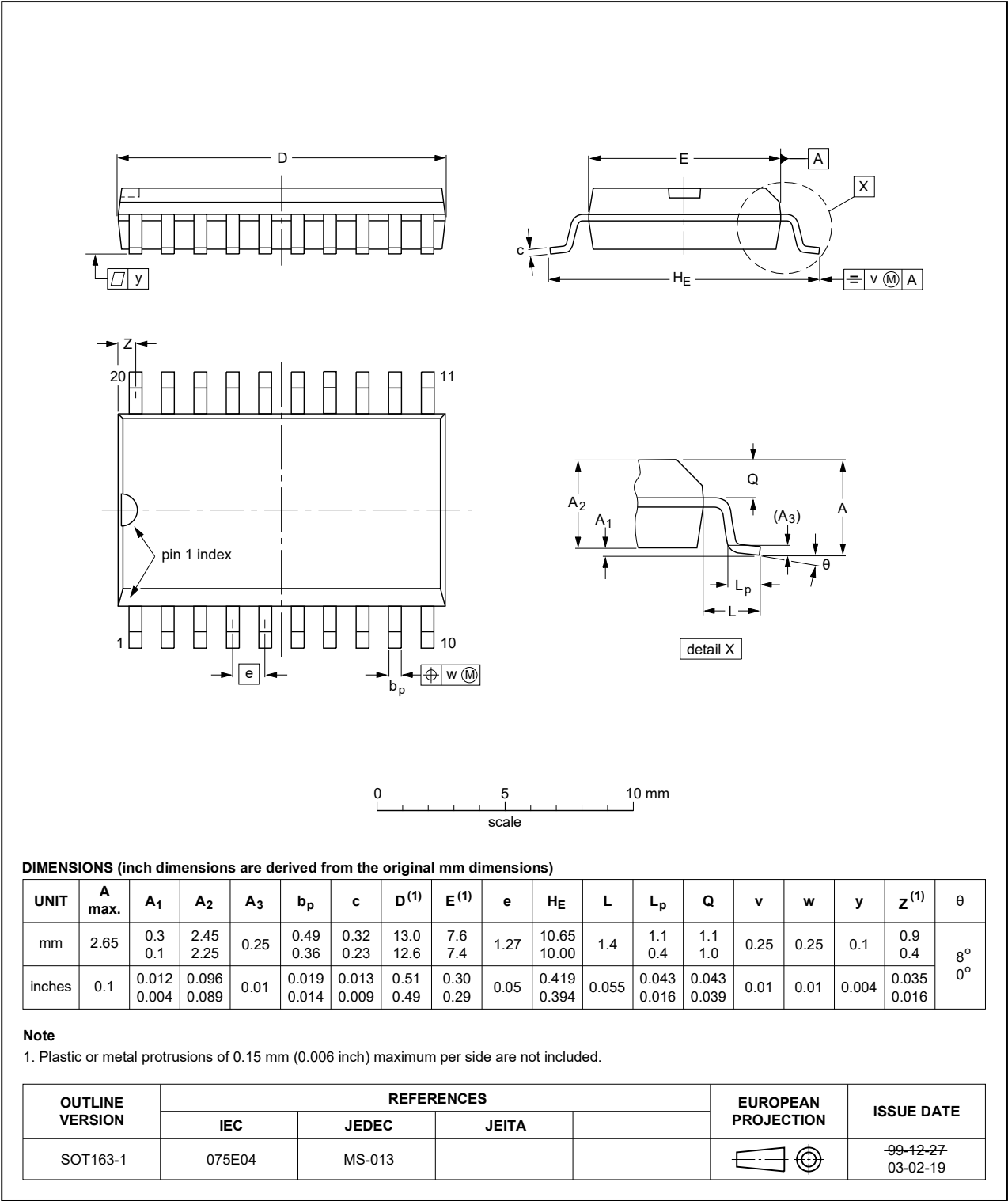


Fig. 11. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

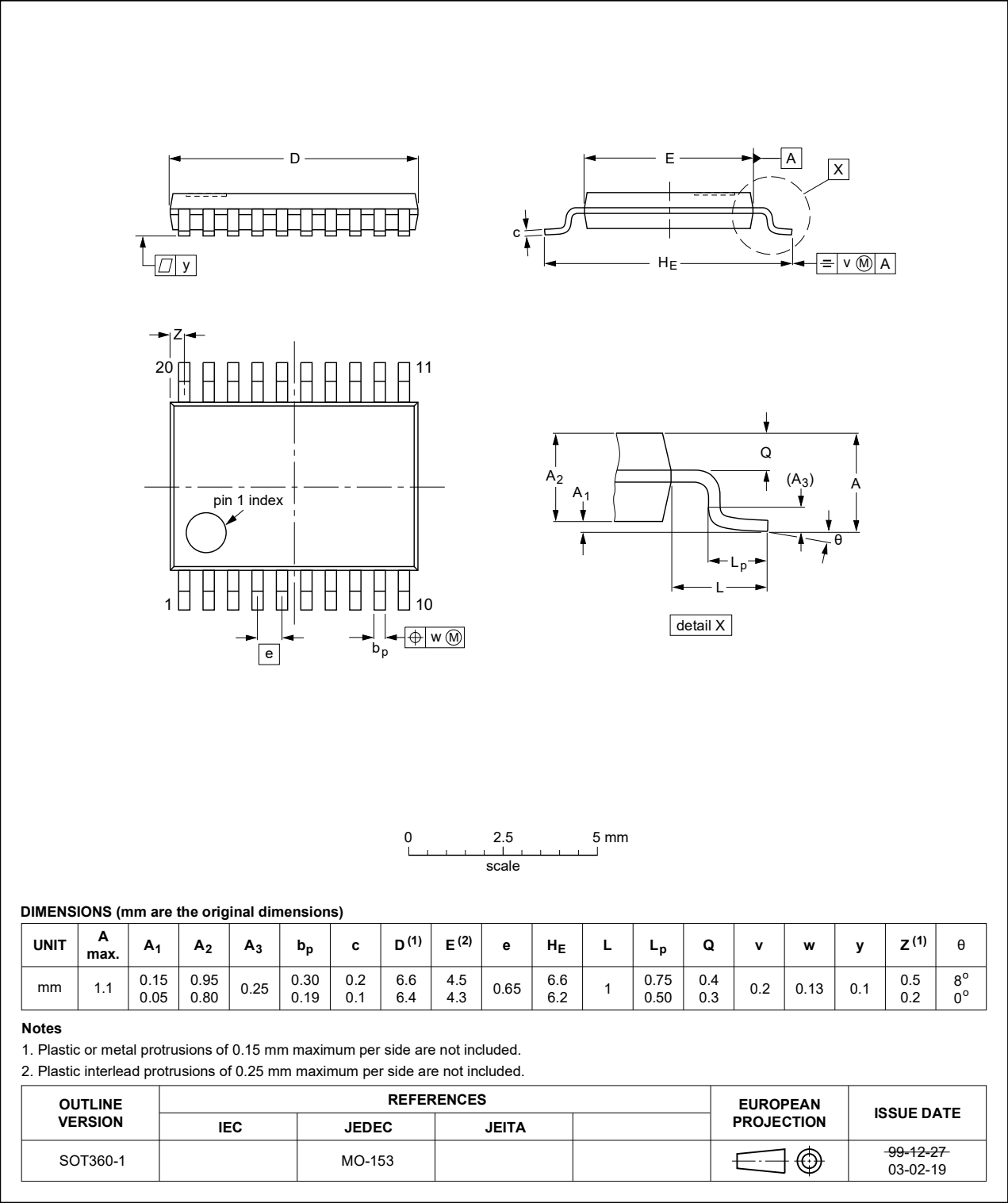


Fig. 12. Package outline SOT360-1 (TSSOP20)

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

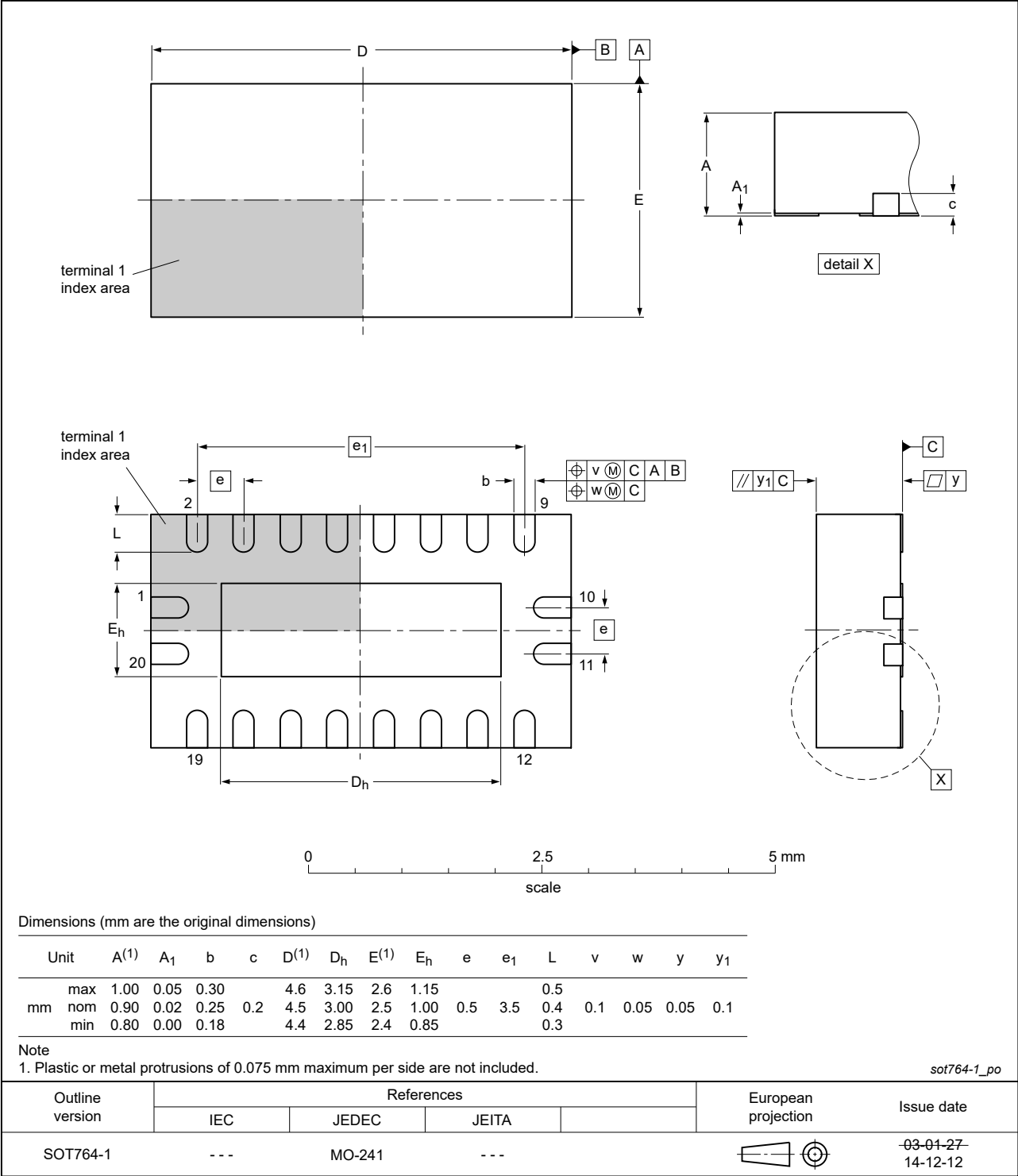


Fig. 13. Package outline SOT764-1 (DHVQFN20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC574A v.6	20210830	Product data sheet	-	74LVC574A v.5
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>Type number 74LVC574ADB (SOT339-1/SSOP20) removed.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 13</a>: Package outline drawing SOT764-1 (DHVQFN20) updated.</li> </ul>			
74LVC574A v.5	20121218	Product data sheet	-	74LVC574A v.4
Modifications:	<ul style="list-style-type: none"> <li>Changed interlacing into interfacing (errata) in features list.</li> </ul>			
74LVC574A v.4	20121203	Product data sheet	-	74LVC574A v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC574A v.3	20040322	Product specification	-	74LVC574A v.2
74LVC574A v.2	20030620	Product specification	-	74LVC574A v.1
74LVC574A v.1	19980729	Product specification	-	-

## 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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