

# ESD Protection Diode Array, 5-Line

## NUP5120X6

This 5-line surge protection array is designed for application requiring surge protection capability. It is intended for use in over-transient voltage and ESD sensitive equipment such as cell phones, portables, computers, printers and other applications. This device features a monolithic common anode design which protects five independent lines in a single SOT-563 package.

### Features

- Protects up to 5 Lines in a Single SOT-563 Package
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body Model and Class C (Exceeding 400 V) per Machine Model.
- Compliance with IEC 61000-4-2 (ESD) 15 kV (Air), 8 kV (Contact)
- This is a Pb-Free Device

### Applications

- Hand Held Portable Applications
- Serial and Parallel Ports
- Notebooks, Desktops, Servers

### MAXIMUM RATINGS (T<sub>J</sub> = 25 °C, unless otherwise specified)

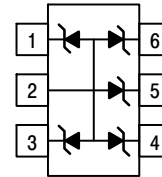
Symbol	Rating	Value	Unit
P <sub>PK</sub> 1	Peak Power Dissipation 8x20 μsec double exponential waveform, (Note 1)	90	W
T <sub>J</sub>	Operating Junction Temperature Range	-40 to 125	°C
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>L</sub>	Lead Solder Temperature – Maximum (10 seconds)	260	°C
ESD	Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Air (ESD) IEC 61000-4-2 Contact (ESD)	16000 400 15000 8000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

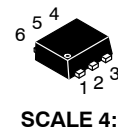
1. Non-repetitive current pulse per Figure 1.

## SOT-563 5-LINE SURGE PROTECTION

### PIN ASSIGNMENT



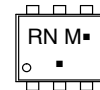
PIN 1. CATHODE  
 2. ANODE  
 3. CATHODE  
 4. CATHODE  
 5. CATHODE  
 6. CATHODE



SCALE 4:1

SOT-563  
 CASE 463A  
 STYLE 6

### MARKING DIAGRAM



RN = Specific Device Code  
 M = Month Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NUP5120X6T1G	SOT-563 (Pb-Free)	4000/Tape & Reel
NUP5120X6T2G	SOT-563 (Pb-Free)	4000/Tape & Reel

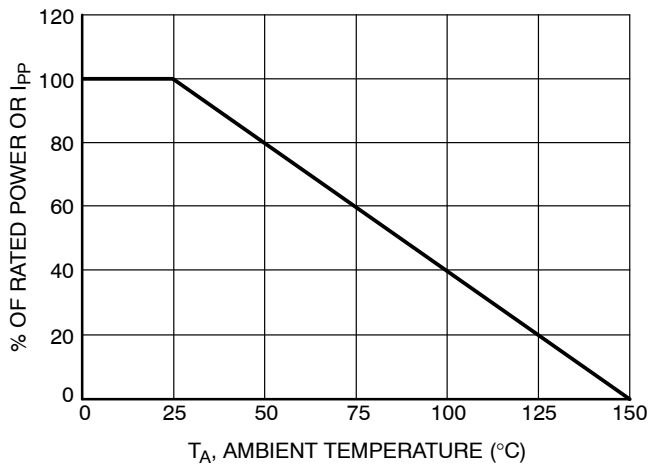
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://BRD8011/D).

## NUP5120X6

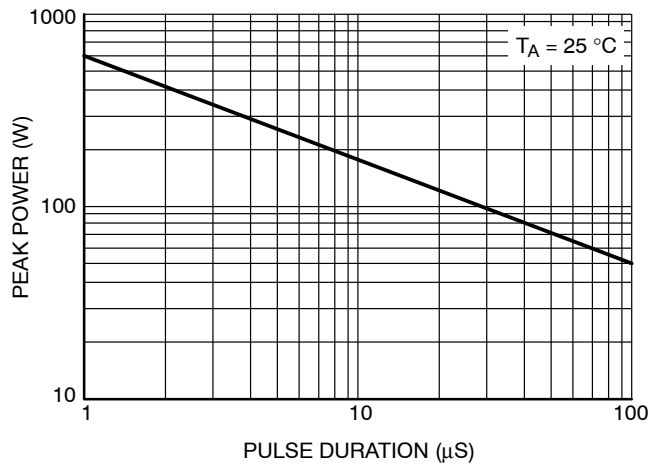
### ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Reverse Working Voltage	(Note 2)	$V_{RWM}$		–	5.0	V
Breakdown Voltage	$I_T = 1\text{ mA}$ , (Note 3)	$V_{BR}$	6.2	6.8	7.2	V
Reverse Leakage Current	$V_{RWM} = 3\text{ V}$	$I_R$	–	0.01	0.5	$\mu\text{A}$
Capacitance	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ (Line to GND) $V_R = 2.5\text{ V}$ , $f = 1\text{ MHz}$ (Line to GND)	$C_J$	–	54	70	pF

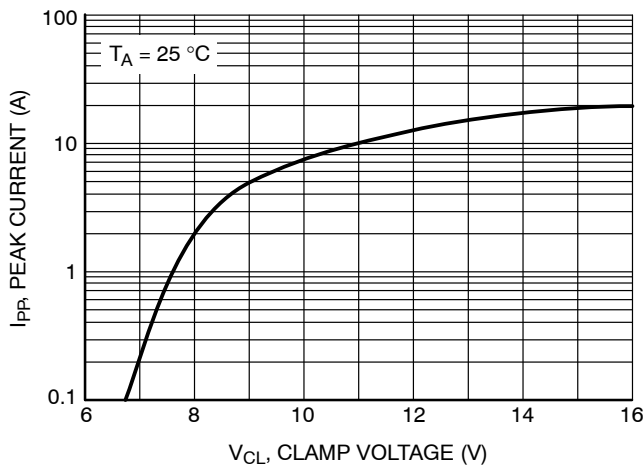
- Surge protection devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
- $V_{BR}$  is measured at pulse test current  $I_T$ .



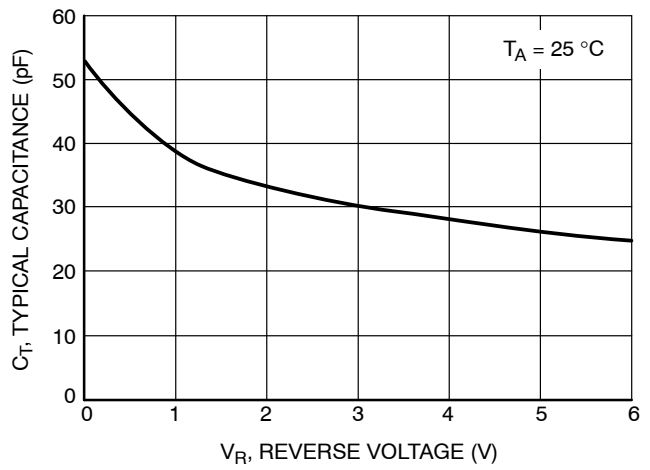
**Figure 1. Power Derating vs. Ambient Temperature**



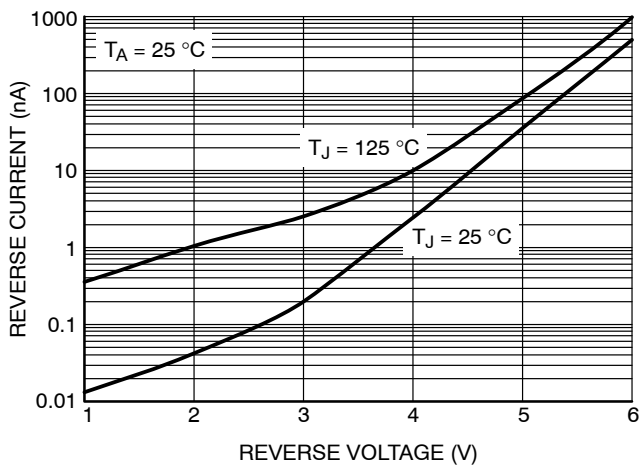
**Figure 2. Peak Power vs. Pulse Duration**



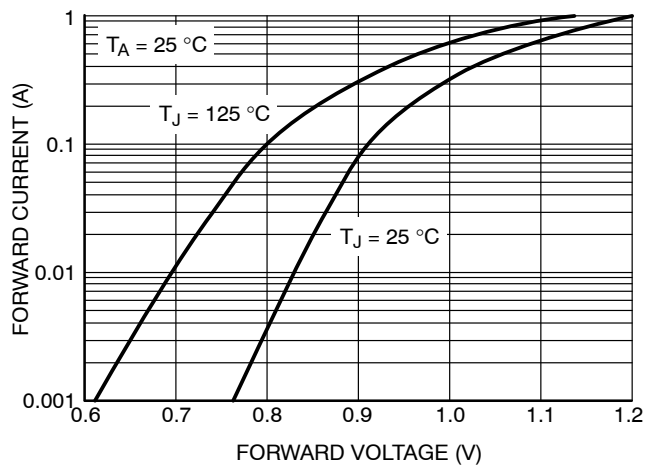
**Figure 3. Peak Current vs. Clamp Voltage**



**Figure 4. Typical Capacitance vs. Reverse Voltage**



**Figure 5. Reverse Current vs. Reverse Voltage**



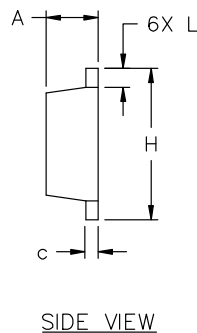
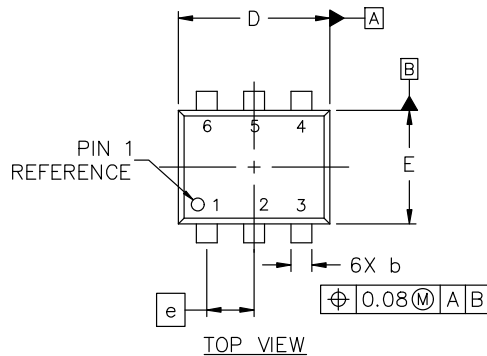
**Figure 6. Typical Forward Current vs. Forward Voltage**


**SOT-563-6 1.60x1.20x0.55, 0.50P**  
**CASE 463A**  
**ISSUE J**

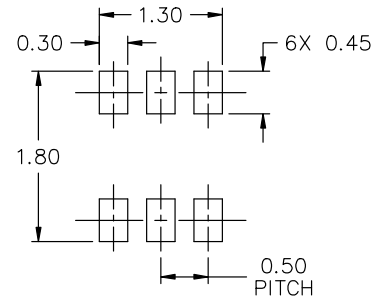
DATE 15 FEB 2024

## NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



## RECOMMENDED MOUNTING FOOTPRINT\*

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

STYLE 1:  
PIN 1. EMITTER 1  
2. BASE 1  
3. COLLECTOR 2  
4. EMITTER 2  
5. BASE 2  
6. COLLECTOR 1

STYLE 2:  
PIN 1. EMITTER 1  
2. EMITTER 2  
3. BASE 2  
4. COLLECTOR 2  
5. BASE 1  
6. COLLECTOR 1

STYLE 3:  
PIN 1. CATHODE 1  
2. CATHODE 1  
3. ANODE/ANODE 2  
4. CATHODE 2  
5. CATHODE 2  
6. ANODE/ANODE 1

STYLE 4:  
PIN 1. COLLECTOR  
2. COLLECTOR  
3. BASE  
4. EMITTER  
5. COLLECTOR  
6. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. CATHODE  
6. CATHODE

STYLE 6:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. CATHODE  
6. CATHODE

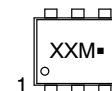
STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. CATHODE  
5. ANODE  
6. CATHODE

STYLE 8:  
PIN 1. DRAIN  
2. DRAIN  
3. GATE  
4. SOURCE  
5. DRAIN  
6. DRAIN

STYLE 9:  
PIN 1. SOURCE 1  
2. GATE 1  
3. DRAIN 2  
4. SOURCE 2  
5. GATE 2  
6. DRAIN 1

STYLE 10:  
PIN 1. CATHODE 1  
2. N/C  
3. CATHODE 2  
4. ANODE 2  
5. N/C  
6. ANODE 1

STYLE 11:  
PIN 1. EMITTER 2  
2. BASE 2  
3. COLLECTOR 1  
4. EMITTER 1  
5. BASE 1  
6. COLLECTOR 2

**GENERIC MARKING DIAGRAM\***


XX = Specific Device Code

M = Month Code

▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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