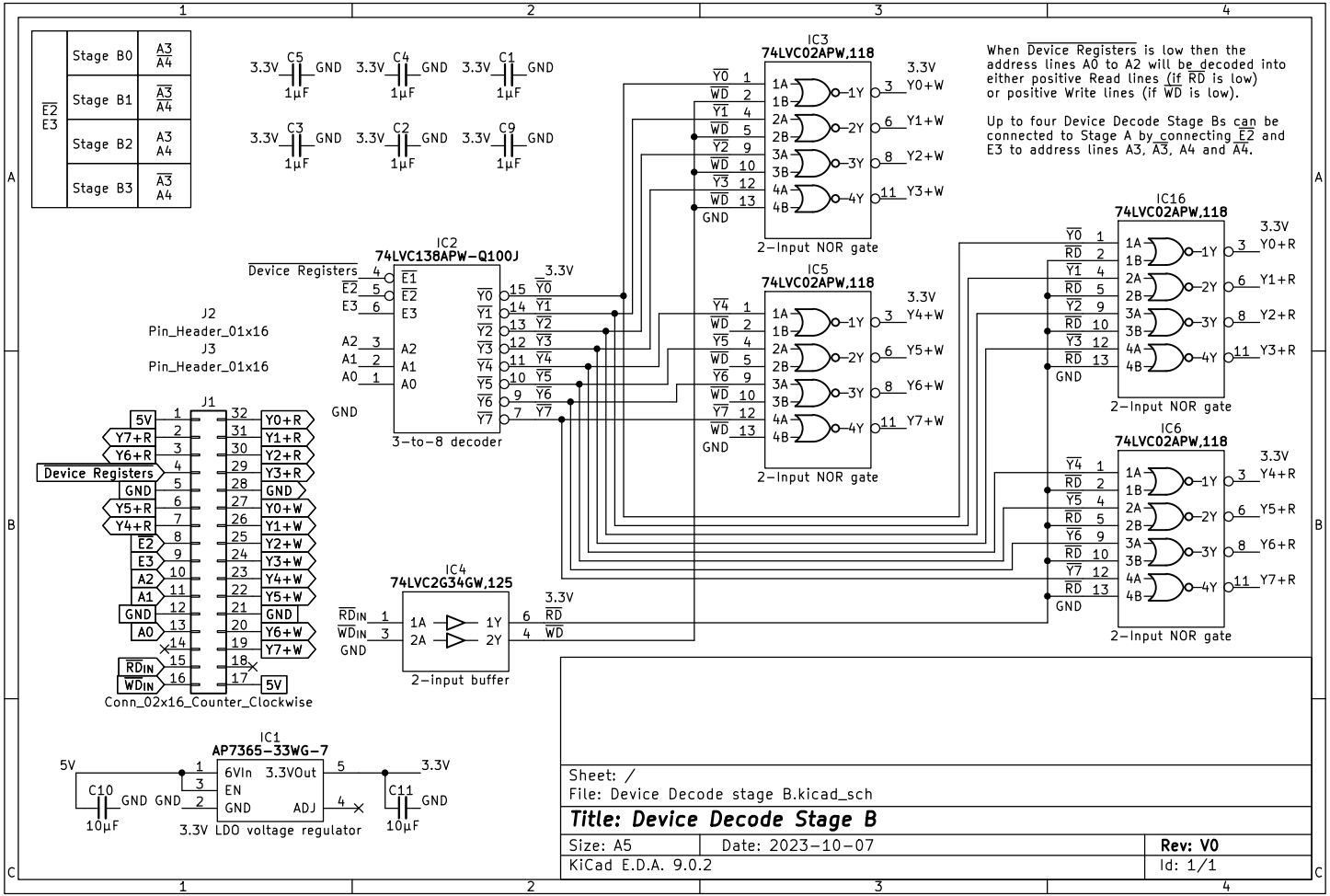
E2
E3
Stage B0
Stage B1
Stage B2
Stage B3
A3
A4
C5
C4
C1
C3
C2
C9
3.3V
GND
1µF
IC3
74LVC02APW,118
IC5
74LVC02APW,118
IC16
74LVC02APW,118
IC6
74LVC02APW,118
2-Input NOR gate
IC2
74LVC138APW-Q100J
Device Registers
3-to-8 decoder
J2
Pin_Header_01x16
J3
Pin_Header_01x16
J1
Conn_02x16_Counter_Clockwise
IC4
74LVC2G34GW,125
2-input buffer
IC1
AP7365-33WG-7
6VIn
3.3VOut
EN
ADJ
C10
10µF
C11
10µF
3.3V LDO voltage regulator
When Device Registers is low then the address lines A0 to A2 will be decoded into either positive Read lines (if RD is low) or positive Write lines (if WD is low).
Up to four Device Decode Stage Bs can be connected to Stage A by connecting E2 and E3 to address lines A3, A3, A4 and A4.
Sheet: /
File: Device Decode stage B.kicad_sch
Title: Device Decode Stage B
Size: A5
Date: 2023-10-07
Rev: V0
KiCad E.D.A. 9.0.2
Id: 1/1