

Readout Board Specifications

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1 Readout Board Specifications

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Status: This document is missing 61 pieces of information concerning 63 specifications

- Specifications are **3.2% complete**.

A pdf version of this document can be found [here](#). Please check the timestamp to ensure it is up to date. The master copy of this document is an emacs org mode file found [here](#).

The latest RB schematic can be found [here](https://gitlab.cern.ch/cms-etl-electronics/readout-board-pcb/uploads/183954f3a47f967752902acf8ae9c3d3/ETL_RB_V1.6.PDF) https://gitlab.cern.ch/cms-etl-electronics/readout-board-pcb/uploads/183954f3a47f967752902acf8ae9c3d3/ETL_RB_V1.6.PDF

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1.1 Description

The readout board will be designed in 3 different flavors, called the RB-3, RB-6, and RB-7, where the suffix number represents the number of “full-modules” that the readout board services.

- An RB-3 will interface with 3 modules, meaning 12 ETROCs and 12 sensors.
- An RB-6 will interface with 6 modules, meaning 24 ETROCs and 24 sensors.
- An RB-7 will interface with 7 modules, meaning 28 ETROCs and 28 sensors.

The readout board consists of one or more lpGBTs, a GBT-SCA, a VTRX+, a number of linPOL12 regulators, and associated connectors / passive components required to interface with the external systems.

- Each RB will have 1 GBT-SCA
- Each RB will have 2 lpGBTs
- Each RB will have 1 VTRX+
- Each RB will have 6 linPOL12s
 - 2 for VTRX+ RX
 - 2 for VTRX+ TX
 - 1 for GBT-SCA analog power
 - 1 for GBT-SCA digital power

1.2 Interfaces

1.2.1 Power Board Interface

The interface to the power board will consist of:

- The power board interface will use connector part number UNKNOWN.
- The pinout of these connectors is UNKNOWN.
- The placement of these connectors is UNKNOWN.
- The quantity of these connectors is UNKNOWN.

1.2.2 Module Interface

1. Mechanical Interface

- the module shall be aligned to the readout board using an UNKNOWN keying mechanism

2. Signal Interface The signal interface to the module will consist of:

- The module will use connector part number UNKNOWN.
- The pinout of the module connectors is UNKNOWN.
- The placement of these connectors is UNKNOWN.

3. BV Interface The signal interface to the module will consist of:

- The BV to module interface will use connector part number UNKNOWN.
- The pinout of these connectors is UNKNOWN.
- The placement of these connectors is UNKNOWN.

1.2.3 Fiber Optic Interface

The fiber optic interface to CMS is through a VTRX+. The readout board will host both the VTRX+, as well as the MT Ferrule that is required to connect between the VTRX+ and a “naked fanout”.

- The size of the cutout for the MT ferrule is UNKNOWN.
- The location of the cutout for the MT ferrule is:
 - RB-3: UNKNOWN.
 - RB-6: UNKNOWN.
 - RB-7: UNKNOWN.

1.2.4 Low Voltage Interface

The readout board will connect to the low voltage supply to receive ~8V power.

- The part number for the LV connector is UNKNOWN.
- The pinout for the LV connector is UNKNOWN.
- The placement for the LV connector is UNKNOWN.

1.2.5 Programming Interface

- The readout board will provide a programming interface to allow fusing/configuration of the lpGBT through I2C.
- The part number for the programming connector is UNKNOWN.
- The pinout for the programming connector is UNKNOWN.
- The placement for the programming connector is UNKNOWN.

1.3 Signal Connectivity

1.3.1 I2C

- The GBT-SCA will provide one I2C connection for each module.
- All ETROCs in a module will share an I2C master.
- The readout board will provide strong I2C pull-ups.
 - It is assumed that the modules will not, and have only weak pull-ups.

1.3.2 IO

- A GBT-SCA provides 32 tri-stateable 1.5V GPIO
- An LPGBT provides 16 tri-stateable 1.2V GPIO
- These IO will be allocated as:

Table 1: Allocation of GPIO on the readout board

	RB-3	RB-6	RB-7
GBT-SCA RESETB	1	1	1
VTRX LD_RESETB	1	1	1
VTRX LD_DIS	1	1	1
Module Reset	3	6	7
PB PGOOD	<u>UNKNOWN</u>	<u>UNKNOWN</u>	<u>UNKNOWN</u>
PB EN	<u>UNKNOWN</u>	<u>UNKNOWN</u>	<u>UNKNOWN</u>

1.3.3 Uplinks

Uplinks carry data from the front-end to the back-end.

- These uplinks will **not** be phase length matched.

1. Quantity

- RB-3 will have UNKNOWN uplinks
- RB-6 will have UNKNOWN uplinks
- RB-7 will have UNKNOWN uplinks

2. Data Rates

- RB-3 will operate at up to UNKNOWN Mbps
- RB-6 will operate at up to UNKNOWN Mbps
- RB-7 will operate at up to UNKNOWN Mbps

1.3.4 Downlinks

Downlinks carry data from the back-end to the front-end.

- The readout board will deliver to each module two downlinks that provide a “fast command” interface to the ETROC.
- These fast-command downlinks will run at UNKNOWN Mbps.
- The fast command downlinks will be multi-dropped on the module, with each downlink serving 2 ETROCs.
 - 6 downlinks for the RB-3, 12 downlinks for the RB-6, and 14 downlinks for the RB-7.
- These downlinks will **not** be phase length matched *between* modules, but **will** be phase length matched *within* modules and to their respective clocks.

1.3.5 Clocking

- The readout board will be responsible for delivering a 40 MHz point-to-point clock to each of the ETROCs it connects to.
 - 12 clocks for the RB-3, 24 clocks for the RB-6, and 28 clocks for the RB-7.
- These clocks will **not** be phase length matched *between* modules, but **will** be phase length matched *within* modules.
- The clock will be distributed only from the **master** IpGBT; the slave IpGBT clock outputs will not be used due to radiation intolerance.

1.3.6 VTRX

1.4 Monitoring

A GBT-SCA ASIC provides 31 analog inputs with 12-bit resolution, and 4 analog outputs with 8-bit resolution, with a range of 0 to 1V.

An IpGBT provides 8 analog inputs with 10-bit resolution and 1 analog output with 12-bit resolution. The readout board will monitor the following analog channels:

1.4.1 Voltage Monitoring

- All voltage dividers will be formed of 0.5% tolerance resistors.
- All voltage dividers will be decoupled by 0.1 uF capacitors.
- The ETROC voltage monitors assume that a 1.2k resistor is in series with the 1V2_MON signal from the module.

1.5 Low Voltage Distribution

- The readout board will provide four 47 uF capacitors connected to each 1.2V ETROC supply.
 - There will be no additional filtering.
- Analog and digital power for the ETROC will not be distinguished.
- The low voltage will be ganged such that UNKNOWN ETROCs share a common power supply.

1.6 Bias Voltage Distribution

- Bias voltage will be a maximum of UNKNOWN volts.
- The bias voltage granularity will be:
 - UNKNOWN channels for an RB-3
 - UNKNOWN channels for an RB-6
 - UNKNOWN channels for an RB-7
- The readout board will provide a filter for each bias voltage channel consisting of a 200 ohm resistor and 1500 pF capacitor, which will be rated for at least 1000V.

1.7 Mechanics

1.7.1 Outer Dimensions

- The outer dimension of the readout board will follow an UNKNOWN shape

1.7.2 Screw Holes & Sizes

- The readout board will have UNKNOWN mounting holes of size UNKNOWN in the following locations:

1. UNKNOWN

1.7.3 Thickness

- The readout board will be 1.0mm thick with a manufacturing specification of $\pm 10\%$.

Table 2: Allocation of monitoring signals on the readout board

Type	Monitored By	Divider	LSB	Range	Qty. RB-3	Qty. RB-6	Qty. RB-7
Sensor BV	GBT-SCA	82/100082	2.980e-01 V	1220.3 V	UNKNOWN	UNKNOWN	UNKNOWN
ETROC +1.2V	GBT-SCA	2.0/4.2	5.128e-04 V	2.1 V	UNKNOWN	UNKNOWN	UNKNOWN
PB +1.2V	GBT-SCA	2.0/4.2	5.128e-04 V	2.1 V	UNKNOWN	UNKNOWN	UNKNOWN
RB LV	GBT-SCA	1/11	2.686e-03 V	11.0 V	1	1	1
VTRX +2.5V RX	lpGBT	1.5/4.5	2.933e-03 V	3.0 V	1	1	1
VTRX +2.5V TX	lpGBT	1.5/4.5	2.933e-03 V	3.0 V	1	1	1
GBTX +1.5VD	lpGBT	2.0/3.5	1.711e-03 V	1.8 V	1	1	1
GBTX +1.5VA	lpGBT	2.0/3.5	1.711e-03 V	1.8 V	1	1	1
VTRX Temp	lpGBT				1	1	1
RB Temp	GBT-SCA				1	1	1
PB Temp	UNKNOWN				1	1	1
Module Temp	UNKNOWN				UNKNOWN	UNKNOWN	UNKNOWN
VTRX RSSI	lpGBT				1	1	1

1.7.4 Drawings

A drawing of the readout board is available at UNKNOWN.

1.8 Component List