Module PCB Specifications

Andrew Peck, Daniel Spitzbart

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1 Module Specifications

- Authors: Andrew Peck, Daniel Spitzbart
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2 Specifications

2.1 Description

2.2 Layout

We denote the "top" side of the PCB as that containing the module and BV connectors.

We denote the "bottom" side of the PCB as that containing the sensor.

2.2.1 Sensor Placement

- **Spec:** The dimensions of a Sensor+ETROC assembly is UNKNOWN $\times$ UNKNOWN mm.
- The position of the two Sensor+ETROC assemblies are (positions relative to UNKNOWN):
  - **Spec:** x= UNKNOWN mm; y= UNKNOWN mm.
  - **Spec:** x= UNKNOWN mm; y= UNKNOWN mm.

2.2.2 Wire bonding

- **Spec:** A wire bonding diagram of an ETROC is shown in UNKNOWN
- **Spec:** The pad pitch will be UNKNOWN mm.
- **Spec:** The pad aperture will be UNKNOWN $\times$ UNKNOWN mm.
- **Spec:** The pad aperture will be NSMD (non-solder-mask-defined) with the mask oversized by UNKNOWN mm.
- **Spec:** The wire bond pads will be located UNKNOWN mm from the edge of the ETROC (measured edge-to-edge).

2.2.3 Grounding

- **Spec:** The RB will geometrically isolate analog and digital ground, with specified areas of the PCB filled by a digital ground pour, and others filled by an analog ground pour. The digital and analog grounds will be connected together at a single point.
  - A drawing of the grounding scheme is shown in UNKNOWN.

2.2.4 Fiducial Markings

- **Spec:** The module PCB will have on its bottom side 4 fiducial markers, composed of circles with crosses through them. These markers shall be placed at:

  1. UNKNOWN
  2. UNKNOWN
  3. UNKNOWN
  4. UNKNOWN

2.3 Connectivity

2.3.1 Readout Board Interface

1. Signal Interface The signal interface to the readout board will consist of:

   - **Spec:** The readout board will use connector part number UNKNOWN.
   - **Spec:** The pinout of the readout board connectors is UNKNOWN.
   - **Spec:** The placement of these connectors is UNKNOWN.

2. BV Interface The BV interface to the readout board will consist of:

   - **Spec:** The BV to readout board interface will use connector part number UNKNOWN.
   - **Spec:** The pinout of these connectors is UNKNOWN.
   - **Spec:** The placement of these connectors is UNKNOWN.

2.3.2 I2C

- **Spec:** The module PCB will provide independent I2C addresses for each ETROC on a module. Addresses will be 0/1/2/3 corresponding to the slot, and are set directly by wire bonds.
  - Addresses **will not** be set by resistors, and can not be modified.
- **Spec:** The module PCB will **not** provide pull-up resistors on I2C lines. These will be provided by the host-system.

2.3.3 Low Voltage

- **Spec:** Each module will receive two *possibly* independent +1.2V supplies.
  - They will not be connected together in any way on the module, but *may* be ganged together on the RB.
- LV wire bonding is described in the Wire Bonding section

1. Decoupling

- **Spec:** The module will provide decoupling capacitors on the +1.2V supplies. The power filtering network will be composed of:
  (a) UNKNOWN resistors of UNKNOWN value
  (b) UNKNOWN resistors of UNKNOWN value
- **Spec:** Decoupling capacitors will be placed as close as possible to the ETROC, and follow standard practices to maintain low inductance connections.
- **Spec:** Decoupling capacitors will be suitably rated to minimize DC bias effects.
- **Spec:** To reduce temperature dependence, ceramics will be chosen where possible with minimal temperature dependence (e.g. X7R).

2. Monitoring

   - **Spec:** The module will provide **two** feedback voltages for point-of-load monitoring. It will be delivered back to the RB through a 1.2k 0.5% resistor. These point-of-load monitoring resistors will be placed close to each pair of ETROCs at their respective ends of the module.

2.3.4 Bias Voltage

- The module will deliver bias voltage to the ETROC
- BV will be a maximum of UNKNOWN volts.
- BV wire bonding is described in the Wire Bonding section

1. Decoupling

   - **Spec:** UNKNOWN

2.3.5 Signal Connectivity

- **Spec:** Each module will receive two UNKNOWN MHz downlinks from the RB
- **Spec:** Each module will receive four 40 MHz clocks from the RB
  - **Spec:** The clocks shall be length matched and skewed such that for a multi-drop pair of lpGBTs, the clock and data are synchronized at each ETROC's input pads.
- **Spec:** Each module will have UNKNOWN uplinks operating at up to UNKNOWN Mbps.
- **Spec:** The module will host UNKNOWN temperature sensors, which will be monitored in the RB.

2.4 Mechanics

2.4.1 Outer Dimensions

- **Spec:** The outer dimension of the Module PCB will follow a rectangular shape, with dimensions of UNKNOWN $\times$ UNKNOWN.

2.4.2 Screw Holes & Sizes

- **Spec:** The Module PCB will have UNKNOWN mounting holes of size UNKNOWN in the following locations:

    1. UNKNOWN

2.4.3 Thickness

- **Spec:** The Module PCB will be 0.5mm thick with a manufacturing specification of $\pm$ 10%.

2.4.4 Drawings

A drawing of the Module PCB is available at UNKNOWN.

2.4.5 Mechanical Interface

- **Spec:** the module shall be aligned to the Readout Board using an UNKNOWN keying mechanism