15.1.1. CHIPID

[0x000] CHIPID0

Stores bits 31:24 of the CHIPID

Bit 7:0 - ChipID[31:24] - Bits 31:24 of the CHIPID

See also: [0x001] CHIPID1, [0x002] CHIPID2, [0x003] CHIPID3

[0x001] CHIPID1

Stores bits 23:16 of the CHIPID

Bit 7:0 - ChipID[23:16] - Bits 23:16 of the CHIPID

See also: [0x000] CHIPID0, [0x002] CHIPID2, [0x003] CHIPID3

[0x002] CHIPID2

Stores bits 15:8 of the CHIPID

Bit 7:0 - ChipID[15:8] - Bits 15:8 of the CHIPID

See also: [0x000] CHIPID0, [0x001] CHIPID1, [0x003] CHIPID3

[0x003] CHIPID3

Stores bits 7:0 of the CHIPID

Bit 7:0 - ChipID[7:0] - Bits 7:0 of the CHIPID

See also: [0x000] CHIPID0, [0x001] CHIPID1, [0x002] CHIPID2

[0x004] USERID0

Stores bits 31:24 of the USERID

Bit 7:0 - UserID[31:24] - Bits 31:24 of the USERID

[0x005] USERID1

Stores bits 23:16 of the USERID

Bit 7:0 - UserID[23:16] - Bits 23:16 of the USERID

[0x006] USERID2

Stores bits 15:8 of the USERID

Bit 7:0 - UserID[15:8] - Bits 15:8 of the USERID

[0x007] USERID3

Stores bits 7:0 of the USERID

Bit 7:0 - UserID[7:0] - Bits 7:0 of the USERID

15.1.2. Calibration Data

[0x008] DACCal0

Calibration data for the voltage DAC. Usage is TBD.

Bit 7:0 - DACCalMinCode[7:0] - Calibration data for the voltage DAC. Usage is TBD.

[0x009] DACCal1

Calibration data for the voltage DAC. Usage is TBD.

Bit 7:0 - DACCalMaxCode[7:0] - Calibration data for the voltage DAC. Usage is TBD.

[0x00a] DACCal2

Calibration data for the voltage DAC. Usage is TBD.

Bit 7:4 - DACCalMinCode[11:8] - Calibration data for the voltage DAC. Usage is TBD.

Bit 3:0 - DACCalMaxCode[11:8] - Calibration data for the voltage DAC. Usage is TBD.

[0x00b] ADCCal0

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain2SeHigh[7:0] - Calibration data for the ADC. Usage is TBD.

[0x00c] ADCCal1

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain2SeLow[7:0] - Calibration data for the ADC. Usage is TBD.

[0x00d] ADCCal2

Calibration data for the ADC.Usage is TBD.

Bit 7:4 - ADCCalGain2SeHigh[11:8] -

Bit 3:0 - ADCCalGain2SeLow[11:8] -

[0x00e] ADCCal3

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain2DifHigh[7:0] - Calibration data for the ADC. Usage is TBD.

[0x00f] ADCCal4

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain2DifLow[7:0] - Calibration data for the ADC. Usage is TBD.

[0x010] ADCCal5

Calibration data for the ADC.Usage is TBD.

Bit 7:4 - ADCCalGain2DifHigh[11:8] -

Bit 3:0 - ADCCalGain2DirfLow[11:8] -

[0x011] ADCCal6

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain4DifHigh[7:0] - Calibration data for the ADC. Usage is TBD.

[0x012] ADCCal7

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain4DifLow[7:0] - Calibration data for the ADC. Usage is TBD.

[0x013] ADCCal8

Calibration data for the ADC.Usage is TBD.

Bit 7:4 - ADCCalGain4DifHigh[11:8] -

Bit 3:0 - ADCCalGain4DirfLow[11:8] -

[0x014] ADCCal9

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain8DifHigh[7:0] - Calibration data for the ADC. Usage is TBD.

[0x015] ADCCal10

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain8DifLow[7:0] - Calibration data for the ADC. Usage is TBD.

[0x016] ADCCal11

Calibration data for the ADC.Usage is TBD.

Bit 7:4 - ADCCalGain8DifHigh[11:8] -

Bit 3:0 - ADCCalGain8DirfLow[11:8] -

[0x017] ADCCal12

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain16DifHigh[7:0] - Calibration data for the ADC. Usage is TBD.

[0x018] ADCCal13

Calibration data for the ADC.Usage is TBD.

Bit 7:0 - ADCCalGain16DifLow[7:0] - Calibration data for the ADC. Usage is TBD.

[0x019] ADCCal14

Calibration data for the ADC.Usage is TBD.

Bit 7:4 - ADCCalGain16DifHigh[11:8] -

Bit 3:0 - ADCCalGain16DirfLow[11:8] -

[0x01a] TEMPCalH

Calibration data for the temperature sensor.

Bit 7:0 - TEMPCal[15:8] - Calibration data for the temperature sensor. Usage is TBD.

[0x01b] TEMPCalL

Calibration data for the temperature sensor.

Bit 7:0 - TEMPCal[7:0] - Calibration data for the temperature sensor. Usage is TBD.

[0x01c] VREFCNTR

Voltage reference control.

Bit 7 - VREFEnable - Enable internal voltage reference.

Bit 5:0 - VREFTune[5:0] - Tuning world for internal voltage reference.

[0x01d] CURDACCalH

Calibration data for current DAC. Usage is TBD.

Bit 7:0 - CURDACCal[15:8] - Calibration data for current DAC. Usage is TBD.

[0x01e] CURDACCalL

Calibration data for current DAC. Usage is TBD.

Bit 7:0 - CURDACCal[7:0] - Calibration data for current DAC. Usage is TBD.

[0x01f] EPRXLOCKFILTER

Lock filter settings for DLL in ePortRxGroups.

Bit 7:4 - EPRXLockThreshold[3:0] - Sets the lock threshold value of the instant lock low pass filter for ePortRx DLL's (default: 5)

Bit 3:0 - EPRXReLockThreshold[3:0] - Sets the relock threshold value of the instant lock low pass filter for ePortRx DLL's (default: 5)

15.1.3. Clock Generator

[0x020] CLKGConfig0

Bit 7:4 - CLKGCalibrationEndOfCount[3:0] - Selects the VCO calibration race goal in number of clock cycles between refClk (refClkCounter) and vco\_40MHz (vcoClkCounter) (2^(CLKGCalibrationEndOfCount[3:0]+1)); default: 12

Bit 3:0 - CLKGBiasGenConfig[3:0] - Bias DAC for the charge pumps [0 : 8 : 120] uA; default: 8

[0x021] CLKGConfig1

Bit 7 - CDRControlOverrideEnable - Enables the control override of the state machine; default: 0

Bit 6 - CLKGDisableFrameAlignerLockControl - Disables the use of the frame aligner's lock status; default: 0

Bit 5 - CLKGCDRRes - CDR's filter resistance; default: 1 when in RX/TRX mode, 0 when in TX mode

Bit 4 - CLKGVcoRailMode - VCO rail mode; [0: voltage mode, fixed to VDDRX; 1: current mode, value selectable using CLKGVcoDAC (default)]

Bit 3:0 - CLKGVcoDAC[3:0] - Current DAC for the VCO [0: 0.470 : 7.1] mA; default: 8

[0x022] CLKGPllRes

Bit 7:4 - CLKGPllResWhenLocked[3:0] - PLL's filter resistance when PLL is locked [R = 1/2 \* 79.8k / CONFIG] Ohm; default: 4; set to 0 if RX or TRX mode

Bit 3:0 - CLKGPllRes[3:0] - PLL's filter resistance when PLL is locking [R = 1/2 \* 79.8k / CONFIG] Ohm; default: 4; set to 0 if RX or TRX mode

[0x023] CLKGPLLIntCur

Bit 7:4 - CLKGPLLIntCurWhenLocked[3:0] - PLL's integral current path when in locked state [0 : 1.1 : 8] uA; default: 5

Bit 3:0 - CLKGPLLIntCur[3:0] - PLL's integral current path when in locking state [0 : 1.1 : 8] uA; default: 5

[0x024] CLKGPLLPropCur

Bit 7:4 - CLKGPLLPropCurWhenLocked[3:0] - PLL's proportional current path when in locked state [0 : 5.46 : 82] uA; default: 5

Bit 3:0 - CLKGPLLPropCur[3:0] - PLL's proportional current path when in locking state [0 : 5.46 : 82] uA; default: 5

[0x025] CLKGCDRPropCur

Bit 7:4 - CLKGCDRPropCurWhenLocked[3:0] - CDR's Alexander phase detector proportional current path when in locked state [0 : 5.46 : 82] uA; default: 5

Bit 3:0 - CLKGCDRPropCur[3:0] - CDR's Alexander phase detector proportional current path when in locking state [0 : 5.46 : 82] uA; default: 5

[0x026] CLKGCDRIntCur

Bit 7:4 - CLKGCDRIntCurWhenLocked[3:0] - CDR's Alexander phase detector integral current path when in locked state [0 : 5.46 : 82] uA; default: 5

Bit 3:0 - CLKGCDRIntCur[3:0] - CDR's Alexander phase detector integral integral current path when in locking state [0 : 5.46 : 82] uA; default: 5

[0x027] CLKGCDRFFPropCur

Bit 7:4 - CLKGCDRFeedForwardPropCurWhenLocked[3:0] - CDR's proportional feed forward current path when in locked state [0 : 5.46 : 82] uA; default: 5

Bit 3:0 - CLKGCDRFeedForwardPropCur[3:0] - CDR's proportional feed forward current path when in locking state [0 : 5.46 : 82] uA; default: 5

[0x028] CLKGFLLIntCur

Bit 7:4 - CLKGFLLIntCurWhenLocked[3:0] - CDR's frequency detector charge pump when in locked state [0 : 5.46 : 82] uA; default: 0

Bit 3:0 - CLKGFLLIntCur[3:0] - CDR's frequency detector charge pump when in locking state [0 : 5.46 : 82] uA; default: 5

[0x029] CLKGFFCAP

Bit 7 - CDRCOConnectCDR - Enables the connectCDR switch [0 - disable, 1 - enable] (only when CDRControlOverrideEnable is 1)

Bit 6 - CLKGCapBankOverrideEnable - Enables the override of the capacitor search during VCO calibration [0 - disable, 1 - enable]; default: 0

Bit 5:3 - CLKGFeedForwardCapWhenLocked[2:0] - CDR's feed forward filter's capacitance when in locked state [0: 44 : 308] fF; default: 3

Bit 2:0 - CLKGFeedForwardCap[2:0] - CDR's feed forward filter's capacitance when in locking state [0: 44 : 308] fF; default: 3

[0x02a] CLKGCntOverride

Bit 7 - CLKGCOoverrideVc - Forces the VCO's control voltage to be in mid range [0 - disable, 1 - enable] (only when CDRControlOverrideEnable is 1)

Bit 6 - CDRCORefClkSel - Forces the reference clock selection for the VCO calibration [0 - data/4, 1 - external refClk] (only when CDRControlOverrideEnable is 1)

Bit 5 - CDRCOEnablePLL - Enables the enablePLL switch [0 - disable, 1 - enable] (only when CDRControlOverrideEnable is 1)

Bit 4 - CDRCOEnableFD - Enables the frequency detector [0 - disable, 1 - enable] (only when CDRControlOverrideEnable is 1)

Bit 3 - CDRCOEnableCDR - Enables the enableCDR switch [0 - disable, 1 - enable] (only when CDRControlOverrideEnable is 1)

Bit 2 - CDRCODisDataCounterRef - Enables the data/4 ripple counter [1 - disable, 0 - enable] (only when CDRControlOverrideEnable is 1)

Bit 1 - CDRCODisDESvbiasGen - Enables the vbias for the CDR [1 - disable, 0 - enable] (only when CDRControlOverrideEnable is 1)

Bit 0 - CDRCOConnectPLL - Enables the connectPLL switch [0 - disable, 1 - enable] (only when CDRControlOverrideEnable is 1)

[0x02b] CLKGOverrideCapBank

Bit 7:0 - CLKGCapBankSelect[7:0] - Selects the capacitor bank value for the VCO [check attached table] (only when CLKGCapBankOverrideEnable is 1); default: n/a

[0x02c] CLKGWaitTime

Bit 7:4 - CLKGwaitCDRTime[3:0] - ljCDR state machine waiting for lock, RX/TRX mode, (16'h0001 << waitCDRTime); (only when CLKGDisableFrameAlignerLockControl == 1); default: 8

Bit 3:0 - CLKGwaitPLLTime[3:0] - ljCDR state machine waiting for lock, TX mode, (16'h0001 << waitPLLTime); (only when lfEnable == 0); default: 8

[0x02d] CLKGLFConfig0

Bit 7 - CLKGLockFilterEnable - Enables the lock filter on the instant lock signal; only in TX mode [0 - disable, 1 enable]; default: 1

Bit 4 - CLKGCapBankSelect[8] - Selects the capacitor bank value for the VCO [check attached table] (only when CLKGCapBankOverrideEnable is 1); default: n/a

Bit 3:0 - CLKGLockFilterLockThrCounter[3:0] - Sets the lock threshold value of the instant lock low pass filter (16'h0001 << lfLockThrCounter); only in TX mode; default: after SEU

[0x02e] CLKGLFConfig1

Bit 7:4 - CLKGLockFilterReLockThrCounter[3:0] - Sets the relock threshold value of the instant lock low pass filter (16'h0001 << lfReLockThrCounter); only in TX mode; default: after SEU

Bit 3:0 - CLKGLockFilterUnLockThrCounter[3:0] - Sets the unlock threshold value of the instant lock low pass filter (16'h0001 << lfUnLockThrCounter); only in TX mode; default: after SEU

[0x02f] FAMaxHeaderFoundCount

Frame aligner configuration register.

Bit 7:0 - FAMaxHeaderFoundCount[7:0] - The number of consecutive valid frame headers that have to be detected before frame lock is assumed.

[0x030] FAMaxHeaderFoundCountAfterNF

Frame aligner configuration register.

Bit 7:0 - FAMaxHeaderFoundCountAfterNF[7:0] - The number of consecutive detected valid headers to be found to clear the invalid frame count. The reset can happen only if the number of detected invalid headers does not exceed the FAMaxHeaderNotFoundCount[7:0].

[0x031] FAMaxHeaderNotFoundCount

Frame aligner configuration register.

Bit 7:0 - FAMaxHeaderNotFoundCount[7:0] - The maximum number of invalid headers (consecutive or not) that can be received before the frame is considered misaligned.

[0x032] FAFAMaxSkipCycleCountAfterNF

Frame aligner configuration register.

Bit 7:0 - FAMaxSkipCycleCountAfterNF[7:0] - The maximum number of skip cycles (consecutive or not) that can be issued CRD is considered to be unlocked.

[0x033] PSDllConfig

Configuration for phase-shifter DLL

Bit 7:4 - EPRXUnLockThreshold[3:0] - Sets the unlock threshold value of the instant lock low pass filter for ePortRx DLL's (default: 5)

Bit 3:2 - PSDLLConfirmCount[1:0] - Number of clock cycles (in the 40 MHz clock domain) to confirm locked state.

PSDLLConfirmCount[1:0] Number of clock cycles

2'd0 1

2'd1 4

2'd2 16

2'd3 31

Bit 1:0 - PSDllCurrentSel[1:0] - Current for the DLL charge pump

PSDllCurrentSel[1:0] Current [uA]

2'd0 1

2'd1 2

2'd2 4

2'd3 8

[0x034] EPRXDllConfig

DLL configuration register

Bit 7:6 - EPRXDllCurrent[1:0] - Current for the DLL charge pump

EPRXDllCurrent[1:0] Current [uA]

2'd0 1

2'd1 2

2'd2 4

2'd3 8

Bit 5:4 - EPRXDLLConfirmCount[1:0] - Number of clock cycles (in the 40 MHz clock domain) to confirm locked state.

EPRXDLLConfirmCount[1:0] Number of clock cycles

2'd0 1

2'd1 4

2'd2 16

2'd3 31

Bit 3 - EPRXDLLFSMClkAlwaysOn - Force clock of ePortRx DLL state machine to be always enabled (disables clock gating).

Bit 2 - EPRXDLLCoarseLockDetection - Use coarse detector for the DLL lock condition.

Bit 1 - EPRXEnableReInit - Allow re-initialization in ePortRxGroup when the tuning is out of range.

Bit 0 - EPRXDataGatingEnable - Enable data gating.

[0x035] FORCEEnable

Enables user to enable specific sub-circuits regardless of the operation mode

Bit 7 - ForceTxEnable - Enable the TX logic regardless of the operation mode

Bit 6 - ForceRxEnable - Enable the RX logic regardless of the operation mode

Bit 5 - LDForceEnable - Enables the Line Driver, regardless of the operation mode, when one of the loop-backs is selected.

Bit 4 - TESTCLKForceEnable - Enable the test clock input pad regardless of the operation mode.

Bit 3 - I2CMclkAlwaysEnable - I2C masters clock always enable (disable clock gating).

Bit 2 - PSFSMClkAlwaysOn - Forces an initialization state machine clock to be always active (disables clock gating)

15.1.4. CHIP Config

[0x036] ChipConfig

Bit 7 - highSpeedDataOutInvert - Inverts high speed data output lines (equivalent to swapping HSOUTP and HSOUTN on the PCB)

Bit 6 - highSpeedDataInInvert - Inverts high speed data input lines (equivalent to swapping HSINP and HSINN on the PCB)

Bit 2:0 - ChipAddressBar[2:0] - Sets most significant bits of the chip address (see Section 3.3).

15.1.5. Equalizer

[0x037] EQConfig

Main equalizer configuration register

Bit 4:3 - EQAttenuation[1:0] - Attenuation of the equalizer. Use a gain setting of 1/1 (EQAttenuation[1:0]=2'd3) when VTRX+ is used.

EQAttenuation[1:0] Gain [V/V]

2'd0 1/3

2'd1 2/3

2'd2 2/3

2'd3 1/1

Bit 1:0 - EQCap[1:0] - Capacitance select for the equalizer

EQCap[1:0] Capacitance [fF]

2'd0 0

2'd1 70

2'd2 70

2'd3 140

[0x038] EQRes

Resistance configuration for the equalizer

Bit 7:6 - EQRes3[1:0] - Resistance to be used in the fourth stage of the data input equalizer

EQRes3[1:0] Resistance [kOhm]

2'd0 0

2'd1 0.4

2'd2 1.0

2'd3 1.6

Bit 5:4 - EQRes2[1:0] - Resistance to be used in the third stage of the data input equalizer

EQRes2[1:0] Resistance [kOhm]

2'd0 0

2'd1 0.6

2'd2 1.2

2'd3 2.4

Bit 3:2 - EQRes1[1:0] - Resistance to be used in the second stage of the data input equalizer

EQRes1[1:0] Resistance [kOhm]

2'd0 0

2'd1 3.0

2'd2 4.9

2'd3 7.1

Bit 1:0 - EQRes0[1:0] - Resistance to be used in the first stage of the data input equalizer

EQRes0[1:0] Resistance [kOhm]

2'd0 0

2'd1 3.0

2'd2 4.9

2'd3 7.1

15.1.6. Line Driver

[0x039] LDConfigH

Line driver configuration register

Bit 7 - LDEmphasisEnable - Enable pre-emphasis in the line driver. The amplitude of the pre-emphasis is controlled by LDEmphasisAmp[6:0] and the duration by LDEmphasisShort.

Bit 6:0 - LDModulationCurrent[6:0] - Sets high-speed line driver modulation current: Im = 137 uA \* LDModulationCurrent[6:0]

[0x03a] LDConfigL

Line driver configuration register

Bit 7 - LDEmphasisShort - Sets the duration of the pre-emphasis pulse. Please not that pre-emphasis has to be enabled (LDEmphasisEnable) for this field to have any impact.

Bit 6:0 - LDEmphasisAmp[6:0] - Sets high-speed line driver pre-emphasis current: Ipre = 137 uA \* LDEmphasisAmp[6:0]. Please note that pre-emphasis has to be enabled (LDEmphasisEnable) for these registers bits to be active.

-Note for the LDConfigH and LDConfigL registers: since the high-speed line driver contains an internal 100 Ohm "termination", the currents set by LDModulationCurrent[6:0] and LDEmphasisAmp[6:0] bits are shared between the internal and external load impedances. This needs to be taken into account when computing the output signal amplitude. To calculate the modulation amplitude the user should thus use the equivalent resistor value of 50 Ohm, that is, the internal 100 Ohm resistor in parallel with the external 100 Ohm termination impedance.

[0x03b] REFCLK

Configuration for the reference clock pad

Bit 4 - TESTCLKsetCM - Enable common mode generation for TSTCLKN/P input pads.

Bit 2 - REFCLKForceEnable - Enable the reference clock pad regardless of the operation mode.

Bit 1 - REFCLKAcBias - Enables the common mode generation for the REFCLK.

Bit 0 - REFCLKTerm - Enables the 100 Ohm termination for the REFCLK input.

[0x03c] SCCONFIG

Serial interface (IC/EC) configuration register.

Bit 0 - scParityCheckDisable - Disable parity check for incoming frames. If asserted, the data will be copied to registers regardless of parity check.

15.1.7. Reset

[0x03d] RESETConfig

Reset configuration.

Bit 7 - ResetOutDriveStrength - Reset out pin driving strength.

Bit 6:5 - ResetOutLength[1:0] -

ResetOutLength[1:0] Reset pulse duration [s]

0 disabled

1 100n

2 1u

3 10u

Bit 3 - BODEnable - Enables brownout detector.

Bit 2:0 - BODlevel[2:0] -

BODlevel[2:0] Brownout voltage level [V]

0 0.70

1 0.75

2 0.80

3 0.85

4 0.90

5 0.95

6 1.00

7 1.05

15.1.8. Power Good

[0x03e] PGConfig

Power Good configuration.

Bit 7 - PGEnable - Enable Power Good feature. For more details see Power-up state machine.

Bit 6:4 - PGLevel[2:0] - Enable Power Good feature. For more details see Power-up state machine.

PGLevel[2:0] Voltage level [V]

0 0.70

1 0.75

2 0.80

3 0.85

4 0.90

5 0.95

6 1.00

7 1.05

Bit 3:0 - PGDelay[4:0] -

PGDelay[3:0] Wait time

0 disabled

1 1 us

2 5 us

3 10 us

4 50 us

5 100 us

6 500 us

7 1 ms

8 5 ms

9 10 ms

10 20 ms

11 50 ms

12 100 ms

13 200 ms

14 500 ms

15 1 s

15.1.9. I2C Masters

[0x03f] I2CMTransConfig

Bit 7 - I2CMTransEnable -

Bit 6:5 - I2CMTransChannel[1:0] -

Bit 4:2 - I2CMTransAddressExt[2:0] -

[0x040] I2CMTransAddress

Bit 6:0 - I2CMTransAddress[6:0] -

[0x041] I2CMTransCtrl

Bit 7:0 - I2CMTransCtrl[7:0] -

[0x042] I2CMTransData0

Bit 7:0 - I2CMTransData[7:0] -

[0x043] I2CMTransData1

Bit 7:0 - I2CMTransData[15:8] -

[0x044] I2CMTransData2

Bit 7:0 - I2CMTransData[23:16] -

[0x045] I2CMTransData3

Bit 7:0 - I2CMTransData[31:24] -

[0x046] I2CMTransData4

Bit 7:0 - I2CMTransData[39:32] -

[0x047] I2CMTransData5

Bit 7:0 - I2CMTransData[47:40] -

[0x048] I2CMTransData6

Bit 7:0 - I2CMTransData[55:48] -

[0x049] I2CMTransData7

Bit 7:0 - I2CMTransData[63:56] -

[0x04a] I2CMTransData8

Bit 7:0 - I2CMTransData[71:64] -

[0x04b] I2CMTransData9

Bit 7:0 - I2CMTransData[79:72] -

[0x04c] I2CMTransData10

Bit 7:0 - I2CMTransData[87:80] -

[0x04d] I2CMTransData11

Bit 7:0 - I2CMTransData[95:88] -

[0x04e] I2CMTransData12

Bit 7:0 - I2CMTransData[103:96] -

[0x04f] I2CMTransData13

Bit 7:0 - I2CMTransData[111:104] -

[0x050] I2CMTransData14

Bit 7:0 - I2CMTransData[119:112] -

[0x051] I2CMTransData15

Bit 7:0 - I2CMTransData[127:120] -

15.1.10. Parallel IO

[0x052] PIODirH

Direction control for Parallel IO port

Bit 7:0 - PIODir[15:8] -

PIODir[n] Function

1'b0 Pin configured as an input

1'b1 Pin configured as an output

[0x053] PIODirL

Direction control for Parallel IO port

Bit 7:0 - PIODir[7:0] -

PIODir[n] Function

1'b0 Pin configured as an input

1'b1 Pin configured as an output

[0x054] PIOOutH

Output control for Parallel IO port

Bit 7:0 - PIOOut[15:8] -

[0x055] PIOOutL

Output control for Parallel IO port

Bit 7:0 - PIOOut[7:0] -

[0x056] PIOPullEnaH

Pull-up/pull-down control for Parallel IO port

Bit 7:0 - PIOPullEnable[15:8] -

[0x057] PIOPullEnaL

Pull-up/pull-down control for Parallel IO port

Bit 7:0 - PIOPullEnable[7:0] -

[0x058] PIOUpDownH

Selects pull up or pull down for Parallel IO port

Bit 7:0 - PIOUpDown[15:8] -

[0x059] PIOUpDownL

Selects pull up or pull down for Parallel IO port

Bit 7:0 - PIOUpDown[7:0] -

[0x05a] PIODriveStrengthH

Selects driving strength for Parallel IO port when configured as an output

Bit 7:0 - PIODriveStrength[15:8] -

[0x05b] PIODriveStrengthL

Selects driving strength for Parallel IO port when configured as an output

Bit 7:0 - PIODriveStrength[7:0] -

15.1.11. Phase Shifter

[0x05c] PS0Config

Main configuration of the phase-shifter clock 0

Bit 7 - PS0Delay[8] - MSB of the delay select for clock 0. For more information check [0x05d] PS0Delay register.

Bit 6 - PS0EnableFineTune - Enable fine deskewing for clock 0.

Bit 5:3 - PS0DriveStrength[2:0] - Sets the driving strength for 0 clock output.

PS0DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - PS0Freq[2:0] - Sets the frequency for 0 clock output.

PS0Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7

[0x05d] PS0Delay

Delay of the phase-shifter clock 0

Bit 7:0 - PS0Delay[7:0] - Delay select for clock 0. Please note that that most significant bit of the PS0Delay field is stored in the [0x05c] PS0Config register.

[0x05e] PS0OutDriver

Output driver configuration for the phase-shifter clock 0

Bit 7:5 - PS0PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for phase-shifter 0 clock output.

PS0PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - PS0PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 0.

PS0PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - PS0PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 0 clock output in self timed mode.

PS0PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x05f] PS1Config

Main configuration of the phase-shifter clock 1

Bit 7 - PS1Delay[8] - MSB of the delay select for clock 1. For more information check [0x060] PS1Delay register.

Bit 6 - PS1EnableFineTune - Enable fine deskewing for clock 1.

Bit 5:3 - PS1DriveStrength[2:0] - Sets the driving strength for 1 clock output.

PS1DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - PS1Freq[2:0] - Sets the frequency for 1 clock output.

PS1Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7

[0x060] PS1Delay

Delay of the phase-shifter clock 1

Bit 7:0 - PS1Delay[7:0] - Delay select for clock 1. Please note that that most significant bit of the PS1Delay field is stored in the [0x05f] PS1Config register.

[0x061] PS1OutDriver

Output driver configuration for the phase-shifter clock 1

Bit 7:5 - PS1PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for phase-shifter 1 clock output.

PS1PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - PS1PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 1.

PS1PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - PS1PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 1 clock output in self timed mode.

PS1PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x062] PS2Config

Main configuration of the phase-shifter clock 2

Bit 7 - PS2Delay[8] - MSB of the delay select for clock 2. For more information check [0x063] PS2Delay register.

Bit 6 - PS2EnableFineTune - Enable fine deskewing for clock 2.

Bit 5:3 - PS2DriveStrength[2:0] - Sets the driving strength for 2 clock output.

PS2DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - PS2Freq[2:0] - Sets the frequency for 2 clock output.

PS2Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7

[0x063] PS2Delay

Delay of the phase-shifter clock 2

Bit 7:0 - PS2Delay[7:0] - Delay select for clock 2. Please note that that most significant bit of the PS2Delay field is stored in the [0x062] PS2Config register.

[0x064] PS2OutDriver

Output driver configuration for the phase-shifter clock 2

Bit 7:5 - PS2PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for phase-shifter 2 clock output.

PS2PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - PS2PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 2.

PS2PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - PS2PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 2 clock output in self timed mode.

PS2PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x065] PS3Config

Main configuration of the phase-shifter clock 3

Bit 7 - PS3Delay[8] - MSB of the delay select for clock 3. For more information check [0x066] PS3Delay register.

Bit 6 - PS3EnableFineTune - Enable fine deskewing for clock 3.

Bit 5:3 - PS3DriveStrength[2:0] - Sets the driving strength for 3 clock output.

PS3DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - PS3Freq[2:0] - Sets the frequency for 3 clock output.

PS3Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7

[0x066] PS3Delay

Delay of the phase-shifter clock 3

Bit 7:0 - PS3Delay[7:0] - Delay select for clock 3. Please note that that most significant bit of the PS3Delay field is stored in the [0x065] PS3Config register.

[0x067] PS3OutDriver

Output driver configuration for the phase-shifter clock 3

Bit 7:5 - PS3PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for phase-shifter 3 clock output.

PS3PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - PS3PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 3.

PS3PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - PS3PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 3 clock output in self timed mode.

PS3PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

15.1.12. Voltage DAC

[0x068] DACConfigH

DACs configuration register.

Bit 7 - VOLDACEnable - Enable voltage DAC.

Bit 6 - CURDACEnable - Enables current DAC.

Bit 3:0 - VOLDACValue[11:8] - Sets output voltage for the Voltage DAC.

See also: [0x069] DACConfigL, [0x06a] CURDACValue

[0x069] DACConfigL

DACs configuration register.

Bit 7:0 - VOLDACValue[7:0] - Sets output voltage for the Voltage DAC.

See also: [0x068] DACConfigH

15.1.13. CURDAC

[0x06a] CURDACValue

Output current

Bit 7:0 - CURDACSelect[7:0] - Sets output current for the current DAC. Current = CURDACSelect \* XX uA.

See also: [0x06b] CURDACCHN, [0x068] DACConfigH

[0x06b] CURDACCHN

Current DAC output multiplexer.

Bit 7:0 - CURDACChnEnable[7:0] - Setting Nth bit in this register attaches current DAC to ADCN pin. Current source can be attached to any number of channels.

See also: [0x06a] CURDACValue, [0x068] DACConfigH

15.1.14. ePortClk

[0x06c] EPCLK0ChnCntrH

Configuration of clock output 0

Bit 6 - EPCLK0Invert - Inverts 0 clock output.

Bit 5:3 - EPCLK0DriveStrength[2:0] - Sets the driving strength for 0 clock output.

EPCLK0DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK0Freq[2:0] - Sets the frequency for 0 clock output.

EPCLK0Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[0]

[0x06d] EPCLK0ChnCntrL

Configuration of clock output 0

Bit 7:5 - EPCLK0PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 0 clock output.

EPCLK0PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK0PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 0.

EPCLK0PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK0PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 0 clock output in self timed mode.

EPCLK0PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x06e] EPCLK1ChnCntrH

Configuration of clock output 1

Bit 6 - EPCLK1Invert - Inverts 1 clock output.

Bit 5:3 - EPCLK1DriveStrength[2:0] - Sets the driving strength for 1 clock output.

EPCLK1DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK1Freq[2:0] - Sets the frequency for 1 clock output.

EPCLK1Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[1]

[0x06f] EPCLK1ChnCntrL

Configuration of clock output 1

Bit 7:5 - EPCLK1PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 1 clock output.

EPCLK1PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK1PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 1.

EPCLK1PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK1PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 1 clock output in self timed mode.

EPCLK1PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x070] EPCLK2ChnCntrH

Configuration of clock output 2

Bit 6 - EPCLK2Invert - Inverts 2 clock output.

Bit 5:3 - EPCLK2DriveStrength[2:0] - Sets the driving strength for 2 clock output.

EPCLK2DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK2Freq[2:0] - Sets the frequency for 2 clock output.

EPCLK2Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[2]

[0x071] EPCLK2ChnCntrL

Configuration of clock output 2

Bit 7:5 - EPCLK2PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 2 clock output.

EPCLK2PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK2PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 2.

EPCLK2PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK2PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 2 clock output in self timed mode.

EPCLK2PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x072] EPCLK3ChnCntrH

Configuration of clock output 3

Bit 6 - EPCLK3Invert - Inverts 3 clock output.

Bit 5:3 - EPCLK3DriveStrength[2:0] - Sets the driving strength for 3 clock output.

EPCLK3DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK3Freq[2:0] - Sets the frequency for 3 clock output.

EPCLK3Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[3]

[0x073] EPCLK3ChnCntrL

Configuration of clock output 3

Bit 7:5 - EPCLK3PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 3 clock output.

EPCLK3PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK3PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 3.

EPCLK3PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK3PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 3 clock output in self timed mode.

EPCLK3PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x074] EPCLK4ChnCntrH

Configuration of clock output 4

Bit 6 - EPCLK4Invert - Inverts 4 clock output.

Bit 5:3 - EPCLK4DriveStrength[2:0] - Sets the driving strength for 4 clock output.

EPCLK4DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK4Freq[2:0] - Sets the frequency for 4 clock output.

EPCLK4Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[4]

[0x075] EPCLK4ChnCntrL

Configuration of clock output 4

Bit 7:5 - EPCLK4PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 4 clock output.

EPCLK4PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK4PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 4.

EPCLK4PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK4PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 4 clock output in self timed mode.

EPCLK4PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x076] EPCLK5ChnCntrH

Configuration of clock output 5

Bit 6 - EPCLK5Invert - Inverts 5 clock output.

Bit 5:3 - EPCLK5DriveStrength[2:0] - Sets the driving strength for 5 clock output.

EPCLK5DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK5Freq[2:0] - Sets the frequency for 5 clock output.

EPCLK5Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[5]

[0x077] EPCLK5ChnCntrL

Configuration of clock output 5

Bit 7:5 - EPCLK5PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 5 clock output.

EPCLK5PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK5PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 5.

EPCLK5PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK5PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 5 clock output in self timed mode.

EPCLK5PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x078] EPCLK6ChnCntrH

Configuration of clock output 6

Bit 6 - EPCLK6Invert - Inverts 6 clock output.

Bit 5:3 - EPCLK6DriveStrength[2:0] - Sets the driving strength for 6 clock output.

EPCLK6DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK6Freq[2:0] - Sets the frequency for 6 clock output.

EPCLK6Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[6]

[0x079] EPCLK6ChnCntrL

Configuration of clock output 6

Bit 7:5 - EPCLK6PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 6 clock output.

EPCLK6PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK6PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 6.

EPCLK6PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK6PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 6 clock output in self timed mode.

EPCLK6PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x07a] EPCLK7ChnCntrH

Configuration of clock output 7

Bit 6 - EPCLK7Invert - Inverts 7 clock output.

Bit 5:3 - EPCLK7DriveStrength[2:0] - Sets the driving strength for 7 clock output.

EPCLK7DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK7Freq[2:0] - Sets the frequency for 7 clock output.

EPCLK7Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[7]

[0x07b] EPCLK7ChnCntrL

Configuration of clock output 7

Bit 7:5 - EPCLK7PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 7 clock output.

EPCLK7PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK7PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 7.

EPCLK7PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK7PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 7 clock output in self timed mode.

EPCLK7PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x07c] EPCLK8ChnCntrH

Configuration of clock output 8

Bit 6 - EPCLK8Invert - Inverts 8 clock output.

Bit 5:3 - EPCLK8DriveStrength[2:0] - Sets the driving strength for 8 clock output.

EPCLK8DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK8Freq[2:0] - Sets the frequency for 8 clock output.

EPCLK8Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[8]

[0x07d] EPCLK8ChnCntrL

Configuration of clock output 8

Bit 7:5 - EPCLK8PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 8 clock output.

EPCLK8PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK8PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 8.

EPCLK8PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK8PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 8 clock output in self timed mode.

EPCLK8PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x07e] EPCLK9ChnCntrH

Configuration of clock output 9

Bit 6 - EPCLK9Invert - Inverts 9 clock output.

Bit 5:3 - EPCLK9DriveStrength[2:0] - Sets the driving strength for 9 clock output.

EPCLK9DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK9Freq[2:0] - Sets the frequency for 9 clock output.

EPCLK9Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[9]

[0x07f] EPCLK9ChnCntrL

Configuration of clock output 9

Bit 7:5 - EPCLK9PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 9 clock output.

EPCLK9PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK9PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 9.

EPCLK9PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK9PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 9 clock output in self timed mode.

EPCLK9PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x080] EPCLK10ChnCntrH

Configuration of clock output 10

Bit 6 - EPCLK10Invert - Inverts 10 clock output.

Bit 5:3 - EPCLK10DriveStrength[2:0] - Sets the driving strength for 10 clock output.

EPCLK10DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK10Freq[2:0] - Sets the frequency for 10 clock output.

EPCLK10Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[10]

[0x081] EPCLK10ChnCntrL

Configuration of clock output 10

Bit 7:5 - EPCLK10PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 10 clock output.

EPCLK10PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK10PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 10.

EPCLK10PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK10PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 10 clock output in self timed mode.

EPCLK10PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x082] EPCLK11ChnCntrH

Configuration of clock output 11

Bit 6 - EPCLK11Invert - Inverts 11 clock output.

Bit 5:3 - EPCLK11DriveStrength[2:0] - Sets the driving strength for 11 clock output.

EPCLK11DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK11Freq[2:0] - Sets the frequency for 11 clock output.

EPCLK11Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[11]

[0x083] EPCLK11ChnCntrL

Configuration of clock output 11

Bit 7:5 - EPCLK11PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 11 clock output.

EPCLK11PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK11PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 11.

EPCLK11PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK11PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 11 clock output in self timed mode.

EPCLK11PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x084] EPCLK12ChnCntrH

Configuration of clock output 12

Bit 6 - EPCLK12Invert - Inverts 12 clock output.

Bit 5:3 - EPCLK12DriveStrength[2:0] - Sets the driving strength for 12 clock output.

EPCLK12DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK12Freq[2:0] - Sets the frequency for 12 clock output.

EPCLK12Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[12]

[0x085] EPCLK12ChnCntrL

Configuration of clock output 12

Bit 7:5 - EPCLK12PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 12 clock output.

EPCLK12PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK12PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 12.

EPCLK12PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK12PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 12 clock output in self timed mode.

EPCLK12PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x086] EPCLK13ChnCntrH

Configuration of clock output 13

Bit 6 - EPCLK13Invert - Inverts 13 clock output.

Bit 5:3 - EPCLK13DriveStrength[2:0] - Sets the driving strength for 13 clock output.

EPCLK13DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK13Freq[2:0] - Sets the frequency for 13 clock output.

EPCLK13Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[13]

[0x087] EPCLK13ChnCntrL

Configuration of clock output 13

Bit 7:5 - EPCLK13PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 13 clock output.

EPCLK13PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK13PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 13.

EPCLK13PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK13PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 13 clock output in self timed mode.

EPCLK13PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x088] EPCLK14ChnCntrH

Configuration of clock output 14

Bit 6 - EPCLK14Invert - Inverts 14 clock output.

Bit 5:3 - EPCLK14DriveStrength[2:0] - Sets the driving strength for 14 clock output.

EPCLK14DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK14Freq[2:0] - Sets the frequency for 14 clock output.

EPCLK14Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[14]

[0x089] EPCLK14ChnCntrL

Configuration of clock output 14

Bit 7:5 - EPCLK14PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 14 clock output.

EPCLK14PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK14PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 14.

EPCLK14PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK14PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 14 clock output in self timed mode.

EPCLK14PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x08a] EPCLK15ChnCntrH

Configuration of clock output 15

Bit 6 - EPCLK15Invert - Inverts 15 clock output.

Bit 5:3 - EPCLK15DriveStrength[2:0] - Sets the driving strength for 15 clock output.

EPCLK15DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK15Freq[2:0] - Sets the frequency for 15 clock output.

EPCLK15Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[15]

[0x08b] EPCLK15ChnCntrL

Configuration of clock output 15

Bit 7:5 - EPCLK15PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 15 clock output.

EPCLK15PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK15PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 15.

EPCLK15PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK15PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 15 clock output in self timed mode.

EPCLK15PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x08c] EPCLK16ChnCntrH

Configuration of clock output 16

Bit 6 - EPCLK16Invert - Inverts 16 clock output.

Bit 5:3 - EPCLK16DriveStrength[2:0] - Sets the driving strength for 16 clock output.

EPCLK16DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK16Freq[2:0] - Sets the frequency for 16 clock output.

EPCLK16Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[16]

[0x08d] EPCLK16ChnCntrL

Configuration of clock output 16

Bit 7:5 - EPCLK16PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 16 clock output.

EPCLK16PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK16PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 16.

EPCLK16PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK16PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 16 clock output in self timed mode.

EPCLK16PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x08e] EPCLK17ChnCntrH

Configuration of clock output 17

Bit 6 - EPCLK17Invert - Inverts 17 clock output.

Bit 5:3 - EPCLK17DriveStrength[2:0] - Sets the driving strength for 17 clock output.

EPCLK17DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK17Freq[2:0] - Sets the frequency for 17 clock output.

EPCLK17Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[17]

[0x08f] EPCLK17ChnCntrL

Configuration of clock output 17

Bit 7:5 - EPCLK17PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 17 clock output.

EPCLK17PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK17PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 17.

EPCLK17PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK17PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 17 clock output in self timed mode.

EPCLK17PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x090] EPCLK18ChnCntrH

Configuration of clock output 18

Bit 6 - EPCLK18Invert - Inverts 18 clock output.

Bit 5:3 - EPCLK18DriveStrength[2:0] - Sets the driving strength for 18 clock output.

EPCLK18DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK18Freq[2:0] - Sets the frequency for 18 clock output.

EPCLK18Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[18]

[0x091] EPCLK18ChnCntrL

Configuration of clock output 18

Bit 7:5 - EPCLK18PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 18 clock output.

EPCLK18PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK18PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 18.

EPCLK18PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK18PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 18 clock output in self timed mode.

EPCLK18PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x092] EPCLK19ChnCntrH

Configuration of clock output 19

Bit 6 - EPCLK19Invert - Inverts 19 clock output.

Bit 5:3 - EPCLK19DriveStrength[2:0] - Sets the driving strength for 19 clock output.

EPCLK19DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK19Freq[2:0] - Sets the frequency for 19 clock output.

EPCLK19Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[19]

[0x093] EPCLK19ChnCntrL

Configuration of clock output 19

Bit 7:5 - EPCLK19PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 19 clock output.

EPCLK19PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK19PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 19.

EPCLK19PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK19PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 19 clock output in self timed mode.

EPCLK19PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x094] EPCLK20ChnCntrH

Configuration of clock output 20

Bit 6 - EPCLK20Invert - Inverts 20 clock output.

Bit 5:3 - EPCLK20DriveStrength[2:0] - Sets the driving strength for 20 clock output.

EPCLK20DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK20Freq[2:0] - Sets the frequency for 20 clock output.

EPCLK20Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[20]

[0x095] EPCLK20ChnCntrL

Configuration of clock output 20

Bit 7:5 - EPCLK20PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 20 clock output.

EPCLK20PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK20PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 20.

EPCLK20PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK20PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 20 clock output in self timed mode.

EPCLK20PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x096] EPCLK21ChnCntrH

Configuration of clock output 21

Bit 6 - EPCLK21Invert - Inverts 21 clock output.

Bit 5:3 - EPCLK21DriveStrength[2:0] - Sets the driving strength for 21 clock output.

EPCLK21DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK21Freq[2:0] - Sets the frequency for 21 clock output.

EPCLK21Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[21]

[0x097] EPCLK21ChnCntrL

Configuration of clock output 21

Bit 7:5 - EPCLK21PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 21 clock output.

EPCLK21PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK21PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 21.

EPCLK21PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK21PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 21 clock output in self timed mode.

EPCLK21PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x098] EPCLK22ChnCntrH

Configuration of clock output 22

Bit 6 - EPCLK22Invert - Inverts 22 clock output.

Bit 5:3 - EPCLK22DriveStrength[2:0] - Sets the driving strength for 22 clock output.

EPCLK22DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK22Freq[2:0] - Sets the frequency for 22 clock output.

EPCLK22Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[22]

[0x099] EPCLK22ChnCntrL

Configuration of clock output 22

Bit 7:5 - EPCLK22PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 22 clock output.

EPCLK22PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK22PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 22.

EPCLK22PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK22PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 22 clock output in self timed mode.

EPCLK22PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x09a] EPCLK23ChnCntrH

Configuration of clock output 23

Bit 6 - EPCLK23Invert - Inverts 23 clock output.

Bit 5:3 - EPCLK23DriveStrength[2:0] - Sets the driving strength for 23 clock output.

EPCLK23DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK23Freq[2:0] - Sets the frequency for 23 clock output.

EPCLK23Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[23]

[0x09b] EPCLK23ChnCntrL

Configuration of clock output 23

Bit 7:5 - EPCLK23PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 23 clock output.

EPCLK23PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK23PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 23.

EPCLK23PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK23PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 23 clock output in self timed mode.

EPCLK23PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x09c] EPCLK24ChnCntrH

Configuration of clock output 24

Bit 6 - EPCLK24Invert - Inverts 24 clock output.

Bit 5:3 - EPCLK24DriveStrength[2:0] - Sets the driving strength for 24 clock output.

EPCLK24DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK24Freq[2:0] - Sets the frequency for 24 clock output.

EPCLK24Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[24]

[0x09d] EPCLK24ChnCntrL

Configuration of clock output 24

Bit 7:5 - EPCLK24PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 24 clock output.

EPCLK24PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK24PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 24.

EPCLK24PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK24PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 24 clock output in self timed mode.

EPCLK24PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x09e] EPCLK25ChnCntrH

Configuration of clock output 25

Bit 6 - EPCLK25Invert - Inverts 25 clock output.

Bit 5:3 - EPCLK25DriveStrength[2:0] - Sets the driving strength for 25 clock output.

EPCLK25DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK25Freq[2:0] - Sets the frequency for 25 clock output.

EPCLK25Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[25]

[0x09f] EPCLK25ChnCntrL

Configuration of clock output 25

Bit 7:5 - EPCLK25PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 25 clock output.

EPCLK25PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK25PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 25.

EPCLK25PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK25PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 25 clock output in self timed mode.

EPCLK25PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0a0] EPCLK26ChnCntrH

Configuration of clock output 26

Bit 6 - EPCLK26Invert - Inverts 26 clock output.

Bit 5:3 - EPCLK26DriveStrength[2:0] - Sets the driving strength for 26 clock output.

EPCLK26DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK26Freq[2:0] - Sets the frequency for 26 clock output.

EPCLK26Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[26]

[0x0a1] EPCLK26ChnCntrL

Configuration of clock output 26

Bit 7:5 - EPCLK26PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 26 clock output.

EPCLK26PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK26PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 26.

EPCLK26PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK26PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 26 clock output in self timed mode.

EPCLK26PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0a2] EPCLK27ChnCntrH

Configuration of clock output 27

Bit 6 - EPCLK27Invert - Inverts 27 clock output.

Bit 5:3 - EPCLK27DriveStrength[2:0] - Sets the driving strength for 27 clock output.

EPCLK27DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK27Freq[2:0] - Sets the frequency for 27 clock output.

EPCLK27Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[27]

[0x0a3] EPCLK27ChnCntrL

Configuration of clock output 27

Bit 7:5 - EPCLK27PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 27 clock output.

EPCLK27PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK27PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 27.

EPCLK27PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK27PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 27 clock output in self timed mode.

EPCLK27PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0a4] EPCLK28ChnCntrH

Configuration of clock output 28

Bit 6 - EPCLK28Invert - Inverts 28 clock output.

Bit 5:3 - EPCLK28DriveStrength[2:0] - Sets the driving strength for 28 clock output.

EPCLK28DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 2:0 - EPCLK28Freq[2:0] - Sets the frequency for 28 clock output.

EPCLK28Freq[2:0] Frequency [MHz]

3'd0 disabled

3'd1 40

3'd2 80

3'd3 160

3'd4 320

3'd5 640

3'd6 1280

3'd7 ePortRxDataIn[28]

[0x0a5] EPCLK28ChnCntrL

Configuration of clock output 28

Bit 7:5 - EPCLK28PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for 28 clock output.

EPCLK28PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPCLK28PreEmphasisMode[1:0] - Sets the pre-emphasis mode for clock output 28.

EPCLK28PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPCLK28PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for 28 clock output in self timed mode.

EPCLK28PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0a6] Reserved1

Reserved

15.1.15. ePortTx

[0x0a7] EPTXDataRate

Data rate control for ePortTx

Bit 7:6 - EPTX3DataRate[1:0] - Data rate for ePortTx group 3

EPTX3DataRate[1:0] Group 3 data rate

2'd0 disabled

2'd1 80M bps

2'd2 160 Mbps

2'd3 320 Mbps

Bit 5:4 - EPTX2DataRate[1:0] - Data rate for ePortTx group 2

EPTX2DataRate[1:0] Group 2 data rate

2'd0 disabled

2'd1 80M bps

2'd2 160 Mbps

2'd3 320 Mbps

Bit 3:2 - EPTX1DataRate[1:0] - Data rate for ePortTx group 1

EPTX1DataRate[1:0] Group 1 data rate

2'd0 disabled

2'd1 80M bps

2'd2 160 Mbps

2'd3 320 Mbps

Bit 1:0 - EPTX0DataRate[1:0] - Data rate for ePortTx group 0

EPTX0DataRate[1:0] Group 0 data rate

2'd0 disabled

2'd1 80M bps

2'd2 160 Mbps

2'd3 320 Mbps

[0x0a8] EPTXControl

EportTx configuration register.

Bit 7:6 - EPTXEcPreEmphasisWidth[2:1] - Sets the width of pre-emphasis pulse for EC channel output

EPTXECPreEmpahasisWidth[2:1] Pulse length [ps]

2'd0 120

2'd1 360

2'd2 600

2'd3 840

Bit 5 - EPTXEcInvert - Invert data for EC channel output

Bit 4 - EPTXEcEnable - Enable EC channel output

Bit 3 - EPTX3MirrorEnable - Enables mirror feature for group 3

Bit 2 - EPTX2MirrorEnable - Enables mirror feature for group 2

Bit 1 - EPTX1MirrorEnable - Enables mirror feature for group 1

Bit 0 - EPTX0MirrorEnable - Enables mirror feature for group 0

[0x0a9] EPTX10Enable

Channel enable control for EPTX0 and EPTX1.

Bit 7 - EPTX13Enable - Enable channel 3 in group 1

Bit 6 - EPTX12Enable - Enable channel 2 in group 1

Bit 5 - EPTX11Enable - Enable channel 1 in group 1

Bit 4 - EPTX10Enable - Enable channel 0 in group 1

Bit 3 - EPTX03Enable - Enable channel 3 in group 0

Bit 2 - EPTX02Enable - Enable channel 2 in group 0

Bit 1 - EPTX01Enable - Enable channel 1 in group 0

Bit 0 - EPTX00Enable - Enable channel 0 in group 0

[0x0aa] EPTX32Enable

Channel enable control for EPTX2 and EPTX3.

Bit 7 - EPTX33Enable - Enable channel 3 in group 3

Bit 6 - EPTX32Enable - Enable channel 2 in group 3

Bit 5 - EPTX31Enable - Enable channel 1 in group 3

Bit 4 - EPTX30Enable - Enable channel 0 in group 3

Bit 3 - EPTX23Enable - Enable channel 3 in group 2

Bit 2 - EPTX22Enable - Enable channel 2 in group 2

Bit 1 - EPTX21Enable - Enable channel 1 in group 2

Bit 0 - EPTX20Enable - Enable channel 0 in group 2

[0x0ab] EPTXEcChnCntr

EC channel driver configuration.

Bit 7:5 - EPTXEcPreEmphasisStrength[2:0] - Sets the pre-emphasis strength for the EC channel.

EPTXEcPreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTXEcPreEmphasisMode[1:0] - Sets the pre-emphasis mode for the EC channel.

EPTXEcPreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTXEcDriveStrength[2:0] - Sets the pre-emphasis strength for the EC channel.

EPTXEcDriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0ac] EPTX00ChnCntr

Control register for output driver of channel 0 in group 0

Bit 7:5 - EPTX00PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 0 in group 0.

EPTX00PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX00PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 0 in group 0.

EPTX00PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX00DriveStrength[2:0] - Sets the driving strength for channel 0 in group 0.

EPTX00DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0ad] EPTX01ChnCntr

Control register for output driver of channel 1 in group 0

Bit 7:5 - EPTX01PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 0 in group 1.

EPTX01PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX01PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 0 in group 1.

EPTX01PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX01DriveStrength[2:0] - Sets the driving strength for channel 0 in group 1.

EPTX01DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0ae] EPTX02ChnCntr

Control register for output driver of channel 2 in group 0

Bit 7:5 - EPTX02PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 0 in group 2.

EPTX02PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX02PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 0 in group 2.

EPTX02PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX02DriveStrength[2:0] - Sets the driving strength for channel 0 in group 2.

EPTX02DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0af] EPTX03ChnCntr

Control register for output driver of channel 3 in group 0

Bit 7:5 - EPTX03PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 0 in group 3.

EPTX03PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX03PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 0 in group 3.

EPTX03PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX03DriveStrength[2:0] - Sets the driving strength for channel 0 in group 3.

EPTX03DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b0] EPTX10ChnCntr

Control register for output driver of channel 0 in group 1

Bit 7:5 - EPTX10PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 1 in group 0.

EPTX10PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX10PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 1 in group 0.

EPTX10PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX10DriveStrength[2:0] - Sets the driving strength for channel 1 in group 0.

EPTX10DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b1] EPTX11ChnCntr

Control register for output driver of channel 1 in group 1

Bit 7:5 - EPTX11PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 1 in group 1.

EPTX11PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX11PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 1 in group 1.

EPTX11PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX11DriveStrength[2:0] - Sets the driving strength for channel 1 in group 1.

EPTX11DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b2] EPTX12ChnCntr

Control register for output driver of channel 2 in group 1

Bit 7:5 - EPTX12PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 1 in group 2.

EPTX12PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX12PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 1 in group 2.

EPTX12PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX12DriveStrength[2:0] - Sets the driving strength for channel 1 in group 2.

EPTX12DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b3] EPTX13ChnCntr

Control register for output driver of channel 3 in group 1

Bit 7:5 - EPTX13PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 1 in group 3.

EPTX13PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX13PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 1 in group 3.

EPTX13PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX13DriveStrength[2:0] - Sets the driving strength for channel 1 in group 3.

EPTX13DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b4] EPTX20ChnCntr

Control register for output driver of channel 0 in group 2

Bit 7:5 - EPTX20PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 2 in group 0.

EPTX20PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX20PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 2 in group 0.

EPTX20PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX20DriveStrength[2:0] - Sets the driving strength for channel 2 in group 0.

EPTX20DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b5] EPTX21ChnCntr

Control register for output driver of channel 1 in group 2

Bit 7:5 - EPTX21PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 2 in group 1.

EPTX21PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX21PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 2 in group 1.

EPTX21PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX21DriveStrength[2:0] - Sets the driving strength for channel 2 in group 1.

EPTX21DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b6] EPTX22ChnCntr

Control register for output driver of channel 2 in group 2

Bit 7:5 - EPTX22PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 2 in group 2.

EPTX22PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX22PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 2 in group 2.

EPTX22PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX22DriveStrength[2:0] - Sets the driving strength for channel 2 in group 2.

EPTX22DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b7] EPTX23ChnCntr

Control register for output driver of channel 3 in group 2

Bit 7:5 - EPTX23PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 2 in group 3.

EPTX23PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX23PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 2 in group 3.

EPTX23PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX23DriveStrength[2:0] - Sets the driving strength for channel 2 in group 3.

EPTX23DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b8] EPTX30ChnCntr

Control register for output driver of channel 0 in group 3

Bit 7:5 - EPTX30PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 3 in group 0.

EPTX30PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX30PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 3 in group 0.

EPTX30PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX30DriveStrength[2:0] - Sets the driving strength for channel 3 in group 0.

EPTX30DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0b9] EPTX31ChnCntr

Control register for output driver of channel 1 in group 3

Bit 7:5 - EPTX31PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 3 in group 1.

EPTX31PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX31PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 3 in group 1.

EPTX31PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX31DriveStrength[2:0] - Sets the driving strength for channel 3 in group 1.

EPTX31DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0ba] EPTX32ChnCntr

Control register for output driver of channel 2 in group 3

Bit 7:5 - EPTX32PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 3 in group 2.

EPTX32PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX32PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 3 in group 2.

EPTX32PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX32DriveStrength[2:0] - Sets the driving strength for channel 3 in group 2.

EPTX32DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0bb] EPTX33ChnCntr

Control register for output driver of channel 3 in group 3

Bit 7:5 - EPTX33PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for channel 3 in group 3.

EPTX33PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - EPTX33PreEmphasisMode[1:0] - Selects the pre-emphasis mode for channel 3 in group 3.

EPTX33PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - EPTX33DriveStrength[2:0] - Sets the driving strength for channel 3 in group 3.

EPTX33DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x0bc] EPTX01\_00ChnCntr

Output driver settings for ePortTx group 0

Bit 7 - EPTX01Invert - Invert data for channel 1 in ePortTx Group 0

Bit 6:4 - EPTX01PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 1 in ePortTx Group 0.

EPTX01PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX00Invert - Invert data for channel 0 in ePortTx Group 0

Bit 2:0 - EPTX00PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 0 in ePortTx Group 0.

EPTX00PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0bd] EPTX03\_02ChnCntr

Output driver settings for ePortTx group 0

Bit 7 - EPTX03Invert - Invert data for channel 3 in ePortTx Group 0

Bit 6:4 - EPTX03PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 3 in ePortTx Group 0.

EPTX03PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX02Invert - Invert data for channel 2 in ePortTx Group 0

Bit 2:0 - EPTX02PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 2 in ePortTx Group 0.

EPTX02PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0be] EPTX11\_10ChnCntr

Output driver settings for ePortTx group 1

Bit 7 - EPTX11Invert - Invert data for channel 1 in ePortTx Group 1

Bit 6:4 - EPTX11PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 1 in ePortTx Group 1.

EPTX11PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX10Invert - Invert data for channel 0 in ePortTx Group 1

Bit 2:0 - EPTX10PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 0 in ePortTx Group 1.

EPTX10PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0bf] EPTX13\_12ChnCntr

Output driver settings for ePortTx group 1

Bit 7 - EPTX13Invert - Invert data for channel 3 in ePortTx Group 1

Bit 6:4 - EPTX13PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 3 in ePortTx Group 1.

EPTX13PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX12Invert - Invert data for channel 2 in ePortTx Group 1

Bit 2:0 - EPTX12PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 2 in ePortTx Group 1.

EPTX12PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0c0] EPTX21\_20ChnCntr

Output driver settings for ePortTx group 2

Bit 7 - EPTX21Invert - Invert data for channel 1 in ePortTx Group 2

Bit 6:4 - EPTX21PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 1 in ePortTx Group 2.

EPTX21PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX20Invert - Invert data for channel 0 in ePortTx Group 2

Bit 2:0 - EPTX20PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 0 in ePortTx Group 2.

EPTX20PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0c1] EPTX23\_22ChnCntr

Output driver settings for ePortTx group 2

Bit 7 - EPTX23Invert - Invert data for channel 3 in ePortTx Group 2

Bit 6:4 - EPTX23PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 3 in ePortTx Group 2.

EPTX23PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX22Invert - Invert data for channel 2 in ePortTx Group 2

Bit 2:0 - EPTX22PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 2 in ePortTx Group 2.

EPTX22PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0c2] EPTX31\_30ChnCntr

Output driver settings for ePortTx group 3

Bit 7 - EPTX31Invert - Invert data for channel 1 in ePortTx Group 3

Bit 6:4 - EPTX31PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 1 in ePortTx Group 3.

EPTX31PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX30Invert - Invert data for channel 0 in ePortTx Group 3

Bit 2:0 - EPTX30PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 0 in ePortTx Group 3.

EPTX30PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

[0x0c3] EPTX33\_32ChnCntr

Output driver settings for ePortTx group 3

Bit 7 - EPTX33Invert - Invert data for channel 3 in ePortTx Group 3

Bit 6:4 - EPTX33PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 3 in ePortTx Group 3.

EPTX33PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - EPTX32Invert - Invert data for channel 2 in ePortTx Group 3

Bit 2:0 - EPTX32PreEmphasisWidth[2:0] - Sets the width of pre-emphasis pulse for channel 2 in ePortTx Group 3.

EPTX32PreEmpahasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

15.1.16. ePortRx

[0x0c4] EPRX0Control

Configuration of ePortRx Group 0

Bit 7 - EPRX03Enable - Enables channel 3 in group 0.

Bit 6 - EPRX02Enable - Enables channel 2 in group 0.

Bit 5 - EPRX01Enable - Enables channel 1 in group 0.

Bit 4 - EPRX00Enable - Enables channel 0 in group 0.

Bit 3:2 - EPRX0DataRate[1:0] - Sets the data rate for group 0.

EPRX0DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX0TrackMode[1:0] - Sets the phase tracking mode for group 0.

EPRX0TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0c5] EPRX1Control

Configuration of ePortRx Group 1

Bit 7 - EPRX13Enable - Enables channel 3 in group 1.

Bit 6 - EPRX12Enable - Enables channel 2 in group 1.

Bit 5 - EPRX11Enable - Enables channel 1 in group 1.

Bit 4 - EPRX10Enable - Enables channel 0 in group 1.

Bit 3:2 - EPRX1DataRate[1:0] - Sets the data rate for group 1.

EPRX1DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX1TrackMode[1:0] - Sets the phase tracking mode for group 1.

EPRX1TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0c6] EPRX2Control

Configuration of ePortRx Group 2

Bit 7 - EPRX23Enable - Enables channel 3 in group 2.

Bit 6 - EPRX22Enable - Enables channel 2 in group 2.

Bit 5 - EPRX21Enable - Enables channel 1 in group 2.

Bit 4 - EPRX20Enable - Enables channel 0 in group 2.

Bit 3:2 - EPRX2DataRate[1:0] - Sets the data rate for group 2.

EPRX2DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX2TrackMode[1:0] - Sets the phase tracking mode for group 2.

EPRX2TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0c7] EPRX3Control

Configuration of ePortRx Group 3

Bit 7 - EPRX33Enable - Enables channel 3 in group 3.

Bit 6 - EPRX32Enable - Enables channel 2 in group 3.

Bit 5 - EPRX31Enable - Enables channel 1 in group 3.

Bit 4 - EPRX30Enable - Enables channel 0 in group 3.

Bit 3:2 - EPRX3DataRate[1:0] - Sets the data rate for group 3.

EPRX3DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX3TrackMode[1:0] - Sets the phase tracking mode for group 3.

EPRX3TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0c8] EPRX4Control

Configuration of ePortRx Group 4

Bit 7 - EPRX43Enable - Enables channel 3 in group 4.

Bit 6 - EPRX42Enable - Enables channel 2 in group 4.

Bit 5 - EPRX41Enable - Enables channel 1 in group 4.

Bit 4 - EPRX40Enable - Enables channel 0 in group 4.

Bit 3:2 - EPRX4DataRate[1:0] - Sets the data rate for group 4.

EPRX4DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX4TrackMode[1:0] - Sets the phase tracking mode for group 4.

EPRX4TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0c9] EPRX5Control

Configuration of ePortRx Group 5

Bit 7 - EPRX53Enable - Enables channel 3 in group 5.

Bit 6 - EPRX52Enable - Enables channel 2 in group 5.

Bit 5 - EPRX51Enable - Enables channel 1 in group 5.

Bit 4 - EPRX50Enable - Enables channel 0 in group 5.

Bit 3:2 - EPRX5DataRate[1:0] - Sets the data rate for group 5.

EPRX5DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX5TrackMode[1:0] - Sets the phase tracking mode for group 5.

EPRX5TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0ca] EPRX6Control

Configuration of ePortRx Group 6

Bit 7 - EPRX63Enable - Enables channel 3 in group 6.

Bit 6 - EPRX62Enable - Enables channel 2 in group 6.

Bit 5 - EPRX61Enable - Enables channel 1 in group 6.

Bit 4 - EPRX60Enable - Enables channel 0 in group 6.

Bit 3:2 - EPRX6DataRate[1:0] - Sets the data rate for group 6.

EPRX6DataRate[1:0] 5 Gbps 10 Gbps

2'd0 disabled disabled

2'd1 160M bps 320 Mbps

2'd2 320 Mbps 640 Mbps

2'd3 640 Mbps 1280 Mbps

Bit 1:0 - EPRX6TrackMode[1:0] - Sets the phase tracking mode for group 6.

EPRX6TrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0cb] EPRXEcControl

Configuration of ePortRx EC channel

Bit 1:0 - EPRXEcTrackMode[1:0] - Sets the phase tracking mode for EC channel

EPRXEcTrackMode[1:0] Mode

2'd0 Fixed phase

2'd1 Initial training

2'd2 Continuous phase tracking

2'd3 Continuous phase tracking with initial phase

[0x0cc] EPRX00ChnCntr

Configuration of the channel 0 in group 0

Bit 7:4 - EPRX00PhaseSelect[3:0] - Selects the phase for channel 0 in group 0.

Bit 3 - EPRX00Invert - Inverts the channel 0 in group 0.

Bit 2 - EPRX00AcBias - Enables the common mode generation for channel 0 in group 0.

Bit 1 - EPRX00Term - Enables the 100 Ohm termination for channel 0 in group 0.

Bit 0 - EPRX00Eq[1] - Equalization control for channel 0 in group 0.

[0x0cd] EPRX01ChnCntr

Configuration of the channel 1 in group 0

Bit 7:4 - EPRX01PhaseSelect[3:0] - Selects the phase for channel 1 in group 0.

Bit 3 - EPRX01Invert - Inverts the channel 1 in group 0.

Bit 2 - EPRX01AcBias - Enables the common mode generation for channel 1 in group 0.

Bit 1 - EPRX01Term - Enables the 100 Ohm termination for channel 1 in group 0.

Bit 0 - EPRX01Eq[1] - Equalization control for channel 1 in group 0.

[0x0ce] EPRX02ChnCntr

Configuration of the channel 2 in group 0

Bit 7:4 - EPRX02PhaseSelect[3:0] - Selects the phase for channel 2 in group 0.

Bit 3 - EPRX02Invert - Inverts the channel 2 in group 0.

Bit 2 - EPRX02AcBias - Enables the common mode generation for channel 2 in group 0.

Bit 1 - EPRX02Term - Enables the 100 Ohm termination for channel 2 in group 0.

Bit 0 - EPRX02Eq[1] - Equalization control for channel 2 in group 0.

[0x0cf] EPRX03ChnCntr

Configuration of the channel 3 in group 0

Bit 7:4 - EPRX03PhaseSelect[3:0] - Selects the phase for channel 3 in group 0.

Bit 3 - EPRX03Invert - Inverts the channel 3 in group 0.

Bit 2 - EPRX03AcBias - Enables the common mode generation for channel 3 in group 0.

Bit 1 - EPRX03Term - Enables the 100 Ohm termination for channel 3 in group 0.

Bit 0 - EPRX03Eq[1] - Equalization control for channel 3 in group 0.

[0x0d0] EPRX10ChnCntr

Configuration of the channel 0 in group 1

Bit 7:4 - EPRX10PhaseSelect[3:0] - Selects the phase for channel 0 in group 1.

Bit 3 - EPRX10Invert - Inverts the channel 0 in group 1.

Bit 2 - EPRX10AcBias - Enables the common mode generation for channel 0 in group 1.

Bit 1 - EPRX10Term - Enables the 100 Ohm termination for channel 0 in group 1.

Bit 0 - EPRX10Eq[1] - Equalization control for channel 0 in group 1.

[0x0d1] EPRX11ChnCntr

Configuration of the channel 1 in group 1

Bit 7:4 - EPRX11PhaseSelect[3:0] - Selects the phase for channel 1 in group 1.

Bit 3 - EPRX11Invert - Inverts the channel 1 in group 1.

Bit 2 - EPRX11AcBias - Enables the common mode generation for channel 1 in group 1.

Bit 1 - EPRX11Term - Enables the 100 Ohm termination for channel 1 in group 1.

Bit 0 - EPRX11Eq[1] - Equalization control for channel 1 in group 1.

[0x0d2] EPRX12ChnCntr

Configuration of the channel 2 in group 1

Bit 7:4 - EPRX12PhaseSelect[3:0] - Selects the phase for channel 2 in group 1.

Bit 3 - EPRX12Invert - Inverts the channel 2 in group 1.

Bit 2 - EPRX12AcBias - Enables the common mode generation for channel 2 in group 1.

Bit 1 - EPRX12Term - Enables the 100 Ohm termination for channel 2 in group 1.

Bit 0 - EPRX12Eq[1] - Equalization control for channel 2 in group 1.

[0x0d3] EPRX13ChnCntr

Configuration of the channel 3 in group 1

Bit 7:4 - EPRX13PhaseSelect[3:0] - Selects the phase for channel 3 in group 1.

Bit 3 - EPRX13Invert - Inverts the channel 3 in group 1.

Bit 2 - EPRX13AcBias - Enables the common mode generation for channel 3 in group 1.

Bit 1 - EPRX13Term - Enables the 100 Ohm termination for channel 3 in group 1.

Bit 0 - EPRX13Eq[1] - Equalization control for channel 3 in group 1.

[0x0d4] EPRX20ChnCntr

Configuration of the channel 0 in group 2

Bit 7:4 - EPRX20PhaseSelect[3:0] - Selects the phase for channel 0 in group 2.

Bit 3 - EPRX20Invert - Inverts the channel 0 in group 2.

Bit 2 - EPRX20AcBias - Enables the common mode generation for channel 0 in group 2.

Bit 1 - EPRX20Term - Enables the 100 Ohm termination for channel 0 in group 2.

Bit 0 - EPRX20Eq[1] - Equalization control for channel 0 in group 2.

[0x0d5] EPRX21ChnCntr

Configuration of the channel 1 in group 2

Bit 7:4 - EPRX21PhaseSelect[3:0] - Selects the phase for channel 1 in group 2.

Bit 3 - EPRX21Invert - Inverts the channel 1 in group 2.

Bit 2 - EPRX21AcBias - Enables the common mode generation for channel 1 in group 2.

Bit 1 - EPRX21Term - Enables the 100 Ohm termination for channel 1 in group 2.

Bit 0 - EPRX21Eq[1] - Equalization control for channel 1 in group 2.

[0x0d6] EPRX22ChnCntr

Configuration of the channel 2 in group 2

Bit 7:4 - EPRX22PhaseSelect[3:0] - Selects the phase for channel 2 in group 2.

Bit 3 - EPRX22Invert - Inverts the channel 2 in group 2.

Bit 2 - EPRX22AcBias - Enables the common mode generation for channel 2 in group 2.

Bit 1 - EPRX22Term - Enables the 100 Ohm termination for channel 2 in group 2.

Bit 0 - EPRX22Eq[1] - Equalization control for channel 2 in group 2.

[0x0d7] EPRX23ChnCntr

Configuration of the channel 3 in group 2

Bit 7:4 - EPRX23PhaseSelect[3:0] - Selects the phase for channel 3 in group 2.

Bit 3 - EPRX23Invert - Inverts the channel 3 in group 2.

Bit 2 - EPRX23AcBias - Enables the common mode generation for channel 3 in group 2.

Bit 1 - EPRX23Term - Enables the 100 Ohm termination for channel 3 in group 2.

Bit 0 - EPRX23Eq[1] - Equalization control for channel 3 in group 2.

[0x0d8] EPRX30ChnCntr

Configuration of the channel 0 in group 3

Bit 7:4 - EPRX30PhaseSelect[3:0] - Selects the phase for channel 0 in group 3.

Bit 3 - EPRX30Invert - Inverts the channel 0 in group 3.

Bit 2 - EPRX30AcBias - Enables the common mode generation for channel 0 in group 3.

Bit 1 - EPRX30Term - Enables the 100 Ohm termination for channel 0 in group 3.

Bit 0 - EPRX30Eq[1] - Equalization control for channel 0 in group 3.

[0x0d9] EPRX31ChnCntr

Configuration of the channel 1 in group 3

Bit 7:4 - EPRX31PhaseSelect[3:0] - Selects the phase for channel 1 in group 3.

Bit 3 - EPRX31Invert - Inverts the channel 1 in group 3.

Bit 2 - EPRX31AcBias - Enables the common mode generation for channel 1 in group 3.

Bit 1 - EPRX31Term - Enables the 100 Ohm termination for channel 1 in group 3.

Bit 0 - EPRX31Eq[1] - Equalization control for channel 1 in group 3.

[0x0da] EPRX32ChnCntr

Configuration of the channel 2 in group 3

Bit 7:4 - EPRX32PhaseSelect[3:0] - Selects the phase for channel 2 in group 3.

Bit 3 - EPRX32Invert - Inverts the channel 2 in group 3.

Bit 2 - EPRX32AcBias - Enables the common mode generation for channel 2 in group 3.

Bit 1 - EPRX32Term - Enables the 100 Ohm termination for channel 2 in group 3.

Bit 0 - EPRX32Eq[1] - Equalization control for channel 2 in group 3.

[0x0db] EPRX33ChnCntr

Configuration of the channel 3 in group 3

Bit 7:4 - EPRX33PhaseSelect[3:0] - Selects the phase for channel 3 in group 3.

Bit 3 - EPRX33Invert - Inverts the channel 3 in group 3.

Bit 2 - EPRX33AcBias - Enables the common mode generation for channel 3 in group 3.

Bit 1 - EPRX33Term - Enables the 100 Ohm termination for channel 3 in group 3.

Bit 0 - EPRX33Eq[1] - Equalization control for channel 3 in group 3.

[0x0dc] EPRX40ChnCntr

Configuration of the channel 0 in group 4

Bit 7:4 - EPRX40PhaseSelect[3:0] - Selects the phase for channel 0 in group 4.

Bit 3 - EPRX40Invert - Inverts the channel 0 in group 4.

Bit 2 - EPRX40AcBias - Enables the common mode generation for channel 0 in group 4.

Bit 1 - EPRX40Term - Enables the 100 Ohm termination for channel 0 in group 4.

Bit 0 - EPRX40Eq[1] - Equalization control for channel 0 in group 4.

[0x0dd] EPRX41ChnCntr

Configuration of the channel 1 in group 4

Bit 7:4 - EPRX41PhaseSelect[3:0] - Selects the phase for channel 1 in group 4.

Bit 3 - EPRX41Invert - Inverts the channel 1 in group 4.

Bit 2 - EPRX41AcBias - Enables the common mode generation for channel 1 in group 4.

Bit 1 - EPRX41Term - Enables the 100 Ohm termination for channel 1 in group 4.

Bit 0 - EPRX41Eq[1] - Equalization control for channel 1 in group 4.

[0x0de] EPRX42ChnCntr

Configuration of the channel 2 in group 4

Bit 7:4 - EPRX42PhaseSelect[3:0] - Selects the phase for channel 2 in group 4.

Bit 3 - EPRX42Invert - Inverts the channel 2 in group 4.

Bit 2 - EPRX42AcBias - Enables the common mode generation for channel 2 in group 4.

Bit 1 - EPRX42Term - Enables the 100 Ohm termination for channel 2 in group 4.

Bit 0 - EPRX42Eq[1] - Equalization control for channel 2 in group 4.

[0x0df] EPRX43ChnCntr

Configuration of the channel 3 in group 4

Bit 7:4 - EPRX43PhaseSelect[3:0] - Selects the phase for channel 3 in group 4.

Bit 3 - EPRX43Invert - Inverts the channel 3 in group 4.

Bit 2 - EPRX43AcBias - Enables the common mode generation for channel 3 in group 4.

Bit 1 - EPRX43Term - Enables the 100 Ohm termination for channel 3 in group 4.

Bit 0 - EPRX43Eq[1] - Equalization control for channel 3 in group 4.

[0x0e0] EPRX50ChnCntr

Configuration of the channel 0 in group 5

Bit 7:4 - EPRX50PhaseSelect[3:0] - Selects the phase for channel 0 in group 5.

Bit 3 - EPRX50Invert - Inverts the channel 0 in group 5.

Bit 2 - EPRX50AcBias - Enables the common mode generation for channel 0 in group 5.

Bit 1 - EPRX50Term - Enables the 100 Ohm termination for channel 0 in group 5.

Bit 0 - EPRX50Eq[1] - Equalization control for channel 0 in group 5.

[0x0e1] EPRX51ChnCntr

Configuration of the channel 1 in group 5

Bit 7:4 - EPRX51PhaseSelect[3:0] - Selects the phase for channel 1 in group 5.

Bit 3 - EPRX51Invert - Inverts the channel 1 in group 5.

Bit 2 - EPRX51AcBias - Enables the common mode generation for channel 1 in group 5.

Bit 1 - EPRX51Term - Enables the 100 Ohm termination for channel 1 in group 5.

Bit 0 - EPRX51Eq[1] - Equalization control for channel 1 in group 5.

[0x0e2] EPRX52ChnCntr

Configuration of the channel 2 in group 5

Bit 7:4 - EPRX52PhaseSelect[3:0] - Selects the phase for channel 2 in group 5.

Bit 3 - EPRX52Invert - Inverts the channel 2 in group 5.

Bit 2 - EPRX52AcBias - Enables the common mode generation for channel 2 in group 5.

Bit 1 - EPRX52Term - Enables the 100 Ohm termination for channel 2 in group 5.

Bit 0 - EPRX52Eq[1] - Equalization control for channel 2 in group 5.

[0x0e3] EPRX53ChnCntr

Configuration of the channel 3 in group 5

Bit 7:4 - EPRX53PhaseSelect[3:0] - Selects the phase for channel 3 in group 5.

Bit 3 - EPRX53Invert - Inverts the channel 3 in group 5.

Bit 2 - EPRX53AcBias - Enables the common mode generation for channel 3 in group 5.

Bit 1 - EPRX53Term - Enables the 100 Ohm termination for channel 3 in group 5.

Bit 0 - EPRX53Eq[1] - Equalization control for channel 3 in group 5.

[0x0e4] EPRX60ChnCntr

Configuration of the channel 0 in group 6

Bit 7:4 - EPRX60PhaseSelect[3:0] - Selects the phase for channel 0 in group 6.

Bit 3 - EPRX60Invert - Inverts the channel 0 in group 6.

Bit 2 - EPRX60AcBias - Enables the common mode generation for channel 0 in group 6.

Bit 1 - EPRX60Term - Enables the 100 Ohm termination for channel 0 in group 6.

Bit 0 - EPRX60Eq[1] - Equalization control for channel 0 in group 6.

[0x0e5] EPRX61ChnCntr

Configuration of the channel 1 in group 6

Bit 7:4 - EPRX61PhaseSelect[3:0] - Selects the phase for channel 1 in group 6.

Bit 3 - EPRX61Invert - Inverts the channel 1 in group 6.

Bit 2 - EPRX61AcBias - Enables the common mode generation for channel 1 in group 6.

Bit 1 - EPRX61Term - Enables the 100 Ohm termination for channel 1 in group 6.

Bit 0 - EPRX61Eq[1] - Equalization control for channel 1 in group 6.

[0x0e6] EPRX62ChnCntr

Configuration of the channel 2 in group 6

Bit 7:4 - EPRX62PhaseSelect[3:0] - Selects the phase for channel 2 in group 6.

Bit 3 - EPRX62Invert - Inverts the channel 2 in group 6.

Bit 2 - EPRX62AcBias - Enables the common mode generation for channel 2 in group 6.

Bit 1 - EPRX62Term - Enables the 100 Ohm termination for channel 2 in group 6.

Bit 0 - EPRX62Eq[1] - Equalization control for channel 2 in group 6.

[0x0e7] EPRX63ChnCntr

Configuration of the channel 3 in group 6

Bit 7:4 - EPRX63PhaseSelect[3:0] - Selects the phase for channel 3 in group 6.

Bit 3 - EPRX63Invert - Inverts the channel 3 in group 6.

Bit 2 - EPRX63AcBias - Enables the common mode generation for channel 3 in group 6.

Bit 1 - EPRX63Term - Enables the 100 Ohm termination for channel 3 in group 6.

Bit 0 - EPRX63Eq[1] - Equalization control for channel 3 in group 6.

[0x0e8] EPRXEcChnCntr

Configuration of the EC channel in ePortRx

Bit 7:4 - EPRXECPhaseSelect[3:0] - Static phase for the EC channel.

Bit 3 - EPRXECInvert - Inverts the EC channel data input.

Bit 2 - EPRXECAcBias - Enables the common mode generation for the EC channel.

Bit 1 - EPRXECTerm - Enables the 100 Ohm termination for EC channel.

Bit 0 - EPRXECEnable - Enables the EC channel.

[0x0e9] EPRXEq10Control

Eport Rx equalization control for groups 1 and 0

Bit 7 - EPRX13Eq[0] - Equalization control for channel 3 in group 1.

EPRX13Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 6 - EPRX12Eq[0] - Equalization control for channel 2 in group 1.

EPRX12Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 5 - EPRX11Eq[0] - Equalization control for channel 1 in group 1.

EPRX11Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 4 - EPRX10Eq[0] - Equalization control for channel 0 in group 1.

EPRX10Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 3 - EPRX03Eq[0] - Equalization control for channel 3 in group 0.

EPRX03Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 2 - EPRX02Eq[0] - Equalization control for channel 2 in group 0.

EPRX02Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 1 - EPRX01Eq[0] - Equalization control for channel 1 in group 0.

EPRX01Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 0 - EPRX00Eq[0] - Equalization control for channel 0 in group 0.

EPRX00Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

[0x0ea] EPRXEq32Control

Eport Rx equalization control for groups 3 and 2

Bit 7 - EPRX33Eq[0] - Equalization control for channel 3 in group 3.

EPRX33Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 6 - EPRX32Eq[0] - Equalization control for channel 2 in group 3.

EPRX32Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 5 - EPRX31Eq[0] - Equalization control for channel 1 in group 3.

EPRX31Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 4 - EPRX30Eq[0] - Equalization control for channel 0 in group 3.

EPRX30Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 3 - EPRX23Eq[0] - Equalization control for channel 3 in group 2.

EPRX23Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 2 - EPRX22Eq[0] - Equalization control for channel 2 in group 2.

EPRX22Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 1 - EPRX21Eq[0] - Equalization control for channel 1 in group 2.

EPRX21Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 0 - EPRX20Eq[0] - Equalization control for channel 0 in group 2.

EPRX20Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

[0x0eb] EPRXEq54Control

Eport Rx equalization control for groups 5 and 4

Bit 7 - EPRX53Eq[0] - Equalization control for channel 3 in group 5.

EPRX53Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 6 - EPRX52Eq[0] - Equalization control for channel 2 in group 5.

EPRX52Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 5 - EPRX51Eq[0] - Equalization control for channel 1 in group 5.

EPRX51Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 4 - EPRX50Eq[0] - Equalization control for channel 0 in group 5.

EPRX50Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 3 - EPRX43Eq[0] - Equalization control for channel 3 in group 4.

EPRX43Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 2 - EPRX42Eq[0] - Equalization control for channel 2 in group 4.

EPRX42Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 1 - EPRX41Eq[0] - Equalization control for channel 1 in group 4.

EPRX41Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 0 - EPRX40Eq[0] - Equalization control for channel 0 in group 4.

EPRX40Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

[0x0ec] EPRXEq6Control

Eport Rx equalization control for group6

Bit 3 - EPRX63Eq[0] - Equalization control for channel 3 in group 6.

EPRX63Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 2 - EPRX62Eq[0] - Equalization control for channel 2 in group 6.

EPRX62Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 1 - EPRX61Eq[0] - Equalization control for channel 1 in group 6.

EPRX61Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

Bit 0 - EPRX60Eq[0] - Equalization control for channel 0 in group 6.

EPRX60Eq[1:0] Zero location [MHz] Peaking [dB]

2'd0 N/A N/A

2'd1 300 4.9

2'd2 125 7.8

2'd3 70 10.7

[0x0ed] POWERUP0

Controls behavior of the power up state machine (for more details refer to Power-up state machine)

Bit 6 - PUSMpllWdogDisable - Disables watch dog monitoring PLL locked signal

Bit 5 - PUSMdllWdogDisable - Disables watch dog monitoring DLL locked signal

Bit 4 - PUSMReadyWhenChnsLocked - When selected, ready signal is reported only after all enabled channels in all ePortRx groups are locked

Bit 3:0 - PUSMPllTimeoutConfig[3:0] - Determines the timeout duration in the WAIT\_PLL\_LOCK state in the power up state machine. For more details see Power-up state machine

PUSMPllTimeoutConfig[3:0] Wait time

4'd0 1 s

4'd1 500 ms

4'd2 100 ms

4'd3 50 ms

4'd4 20 ms

4'd5 10 ms

4'd6 5 ms

4'd7 2 ms

4'd8 1 ms

4'd9 500 us

4'd10 200 us

4'd11 100 us

4'd12 50 us

4'd13 20 us

4'd14 10 us

4'd15 disabled

[0x0ee] POWERUP1

Controls behavior of the power up state machine (for more details refer to Power-up state machine)

Bit 7:4 - PUSMDllTimeoutConfig[3:0] - Determines the timeout duration in the WAIT\_DLL\_LOCK state in the power up state machine. For more details see Power-up state machine

PUSMDllTimeoutConfig[3:0] Wait time

4'd0 1 s

4'd1 500 ms

4'd2 100 ms

4'd3 50 ms

4'd4 20 ms

4'd5 10 ms

4'd6 5 ms

4'd7 2 ms

4'd8 1 ms

4'd9 500 us

4'd10 200 us

4'd11 100 us

4'd12 50 us

4'd13 20 us

4'd14 10 us

4'd15 disabled

Bit 3:0 - PUSMChannelsTimeoutConfig[3:0] - Determines the timeout duration in the WAIT\_CHNS\_LOCKED state in the power up state machine. For more details see Power-up state machine.

PUSMChannelsTimeoutConfig[3:0] Wait time

4'd0 1 s

4'd1 500 ms

4'd2 100 ms

4'd3 50 ms

4'd4 20 ms

4'd5 10 ms

4'd6 5 ms

4'd7 2 ms

4'd8 1 ms

4'd9 500 us

4'd10 200 us

4'd11 100 us

4'd12 50 us

4'd13 20 us

4'd14 10 us

4'd15 disabled

15.1.17. Power Up State Machine

[0x0ef] POWERUP2

Controls behavior of the power up state machine (for more details refer to Power-up state machine)

Bit 2 - dllConfigDone - When asserted, the power up state machine is allowed to proceed to PLL initialization. Please refer Configuration for more details.

Bit 1 - pllConfigDone - When asserted, the power up state machine is allowed to proceed to initialization of components containing DLLs (ePortRx, phase-shifter). Please refer Configuration for more details.

Bit 0 - updateEnable - When asserted, the power up state machine copies the values from fuses to configuration registers during power. Please refer Configuration for more details.

15.2. Read/Write

15.2.1. I2C Masters

[0x0f0] I2CM0Config

General configuration register for I2C Master 0

Bit 6 - I2CM0SCLPullUpEnable - Enable pull up for M0SCL pin.

Bit 5 - I2CM0SCLDriveStrength - M0SCL drive strength (CMOS I/O Pin Characteristics)

Bit 4 - I2CM0SDAPullUpEnable - Enable pull up for M0SDA pin.

Bit 3 - I2CM0SDADriveStrength - M0SDA drive strength (CMOS I/O Pin Characteristics).

Bit 2:0 - I2CM0AddressExt[2:0] - 3 additional bits of address of slave to address in an I2C transaction for I2C Master 0; only used in commands with 10-bit addressing

[0x0f1] I2CM0Address

7 bits of address of slave to address in an I2C transaction for I2C Master 0

Bit 6:0 - I2CM0Address[6:0] - 7 bits of address of slave to address in an I2C transaction

[0x0f2] I2CM0Data0

Data input for I2C Master 0

Bit 7:0 - I2CM0Data[7:0] - Bits 7:0 of the data input

[0x0f3] I2CM0Data1

Data input for I2C Master 0

Bit 7:0 - I2CM0Data[15:8] - Bits 15:8 of the data input

[0x0f4] I2CM0Data2

Data input for I2C Master 0

Bit 7:0 - I2CM0Data[23:16] - Bits 23:16 of the data input

[0x0f5] I2CM0Data3

Data input for I2C Master 0

Bit 7:0 - I2CM0Data[31:24] - Bits 31:24 of the data input

[0x0f6] I2CM0Cmd

Command word register for I2C Master 0

Bit 3:0 - I2CM0Cmd[3:0] - Command word.

[0x0f7] I2CM1Config

General configuration register for I2C Master 1

Bit 6 - I2CM1SCLPullUpEnable - Enable pull up for M1SCL pin.

Bit 5 - I2CM1SCLDriveStrength - M1SCL drive strength (CMOS I/O Pin Characteristics)

Bit 4 - I2CM1SDAPullUpEnable - Enable pull up for M1SDA pin.

Bit 3 - I2CM1SDADriveStrength - M1SDA drive strength (CMOS I/O Pin Characteristics).

Bit 2:0 - I2CM1AddressExt[2:0] - 3 additional bits of address of slave to address in an I2C transaction for I2C Master 1; only used in commands with 10-bit addressing

[0x0f8] I2CM1Address

7 bits of address of slave to address in an I2C transaction for I2C Master 1

Bit 6:0 - I2CM1Address[6:0] - 7 bits of address of slave to address in an I2C transaction

[0x0f9] I2CM1Data0

Data input for I2C Master 1

Bit 7:0 - I2CM1Data[7:0] - Bits 7:0 of the data input

[0x0fa] I2CM1Data1

Data input for I2C Master 1

Bit 7:0 - I2CM1Data[15:8] - Bits 15:8 of the data input

[0x0fb] I2CM1Data2

Data input for I2C Master 1

Bit 7:0 - I2CM1Data[23:16] - Bits 23:16 of the data input

[0x0fc] I2CM1Data3

Data input for I2C Master 1

Bit 7:0 - I2CM1Data[31:24] - Bits 31:24 of the data input

[0x0fd] I2CM1Cmd

Command word register for I2C Master 1

Bit 3:0 - I2CM1Cmd[3:0] - Command word.

[0x0fe] I2CM2Config

General configuration register for I2C Master 2

Bit 6 - I2CM2SCLPullUpEnable - Enable pull up for M2SCL pin.

Bit 5 - I2CM2SCLDriveStrength - M2SCL drive strength (CMOS I/O Pin Characteristics)

Bit 4 - I2CM2SDAPullUpEnable - Enable pull up for M2SDA pin.

Bit 3 - I2CM2SDADriveStrength - M2SDA drive strength (CMOS I/O Pin Characteristics).

Bit 2:0 - I2CM2AddressExt[2:0] - 3 additional bits of address of slave to address in an I2C transaction for I2C Master 2; only used in commands with 10-bit addressing

[0x0ff] I2CM2Address

7 bits of address of slave to address in an I2C transaction for I2C Master 2

Bit 6:0 - I2CM2Address[6:0] - 7 bits of address of slave to address in an I2C transaction

[0x100] I2CM2Data0

Data input for I2C Master 2

Bit 7:0 - I2CM2Data[7:0] - Bits 7:0 of the data input

[0x101] I2CM2Data1

Data input for I2C Master 2

Bit 7:0 - I2CM2Data[15:8] - Bits 15:8 of the data input

[0x102] I2CM2Data2

Data input for I2C Master 2

Bit 7:0 - I2CM2Data[23:16] - Bits 23:16 of the data input

[0x103] I2CM2Data3

Data input for I2C Master 2

Bit 7:0 - I2CM2Data[31:24] - Bits 31:24 of the data input

[0x104] I2CM2Cmd

Command word register for I2C Master 2

Bit 3:0 - I2CM2Cmd[3:0] - Command word.

15.2.2. ePortRx

[0x105] EPRXTrain10

Channel phase training request for groups 1 and 0

Bit 7:4 - EPRX1Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

Bit 3:0 - EPRX0Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

[0x106] EPRXTrain32

Channel phase training request for groups 3 and 2

Bit 7:4 - EPRX3Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

Bit 3:0 - EPRX2Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

[0x107] EPRXTrain54

Channel phase training request for groups 5 and 4

Bit 7:4 - EPRX5Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

Bit 3:0 - EPRX4Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

[0x108] EPRXTrainEc6

Channel phase training request for group 6 and EC channel

Bit 4 - EPRXEcTrain - Initialize phase training for EC channel.

Bit 3:0 - EPRX6Train[3:0] - Initialize phase training. N-th bit control N-th channel training.

One should assert bits corresponding to channels to be trained and dessert them.

15.2.3. E-FUSES

[0x109] FUSEControl

Fuse control register.

Bit 7:4 - FuseBlowPulseLength[3:0] - Duration of fuse blowing pulse (default:12).

Bit 1 - FuseRead - Execute fuse readout sequence.

Bit 0 - FuseBlow - Execute fuse blowing sequence.

[0x10a] FUSEBlowDataA

Data to be programmed to the fuses.

Bit 7:0 - FuseBlowData[7:0] - Bits 7:0 of the data word.

[0x10b] FUSEBlowDataB

Data to be programmed to the fuses.

Bit 7:0 - FuseBlowData[15:8] - Bits 15:8 of the data word.

[0x10c] FUSEBlowDataC

Data to be programmed to the fuses.

Bit 7:0 - FuseBlowData[23:16] - Bits 23:16 of the data word.

[0x10d] FUSEBlowDataD

Data to be programmed to the fuses.

Bit 7:0 - FuseBlowData[31:24] - Bits 31:24 of the data word.

[0x10e] FUSEBlowAddH

Address of the fuse block to be programmed.

Bit 7:0 - FuseBlowAddress[15:8] - Bits 15:8 of the address.

[0x10f] FUSEBlowAddL

Address of the fuse block to be programmed.

Bit 7:0 - FuseBlowAddress[7:0] - Bits 7:0 of the address.

[0x110] FuseMagic

Registers containing magic number for the fuse block.

Bit 7:0 - FuseMagicNumber[7:0] - One has to write a magic number 0xA3 to this register in order to unlock fuse blowing.

15.2.4. ADC

[0x111] ADCSelect

ADC MUXes control.

Bit 7:4 - ADCInPSelect[3:0] - Controls MUX for ADC Positive Input

ADCInPSelect[3:0] Input

4'd0 ADC0 (external pin)

4'd1 ADC1 (external pin)

4'd2 ADC2 (external pin)

4'd3 ADC3 (external pin)

4'd4 ADC4 (external pin)

4'd5 ADC5 (external pin)

4'd6 ADC6 (external pin)

4'd7 ADC7 (external pin)

4'd8 EOM DAC (internal signal)

4'd9 VDDIO \* 0.42 (internal signal)

4'd10 VDDTX \* 0.42 (internal signal)

4'd11 VDDRX \* 0.42 (internal signal)

4'd12 VDD \* 0.42 (internal signal)

4'd13 VDDA \* 0.42 (internal signal)

4'd14 Temperature sensor (internal signal)

4'd15 VREF / 2 (internal signal)

Bit 3:0 - ADCInNSelect[3:0] - Controls MUX for ADC Negative Input

ADCInNSelect[3:0] Input

4'd0 ADC0 (external pin)

4'd1 ADC1 (external pin)

4'd2 ADC2 (external pin)

4'd3 ADC3 (external pin)

4'd4 ADC4 (external pin)

4'd5 ADC5 (external pin)

4'd6 ADC6 (external pin)

4'd7 ADC7 (external pin)

4'd8 EOM DAC (internal signal)

4'd9 VDDIO \* 0.42 (internal signal)

4'd10 VDDTX \* 0.42 (internal signal)

4'd11 VDDRX \* 0.42 (internal signal)

4'd12 VDD \* 0.42 (internal signal)

4'd13 VDDA \* 0.42 (internal signal)

4'd14 Temperature sensor (internal signal)

4'd15 VREF / 2 (internal signal)

See also: [0x113] ADCConfig, [0x112] ADCMon

[0x112] ADCMon

Control ADC's internal signals

Bit 5 - TEMPSensReset - Resets temperature sensor.

Bit 4 - VDDmonEna - Enable resistive divider for VDD probing.

Bit 3 - VDDTXmonEna - Enable resistive divider for VDDTX probing.

Bit 2 - VDDRXmonEna - Enable resistive divider for VDDRX probing.

Bit 1 - VDDPSTmonEna - Enable resistive divider for VDDPST probing.

Bit 0 - VDDANmonEna - Enable resistive divider for VDDAB probing.

See also: [0x113] ADCConfig, [0x111] ADCSelect

[0x113] ADCConfig

ADC configuration register

Bit 7 - ADCConvert - Start ADC conversion.

Bit 2 - ADCEnable - Enables ADC core and differential amplifier.

Bit 1:0 - ADCGainSelect[1:0] - Selects gain for the differential amplifier

ADCGainSel[1:0] Gain

2'd0 x2

2'd1 x8

2'd2 x16

2'd3 x32

See also: [0x112] ADCMon, [0x111] ADCSelect

15.2.5. Eye Opening Monitor

[0x114] EOMConfigH

Bit 7:4 - EOMendOfCountSel[3:0] - Amount of refClk clock cycles (40 MHz cycles) the EOM counter is gated (2^(selEndOfCount+1))

Bit 2 - EOMBypassPhaseInterpolator - Bypass the VCO 5.12 GHz clock (uses the refClk as the phase interpolated clock; the phase interpolation has to be done off-chip) [0 - vco, 1 - refClk]

Bit 1 - EOMStart - Starts EOM acquisition

Bit 0 - EOMEnable - Enables the EOM; wait few ms for all bias voltages to stabilize before starting EOM measurement

[0x115] EOMConfigL

Bit 5:0 - EOMphaseSel[5:0] - Selects the sampling phase from the phase interpolation block; steps [0:1/(fvco\*64):63/(fvco\*64)] s

[0x116] EOMvofSel

Bit 4:0 - EOMvofSel[4:0] - Selects the comparison voltage; the comparator is differential; steps [-VDDRX/2:VDDRX/30:VDDRX/2] V; value 5'd32 is invalid

15.2.6. Process Monitor

[0x117] ProcessAndSeuMonitor

Process Monitor block configuration register

Bit 4 - DLDPFecCounterEnable - Enable downlink FEC counter.

Bit 3 - SEUEnable - Enable SEU counter.

Bit 2:1 - PMChannel[1:0] - Select process monitor channel to be measured.

Bit 0 - PMEnable - Enable process monitor block.

15.2.7. Testing

[0x118] ULDataSource0

Uplink data path test patterns.

Bit 7:5 - ULECDataSource[2:0] - Data source for uplink EC channel

ULGECDataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[1:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[1:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

Bit 3:0 - ULSerTestPattern[3:0] - Controls the serializer data source.

ULSerTestPattern[3:0] Name Description

4'd0 DATA Normal mode of operation

4'd1 PRBS7 PRBS7 test pattern

4'd2 PRBS15 PRBS15 test pattern

4'd3 PRBS23 PRBS23 test pattern

4'd4 PRBS31 PRBS31 test pattern

4'd5 CLK5G12 5.12 GHz clock pattern (in 5Gbps mode it will produce only 2.56 GHz)

4'd6 CLK2G56 2.56 GHz clock pattern

4'd7 CLK1G28 1.28 GHz clock pattern

4'd8 CLK40M 40 MHz clock pattern

4'd9 DLFRAME\_10G24 Loopback, downlink frame repeated 4 times

4'd10 DLFRAME\_5G12 Loopback, downlink frame repeated 2 times, each bit repeated 2 times

4'd11 DLFRAME\_2G56 Loopback, downlink frame repeated 1 times, each bit repeated 4 times

4'd12 CONST PATTERN 8 x DPDataPattern[31:0]

4'd13

Reserved

4'd14

Reserved

4'd15

Reserved

[0x119] ULDataSource1

Uplink data path test patterns.

Bit 7:6 - LDDataSource[1:0] - Data source for the line driver.

LDDataSource[1:0] Description

2'd0 Data from serializer (normal mode of operation)

2'd1 Data resampled by CDR loopback

2'd2 Equalizer output data loopback

2'd3 reserved

Bit 5:3 - ULG1DataSource[2:0] - Data source for uplink data group 1

ULG1DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

Bit 2:0 - ULG0DataSource[2:0] - Data source for uplink data group 0

ULG0DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

[0x11a] ULDataSource2

Uplink data path test patterns.

Bit 5:3 - ULG3DataSource[2:0] - Data source for uplink data group 3

ULG3DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

Bit 2:0 - ULG2DataSource[2:0] - Data source for uplink data group 2

ULG2DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

[0x11b] ULDataSource3

Uplink data path test patterns.

Bit 5:3 - ULG5DataSource[2:0] - Data source for uplink data group 5

ULG5DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

Bit 2:0 - ULG4DataSource[2:0] - Data source for uplink data group 4

ULG4DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

[0x11c] ULDataSource4

Uplink data path test patterns.

Bit 7:6 - DLECDataSource[1:0] -

Bit 5:3 - ULICDataSource[2:0] -

Bit 2:0 - ULG6DataSource[2:0] - Data source for uplink data group 6

ULG6DataSource[2:0] Name Description

3'd0 EPORTRX\_DATA Normal mode of operation, data from ePortRx

3'd1 PRBS7 PRBS7 test pattern

3'd2 BIN\_CNTR\_UP Binary counter counting up

3'd3 BIN\_CNTR\_DOWN Binary counter counting down

3'd4 CONST\_PATTERN Constant pattern (DPDataPattern[31:0])

3'd5 CONST\_PATTERN\_INV Constant pattern inverted (~DPDataPattern[31:0])

3'd6 DLDATA\_LOOPBACK Loop back, downlink frame data

3'd7 Reserved Reserved

[0x11d] ULDataSource5

Bit 7:6 - DLG3DataSource[1:0] - Controls the ePortTx group 3 data source

DLG3DataSource[1:0] Name Description

2'd0 LINK\_DATA Normal mode of operation, data from ePortRx

2'd1 PRBS7 PRBS7 patter on each channel

2'd2 BIN\_CNTR\_UP Binary counter counting up on each channel

2'd3 CONST\_PATTERN Constant pattern

Bit 5:4 - DLG2DataSource[1:0] - Controls the ePortTx group 2 data source

DLG2DataSource[1:0] Name Description

2'd0 LINK\_DATA Normal mode of operation, data from ePortRx

2'd1 PRBS7 PRBS7 patter on each channel

2'd2 BIN\_CNTR\_UP Binary counter counting up on each channel

2'd3 CONST\_PATTERN Constant pattern

Bit 3:2 - DLG1DataSource[1:0] - Controls the ePortTx group 1 data source

DLG1DataSource[1:0] Name Description

2'd0 LINK\_DATA Normal mode of operation, data from ePortRx

2'd1 PRBS7 PRBS7 patter on each channel

2'd2 BIN\_CNTR\_UP Binary counter counting up on each channel

2'd3 CONST\_PATTERN Constant pattern

Bit 1:0 - DLG0DataSource[1:0] - Controls the ePortTx group 0 data source

DLG0DataSource[1:0] Name Description

2'd0 LINK\_DATA Normal mode of operation, data from ePortRx

2'd1 PRBS7 PRBS7 patter on each channel

2'd2 BIN\_CNTR\_UP Binary counter counting up on each channel

2'd3 CONST\_PATTERN Constant pattern

[0x11e] DPDataPattern3

Constant patter to be used in test pattern generation/checking

Bit 7:0 - DPDataPattern[31:24] - Bits 31:24 of the canst pattern.

[0x11f] DPDataPattern2

Constant patter to be used in test pattern generation/checking

Bit 7:0 - DPDataPattern[23:16] - Bits 23:16 of the canst pattern.

[0x120] DPDataPattern1

Constant patter to be used in test pattern generation/checking

Bit 7:0 - DPDataPattern[15:8] - Bits 15:8 of the canst pattern.

[0x121] DPDataPattern0

Constant patter to be used in test pattern generation/checking

Bit 7:0 - DPDataPattern[7:0] - Bits 7:0 of the canst pattern.

[0x122] EPRXPRBS3

Control registers for build-in PRBS7 generators in ePortRx.

Bit 4 - EPRXECPrbsEnable -

Bit 3 - EPRX63PrbsEnable - Enables PRBS7 generator for channel 3 in group 6. If enabled, the data from the input pin are discarded.

Bit 2 - EPRX62PrbsEnable - Enables PRBS7 generator for channel 2 in group 6. If enabled, the data from the input pin are discarded.

Bit 1 - EPRX61PrbsEnable - Enables PRBS7 generator for channel 1 in group 6. If enabled, the data from the input pin are discarded.

Bit 0 - EPRX60PrbsEnable - Enables PRBS7 generator for channel 0 in group 6. If enabled, the data from the input pin are discarded.

[0x123] EPRXPRBS2

Control registers for build-in PRBS7 generators in ePortRx.

Bit 7 - EPRX53PrbsEnable - Enables PRBS7 generator for channel 3 in group 5. If enabled, the data from the input pin are discarded.

Bit 6 - EPRX52PrbsEnable - Enables PRBS7 generator for channel 2 in group 5. If enabled, the data from the input pin are discarded.

Bit 5 - EPRX51PrbsEnable - Enables PRBS7 generator for channel 1 in group 5. If enabled, the data from the input pin are discarded.

Bit 4 - EPRX50PrbsEnable - Enables PRBS7 generator for channel 0 in group 5. If enabled, the data from the input pin are discarded.

Bit 3 - EPRX43PrbsEnable - Enables PRBS7 generator for channel 3 in group 4. If enabled, the data from the input pin are discarded.

Bit 2 - EPRX42PrbsEnable - Enables PRBS7 generator for channel 2 in group 4. If enabled, the data from the input pin are discarded.

Bit 1 - EPRX41PrbsEnable - Enables PRBS7 generator for channel 1 in group 4. If enabled, the data from the input pin are discarded.

Bit 0 - EPRX40PrbsEnable - Enables PRBS7 generator for channel 0 in group 4. If enabled, the data from the input pin are discarded.

[0x124] EPRXPRBS1

Control registers for build-in PRBS7 generators in ePortRx.

Bit 7 - EPRX33PrbsEnable - Enables PRBS7 generator for channel 3 in group 3. If enabled, the data from the input pin are discarded.

Bit 6 - EPRX32PrbsEnable - Enables PRBS7 generator for channel 2 in group 3. If enabled, the data from the input pin are discarded.

Bit 5 - EPRX31PrbsEnable - Enables PRBS7 generator for channel 1 in group 3. If enabled, the data from the input pin are discarded.

Bit 4 - EPRX30PrbsEnable - Enables PRBS7 generator for channel 0 in group 3. If enabled, the data from the input pin are discarded.

Bit 3 - EPRX23PrbsEnable - Enables PRBS7 generator for channel 3 in group 2. If enabled, the data from the input pin are discarded.

Bit 2 - EPRX22PrbsEnable - Enables PRBS7 generator for channel 2 in group 2. If enabled, the data from the input pin are discarded.

Bit 1 - EPRX21PrbsEnable - Enables PRBS7 generator for channel 1 in group 2. If enabled, the data from the input pin are discarded.

Bit 0 - EPRX20PrbsEnable - Enables PRBS7 generator for channel 0 in group 2. If enabled, the data from the input pin are discarded.

[0x125] EPRXPRBS0

Control registers for build-in PRBS7 generators in ePortRx.

Bit 7 - EPRX13PrbsEnable - Enables PRBS7 generator for channel 3 in group 1. If enabled, the data from the input pin are discarded.

Bit 6 - EPRX12PrbsEnable - Enables PRBS7 generator for channel 2 in group 1. If enabled, the data from the input pin are discarded.

Bit 5 - EPRX11PrbsEnable - Enables PRBS7 generator for channel 1 in group 1. If enabled, the data from the input pin are discarded.

Bit 4 - EPRX10PrbsEnable - Enables PRBS7 generator for channel 0 in group 1. If enabled, the data from the input pin are discarded.

Bit 3 - EPRX03PrbsEnable - Enables PRBS7 generator for channel 3 in group 0. If enabled, the data from the input pin are discarded.

Bit 2 - EPRX02PrbsEnable - Enables PRBS7 generator for channel 2 in group 0. If enabled, the data from the input pin are discarded.

Bit 1 - EPRX01PrbsEnable - Enables PRBS7 generator for channel 1 in group 0. If enabled, the data from the input pin are discarded.

Bit 0 - EPRX00PrbsEnable - Enables PRBS7 generator for channel 0 in group 0. If enabled, the data from the input pin are discarded.

[0x126] BERTSource

Data source for the built-in BER checker.

Bit 7:0 - BERTSource[7:0] - Please refer to Section 14.2 for more details.

[0x127] BERTConfig

Configuration for the Bit Error Rate Test.

Bit 7:4 - BERTMeasTime[3:0] - Test time. For more details please refer to Table 14.5

Bit 1 - SKIPDisable - Disable the skip cycle signal originating from the frame aligner. It is used when testing raw PRBS sequences on the downlink.

Bit 0 - BERTStart - Asserting this bit start the BERT measurement.

[0x128] BERTDataPattern3

Fixed data pattern used by the BERT checker.

Bit 7:0 - BERTDataPattern[31:24] - Bits 31:24 of the fixed pattern for BERT.

[0x129] BERTDataPattern2

Fixed data pattern used by the BERT checker.

Bit 7:0 - BERTDataPattern[23:16] - Bits 23:16 of the fixed pattern for BERT.

[0x12a] BERTDataPattern1

Fixed data pattern used by the BERT checker.

Bit 7:0 - BERTDataPattern[15:8] - Bits 15:8 of the fixed pattern for BERT.

[0x12b] BERTDataPattern0

Fixed data pattern used by the BERT checker.

Bit 7:0 - BERTDataPattern[7:0] - Bits 7:0 of the fixed pattern for BERT.

15.2.8. Reset Manager

[0x12c] RST0

Reset related register. Enables resetting several components.

Bit 7 - RSTpllDigital - Resets the PLL control logic.

Bit 6 - RSTfuses - Resets the e-fuses control logic.

Bit 5 - RSTconfig - Resets the configuration block.

Bit 4 - RSTrxLogic - Resets the RXphy of serial configuration interface.

Bit 3 - RSTtxLogic - Resets the TXphy of serial configuration interface.

Bit 2 - RSTi2cm0 - Resets channel 0 I2C master. One should generate a pulse on this bit (0->1->0).

Bit 1 - RSTi2cm1 - Resets channel 1 I2C master. One should generate a pulse on this bit (0->1->0).

Bit 0 - RSTi2cm2 - Resets channel 2 I2C master. One should generate a pulse on this bit (0->1->0).

[0x12d] RST1

Reset related register. Enables resetting several components.

Bit 7 - RSTframeAligner - Resets the frame aligner.

Bit 6 - RSTeprx6Dll - Resets the master DLL in ePortRx group 6.

Bit 5 - RSTeprx5Dll - Resets the master DLL in ePortRx group 5.

Bit 4 - RSTeprx4Dll - Resets the master DLL in ePortRx group 4.

Bit 3 - RSTeprx3Dll - Resets the master DLL in ePortRx group 3.

Bit 2 - RSTeprx2Dll - Resets the master DLL in ePortRx group 2.

Bit 1 - RSTeprx1Dll - Resets the master DLL in ePortRx group 1.

Bit 0 - RSTeprx0Dll - Resets the master DLL in ePortRx group 0.

[0x12e] RST2

Reset related register. Enables resetting several components.

Bit 7 - SKIPforce - Toggling this bit allows to issue a skip cycle command (equivalent to the one issued by the frame aligner).

This functionality is is foreseen only for debugging purposes.

Bit 6 - ResetOutForceActive - As long as this bit is set low, the resetOut signal is active (low level).

Bit 3 - RSTps3Dll - Resets DLL in 3 phase aligner channel.

Bit 2 - RSTps2Dll - Resets DLL in 2 phase aligner channel.

Bit 1 - RSTps1Dll - Resets DLL in 1 phase aligner channel.

Bit 0 - RSTps0Dll - Resets DLL in 0 phase aligner channel.

15.2.9. Power Up

[0x12f] POWERUP3

Controls behavior of the power up state machine (for more details refer to Power-up state machine)

Bit 7 - PUSMForceState - Allows to override the state of power up state machine. To enable this feature, register PUSMForceMagic has to be set to 0xA3 (magic number)

Bit 4:0 - PUSMStateForced[4:0] - Selects state of the power up state machine when STATEOVRD pin is asserted or PUSMForceState bit is asserted. For more details refer to Power-up state machine and STATEOVRD)

[0x130] POWERUP4

Controls behavior of the power up state machine (for more details refer to Power-up state machine)

Bit 7:0 - PUSMForceMagic[7:0] - Has to be set to 0xA3 (magic number) in order to enable PUSMForceState feature.

15.2.10. Debug

[0x131] CLKTree

Clock tree disable feature. Could be used for TMR testing.

Bit 7:3 - ClkTreeMagicNumber[4:0] - Has to be set to 5'h15 in order for clock masking (disabling) to be active

Bit 2 - clkTreeCDisable - If asserted and ClkTreeMagicNumber set to 5'h15, branch C of clock tree is disabled

Bit 1 - clkTreeBDisable - If asserted and ClkTreeMagicNumber set to 5'h15, branch B of clock tree is disabled

Bit 0 - clkTreeADisable - If asserted and ClkTreeMagicNumber set to 5'h15, branch A of clock tree is disabled

[0x132] DataPath

Data path configuration.

Bit 7 - DLDPBypasDeInterlevear - Bypass de-interleaver in the downlink data path.

Bit 6 - DLDPBypasFECDecoder - Bypass FEC decoder in the downlink data path.

Bit 5 - DLDPBypassDeScrambler - Bypass de-scrambler in the downlink data path.

Bit 4 - DLDPFECErrCntEna - Unused.

Bit 2 - ULDPBypassInterleaver - Bypass interleaver in the uplink data path.

Bit 1 - ULDPBypassScrambler - Bypass scrambler in the uplink data path.

Bit 0 - ULDPBypassFECCoder - Bypass FEC coder in the uplink data path.

[0x133] TO0Sel

Control register for test output 0

Bit 7:0 - TO0Select[7:0] - Selects a signal to be outputted on TSTOUT0 according to TOnSelect

[0x134] TO1Sel

Control register for test output 1

Bit 7:0 - TO1Select[7:0] - Selects a signal to be outputted on TSTOUT1 according to TOnSelect

[0x135] TO2Sel

Control register for test output 2

Bit 7:0 - TO2Select[7:0] - Selects a signal to be outputted on TSTOUT2 according to TOnSelect

[0x136] TO3Sel

Control register for test output 3

Bit 7:0 - TO3Select[7:0] - Selects a signal to be outputted on TSTOUT3 according to TOnSelect

[0x137] TO4Sel

Control register for test output 4

Bit 7:0 - TO4Select[7:0] - Selects a signal to be outputted on TSTOUT4 according to TOnSelect

[0x138] TO5Sel

Control register for test output 5

Bit 7:0 - TO5Select[7:0] - Selects a signal to be outputted on TSTOUT5 according to TOnSelect

[0x139] TODrivingStrength

Driving strength control for CMOS test outputs

Bit 3 - TO3DS - Drive strength for TSTOUT3 (CMOS I/O Pin Characteristics)

Bit 2 - TO2DS - Drive strength for TSTOUT2 (CMOS I/O Pin Characteristics)

Bit 1 - TO1DS - Drive strength for TSTOUT1 (CMOS I/O Pin Characteristics)

Bit 0 - TO0DS - Drive strength for TSTOUT0 (CMOS I/O Pin Characteristics)

[0x13a] TO4Driver

Output driver control for test output 4

Bit 7:5 - TO4PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for TO4.

TO4PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - TO4PreEmphasisMode[1:0] - Selects the pre-emphasis mode for TO4.

TO4PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - TO4DriveStrength[2:0] - Sets the pre-emphasis strength for TO4.

TO4DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x13b] TO5Driver

Output driver control for test output 5

Bit 7:5 - TO5PreEmphasisStrength[2:0] - Sets the pre-emphasis strength for TO5.

TO5PreEmphasisStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

Bit 4:3 - TO5PreEmphasisMode[1:0] - Selects the pre-emphasis mode for TO5.

TO5PreEmphasisMode[1:0] Mode

2'd0 disabled

2'd1 disabled

2'd2 Self timed

2'd3 Clock timed

Bit 2:0 - TO5DriveStrength[2:0] - Sets the pre-emphasis strength for TO5.

TO5DriveStrength[2:0] Strength [mA]

3'd0 0

3'd1 1.0

3'd2 1.5

3'd3 2.0

3'd4 2.5

3'd5 3.0

3'd6 3.5

3'd7 4.0

[0x13c] TOPreEmp

Pre-emphasis control for differential test outputs

Bit 7 - TO5Invert -

Bit 6:4 - TO5PreEmphasisWidth[2:0] - Sets the pre-emphasis strength for TO5.

TO5PreEmphasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

Bit 3 - TO4Invert -

Bit 2:0 - TO4PreEmphasisWidth[2:0] - Sets the pre-emphasis strength for TO4.

TO4PreEmphasisWidth[2:0] Pulse length [ps]

3'd0 120

3'd1 240

3'd2 360

3'd3 480

3'd4 600

3'd5 720

3'd6 840

3'd7 960

15.3. Read Only

15.3.1. LPGBTSettings

[0x140] ConfigPins

Status of the lpGBT external configuration pins

Bit 7:4 - LPGBTMode[3:0] - State of MODE pins. The function of the pin is described in MODE3, MODE2, MODE1, MODE0.

Bit 3 - ConfigSelect - State of SC\_I2C pin. The function of the pin is described in SC\_I2C.

Bit 2 - VCOBypass - State of the VCOBYPASS pin. The function of the pin is described in VCOBYPASS.

Bit 1 - lockMode - State of the LOCKMODE pin. The function of the pin is described in LOCKMODE.

Bit 0 - stateOverride - State of the STATEOVRD. The function of the pin is described in STATEOVRD. `

[0x141] I2CSlaveAddress

Chip address.

Bit 6:0 - AsicControlAdr[6:0] - Address of the chip used in slow control protocols (I2C, IC, EC).

15.3.2. ePortRx

[0x142] EPRX0Locked

ePortRx group 0 status register

Bit 7:4 - EPRX0ChnLocked[3:0] - Status of phase selection logic for channels in group 0. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX0State[1:0] - State of initialization state machine for ePortRx group 0. State can be according to the table:

EPRX0State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x143] EPRX0CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 0

Bit 7:4 - EPRX0CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 0

Bit 3:0 - EPRX0CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 0

[0x144] EPRX0CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 0

Bit 7:4 - EPRX0CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 0

Bit 3:0 - EPRX0CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 0

[0x145] EPRX1Locked

ePortRx group 1 status register

Bit 7:4 - EPRX1ChnLocked[3:0] - Status of phase selection logic for channels in group 1. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX1State[1:0] - State of initialization state machine for ePortRx group 1. State can be according to the table:

EPRX1State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x146] EPRX1CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 1

Bit 7:4 - EPRX1CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 1

Bit 3:0 - EPRX1CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 1

[0x147] EPRX1CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 1

Bit 7:4 - EPRX1CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 1

Bit 3:0 - EPRX1CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 1

[0x148] EPRX2Locked

ePortRx group 2 status register

Bit 7:4 - EPRX2ChnLocked[3:0] - Status of phase selection logic for channels in group 2. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX2State[1:0] - State of initialization state machine for ePortRx group 2. State can be according to the table:

EPRX2State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x149] EPRX2CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 2

Bit 7:4 - EPRX2CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 2

Bit 3:0 - EPRX2CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 2

[0x14a] EPRX2CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 2

Bit 7:4 - EPRX2CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 2

Bit 3:0 - EPRX2CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 2

[0x14b] EPRX3Locked

ePortRx group 3 status register

Bit 7:4 - EPRX3ChnLocked[3:0] - Status of phase selection logic for channels in group 3. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX3State[1:0] - State of initialization state machine for ePortRx group 3. State can be according to the table:

EPRX3State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x14c] EPRX3CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 3

Bit 7:4 - EPRX3CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 3

Bit 3:0 - EPRX3CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 3

[0x14d] EPRX3CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 3

Bit 7:4 - EPRX3CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 3

Bit 3:0 - EPRX3CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 3

[0x14e] EPRX4Locked

ePortRx group 4 status register

Bit 7:4 - EPRX4ChnLocked[3:0] - Status of phase selection logic for channels in group 4. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX4State[1:0] - State of initialization state machine for ePortRx group 4. State can be according to the table:

EPRX4State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x14f] EPRX4CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 4

Bit 7:4 - EPRX4CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 4

Bit 3:0 - EPRX4CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 4

[0x150] EPRX4CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 4

Bit 7:4 - EPRX4CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 4

Bit 3:0 - EPRX4CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 4

[0x151] EPRX5Locked

ePortRx group 5 status register

Bit 7:4 - EPRX5ChnLocked[3:0] - Status of phase selection logic for channels in group 5. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX5State[1:0] - State of initialization state machine for ePortRx group 5. State can be according to the table:

EPRX5State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x152] EPRX5CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 5

Bit 7:4 - EPRX5CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 5

Bit 3:0 - EPRX5CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 5

[0x153] EPRX5CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 5

Bit 7:4 - EPRX5CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 5

Bit 3:0 - EPRX5CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 5

[0x154] EPRX6Locked

ePortRx group 6 status register

Bit 7:4 - EPRX6ChnLocked[3:0] - Status of phase selection logic for channels in group 6. Bit 0 corresponds to channel 0, bit 1 to channel 1 and so on. Logic value of 1 means that the channel is locked.

Bit 1:0 - EPRX6State[1:0] - State of initialization state machine for ePortRx group 6. State can be according to the table:

EPRX6State[1:0] State

2'd0 Reset

2'd1 Force down

2'd2 Confirm early state

2'd3 Free running state

[0x155] EPRX6CurrentPhase10

Currently selected phases for channels 0 and 1 in ePortRx group 6

Bit 7:4 - EPRX6CurrentPhase1[3:0] - Currently selected phases for channels 1 in ePortRx group 6

Bit 3:0 - EPRX6CurrentPhase0[3:0] - Currently selected phases for channels 0 in ePortRx group 6

[0x156] EPRX6CurrentPhase32

Currently selected phases for channels 2 and 3 in ePortRx group 6

Bit 7:4 - EPRX6CurrentPhase3[3:0] - Currently selected phases for channels 3 in ePortRx group 6

Bit 3:0 - EPRX6CurrentPhase2[3:0] - Currently selected phases for channels 2 in ePortRx group 6

[0x157] EPRXEcCurrentPhase

Status register for ePortRxEc

Bit 3:0 - EPRXEcCurrentPhase[3:0] - Currently selected phase for EC channel phase aligner.

[0x158] EPRX0DllStatus

Status register of lock filter for ePortRxGroup0

Bit 7 - EPRX0DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX0DllLFState[1:0] - State of lock filter state machine

EPRX0DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX0DllLOLCnt[4:0] - Loss of Lock counter value

[0x159] EPRX1DllStatus

Status register of lock filter for ePortRxGroup1

Bit 7 - EPRX1DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX1DllLFState[1:0] - State of lock filter state machine

EPRX1DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX1DllLOLCnt[4:0] - Loss of Lock counter value

[0x15a] EPRX2DllStatus

Status register of lock filter for ePortRxGroup2

Bit 7 - EPRX2DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX2DllLFState[1:0] - State of lock filter state machine

EPRX2DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX2DllLOLCnt[4:0] - Loss of Lock counter value

[0x15b] EPRX3DllStatus

Status register of lock filter for ePortRxGroup3

Bit 7 - EPRX3DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX3DllLFState[1:0] - State of lock filter state machine

EPRX3DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX3DllLOLCnt[4:0] - Loss of Lock counter value

[0x15c] EPRX4DllStatus

Status register of lock filter for ePortRxGroup4

Bit 7 - EPRX4DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX4DllLFState[1:0] - State of lock filter state machine

EPRX4DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX4DllLOLCnt[4:0] - Loss of Lock counter value

[0x15d] EPRX5DllStatus

Status register of lock filter for ePortRxGroup5

Bit 7 - EPRX5DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX5DllLFState[1:0] - State of lock filter state machine

EPRX5DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX5DllLOLCnt[4:0] - Loss of Lock counter value

[0x15e] EPRX6DllStatus

Status register of lock filter for ePortRxGroup6

Bit 7 - EPRX6DllLocked - Lock status of the master DLL

Bit 6:5 - EPRX6DllLFState[1:0] - State of lock filter state machine

EPRX6DllLFState[1:0] Description

2'b00 Unlocked State

2'b01 Confirm Lock State

2'b10 Locked State

2'b11 Confirm Unlock State

Bit 4:0 - EPRX6DllLOLCnt[4:0] - Loss of Lock counter value

15.3.3. I2C Masters

[0x15f] I2CM0Ctrl

Contents of control register written by user for I2C Master 0

Bit 7:0 - I2CM0Ctrl[7:0] - Contents of control register written by user

[0x160] I2CM0Mask

Contents of mask register written by user for I2C Master 0

Bit 7:0 - I2CM0Mask[7:0] - Content of the status register.

[0x161] I2CM0Status

Contents of status register for I2C Master 0

Bit 7:0 - I2CM0Status[7:0] - Content of the status register.

[0x162] I2CM0TranCnt

Contents of transaction counter for I2C Master 0

Bit 7:0 - I2CM0TranCnt[7:0] - Content of transaction counter.

[0x163] I2CM0ReadByte

Data read from an I2C slave in a single-byte-read for I2C Master 0

Bit 7:0 - I2CM0ReadByte[7:0] - Data read from an I2C slave in a single-byte-read

[0x164] I2CM0Read0

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[7:0] - Data read from an I2C slave in a multi-byte-read

[0x165] I2CM0Read1

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[15:8] - Data read from an I2C slave in a multi-byte-read

[0x166] I2CM0Read2

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[23:16] - Data read from an I2C slave in a multi-byte-read

[0x167] I2CM0Read3

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[31:24] - Data read from an I2C slave in a multi-byte-read

[0x168] I2CM0Read4

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[39:32] - Data read from an I2C slave in a multi-byte-read

[0x169] I2CM0Read5

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[47:40] - Data read from an I2C slave in a multi-byte-read

[0x16a] I2CM0Read6

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[55:48] - Data read from an I2C slave in a multi-byte-read

[0x16b] I2CM0Read7

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[63:56] - Data read from an I2C slave in a multi-byte-read

[0x16c] I2CM0Read8

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[71:64] - Data read from an I2C slave in a multi-byte-read

[0x16d] I2CM0Read9

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[79:72] - Data read from an I2C slave in a multi-byte-read

[0x16e] I2CM0Read10

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[87:80] - Data read from an I2C slave in a multi-byte-read

[0x16f] I2CM0Read11

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[95:88] - Data read from an I2C slave in a multi-byte-read

[0x170] I2CM0Read12

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[103:96] - Data read from an I2C slave in a multi-byte-read

[0x171] I2CM0Read13

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[111:104] - Data read from an I2C slave in a multi-byte-read

[0x172] I2CM0Read14

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[119:112] - Data read from an I2C slave in a multi-byte-read

[0x173] I2CM0Read15

Data read from an I2C slave in a multi-byte-read by I2C Master 0

Bit 7:0 - I2CM0Read[127:120] - Data read from an I2C slave in a multi-byte-read

[0x174] I2CM1Ctrl

Contents of control register written by user for I2C Master 1

Bit 7:0 - I2CM1Ctrl[7:0] - Contents of control register written by user

[0x175] I2CM1Mask

Contents of mask register written by user for I2C Master 1

Bit 7:0 - I2CM1Mask[7:0] - Content of the status register.

[0x176] I2CM1Status

Contents of status register for I2C Master 1

Bit 7:0 - I2CM1Status[7:0] - Content of the status register.

[0x177] I2CM1TranCnt

Contents of transaction counter for I2C Master 1

Bit 7:0 - I2CM1TranCnt[7:0] - Content of transaction counter.

[0x178] I2CM1ReadByte

Data read from an I2C slave in a single-byte-read for I2C Master 1

Bit 7:0 - I2CM1ReadByte[7:0] - Data read from an I2C slave in a single-byte-read

[0x179] I2CM1Read0

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[7:0] - Data read from an I2C slave in a multi-byte-read

[0x17a] I2CM1Read1

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[15:8] - Data read from an I2C slave in a multi-byte-read

[0x17b] I2CM1Read2

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[23:16] - Data read from an I2C slave in a multi-byte-read

[0x17c] I2CM1Read3

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[31:24] - Data read from an I2C slave in a multi-byte-read

[0x17d] I2CM1Read4

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[39:32] - Data read from an I2C slave in a multi-byte-read

[0x17e] I2CM1Read5

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[47:40] - Data read from an I2C slave in a multi-byte-read

[0x17f] I2CM1Read6

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[55:48] - Data read from an I2C slave in a multi-byte-read

[0x180] I2CM1Read7

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[63:56] - Data read from an I2C slave in a multi-byte-read

[0x181] I2CM1Read8

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[71:64] - Data read from an I2C slave in a multi-byte-read

[0x182] I2CM1Read9

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[79:72] - Data read from an I2C slave in a multi-byte-read

[0x183] I2CM1Read10

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[87:80] - Data read from an I2C slave in a multi-byte-read

[0x184] I2CM1Read11

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[95:88] - Data read from an I2C slave in a multi-byte-read

[0x185] I2CM1Read12

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[103:96] - Data read from an I2C slave in a multi-byte-read

[0x186] I2CM1Read13

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[111:104] - Data read from an I2C slave in a multi-byte-read

[0x187] I2CM1Read14

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[119:112] - Data read from an I2C slave in a multi-byte-read

[0x188] I2CM1Read15

Data read from an I2C slave in a multi-byte-read by I2C Master 1

Bit 7:0 - I2CM1Read[127:120] - Data read from an I2C slave in a multi-byte-read

[0x189] I2CM2Ctrl

Contents of control register written by user for I2C Master 2

Bit 7:0 - I2CM2Ctrl[7:0] - Contents of control register written by user

[0x18a] I2CM2Mask

Contents of mask register written by user for I2C Master 2

Bit 7:0 - I2CM2Mask[7:0] - Content of the status register.

[0x18b] I2CM2Status

Contents of status register for I2C Master 2

Bit 7:0 - I2CM2Status[7:0] - Content of the status register.

[0x18c] I2CM2TranCnt

Contents of transaction counter for I2C Master 2

Bit 7:0 - I2CM2TranCnt[7:0] - Content of transaction counter.

[0x18d] I2CM2ReadByte

Data read from an I2C slave in a single-byte-read for I2C Master 2

Bit 7:0 - I2CM2ReadByte[7:0] - Data read from an I2C slave in a single-byte-read

[0x18e] I2CM2Read0

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[7:0] - Data read from an I2C slave in a multi-byte-read

[0x18f] I2CM2Read1

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[15:8] - Data read from an I2C slave in a multi-byte-read

[0x190] I2CM2Read2

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[23:16] - Data read from an I2C slave in a multi-byte-read

[0x191] I2CM2Read3

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[31:24] - Data read from an I2C slave in a multi-byte-read

[0x192] I2CM2Read4

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[39:32] - Data read from an I2C slave in a multi-byte-read

[0x193] I2CM2Read5

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[47:40] - Data read from an I2C slave in a multi-byte-read

[0x194] I2CM2Read6

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[55:48] - Data read from an I2C slave in a multi-byte-read

[0x195] I2CM2Read7

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[63:56] - Data read from an I2C slave in a multi-byte-read

[0x196] I2CM2Read8

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[71:64] - Data read from an I2C slave in a multi-byte-read

[0x197] I2CM2Read9

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[79:72] - Data read from an I2C slave in a multi-byte-read

[0x198] I2CM2Read10

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[87:80] - Data read from an I2C slave in a multi-byte-read

[0x199] I2CM2Read11

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[95:88] - Data read from an I2C slave in a multi-byte-read

[0x19a] I2CM2Read12

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[103:96] - Data read from an I2C slave in a multi-byte-read

[0x19b] I2CM2Read13

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[111:104] - Data read from an I2C slave in a multi-byte-read

[0x19c] I2CM2Read14

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[119:112] - Data read from an I2C slave in a multi-byte-read

[0x19d] I2CM2Read15

Data read from an I2C slave in a multi-byte-read by I2C Master 2

Bit 7:0 - I2CM2Read[127:120] - Data read from an I2C slave in a multi-byte-read

15.3.4. ECLK

[0x19e] PSStatus

Status of phase-shifter DLL initialization state machines

Bit 7:6 - PS3DllInitState[1:0] - Status of the DLL initialization state machine for phase-shifter channel 3

Bit 5:4 - PS2DllInitState[1:0] - Status of the DLL initialization state machine for phase-shifter channel 2

Bit 3:2 - PS1DllInitState[1:0] - Status of the DLL initialization state machine for phase-shifter channel 1

Bit 1:0 - PS0DllInitState[1:0] - Status of the DLL initialization state machine for phase-shifter channel 0

[0x19f] PIOInH

Allows read back of the PIO state

Bit 7:0 - PIOIn[15:8] -

PIOIn[n] Input signal level

1'b0 Low

1'b1 High

[0x1a0] PIOInL

Allows read back of the PIO state

Bit 7:0 - PIOIn[7:0] -

PIOIn[n] Input signal level

1'b0 Low

1'b1 High

[0x1a1] FUSEStatus

Status of fuse block.

Bit 3 - FuseBlowError - Error flag (attempt to blow fuses without magic number).

Bit 2 - FuseDataValid - Fuse read sequence was successful, SelectedFuseValues[31:0] is valid.

Bit 1 - FuseBlowDone - Fuse blowing sequence was successful.

Bit 0 - FuseBlowBusy - Fuse block is busy (either read or blowing sequence).

[0x1a2] FUSEValuesA

Value of selected FUSE block. (should be accessed only if FuseDataValid bit is set in [0x1a1] FUSEStatus register).

Bit 7:0 - SelectedFuseValues[7:0] - Bits 7:0 of the data word.

[0x1a3] FUSEValuesB

Value of selected FUSE block. (should be accessed only if FuseDataValid bit is set in [0x1a1] FUSEStatus register).

Bit 7:0 - SelectedFuseValues[15:8] - Bits 15:8 of the data word.

[0x1a4] FUSEValuesC

Value of selected FUSE block. (should be accessed only if FuseDataValid bit is set in [0x1a1] FUSEStatus register).

Bit 7:0 - SelectedFuseValues[23:16] - Bits 23:16 of the data word.

[0x1a5] FUSEValuesD

Value of selected FUSE block. (should be accessed only if FuseDataValid bit is set in [0x1a1] FUSEStatus register).

Bit 7:0 - SelectedFuseValues[31:24] - Bits 31:24 of the data word.

15.3.5. Process Monitor

[0x1a6] ProcessMonitorStatus

Process Monitor block status register.

Bit 1 - PMDone - Measurement done.

Bit 0 - PMBusy - Measurement in progress.

[0x1a7] PMFreqA

Process Monitor frequency measurement result.

Bit 7:0 - PMFreq[23:16] - Bits 23:16 of frequency measurement result.

[0x1a8] PMFreqB

Process Monitor frequency measurement result.

Bit 7:0 - PMFreq[15:8] - Bits 15:8 of frequency measurement result.

[0x1a9] PMFreqC

Process Monitor frequency measurement result.

Bit 7:0 - PMFreq[7:0] - Bits 7:0 of frequency measurement result.

15.3.6. SEU

[0x1aa] SEUCountH

Value of SEU counter.

Bit 7:0 - SEUCount[15:8] - Bits 15:8 of SEU counter.

[0x1ab] SEUCountL

Value of SEU counter.

Bit 7:0 - SEUCount[7:0] - Bits 7:0 of SEU counter.

15.3.7. Clock Generator

[0x1ac] CLKGStatus0

Bit 7:4 - CLKG\_PLL\_R\_CONFIG[3:0] - Selected PLL's filter resistance value [min:step:max] Ohm

Bit 3:0 - CLKG\_CONFIG\_I\_PLL[3:0] - Selected PLL's integral current [min:step:max] uA

[0x1ad] CLKGStatus1

Bit 7:4 - CLKG\_CONFIG\_I\_FLL[3:0] - Selected CDR's FLL current [min:step:max] uA

Bit 3:0 - CLKG\_CONFIG\_I\_CDR[3:0] - Selected CDR's integral current [min:step:max] uA

[0x1ae] CLKGStatus2

Bit 7:4 - CLKG\_CONFIG\_P\_FF\_CDR[3:0] - Selected CDR's proportional feedforward current [min:step:max] uA

Bit 3:0 - CLKG\_CONFIG\_P\_CDR[3:0] - Selected CDR's phase detector proportional current [min:step:max] uA

[0x1af] CLKGStatus3

Bit 7:0 - CLKG\_lfLossOfLockCount[7:0] - Lock filter loss of lock (increases when lock filter's state goes lfConfirmUnlockState -> lfUnLockedState); only in TX mode

[0x1b0] CLKGStatus4

Bit 7:4 - CLKG\_CONFIG\_P\_PLL[3:0] - Selected PLL's proportional current [min:step:max] uA

Bit 3:0 - CLKG\_BIASGEN\_CONFIG[3:0] - Selected bias DAC for the charge pumps [min:step:max] uA

[0x1b1] CLKGStatus5

Bit 7:0 - CLKG\_vcoCapSelect[8:1] - Selected vco capacitor bank (thermistor value)

[0x1b2] CLKGStatus6

Bit 7 - CLKG\_vcoCapSelect[0] - Selected vco capacitor bank (thermistor value)

Bit 6:5 - CLKG\_dataMuxCfg[1:0] - Selected data MUX loopback (test only)

CLKG\_dataMuxCfg[1:0] Description

2'd0 invalid state

2'd1 Equalizer output data loopback

2'd2 Data resampled by CDR loopback

2'd3 disabled

Bit 3:0 - CLKG\_vcoDAC[3:0] - Selected current DAC for the VCO [min:step:max] uA

[0x1b3] CLKGStatus7

Bit 7 - CLKG\_connectCDR - 0: CDR loop is disconnected from VCO; 1: CDR loop is connected to VCO;

Bit 6 - CLKG\_connectPLL - 0: PLL loop is disconnected from VCO; 1: PLL loop is connected to VCO;

Bit 5 - CLKG\_disDataCounterRef - 0: data/4 ripple counter is enabled; 1: disabled

Bit 4 - CLKG\_enableCDR - 0: Alexander PD UP/DOWN buffers + Alexander PD are disabled; 1: enabled

Bit 3 - CLKG\_enableFD - 0: PLL's FD + FD up/down signals are disabled; 1: enabled

Bit 2 - CLKG\_enablePLL - 0: PLL's PFD up/down signals are disabled; 1: enabled

Bit 1 - CLKG\_overrideVc - 0: The VCO's control voltage override is disabled; 1: enabled vcoControlVoltage is mid range

Bit 0 - CLKG\_refClkSel - 0: clkRef-> data counter; 1: clkRef->40MHz ref

[0x1b4] CLKGStatus8

Bit 7 - CLKG\_vcoRailMode - 0: voltage mode, 1: current mode

Bit 6 - CLKG\_ENABLE\_CDR\_R - 0: CDR's resistor is disconnected; 1: connected

Bit 5 - CLKG\_smLocked - ljCDR state machine locked flag

Bit 4 - CLKG\_lfInstLock - lock filter instant lock signal (only in TX mode)

Bit 3 - CLKG\_lfLocked - lock filter locked signal (only in TX mode)

Bit 2:0 - CLKG\_CONFIG\_FF\_CAP[2:0] - CDR's feed forward filter's capacitance

[0x1b5] CLKGStatus9

Bit 5:4 - CLKG\_lfState[1:0] - ljCDR's lock filter state machine

CLKG\_lfState[1:0] Value Description

lfUnLockedState 2'b00 low-pass lock filter is unlocked

lfConfirmLockState 2'b01 low-pass lock filter is confirming lock

lfLockedState 2'b10 low-pass lock filter is locked

lfConfirmUnlockState 2'b11 low-pass lock filter is confirming unlock

Bit 3:0 - CLKG\_smState[3:0] - ljCDR's state machine

CLKG\_smState[3:0] Value Description

smResetState 4'h0 reset state

smInit 4'h1 initialization state (1cycle)

smCapSearchStart 4'h2 start VCO calibration (jump to smPLLInit or smCDRInit when finished)

smCapSearchClearCounters0 4'h3 VCO calibration step; clear counters

smCapSearchClearCounters1 4'h4 VCO calibration step; clear counters

smCapSearchEnableCounter 4'h5 VCO calibration step; start counters

smCapSearchWaitFreqDecision 4'h6 VCO calibration step; wait for race end

smCapSearchVCOFaster 4'h7 VCO calibration step; VCO is faster than refClk, increase capBank

smCapSearchRefClkFaster 4'h8 VCO calibration step; refClk is faster than VCO, decrease capBank

smPLLInit 4'h9 PLL step; closing PLL loop and waiting for lock state

smCDRInit 4'hA CDR step; closing CDR loop and waiting for lock state

smPLLEnd 4'hB PLL step; PLL is locked

smCDREnd 4'hC CDR step; CDR is locked

15.3.8. FEC

[0x1b6] DLDPFecCorrectionCountH

Number of error reported by the FEC decoder in the downlink data path.

Bit 7:0 - DLDPFecCorrectionCount[15:8] - Bits 15:8 of the FEC correction counter.

[0x1b7] DLDPFecCorrectionCountL

Number of error reported by the FEC decoder in the downlink data path.

Bit 7:0 - DLDPFecCorrectionCount[7:0] - Bits 7:0 of the FEC correction counter.

15.3.9. ADC

[0x1b8] ADCStatusH

ADC status register

Bit 7 - ADCBusy - ADC core is performing conversion.

Bit 6 - ADCDone - ADC conversion is done. Result of conversion can be accessed in ADCValue

Bit 1:0 - ADCValue[9:8] - Result of the last conversion.

See also: [0x1b9] ADCStatusL

[0x1b9] ADCStatusL

ADC status register

Bit 7:0 - ADCValue[7:0] - Result of the last conversion.

See also: [0x1b8] ADCStatusH

15.3.10. Eye Opening Monitor

[0x1ba] EOMStatus

Bit 3:2 - EOMsmState[1:0] - EOM state machine

EOMsmState[1:0] Value Description

smIdle 2'b00 idle state

smResetCounters 2'b01 resets the EOM ripple counter

smCount 2'b10 EOM ripple counter is counting

smEndOfCount 2'b11 finished state; waiting for EOMStart to go down

Bit 1 - EOMBusy - Its hold high by the state machine when the ripple counter is in use

Bit 0 - EOMEnd - Its hold high when the counting is done. It is kept high until (EOMStart | EOMEnable) goes low

[0x1bb] EOMCouterValueH

Bit 7:0 - EOMcounterValue[15:8] - MSB word of EOM ripple counter (bigger the value, more the eye is open in this (x,y) position)

[0x1bc] EOMCouterValueL

Bit 7:0 - EOMcounterValue[7:0] - LSB word of EOM ripple counter (bigger the value, more the eye is open in this (x,y) position)

[0x1bd] EOMCounter40MH

Bit 7:0 - EOMCounter40M[15:8] - MSB word of EOM gating counter (toggles at 40 MHz); used to estimate number of data transitions

[0x1be] EOMCounter40ML

Bit 7:0 - EOMCounter40M[7:0] - LSB word of EOM gating counter (toggles at 40 MHz); used to estimate number of data transitions

15.3.11. BERT Tester

[0x1bf] BERTStatus

Status register of BERT checker.

Bit 2 - BERTPrbsErrorFlag - This flag is set when data input was always zero during the test.

Bit 1 - BERTBusy - Measurement is ongoing when this bit is asserted.

Bit 0 - BERTDone - Measurement is down when this bit is asserted.

[0x1c0] BERTResult4

BERT result.

Bit 7:0 - BERTErrorCount[39:32] - Bits 39:32 of BERT result.

[0x1c1] BERTResult3

BERT result.

Bit 7:0 - BERTErrorCount[31:24] - Bits 31:24 of BERT result.

[0x1c2] BERTResult2

BERT result.

Bit 7:0 - BERTErrorCount[23:16] - Bits 23:16 of BERT result.

[0x1c3] BERTResult1

BERT result.

Bit 7:0 - BERTErrorCount[15:8] - Bits 15:8 of BERT result.

[0x1c4] BERTResult0

BERT result.

Bit 7:0 - BERTErrorCount[7:0] - Bits 7:0 of BERT result.

15.3.12. ROM

[0x1c5] ROM

Register with fixed (non zero value). Can be used for testing purposes.

Bit 7:0 - ROMREG[7:0] - All read requests for this register should yield value 0xA5.

15.3.13. POR

[0x1c6] PORBOR

Status of POR and BOR instances

Bit 6 - PORC - State of PORC output

Bit 5 - PORB - State of PORB output

Bit 4 - PORA - State of PORA output

Bit 2 - BODC - State of BORC output

Bit 1 - BODB - State of BORB output

Bit 0 - BODA - State of BORA output

15.3.14. Power Up State Machine

[0x1c7] PUSMStatus

Status of power up state machine

Bit 4:0 - PUSMState[4:0] - Current state of the power up state machine

[0x1c8] PUSMActions

Status of power up state machine actions

Bit 5 - PUSMPllTimeoutAction - This flag is set if the PLL timeout action has be executed since the last chip reset.

Bit 4 - PUSMDllTimeoutAction - This flag is set if the DLL timeout action has be executed since the last chip reset.

Bit 3 - PUSMChannelsTimeoutAction - This flag is set if the wait for channels locked timeout action has be executed since the last chip reset.

Bit 2 - PUSMbrownoutAction - This flag is set if the brownout action has be executed since the last chip reset.

Bit 1 - PUSMPLLwatchdogAction - This flag is set if the PLL watchdog action has be executed since the last chip reset.

Bit 0 - PUSMDLLwatchdogAction - This flag is set if the DLL watchdog action has be executed since the last chip reset.

15.3.15. Debug

[0x1c9] TOValue

Test output read back

Bit 5:0 - TOVal[5:0] - Current value of all test outputs

[0x1ca] SCStatus

Serial interface (IC/EC) status register.

Bit 0 - SCParityValid - The last parity bit check result.

[0x1cb] FAState

State of the frame aligner state machine

Bit 3:0 - FAState[3:0] - State of the frame aligner state machine. TODO add the description.

[0x1cc] FACounter

Value of the counter in frame aligner.

Bit 7:0 - FACounter[7:0] - Interpretation of this field depends on the current state.

[0x1cd] ConfigErrorCounterH

Counter of SEU events in configuration memory.

Bit 7:0 - ConfigErrorCounter[15:8] - Bits 15:8 of the configuration memory SEU counter.

See also: [0x1ce] ConfigErrorCounterL

[0x1ce] ConfigErrorCounterL

Counter of SEU events in configuration memory.

Bit 7:0 - ConfigErrorCounter[7:0] - Bits 7:0 of the configuration memory SEU counter.

See also: [0x1cd] ConfigErrorCounterH