CSCE 312 Spring 2020 Project 2 Phase 1: In-Lab Exercises

Texas A&M University

February 14th, 2020

1 Phase 1: In-lab Exercises

1.1 Instructions

1. You are expected to work in groups of 4 at each table. All brainstorming discussions must be done as a team to promote collaborative thinking.

    (a) If you happen to be at a table with fewer than 4 people, you can choose to work with fewer people or let your TA's know to assist you in finding extra partner(s).

2. Download the collateral from Slack and use the skeletal files provided. **Do not change the name of the files**.

3. Add your full name and UIN to the introductory comment present in each .hdl file.

4. Complete the problem set provided in this document on your own sheet of paper. **Make sure your drawings are clear and handwriting is legible. Show your work**.

5. Implement the .hdl, .tst, and .cmp file for each chip. Keep these handy because you will use them and turn them in for Project 2 Phase 2.

1.2 Submission

1. **Submissions must be done individually**. Even though you are finding the solutions as a team, each of you is supposed to do the implementation individually, so we know you got the concepts.

2. Including your name and UIN, turn in your sheet of paper with the solutions to the problem set **by the end of the lab session**. Include your name and UIN.

3. In a zipped folder named `LastName_FirstName_UIN_Lab2.zip` turn in the .hdl, .tst, and .cmp files **before midnight on eCampus**.

1.3   Problem Set (30 Points)

1. (6 points) A **Half Adder** is characterized with two 1-bit data inputs a and b, a 1-bit data output sum, and a 1-bit carry output $carry$.

   (a) (½ point) Draw the interface block diagram (inputs and outputs) of the Half Adder.
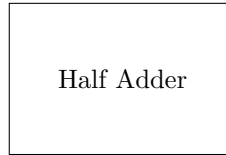
   Half Adder

   (b) (½ point) Complete the truth table for the Half Adder.

Inputs		Outputs	
a	b	carry	sum
0	0		
0	1		
1	0		
1	1		

   (c) (1 point) Write the logic expressions for outputs $carry$ and sum from the truth table above, then minimize them using Boolean Algebra.

   (d) (1 point) Draw logic gate diagrams to implement the minimized logic expressions for $carry$ and sum.

   (e) (3 points) Implement the .hdl, .tst, and .cmp files for the Half Adder chip.

2. (10 points) A **Full Adder** is characterized with two 1-bit data inputs a and b, a 1-bit carry input c, a 1-bit data output sum, and a 1-bit carry output $carry$.

(a) (½ point) Draw the interface block diagram (inputs and outputs) of the Full Adder.

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┌─────────────┐
│             │
│  Full Adder │
│             │
└─────────────┘
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(b) (1½ points) Complete the truth table for the Full Adder.

| Inputs			Outputs	
a	b	c	carry	sum
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(c) (2 points) Write the logic expressions for outputs $carry$ and sum from the truth table above, then minimize them using Boolean Algebra.

(d) (2 points) Draw logic gate diagrams to implement the minimized logic expressions for $carry$ and sum.
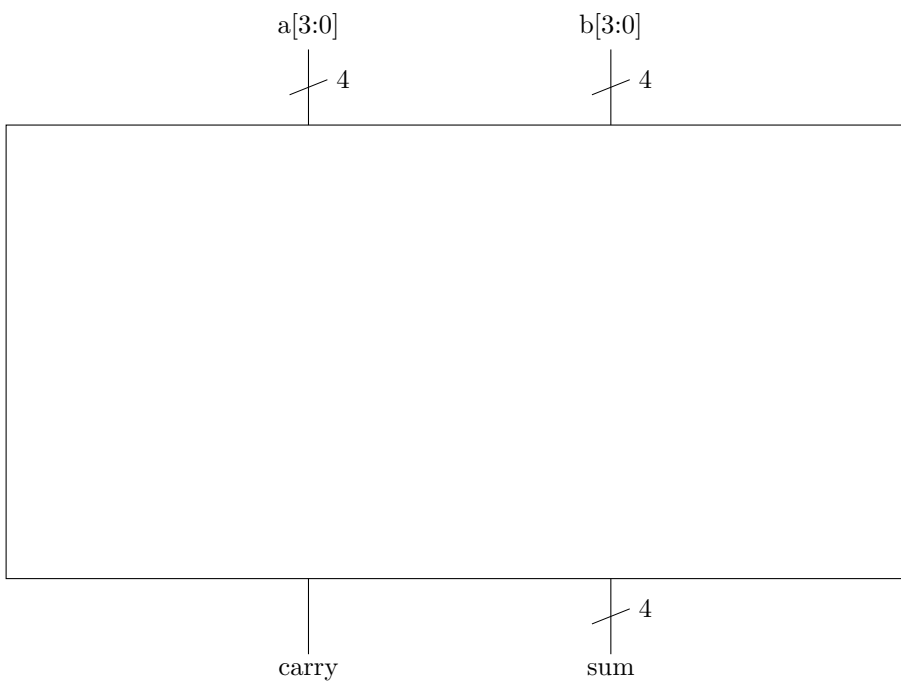
(e) (4 points) Implement the .hdl, .tst, and .cmp files for the Full Adder chip.

3. (12 points) A 4-bit ripple carry adder **Add4** is characterized by two 4-bit data inputs $a[3:0]$ and $b[3:0]$, a 4-bit data output $sum[3:0]$, and a 1-bit carry output $carry$.

(a) (4 points) Draw the inner logic block diagram of Add4 using one Half Adder and three Full Adders.

a[3:0]　　　　　　　　b[3:0]

4　　　　　　　　4

4

carry　　　　　　　　sum
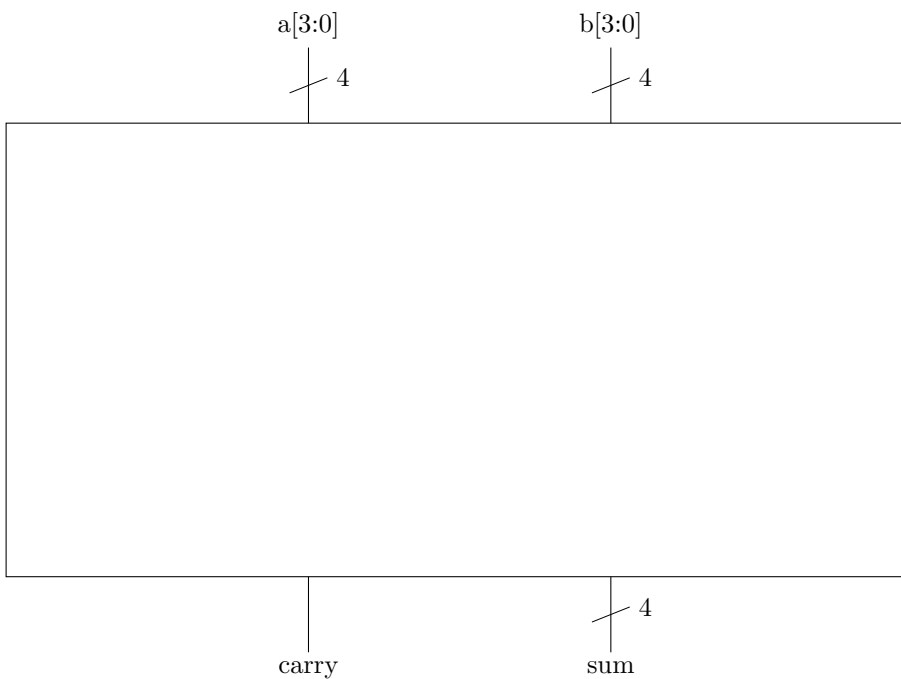
(b) (4 points) Draw the inner logic block diagram of Add4 using full adders only.

a[3:0]　　　　　　　　b[3:0]

4　　　　　　　　4

4

carry　　　　　　　　sum

(c) (4 points) Implement the .hdl, .tst, and .cmp files for the Add4 chip **using full adders only**.