CSCE 312 Spring 2020 Project 3 Phase 1: In-Lab Exercises

Texas A&M University

February 28th, 2020

1 Phase 1: In-lab Exercises

1.1 Instructions

1. You are expected to work in groups of 4 at each table. All brainstorming discussions must be done as a team to promote collaborative thinking.

    (a) If you happen to be at a table with fewer than 4 people, you can choose to work with fewer people or let your TA's know to assist you in finding extra partner(s).

2. Download the collateral from Slack and use the skeletal files provided. **Do not change the name of the files nor the names of the pins**.

3. Add your full name and UIN to the introductory comment present in each .hdl file.

4. Complete the problem set provided in this document on your own sheet of paper. **Make sure your drawings are clear and handwriting is legible. Show your work**.

5. Implement the .hdl file for each chip. Keep these handy because you will use some of them and turn them in for Project 3 Phase 2.

6. *The .tst and .cmp files are optional for today's assignment, but we recommend verifying the behavior of your chip as it will be graded based on correctness.*

1.2 Submission

1. **Submissions must be done individually**. Even though you are finding the solutions as a team, each of you is supposed to do the implementation individually, so we know you got the concepts.

2. Including your name and UIN, turn in your sheet of paper with the solutions to the problem set **by the end of the lab session**.

3. In a zipped folder named `LastName_FirstName_UIN_Lab3.zip` turn in the .hdl files **before midnight tonight on eCampus**.

1.3 Problem Set (30 Points)

1. (1 point) A **Data Flip Flop (DFF)** is characterized with one 1-bit data input *in*, one 1-bit data output *out*, and one 1-bit clock input *clk*. At clock cycle *t*, what is the output *out(t)*?

2. (7 points) A **Bit** is characterized with one 1-bit data input *in*, one 1-bit control signal *load*, one 1-bit clock signal *clk*, and one 1-bit output *out*.

   (a) (1 point) Draw the interface block diagram (inputs and outputs) of a Bit.

Bit
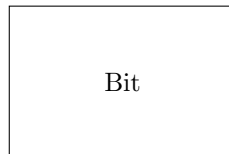
   (b) (1 point) Finish the conditional statements below describing the behavior of a Bit.

   If load(t) then: _____
   else _____

   (c) (2 points) Draw the logic gate diagram for a Bit using a DFF.

   (d) (3 points) Implement the .hdl file for the **Bit** chip.

3. (9 points) An **n-bit Register** is characterized with one n-bit data input *in*, one 1-bit control signal *load*, one 1-bit clock signal *clk*, and one n-bit data output *out*.

(a) (1 point) Draw the interface block diagram (inputs and outputs) of the multi-bit Register. Make sure you indicate the number of bits going through wires with more than 1 bit.

```
┌─────────────────────┐
│                     │
│    n-bit Register   │
│                     │
└─────────────────────┘
```

(b) (3 points) Draw a the logic gate diagram to implement a 4-bit register with one 4-bit input *in*, one 4-bit output *out*, one 1-bit control signal *load*, and one 1-bit clock signal *clk*.

(c) (5 points) Implement the .hdl file for the **16-bit Register** provided.

4. (13 points) A **16-bit RAM8** is characterized by one 16-bit data input *in*, one 3-bit control input *address*, one 1-bit control signal *load*, one 1-bit clock signal *clk*, and one 16-bit data output *out*.

   (a) (2 points) Draw the interface block diagram (inputs and outputs) of the 16-bit RAM8. Make sure you indicate the number of bits going through wires with more than 1 bit.
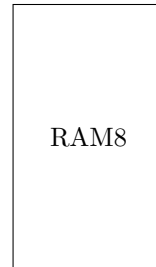
RAM8

   (b) (3 points) Draw the inner logic block diagram of the 16-bit RAM8.

load

16
in[15:0]

16
out[15:0]

3
addr[15:0]

clk
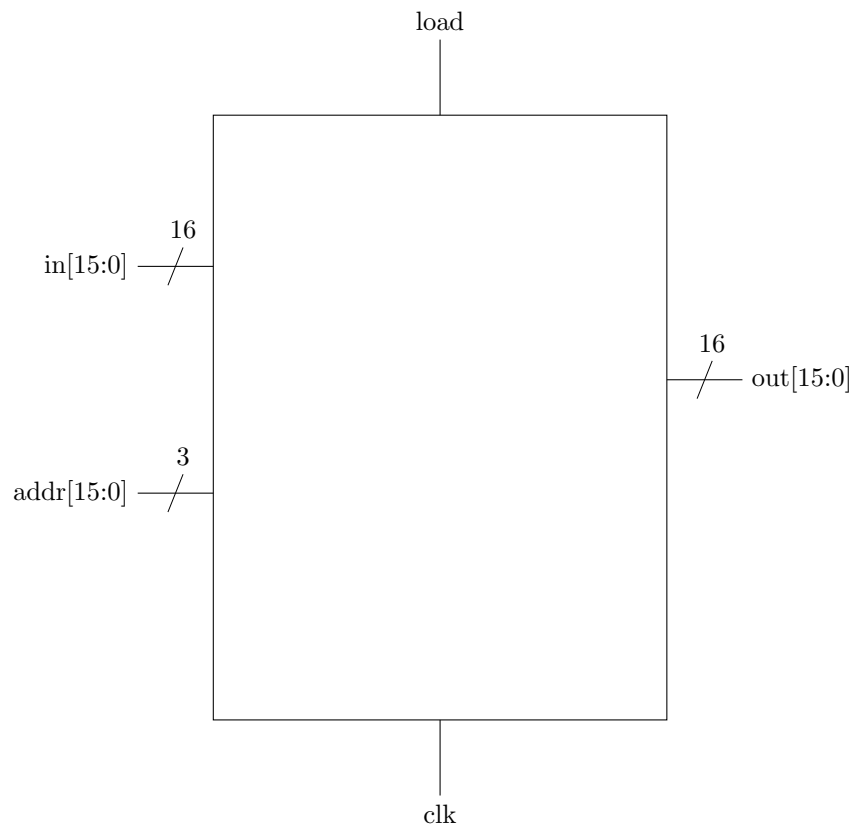
   (c) (8 points) Implement the .hdl file for the **16-bit RAM8** file provided.